External Project Report on Digital Logic Design (EET1211)

DIGITAL STOPWATCH

Submitted by

UPENDRA SINGH	Reg. No.: 2241019526
SIDDHANT SINGH	Reg. No.: 2241019517
SHASHANK SINGH	Reg. No.: 2241019513
SHRUTI SINGH	Reg. No.: 2241019515

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INSTITUTE OF TECHNICAL EDUCATION AND RESEARCH
(FACULTY OF ENGINEERING)
SIKSHA 'O' ANUSANDHAN (DEEMED TO BE UNIVERSITY), BHUBANESWAR, ODISHA

Declaration

We, the undersigned students of B. Tech. of **CSE** Department hereby declare that we own the full responsibility for the information, results etc. provided in this PROJECT titled **"DIGITAL STOPWATCH"** submitted to **Siksha 'O' Anusandhan Deemed to be University, Bhubaneswar** for the partial fulfillment of the subject **Digital Logic Design (EET 1211)**. We have taken care in all respect to honour the intellectual property right and have acknowledged the contribution of others for using them in academic purpose and further declare that in case of any violation of intellectual property right or copyright we, as the candidate(s), will be fully responsible for the same.

UPENDRA SINGH
Registration No.: 2241019526

SIDDHANT SINGH
Registration No.: 2241019517

SHASHANK SINGH
Registration No.: 2241019513

SHRUTI SINGH
Registration No.: 2241019515

DATE:

PLACE:

Abstract

Stopwatches find use as time keeping device in many fields, namely sports. Stopwatches may be analog or digital. Its function is to find out how long it takes in an activity. Digital stopwatches are much more common the analog version owing to their higher accuracy and ease of use. Here we have tried to realize a digital stopwatch of reasonable accuracy and reliability.

A digital stopwatch can be a circuit displaying the actual time in minutes, hours and seconds or a circuit displaying the number of clock pulses. Here we design the second type wherein the circuit displays count from 0 to 59, representing a 60 second time interval. In other words, here the circuit displays the time in seconds only. This is a simple circuit consisting of a 555 timer to produce the clock pulses and two counter ICs to carry out the counting operation.

The stopwatch logical design based on the two phases of the counting operation. It displays clock pulses count from 0 to 59 and representing a 60 second time interval. The first counter will count from 0 to 9, the second counter starts its counting when the count value of first reaches 9. The counter connected in cascading format and each counter output is connected to BCD to 7 segment decoders used to drive the 7 segment displays.

There are two seven segments, so this **stopwatch circuit** can count 00-99 seconds time.

Contents

1. Introduction

Stopwatches can be classified into two categories, Type I and Type II. In general, stopwatches are classified as Type I if they have a digital design employing quartz oscillators and electronic circuitry to measure time intervals (Figure 2). Type II stopwatches have an analog design and use mechanical mechanisms to measure time intervals.

DIGITAL STOPWATCH CIRCUIT PRINCIPLE:

The circuit is based on the principle of 2-stage counter operation, based on synchronous cascading. The idea is to display clock pulses count from 0 to 59, representing a 60-second time interval. This is done by using a 555 Timer IC connected in a stable mode to produce the clock pulses of 1-second intervals each. While the first counter counts from 0 to 9, the second counter starts its counting operation every time the count value of the first counter reaches 9. The counter ICs connected in cascading format and each counter output is connected to **BCD to 7 segment decoder** used to drive the 7-segment displays.

2. Problem Statement

This section explains the problem and working of the digital stopwatch.

CIRCUIT EXPLANATION:

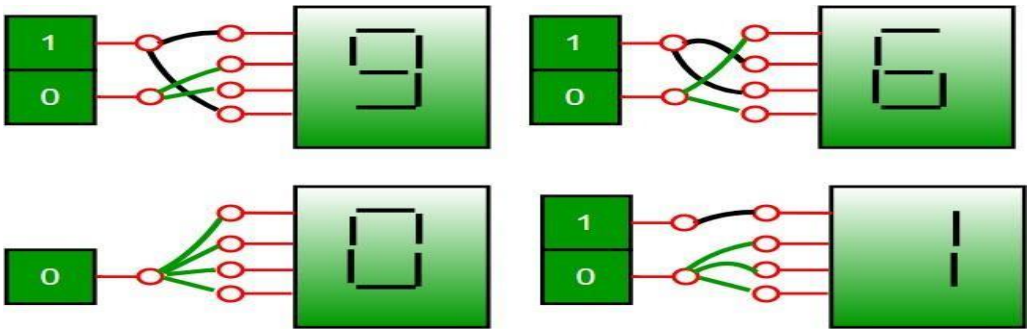
In the circuit we have used a 555 timer IC based astable multi-vibrator which is for creating 1 second delay. And two common cathode seven segment decoder IC's namely CD4033. The output of a stable multivibrator is directly applied to seven segment decoder IC's (U4) Clock pin (1) and carry output pin (5) of U4 IC is directly connected to clock pin (1) of second seven segment decoder(U3). And two seven segments are connected with these decoders (U3 and U4). Its connections are shown in stopwatch circuit diagram given below. One push button is used to stop /start the stopwatch and one push button is used to reset the stopwatch. A 5-volt voltage regulator is used for providing 5 volts to whole circuit. And a 9-volt battery is used for powering the circuit. Rest of connections are shown in the circuit diagram.

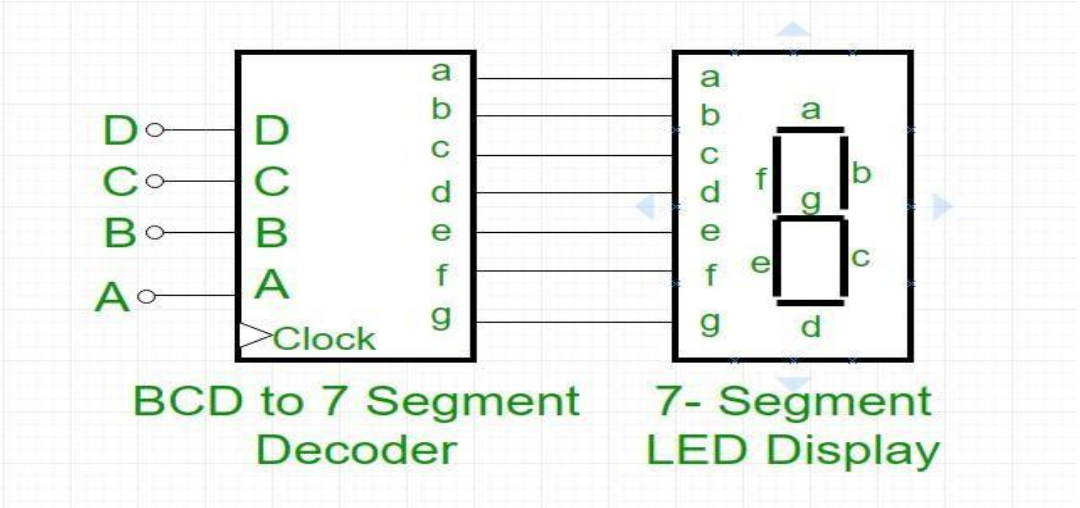
WORKING:

This specific stop watch is designed in such a way that it counts up to 99 seconds. Here we are using two 7 segment displays, two ICs 4026, a Seven Segment Display Decade counter and an IC 555 to feed the required pulse to the decade IC's.

The working of the stop watch starts with the 555 timer where it is wired as an A stable Multivibrator. We are using A-stable mode this means there will be no stable level at the output. So the output will be swinging between high and low. The time of pulse is set by setting the values of R1, R2 and capacitance. This character of unstable output is used as a clock or square wave output for the 4026 IC. At first, right side seven segment starts counting from 0 to 9, and then carry is shifted to another seven segment display, in this way it works as stop watch or counter from 0 to 99.

3. Methodology

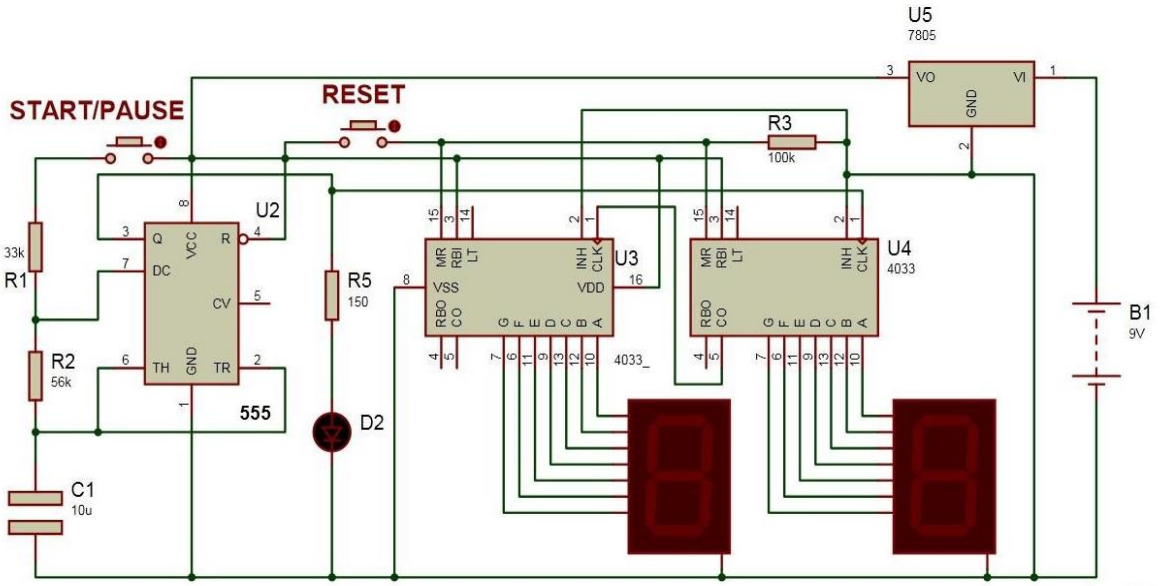


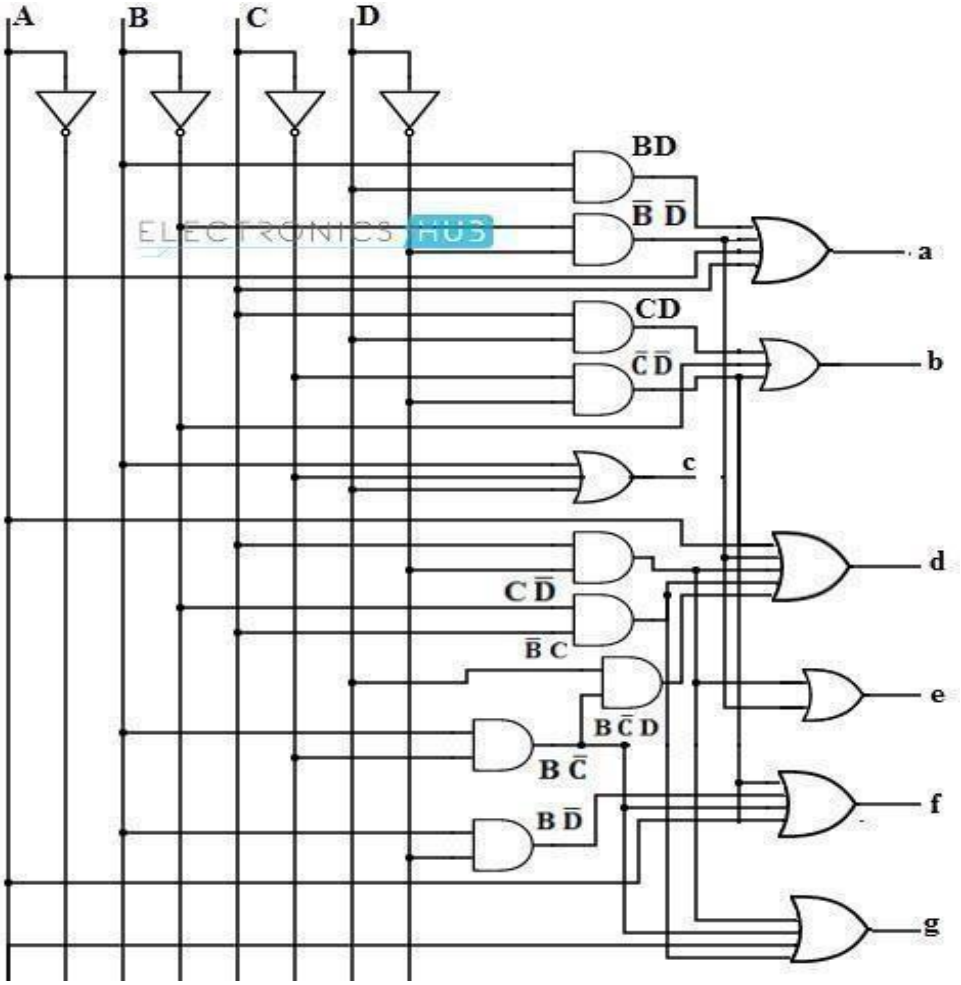


A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

4. Implementation

CIRCUIT DIAGRAM OF DIGITAL STOPWATCH





VHDL CODE

```
library IEEE;
use
IEEE.STD_LOGIC_1164.ALL;
use
ieee.std_logic_unsigned.all;
entity main is
   Port    (    start    :    in
        STD_LOGIC; stop : in
        STD_LOGIC; reset : in
        STD_LOGIC; clock : in
        STD_LOGIC;
output : out STD_LOGIC_VECTOR (7 downto 0));
end main;

architecture Behavioral of main
is constant clock_period : time :=
1 ms; --variable cnt : INTEGER :=
'0'; type state_type is (s0,s1,s2);
signal ps,ns : state_type:=s0;
signal   temp   :   std_logic_vector   (7   downto   0)   :=
"00000000"; begin
SEQ:process(clock)
begin if
(rising_edge(clock))
then
ps <= ns;
case ps is when
        s0 =>
             if (start = '1') then
                      temp    <=    temp    +
                      "00000001";  output  <=
                      temp; ns <= s1;
          end if; if (stop = '1') then
               output  <=  temp;  ns
               <= ps;
               end if; if (reset = '1')
               then     output     <=
               temp; ns <= ps;
```

```
                end if;
                    when  s1  =>
               if (start = '1') then
                        temp    <=    temp    +
                        "00000001";  output  <=
                        temp; ns <= ps;
                end if; if (stop = '1')
                then    output    <=
                temp;
                       ns <= s2;
                end if;
                if (reset = '1') then temp
                        <=   "00000000";
                        output  <=  temp;
                        ns <= s0;
                end if;
                        when s2 =>
               if (start = '1') then
                        temp    <=    temp    +
                        "00000001";  output  <=
                        temp; ns <= s1;
                end if; if (stop = '1')
                then    output    <=
                temp; ns <= ps;
                end  if;  if  (reset  =  '1')
                then        temp        <=
                "00000000"; output <=
                temp; ns <= s0;
                end if;
               when others =>
                        null;
        end case;
  end if;
end     process;

end

Behavioral;
```

5. Results & Interpretation

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0

6. Conclusion

We conclude that after completion of this digital stop watch project we have learnt some knowledge in designing the circuit and understood the coding process. The circuit has been implemented on Vivado.

After the competition of the project, we have analysed the following applications of the digital stopwatch:

1. Laboratory experiments

2. Sporting events

3. Competitions

Also, there are few limitations of the digital stopwatch:

- The circuit does not display the actual time, but rather the count of clock pulses.
- The use of digital counter ICs produces a time delay in the whole operation, because of the propagation delay.
- This is a theoretical circuit and may require changes.

References

1.) Kenneth .J. Ayala, The 8051 Micro-controller and its applications, prentice hall, new edition, 2006. about the microcontroller functioning‖

2.) www.circuitstoday.com basics of Seven segment display, transistor‖

3.) www.8051projects.info about 89S52 micro-controller‖

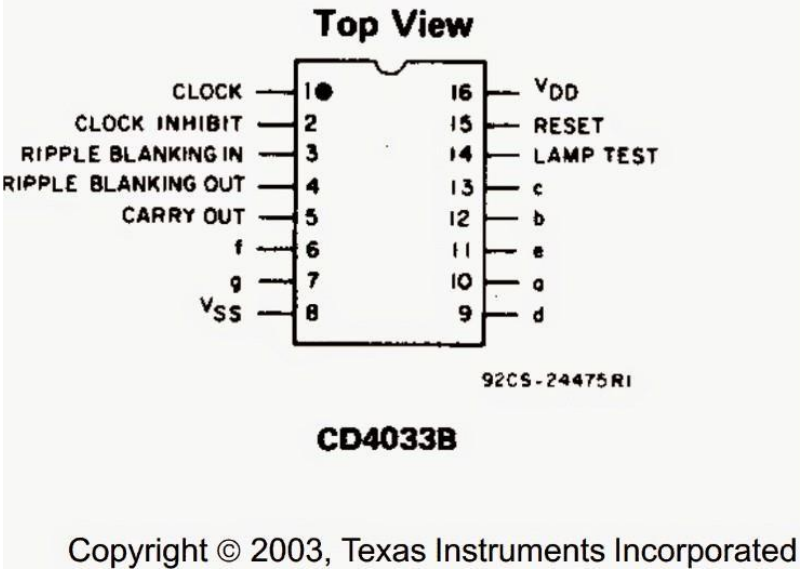
4.) Data-sheet's 434Mhz RF module Rx. Tx.

Appendices:

How IC 4033 Works

The IC 4033 is another Johnson decade counter/decoder IC specifically designed for working with 7 segment displays.

Basically, it's a clock or pulse counter IC which responds to positive pulses at its clock input and decodes it serially to produce a directly readable display of the count number through the connected 7 segment display module



Pin#1: It's the clock input pinout of the IC, which is assigned for accepting positive clock signals or the pulses which needs to be checked or counted.

Pin#2: It's the clock inhibit pinout of the IC, As the name refers to, this pinout could be used for inhibiting the IC from responding to the input pulses by configuring this pinout to the positive supply or the Vdd. Conversely in order to allow normal functioning of the IC this pinout should be grounded.

Pin#3/#4: These are the Ripple blanking IN and Ripple blanking OUT pinouts of the IC, which provides the user with the option of either allowing the non-significant zeros to be displayed or to be left out from the connected digital displays.

Pin#14: It's the "lamp test" pinout of the IC. As the name signifies it is used for testing the connected digital displays in terms of illumination level. When this pinout is connected to a high level or the positive supply, the normal function of the IC is disabled and all the digits of the 7 segment display are applied with a high state so that the digits are allowed to get illuminated together. This allows us to test the intensity levels of the digits and if any of the display digits are not functioning optimally or are dim due to some malfunction.

Pin#6,7,9,10,11,12,13: All these pin outs are the outputs of the IC which are configured with the discussed 7 segment digital display module.

Pin#15: It's the reset input of the IC, a high logic or applying the supply voltage to this pin resets the IC completely, resulting in clearing all the data from the display and restoring it to zero.

Pin#5: It's the carryout pin out of the IC, it sends a high logic output after every 10 legit clocks at the clock pin#1 of the IC. Thus pin#5 is used as a clock output or a carry forward extension for the next corresponding IC 4033 when many of these are cascaded together in a multi-digit display counter systems.

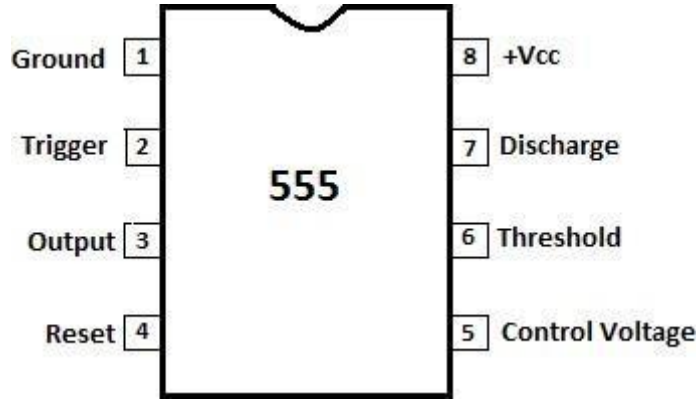
Pin#16 is the VDD or the supply input of the IC.

Pin#8 is the VSS, or the ground or the negative supply input pinout of the IC 4033.

The IC works best with supply voltages between 5V and 20V.

The 555 timer IC

is an integral part of electronics projects. Be a simple project involving a single 8-bit microcontroller and some peripherals or a complex one involving system on chips (SoCs), a 555 timer is involved. These provide time delays, as an oscillator and as a flip-flop element among other applications.



Pin#1 (GND) Ground reference voltage, low level (0 V)

Pin#2 (TRIG) The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 VCC, CTRL being 2/3 VCC by default if CTRL is left open). In other words, OUT is high as long as the trigger is low. The output of the timer totally depends upon the amplitude of the external trigger voltage applied to this pin.

Pin#3 (OUT) This output is driven to approximately 1.7V below +VCC, or to GND.

Pin#4 (RESET) A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides threshold.

Pin#5 (CTRL) Provides “control” access to the internal voltage divider (by default, 2/3 VCC).

Pin#6 (THR) The timing (OUT high) interval ends when the voltage at the threshold is greater than that at CTRL (2/3 VCC if CTRL is open).
Pin#7 (DIS) Open collector output which may discharge a capacitor between intervals. In phase with output.

Pin#8 (VCC) Positive supply voltage, which is usually between 3 and 15 V depending on the variation.