RSSI Amplifier Design for a Feature Extraction Technique to Detect Seizures with Analog Computing

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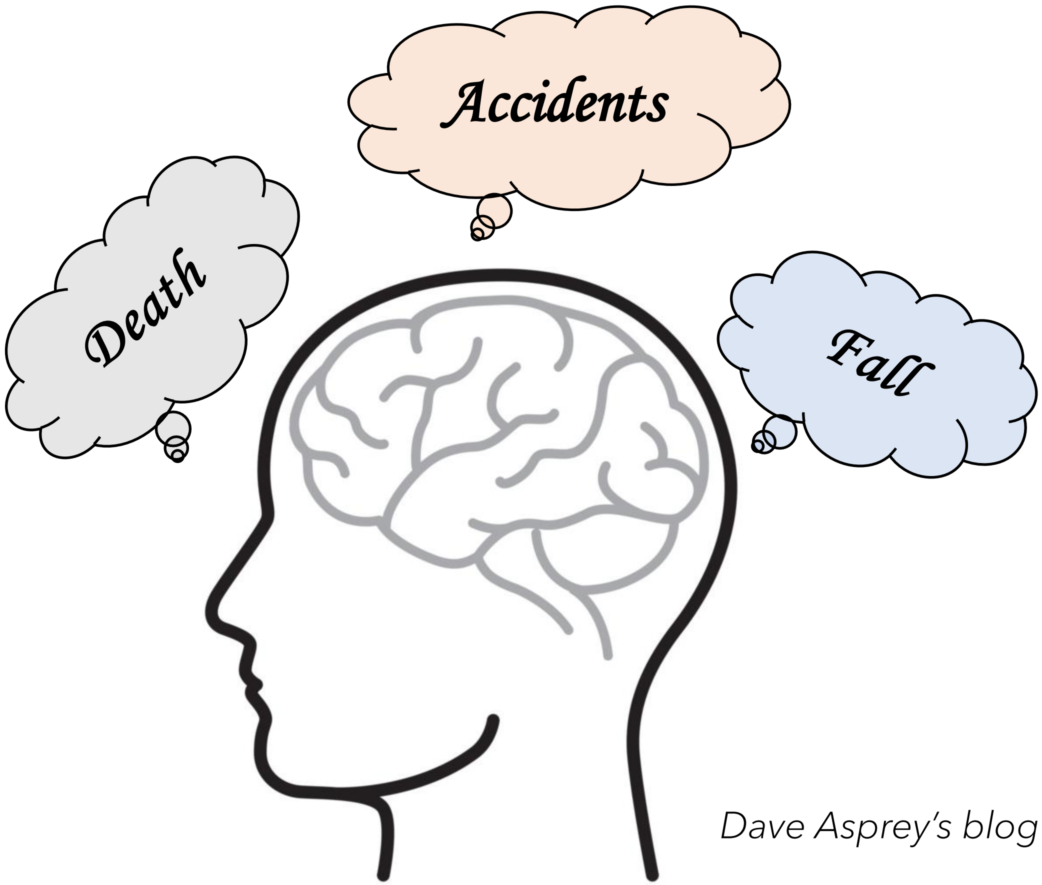
What is a Seizure?

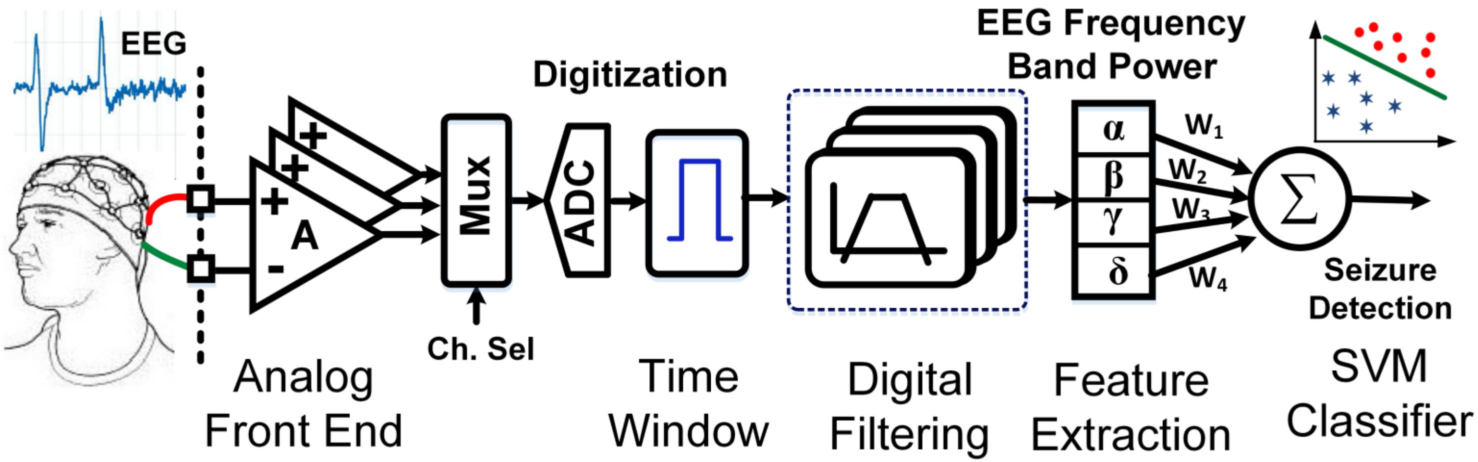


Dave Asprey's blog [1]

[1] https://blog.daveasprey.com/why-your-brain-is-nowhere-near-full-capacity-despite-what-cambridge-research-says/

Seizure Classification Methods

Conventional EEG Processing System



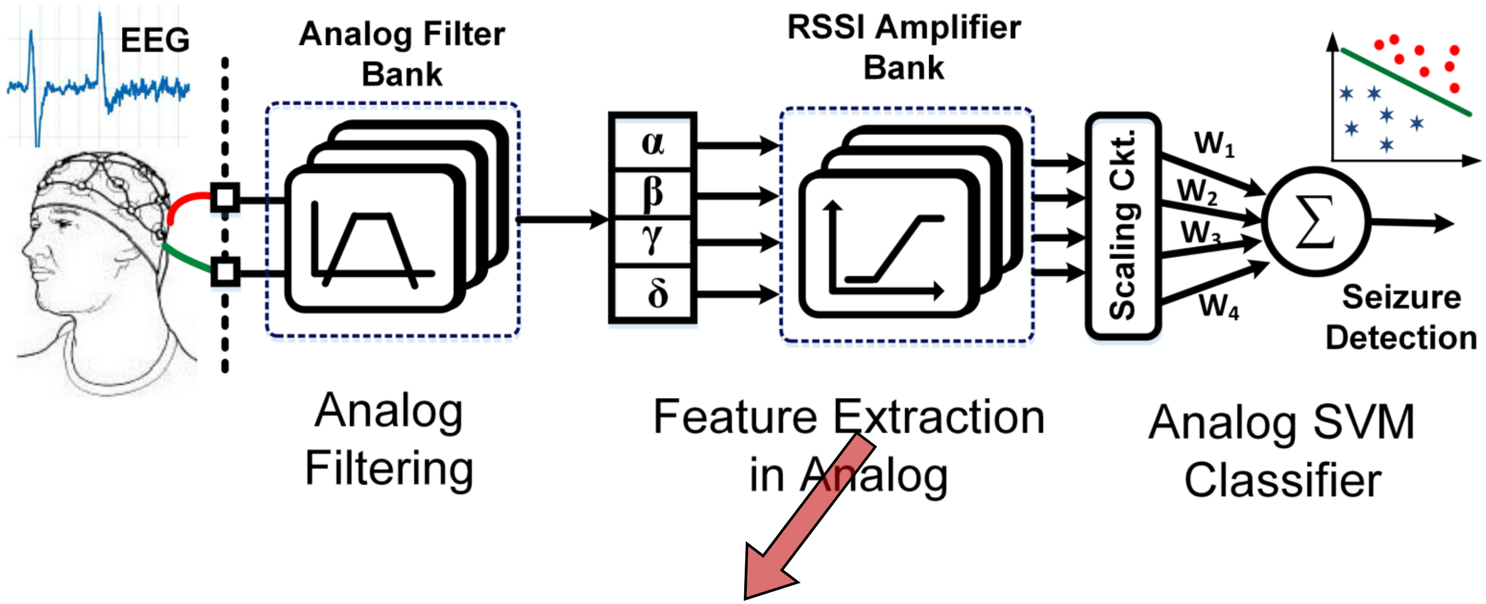
Consumes power in uW range

Chip sizes up to 5mm^2

M. A. B. Miyazaki and J. Yoo, ISCAS. IEEE-2013

Seizure Classification Methods

Proposed EEG Processing System

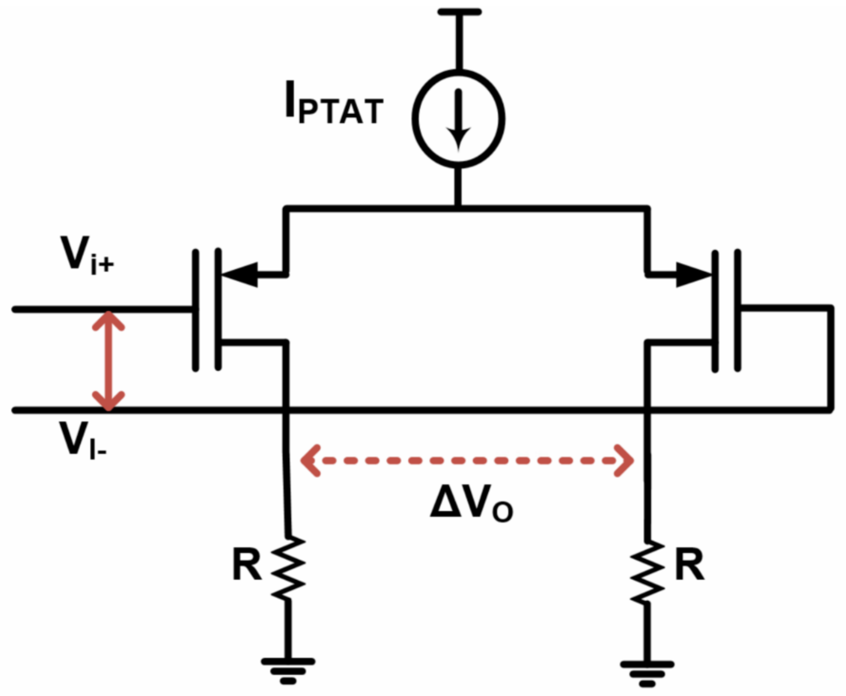


Six stage of limiting diff-amps are cascaded for required dynamic range

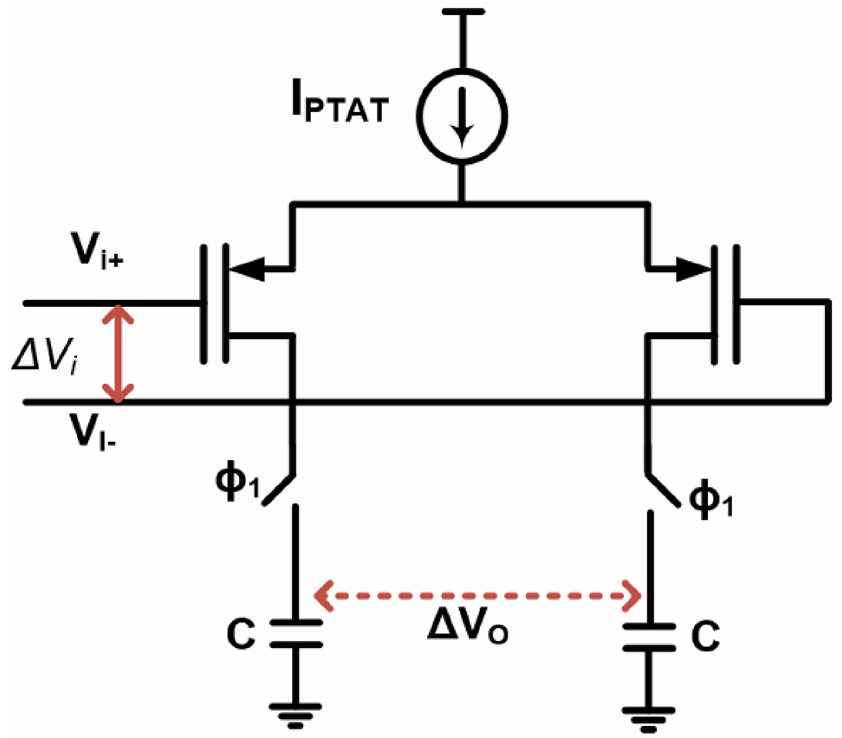
Outline of the Talk

- RSSI Amplifier
- PTAT Current Source
- Offset Correction
- RSSI Circuit Architecture
- Feature Extraction with RSSI Blocks
- Simulation Based Results
- Acknowledgement

Switched Capacitor RSSI Amplifier

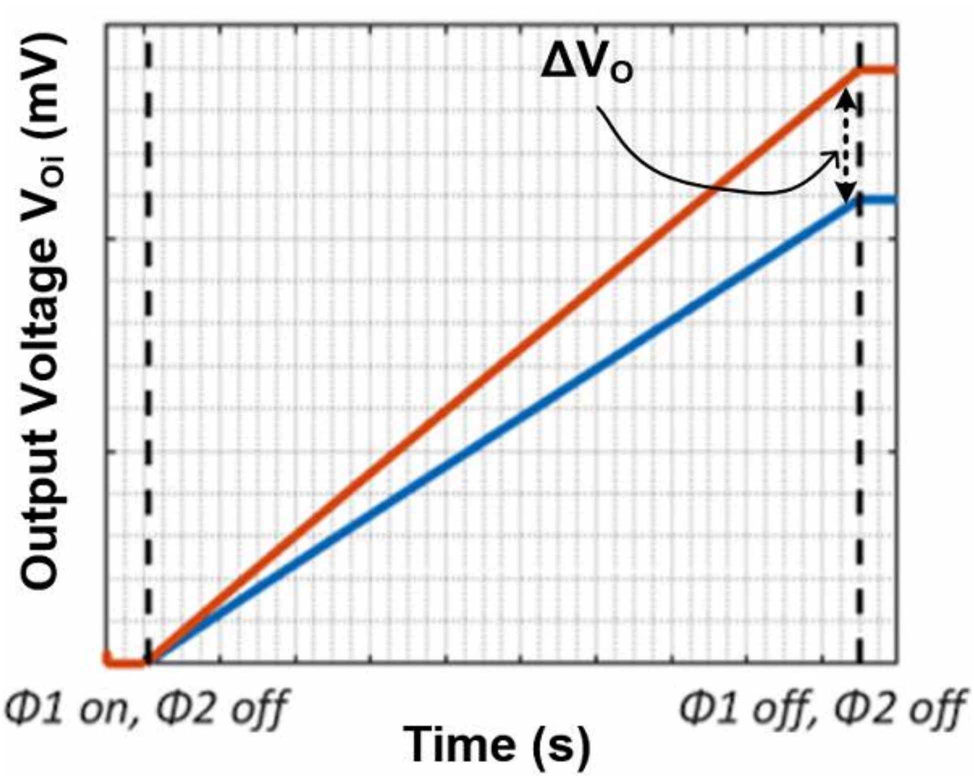


(a) RSSI Amplifier with Resistive Load



(b) RSSI Amplifier with Switched Capacitor Load

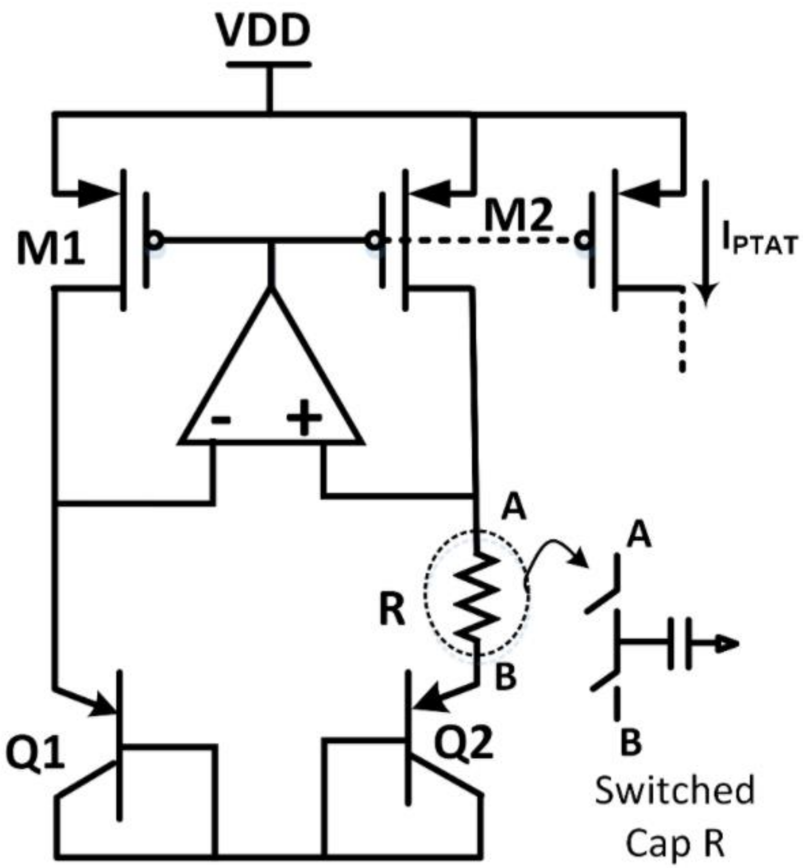
Switched Capacitor RSSI Amplifier

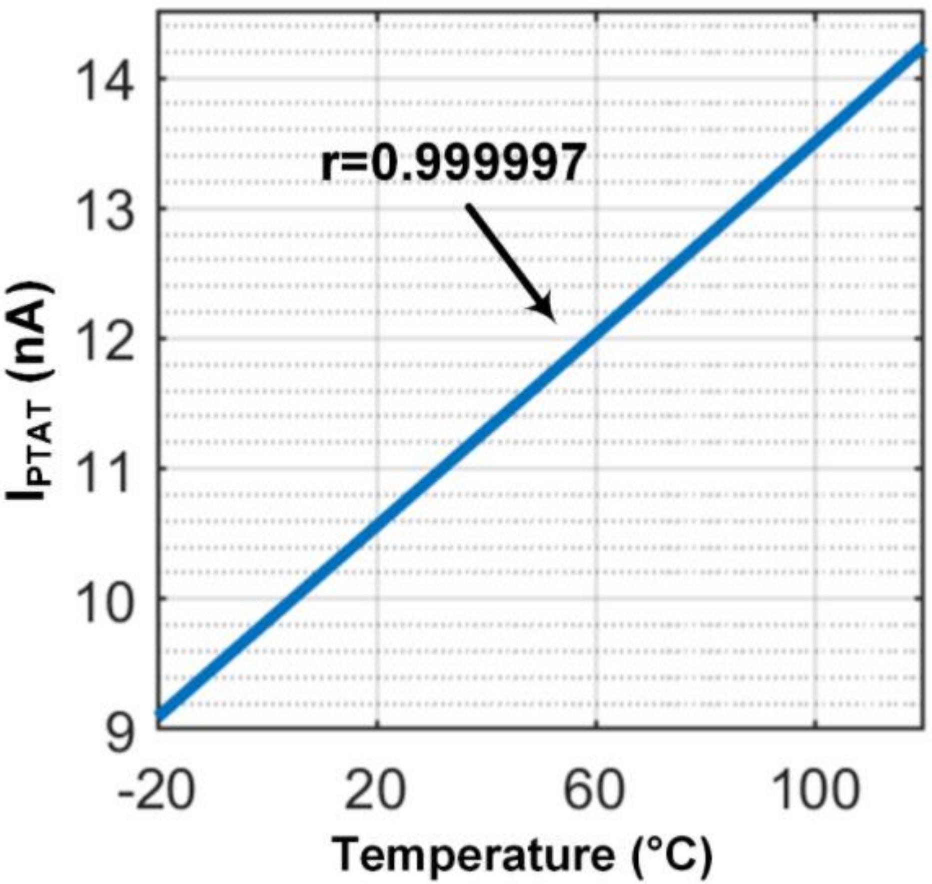


$$\Delta V_o = \Delta V_i \frac{g_m T_{ON}}{C} \qquad (1)$$

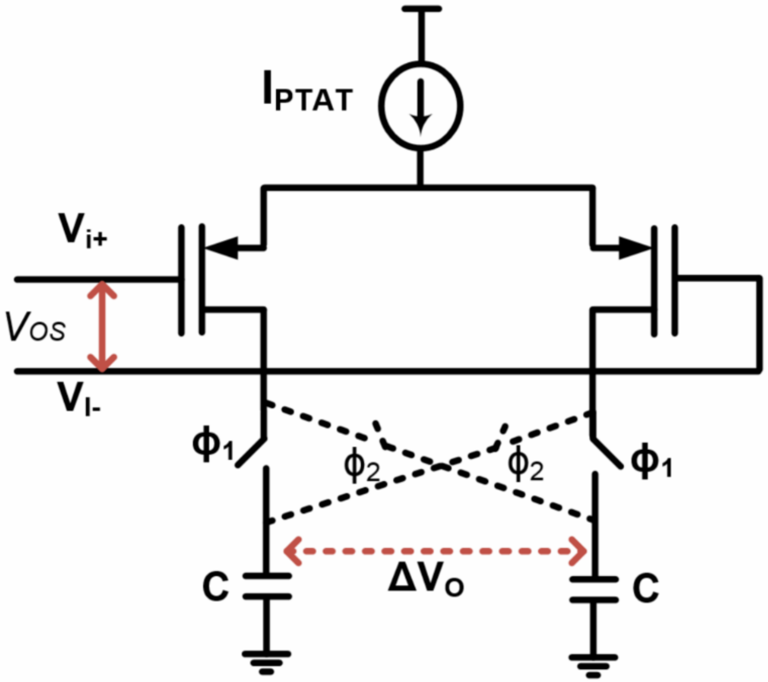
$$g_m = \frac{I_{PTAT}}{\eta V_t} \qquad (2)$$

PTAT Current Source

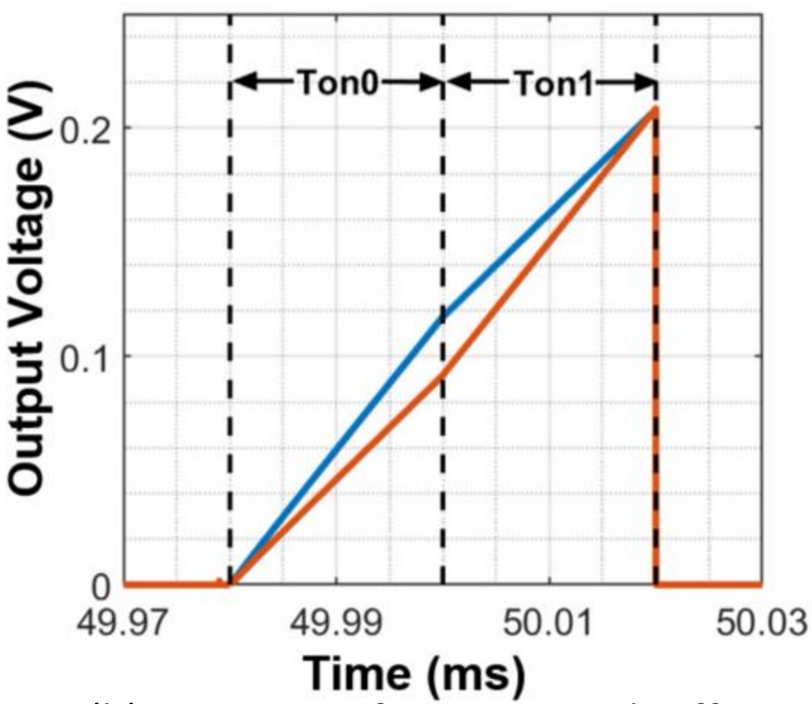




Offset Correction



(a) Offset correction structure



(b) Output performance with offset

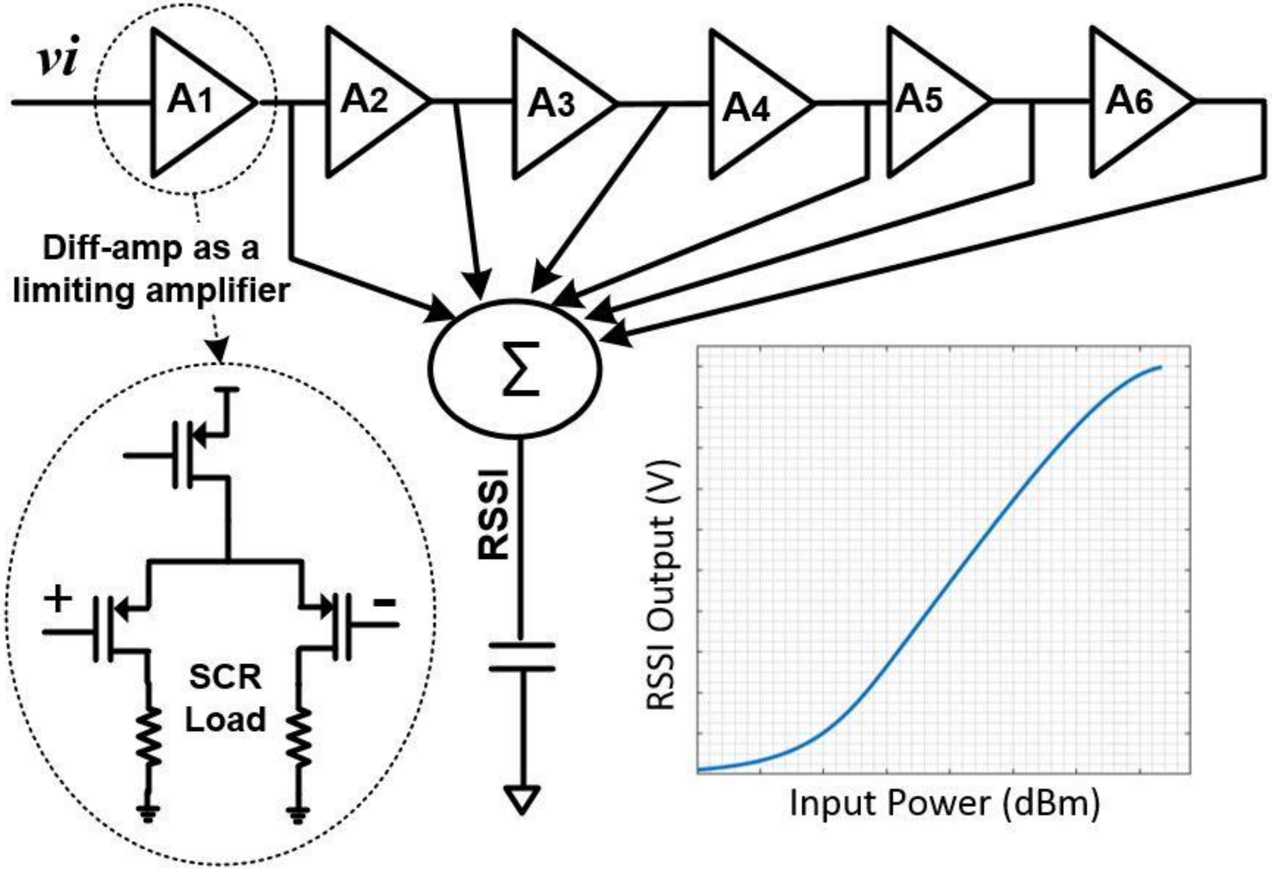
At the end of Φ_2: $\Delta V_O = \frac{g_m T_{ON}}{C} V_{OS}$ (3)

$+$ → 0

At the end of Φ_1: $\Delta V_O = \frac{g_m T_{ON}}{C} (-V_{OS})$ (4)

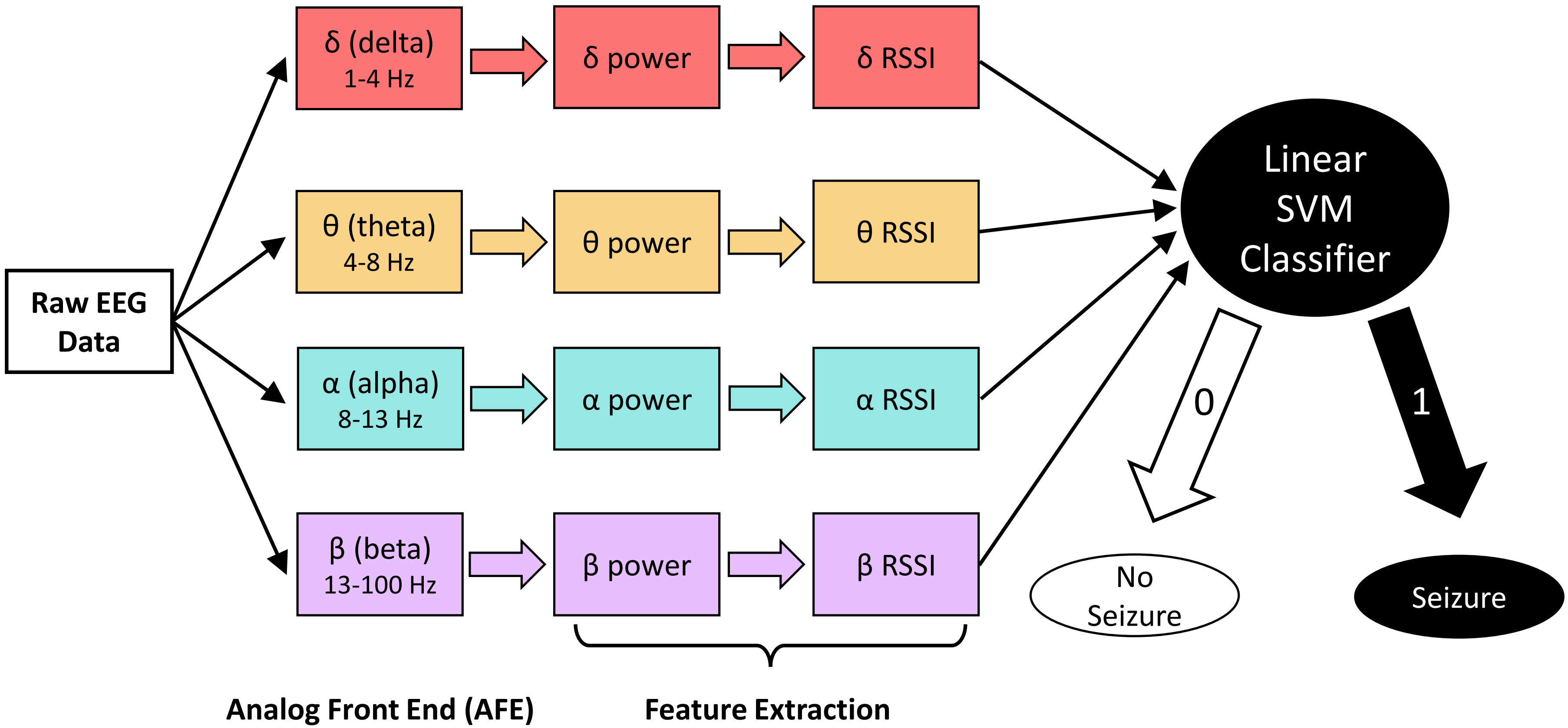
With 10mV offset, output voltage is reduced to 250µV

RSSI Circuit Architecture

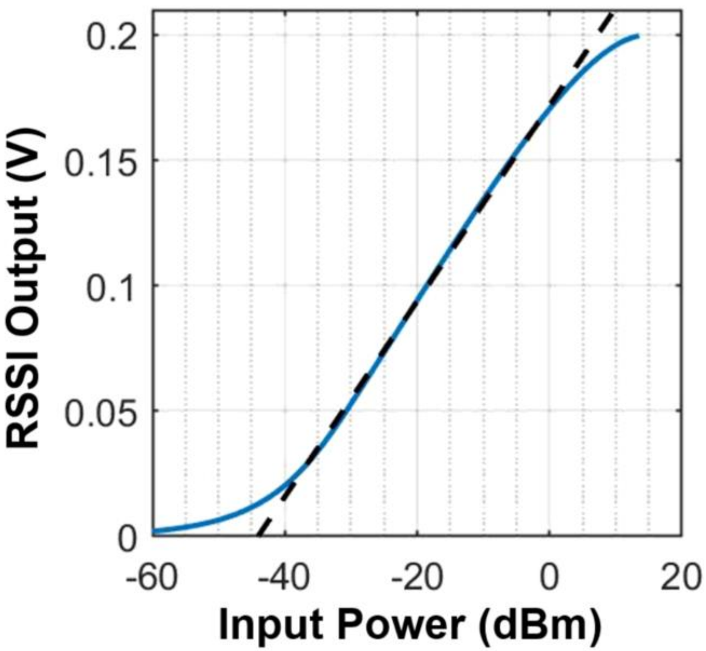


$$V_{RSSI} = \frac{1}{6}\sum_{\mathrm{i}=1}^{6} \Delta V_{Oi} \qquad (5)$$

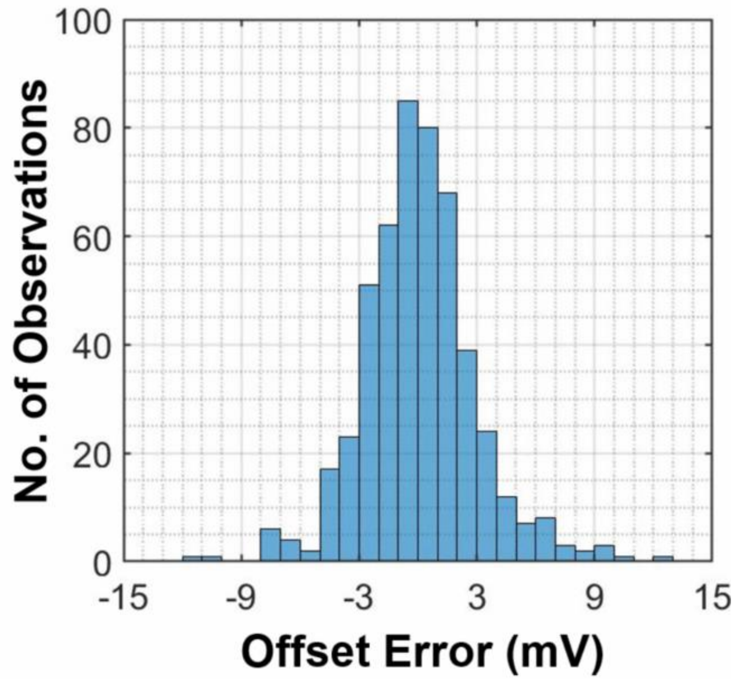
Feature Extraction with RSSI Blocks



Simulation Based Results



(a) RSSI Output and its Linearity Performance

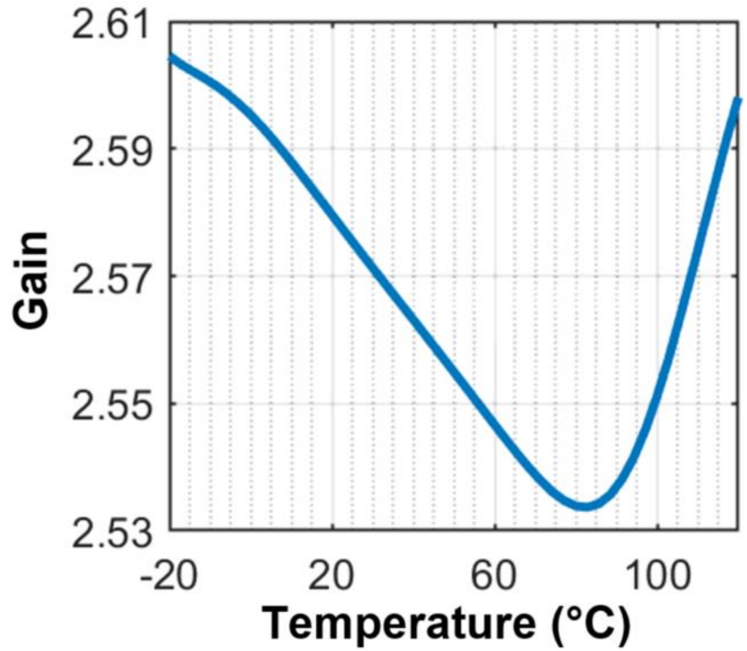


(b) Mismatch Simulation without Input

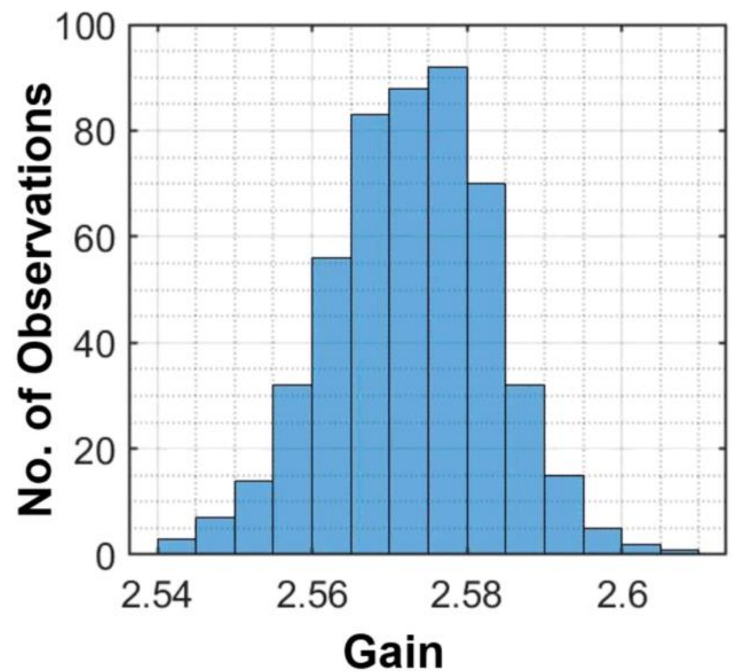
Dynamic range: 53dB
Linearity error: ± 0.5dB

Minimum detectable signal: 250uV
3σ of mismatch: 9mV

Simulation Based Results



(a) Gain Variation with Temperature



(b) Gain Variation with Process Simulation

Temperature variation of the gain: 2.88%

Average gain: 2.57

3σ variation: 0.033

Simulation Based Results

	This work	[3]	[4]	[5]
Process	65 nm	180 nm	600 nm	65 nm
VDD	1	1.8	2	1 or 3
Dynamic Range (dB)	53	70	75	60
Power	24 nW	20 mW	6.2 mW	8 mW
Linearity Error (dB)	± 0.5	≤ 1	≤ 1	≤ 1
Settling Time (us)	120	20	N/A	N/A

TABLE I: Performance Comparison

	This work	[6]	[7]	[8]	[9]
FE Power (uW/Channel)	0.096	0.48	100	7	33
% of Seizure Detected	95.74%	98.5%	84.4%	95.1%	96%
False Positive Rate	Almost 0	4.4/hour	4.5%	0.94%	0.15/hour
# of Channel Used	23	8	8	8	18

TABLE II: Feature Extraction Parameters

[3] S. Lee, Y. Song, and S. Nam, ISOCC. IEEE-2008
[4] Po-Chiun Huang, Yi-Huei Chen, and Chorng-Kuang Wang, JSSC. IEEE-2000
[5] J. Jang, J. Lee, K. Lee, J. Lee, M. Kim, Y. Lee, J. Bae, and H. Yoo, JSSC. IEEE-2018

[6] B. G. Do Valle, S. S. Cash, and C. G. Sodini , TBioCAS. IEEE-2016
[7] J. Yoo, L. Yan, D. El-Damak, M. A. B. Miyazaki, A. H. Shoeb, andA. P. Chandrakasan, JSSC. IEEE-2012
[8] M. A. Bin Miyazaki and J. Yoo, TVioCAS. IEEE-2016
[9] M. Shoaib, N. K. Jha, and N. Verma, CICC. IEEE-2012

Acknowledgement

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Thanks