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Two-Stage Differential Charge and Transresistance Amplifiers

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Abstract *– A novel approach to the design of high-performance differential charge and transresistance amplifiers is proposed. It is based on a two-stage topology: the first stage provides common-mode rejection and performs a differential to single-ended signal conversion; the second one filters the signal. From this technique, two novel topologies are presented, analyzed, and measured. Their performance are compared with that of a conventional topology used as benchmark and results in a better CMRR, that only depends on the matching between two resistors.*

Keywords *– Charge amplifier, charge to voltage converter, accelerometer, piezoelectric sensor, charge type sensor, transresistance amplifier, current to voltage converter, photodiode, current type sensor.*

I. INTRODUCTION

Charge amplifiers transform electrical charge into voltage by integration and are typically defined as transcapacitance circuits [1]-[2]. In data acquisition systems they are the first conditioning stage to process the information carried by a charge signal coming from a sensor, and to deliver it in a suitable form for further analog processing or digitalization. Desirable properties of charge amplifiers are: negligible input and output impedance effects, for optimum coupling with the sensor and the subsequent electronics; high sensitivity and low noise, to increase the signal-to-noise ratio (*SNR*).

It is noted that, since current is defined as the derivative of charge, the charge amplifiers topologies are of application with both charge and current sources (e.g.: piezoelectric accelerometers and photodiodes) by only some minor redesign. Anyway, when a current input is applied, the circuit is better named transresistor or current-to-voltage converter. In the paper this twofold application is taken into account, showing both charge amplifier and transresistor results and peculiarities.

The typical differential input signal of this kind of circuits can be represented by either a charge or current differential source, according to its physical nature. The useful part of the input signal is completely contained in its differential-mode (Q_D, I_D) and, in practice, it is always mixed with unwanted signals (e.g. *dc* offset, interference, or thermal noise) that essentially appear as common-mode. Since charge and current generating sensors are usually operated under virtual ground conditions (i.e. a zero voltage is forced between their terminals) these unwanted signals ideally only affect when they are in charge or current form (Q_C, I_C).

Technical literature is scarce in differential circuits for charge and current type sensors. Either the counterpart of the well-known three-op-amp instrumentation amplifier (figure 1a) or the simpler topology [3] (figure 1b) are almost the only available solutions, but they require at least two matching conditions between resistances and capacitors that, in practice, can be hard to fulfill. In an attempt to fill this gap, this paper describes a design technique from which two novel differential charge amplifiers based on a two-stage topology are obtained. It is showed that, with respect to the known circuits of figure 1, they only rely on the matching between two resistors and achieve a better common-mode rejection ratio (*CMRR*).

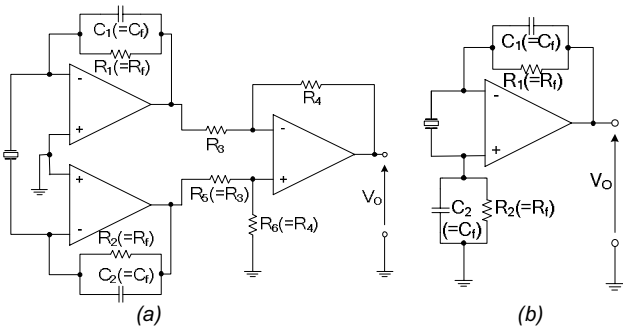


Figure 1. Conventional differential charge amplifier topologies: *(a)* three op-amp, *(b)* reference [3]. Table 1 shows their basic features.

II. THEORETICAL ANALYSIS

Differential circuits are described by two transfer functions [4]: G_D is the ratio between the output and the differential-mode input, with a null common-mode input; G_C is the ratio between the output and the common-mode input, with a null differential-mode input. Both parameters can refer to current or voltage output and to charge or current input, as the case may be. The *CMRR* is defined as the ratio G_D/G_C. Ideally, it is desirable to obtain $G_C=0$ (i.e. $CMRR=\infty$), but usually components mismatch make this limit unreachable, so that the real aim of the design is to obtain circuits that, for the desired G_D, yield the highest *CMRR*.

A first way to obtain a differential charge amplifier is given by the counterpart of the popular three-op-amp differential amplifier (figure 1a). It has been proposed for both photodiode [5]-[6] and charge sensors [7], and used with minor modifications in a number of applications [8]. For this circuit, table 1 shows the required matching conditions, its ideal transfer function, and sensitivity (1)-(5). Its *CMRR* relies on matching between resistors, capacitors, and even op-amps.

Table 1. Basic features of the conventional circuits of figure 1 and the proposed ones of figure 3. They are shown: the matching conditions required to obtain an ideally infinite *CMRR*; the ideal transfer functions and sensitivity with respect to both charge and current input signal.

Circuit	**Matching condition** (G_C=0, $CMRR$=∞)	**Transresistance amplifier** *(current type input)*		**Charge amplifier** *(charge type input)*	
		$G_D = V_O/I_D$	S_I	$G_D = V_O/Q_D$	S_Q
Figure 1a (three op-amp)	$R_1 = R_2 = R_f ; C_1 = C_2 = C_f$ $R_6/R_5 = R_4/R_3$ (1)	$\frac{2R_f}{1+sR_fC_f}\frac{R_4}{R_3}$ (2)	$2R_f\frac{R_4}{R_3}$ (3)	$\frac{2sR_f}{1+sR_fC_f}\frac{R_4}{R_3}$ (4)	$\frac{2}{C_f}\frac{R_4}{R_3}$ (5)
Figure 1b (reference [3])	$R_1 = R_2 = R_f$ $C_1 = C_2 = C_f$ (6)	$\frac{2R_f}{1+sR_fC_f}$ (7)	$2R_f$ (8)	$\frac{2sR_f}{1+sR_fC_f}$ (9)	$\frac{2}{C_f}$ (10)
Figure 3a	$R_1 = R_2 = R$ (11)	$\frac{2R}{R_3}\frac{R_f}{1+sR_fC_f}$ (12)	$\frac{2R}{R_3}R_f$ (13)	$\frac{2R}{R_3}\frac{sR_f}{1+sR_fC_f}$ (14)	$\frac{2R}{R_3}\frac{1}{C_f}$ (15)
Figure 3b	$R_1 = R; R_2 = R_a + R_b = R$ $\begin{cases} R_a = (1-a)R \\ R_b = aR \end{cases}$ $0 < a \le 1$ (16)	$\frac{2}{a}\frac{R_f}{1+sR_fC_f}$ (17)	$\frac{2}{a}R_f$ (18)	$\frac{2}{a}\frac{sR_f}{1+sR_fC_f}$ (19)	$\frac{2}{a}\frac{1}{C_f}$ (20)

A more compact solution (figure 1b) was proposed in a recent patent [3]. The basic characteristics reported in table 1 (6)-(10) permit to conclude that the circuit needs two matching conditions on resistors and capacitors to properly reject the common-mode input. With respect to the circuit in figure 1a, this alternative is very attractive because it requires less components and matching conditions, but it is unbalanced and has the disadvantage that the common-mode voltage of the sensor is signal-dependent and may induce some kind of non-linearity in the op-amp.

A close look at the two above presented circuits shows that their limitations are mainly due to the fact that the common-mode rejection and the integration are simultaneously accomplished by a pair of matched branches, which include capacitances in addition to resistances. However, the basic functions required to a differential charge amplifier (i.e. common-mode rejection, differential to single-ended signal conversion, charge-to-voltage signal conversion or integration, and amplification) can be also implemented in a different way. The proposed design technique of figure 2 suggests to split the basic functions into two independent stages: the first one converts the differential-mode input into a single-ended signal rejecting the common-mode input, while the second one performs an integration providing a single-ended output voltage. For the two stages to be independent, the output impedance of the first one and the input impedance of the second one have to be properly matched.

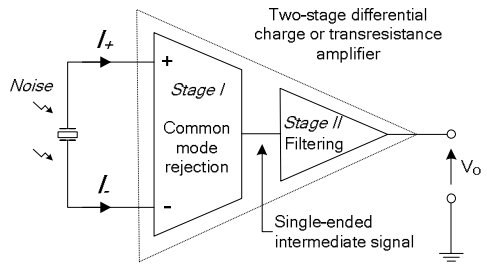


Figure 2. General approach proposed to implement two-stage differential charge and transresistance amplifiers. The first stage provides common-mode rejection and differential to single-ended signal conversion, the second one filters the resulting signal.

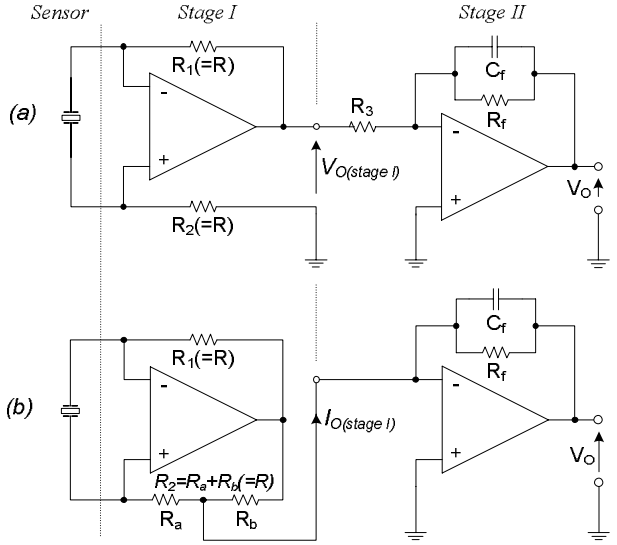


Figure 3. Two-stage differential charge amplifiers, proposed as *(a)* first, and *(b)* second implementation of the general approach depicted in figure 2. Table 1 shows their basic features.

The general approach here presented allows several alternative implementations. A first example is given by the circuit of figure 3a: its first stage, formerly proposed for photodiode applications [5], is derived from the typical difference amplifier, while the second stage is a standard lossy integrator. A second implementation is given by the circuit in figure 3b: its first stage is the so called improved Howland circuit [9], while the second one is a standard current integrator. This last circuit is an improvement of the one proposed in [10] by the authors: it provides additional gain by just adding the resistor R_a to the topology (for R_a=0Ω the circuit in [10] is obtained). The main difference between the circuits of figures 3a and 3b is in the first stage, which respectively yields an intermediate voltage or current mode signal.

Table 1 summarizes the basic features of all of the so far presented topologies: the matching conditions needed to obtain an infinite *CMRR*; the ideal transfer functions and sensitivities with respect to both charge and current inputs.

It is so clearer that the proposed circuits of figure 3 only need a single matching condition instead of the multiple ones required for the conventional circuits of figure 1. Moreover, the required matching is easier to achieve, because it does not involve capacitors that, especially in a discrete implementation, often have quite wide tolerance, resulting in a worse matching as compared to resistor.

The presented circuits can be also compared for their sensitivity, the sensor common-mode voltage rejection, and the complexity. The novel circuits of figure 3, in comparison to that of figure 1a, feature the same sensitivity with lower component count, their main drawback being the signal dependent common-mode voltage of the sensor. The same circuits, with respect to that of figure 1b, feature higher sensitivity, but at the expense of using additional components.

All the circuits of figures 1 and 3 can be used both as charge or transresistance amplifiers with only minor redesign. Table 1 and figure 4 illustrate the different frequency responses (G_D) and sensitivities (S_Q, S_I) obtained from the same topologies, but considering either charge or current as input. The charge amplifier has a high-pass response and its pole is usually placed at very low frequency to approximate an ideal integrator. The transresistance amplifier has a low-pass response and the pole only defines the passband. In the first case the sensitivity S_Q is mainly defined by the capacitance C_f that performs the charge-to-voltage conversion (the resistance R_f just sets the op-amp closed loop gain in *dc*), while in the second one the sensitivity S_I mainly depends on the resistance R_f that performs the current-to-voltage conversion (the capacitance C_f, if kept, only serves to limit the bandwidth).

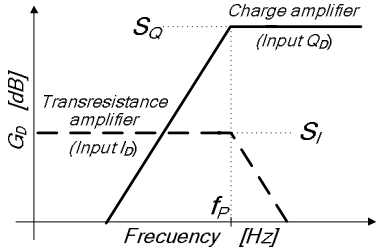


Figure 4. Typical high-pass and low-pass frequency responses of charge and transresistance amplifiers. The passband is defined by the dominant pole frequency f_P and the sensitivities by S_Q and S_I.

In the remainder of this paper the attention is focused on the novel circuits of figure 3, which are compared with that of figure 1b, chosen as benchmark. Besides the results just obtained, assuming ideal active and passive devices, other relevant effects such as mismatch, sensor parasitics, and op-amp limitations are also considered. Finally, the measurement results of the circuits are included and discussed.

A. Sensor Model

It is necessary to consider the nature of the typical sensors applied to the charge amplifiers. A suitable model for most practical purposes is shown in figure 5, where: R_S is the leakage resistance; C_S represents the capacitive nature; I_D is the generated differential-mode current that carries the information provided by the sensor according to the measured physical magnitude; I_C is the common-mode current, typically due to environmental interference. Because of the relationship between charge and current ($I(s)=sQ(s)$ in the s-domain) it is easy to swap between both equivalent sensor models of figure 5, allowing the study of the same circuit from different points of view.

The model applies for instance to piezoelectric sensors [11], where typically C_S is in the order of hundreds of pico farads and R_S is in the order of tens of mega ohms. Additionally, the sensor exhibits some kind of resonance, a typical characteristics of piezoelectric materials. It is most times avoided when the sensor is used as accelerometer or pressure sensor, or exploited such as for instance in ultrasonic receivers and transmitters. Thus, the resonance needs to be modeled when the overall transfer function from physical magnitude to voltage has to be predicted, but is not required in general to optimize the charge amplifiers.

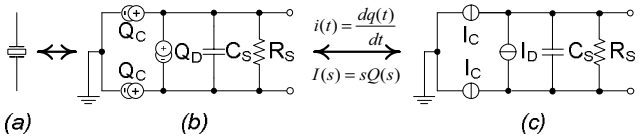


Figure 5. The typical sensor *(a)* used in conjunction with charge and transresistance amplifiers can be represented by its charge *(b)* or current *(c)* equivalent model, considering that $I(s)=sQ(s)$.

B. CMRR and Mismatch Analysis

The effects produced by the component mismatch on the *CMRR* are studied for the single-stage circuit of figure 1b, and for the two-stage circuits of figure 3 (in this case the *CMRR* only depends on their first-stage that performs a differential to single-ended signal conversion). Ideal op-amps and the source models of figure 5c are considered for all circuits.

For the circuit of figure 1b the output is given by,

$$V_O = \underbrace{-\frac{(R_1+R_2)+sR_1R_2(C_1+C_2)}{R_1R_2C_1C_2s^2+(R_1C_1+R_2C_2)s+1}}_{G_D} \cdot \left[I_D + \underbrace{\frac{(R_1-R_2)-sR_1R_2(C_1-C_2)}{(R_1+R_2)+sR_1R_2(C_1+C_2)}}_{1/CMRR} I_C \right] . \quad (21)$$

It clearly shows that a perfect common-mode rejection (*CMRR*=∞) requires the two matching conditions (6),

between resistances and capacitors. Applying (6) to (21), the ideal circuit response of table 1 (7)-(10) is obtained.

In practice, the matching conditions can only be approximated resulting in a finite *CMRR*. Considering component tolerances in the worst-case situation, given e.g. by $R_1=R_f(1+t_R)$, $R_2=R_f(1-t_R)$, $C_1=C_f(1+t_C)$, and $C_2=C_f(1-t_C)$, the minimum *CMRR* is given by,

$$CMRR_{\min} = \frac{1 - sR_fC_f\left(t_R{}^2 - 1\right)}{t_R + sR_fC_f\left(t_R{}^2 - 1\right)t_C}$$
$$\begin{cases} s_{POLE} = -\left(t_R/t_C\right)\Big/\left[R_fC_f\left(t_R{}^2-1\right)\right] \\ s_{ZERO} = 1\Big/\left[R_fC_f\left(t_R{}^2-1\right)\right] \end{cases}; \quad (22)$$

being: R_f and C_f the ideal component values; t_R and t_C the component tolerances (e.g. $t_R = 0.01$ for *1%* resistor). It is noted from (22) that in *dc* (i.e. $s=0$) the $CMRR_{min}$ is $1/t_R$, while at higher frequencies it is $-1/t_C$. This means that $|CMRR_{min}|$ is determined by resistance mismatch at low frequency and by capacitor mismatch at the higher ones. At intermediate frequencies it may exhibit three different behaviors depending on the ratio t_R/t_C that determines the relative position of its pole and zero. For a discrete realization the condition $t_C>t_R$ can be typically assumed, so that $|CMRR_{min}|$ decreases with frequency.

The matching between the resistors is the most critical one because, in general, it is very important to reject the common-mode input low frequency components that often have the highest power levels.

For the first stage of the circuit in figure 3a the output is given by,

$$V_{O(Stage\,1)} = \underbrace{-\left(R_1+R_2\right)}_{G_D}\left(I_D + \underbrace{\frac{R_1-R_2}{R_1+R_2}}_{1/CMRR} I_C\right). \quad (23)$$

So, assuming the matching condition (11) in table 1, the ideal behavior is given by: $G_D=V_{O(StageI)}/I_D=-2R$ and $CMRR=\infty$.

In practice, the theoretically infinite *CMRR* is limited by the resistance tolerances that yield mismatch. Substituting the worst-case conditions $R_1=R(1+t_R)$ and $R_2=R(1-t_R)$ into (23), the minimum *CMRR* is obtained as given by,

$$CMRR_{\min} = 1/t_R\,. \quad (24)$$

$|CMRR_{min}|$ is inversely proportional to t_R, the resistors tolerance: e.g., it is *40dB* and *60dB* for *1%* and *1‰* resistors respectively. So, high precision resistors are required to optimize the *CMRR*. It is also noted that to obtain a high *CMRR* only $R_1=R_2=R$ is required, but it is irrelevant how the resistances values differ from the ideal value *R*. If, e.g. $R_1=R_2=R(1+t_R)$, the gain corresponding to G_D is $-2R(1+t_R)$ instead of the ideal value $-2R$, but still $CMRR=\infty$.

For the first stage of the circuit in figure 3b the output current is given by,

$$I_{O(Stage\,1)} = \underbrace{-\frac{R_1+(R_a+R_b)}{R_b}}_{G_D}\left[I_D + \underbrace{\frac{R_1-(R_a+R_b)}{R_1+(R_a+R_b)}}_{1/CMRR} I_C\right]. \quad (25)$$

So, considering the matching condition (16) in table 1, its ideal behavior results in: $G_D=I_{O(StageI)}/I_D=-2/a$, $CMRR=\infty$. It is noted that G_D only depends on the parameter named *a*.

In practice, this ideal response is affected by resistors mismatch. The mismatch analysis is identical to that described in the previous section, by simply considering that the resistances to be matched are now R_1 and $R_2=R_a+R_b$. So, $CMRR_{min}$ results again as given by (24).

III. EXPERIMENTAL MEASUREMENTS

In order to verify the theoretical predictions and lead to more definite conclusions, the proposed (figure 3) and reference (figure 1b) circuits are measured and compared.

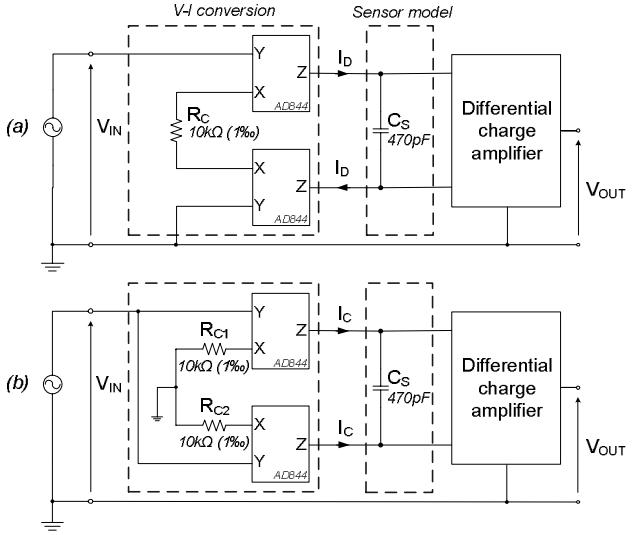


Figure 6. The measurement system used to test the transfer functions *(a)* G_D, and *(b)* G_C. It is composed by: the test signal generation block, which generates a *(a)* differential or *(b)* common mode current; the sensor capacitance; and the circuit under test.

The experimental set ups used to measure G_D (figure 6a) and G_C (figure 6b) consist of a voltage signal generator, a voltage-to-current converter, and the circuit under test. Depending on whether G_D or G_C is measured, a differential or common mode current is applied to the circuit. The *CMRR* is indirectly obtained by G_D/G_C.

The voltage-to-current conversion is obtained by the current conveyors *AD844* and the resistances $R_C=10k\Omega$ (*1‰*). The voltage V_{IN} applied to the Y-input is copied to

the X-input and results, by the (trans)resistance R_C, in a current that flows through the same input and is copied to the high-impedance output Z, yielding the output current I_{OUT}. The resulting transfer function is: $I_{OUT}/V_{IN}=1/R_C$. In figure 6a R_C is shared to obtain the needed differential current avoiding matching requirements. In figure 6b R_{C1} and R_{C2} are matched to obtain identical output currents as required. In both cases, the circuits exhibit a passband of about *1MHz* with a resistive load of $10k\Omega$ (wider for lower loads).

The measurements are obtained by the vector signal analyzer *HP89410A* that provides the frequency response of the whole system. Up to *1MHz* the entire system response is given by: $V_{OUT}/V_{IN}=TF/R_C$, being *TF* the unknown response. So, *TF* is obtained attenuated by R_C (for $R_C=10k\Omega$ the attenuation is *80dB*).

In order to make a fair comparison, all the tested circuits are designed with the same performance: a pole frequency $f_P=79.6Hz$; a charge and current sensitivities $S_Q=2\cdot10^9 V/C$ (*186dB*) and $S_I=4\cdot10^6 V/A$ (*132dB*). So, the benchmark circuit of figure 1b was built by: $R_1=R_2=R=2M\Omega$, $C_1=C_2=C=1nF$. The circuit of figure 3a was built by: $R_1=R_2=R=10k\Omega$, $R_3=5k\Omega$, $R_f=1M\Omega$, $C_f=2nF$. The circuit of figure 3b was built by: $R_f=1M\Omega$, $C_f=2nF$, $R_1=R_2=R=200k\Omega$, $R_a=R_b=100k\Omega$ ($a=0.5$). The resistor and capacitor tolerances are *1%* and *20%* respectively. The $2M\Omega$, $200k\Omega$ and $5k\Omega$ resistors, and the *2nF* capacitors are built-up, depending on the case, by the series or parallel association of two equal components. The *TL054* enhanced-JFET low offset and noise op-amp is used.

When measuring the circuits a last problem appears. Taking for instance the one in figure 3a, it is showed by the curve named *"NoComp"* in figure 7a, that its G_D vs. frequency response has a large resonance peak. This can be explained considering that, ideally, the feedback action of the first-stage op-amp virtually shorts the sensor, but in practice a finite error voltage remains across it. This error is negligible at low frequencies, but it increases at the higher ones because the op-amp open-loop gain rolls off. So, the circuit input stage can be modeled as an *LC* parallel between the sensor capacitance and the inductive-like behavior of the op-amp based first-stage circuit [5].

The resonance peak can be attenuated by reducing the gain of G_D just before the resonance frequency. For the first-stage of the circuit in figure 3a this can be easily obtained in practice by adding two bypass capacitors, named C_1 and C_2, in parallel to R_1 and R_2 (for the (12)-(15) the gain is proportional to $R=R_1=R_2$). Relatively small capacitors are enough because R is in general high, and because of the contribution from the op-amp parasitic capacities.

For the circuit in figure 3a, figure 7 show the measured $|G_D|$ and $|CMRR|$ vs. frequency comparing different cases: *(1)* no compensation; *(2)* compensation by only a feedback capacitor ($C_1=33pF$, $C_2=0F$); *(3)* compensation by two capacitors ($C_1=C_2=33pF$). The latter option, resulting in a more symmetrical topology, gives the best results.

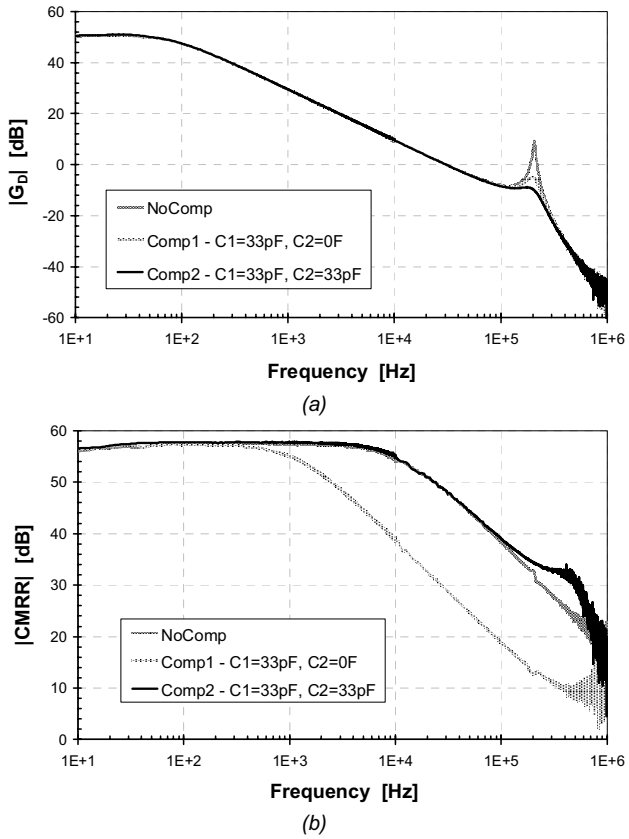
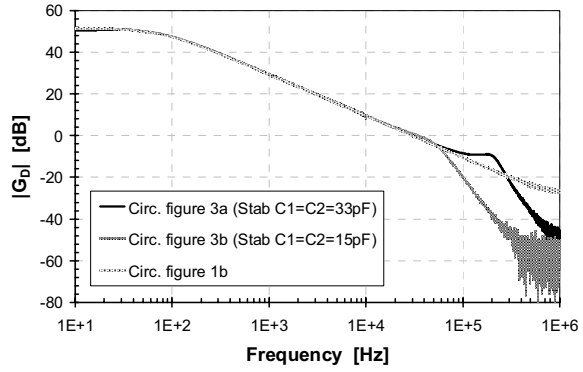


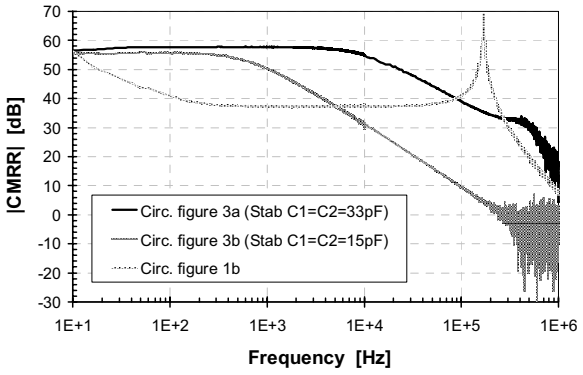
Figure 7. *(a)* G_D, and *(b) CMRR* vs. frequency for the circuit in figure 3a (G_D is *80dB* attenuated). The original response (*NoComp*) is compared with the ones obtained attenuating the G_D resonant peak by a single feedback capacitor (*Comp1*) or by two capacitors (*Comp2*). The best results are from this latter case.

Analogously to the previous case, the performance of the circuit in figure 3b can be optimized compensating it by two capacitors ($C_1=C_2=15pF$): C_1 is placed in parallel to R_1, C_2 from the non-inverting op-amp input to ground.

To compare the obtained performance, figure 8 shows $|G_D|$ and $|CMRR|$ vs. frequency for the benchmark circuit of figure 1b, and the novel circuits of figure 3a (compensated by $C_1=C_2=33pF$) and figure 3b (compensated by $C_1=C_2=15pF$). All the circuits show the same $|G_D|$ vs. frequency response, with some minor differences at higher frequencies that are due to the op-amp limitations. The differences between the studied circuits mainly reflect in their $|CMRR|$ vs. frequency responses. The particular shapes are mainly due to mismatch at low frequency and induced by op-amp limitation at the higher ones. The measured $|CMRR|$ is about *57dB* at *10Hz* for all the circuits. By (22) and (24), the $|CMRR_{min}|$ is *40dB* so the matching actually obtained from the test is better than the theoretical worst case.



(a)



(b)

Figure 8. *(a)* G_D, and *(b) CMRR*, vs. frequency for the benchmark circuit of figure 1b, the proposed circuits of figure 3a (compensed with C_1=C_2=*33pF*) and figure 3b (compensed with C_1=C_2=*15pF*).

For the benchmark circuit of figure 1b, the *CMRR* falls at very low frequencies since capacitor mismatch adds its effect to the resistor mismatch, as theoretically explained by (22). Contrarily, the novel circuits of figure 3 exhibit a higher *CMRR* because it depends only on two resistors matching, as theoretically explained by (23). The op-amp limitations, negligible at lower frequencies, are more relevant as the frequency increases and become dominant when they produce a drop in the *CMRR* higher than the one mismatch does. This corresponds to the corner frequencies located at about *700Hz* for the circuit in figure 3b, *11kHz* for the circuit of figure 3a, and it corresponds to the resonance peak for the circuit of figure 1b.

It is concluded that, for the same G_D, both novel circuits of figure 3 have a better *CMRR* than the reference circuit of figure 1b, because they rely on only a resistor matching. In particular, the circuit of figure 3a has the best *CMRR* because the low frequency value is maintained for a wider frequency band. In effect, at about 5.3kHz the |*CMRR*| of the circuit in figure 3a is *19dB* higher than the one of the other circuits. These results validate the advantages of the design technique proposed.

IV. CONCLUSIONS

Differential charge-amplifiers are widely used to interface differential charge generating sensors because they reject the common-mode input, typically due to interferences. Anyway, the *CMRR* of the most widely known topologies is practically limited because it relies on at least two matching conditions between resistors and capacitors. This is because the common-mode rejection and the charge-to-voltage conversion are both implemented by a single stage circuit.

This paper suggests a design technique to obtain two-stage differential charge amplifiers, so that the common-mode input is rejected by the first stage and the integration is separately implemented by the second one. From this general approach, two novel circuits are obtained. It is concluded that, as demonstrated by mathematical analysis and measurements, they have a better *CMRR* than the conventional topologies, because it only relies on a single resistor matching condition (easier to obtain in practice).

It is also explained how the charge amplifier topologies, with only some minor redesign and better named transresistance amplifiers, can apply to current generating sensors. This permits to easily extend the results to this class of circuits.

Finally, because the frequency response of the proposed circuits show an unwanted resonance pick, it is suggested a simple technique to improve the stability.

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