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Performance Assessment of Memristor Networks as Shortest Path Problem Solvers

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Outline

Introduction

- Memristor networks as a massively parallel computing approach
- Computing platform functionality

Modeling Directed Graphs with Memristors

- The shortest path problem

Setup of Memristor Network Computing Platform

- Important considerations
- Simulation results
  - Impact of device switching properties
  - Comparison with known algorithmic solutions

Concluding remarks

Introduction

- Studying the overall response of memristors networks gained an ever-increasing interest after it was shown that such device technology could lead to a new **massively parallel analog computing approach**

- Memristor networks seem to be **promising as computing medium for complex optimization problems**.
  - the problem of computing the shortest-path (SPP)

Y. V. Pershin, M. Di Ventra, *Phys. Rev. E*, 84(4), 46703, 2011

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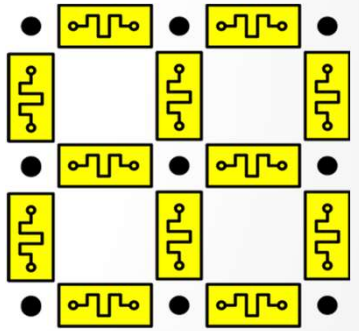

Introduction

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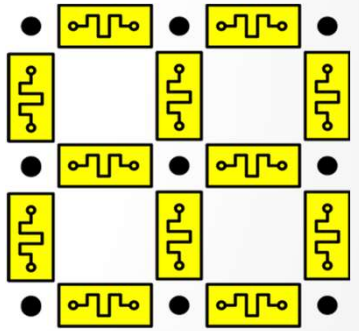
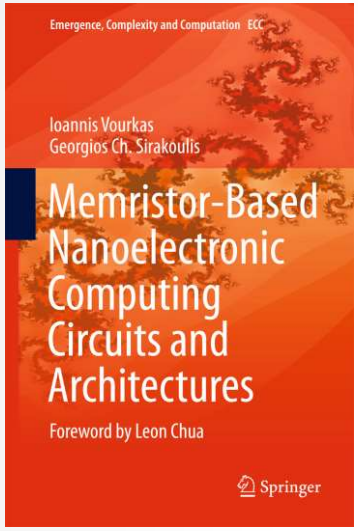
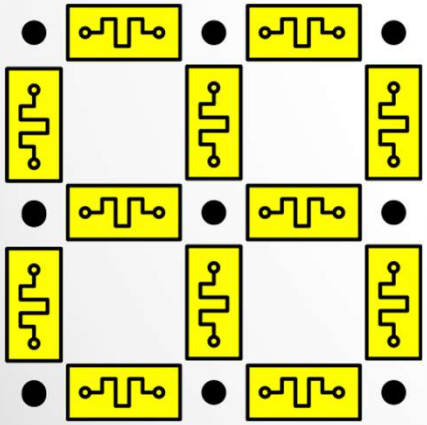


- We *revisit* this topic presenting a case study of the performance of memristor networks as SPP solvers w.r.t.:
  - the memristor device properties
  - the graph topological features

Modeling Edges of *Directed Graphs*

A methodology from the recent literature

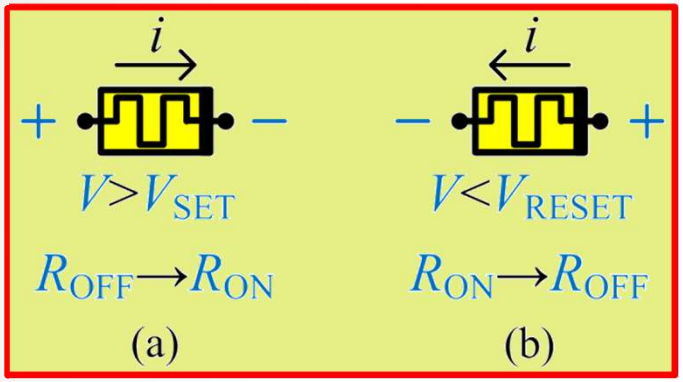


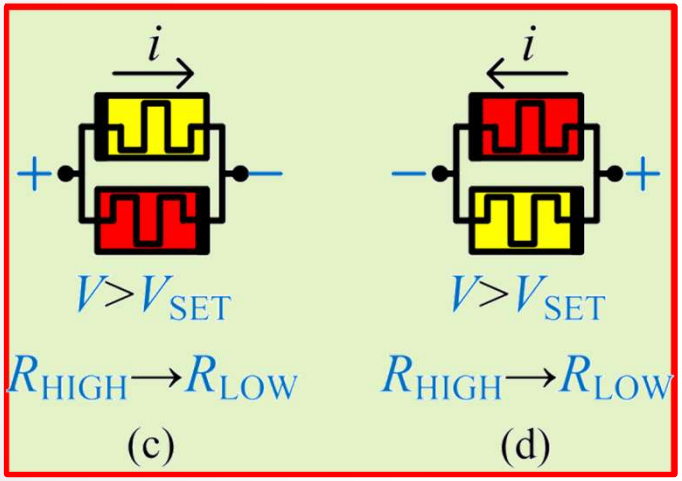


	Graph connection	Corresponding circuit model	Description
(a)	e = const	R	Bidirectional connection with fixed edge weight e corresponds to a resistor
(b_1)			Unidirectional connection corresponds to a properly polarized memristor. The use of a series or parallel resistor of value equal to R_{OFF} is optional and depends on the selection of (d)
(b_2)			
(c_1)			
(c_2)			
(d)			Bidirectional connection with variable edge weight corresponds to a pair of serial/ parallel memristors with opposite polarities
(e)	$e = f(v)$		Circuit correspondence for bidirectional connection with **reversible** variable edge weight depending on the applied voltage
(f)	$e \approx 0$	R_{MIN}	Connections with zero edge weight correspond to short-circuit, i.e. a resistor with resistance close to zero ($R_{MIN} \approx 0$)
(g)		R_{MAX}	No connection between adjacent vertices corresponds to open-circuit, i.e. a resistor with very high resistance ($R_{MAX} >> R_{OFF}$)

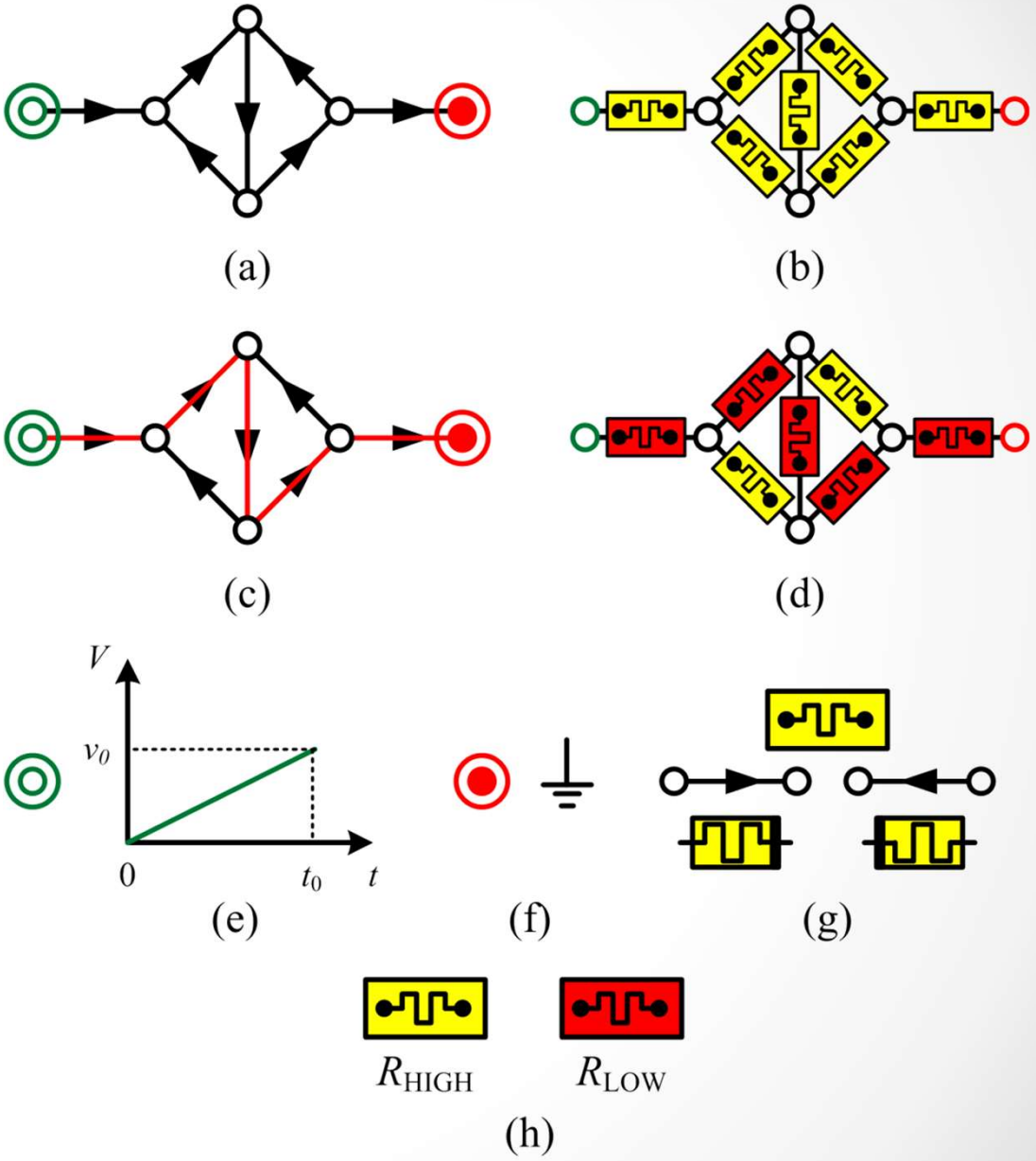
Functionality of Computing Medium

Polarity-dependent Switching



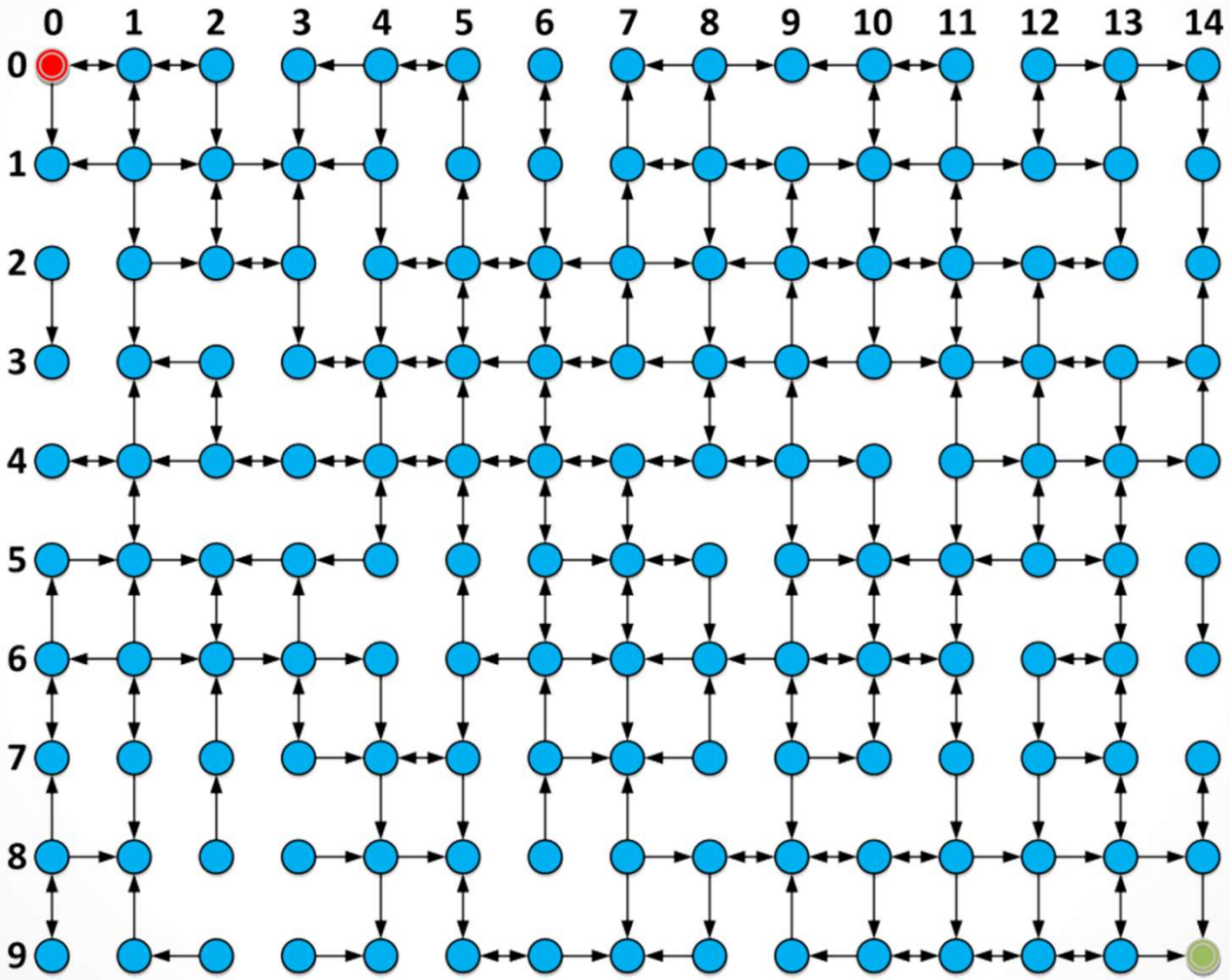


Independency on the sign of the applied voltage



Modeling Edges of *Directed Graphs*

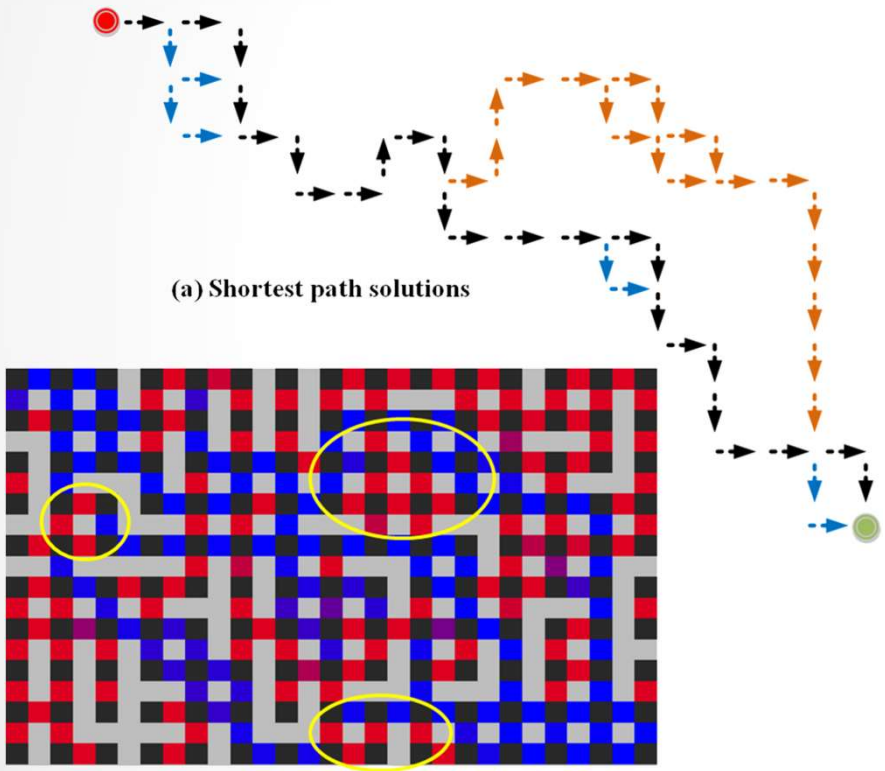
An example of a directed (oriented) graph



Modeling Edges of *Directed Graphs*

Simulation results

From one source to one destination



(a) Shortest path solutions

(b) Visualization of the memristive network simulation result

Computing Capabilities

- First computes the **best** possible solution
- Next reveals all existing solutions **in order** according to their length
- The shortest path is found without supervision: it emerges from the dynamical evolution of the system.
- The computation is fully parallel.

Memristor model used in simulations

Y. V. Pershin, and M. Di Ventra, *IEEE Trans. Circ. Syst. I, Reg. Papers*, vol. 57, no. 8, 1857 - 1864, 2010

Y. V. Pershin and M. Di Ventra, *Radioengineering*, vol. 22, no. 2, pp. 485–489, 2013

Basic Setup of Memristive Networks

Important considerations:

- Correct/required (minimum) **input voltage amplitude**
- **Time** required to finish computation
- The ability to know **if a solution was found**
  - **Reading** of the solution (step by step)

Basic Setup of Memristive Networks

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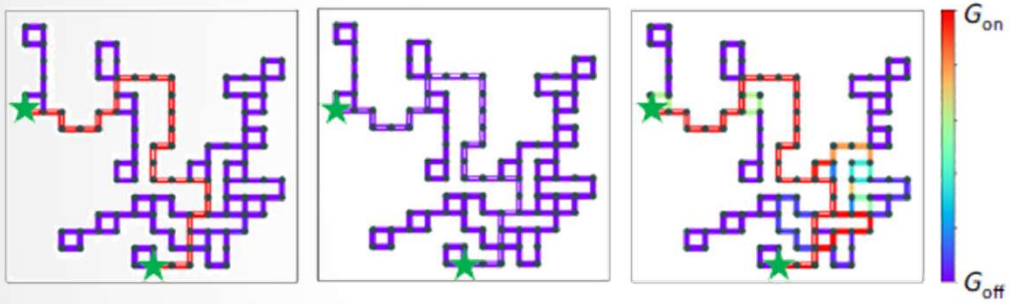
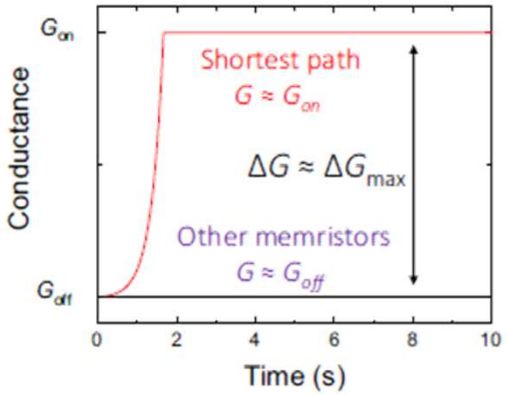
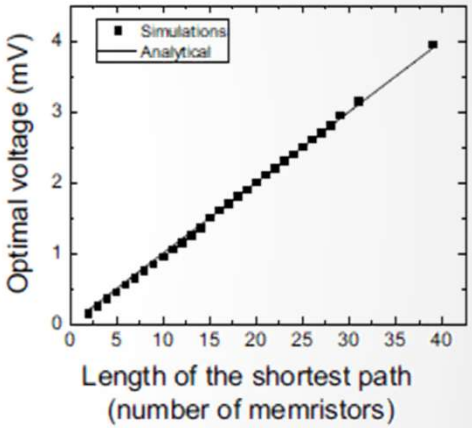




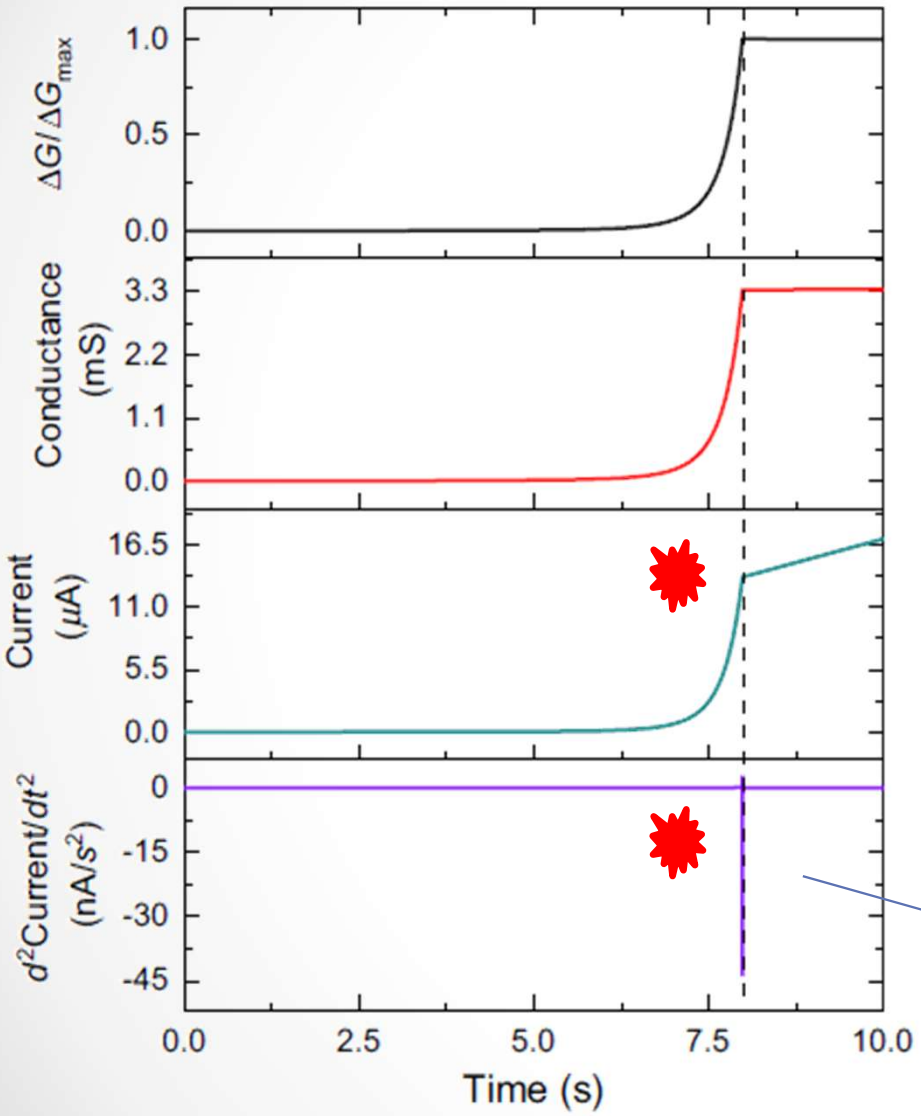


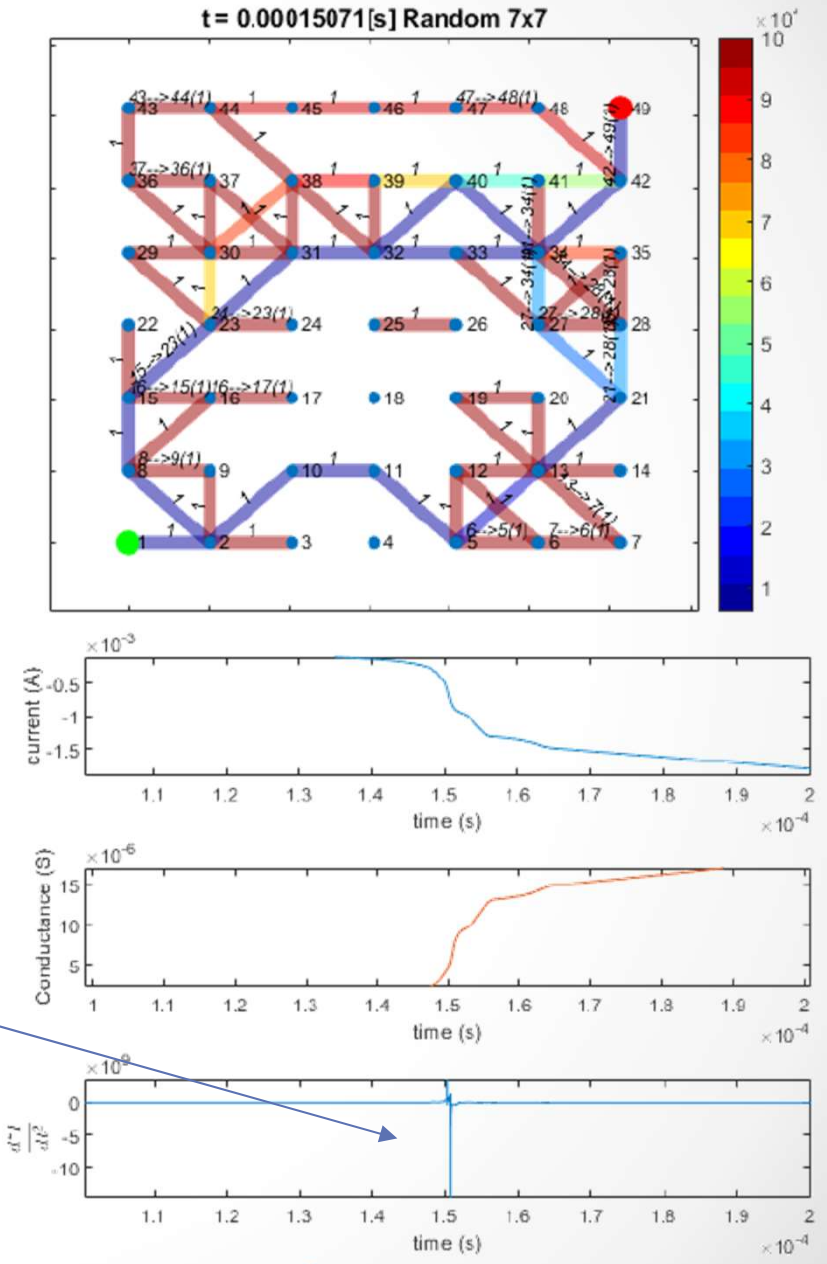
- **Detection**: A recent work suggested using the *overall network conductance*, the input *current* and the *second time-derivative* of it.
- **Read-out**: The shortest path starts with the start node. The next node on the shortest path is the one connected through the highest conductive memristor

An optimal input voltaje will turn on the shortest path but NOT any other longer paths

A. Mizrahi, *et al*. *Phys. Rev. Applied* 10(6), 064035, 2018

The moment when computation is finished





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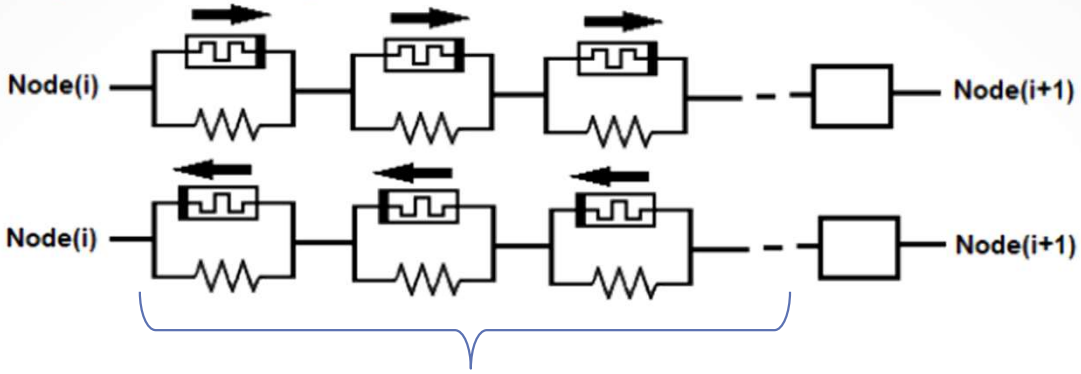
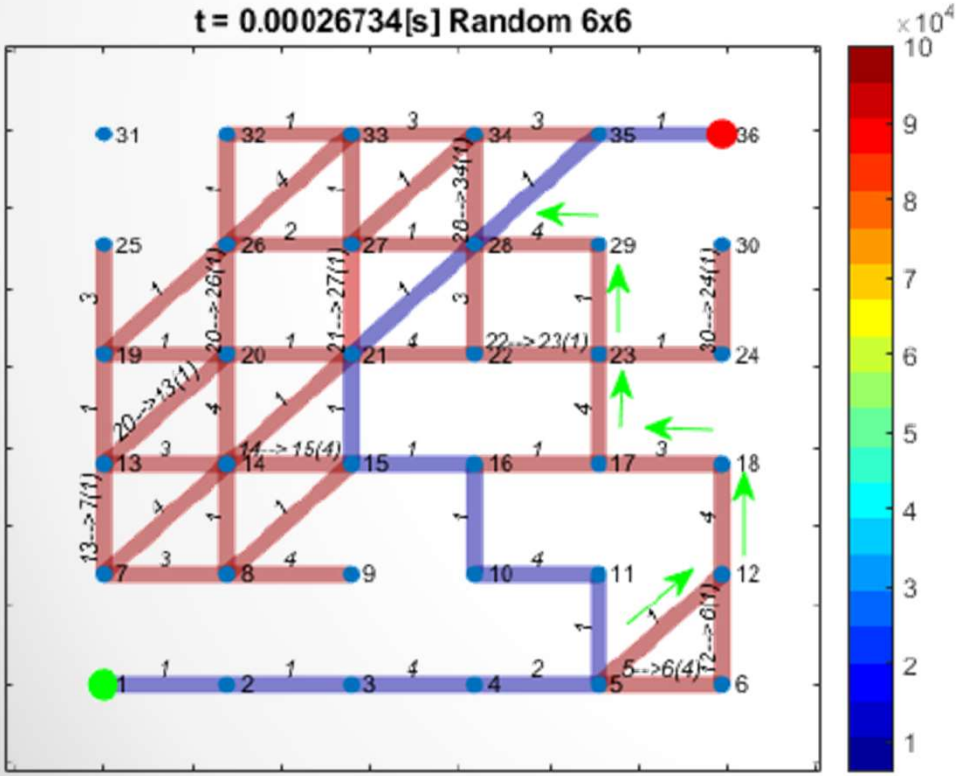
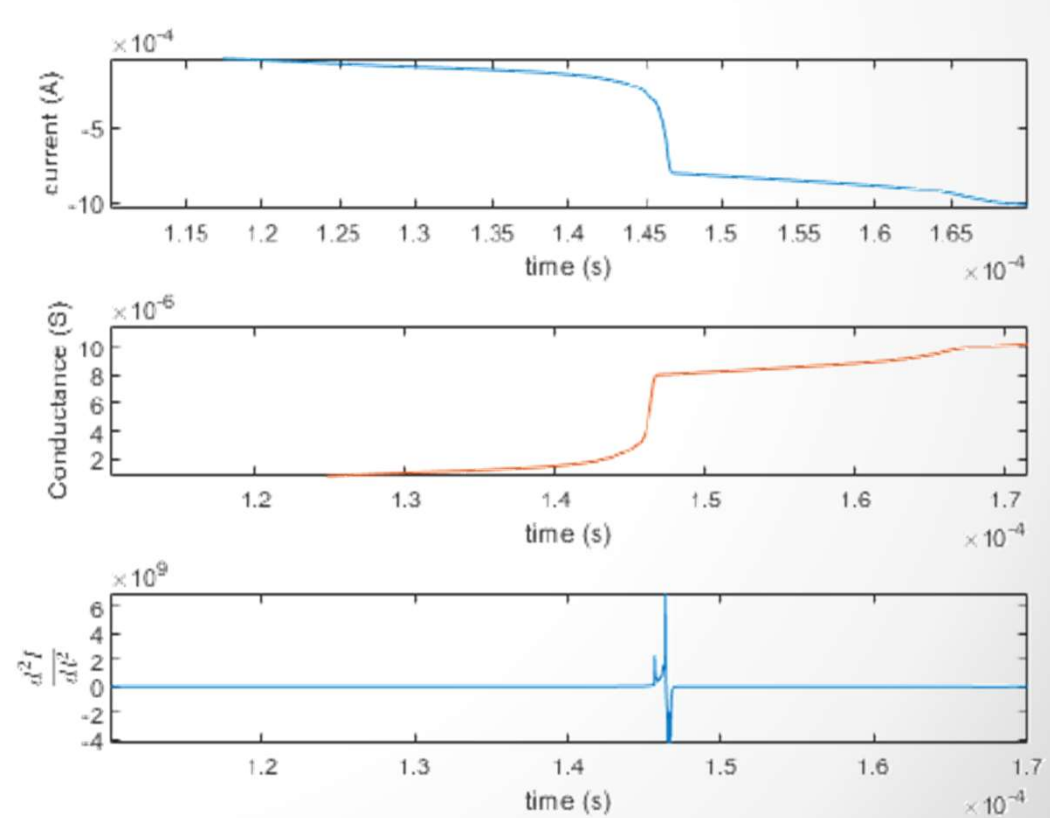
Modeling Weights in Directed Graphs

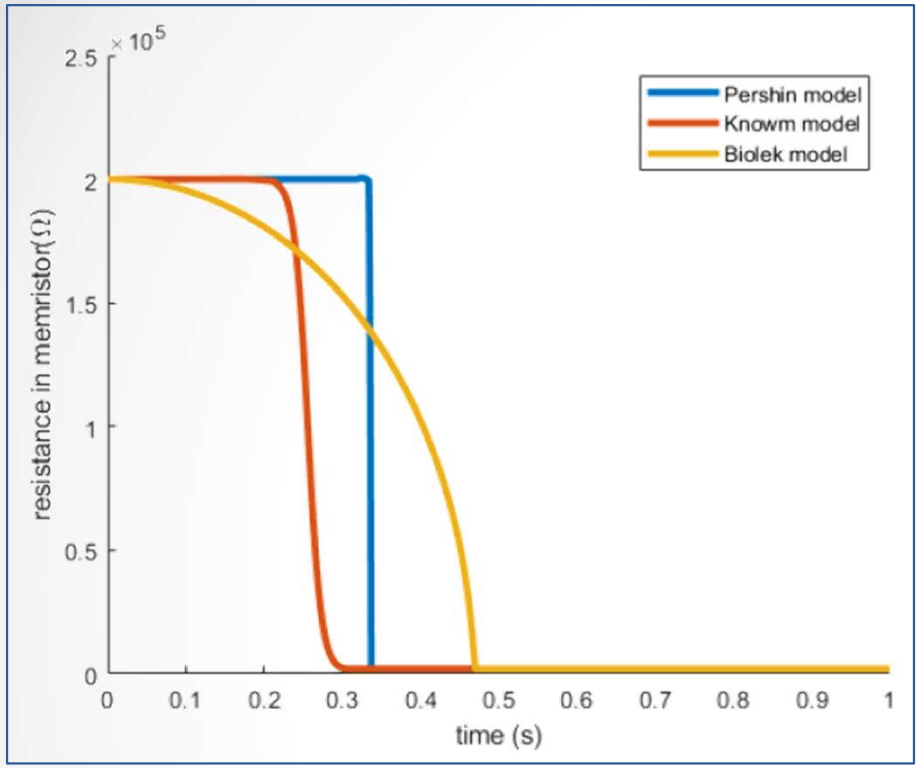


n connections





Impact of Different Switching Behavior



We compared device models that present *fundamentally different switching behavior*, and checked their suitability for such computing tasks.

- HP (linear) model
- Behavioral threshold-type model
- …

Z. Biolek, *at al*., "SPICE model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, 2009

Y. V. Pershin, and M. Di Ventra, *IEEE Trans. Circ. Syst. I, Reg. Papers*, vol. 57, no. 8, 1857 - 1864, 2010

$$v = \mathcal{R}(w,i)\,i$$

$$\frac{dw}{dt} = f(w,i)$$

$$v(t) = \left(\mathcal{R}_{ON}\frac{w(t)}{D} + \mathcal{R}_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t)$$

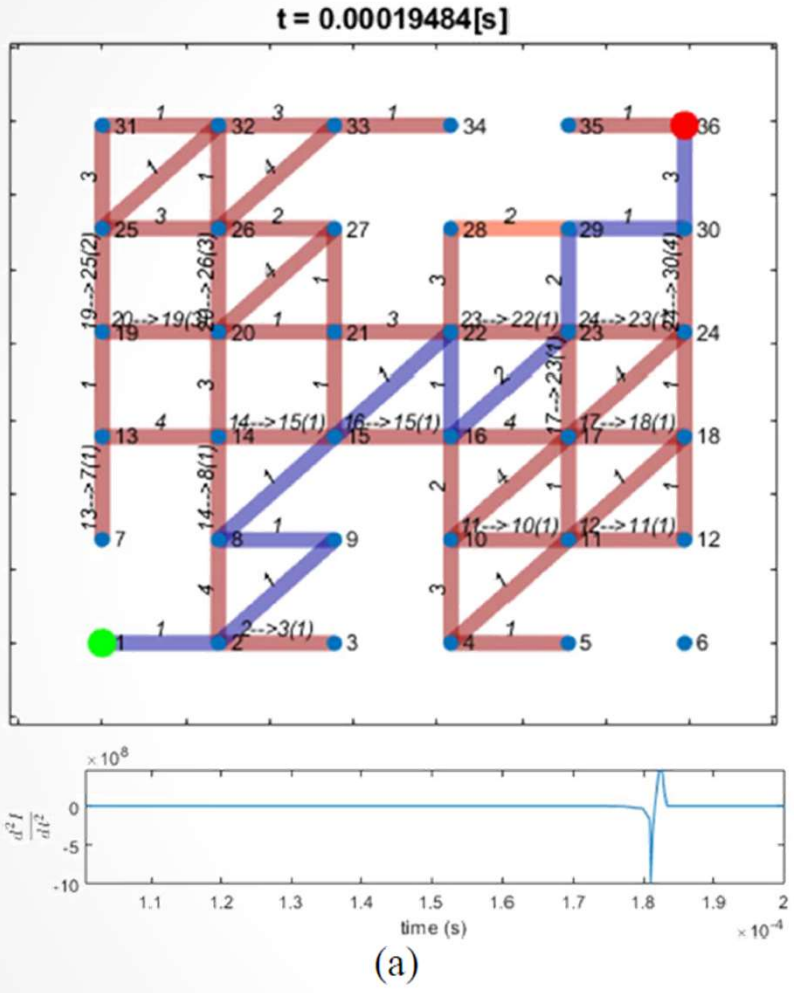
$$\frac{dw(t)}{dt} = \mu_V \frac{\mathcal{R}_{ON}}{D}\, i(t)$$

$$\begin{aligned} I &= X^{-1} V_M, \\ \frac{dX}{dt} &= f(V_M)\left[\theta(V_M)\,\theta(R_{off} - X) + \theta(-V_M)\,\theta(X - R_{on})\right] \end{aligned}$$

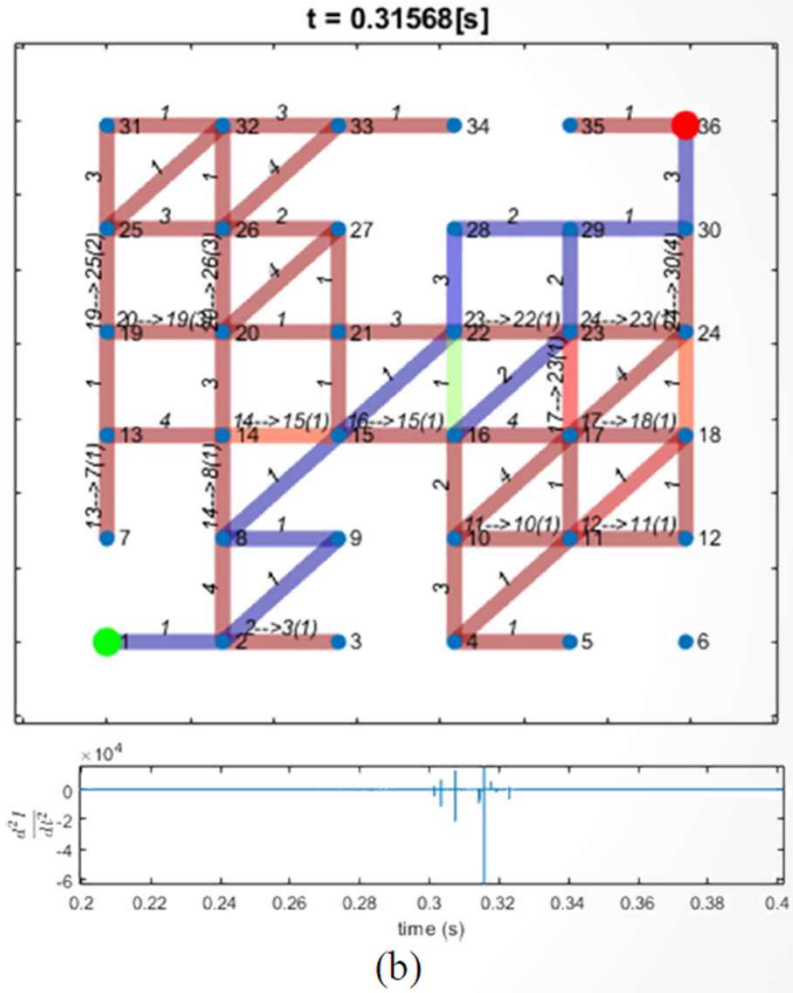
$$f(V_M) = \beta V_M + 0.5(\alpha - \beta)\left[|V_M + V_t| - |V_M - V_t|\right]$$

Impact of Different Memristor Models

a solution is always found regardless of the model type, but…



Threshold-type model

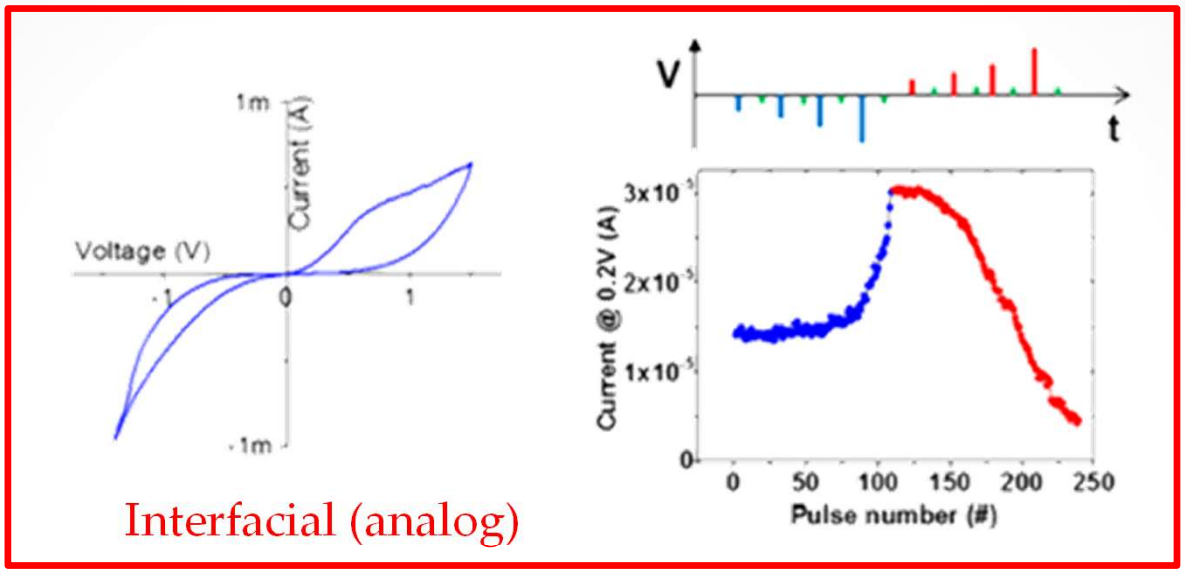


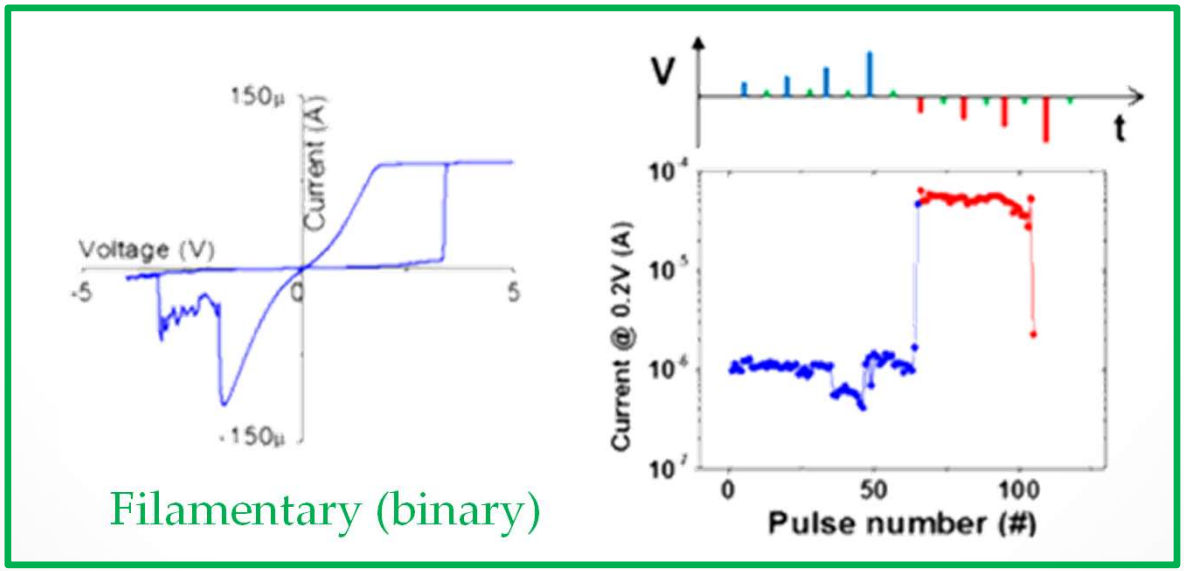
Linear HP model

Partially formed paths emerge

Problems in read-out phase

Analog Vs *Binary* Memristor Switching

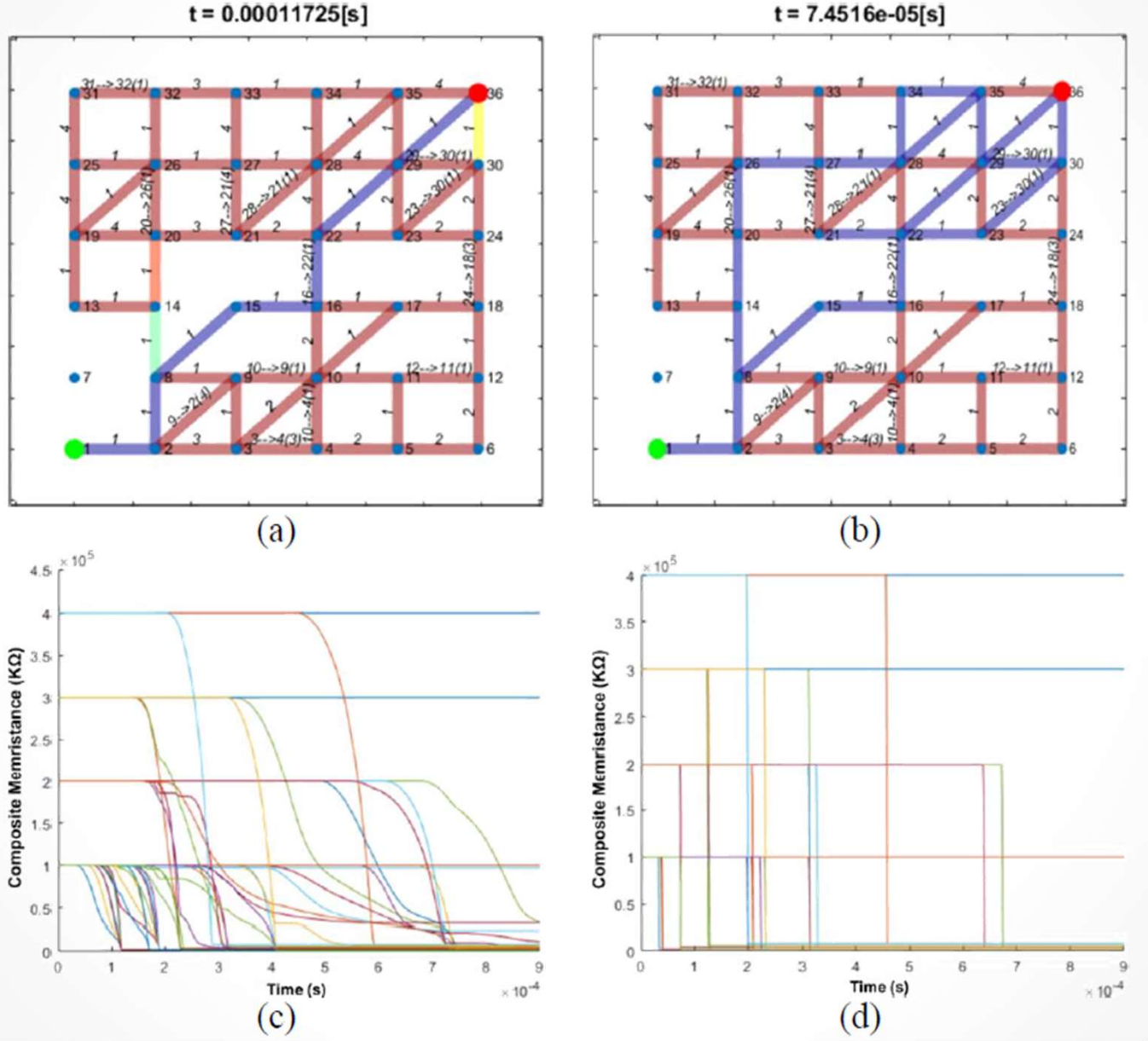




G. Sassine *et al.*, "Interfacial versus filamentary resistive switching in TiO2 and HfO2 devices," *J. Vac. Sci. Technol*. vol. B34 (012202), 2016

Analog Vs *Binary* Memristor Switching

A



B

Analog Vs *Binary* Memristor Switching

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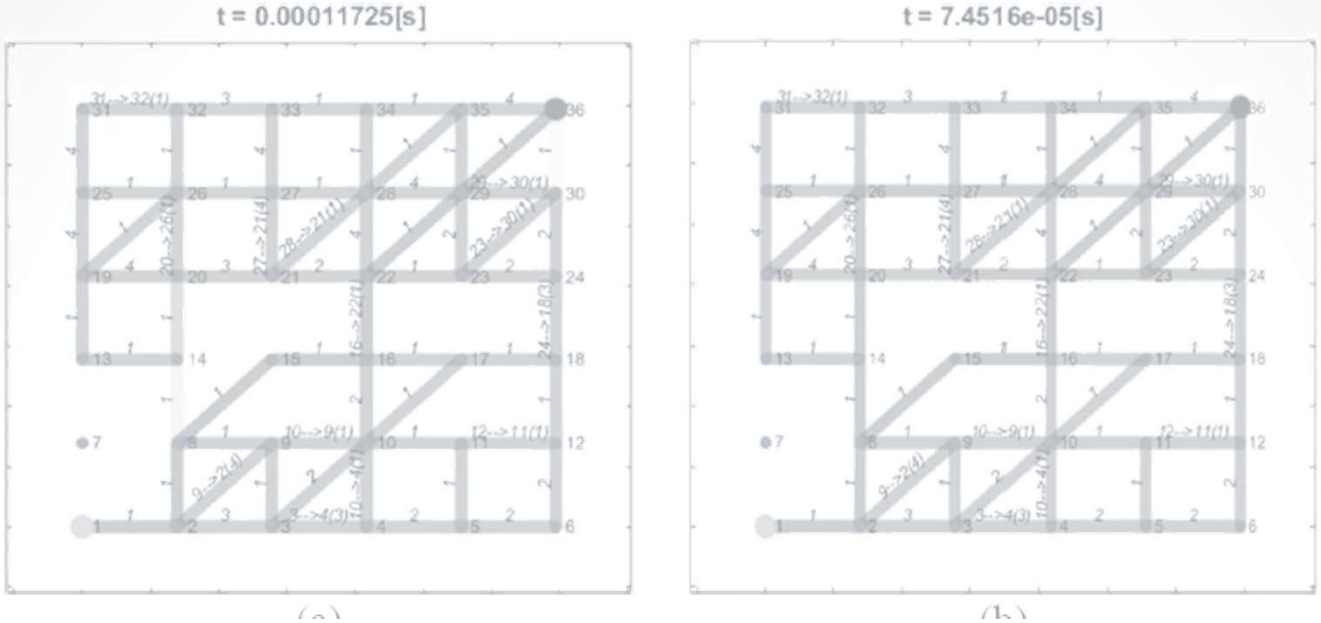


B

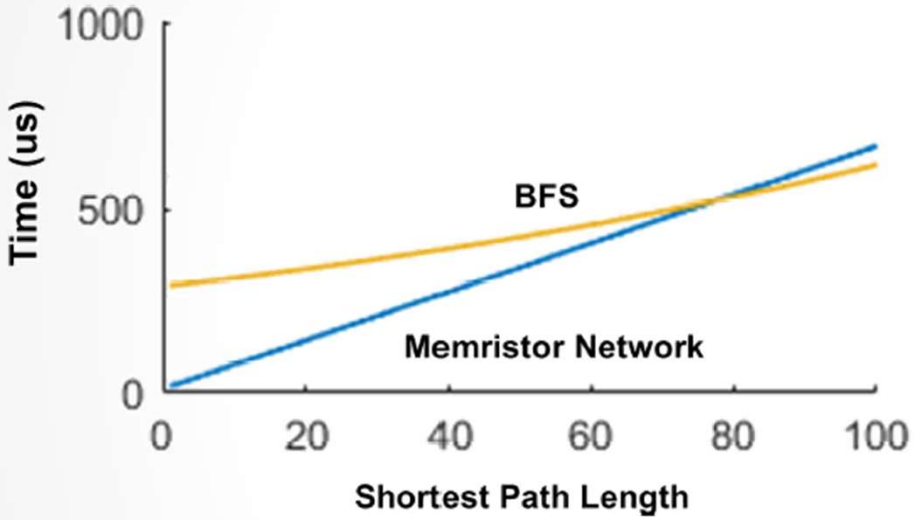
For binary memristors…

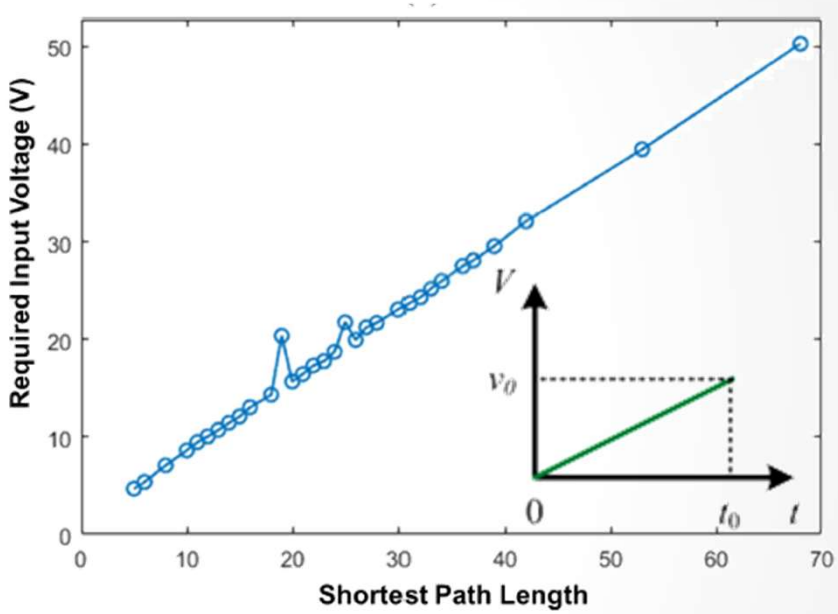
- We observed in several cases that the final network state had many low-resistive edges that were **NOT part of** the SPP solution

- Branches with small differences in the total weight switch to LRS altogether simultaneously, thus creating erroneous solutions to the SPP and/or problems for correct read-out

Comparison with Algorithmic Solutions

- *Computation time correlates strongly with the length of the shortest path* in the graph
  - this scaling **does not depend on the topology of the graph**
  - this is a great **advantage** compared to known algorithmic methods





- Compared to **Breadth First Search (BFS)** algorithm, the memristor network-based approach results **more efficient** especially for large graphs with small shortest paths.

- Adding an offset to the ramped voltage input according to an "expected" shortest path length, will reduce the total computation time.

Concluding Remarks

- We highlighted **the potential of memristor-network based graph solvers** for shortest path computations

- Observations concern the **desired memristor device behavior** and the impact on computation time, on the detection of a solution, as well as on the precise read-out of the solution

- The memristor-network based computations proved advantageous over conventional algorithmic solutions and can be further improved by fine tuning the applied input voltage

However…

- The practical feasibility of such computing architectures requires further clarity on several aspects of hardware

Thank you All for your kind attention!

• • •

Questions ?

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