An Ultra-Low-Power CMOS Voltage-Controlled Ring Oscillator for Passive RFID Tags

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***Abstract*—An ultra-low-power CMOS voltage-controlled ring oscillator (VCRO) for passive ultra-high-frequency (UHF) radio-frequency identification (RFID) tags is presented. The gates of the complementary CMOS transistors in pseudo-differential (PD) delay cells are biased through quasi-floating gate (QFG) technique. The boosted gate-drive voltage enables operation of the differential delay cells with supply voltages smaller than the minimum required overdrive voltage of the two stacked transistors and accordingly facilitates the oscillation at ultra-low-power regime. QFG biasing technique also offers an additional control knob to tune the output frequency of the ring oscillator. The proposed two-stage PD-VCRO is designed and laid-out in a standard 0.13-μm CMOS technology. A voltage level converter is also presented to interface the output of the proposed VCRO with the succeeding circuitry. The entire VCRO core occupies an area of 25 μm$\times$20 μm. For a supply voltage of as low as 140 mV, an output frequency of 4 MHz is achieved at 3.6 nW power consumption. Although the intended application for the proposed VCRO is passive RFID tags, the architecture can be used in other ultra-low-power applications.**

***Index Terms*—Ring oscillator, voltage controlled, ultra low power, RFID, passive, CMOS.**

I. Introduction

Radio frequency identification (RFID) is an emerging technology which has gained an extensive attention in recent years. RFID tags are being deployed in numerous applications ranging from retail management, internet of things, health care, access control, payment systems and many more [1]. Among the three popular categories of RFID tags, namely active, semi-passive, and passive tags, the latter is the most attractive candidate for large scale deployment in virtue of its low cost, longevity, and maintenance free lifetime. Passive tags harvest their entire required energy either from the incoming radio-frequency (RF) signal transmitted by the reader or from the environment in the form of thermal energy, light and/or vibration. However, the absence of a dedicated energy source (e.g., a battery) poses some stringent challenges, entailing an energy aware design at both system and circuit levels.

The block diagram of a generic passive RFID tag (transponder) is shown in Fig. 1. The analog front-end is responsible for power harvesting and signal modulation/demodulation while the back-end processing unit controls data coding/decoding and memory/sensor access. As shown in the figure, a clock generator is an integral part of the processing unit. The

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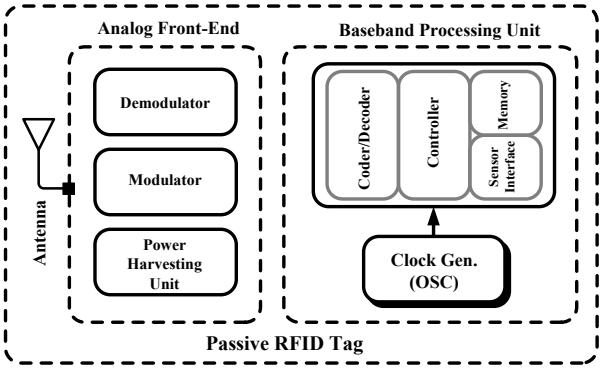

Fig. 1. Block diagram of a generic passive RFID tag.

EPCglobal™ Gen 2 mandates a minimum clock frequency of 1.92 MHz to guarantee a high-performance data transfer [2], [3]. To generate the required clock, a viable solution is to extract it from the incoming RF signal. However, such an approach requires a chain of dividers to convert the ultra-high-frequency (UHF) carrier (860 MHz to 960 MHz) to the required baseband clock frequency [4]. The complexity and power overhead imposed by the dividers typically rules out this scheme in passive RFID tags, suggesting incorporation of a local (voltage-controlled) oscillator.

Passive LC oscillators and ring oscillators (ROs) are the two main categories of oscillators in CMOS technology. Unfortunately, the inductor as an essential component of LC oscillators does not simply lend itself to high-level of integration at UHF frequencies. LC oscillators also suffer from a limited frequency tuning range specifically in low-voltage applications where they have a narrow frequency tuning range [5]. In contrast, ring oscillators are not inherently dependant upon passive components (e.g., inductors) which is greatly desirable in the context of passive RFID tag design. Apart from silicon area considerations, low power consumption is also of paramount importance in passive tags considering their tight power budget. The local oscillator is a major contributor to the overall power consumption in passive tags. It is worth mentioning that passive UHF tags use backscattering method for the communication from the tag to the reader and theoretically do not allocate power for data transmission.

Extensive research has been conducted to address the power consumption of the ring oscillators at a circuit-level perspective. In [6], the the delay cells of a RO are biased in the weak inversion region. The proposed oscillator achieves a power consumption of 24 nW for a 5.12 MHz oscillation

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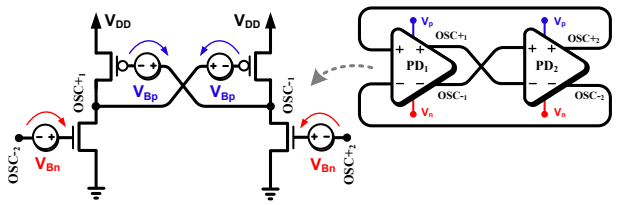

Fig. 2. Schematic diagram of the proposed two-stage ring oscillator.

frequency with 0.3 V power supply. In [7], a supply voltage of 0.3 V allows MOS transistors in the current-starved inverters to operate in subthreshold, near-threshold and above threshold regions. The proposed design consumes 95 nW for the entire RO-based temperature sensor while oscillating at 2 MHz to 8 MHz. The DC current of the current-starved inverters are controlled to minimize the power consumption in [4]. The proposed design in [4] oscillates at 1.28 MHz and consumes 440 nW from a 0.9 V supply.

In this paper, the gate-drive voltage of CMOS transistors in pseudo-differential delay cells are boosted through the use of quasi-floating gate (QFG) architecture [8]. The boosted gate-drive voltages facilitate oscillation with supply voltages as low as 90 mV which accordingly results in a low power consumption. The QFG technique practically imposes minimal area overhead and provides a secondary control mechanism over oscillation frequency. The paper is organized as follows: Section II describes the proposed low-power oscillator. Section III presents the simulation results and Section IV concludes the paper.

II. The Proposed Low-Power Ring Oscillator

As mentioned in Section I, low power consumption, small area, and tunability are major performance requirements of the local oscillator in the context of UHF passive RFID applications. Ring oscillators are a suitable candidate for such applications. The delay cells in a ring oscillator are implemented as either single-ended or differential inverting amplifiers [5]. While the single-ended ring oscillator (SRO) requires an odd number of stages (minimum of three stages), its differential counterpart could be implemented with lower number of stages (minimum of two stages accommodating 4 current branches). The differential ring oscillator provides a better common-mode noise and supply rejection ratio and is capable of producing quadrature output signals. The power consumption of a ring oscillator is the summation of the static (P_S) and dynamic (P_D) power of the inverting amplifiers and is given by [9]:

$$\begin{aligned} P_{tot} &= P_S + P_D \\ &= I_{leak}\ V_{DD} + N\ f\ C_L V_{DD}^2 \end{aligned} \tag{1}$$

where I_{leak} is the leakage current of the inverting amplifier, V_{DD} is the supply voltage, N is the number of current branches, f is the frequency of oscillation and C_L is the capacitance of the output nodes. As suggested by Eq. 1, for a given frequency of operation, the supply voltage, V_{DD}, and the number of stages, N, have to be minimized to reduce the power consumption.

In the proposed RO, a two-stage pseudo-differential (PD) quasi-floating-gate (QFG) architecture is employed. The PD

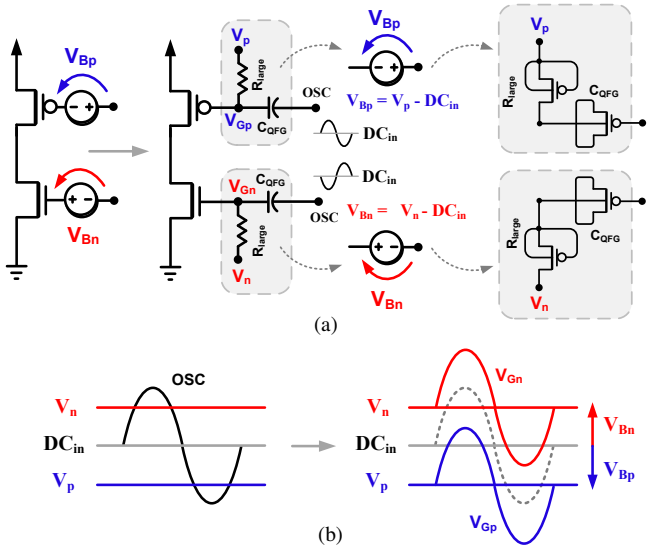

Fig. 3. Implementation of the floating voltage sources through QFG architecture. (a) Schematic diagram of circuit-level implementation, (b) Schematic diagram of the boosted waveforms.

architecture saves the voltage headroom for the tail transistor and allows oscillation with the minimum number of stages. To meet the *Barkhausen* criterion [10], each PD stage utilizes a local positive feedback in the form of two cross-coupled PMOS devices. The schematic diagram of the proposed QFG-biased PDRO is shown in Fig. 2 where the gate-drive voltages of transistors are boosted through floating voltage sources. As shown in the figure, the floating voltage sources shift the AC input to the gates of transistors in a positive and negative direction for the NMOS and PMOS transistors, respectively. The boosted gate-drive voltages partially compensate the threshold voltage of transistors, facilitating oscillation with supply voltages smaller than the summation of the threshold voltages of the stacked transistors in the PD architecture. The floating voltage sources $V_{Bp,n}$ can be efficiently implemented through the use of QFG architecture [8]. The QFG biasing scheme is shown in Fig. 3(a) where the AC input (OSC) is coupled to the gate of the transistor through the capacitor C_{QFG} while the large resistor R_{large} weakly connects the gate to the desired DC bias voltages ($V_{n,p}$). As shown in Fig. 3(b), the effective value of the floating voltage sources are given by:

$$V_{Bn,p} = V_{n,p} - V_{DCin} \tag{2}$$

where V_{DCin} is the average voltage of the AC input, OSC, and is approximately equal to $V_{DD}/2$ for a rail-to-rail oscillator output. Boosting the gate-source voltages of the transistors as shown in Fig. 3(a) virtually enhances the effective supply voltage by: $V_{Bn}+|V_{Bp}| = V_n - V_p$, which allows oscillation with smaller V_{DD}. Note that $V_p < V_{DCin}$ and accordingly, V_{Bp} is a negative voltage offset (see Fig. 3(b)).

As shown in Fig. 3(a), to save silicon area, the large resistor R_{large} can be implemented by the large leakage resistance of the reverse biased p-n junction of a PMOS in cut-off region [8]. The value of this resistor is not that critical as long as it is relatively large. The implementation of the coupling capacitor C_{QFG} requires further attention during the design process. The

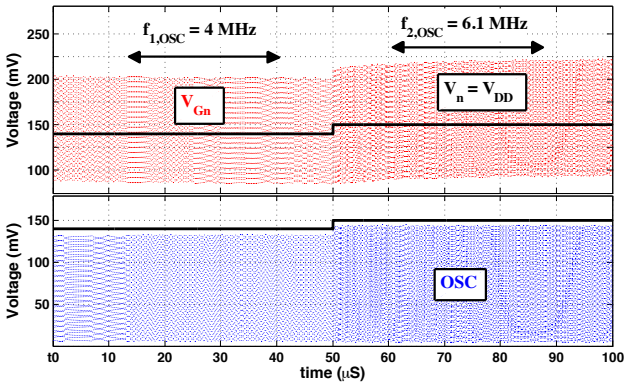

Fig. 4. Transient settling behavior of the proposed QFG-biased VCRO.

value of C_{QFG} affects the performance of the RO through two separate mechanisms as follows:

1) Coupling the AC signal, V_{OSC} to the gate terminals through C_{QFG} forms a capacitive divider at the gate of transistors and slightly attenuates the amplitude of the AC component. The QFG-coupled gate voltages $V_{Gn,p}$ are given by (see Fig. 3(a)):

$$V_{Gn,p} = V_{OSC} \times \frac{C_{QFG}}{C_{QFG} + C_{Gn,p}} \tag{3}$$

where $C_{Gn,p}$ is the total parasitic capacitance seen at the gate of NMOS and PMOS transistors. Eq. 3 suggests the use of a large coupling capacitor in order to fully exploit the available gate-drive voltage. However, aside from area considerations, an excessively large C_{QFG} increases the delay of the PD cells and accordingly reduces the oscillation frequency. Moreover, as shown in Eq. 1, the large output capacitance C_L, increases the total power consumption of the oscillator. Therefore, for a fixed set of design parameters there is an optimum range of C_{QFG} which results in a good performance in terms of oscillation frequency, silicon area, and power consumption.

2) The QFG architecture of Fig. 3(a) forms a low-pass RC filter along the path from the bias node ($V_{n,p}$) to the gate of transistors. Thus, the DC value of the gate experiences a delay before fully settling to the desired value $V_{n,p}$. The settling behaviour is of particular importance if the RO is to be used as the VCO in a phase-locked loop. The time constant associated to this RC filter is given by:

$$\tau = R_{large} \times (C_{QFG} + C_{Gn,p}) \tag{4}$$

Eq. 4 further highlights the significance of the C_{QFG} value. In the proposed QFG-biased RO, for a nominal frequency of 4 MHz, the associated time constant is 12 μs which yields to T_{settle} ≈50 μs. The 50 μs settling time corresponds to 200 cycles of the oscillator output at 4 MHz which satisfies the settling requirements of a VCO in PLL applications. As shown in Fig. 3(a), to save area, the coupling capacitors are implemented with MOSCAP devices.

To fully exploit the voltage levels already available in the circuit for the boosting purpose, V_n and V_p are connected to V_{DD} and ground, respectively, hence allowing a lower supply voltage value (see Fig. 3(a)). Note that in view of Eq. 2 and the discussion that followed, such a biasing scheme enhances the effective supply voltage by V_{DD} (i.e., $V_n - V_p = V_{DD} - 0$). Therefore, the supply voltage and accordingly V_n are used as the VCO control voltage while V_p is kept constant at zero. Fig. 4 shows the transient waveform of $V_{G,n}$ in response to a step signal applied to the control voltage (V_{DD}=V_n). It is worth mentioning that both V_n and V_p could be used as a secondary frequency tuning knob. As discussed earlier, for a fixed V_{DD}, increasing V_n (V_p) virtually increases (decreases) the supply voltage and accordingly could be used to increase (decrease) the oscillation frequency.

The circuit-level diagram of the proposed VCRO is shown in Fig. 5. As shown, to interface the output of the VCRO with a succeeding circuitry that potentially uses a higher supply voltage, a quadrature-to-differential low-to-high voltage converter is proposed. The common-mode voltage of the input devices in the proposed converter is boosted through the use of QFG technique. The two output inverter buffers produce 50% duty-cycle fully differential outputs with a voltage swing of 0 to $V_{DD,H}$ from the low-voltage quadrature inputs. Note that, the capacitive loading effect of the converter slightly reduces the oscillation frequency and thus has to be accounted for in the design of the VCRO.

III. Post-Layout Simulation Results

A proof-of-concept prototype of the proposed VCRO is designed and laid out in 0.13 μm CMOS technology. For a supply voltage in the range of 90 mV to 160 mV, the input and load transistors in the delay cells operate in weak to moderate inversion regions and are sized to minimize the power consumption. PMOS transistors in cut-off region are used to implement R_{Large} and MOSCAP devices are used for C_{QFG}. Fig. 6(a) shows the oscillation frequency as a function of the supply voltage, while V_n is tied to V_{DD} (i.e., $V_n = V_{DD}$) and V_p is connected to ground (i.e., $V_p = 0$). As shown, an oscillation frequency (f_{OSC}) of 4 MHz is obtained for a

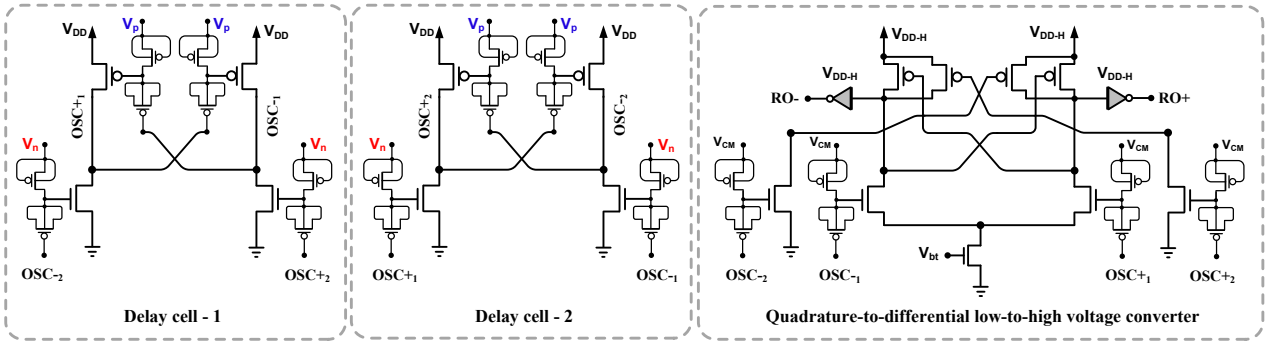

Fig. 5. Schematic diagram of the proposed VCRO and voltage level converter.

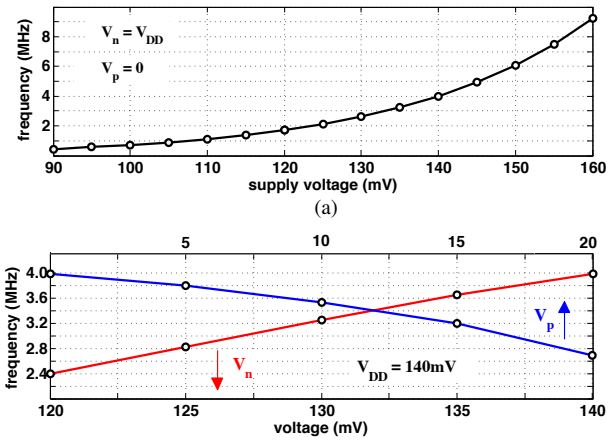

Fig. 6. Oscillation frequency of the proposed VCRO. (a) As a function of V_{DD}, (b) As a function of V_n and V_p .

140 mV supply voltage. f_{OSC} spans a range of 450 kHz to 9.2 MHz for a V_{DD} variation of 90 mV to 160 mV. The power consumption of the VCRO for this range extends from 0.24 nW to 9.8 nW, with 3.6 nW for the nominal oscillation frequency of 4 MHz. Fig. 6(b) shows the frequency as a function of V_n and V_p. For a fixed V_{DD} of 140mV, increasing V_n from 120mV to 140mV increases f_{OSC} from 2.4 MHz to 4 MHz while increasing V_p from 0 to 20 mV decreases f_{OSC} from 4 MHz to 2.7 MHz. For a V_{DDH}=0.6 V, the proposed low-to-high voltage converter consumes a power of 320 nW to generate a rail-to-rail differential clock (RO±) at 4 MHz frequency from the quadrature inputs (0 mV-to-140 mV swing $OSC_{\pm 1,2}$) while V_{bt}=200 mV and V_{CM}=400 mV (see Fig. 5).

The layout view of the proposed VCRO core is shown Fig. 7. The proposed VCRO occupies an area of 500 μm^2 (25 μm×20 μm) while only the first three metal layers (in a 0.13μm CMOS technology) are used for routing.

Table. I provides a performance summary of the proposed VCRO and compares it with the state-of-the-art VCOs in the similar range of oscillation frequency.

IV. Conclusion

An ultra-low-power voltage-controlled ring oscillator for passive RFID tag applications is presented. Using quasi-floating gate technique, the common-mode voltage of the devices in pseudo-differential delay cells are boosted, therefore, allowing oscillation with a low supply voltage. The QFG technique also offers a secondary frequency tuning knob. A quadrature-to-differential low-to-high voltage converter is presented to interface the low-swing output of the proposed VCRO with a higher voltage domain. Post-layout simulation results of the proposed VCRO confirm a nominal oscillation frequency of 4 MHz with a supply voltage as low as 140 mV while consuming 3.6 nW power. The VCRO core occupies an area of 500 μm^2.

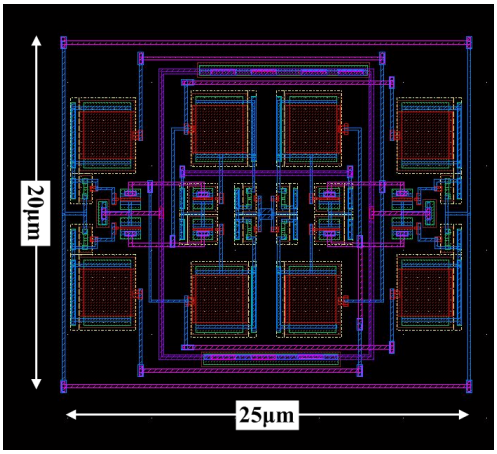

Fig. 7. Layout view of the proposed VCRO.

TABLE I
Performance Summary and Comparison.

Reference	[4][a]	[6][b]	[11][a]	[12][a]	This work[c]
Technology	0.14 μm	90 nm	0.13 μm	0.13 μm	0.13 μm
Architecture	SRO	PDRO	Relaxation	Relaxation	PDRO
Frequency	1.28 MHz	5.12 MHz	5.65 MHz	2.52 MHz	4 MHz
Supply	900 mV	300 mV	600 mV	800 mV	140 mV
Power	440 nW	24 nW	720 nW	320 nW	3.6 nW

[a] Measurement results. [b] Simulation results.
[c] Post-layout simulation results.

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