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Simulation of four-quadrant four transistors synapse analog multiplier

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ABSTRACT

In this paper, a new implementation of CMOS four-quadrant analogue synapse multiplier circuit for analogue signal processing will be proposed. Especially, it can be used for multi-layer perceptron neural networks. The proposed multiplier is composed of only four transistors and it will multiply two input currents and produces an output current. The global multiplier circuit consists of 10 transistors, but only four of them will be implemented inside the synapse, while the others will be implemented inside the input and the neuron. The main characteristics of the proposed circuit are the small silicon area and the low power consumption. A comparison among some other multipliers will be presented.

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Analogue multipliers; analogue signal processing; neural networks; synapses; CMOS VLSI implementation

1. Introduction

The four-quadrant multiplier is an important building block of analogue signal processing system. It has many applications in modulation, demodulation, frequency translation and neural network systems. The low power consumption and the small silicon area must be the key factors for designing an analogue multiplier, especially in multi-layer perceptron feed-forward neural networks, where the number of synapses can be in the range of thousands. For example, the multiplier is the basic element of the synapse implementation of a multi-layer perceptron feed forward neural networks, where the synapse multiplies the weight by the input. It must perform a linear product of two continuous signals x and y, yielding an output $z = Kxy$, where K is a constant with suitable dimension. The linearity, speed, supply voltage and power dissipation are the main metrics of performance.

A tutorial of multipliers suitable for signal processing (filter, mixers and modulators) and some of them for neural networks has been presented in [1]. A novel current mode CMOS four-quadrant analogue multiplier circuit is presented in [2], where the multiplication is implemented by four translinear loops with MOS transistors operating in weak inversion. A 340-μW high-speed, low-power four-quadrant CMOS current-mode multiplier has been presented in [3]. Kapanoglu and Yildirim present low-power four-quadrant CMOS analogue multiplier for artificial neural networks with 133 μW [4]. Sawigun and Mahattanakul present a 290-μW, a 1.5-V, wide-input range, high-bandwidth, CMOS four-quadrant analogue multiplier [5]. Chunhong and Zheng present a low-power CMOS analogue multiplier with 45 μw and poor linearity [6].

A feed forward multi-layer perceptron network with 64 inputs, 64 hidden neurons and 10 outputs is presented in [7]. It is based on the current-mode approach and weak inversion-biased MOS transistors. The chip can be employed in a chip-in-the-loop neural architecture learning. Hollis and Paulos present an example of artificial neural networks using MOS analogue multipliers [8], and Han presents a biologically inspired hardware implementation of neural networks with programmable conductance [9].

In [10], a nonlinear quadratic relation multiplier has been presented and it has been used for an analogue CMOS self-learning multi-layer perception chip trained by the back propagation algorithm; the chip has been fabricated and successfully tested. In [11], the multiplier proposed in [10] has been modified in order to get linear multiplier instead of nonlinear, in which the neural networks can learn and work better. The multiplier proposed in [11] has been fabricated and tested and presented in [12]. The multiplier in [12] has been improved in two ways, which are presented in [13] OTANPS and [14] OTANNO. In [13], the layout has been simplified and the number of transistors of each synapse is decreased by four transistors. In [14], the layout has been simplified and the number of transistors of each synapse is decreased by four transistors.

In this paper, the idea of the proposed multiplier is first discussed in [15] and is based on the current mode. The two inputs are currents and the multiplication output is current. It is composed of only four transistors to be implemented in the synapse. The silicon area and the power consumption have been decreased with respect to previous. [11–14]

2. Circuit description and equation

The proposed four-transistor synapse multiplier "FTSM" circuit is shown in Figure. Figure 1(a) shows the whole circuit, while Figure 1(b) shows the implementation in the multi-layer perceptron. The FTSM is composed of M1, M2, M3 and M4. The transistors Mn and Mp are implemented in the input module,

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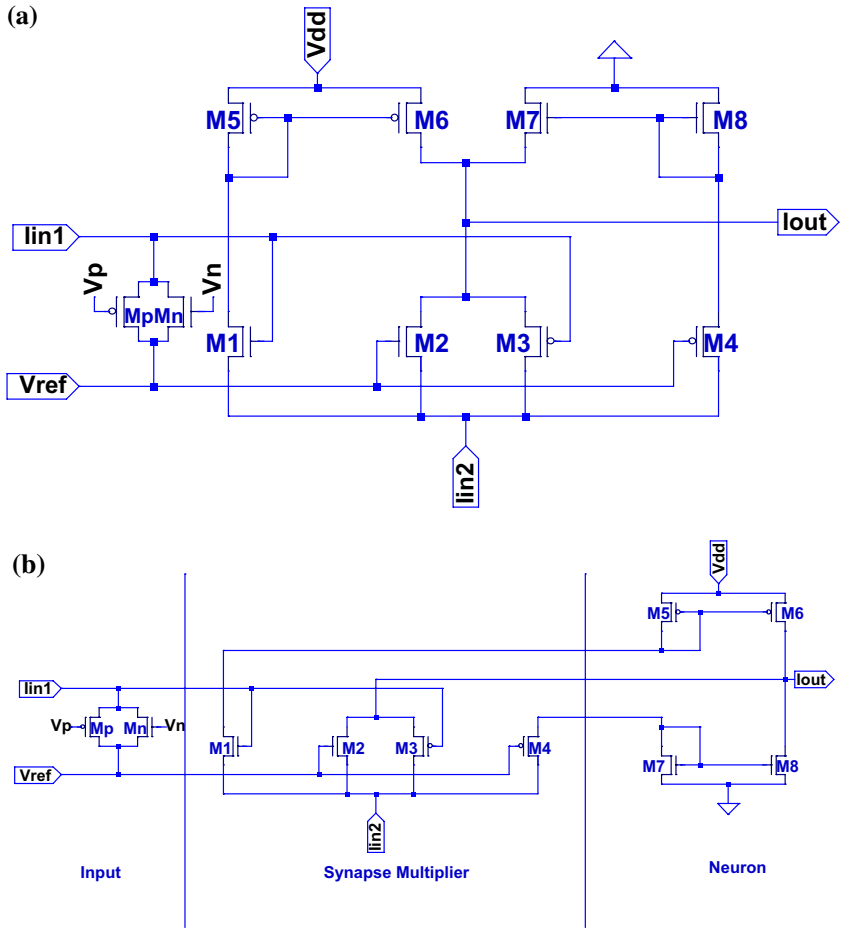

Figure 1. (a) is the proposed multiplier "FTSM" whole circuit; (b) is the implementation in the multi-layer perceptron which shows the synapse with four transistors.

while the transistors M5, M6, M7 and M8 are implemented in the neuron module.

The transistors M1, M2, M5 and M6 can be viewed as an N-channel two differential pair. The transistors M3, M4, M7 and M8 can be viewed as a P-channel two differential pair. If I_{in2} is positive (current from V_{dd} to ground) then the N-channel differential pair works or is on and P-channel differential pair doesn't work or is off, and vice versa if I_{in2} is negative then the N-channel differential pair doesn't work or is off and P-channel differential pair work or is on.

If the transistors M1 and M2 work in strong inversion region, then the relation between I_{outN} and I_{in2} is a square root and the relation between I_{outN} and I_{in1} is linear. By knowing the maximum current I_{in2}, we can design the dimensions of the transistors M1 and M2 in order to work in weak inversion and not in strong inversion, then the output current I_{outN} is given by [16]:

$$I_{outN} = I_{in2}\mathrm{Tanh}\left(\frac{V_{in} - V_{ref}}{2nVt}\right) \tag{1}$$

If $|V_{in} - V_{ref}| << 2nVt$ or V_{in} varies in the range $[V_{ref} - 2nVt: V_{ref} + 2nVt]$, then the Equation (1) can be rewritten as follows ($\tanh(x) = x$):

$$I_{outN} = I_{in2}\left(\frac{V_{in} - V_{ref}}{2nVt}\right) \tag{2}$$

where V_{in} is given by

$$V_{in} = I_{in1} * R_{Mp-Mn} + V_{ref} \tag{3}$$

R_{Mp-Mn} is the equivalent resistance derived from Mn and Mp (Mn and Mp must work in triode region), and V_{ref} (1.65 V) is the reference voltage and equals to half of V_{dd} (3.3 V). Then, I_{outN} is given by

$$I_{outN} = \frac{R_{Mn-Mp}}{2nVt}\left(I_{in1} * I_{in2}\right) \tag{4}$$

The relation between I_{outN} and I_{in2} and the relation between I_{outN} and I_{in1} are linear. The Equation (4) can be simplified as follows:

$$I_{outN} = a\left(I_{in1} * I_{in2}\right) \tag{5}$$

where the parameter a is constant and its value depends on the dimensions of Mn and Mp, I_{in1} can take positive and negative values and I_{in2} takes only positive values.

The same analysis and design can be done for the transistors M3 and M4, then the output current I_{outP} is given by

$$I_{outP} = I_{in2}\mathrm{Tanh}\left(\frac{V_{ref} - V_{in}}{2nVt}\right) \tag{6}$$

After simplifying,

$$I_{outP} = I_{in2}\left(\frac{V_{ref} - V_{in}}{2nVt}\right) = -\frac{R_{Mn-Mp}}{2nVt}\left(I_{in1} * I_{in2}\right) = -a\left(I_{in1} * I_{in2}\right) \tag{7}$$

where I_{in1} can take positive and negative values and I_{in2} takes only negative values. Then, I_{out} is given by

$$I_{out} = \begin{cases} I_{outN} \rightarrow I_{in2} > 0 \\ I_{outP} \rightarrow I_{in2} < 0 \end{cases} \tag{8}$$

By substituting Equations (5) and (7) in Equation (8), we get

$$I_{out} = \begin{cases} a\left(I_{in1} * I_{in2}\right) \rightarrow I_{in2} > 0 \\ -a\left(I_{in1} * I_{in2}\right) \rightarrow I_{in2} < 0 \end{cases} \tag{9}$$

I_{in1} can have positive or negative values in N-channel and P-channel differential pairs, while I_{in2} has positive values in N-channel and negative values in P-channel differential pairs. As a result, I_{out} is abbreviated to

$$I_{out} = a\left(I_{in1} * I_{in2}\right) \tag{10}$$

where I_{in1} and I_{in2} can have positive or negative values.

3. Simulation results

The circuit discussed above have been designed and simulated using WinSpice "Wspice3 Simulator for Windows" and using the parameters of the technology 0.35 μm, which is used for analogue implementation.

3.1. Circuit dimensions

The dimensions "width and the length" of the MOS transistors have been computed on the base of the technology parameters (e.g. the mobility of the electron, oxide capacitor, etc.). Also, the dimensions of the transistors are calculated and designed based on the following considerations:

- M1, M2, M3 and M4 are designed in a way to make the differential pairs work in weak inversion region;
- The dimensions of M1 and M2 must be equal and the dimensions of M3 and M4 must be equal;
- The value of the dimensions of the transistors M1 and M2 must be different than the dimensions of the M3 and M4 because of the mobility factor, where the mobility of N-channel transistors are bigger nearly three to four times than the mobility of P-channel transistors.
- M5, M6, M7 and M8 are designed as current mirror;
- Mn and Mp must be designed in order to work in triode region and to create linear resistor (the required resistance is 50 K).

The following table shows two designed dimensions (width μm/length μm) of each transistor in a way to work in weak inversion region with always *I*in1 = 1 and *I*in2 = 10 or *I*in2 = 1 μA. The supply voltage of the circuit is 3.3 V.

Circuit dimensions if I_{in2} = 10 μA				
M1	M2	M5	M6	Mn
25/2	25/2	4/4	4/4	1/10
M3	M4	M7	M8	Mp
100/2	100/2	4/4	4/4	3/10
Circuit dimensions if I_{in2} = 1 μA				
M1	M2	M5	M6	Mn
2.5/2	2.5/2	2/2	2/2	1/10
M3	M4	M7	M8	Mp
10/2	10/2	2/2	2/2	3/10

From the table, it is clear that to save the silicon area and in the same time to keep the circuit works in weak inversion, the decreasing factor must be the same for the dimensions of transistors M1, M2, M3 and M4 and for the current I_{in2}. The dimensions of transistors M1, M2, M3 and M4 and the current I_{in2} are decreased by the same factor 10.

Circuit area if I_{in2} = 10 μA			
Input	Synapse	Neuron	Total
Mn + Mp	M1 + M2 + M3 + M4	M5 + M6 + M7 + M8	
40 μm^2	500 μm^2	64 μm^2	604 μm^2
Total after the layout		=2.77 × 604	1673 μm^2
Circuit area if I_{in2} = 1 μA			
Input	Synapse	Neuron	Total
Mn + Mp	M1 + M2 + M3 + M4	M5 + M6 + M7 + M8	
40 μm^2	50 μm^2	16 μm^2	106 μm^2
Total after the layout		=2.77 × 106	293 μm^2

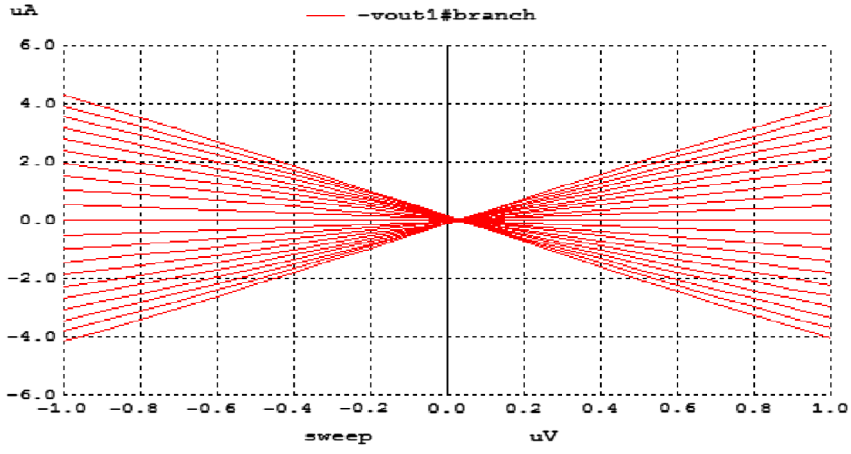

Figure 2. Weak inversion DC transfer characteristics I_{out} vs. I_{in1} with I_{in2} (10 μA) as a parameter.

3.2. DC transfer characteristics

The DC transfer characteristics are shown in Figures 2 and 3. I_{out} [−4u:+4u] vs. I_{in1} [−1u:+1u] with I_{in2} as a parameter varies in the range [−10u:+10u] with step 1u as shown in Figure 2. I_{out} [−4u:4u] vs. I_{in2} [−10u:+10u] with I_{in1} as a parameter varies in the range [−1u:+1u] with step 0.1u as shown in Figure 3.

Figures 2 and 3 show the DC transfer characteristics of the multiplier using the dimensions of transistors M1, M2, M3 and M4 for the current I_{in2} = 10 µA.

The DC transfer characteristics with I_{in2} = 1 µA are shown in Figures 4 and 5. Figure 4 (I_{out} [−0.4u:+0.4u] vs. I_{in1} [−1u:+1u] with I_{in2} as a parameter varies in the range [−1u:+1u] with step 0.2u) and Figure 5 (I_{out} [−0.4u:0.4u] vs. I_{in2} [−1u:+1u] with I_{in1} as

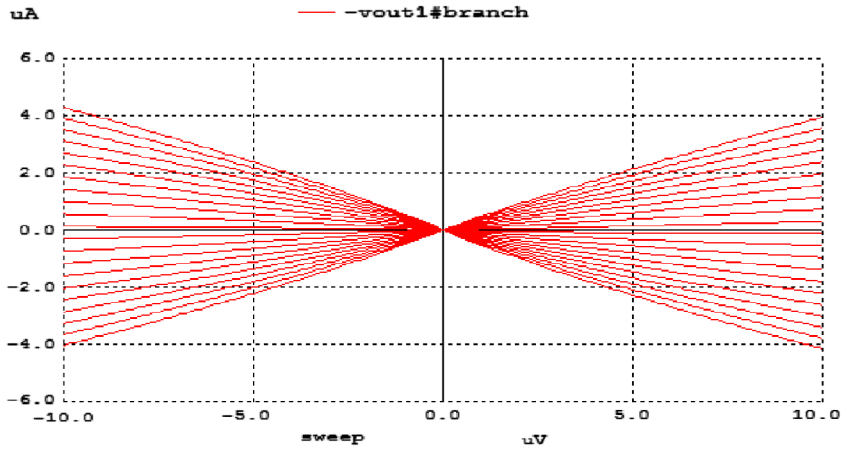

Figure 3. Weak inversion DC transfer characteristics I_{out} vs. I_{in2} (10µA) with I_{in1} as a parameter.

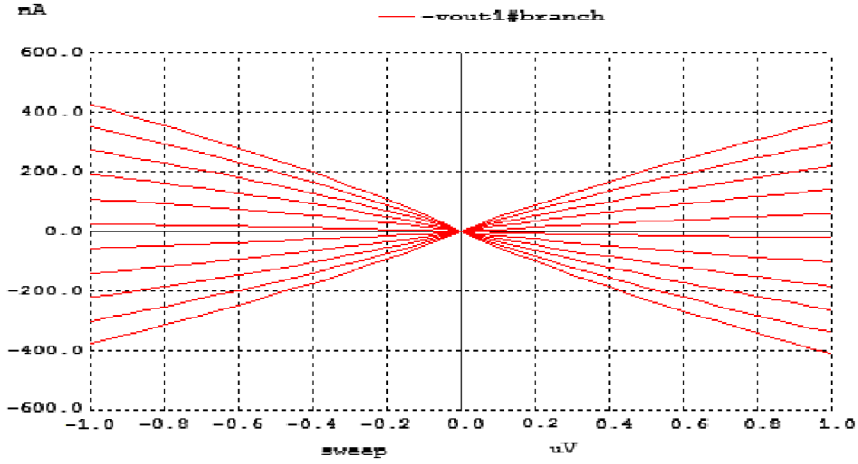

Figure 4. Weak inversion DC transfer characteristics I_{out} vs. I_{in1} with I_{in2} (1 µA) as a parameter.

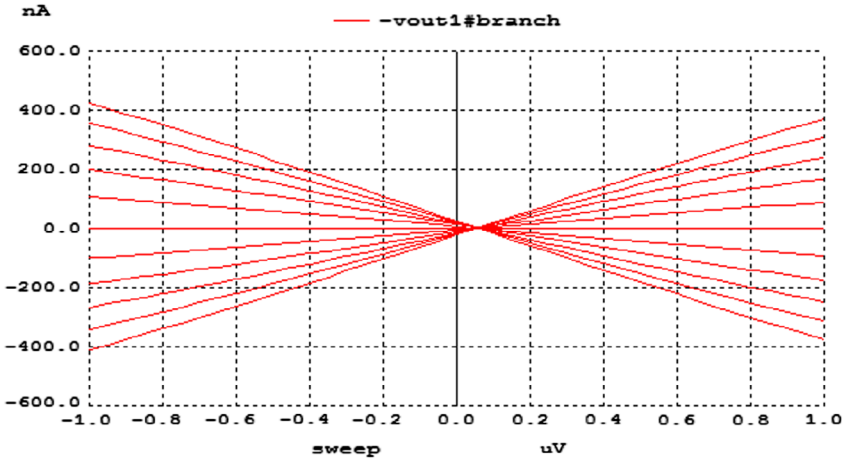

Figure 5. Weak inversion DC transfer characteristics I_{out} vs. I_{in2} (1 µA) with I_{in1} as a parameter.

a parameter varies in the range [−1u:+1u] with step 0.2u) shows the same simulation of Figures 2 and 3 but using I_{in2} = 1μA. It is noted that the output current I_{out} is decreased by the same factor 10.

3.3. Transient response

The transient response of the synapse multiplier circuit has been done to investigate the behaviour of the circuit in real-time multiplication. The simulation result is shown in Figures 6 and 7 (where I_{in2} = 10 μA) and Figure 8 (where I_{in2} = 1 μA).

The transient response of the multiplier simulation is shown in Figure 6, where the first input (I_{in1}) a sinusoidal current of 2 MHz frequency and peak to peak current 1 μA (a); the second input (I_{in2}) a sinusoidal current of 0.1 MHz frequency and peak to peak current 10 μA (b); the output result of the multiplier which is the multiplication of the two input signals (c).

Another simulation of the transient response of the multiplier simulation is shown in Figure 7. It is similar to Figure 6 but using (a) 0.2 MHz instead of 0.1 MHz of the second input (I_{in2}), (b) 10 MHz of the first input (I_{in1}) and 0.5 MHz of the second input (I_{in2}).

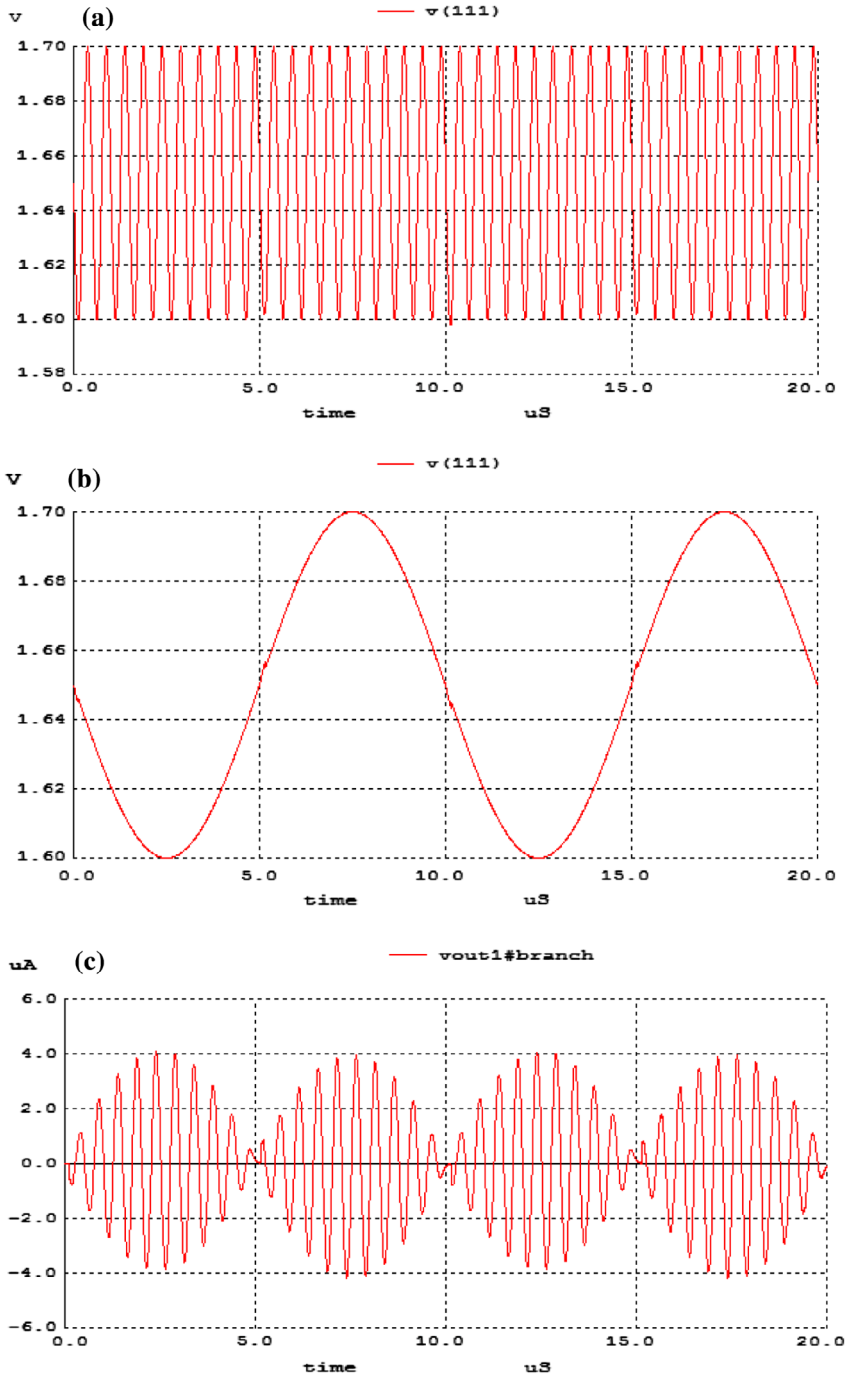

Figure 6. The transient response of the four-transistor multiplier simulation: (a) the first input (I_{in1}); (b) the second input (I_{in2}); (c) the output of the multiplier.

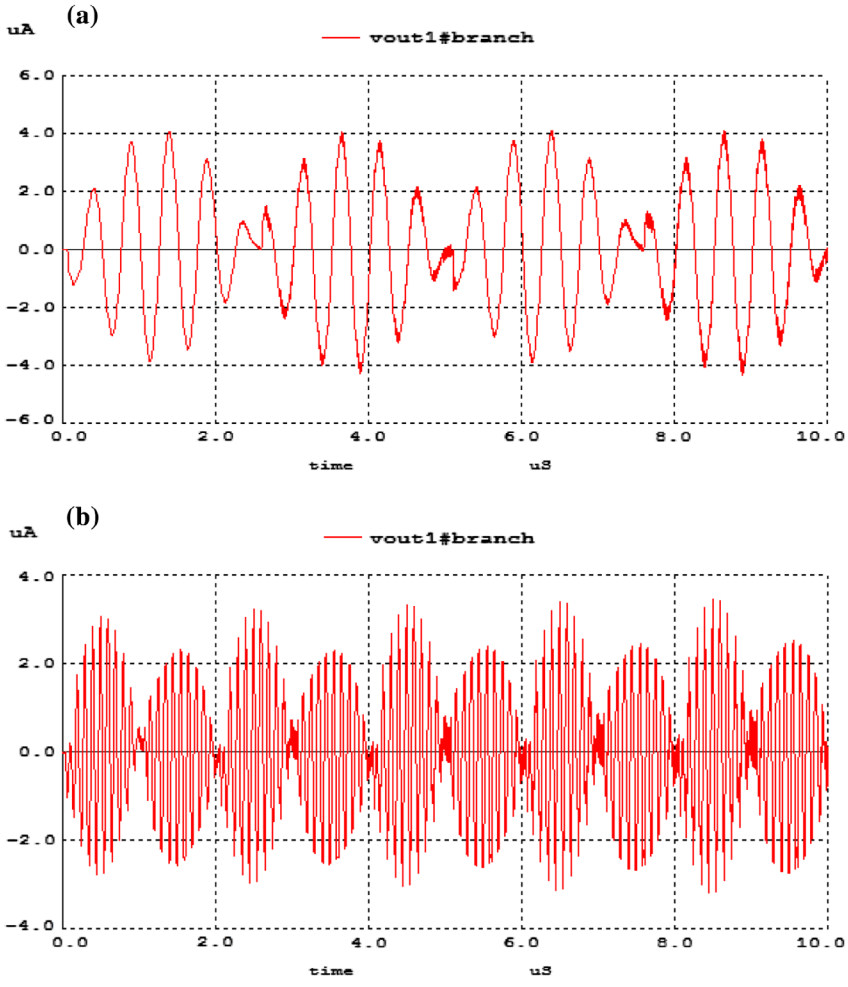

Figure 7. It is similar to previous figure but using different settings.

The transient response of the multiplier simulation is shown in Figure 8, where the simulation is done by feeding on the first input (I_{in1}) a sinusoidal current of 2 MHz frequency and peak to peak current 1μA and on the second input (I_{in2}) a sinusoidal current of 0.1 MHz frequency and peak to peak current 1 μA (a), while (b) it is the same as (a) but using 0.2 MHz instead of 0.1 MHz of the second input (I_{in2}).

3.4. Circuit consumption

The circuit consumption is measured by the maximum power dissipation "MPD" of the circuit, which is given by multiplying the total maximum current I_{max} derived from the power supply voltage V_{dd} times V_{dd}. If OTAN is on or works ($V_w > V_{ref}$), then OTAP is off and vice versa if ($V_w < V_{ref}$); then, MPD is given by

$$\text{MPD} = \text{MPD (M5)} + \text{MPD (M6)} \tag{11}$$

where,

MPD (M5) = $I_{max(M5)} \times V_{dd}$;
MPD (M6) = $I_{max(M6)} \times V_{dd}$.
Then, MPD becomes (V_{dd} = 3.3 V):

$$\text{MPD} = V_{dd}\left(I_{max(M5)} + I_{max(M6)}\right) = 3.3\,V * 4\,\mu\text{A} = 13.2\,\mu\text{W}$$

4. Comparison with similar versions

The next table shows the comparison among the proposed multiplier FTSM and our previous versions: the Non-linear multiplier [10], the Linear Multiplier [11], the OTANPS [13], and the OTANNO [14].

	Non -Linear multiplier [10]	Linear multiplier [11]	OTANPS [13]	OTANNO [14]	FTSM the current proposed
Input module # of transistors	0	0	0	8	2
Neuron module # of transistors	0	0	4	2	4
Synapse module # of transistors	14	14	10	4	4
Total area μm²	6059	4900	260	400	50
Total Consumption μW	30	15	47.85		13.2 μW
Inputs are	Voltages	Voltages	Voltages	Voltages	Currents
Output is	Voltage	Voltage	Voltage	Voltage	Current
Layout design	Complex			Easy	Easier
DC characteristics	Non linear	Linear	Linear	Linear	Linear
Time response	300 us			100 us	100 us

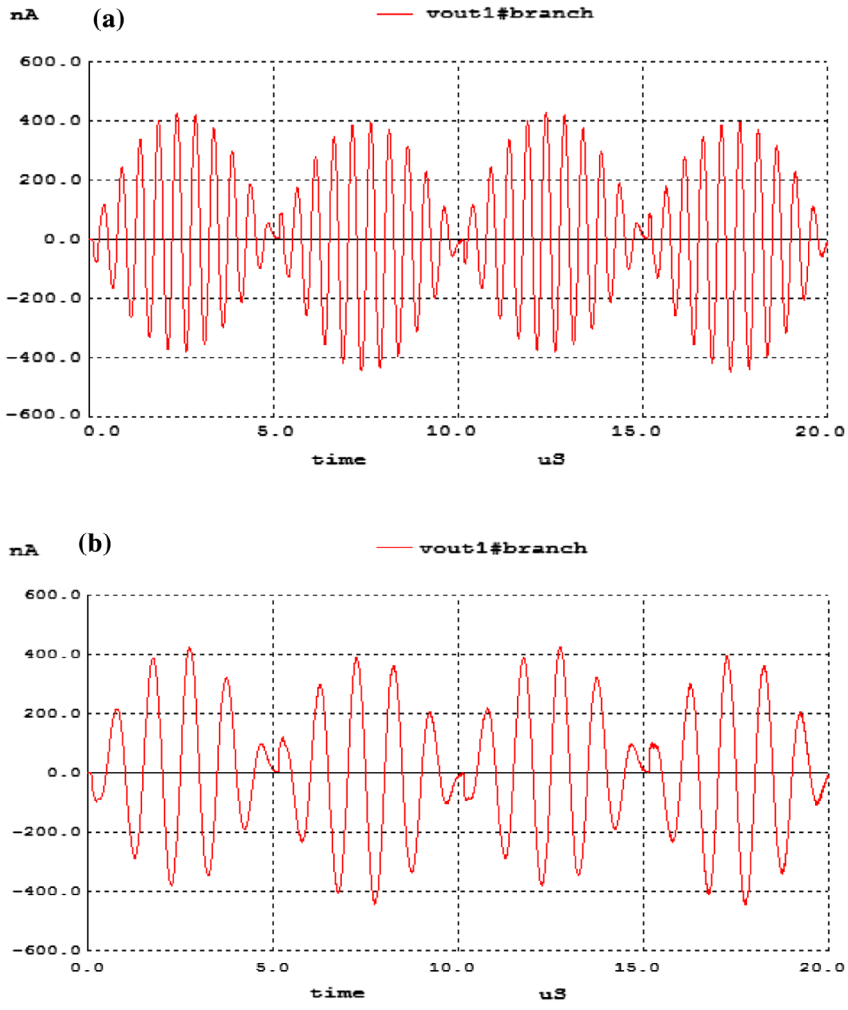

Figure 8. It is similar to previous two figures but using different settings.

5. Comparison with other multipliers

The next table shows a comparison between the proposed multiplier and others. The number of transistors is the main new feature of the proposed multiplier.

The multiplier	Power consumption	Number of transistors	Supply voltage	Usable frequency
This paper	13.2 µW	4	3.3 V	10 MHz
[17]	1.79 µW	37	0.6 V	57 kHz
[18]	113 µW	14	1.2 V	1 GHz.
[19]	207 µW	24	1.8 V	31.2 MHz
[20]	1.12 µW	>26	1.0 V	768 kHz
[21]	2.3 µW	16	1.0 V	2.8 MHz.
[22]	0.151 mW	–	–	–
[23]	–	34 + 8 resistors	–	100 MHz
[24]	1.56 µW	16	0.5 V	10 MHz
[25]	19.9 µW	10	0.75 V	10 MHz
[26]	6.4 mW	48	−2.5 → 2.5	5 MHz
[27]	25.14 mW	10 + 8 resistors + OpAmp	0.9v	72.45 MHz

6. Conclusions

In this paper, a new analogue four-quadrant Four-Transistors Synapse Multiplier "FTSM" is presented. The multiplier can be used especially in neural networks applications and in other signal processing operations. The multiplier circuit as whole circuit must be divided into three parts. The neural network input includes the first part and the neuron module contains the third part. Consequently, the synapse includes the second part, which has only four transistors for multiplications. The FTSM silicon area is 50 µm^2, and the power dissipation is 13.2 µW. The circuit simulations of the multiplier are presented.

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Disclosure statement

No potential conflict of interest was reported by the author.

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