A 336fs$_{rms}$ 0.89mW 200MS/s 5MHz Bandwidth 2-2 MASH ΔΣ Time-to-Digital Converter with Differential Time-Mode Arithmetic Units

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2020 IEEE International Symposium on Circuits and Systems
Virtual, October 10-21, 2020

Conventional GRO-TDC

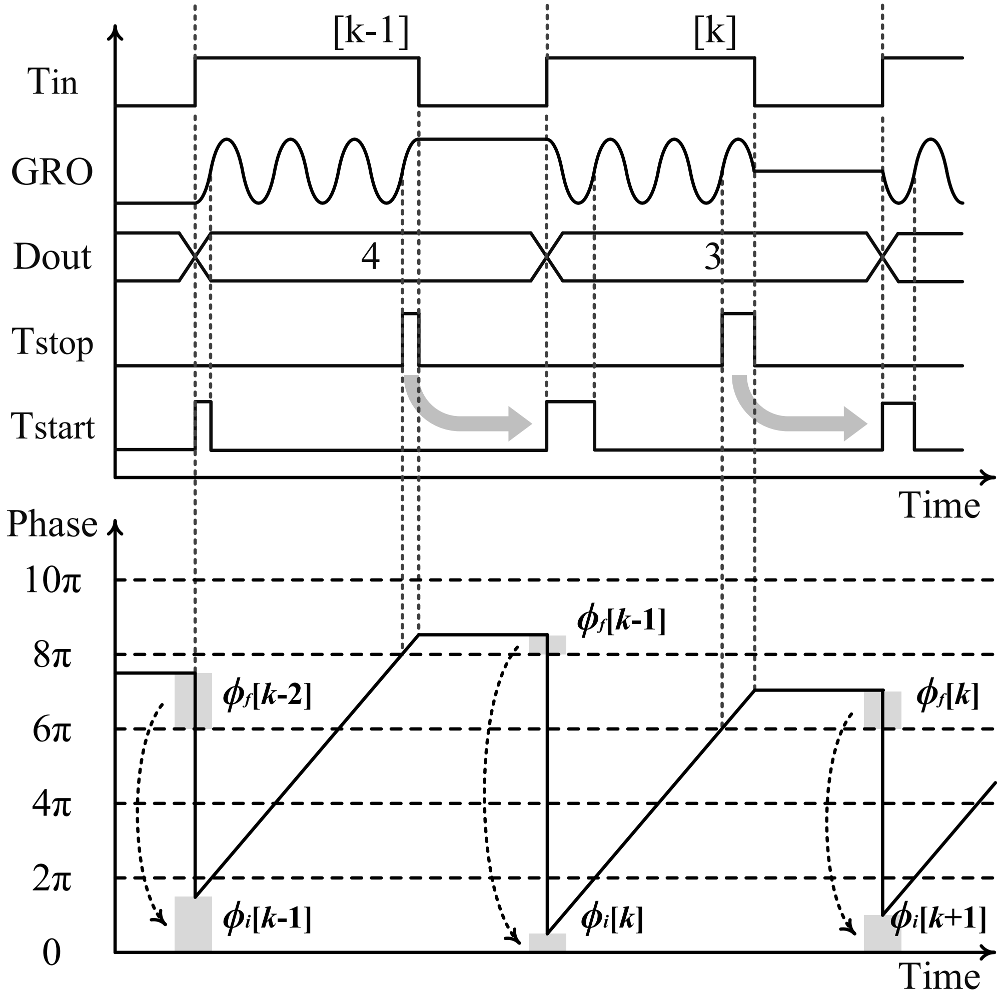


Fig. 2. Timing diagram

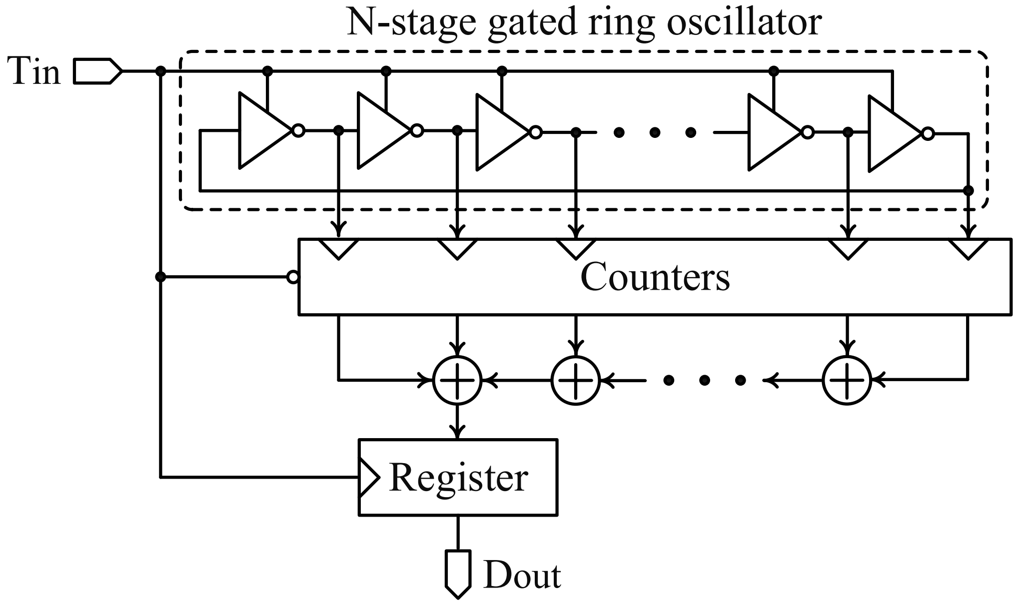


Fig. 1. Block diagram

$$\begin{cases} T_{start}[k] = T_{GRO} - T_{stop}[k-1] \\ T_{in}[k] = T_{GRO} * (D_{out}[k] - 1) + T_{start}[k] + T_{stop}[k] \end{cases}$$

the quantization error of conventional GRO-TDC

$$T_{e,1st}[k] = T_{stop}[k] - T_{stop}[k-1]$$

Single-loop 2nd-order GRO-TDC

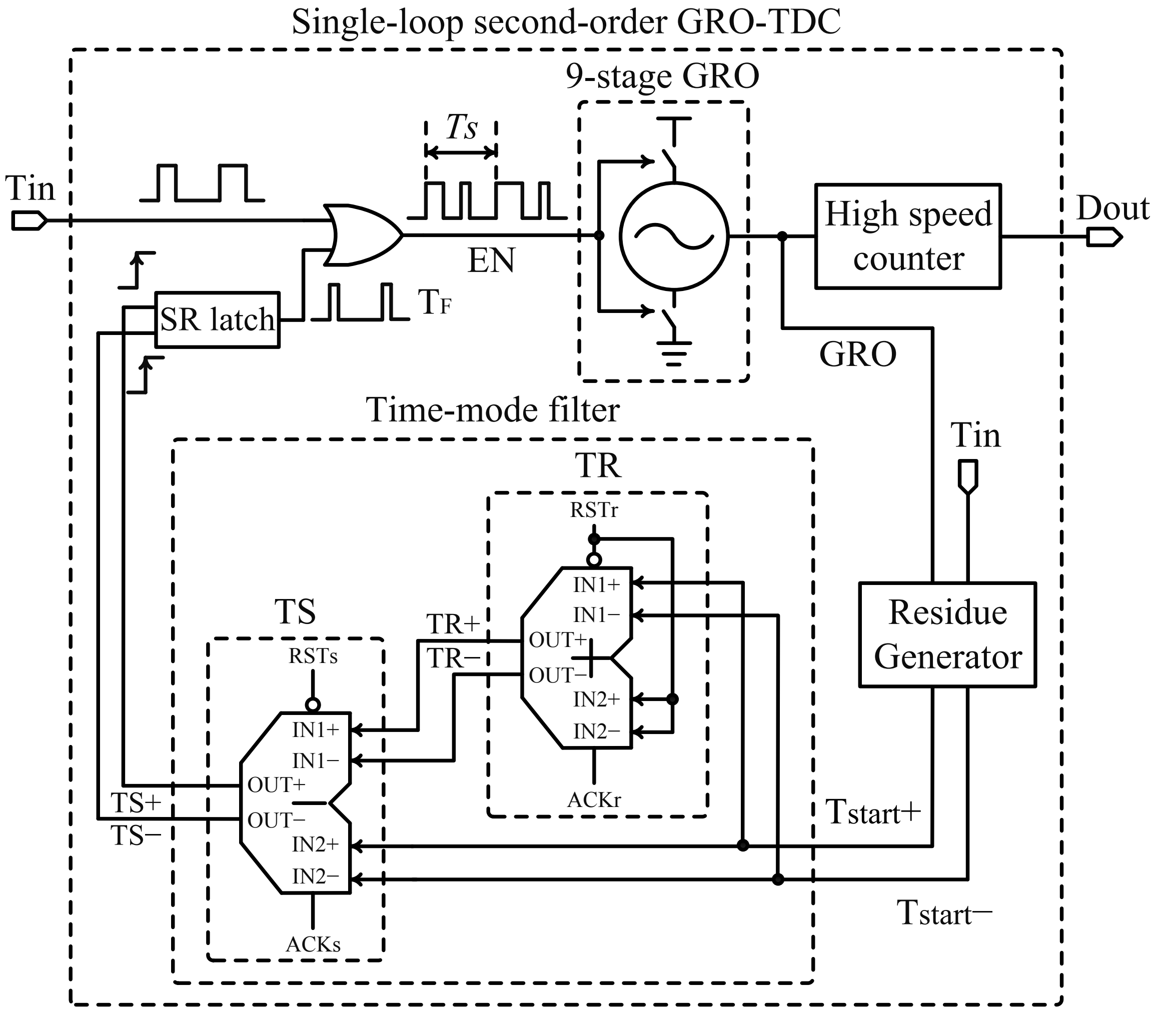


Fig. 1. Block diagram

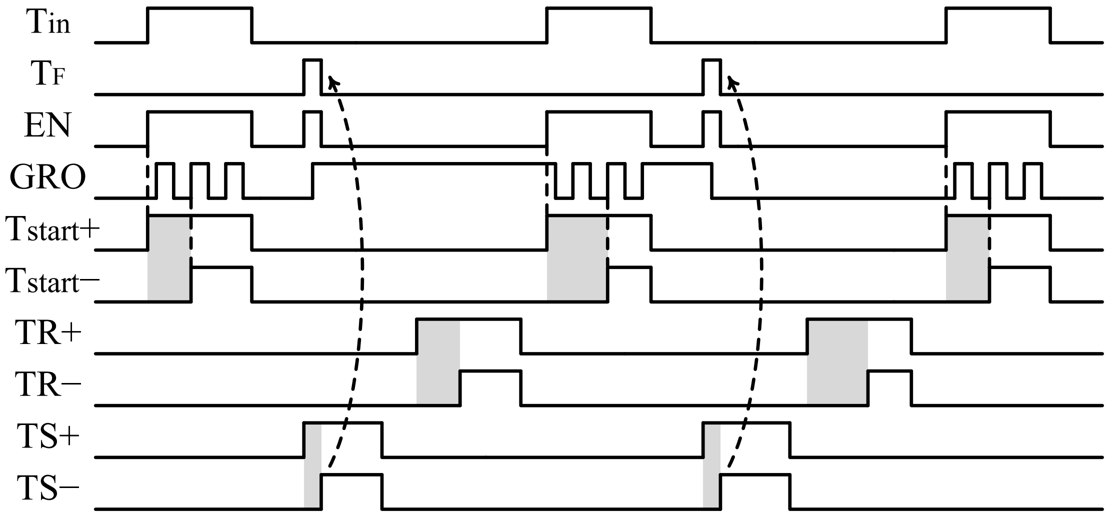


Fig. 2. Timing diagram

Structure

1. GRO-TDC: achieve 1st-order noise shaping
2. Time-mode error-feedback loop: extract the quantization error and feedback to the input via time-mode filter

Single-loop 2nd-order GRO-TDC

GRO-TDC $\begin{cases} T_{start}[k] = T_{GRO} - T_{stop}[k-1] \\ T_{in}[k] = T_{GRO} * (D_{out}[k] - 1) + T_{start}[k] + T_{stop}[k] \end{cases}$ ➡ $T_{e,1st}[k] = T_{stop}[k] - T_{stop}[k-1]$

➡ The difference operation on T_{stop} results in the 1st-order noise shaping of quantization noise in the frequency domain.

Time-mode filter $T_F = T_{start}[k] - T_{start}[k-1] = T_{stop}[k-1] - T_{stop}[k-2]$

Single-loop 2nd-order GRO-TDC $T_{e,2nd}[k] = T_{stop}[k] - 2T_{stop}[k-1] + T_{stop}[k-2]$

➡ The discrete-time second-order difference operation is obtained, corresponds with a second-order noise shaping in the frequency domain.

2-2 MASH ΔΣ TDC

The output $D_{out1}(z)$ of the first-stage can be expressed in z-domain as

$$D_{out1}(z) = T_{in}(z) + (1 - z^{-1})^2 Q_1(z)$$

The quantization error $-z^{-1}Q_1(z)$ of 1st-stage then feed to the input of 2nd-stage, thus the output $D_{out2}(z)$ of the 2nd-stage equals to

$$D_{out2}(z) = -z^{-1}Q_1(z) + (1 - z^{-1})^2 Q_2(z)$$

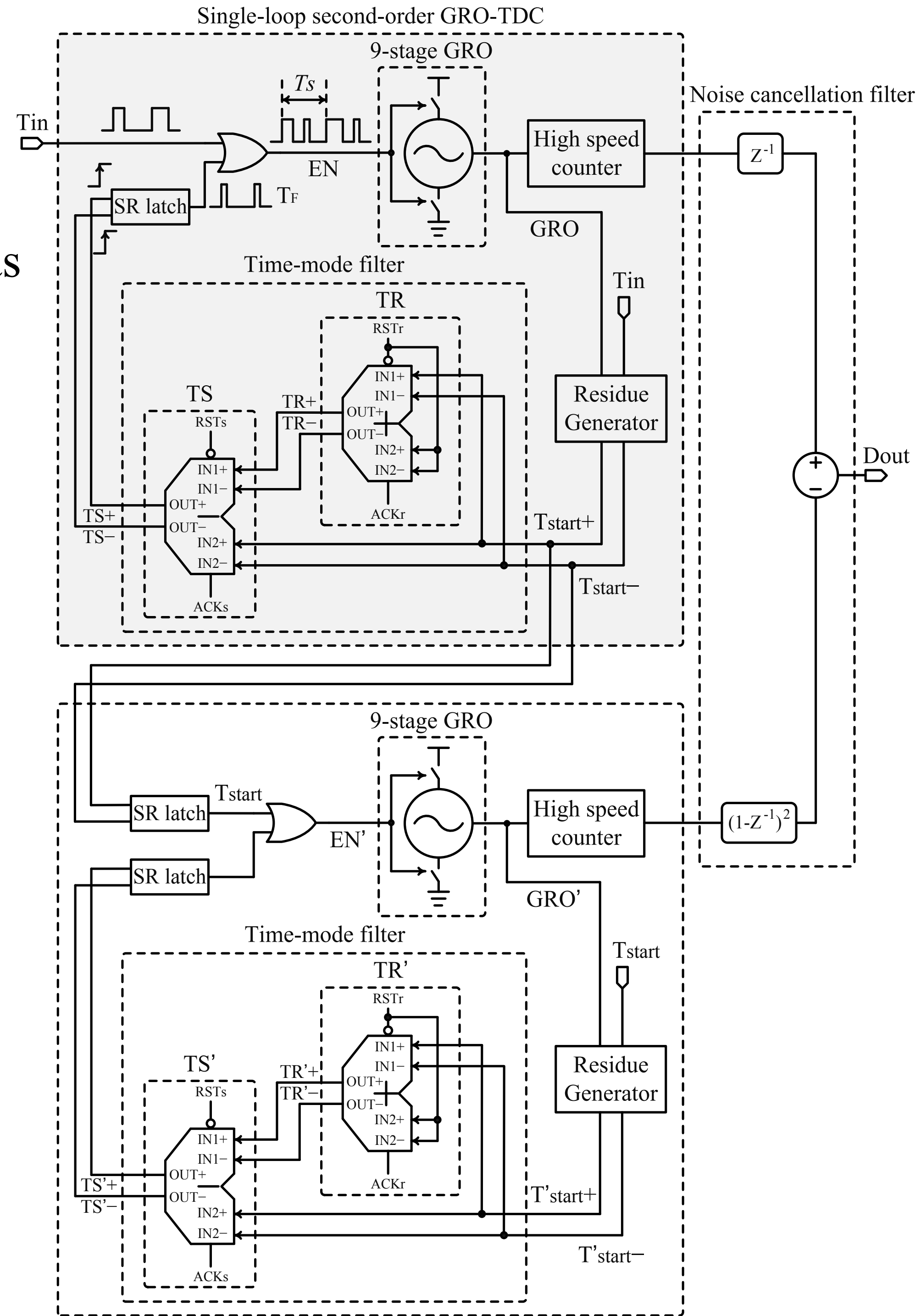
Two stages are cascaded together with the help of noise cancellation filter N_1 and N_2

$$N_1(z) = z^{-1}$$

$$N_2(z) = (1 - z^{-1})^2$$

Thus the output $D_{out}(z)$ of the proposed 2-2 MASH ΔΣ TDC can be expressed in z-domain as

$$D_{out}(z) = z^{-1}T_{in}(z) + (1 - z^{-1})^4 Q_2(z)$$



Time-mode arithmetic unit

The discharging time ΔT_{C1} of capacitor C1 during the duration of t_1 can be explained as follows

$$\Delta T_{C1} = t_1 + T_d + T_i - T_b$$

Note that the cross-connected input for the time variable t_2 makes the discharging time ΔT_{C2} of capacitor C2 to be

$$\Delta T_{C2} = T_d + T_i - T_b - t_2$$

The rising edge of ACK makes the capacitors C1 and C2 discharge again. The time interval between the OUT+ and OUT−, expressed T_{OUT}, will be equal to

$$T_{OUT} = (T_{FS} - \Delta T_{C2}) - (T_{FS} - \Delta T_{C1}) = t_1 + t_2$$

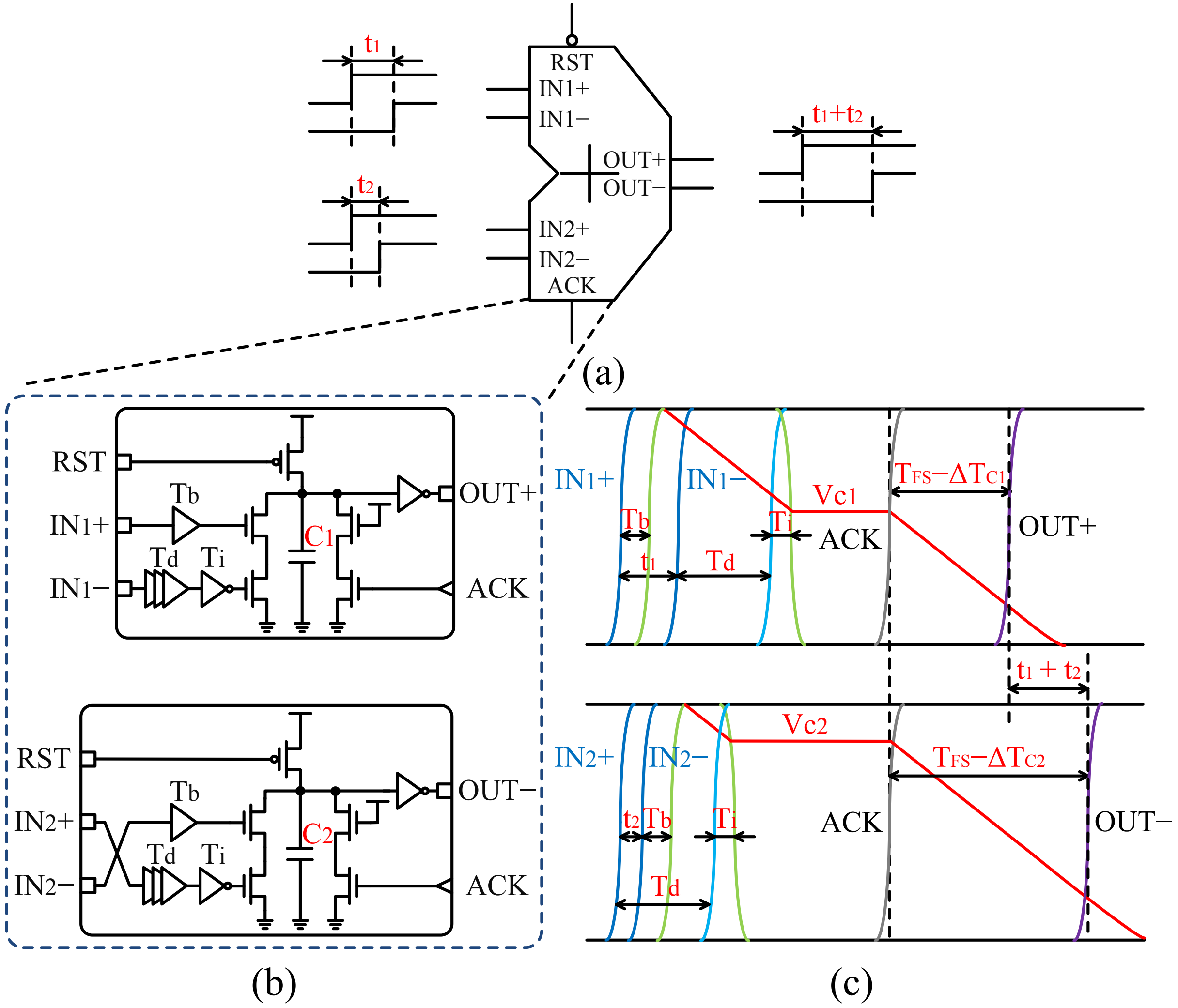


Fig. 1. (a) Symbol of the proposed time adder;
(b) Schematic of the time adder;
(c) Timing diagram of the time adder

Time Adder: $T_{OUT} = t_1 + t_2$

Fundamental Block for Time-Mode Signal Processing

- 2x Time Amplifier: $T_{OUT} = 2t_1$
- Time Register: $T_{OUT} = t_1$
- Time Subtractor: $T_{OUT} = t_1 - t_2$

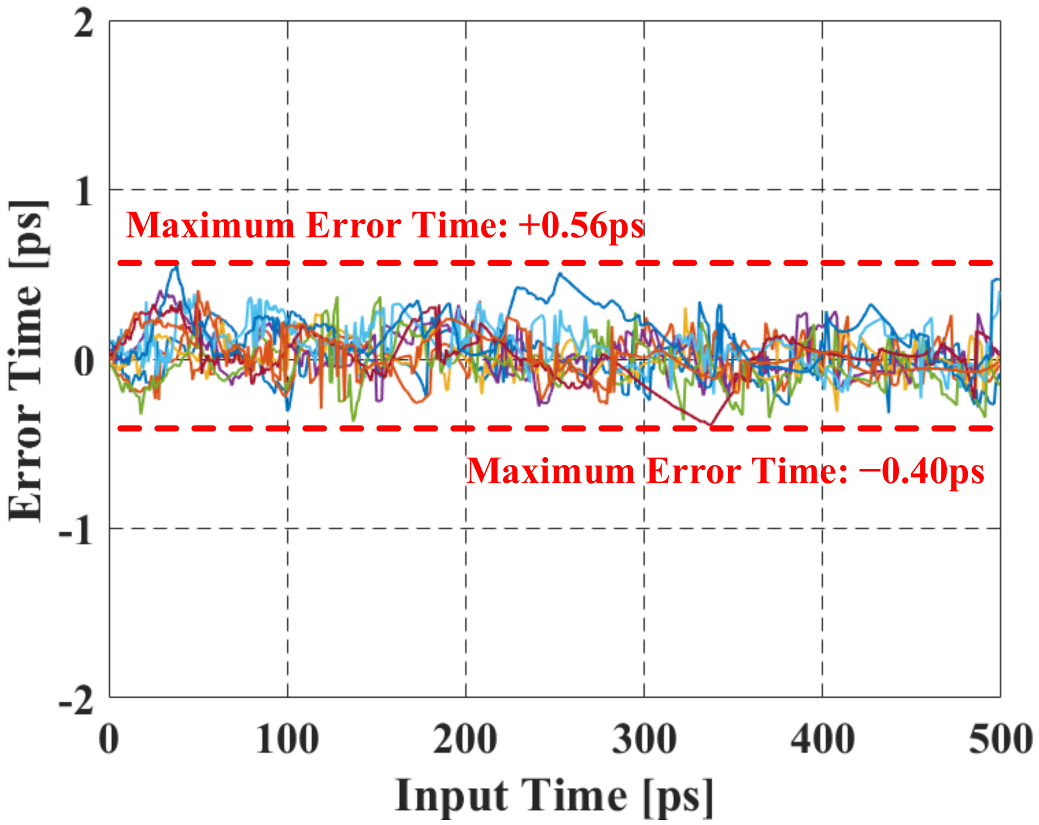


Fig. 1. Simulation results of the time register under various PVT conditions

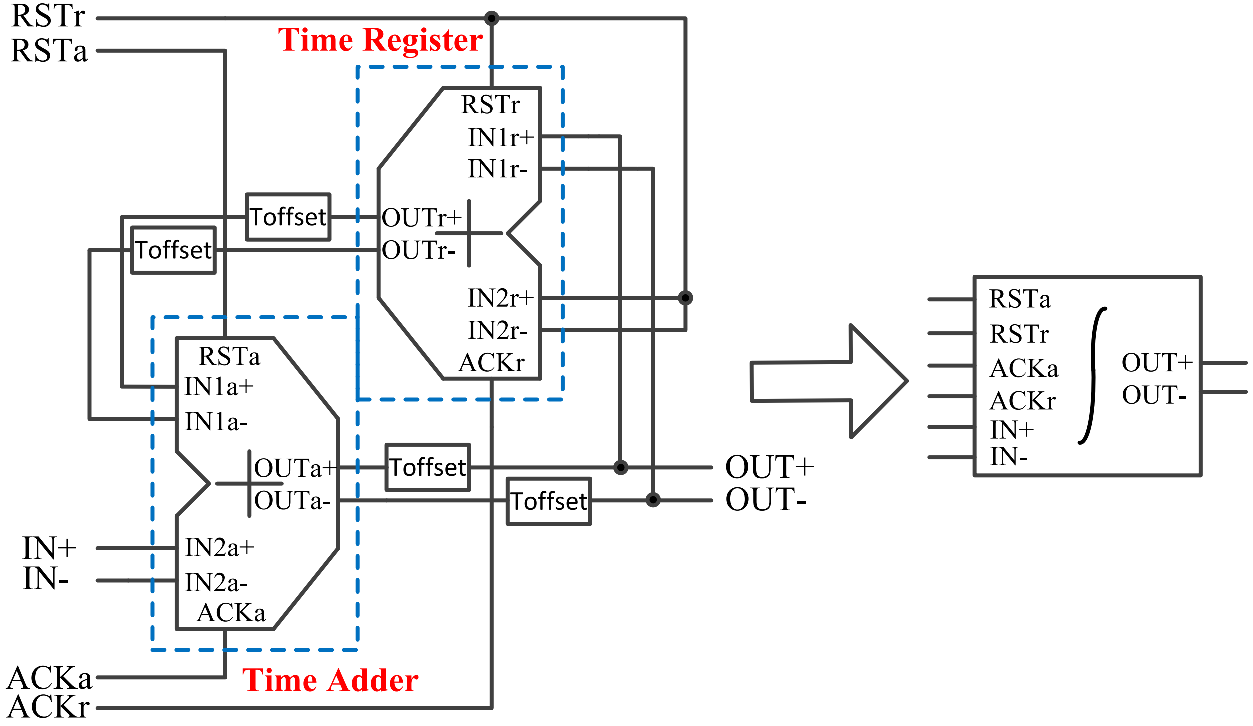


Fig. 2. one example of how to use a time adder and a time register to construct a time integrator

Multi-path Gated Ring Oscillator & Residue Generator

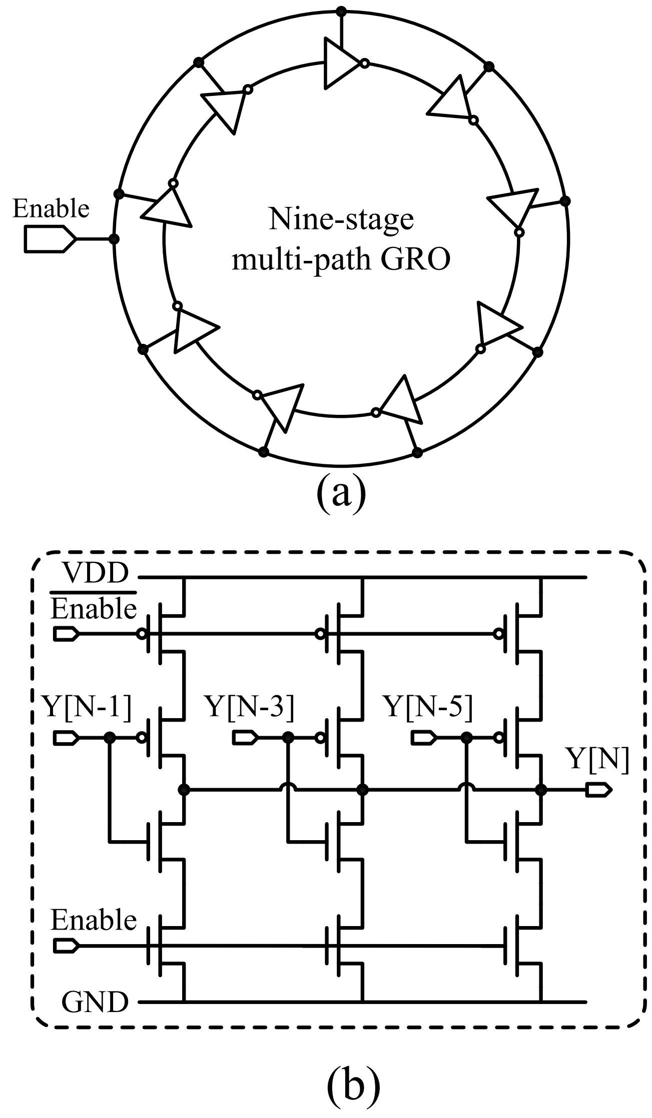


Fig. 1. Nine-stage multi-path GRO

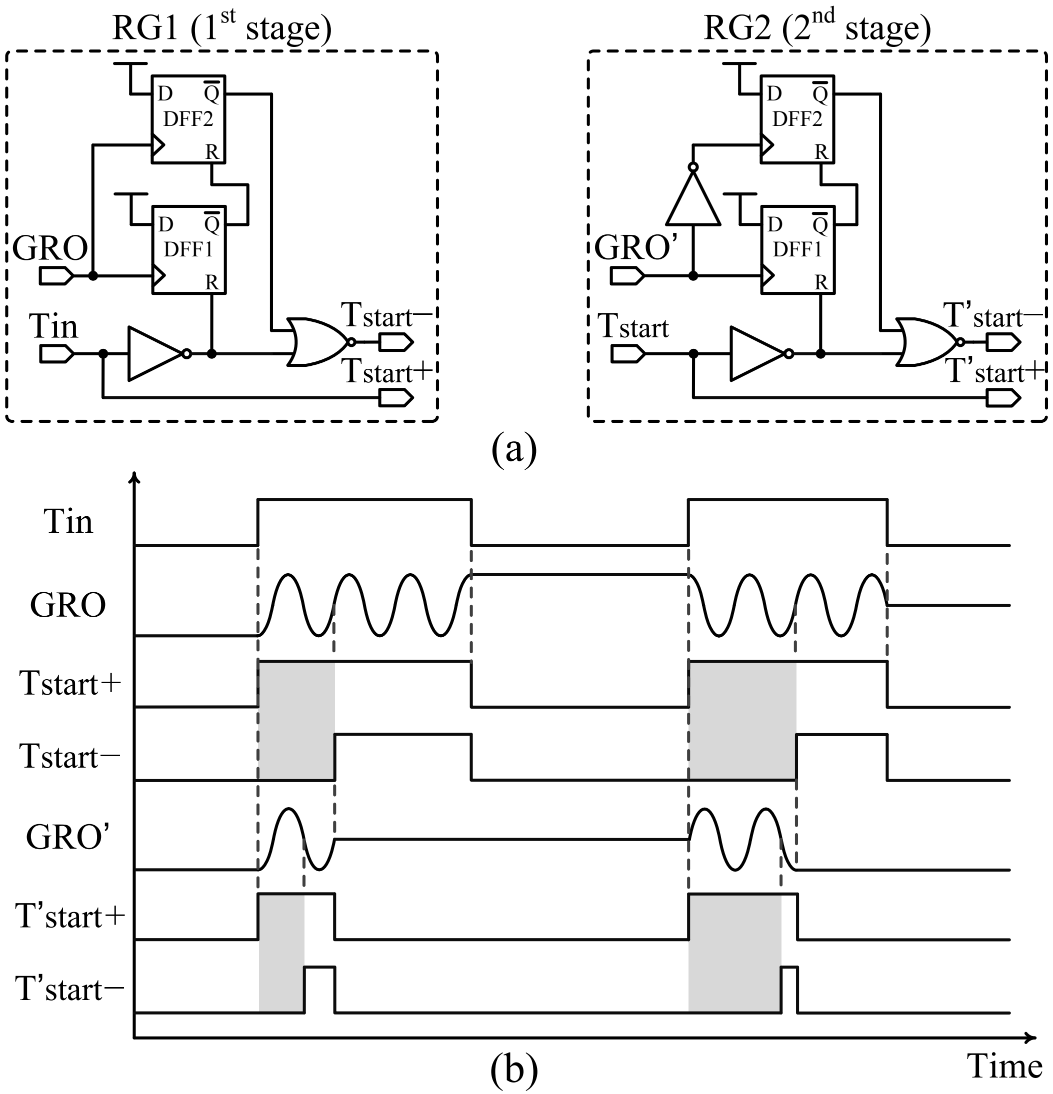


Fig. 2. Residue Generator

Simulation Results of 2-2 MASH ΔΣ TDC

Process: SMIC 65nm 1.2V CMOS

$T_{in,ptp}$ = 350ps, f_{in} = 928KHz @ f_s = 200MHz

Integrated Noise:
$T_{int,rms}$ = 336$\mathrm{fs_{rms}}$ @ 5MHz
$T_{int,rms}$ = 812$\mathrm{fs_{rms}}$ @ 10MHz

Equivalent Resolution:
Res. = 1.2ps @ 5MHz
Res. = 2.9ps @ 10MHz

Figure of Merit:
FoM = 210fJ/step @ 5MHz
FoM = 253fJ/step @ 10MHz

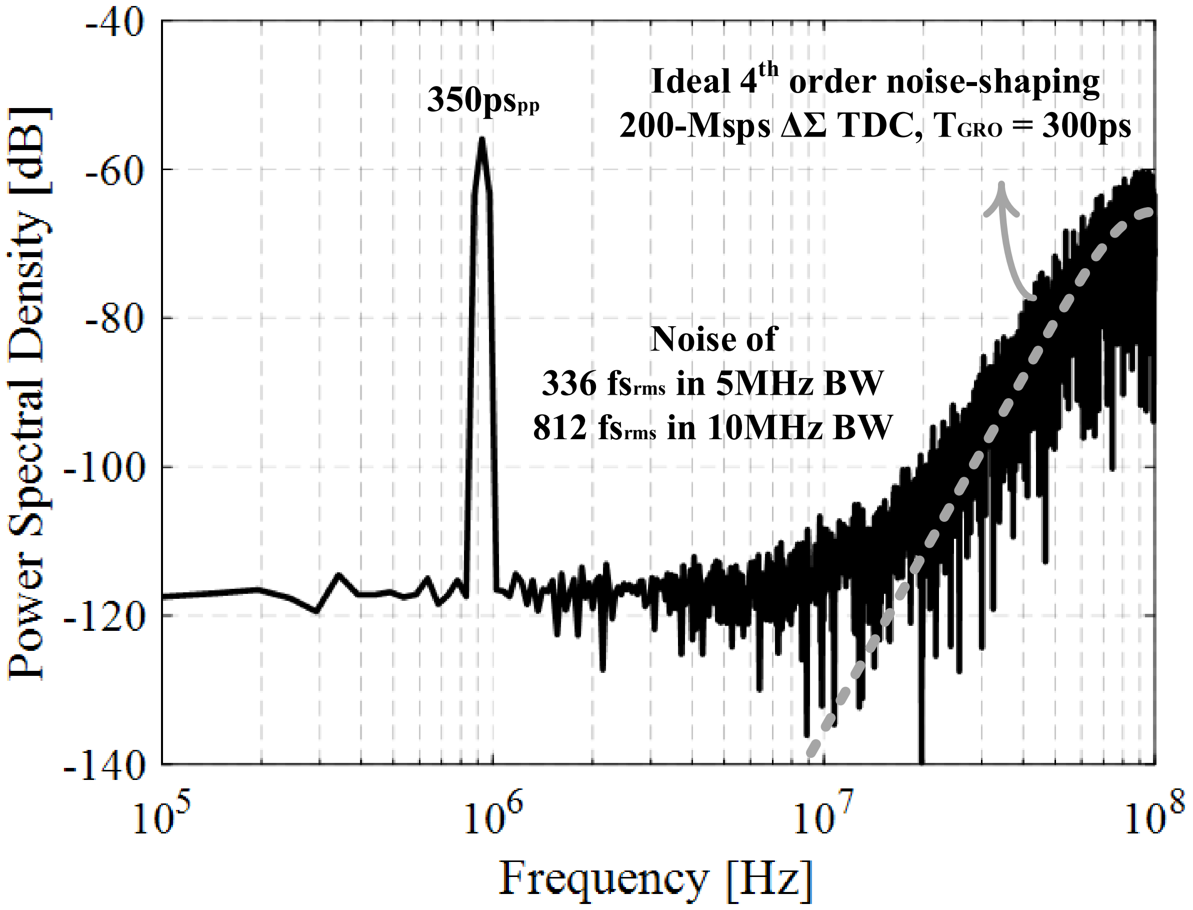


Fig. 1. Output spectrum for transistor-level simulation

TABLE I. PERFORMANCE COMPARISON WITH NOISE SHAPING TDCS

<table>
<tr><th></th><th>JSSC'14</th><th>JSSC'15</th><th>ISCAS'16</th><th colspan="2">This[a]</th></tr>
<tr><td>Scheme</td><td>SRO</td><td>MASH</td><td>CP-SAR</td><td colspan="2">MASH</td></tr>
<tr><td>Order</td><td>1st</td><td>4th</td><td>1st</td><td colspan="2">4th</td></tr>
<tr><td>Tech. (nm)</td><td>90</td><td>65</td><td>65</td><td colspan="2">65</td></tr>
<tr><td>Sampling (MHz)</td><td>500</td><td>150</td><td>200</td><td colspan="2">200</td></tr>
<tr><td>Bandwidth (MHz)</td><td>1</td><td>15</td><td>5</td><td>5</td><td>10</td></tr>
<tr><td>Int. noise (fs_{rms})</td><td>315</td><td>760</td><td>269</td><td>336</td><td>812</td></tr>
<tr><td>Resolution (ps)[b]</td><td>1.09</td><td>2.64</td><td>0.63</td><td>1.2</td><td>2.9</td></tr>
<tr><td>Range (ns)</td><td>12.5</td><td>5.4</td><td>3</td><td colspan="2">1</td></tr>
<tr><td>Power (mW)</td><td>2</td><td>3.52</td><td>0.9</td><td colspan="2">0.89</td></tr>
<tr><td>FOM (fJ/step)[c]</td><td>860</td><td>190</td><td>99</td><td>210</td><td>253</td></tr>
</table>

[a] Transistor-level simulation

[b] Resolution=$\sqrt{12}\times$Intergrated noise

[c] FOM=Power/(2$\times$Bandwidth$\times 2^{(\mathrm{SNDR}-1.76)/6.02}$)

Thanks for your attention