IEEE Xplore® Digital Library

ISCAS 2020
2020 IEEE International Symposium on Circuits and Systems
Virtual, October 10-21, 2020

CAS

Design of Power Efficient Posit Multiplier

Hao Zhang and Seok-Bum Ko

Department of Electrical and Computer Engineering
University of Saskatchewan, Canada

2020 IEEE International Symposium on Circuits and Systems
Virtual, October 10-21, 2020

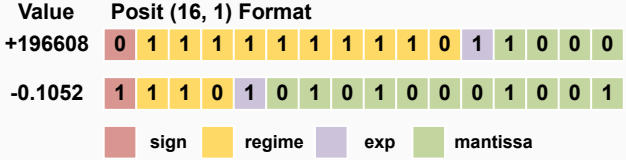
University of Saskatchewan

Table of Contents

Introduction

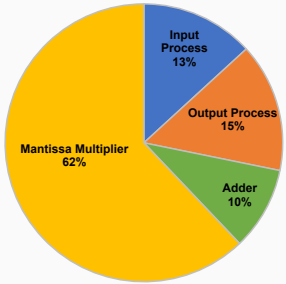
The Posit Number Format

- Posit designed as an alternative to IEEE754 for applications.
  - larger dynamic range, non-uniformed number distribution
  - deep learning (8/16-bit), scientific computing (32-bit)
- Dynamic component bit-width.
  - Mantissa range from 1 to $(nb - es)$-bit.
  - Hardware is designed with the maximum bit-width.
  - **Power wasted when computing small width mantissa**.



Power Reduction for Mantissa Multiplier

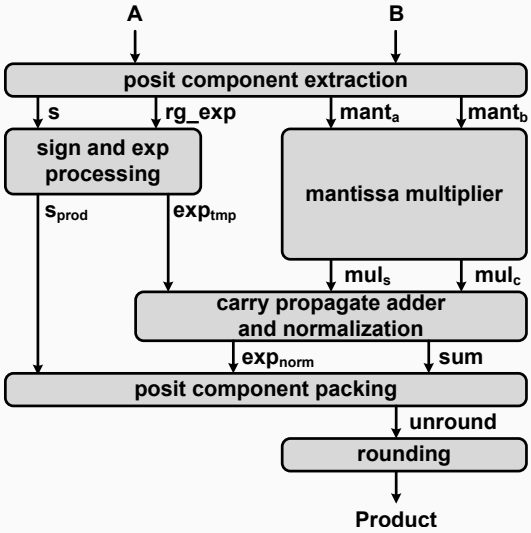
- Mantissa multiplier is the most power-consuming component.
- Focused on the optimization of mantissa multiplier:
  - **Decompose into multiple elements**.
  - **Only enable required elements**.
  - **Control generated during pre-processing**.



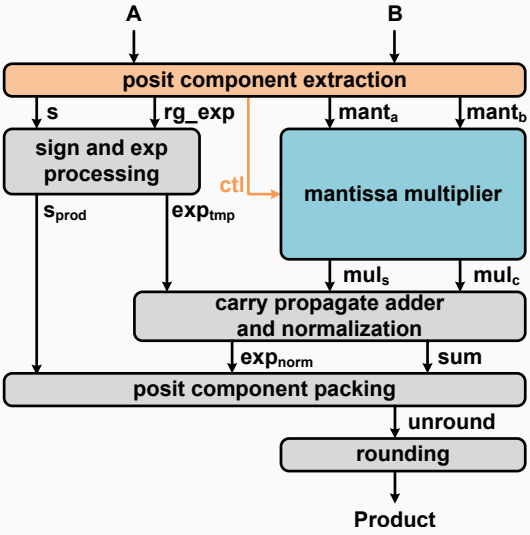
Power distribution of a Posit multiplier

The Proposed Posit Multiplier

The Baseline (Normal) Posit Multiplier



The Proposed Posit Multiplier

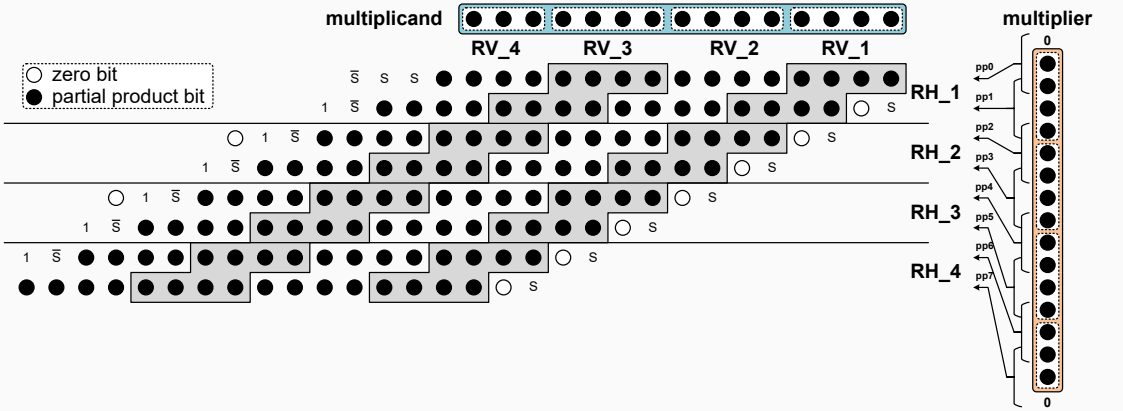


1. The generation of control signal.

2. The decomposition of mantissa multiplier.

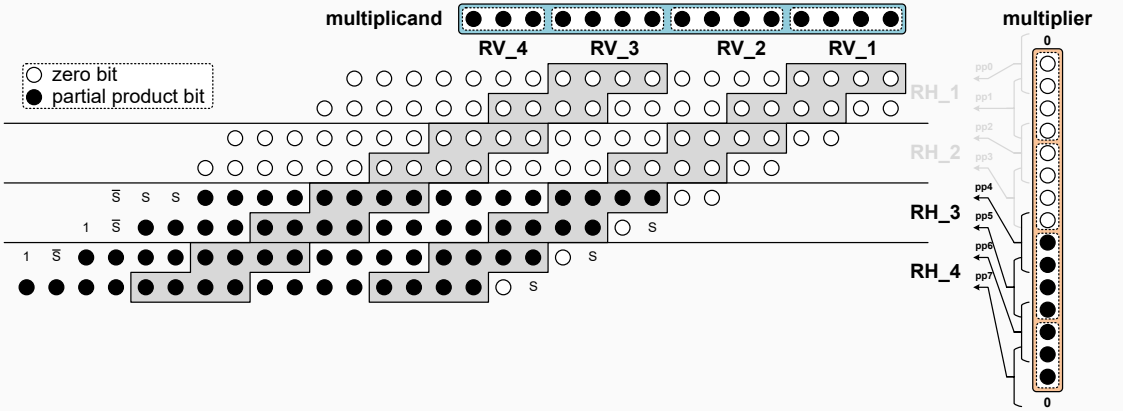
Decomposition of The Mantissa Multiplier

Multiplicand = 15-bit, Multiplier = 15-bit - All enabled



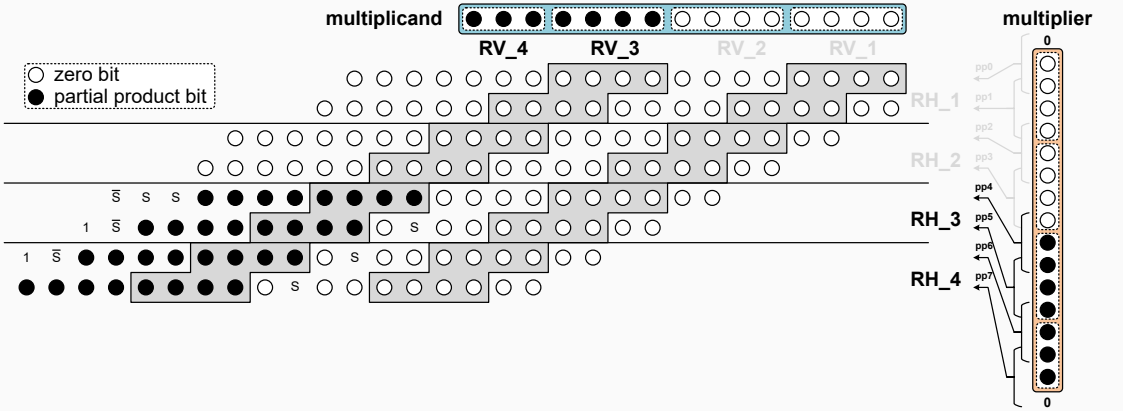
Decomposition of The Mantissa Multiplier

Multiplicand = 15-bit, Multiplier = 7-bit - Partially enabled



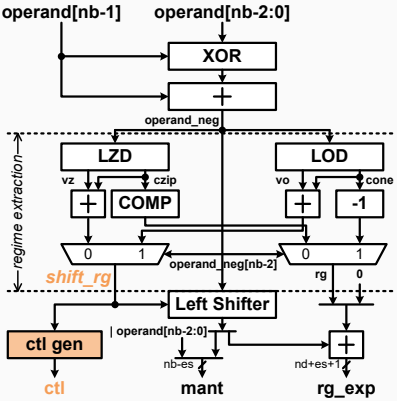
Decomposition of The Mantissa Multiplier

Multiplicand = 7-bit, Multiplier = 7-bit - Partially enabled



Generation of Control Signal

Posit Input Processing:



$mant\_bit = nb - es - shift\_rg$

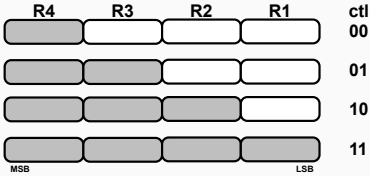
Truth Table to Generate Control Signal:

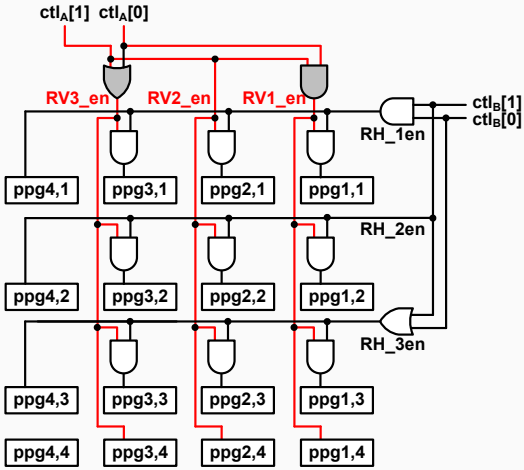
shift_rg	*ctl*	Enable				*shift_rg*	*ctl*	Enable			
		R_1	R_2	R_3	R_4			R_1	R_2	R_3	R_4
0000	xx					1000	01			✓	✓
0001	xx					1001	01			✓	✓
0010	11	✓	✓	✓	✓	1010	01			✓	✓
0011	11	✓	✓	✓	✓	1011	01			✓	✓
0100	10		✓	✓	✓	1100	00				✓
0101	10		✓	✓	✓	1101	00				✓
0110	10		✓	✓	✓	1110	00				✓
0111	10		✓	✓	✓	1111	00				✓

$ctl[1] = \overline{shift\_rg[3]}$ $\quad$ $ctl[0] = \overline{shift\_rg[2]}$

Apply Control Signal to Mantissa Multiplier

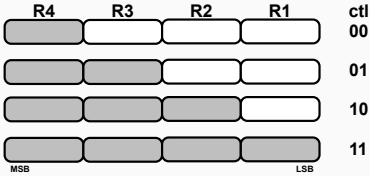
Column - Whether multiplicand is valid

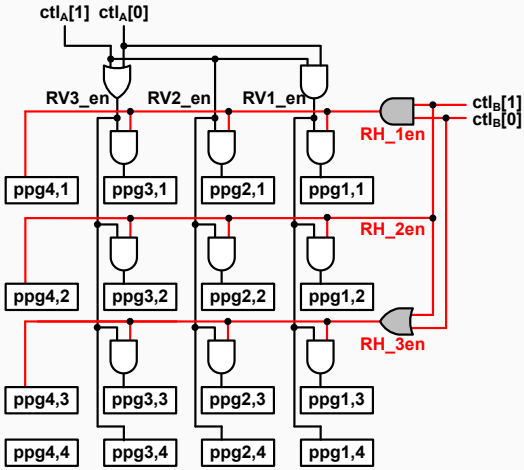




Apply Control Signal to Mantissa Multiplier

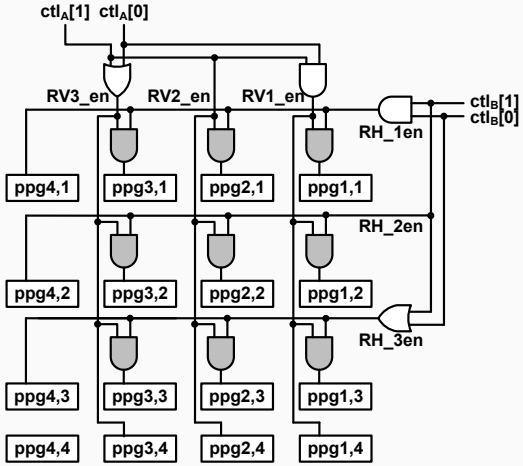
Row - Whether multiplier is valid





Apply Control Signal to Mantissa Multiplier

Each cell - When both operands are valid



Extension to Other Bit-Width

For posit formats other than posit (16, 1):

- For 8-bit cases, still use 4-bit granularity. But only 2 regions and thus 1-bit control signal.
- For 32-bit cases, we change to 8-bit granularity. Still 4 regions and 2-bit control signal as in 16-bit cases.
  - 4-bit granularity: similar power reduction, much larger area overhead.

For other group size:

- When using 2-bit granularity, more precise control can be achieved. However,
  - more area overhead;
  - radix-4 Booth multiplier uses 3-bit multiplier bits for encoding.

Results and Analysis

Module Comparison (Norm vs Prop)

Area and power comparison of each module for Posit(16,1) multipliers

Module	Area			Power		
	Norm	Prop	ratio	Norm	Prop	ratio
Input Process	7343	7344	+0.01%	1.32	1.33	+0.76%
Mantissa Multiplier	11506	12560	+9.16%	9.51	6.81	**-28.39%**
Final Adder	2422	2415	-0.28%	1.42	0.99	**-30.28%**
Output Process	3937	3926	-0.27%	1.72	1.70	-1.16%
Total	25234	26245	+4.00%	13.97	10.83	-22.48%

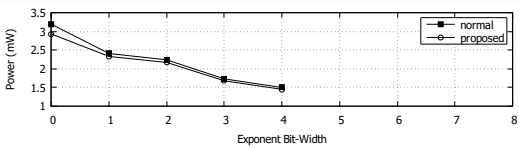
- Synopsys DC, STM-90nm with normal case (1.00V and 25°C)
- Reduced signal toggle rate in both multiplier and adder.

Comparison with IEEE754 and Normal Posit Multiplier

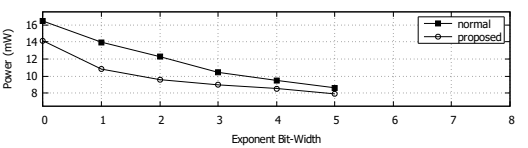
Design	Delay		Area		Power	
	ns	FO4†	μm^2	NAND2†	*mW*	ratio
IEEE-FLP8	0.67	15	3840	873	0.93	0.40
Posit(8,0)-Norm	1.27	28	7752	1762	3.19	1.09
Posit(8,0)-Prop	**1.29**	**29**	**7984**	**1814**	**2.93**	**1**
IEEE-FLP16	1.1	24	15963	3628	5.82	0.54
Posit(16,1)-Norm	1.67	37	25234	5735	13.97	1.29
Posit(16,1)-Prop	**1.68**	**37**	**26245**	**5964**	**10.83**	**1**
IEEE-FLP32	1.45	32	53214	12094	28.24	0.65
Posit(32,2)-Norm	2.16	48	81394	18498	55.60	1.27
Posit(32,2)-Prop	**2.20**	**49**	**83510**	**18979**	**43.64**	**1**

- On average 16% power reduction compared to normal designs.
- More expensive than IEEE multipliers, but, smaller bit-width Posit are enough.

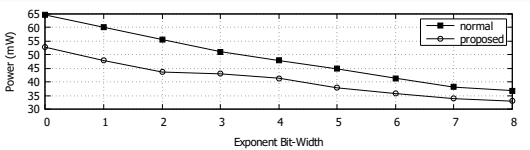
Power Comparison Under Various Exponent Bit-Width



8-bit Posit



16-bit Posit



32-bit Posit

- With more exp bit-width, gap is reduced due to reduced mantissa bit-width.
- In practical applications, Posit with small exp bit-width is enough.

Conclusion

Conclusion

- Power efficient posit multiplier architecture is proposed.
  - Mantissa multiplier is decomposed and the unused parts are disabled.
  - Control signal is generated from regime bit-width which is calculated during posit component extraction.
- An average of 16% power reduction can be achieved for 8/16/32-bit posit multipliers.
- In the future, power reduction method for posit adder and posit fused operations.

Acknowledgements

- This work was supported in part by the Natural Sciences and Engineering Research Council (NSERC) of Canada.

- This work was also supported in part by the Research and Development Program of MOTIE/KEIT (Developing Processor-Memory-Storage Integrated Architecture for Low Power, High Performance Big Data Servers, No. 10077609).

Thank You!

Please leave your questions in the Q&A forum or the discussion board.