SN74AUP1G17 Low-Power Single Schmitt-Trigger Buffer

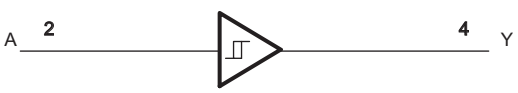
1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption (I_{CC} = 0.9 µA Maximum)
- Low Dynamic-Power Consumption (C_{pd} = 4.4 pF Typical at 3.3 V)
- Low Input Capacitance (C_i = 1.5 pF Typical)
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 5.1 ns Maximum at 3.3 V
- Suitable for Point-to-Point Applications

2 Applications

- Grid Infrastructure
- PC & Notebooks
- Tablets
- Factory Automation & Control
- Gaming
- Server

Logic Diagram (Positive Logic)
(DBV, DCK, DPW, DRL, DRT, DRY, and YZP Packages)



3 Description

The AUP family of devices is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity (see *AUP – The Lowest-Power Family* and *Excellent Signal Integrity*).

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

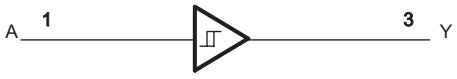
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G17DBV	SOT-23 (5)	1.60 mm × 2.90 mm
SN74AUP1G17DCK	SC70 (5)	1.25 mm × 2.00 mm
SN74AUP1G17DRL	SOT-5X3 (5)	1.60 mm × 1.20 mm
SN74AUP1G17DRY	SON (6)	1.00 mm × 1.45 mm
SN74AUP1G17DSF	SON (6)	1.00 mm × 1.00 mm
SN74AUP1G17YFP	DSBGA (4)	0.76 mm × 0.76 mm
SN74AUP1G17YZP	DSBGA (5)	0.89 mm × 1.39 mm
SN74AUP1G17DPW	X2SON (5)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)
(YFP Package)



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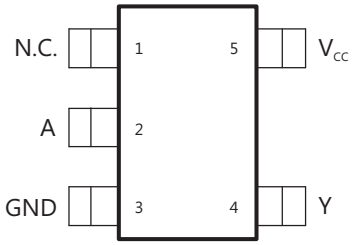
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (March 2010) to Revision J	Page
• Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table, see *Mechanical, Packaging, and Orderable Information* at the end of the data sheet	1

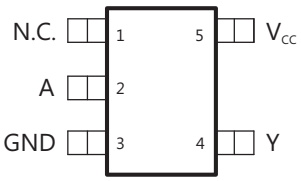
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View

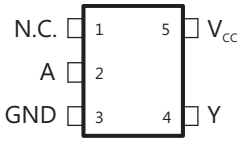


N.C. – No internal connection.

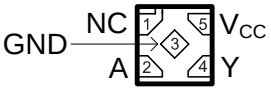
DCK Package
5-Pin SC70
Top View



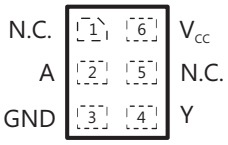
DRL Package
5-Pin SOT-5X3
Top View



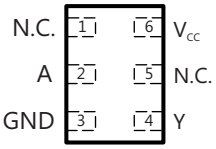
DPW Package
5-Pin X2SON
Top View



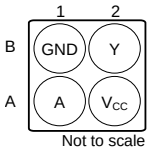
DRY Package
6-Pin SON
Top View



DSF Package
6-Pin SON
Top View

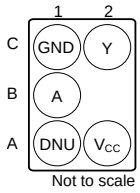


YFP Package
4-Pin DSBGA
Bottom View



See mechanical drawings for dimensions.

YZP Package
5-Pin DSBGA
Bottom View



DNU – Do not use

Pin Functions

PIN					I/O	DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YFP	YZP		
A	2	2	A1	B1	I	Input
DNU	—	—	—	A1	—	Do not use
GND	3	3	B1	C1	—	Ground
N.C.	1	1	—	—	—	No connection
		5				
V_{CC}	5	6	A2	A2	—	Positive supply
Y	4	4	B2	C2	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}(2)	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}(2)	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.
(2) Defined by the signal-integrity requirements and design-goal priorities

6.4 Thermal Information

THERMAL METRIC[1]		SN74AUP1G17								UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT-5X3)	DPW (X2SON)	DRY (SON)	DSF (SON)	YFP (DSBGA)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	267.2	284.1	294.7	489.2	347.8	386.2	179.3	146.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	191.9	208.5	132.5	226.3	237.7	192.9	2.8	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.1	103.1	143.6	352.9	210.6	242.2	58.3	39.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	83.0	76.6	14.5	38.2	64.4	28.9	1.1	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.8	102.3	144.1	352.1	210.6	241.9	58.6	39.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	150.8	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+} Positive-going input threshold voltage	T_A = 25°C	0.8 V	0.3		0.6	V
	T_A = –40°C to +85°C		0.3		0.6	
	T_A = 25°C	1.1 V	0.53		0.9	
	T_A = –40°C to +85°C		0.53		0.9	
	T_A = 25°C	1.4 V	0.74		1.11	
	T_A = –40°C to +85°C		0.74		1.11	
	T_A = 25°C	1.65 V	0.91		1.29	
	T_A = –40°C to +85°C		0.91		1.29	
	T_A = 25°C	2.3 V	1.37		1.77	
	T_A = –40°C to +85°C		1.37		1.77	
	T_A = 25°C	3 V	1.88		2.29	
	T_A = –40°C to +85°C		1.88		2.29	
V_{T-} Negative-going input threshold voltage	T_A = 25°C	0.8 V	0.1		0.6	V
	T_A = –40°C to +85°C		0.1		0.6	
	T_A = 25°C	1.1 V	0.26		0.65	
	T_A = –40°C to +85°C		0.26		0.65	
	T_A = 25°C	1.4 V	0.39		0.75	
	T_A = –40°C to +85°C		0.39		0.75	
	T_A = 25°C	1.65 V	0.47		0.84	
	T_A = –40°C to +85°C		0.47		0.84	
	T_A = 25°C	2.3 V	0.69		1.04	
	T_A = –40°C to +85°C		0.69		1.04	
	T_A = 25°C	3 V	0.88		1.24	
	T_A = –40°C to +85°C		0.88		1.24	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	T_A = 25°C		0.8 V	0.07		0.5	V
	T_A = –40°C to +85°C			0.07		0.5	
	T_A = 25°C		1.1 V	0.08		0.46	
	T_A = –40°C to +85°C			0.08		0.46	
	T_A = 25°C		1.4 V	0.18		0.56	
	T_A = –40°C to +85°C			0.18		0.56	
	T_A = 25°C		1.65 V	0.27		0.66	
	T_A = –40°C to +85°C			0.27		0.66	
	T_A = 25°C		2.3 V	0.53		0.92	
	T_A = –40°C to +85°C			0.53		0.92	
	T_A = 25°C		3 V	0.79		1.31	
	T_A = –40°C to +85°C			0.79		1.31	
V_{OH}	I_{OH} = –20 µA	T_A = 25°C	0.8 V to 3.6 V	V_{CC} – 0.1			V
		T_A = –40°C to +85°C		V_{CC} – 0.1			
	I_{OH} = –1.1 mA	T_A = 25°C	1.1 V	0.75 × V_{CC}			
		T_A = –40°C to +85°C		0.7 × V_{CC}			
	I_{OH} = –1.7 mA	T_A = 25°C	1.4 V	1.11			
		T_A = –40°C to +85°C		1.03			
	I_{OH} = –1.9 mA	T_A = 25°C	1.65 V	1.32			
		T_A = –40°C to +85°C		1.3			
	I_{OH} = –2.3 mA	T_A = 25°C	2.3 V	2.05			
		T_A = –40°C to +85°C		1.97			
	I_{OH} = –3.1 mA	T_A = 25°C		1.9			
		T_A = –40°C to +85°C		1.85			
	I_{OH} = –2.7 mA	T_A = 25°C	3 V	2.72			
		T_A = –40°C to +85°C		2.67			
	I_{OH} = –4 mA	T_A = 25°C		2.6			
		T_A = –40°C to +85°C		2.55			
V_{OL}	I_{OL} = 20 µA	T_A = 25°C	0.8 V to 3.6 V			0.1	V
		T_A = –40°C to +85°C				0.1	
	I_{OL} = 1.1 mA	T_A = 25°C	1.1 V			0.3 × V_{CC}	
		T_A = –40°C to +85°C				0.3 × V_{CC}	
	I_{OL} = 1.7 mA	T_A = 25°C	1.4 V			0.31	
		T_A = –40°C to +85°C				0.37	
	I_{OL} = 1.9 mA	T_A = 25°C	1.65 V			0.31	
		T_A = –40°C to +85°C				0.35	
	I_{OL} = 2.3 mA	T_A = 25°C	2.3 V			0.31	
		T_A = –40°C to +85°C				0.33	
	I_{OL} = 3.1 mA	T_A = 25°C				0.44	
		T_A = –40°C to +85°C				0.45	
	I_{OL} = 2.7 mA	T_A = 25°C	3 V			0.31	
		T_A = –40°C to +85°C				0.33	
	I_{OL} = 4 mA	T_A = 25°C				0.44	
		T_A = –40°C to +85°C				0.45	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
I_I A inputs	V_I = GND to 3.6 V	T_A = 25°C	0 V to 3.6 V			0.1	µA
		T_A = –40°C to +85°C				0.5	
I_{off}	V_I or V_O = 0 V to 3.6 V	T_A = 25°C	0 V			0.2	µA
		T_A = –40°C to +85°C				0.6	
ΔI_{off}	V_I or V_O = 0 V to 3.6 V	T_A = 25°C	0 V to 0.2 V			0.2	µA
		T_A = –40°C to +85°C				0.6	
I_{CC}	V_I = GND or (V_{CC} to 3.6 V), I_O = 0	T_A = 25°C	0.8 V to 3.6 V			0.5	µA
		T_A = –40°C to +85°C				0.9	
ΔI_{CC}	V_I = V_{CC} 0.6 V, I_O = 0	T_A = 25°C	3.3 V			40	µA
		T_A = –40°C to +85°C				50	
C_i	V_I = V_{CC} or GND		0 V		1.5		pF
			3.6 V		1.5		
C_o	V_O = GND		0 V		2.5		pF

6.6 Switching Characteristics: C_L = 5 pF

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		22.7		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	6.3	8	12.8	
				T_A = –40°C to +85°C	3.9		14.6	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	4.6	5.8	8.4	
				T_A = –40°C to +85°C	2.8		10	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	3.9	4.8	7.2	
				T_A = –40°C to +85°C	2.4		8.1	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	3.1	3.6	5.1	
				T_A = –40°C to +85°C	2		6.1	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	2.7	3	4.4	
				T_A = –40°C to +85°C	1.9		5.1	

6.7 Switching Characteristics: C_L = 10 pF

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		25.1		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	7.1	9.1	13.8	
				T_A = –40°C to +85°C	4.7		15.6	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	5.2	6.5	9.4	
				T_A = –40°C to +85°C	3.4		11	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	4.5	5.4	8	
				T_A = –40°C to +85°C	2.9		9	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	3.5	4.2	5.7	
				T_A = –40°C to +85°C	2.4		6.8	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	3.1	3.5	4.9	
				T_A = –40°C to +85°C	2.2		5.7	

6.8 Switching Characteristics: C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		27.6		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	7.8	10.1	14.8	
				T_A = –40°C to +85°C	5.3		16.7	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	5.8	7.4	10.3	
				T_A = –40°C to +85°C	3.9		12	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	5	6.1	8.8	
				T_A = –40°C to +85°C	3.4		10	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	4	4.7	6.4	
				T_A = –40°C to +85°C	2.8		7.5	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	3.5	4.1	5.4	
				T_A = –40°C to +85°C	2.6		6.2	

6.9 Switching Characteristics: C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A	Y	V_{CC} = 0.8 V	T_A = 25°C		35.1		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	10	13.1	18.1	
				T_A = –40°C to +85°C	7.5		19.8	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	7.4	9.6	12.9	
				T_A = –40°C to +85°C	5.6		14.9	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	6.4	7.9	11	
				T_A = –40°C to +85°C	4.8		12.4	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	5.2	6.1	7.9	
				T_A = –40°C to +85°C	4		9.3	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	4.6	5.3	6.7	
				T_A = –40°C to +85°C	3.6		7.7	

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.2	
			3.3 V ± 0.3 V	4.4	

6.11 Typical Characteristics

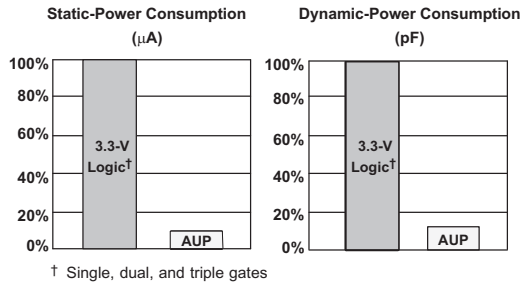


Figure 1. AUP – The Lowest-Power Family

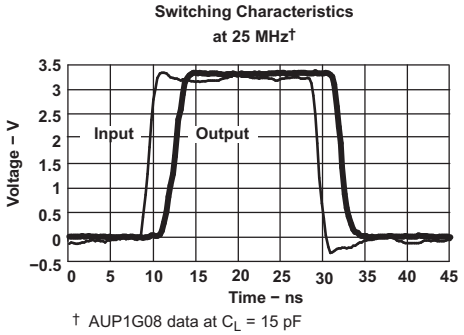
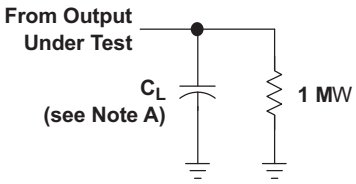


Figure 2. Excellent Signal Integrity

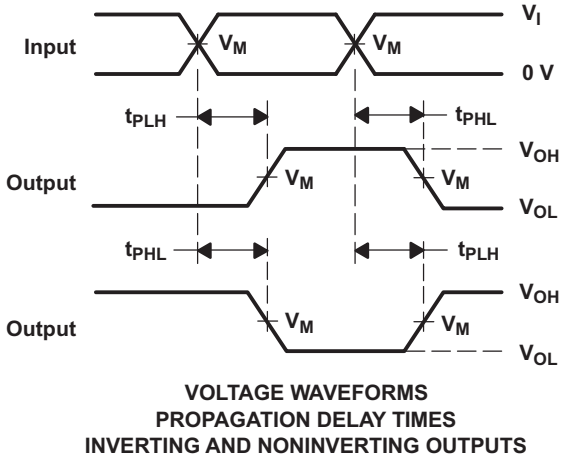
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Duration

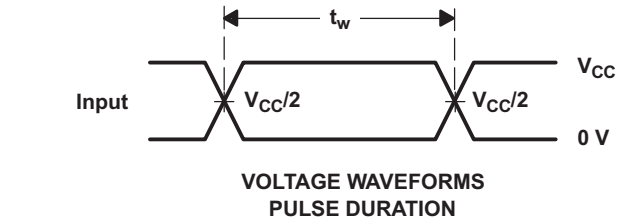


LOAD CIRCUIT

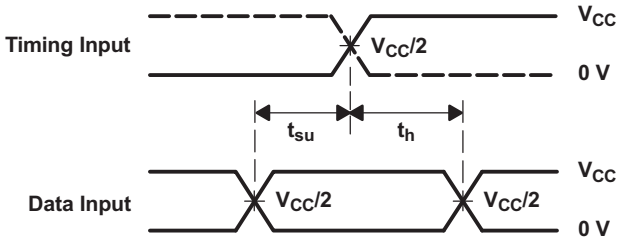
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

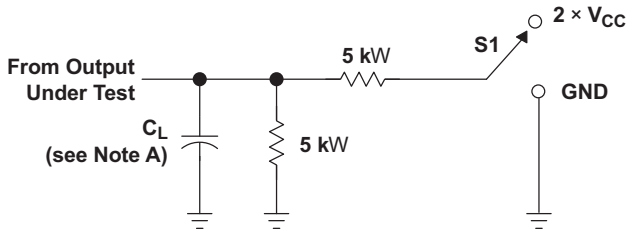


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 W, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit And Voltage Waveforms

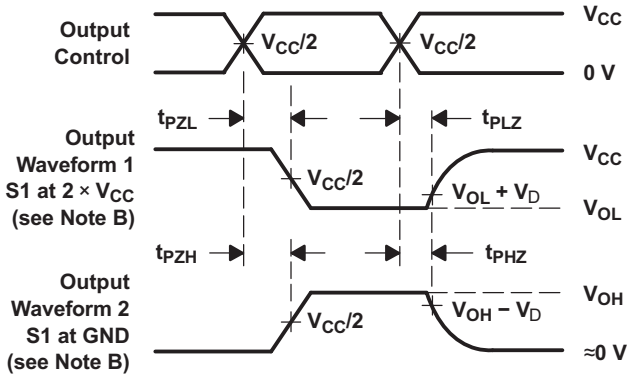
7.2 Enable and Disable Times



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	2 × V_{CC} GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_D	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit And Voltage Waveforms

8 Detailed Description

8.1 Overview

This device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

The AUP family is TI's premier solution to the industry's low power needs in battery-powered portable applications. This family assures a very low static and dynamic power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in an increased battery life.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device and excess power consumption.

8.2 Functional Block Diagrams

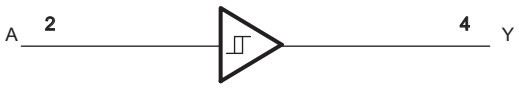


Figure 5. Logic Diagram (Positive Logic)
(DBV, DCK, DPW, DRL, DRT, DRY, and YZP Packages)

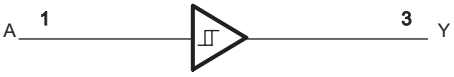


Figure 6. Logic Diagram (Positive Logic)
(YFP Package)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* table must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* table to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

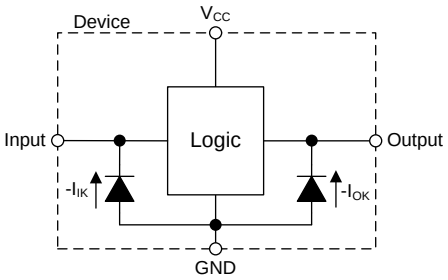


Figure 7. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics* table.

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings* table.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1G17 device.

Table 1. Function Table

INPUT A	OUTPUT Y
H	H
L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many situations in which a device needs to be initialized or held off for a short time at system turn-on. This application of the SN74AUP1G17 utilizes the delay created in an RC circuit to hold a line low for a short time when the system is first started, then maintains the line high while the system operates. The SN74AUP1G17 is ideal for this application because it must be tied directly to the primary supply for correct operation and is designed to draw minimal supply current during operation.

9.2 Typical Application

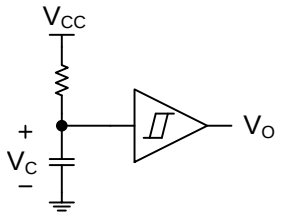


Figure 8. Turn-On Pulse Generator (Normally High Output)

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The drive strength also creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For specified high and low levels, see (V_{T+} and V_{T-}) in the *Electrical Characteristics* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Absolute Maximum Ratings* table at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed (I_O max) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

Typical Application (continued)

9.2.3 Application Curve

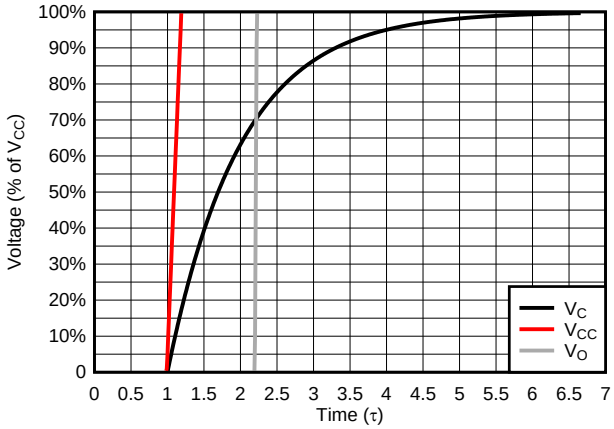


Figure 9. Simulated Output Response to Supply Turn-On

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 11 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

11.2 Layout Example

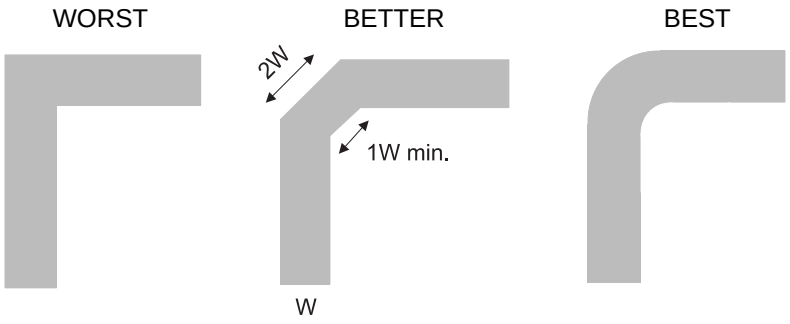


Figure 10. Trace Example

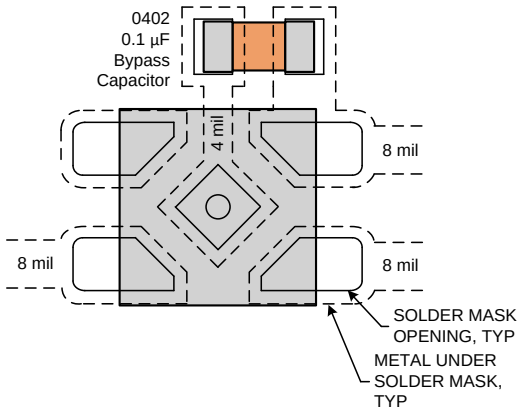


Figure 11. Example Layout With DPW (X2SON-5) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Designing and Manufacturing with TI's X2SON Packages*
- *Implications of Slow or Floating CMOS Inputs*
- *How to Select Little Logic*
- *Introduction to Logic*
- *Semiconductor Packing Material Electrostatic Discharge (ESD) Protection*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G17DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(H175, H17F, H17K, H17R)	Samples
SN74AUP1G17DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H17F	Samples
SN74AUP1G17DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H17F	Samples
SN74AUP1G17DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(H175, H17F, H17K, H17R)	Samples
SN74AUP1G17DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H75, H7F, H7K, H7R)	Samples
SN74AUP1G17DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H75, H7F, H7K, H7R)	Samples
SN74AUP1G17DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H75, H7F, H7K, H7R)	Samples
SN74AUP1G17DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C3	Samples
SN74AUP1G17DRLR	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(H77, H7R)	Samples
SN74AUP1G17DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H7	Samples
SN74AUP1G17DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	H7	Samples
SN74AUP1G17YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		H7 (2, N)	Samples
SN74AUP1G17YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	H7N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AUP1G17 :

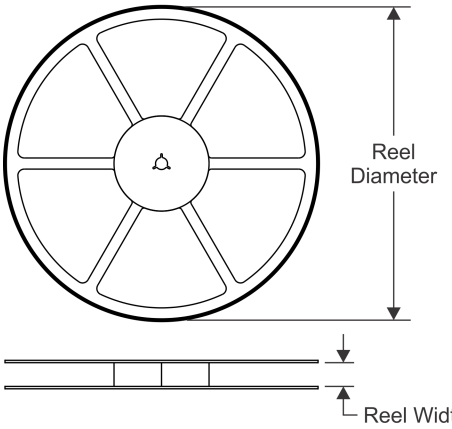
- Enhanced Product: SN74AUP1G17-EP

NOTE: Qualified Version Definitions:

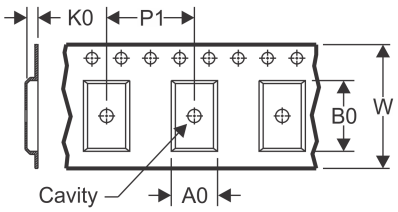
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

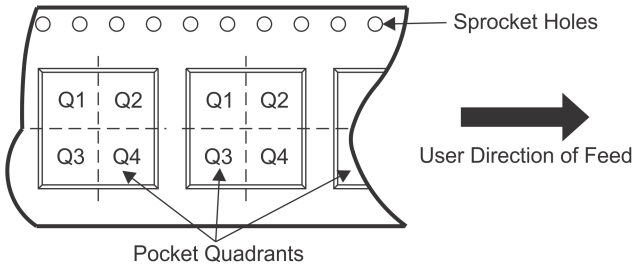


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

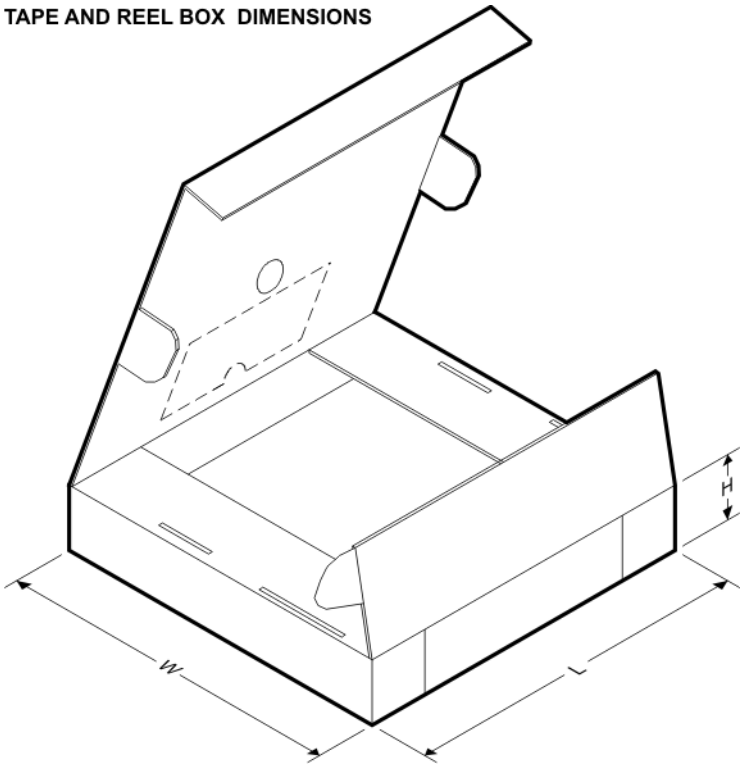
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G17DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G17DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G17DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G17DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G17DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G17DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP1G17DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G17DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP1G17DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G17DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G17DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G17DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G17DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G17DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1G17DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G17YFPR	DSBGA	YFP	4	3000	178.0	9.2	0.89	0.89	0.58	4.0	8.0	Q1
SN74AUP1G17YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

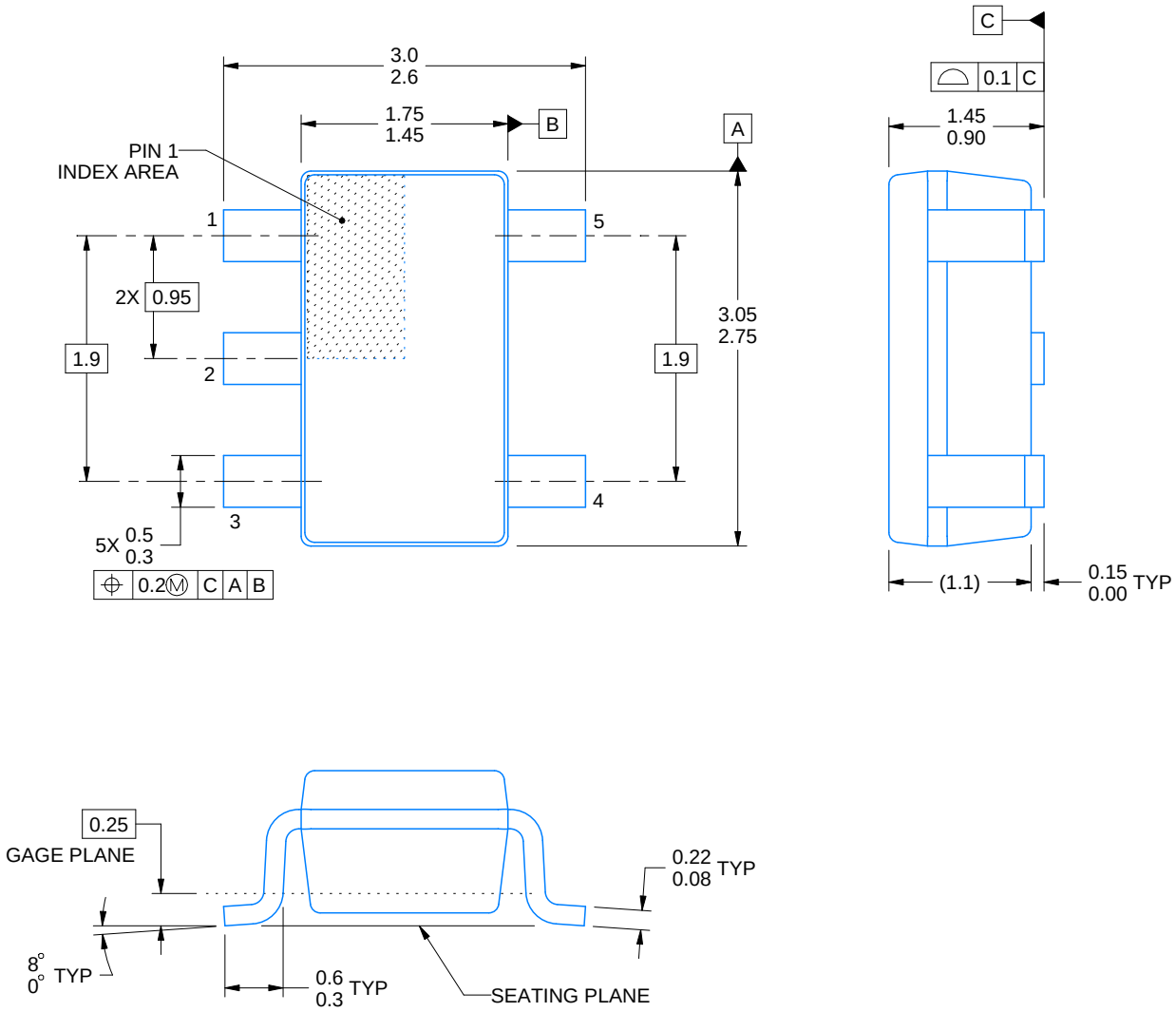
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G17DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AUP1G17DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G17DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AUP1G17DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AUP1G17DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G17DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G17DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G17DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G17DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G17DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G17DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G17DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G17DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G17DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1G17DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G17YFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0
SN74AUP1G17YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

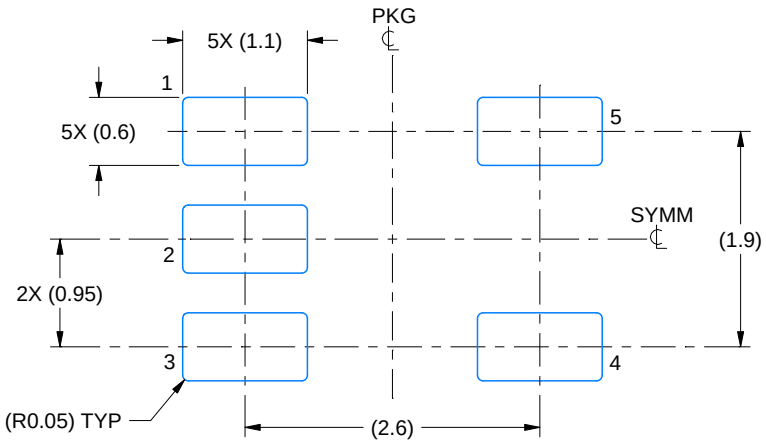
SMALL OUTLINE TRANSISTOR



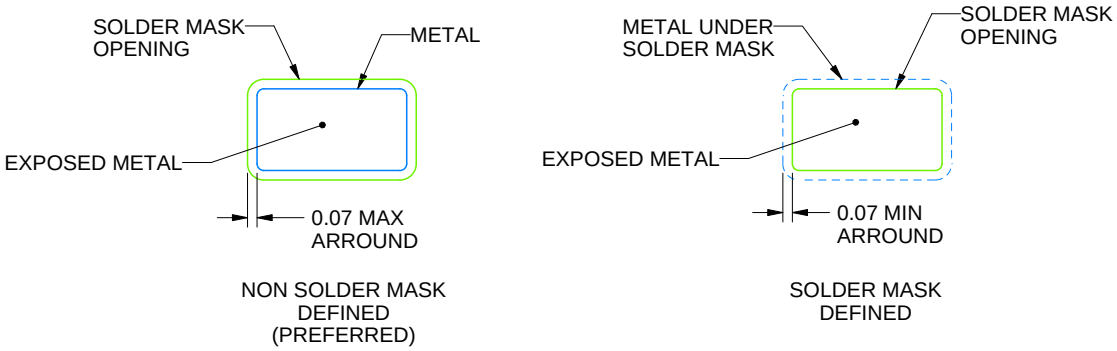
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

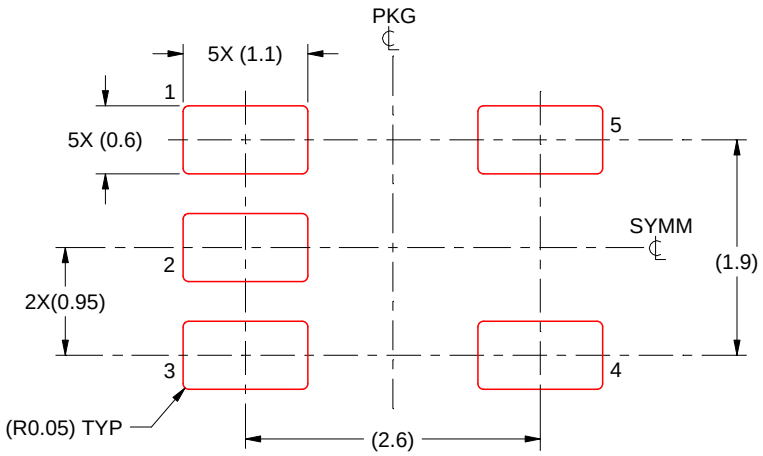


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

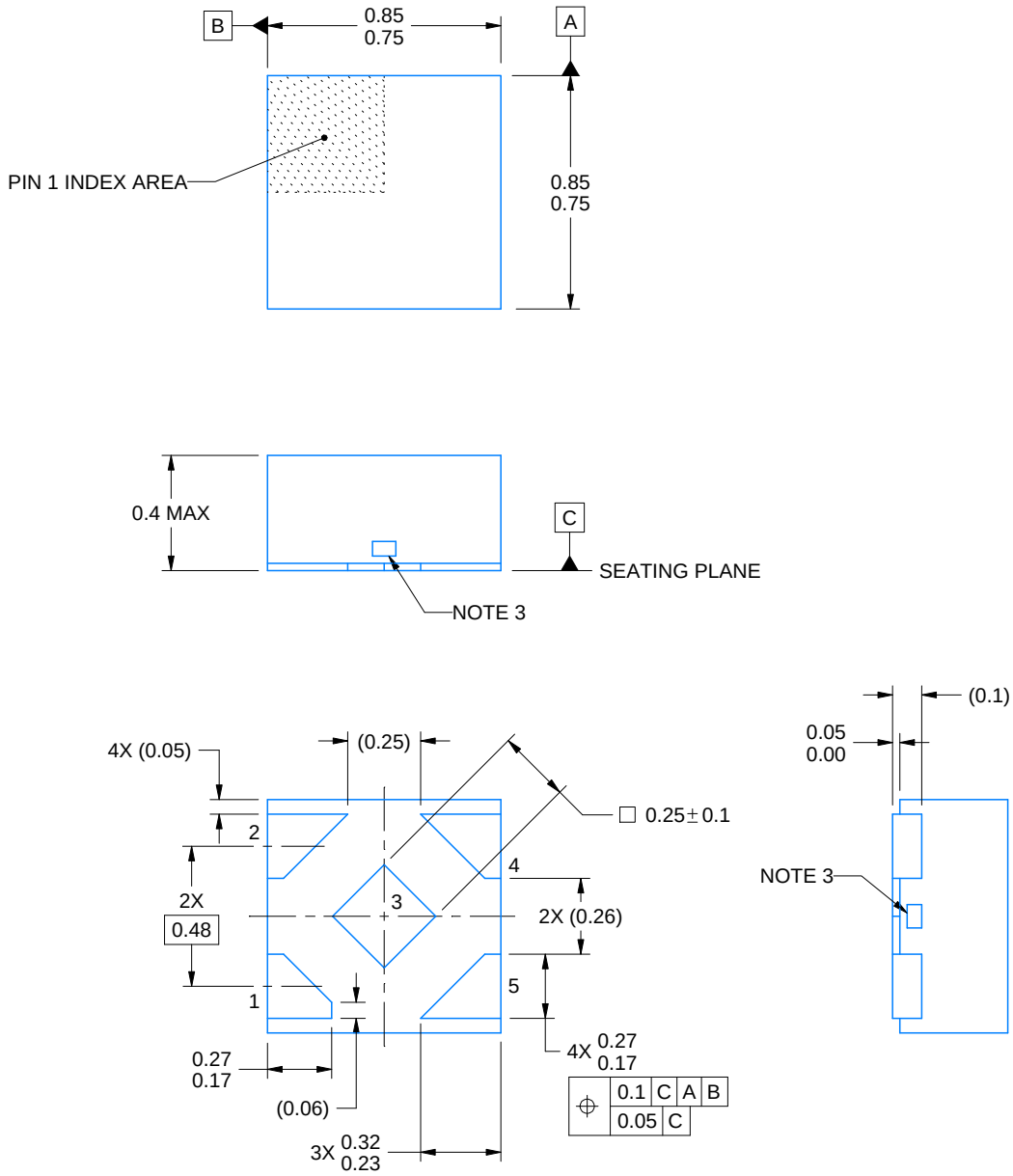
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

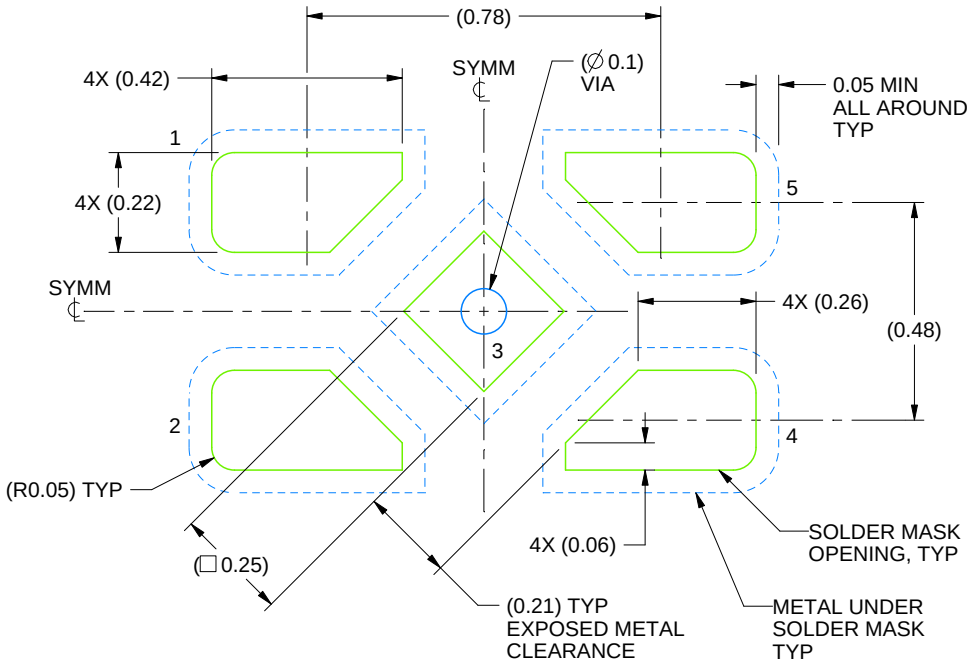
PLASTIC SMALL OUTLINE - NO LEAD



4223102/B 09/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

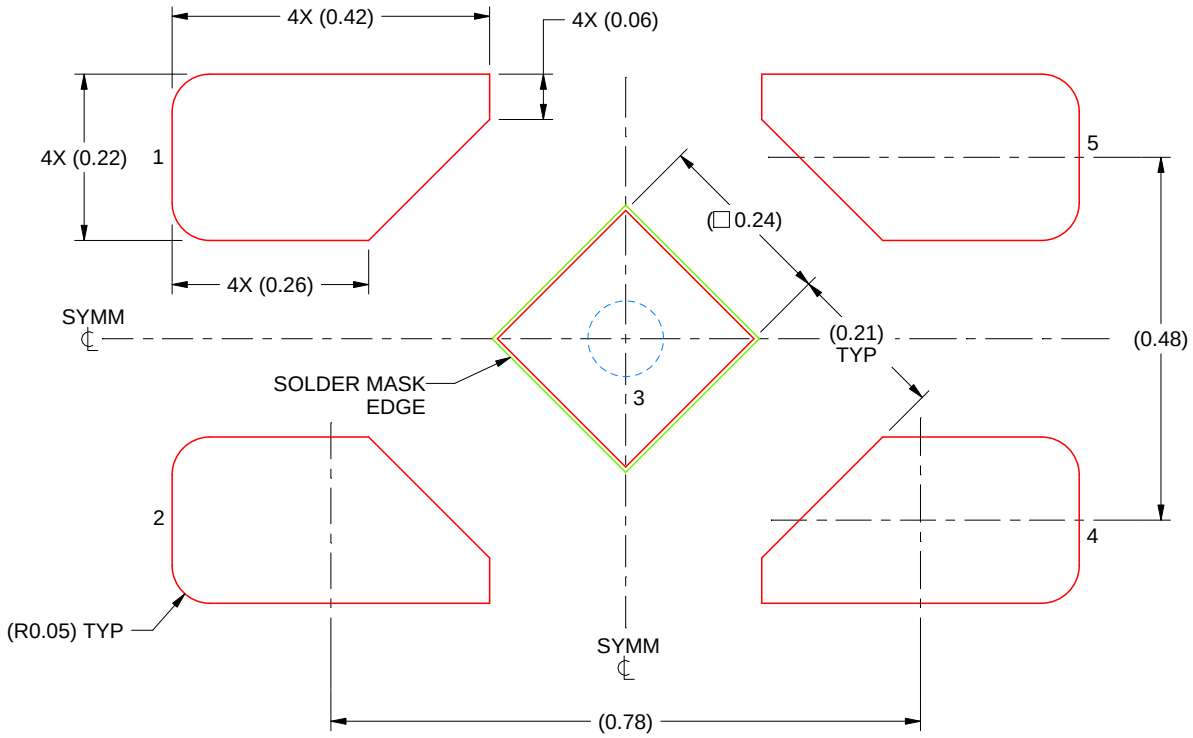


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/B 09/2017

NOTES: (continued)

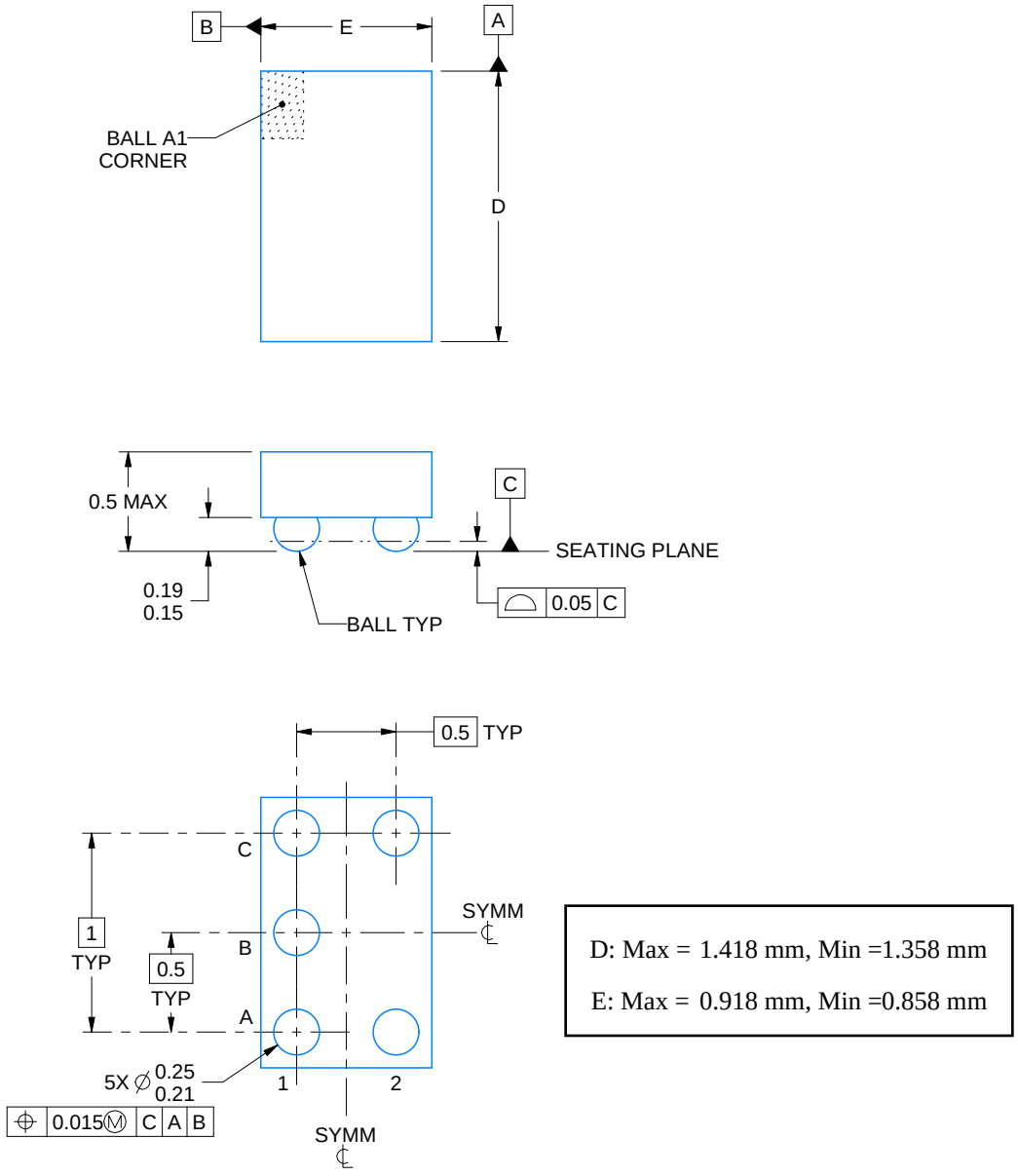
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



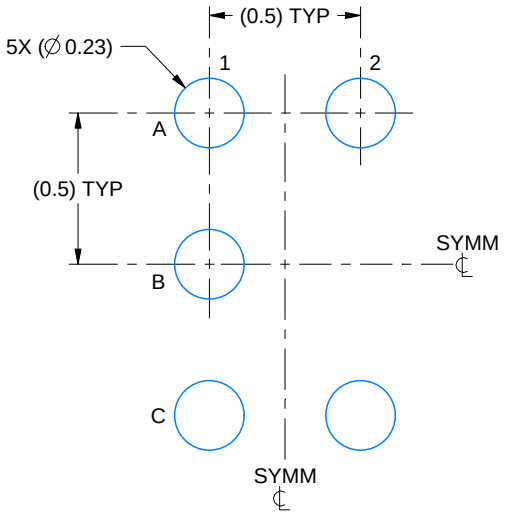
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

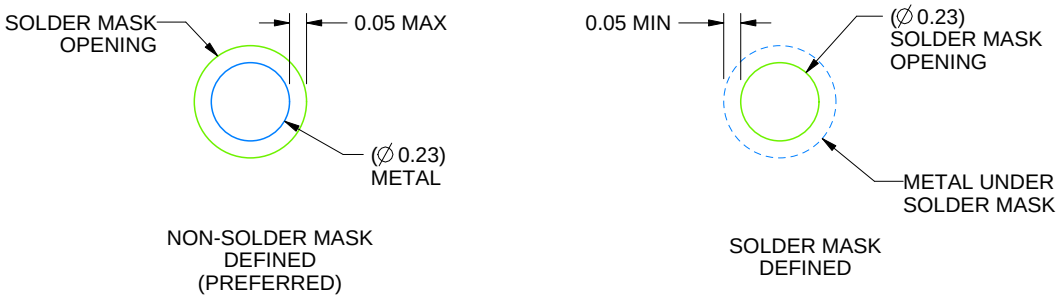
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

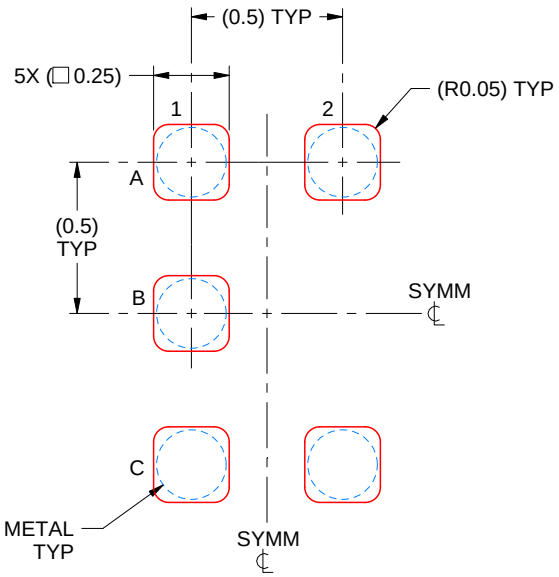


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

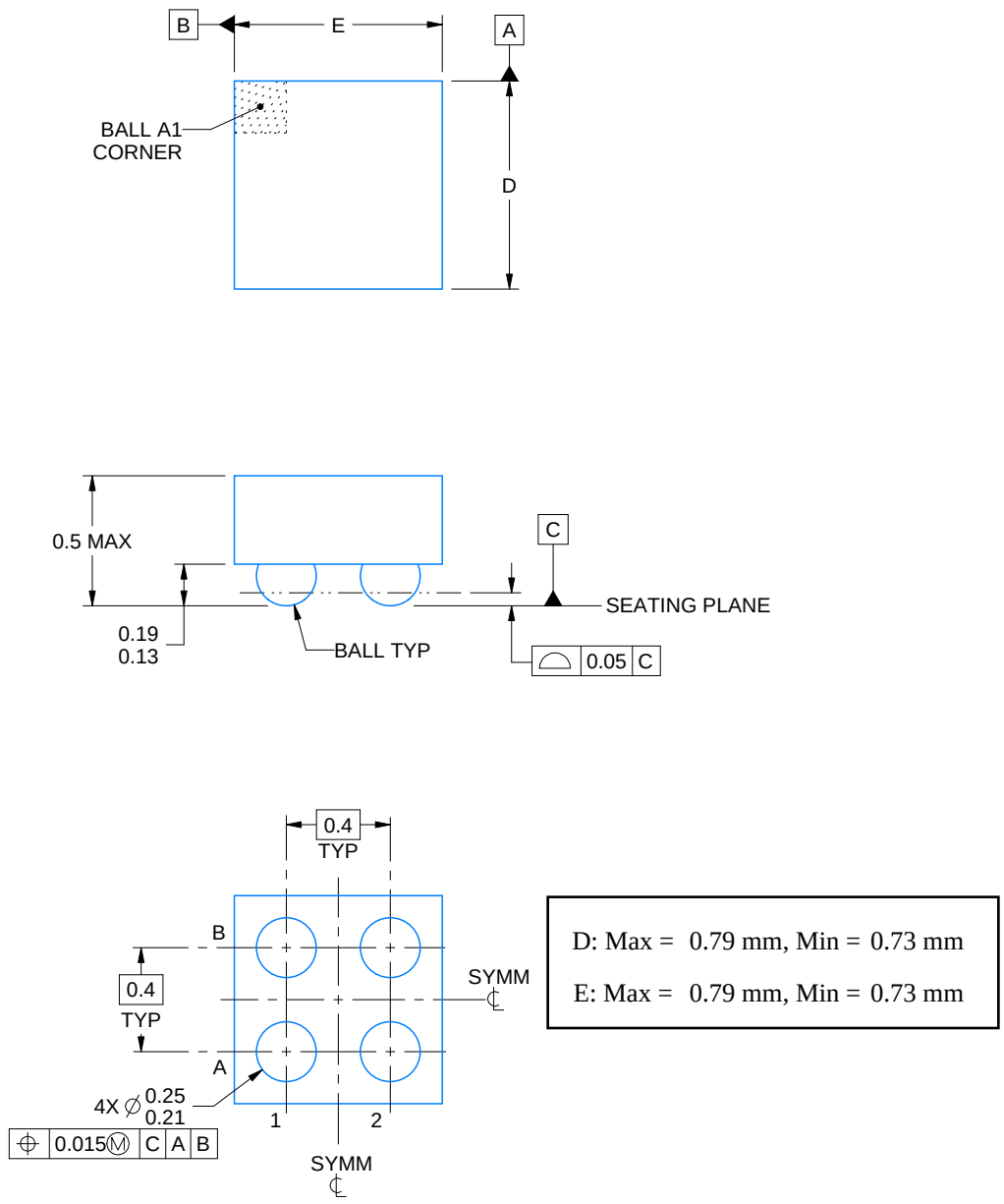
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

YFP0004

DSBGA - 0.5 mm max height

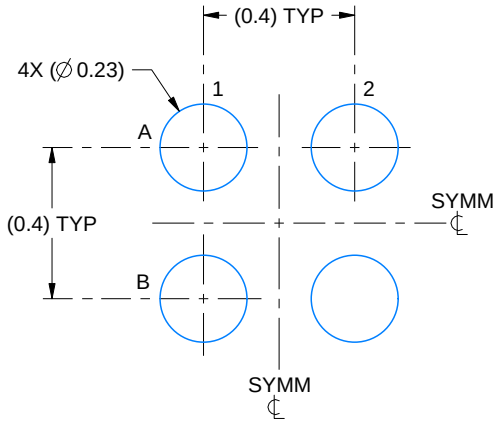
DIE SIZE BALL GRID ARRAY



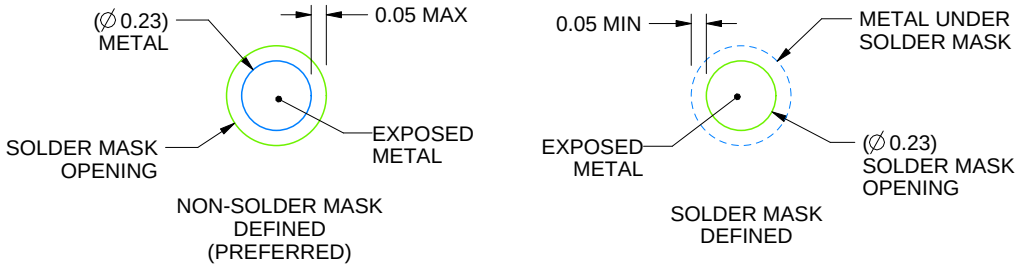
4223507/A 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

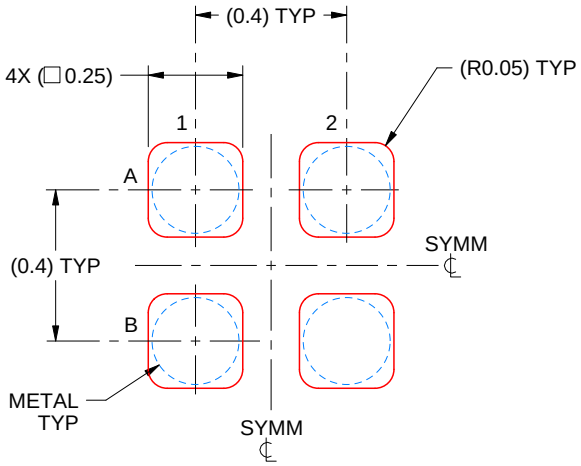
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

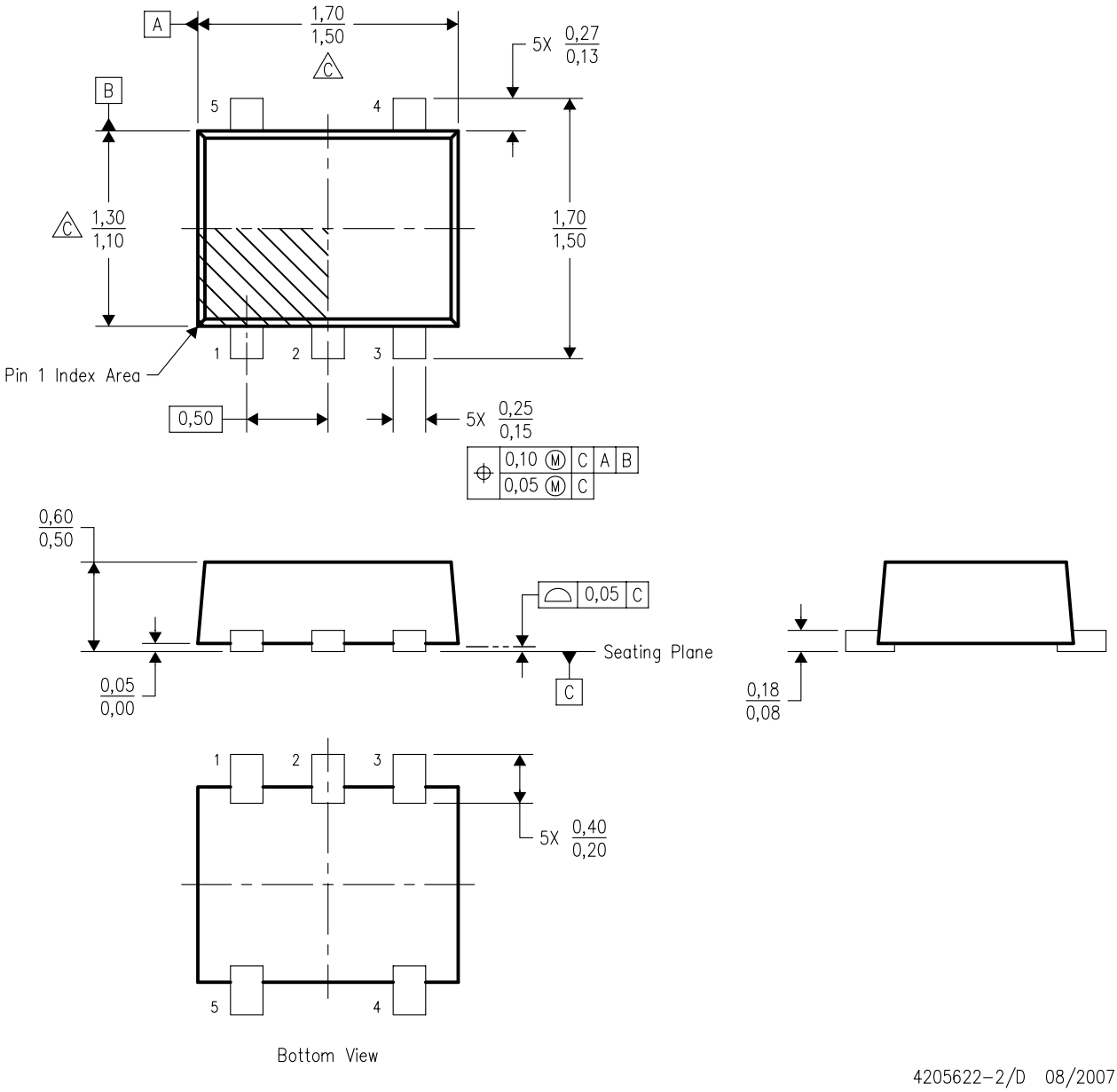


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

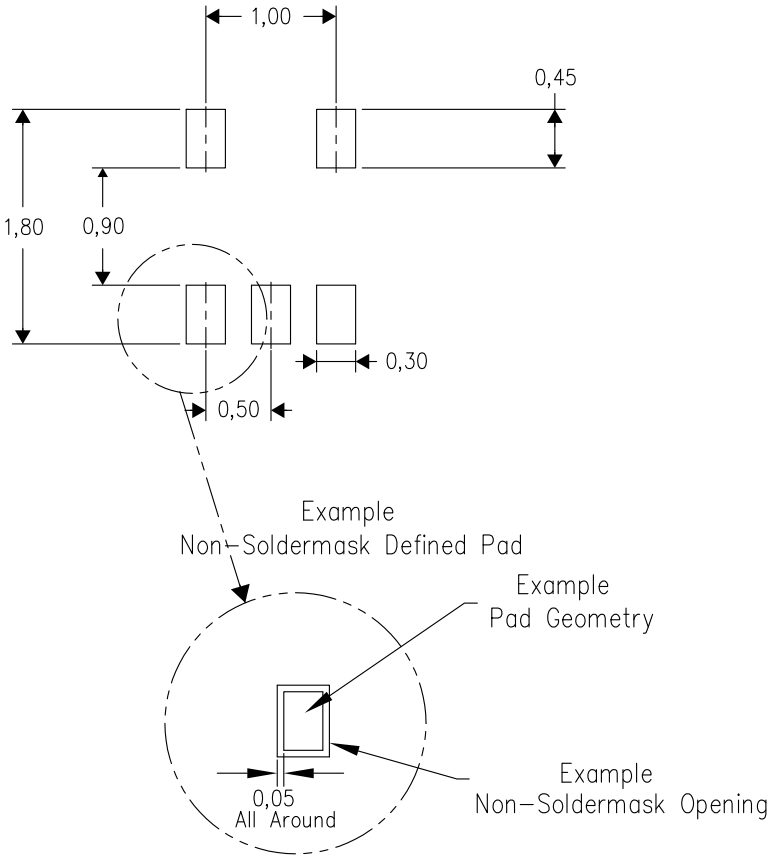
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



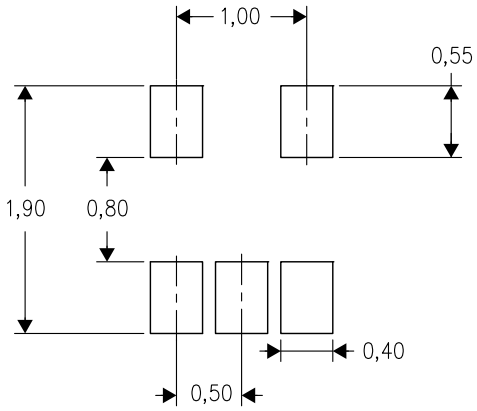
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



Example Stencil Design
(Note E)



4208207–2/E 06/12

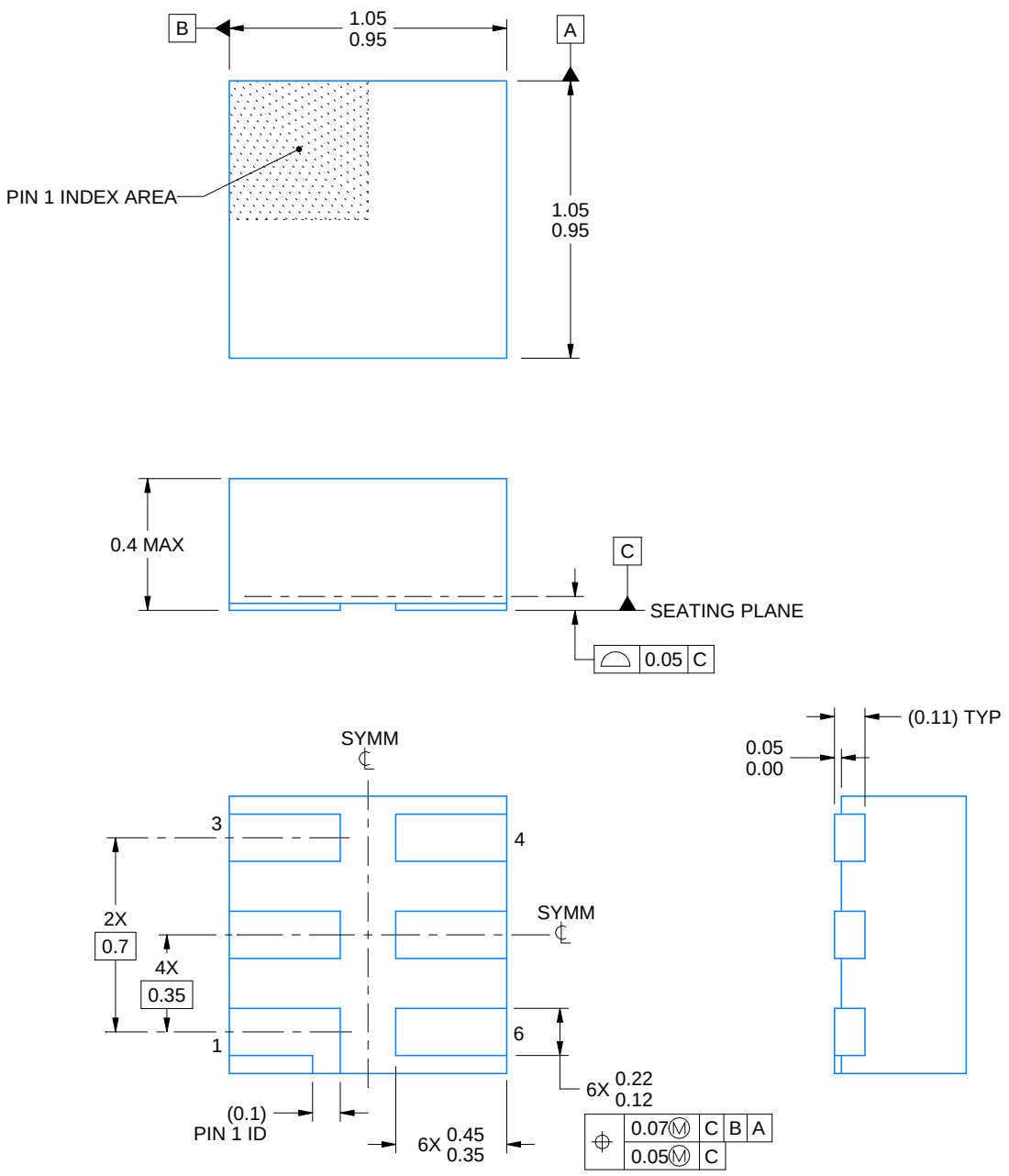
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

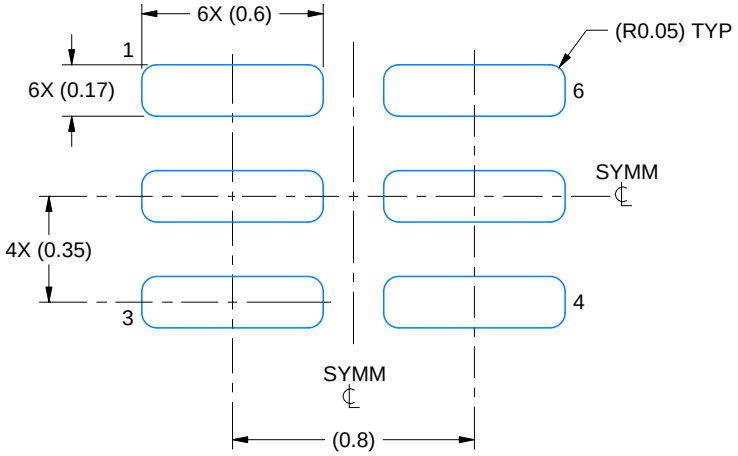
PLASTIC SMALL OUTLINE - NO LEAD



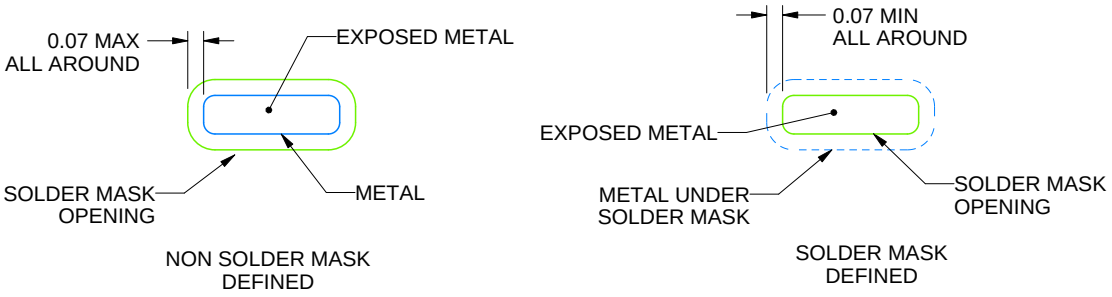
4220597/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

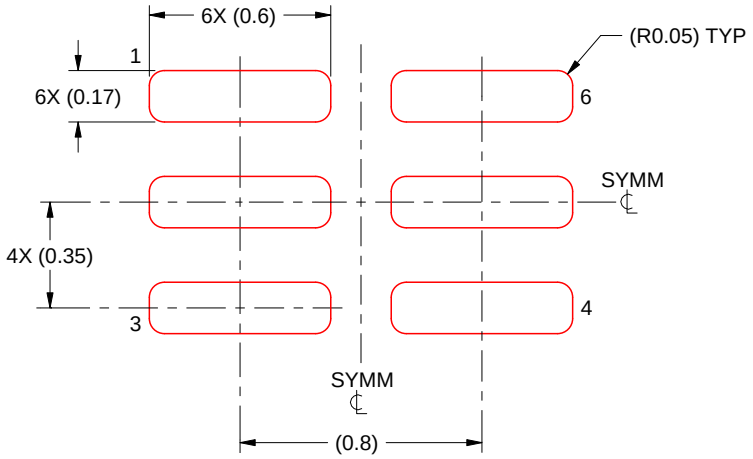
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



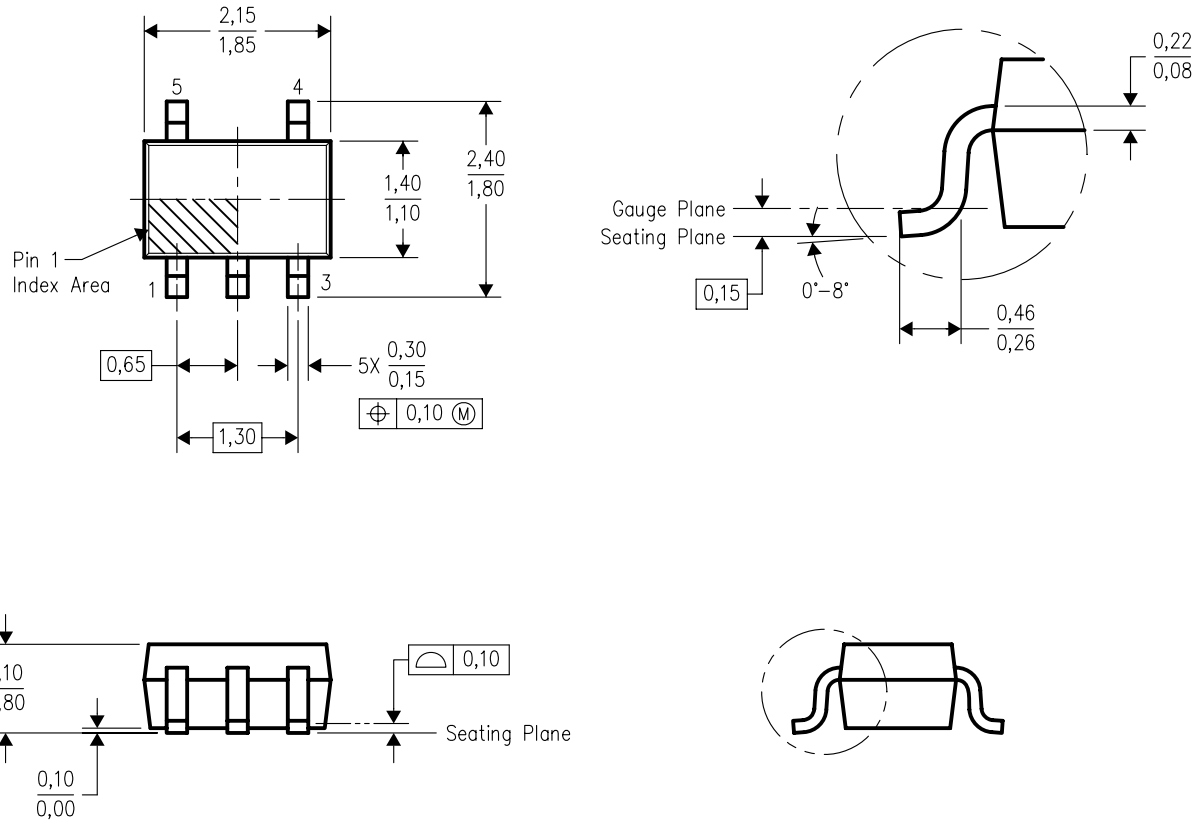
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

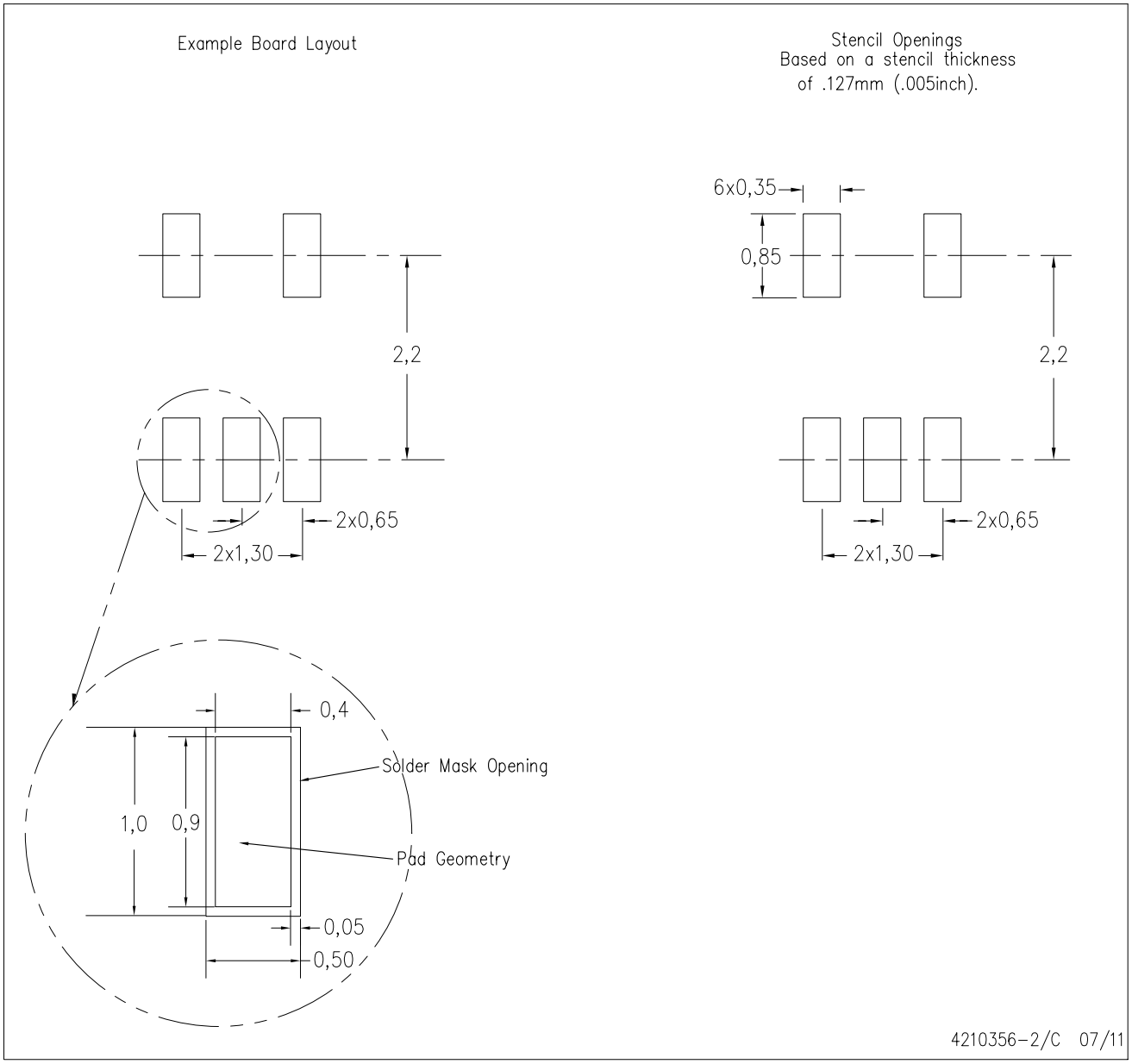
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



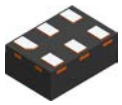
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

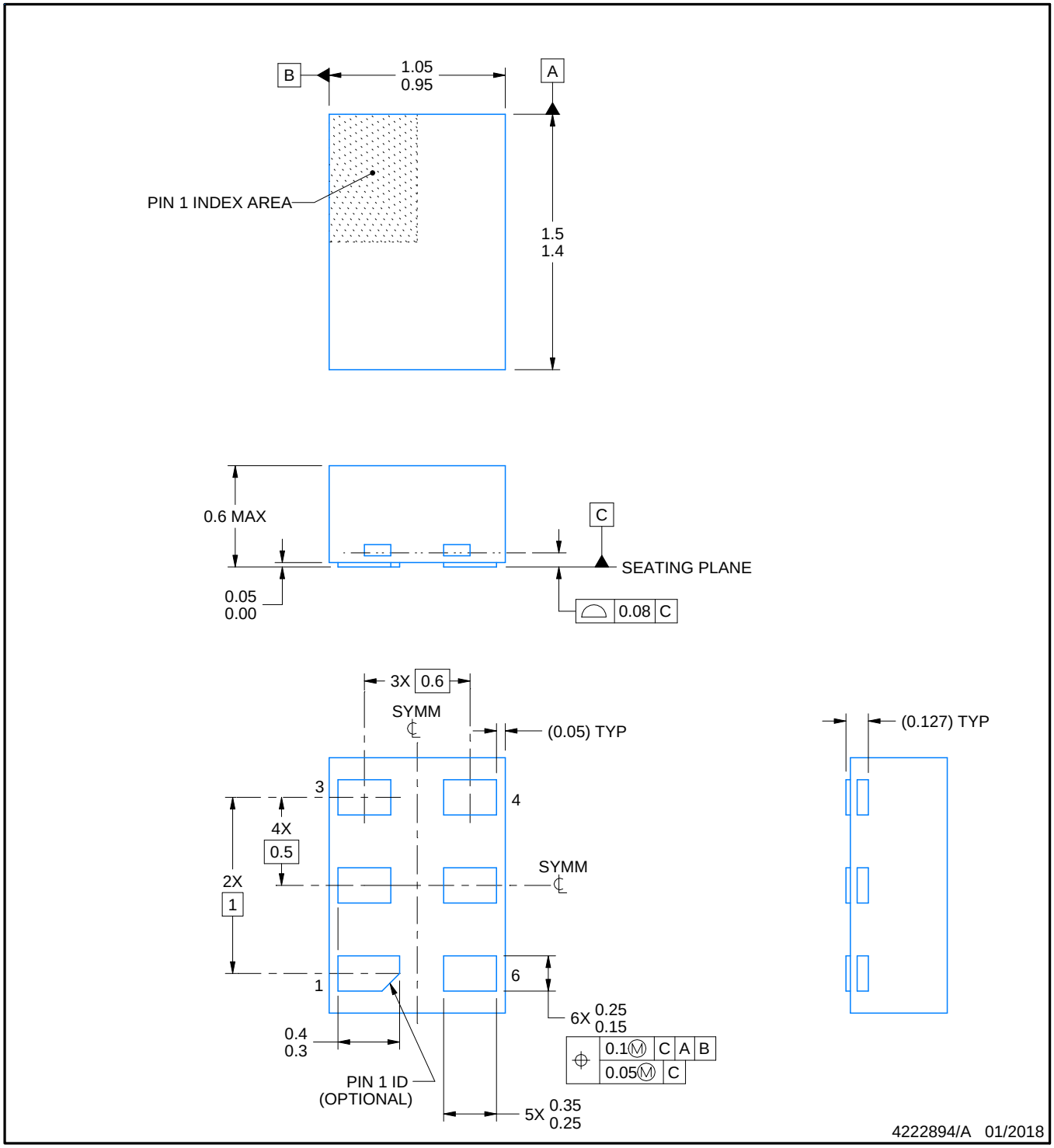
DRY0006A



PACKAGE OUTLINE

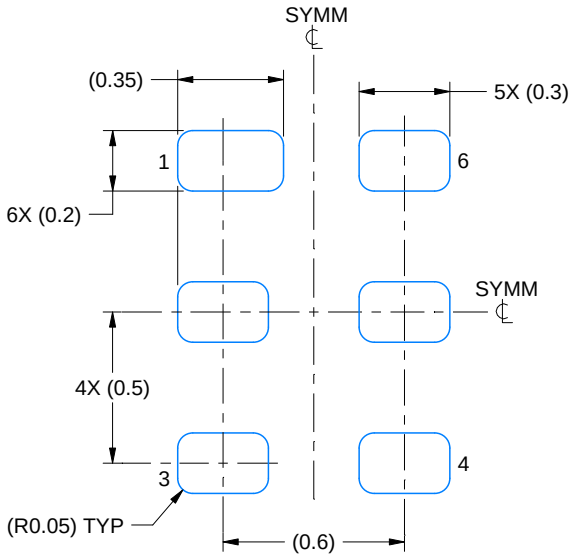
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

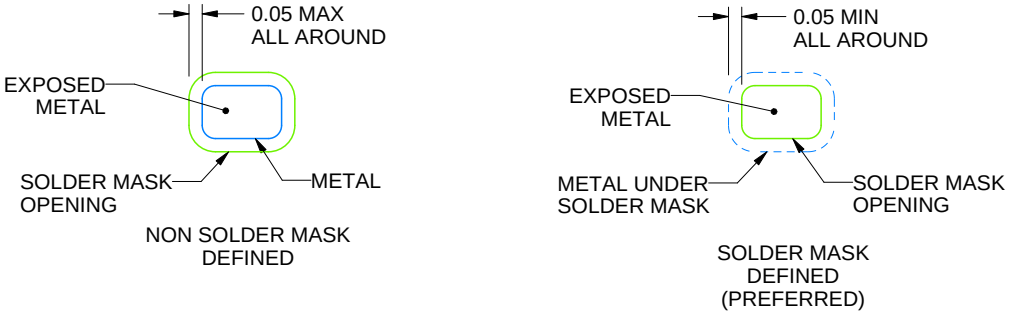


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

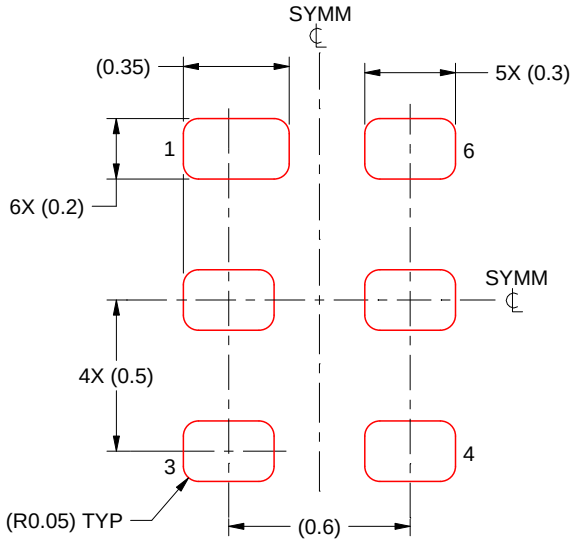
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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