40nW subthreshold event detector chip for seismic sensors

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***Abstract*— Unattended ground sensors (UGS) are widely used for persistent, surveillance that detects potential threats from intruders without generating false alarms. Seismic sensors are used to catch vibrations produced by intruders. Battery life is the limiting factor for solutions using digital processing. Thus power management strategies need to be employed to ensure longevity of the sensor networks. A 40nW subthreshold analog CMOS (complementary metal oxide semiconductor) is fabricated and tested, that wakes up a threat classifying stage. The system architecture is proposed along with optimizations for the different stages of the system. Variations in the subthreshold system will be discussed resulting in different system responses.**

Keywords- Sensors, low power, subthreshold, analog, variations.

I. INTRODUCTION

Smart sensor-based surveillance systems deliver enhanced performance when sensor fields are employed with electronic intelligence implemented at sensor nodes. Potential threats (humans or approaching vehicles) in remote locations are scarce and an event is considered a rare event. The main processing block within the sensor need not be on continuously and as a result can be in a sleep state. The main processing block classifies the kind of intrusion, whether a threat or not. An ultra-low power front end sensor is always on to detect events. If a true event has occurred, eliminating false positives, the main processing block is turned on.

We have designed and tested a subthreshold event detector chip for movement and seismic detection for perimeter intrusion. The chip helps reduce maintenance costs by increasing the life time of the sensors The front–end consumes 40nW of power and such ideas can be implemented in other devices where battery life is of crucial importance. The tremendous improvement in power consumption implies longer life as well as the ability to add more processing capability on chip.

The present working vibration sensor called the Smart Fence Unattended Ground Sensor (UGS), shown in Figure 1a, brings advanced situational awareness to perimeter security. The current sensor only constitutes digital micro-processors. The seismic based human threat sensor is to detect approaching humans and discriminate between series of events caused by animal, and passenger vehicles vs. background and a single vibration event, e.g. the falling of a tree limb. A geophone based seismometer has been employed which is an inexpensive sensor that provides easy and instant deployment as well as long range detection capability. The system was set up to discriminate between human footsteps, vehicles, background (including disconnected incidents, animals' footsteps). As soon as any event is detected a command center GUI raises alerts and slews video for threat confirmation when ground sensors detect the approach of human footsteps and the track of a vehicle to a virtual perimeter or fence-enhanced area.

The box in Figure 1a consists of the circuitry; there is also a geo-sensor or vibration sensor along with an antenna to communicate with the command center. In its idle state, power consumption is 2mA over 3.7V (7.4mW) which is being reduced in the subthreshold approach taken in the paper. Figure 1b shows the seismic event detector consisting of the seismic sensor followed by a passive low pass filter to cancel high frequency noise. The pre-amp and one of the first microcontroller consist of the event detector that is on continuously and wakes up the next micro- controller (that is mostly in the sleep state and does the classification) only when an event has been detected.

Low power digital processing at this end can be used, but apart from the processing, a digital implementation mandates the additional complication of ADCs and DACs, which certainly burn additional power and consume additional on chip surface area. There are various low power ADCs as in [1], depending on the application, the power can go as low as 35nW. In addition to the SAR, that already consumes decent amount of power an off the shelf DSP. A DSP from Texas Instruments like the C5000 ultra low power DSPs, has a standby power of 0.15mW already.

Low power analog methods can be used for the front end like a low power cochlea as in [2] and [3], where frequency bands are compared. Other methods for low power event

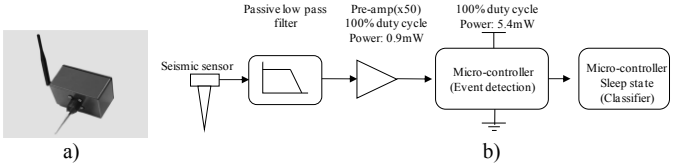

Figure 1: UGS seismic sensor

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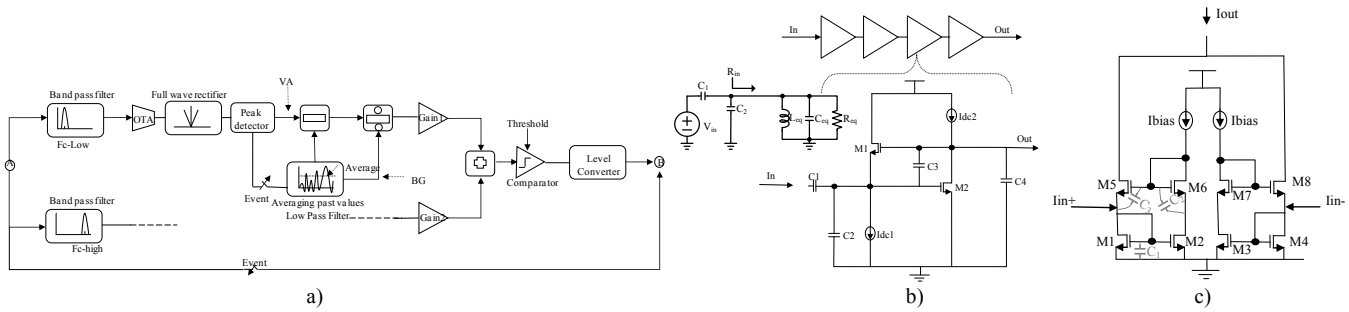

Figure 2: a) Subthreshold event detector system level. b) C4 BPF and effective input impedance. c) Wilson current mirror as full wave rectifier.

detectors use a time-domain approach instead of frequency analyses using band pass filtering. Such approaches are based on autocorrelation as in [4], consuming 835nW of power, and periodicity detectors of a time-domain envelope of acoustic signals as in [5], consuming 1.8uW. These approaches are all analog solutions to different types of event detectors with different functionality. Ideas can be adopted for the seismic event detection along with the pre-processing needed for our system.

The motivation for moving from the previous digital sensor system to an analog system is for the extremely low power operability, architectural simplicity and area compactness, of transistors in the analog sub-threshold region of transistors. Low precision analog VLSI circuits are suited for tasks corresponding to perception of a continuously changing environment such as event detection especially when cost, size and power consumption are the biggest concerns [6].

The behavior of complementary metal-oxide-semiconductor (CMOS) transistors is similar to that of bipolar junction transistors (BJTs) in this region and there is very little current flow comparable to the leakage current flow in transistors. The drain currents rarely exceed several hundred nano- to pico-amperes, thus using these transistors in this region can dramatically decrease the power consumption of the sensor. In this regime of operation, the drain current vs gate-source voltage characteristic follows a simple exponential relationship. The only caveat in designing subthreshold circuits is its intrinsic variability due to process and temperature variations.

II. METHOD

The following describes the overall system level design followed by the circuit level of the blocks within the system. The circuits are designed in a 150nm process in subthreshold analog CMOS domain.

A. System Level

The circuits are designed in a 150nm process in the subthreshold analog CMOS domain. The event detector designed in subthreshold analog domain is shown in Figure 2a. Band pass filters are used to find the power in two frequency bands. In the digital version a fast Fourier transform (FFT) is carried out at these two different frequencies. The filtered signal goes through an envelope detector to catch the peak voltage of the time varying signal. A comparator is used to detect whether a certain threshold has been passed. The summation of the voltage peaks from both bands is compared with back ground noise and is then compared with a threshold to trigger an event. If that were the case loud noise sources at those frequencies would trigger the system unnecessarily. Therefore a comparison of the voltage amplitude (VA) with the Back ground noise (BG) value is carried out as can be seen in (1).

$$\frac{VA_1 - BG_1}{BG_1} \tag{1}$$

The contribution from each of the signals as in (1), are adjusted using Gain1 and Gain2. The different gain settings are used for different environments, where one or the other frequency band needs a boost compared with the other. Equation (2)shows the mathematical operations taking place in the wake up detector. The indices 1 and 2 represent the two signal bands.

$$\frac{VA_1 - BG_1}{BG_1} Gain_1 + \frac{VA_2 - BG_2}{BG_2} Gain_2 > Threshold \tag{2}$$

Division is made simpler because translinear principle [8] can be used. Due to the exponential relationship of the current with respect to the gate-source voltage in subthreshold region, translinear principle can be used.

A level converter is introduced into the circuit since the output does not swing too high because of the subthreshold operation. A level converter is used to convert the subthreshold voltage level of the core analog processing block for connection to the outside world or connecting to digital processing blocks that require rail to rail swing. Details on these other blocks can be seen in our previous paper [9].

As soon as an event is detected at letter B in Figure 2a, the switch before the averaging circuit is opened and at that point VA is compared with a constant BG value. After many of such events, the main controller is woken up and the input from letter A goes directly to the micro-controller (at letter B) for further processing.

B. Filter design

1) Band pass filter

In the digital system only key features are extracted from the incoming signal. Only the 40Hz and 100Hz components are selected after a Fast Fourier Transform (FFT) is done using the

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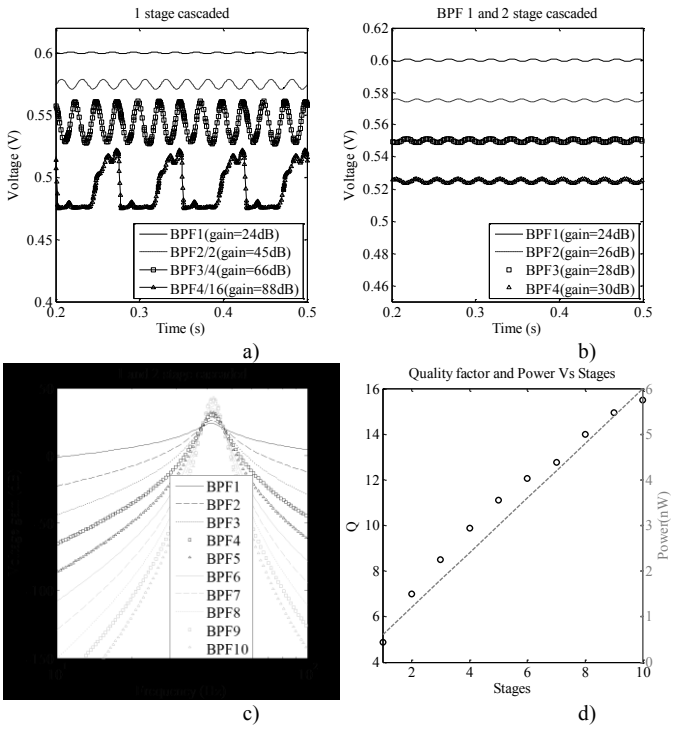

Figure 3: a) high gain stages cascaded, b) high gain and low gain stages cascaded, c) 10 stages cascaded, d) Q and power vs number of stages.

Goertzel algorithm. The Goertzel algorithm is an efficient method to evaluate individual terms of a Discrete Fourier Transform (DFT).

It was due to linearity issues especially while operating in the subthreshold region that a capacitively coupled current conveyor (C4) [7], shown in Figure 2b, has been chosen over other band pass filter structures. The reason for this choice is its simplicity and compactness. Since the operating frequency range for this application is very low, <100Hz, the time constants associated with the filter are large. For traditional integrated resistance values, these large time constants require very large shunting capacitances, which are impractical to implement in circuit monolithics. But an OTA operated in subthreshold regimes can be configured to deliver very large two-terminal resistances that allow large time constants to be achievable with small capacitances on chip. The transfer function along with other filter specifications of one of the stages of the C4 filter is shown in [9].

A crucial frequency to reject is the 60Hz power line noise and therefore large Q is required. 4 stages have been cascaded to create the necessary filter specifications. The first stage adds the gain to the filter and the other 3 stages have gains close to unity so as not to create large signals at the final stage, thus maintaining subthreshold operation. The last 3 stages are there only to increase the overall Q of the filter.

It has been shown in [9] that in order to maximize the Quality factor, the condition stipulated by (3)is required.

$$\frac{gm_2}{gm_1} = \frac{C_4}{C_3} \tag{3}$$

By varying the ratios of gms we can find the peak of Q.

2) Stage design and optimizing number of stages

Adding more stages to the design will increase the Q, but depending on the gains in the stage, distortion also increases. Figure 3a has a cascade of 1 type of stage having high gain and the output from the fourth stage sees distortion. Figure 3b shows a cascade with 2 types of stages. The first stage has higher gain, whereas the 2nd through 4th stage have a gain close to 1 and were just added to improve overall Q of the system as well as increase roll-off. Figure 3c and d, is similar to Figure 3b, except the 2nd type stage has been cascaded 9 times to create a total of 10 filters back to back or a 20th order system. The roll off increase by $20dB \times n(stages)$. But we see that the Q doesn't increase as fast with increase in stage unlike the power that increases linearly with number of stages. It is for this reason that 4 stages have been chosen having a Q of 10.

C. Envelope Detector

The envelope detector consists of three stages. The first state is an OTA, to convert the voltage signal from the band pass filter into a current. The next stage is a current rectifier as seen in Figure 2c. After rectification a peak detector is used to catch the envelope of the signal. Details of the envelope detector blocks are in [9].

The full wave rectifier consists of two Wilson current mirrors to rectify both phases of the signal. Qualitatively, by looking at Figure 2c, when I_{in+} (OTA output current) is greater than I_{bias}, the V_{DS2} of M_2 drops to maintain the same I_{bias} with increased V_{GS2}. This in turn drops V_{GS6} and M_5 turns off. When I_{in-} is less than I_{bias} and since M_1 mirrors I_{bias}, the additional current is supplied by M_5 and the current is seen at I_{out}. Thus M_5 turns on and off in one cycle. M_8 acts the same way in opposite phase and thus there is always an on current only in one phase and we have a full wave rectification.

Figure 4 shows effects on the rectification due to 1 KHz signal for sub-vt and above-vt systems. On the positive phase M_1 turns on while M_5 is off, the transistors switch states on the negative phase. M_1 consists of the bias current, I_{bias}, as well as the sinusoidal swing, whereas M_5 only consists of the swing of 30pA. With increase in frequency the response of switching 'on' transistor M_5 is slower. This delay in turning M_5 on is the dead zone. The zoomed-in inset shows this lag in M_5 turning on and thus resulting in distortion in the rectifier's output current. A dead zone is seen in the sub-vt system on the left, where as no observable dead zone for the above-vt system.

Following are the calculations to find the maximum frequency of operation for a sub-vt rectifier. As mentioned earlier with a swinging I_{in},V_{GS} of M_2 and M_6 change, and this is done so by charging caps C_1, C_2 and C_3. By increasing frequency the reactance of the capacitors drop, thus requiring more charging current. Due to the low Ibias in subthreshold, the charging current is limited and thus the worst case dead zone can be calculated from this limit.

$$I_{bias} = I_{M6} + I_{C2} + I_{C3} \tag{4}$$

When V_{GS} of M_6 falls to zero, the current though M_6 should be zero save for a leakage current of about 10pA, the rest of I_{bias} flows through C_2 and C_3. Since M_6 and M_5 are matched transistors we assume equal I_{C2} and I_{C3} equal to 10pA each. This approximation can be seen in the left graphs of Figure 4.

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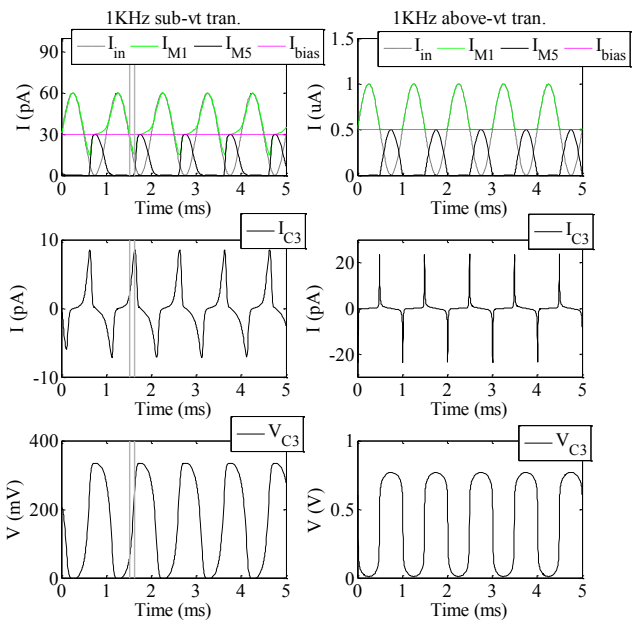

Figure 4: 1KHz size wave applied to sub-vt and above-vt system. Sub-vt system shows observable dead zone limiting frequency of operation.

When I_{C3} peaks, M_5 turns on having a V_{GS} equal to V_{C3}. Also I_{C3} should peak before the I_{in} peaks in its negative cycle (or its minimum value) or M_5 will never supply a full I_{out} equal to the peak I_{in}.

Assuming that the peak occurs at the middle of the limiting dead zone interval, which is T/2 (when I_{in} falls below I_{bias}) to 3T/4 (when I_{in} is minimum) and I_{C3} is a triangular wave until its peak, the worst case dead zone (t_{dz}) can be found from below:

$$\int_0^{t_{dz}} \frac{I_{C3}(\max)}{t_{dz}} t\, dt = C_3 \Delta V_{C3} \quad (5)$$

with I_{C3}(max) of 10pA, C_3 from spice data, 1fF, and ΔV_{C3} shown between the gray lines in the graph, equaling about 220mV, we get t_{dz} = 44us, and shortest time period is

$$T = t_{dz} \times 4 \times 2 \quad (6)$$

giving us the maximum frequency at 2.8 KHz.

The dead zone can be reduced by increasing Ibias, as there will be a larger I_{C3}. Looking at the graph on the right, the rectifier is above-vt with no observable dead zone.

D. System Simulations

SPECTRE is used to simulate the proposed event detector system using a 150nm process, with a supply of 1.8V. A footstep signal which is a sampled input received from the geophone is used to simulate the system. Figure 5 shows the time domain analysis of the system. From the graph on the bottom it can be seen that the background changes very slowly because of the slow or long averaging window. The final output after the components from both bands have been summed, compared and then level converted can be seen on the bottom graph. The final level converted signal goes from 0 to 1 V which is sufficient to turn on and off switches. There are 6 footstep events at the input signal and all 6 events are pulsed at the final output as can be seen in the graphs.

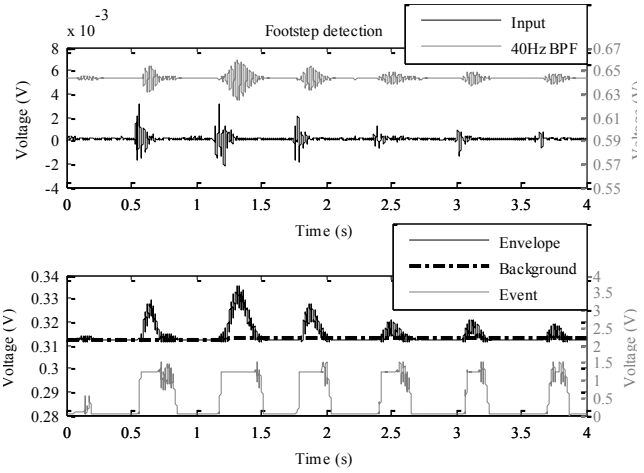

Figure 5: Foot step simulation.

III. HARDWARE

A. Chip layout and die

The complete layout of the event detector chip is shown in Figure 6a. The chip consists of all components as in the system diagram in Figure 2a. The system also consists of test circuits like buffers and switches. Some of the components we see in the figure are the 40Hz and 100Hz BPFs; the C.S block is for the current sources; the envelope detector; divider along with the adder, comparator and level converter; D.C is for digital control (like switches, etc.) and the output buffers.

The area of the chip is 1mm by 1mm and is fabricated by Cypress Semiconductor in a 150nm process. Due to the low frequency of operation the capacitors related to the filters are large and is apparent in the figure. The analog circuits compared with the capacitors occupy very little area. Figure 6b shows the unpackaged die micrograph.

B. Chip simulations

1) Band Pass Filters

The response of different sections of the 40Hz BPF is shown in Figure 6c. The figure shows the response of stage 1 (S1), stage 2, 3 and 4 (S2). S1 and S2 are designed with different gains and Qs. S2-S4 is the cascade of the last 3 stages and S1-S4 is the cascade of all 4 stages. S2-S4 are controlled by one current source parameter. And thus mismatches in mirroring the currents leads to offsets in center frequency peaks of each of the stages, resulting in drop in gain and Q when cascaded. Also in the Figure 2b Idc1 and Idc2 are also only controlled by one current source and could be another source for mismatches and thus loss in gain. To increase control of various parameters of each of the stage of the filter, more current sources would be required leading to more programming.

Similar response is seen for the 100Hz filter in Figure 6d. Although overall gain maybe low in the 40Hz BPF, gain can be increased at the OTA stage of the envelope detector, or at the divider stage.

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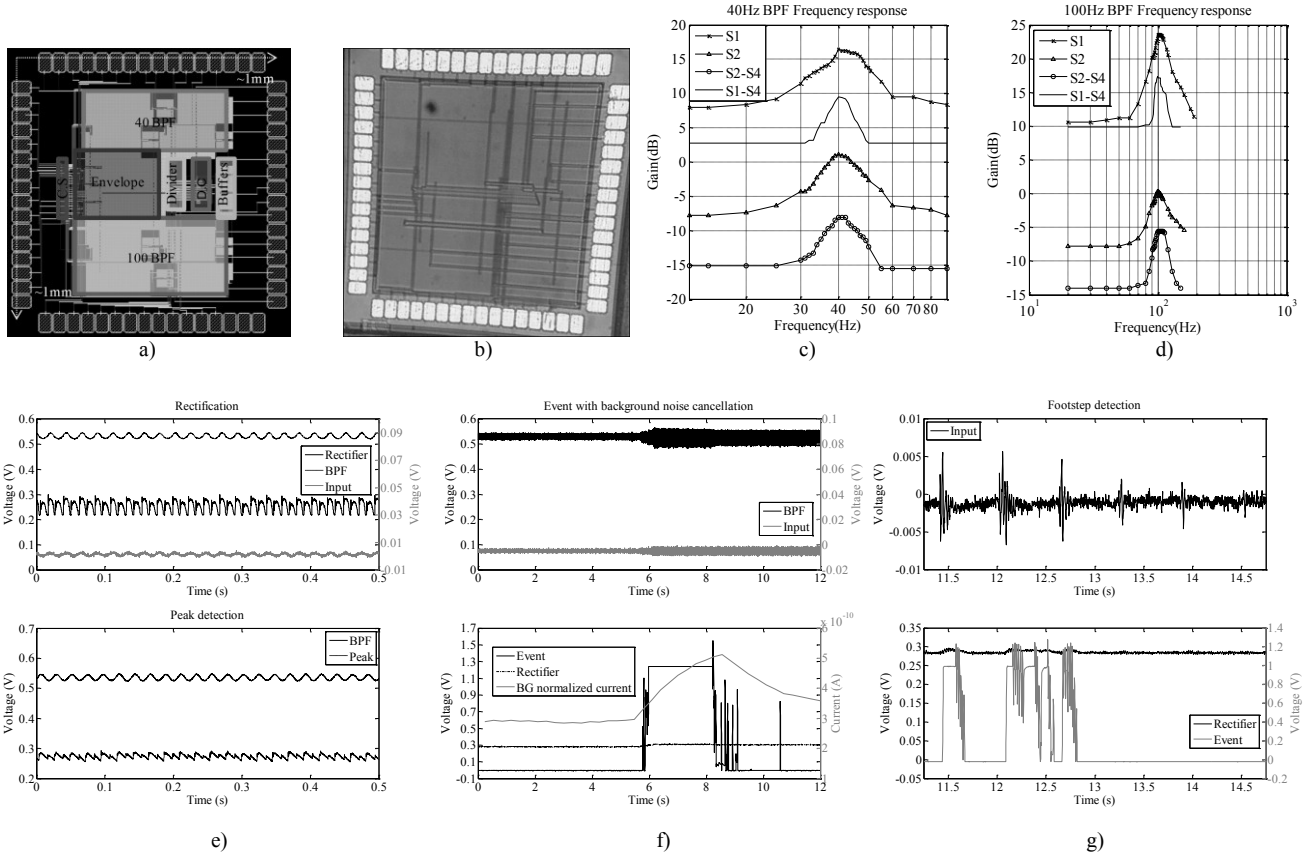

Figure 6: a) Chip layout. b) Chip micrograph. c) Reponses of different sections of 40Hz BPF. d) Reponses of different sections of 100Hz BPF. e) Full wave rectification for 1mV 40Hz sine wave along with peak detector response. f) Event detection for step increase in input amplitude. g) Event detection for footstep data

2) Envelope Detector

The full wave rectification can be seen in Figure 6e. A 1mV 40Hz sine wave is applied. The rectified output shows a mismatch in the amplitudes of the different phases and this can be adjusted by changing the bias voltage at the OTA. Figure 6e shows the output of the peak detector as well. Here the rise time is fast whereas the fall time is slow for the peak detection. The response is like a triangular wave and the slow fall time can be changed to make it even slower to get a steady DC voltage.

3) Event detection

The divider circuit in Figure 2a is used to divide out the background signal from the instantaneous signal. The divider output also includes a multiplication factor, which is Gain1 and Gain2. The purpose of the background noise cancellation is to remove constant noise sources from the environment such as generators and motors in the area.

Figure 6f shows the background noise cancellation. The input is a 1mV sine wave which is then stepped up to an amplitude of 3mV. A higher DC peak value for the 3mV signal is observed. This experiment shows that only the instantaneous input step is caught and then after a while it is considered a non-event and considered as background noise. The current output from the divider that does the background cancellation is also shown. The rise of the output current is indicative of an event. The onset of the step in voltage causes an increase in the output current from the divider. After a while this output current falls down back to its original value, showing that the constant high input voltage is a background constant noise and not an instantaneous event. This mechanism helps cancel out false positives and makes the event detector sturdy to different types of environmental noise sources. The event from the level converter, is also shown.

The final experiment is show in Figure 6g depicting the event detector's response to footstep signals. The same sampled footstep data used for the Cadence simulations is used here. The first 3 events are detected but not the last 3. The reason for missing the 3 events is due to low gain from the BPFs as a result of unmatched center frequencies. These events can also be missed because of the inherent dead-zone of the rectifier. The latter issue can be prevented by improving the gain of the filters or by adding an extra gain stage at the input of the system.

IV. CONCLUSION

An ultra lower power event detector has been designed for long-term persistent sensor-based surveillance systems. An analog front end event detector operating in subthreshold region of CMOS transistors consuming 38nW of power has been designed, enhancing the longevity of the sensor. The

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TABLE 1
POWER METRIC FOR EVENT DETECTOR CHIP

Component	Stage	Power (nW)
40Hz filter	Stage 1	0.115
	Stage2-4	0.396
100Hz filter	Stage1	0.18
	Stage2-4	0.432
Envelop Detector	OTA	2.059
(40 and 100Hz)	Rectifier	0.162
	Peak detector	0.144
Divider	Input currents	0.432
	Gain factor	0.72
	Output	0.54
Comparator		11.88
Buffers	In between filters	2.138
	Envelope to divider	1.425
	Additional for above (due to LPF)	18
Total		**38.6**

fabricated chip ensures feasibility of the design and the realistic power savings achievable. Figure 5, Figure 6g show the responses of the Cadence simulated subthreshold system and the chip respectively. The chip detects the first 3, but not the last 3. This can be as a result of low gain in the system as a result of loss in gain at the BPF stages and also because of the dead-zone inherent in the full wave rectifier. The other reason for not catching the last 3 events could be due to the fact that the footstep signal is comparable with the noise floor and thus not differentiable from noise.

A complete list of power consumption by various parts of the circuit are shown for the chip in Table 1. Most of the power consumption goes into the comparator and the buffers. The comparator needs this extra power to increase the gain of the signal received from the system for comparison.

Comparing to the digital system in terms of power; the digital system consumed 7.4mW and the subthreshold analog system consumes about 40nw, delivering about a 160 times power reduction. In terms of performance, from the previous figure we seen that a few events were lost, and this is due to loss in gain in some of the stages. These issues can be fixed. Overall, with the power savings in mind, this is a huge improvement and thus can add to battery life, or the tremendous improvement in power consumption implies capability to add 160 times signal processing capability at the front end of these security sensors.

The noise cancelling mechanism helps improve the systems SNR, it also rejects false positives received from generators, motors or any other constant noise sources. The 2 filters help clean up the incoming signal as well as help to do a pre-classification. From previous statistical data, the 40Hz and 100Hz bands provide important information for footstep and vehicular signals. All the above benefits along with the operation of the entire front end event detector for seismic sensors in subthreshold domain provide insights into the tremendous power saving achievable.

One of the main concerns of the chip is that in operating in subthreshold region, current sources need to be stabilized. Better PVT independent current sources need to be designed. Variations in currents were observed with temperature changes. Future versions of the chip would require better current sources that are PVT independent.

Even if current sources are sturdy, matching these current sources throughout various parts of the chip can lead to mismatches and thus different operation for different circuit components. This was seen in the BPFs, where the center frequencies among stages differed, thus losing gain and quality factor in the filters. Monte Carlo simulations for the various current sources for the 4 stage BPF is shown in Table 2. Although the overall center frequency for the 40Hz BPF doesn't have a large standard deviation, the overall gain can drastically decrease, with a standard deviation of about 7V/V.

ACKNOWLEDGMENTS

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TABLE 2
VARIATIONS IN CURRENT SOURCES. N=100

Current source	Average	St. dev.
BPF1 Idc1	30.4706p	3.34431p
BPF1 Idc2	30.2226p	3.4439p
BPF2 Idc1	30.5717p	3.17378p
BPF2 Idc2	29.7847p	2.78516p
BPF3 Idc1	30.2323p	3.47548p
BPF3 Idc2	30.7218p	3.13852p
BPF4 Idc1	30.2577p	3.09612p
BPF4 Idc2	29.9211p	3.23608p
Overall fc	**42.7847Hz**	**3.05028Hz**
Overall gain	**14.8512V/V**	**6.84686V/V**