A Perceptron Circuit with DAC-based Multiplier for Sensor Analog Front-ends

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***Abstract*—This paper presents a perceptron circuit which can be implemented into sensor analog front-end consistent with neural network-based machine learning. We introduce a DAC-based multiplier in the perceptron circuit, where the DAC is used as a programmable resistor. Compared with a traditional transconductor-based multiplier, the precision of our multiplier is formulated only by the digital codes, and it has a wide input range and a good temperature dependency. The simulation result demonstrates the DAC-based multiplier amplifies smoothly analog signals by the digital codes.**

I. Introduction

In recent years, a machine learning has remarkably developed, and many cases of its social implementation have been reported. A neural network is one of fundamental architectures for the machine learning, and the VLSI implementation has been researched traditionally [1]. Recent trends of machine learning implementation are configuration on FPGAs and acceleration by GPUs [2], [3].

On the other hand, a wireless sensor network is widely used to collect data in various places such as factories, farms, and cities. An advanced sensor node has a multi-input to compensate a sensing information by employing different sensor signals. For example, [7] introduces an 8-channel EEG/electrode-tissue impedance acquisition system, where nine active electrodes and one back-end analog signal processor work being closely correlated. In [8], a pressure sensor and a microphone are combined to visualize the blood pressure measurement.

In the compensation and combination of the input signals, it is known that a machine learning technique is useful. Hence, a sensor node is requested to incorporate an architecture for neural network computing. Unlike GPU or FPGA-based neural network architectures, however, a sensor node must be low power and with a small hardware even sacrificing a large computation.

Therefore, we attempt to embed a learning circuit mechanism into an analog front-end of a sensor node. This paper focuses on a perceptron which is an essential function of neural networks. Aiming a small embedding, we realize it by analog circuits introducing a DAC-based multiplier in the perceptron circuit. The DAC-based multiplier is to amplify an analog input signal by a preset digital code. Compared with a traditional analog multiplier of transconductor-based, the precision of our multiplier is formulated only by the digital codes, and it has a wide input range and a good temperature dependency. The simulation result demonstrates a perceptron circuit with the DAC-based multiplier combine smoothly multiple analog signals amplified by the digital codes.

The rest of the paper is organized as follows. Section II describes a perceptron circuit used in neural network systems. Section III introduces a DAC-based multiplier and describes the simulation results. Section IV summarizes this work.

II. Perceptron Circuit

As described in [1], a perceptron is an essential function used in neural network systems. A typical model of the perceptron is illustrated in Fig. 1. The inputs are $f_1(t) \ldots, f_n(t)$, each of which is multiplied by a weight $w_1, \ldots, w_n$, and all weighted inputs are summed at the output.

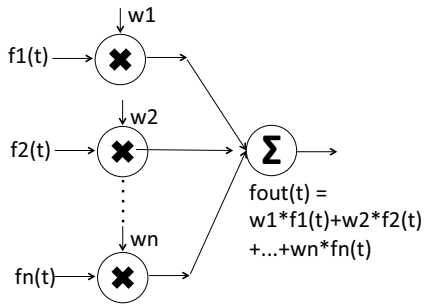

Fig. 1. A typical perceptron function.

In general, realizing this perceptron function in an analog front-end of a sensor node, time division multiplexed input is used. Here, as shown in Fig. 2, each input of $f_1(t) \ldots, f_n(t)$ is controlled by switches $S_1 \ldots, S_n$ exclusively, and a selected input is transmitted to the ADC. Plus, in an application of biological sensor systems, an input signal is so tiny, an input analog buffer is placed at each input. However, a VLSI implementation yields a variation of gains among the input analog buffers due to a process-induced variation, and it degrades the precision of sensing values.

To avoid degrading the precision of analog values, an analog multipliers and adder are used as shown in Fig. 3. In this figure, Vin1 and Vin2 are amplified by the weight signals, w1 and w2, respectively. The input is connected to the variable resistor R1 which is realized by a transconductor of PMOS or NMOS transistor [6]. The weight value is determined by

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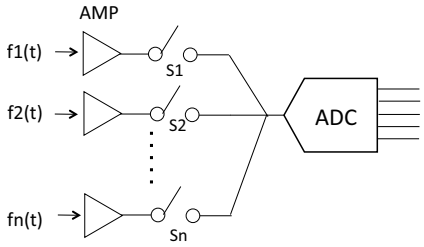

Fig. 2. An example of analog front-end with time division multiplexed input.

a ratio of R1 and R2. However, this implementation also has defects in the temperature dependency and the input range, which are described below.

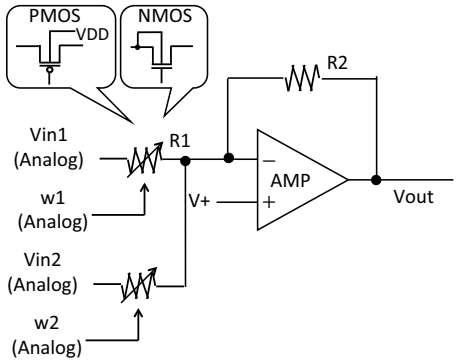

Fig. 3. Analog multiplier and adder for perceptron.

III. DAC-BASED MULTIPLIER

A. DAC-based Programmable Gain Amplifiers

We adopt two types of programmable gain amplifiers introduced in [4] to realize a multiplier overcoming defects described above. The schematics of the programmable gain amplifiers are illustrated in Fig. 4 and 5 (called pattern (1) and (2), respectively). Both patterns basically configure the negative feedback of the opamp, but the resistor in the feedback is replaced by the DAC.

In detail, the DAC is inserted at the input of the negative feedback circuit in pattern (1), while it is at the loop of the feedback in pattern (2). Changing of the DAC output current looks as if the resistance value were to change.

We design these patterns and verify the function by the simulation. All circuits are designed with a model of $0.6\mu m/5V$ manufacturing process. The V_{tn} and V_{tp} of NMOS and PMOS are $0.7V$ and $0.9V$, respectively. Plus, β_n and β_p are $1.0\times10^{-4}A/V^2$, $0.4\times10^{-4}A/V^2$. A typical two-stage opamp used in this paper is shown in Fig. 6, where the DC gain= 101.82(dB), the unity gain frequency=24.48(MHz) the phase margin=62.46(deg.), and the DC offset=5.0(mV). As well, the schematic of the 4bit DAC is illustrated in Fig. 7.

In the simulation, we observe the changing of the output amplitude for pattern (1) and (2) when changing the DAC input

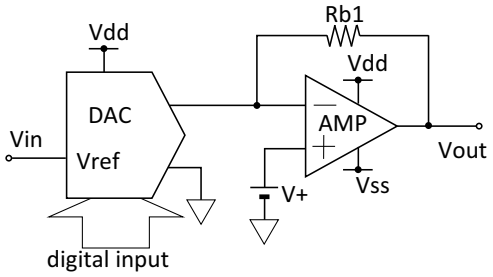

Fig. 4. A programmable gain amplifier pattern (1).

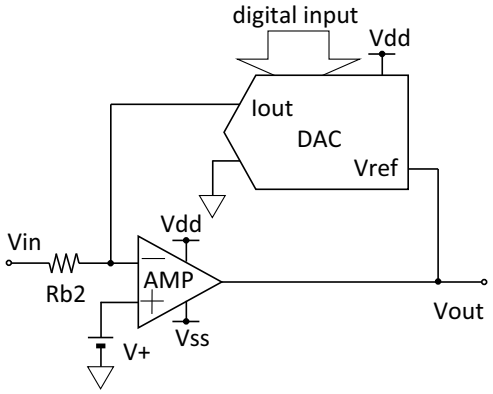

Fig. 5. A programmable gain amplifier pattern (2).

codes from zero to the fullscale, and the results are shown in Fig. 8 and 9, respectively. In Fig. 8, we can observe the output amplified by $N \cdot R_{b1}$. As well, the output shown in Fig. 9 is amplified by $1/N \cdot R_{b2}$.

In addition, we realize a multiplier combining the circuit pattern (1) and (2) as illustrated in Fig. 10. The output waveforms are shown in Fig. 11 when we give a sine signal with the amplitudes of 5mV and 1.0 KHz frequency to the input V_{ref}. According to $V_{out} = -\frac{X1}{X2}V_{in}$, the simulation results show the output amplitude of $1\times$, $10\times$, and $100\times$ are 4.98mV, 49.40mV, and 500.66mV for the input signal of 5mV, respectively. Notice that this multiplier has one analog input and the other of digital. The analog input is amplified by only

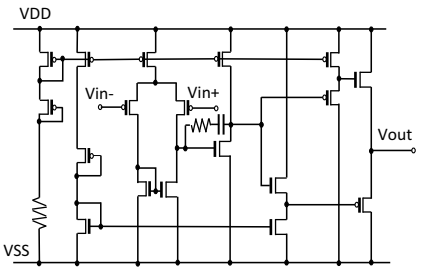

Fig. 6. A schematic of opamp

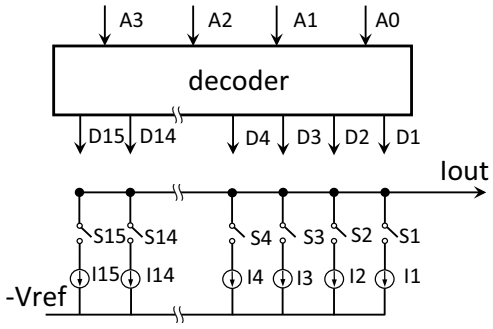

Fig. 7. Our current-type DAC

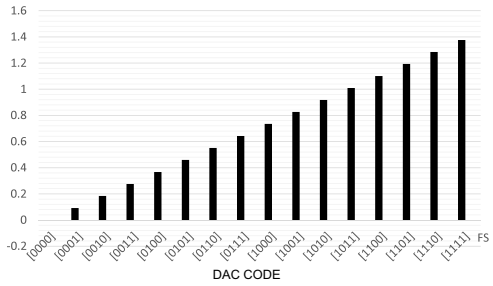

Fig. 8. Changing of the output amplitude for each input code of DAC: circuit pattern (1)

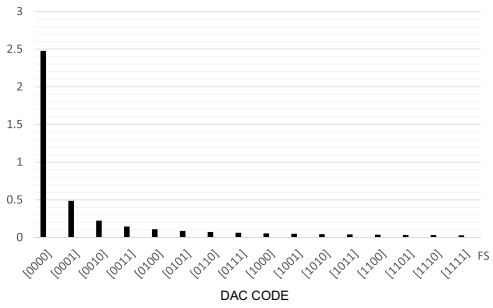

Fig. 9. Changing of the output amplitude for each input code of DAC: circuit pattern (2)

digital codes, so that the precision is not affected by a process-induced variation.

B. Comparison with Traditional Analog Multiplier

Furthermore, we investigate the temperature dependency and input range compared with traditional analog multiplier shown in Fig. 3. Fig. 12 and 13 show the simulation results with respect to the temperature dependency and the input range, respectively. Our DAC-based multiplier demonstrates better performance in the both results.

C. Simulation of Multiple Inputs

We design a perceptron circuit composed of DAC-based multipliers. The schematic is shown in Fig. 14, where three

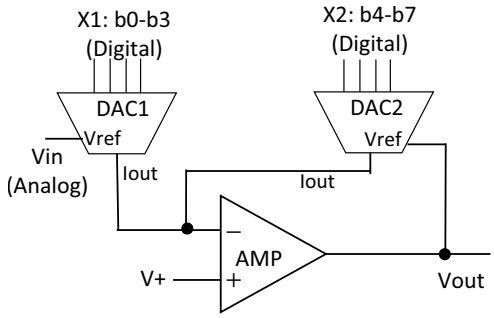

Fig. 10. The multiplier with a combination circuit pattern (1) and (2)

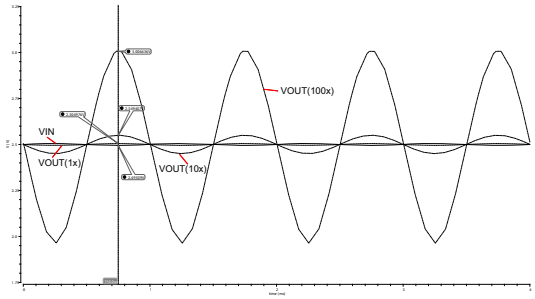

Fig. 11. The output waveform of the multiplier with a combination circuit pattern (1) and (2): input signal, 10 × and 100 × output signals.

inputs are connected to DAC1, 2 and 3. The gains of multipliers are determined by ratios of X1/X4, X2/X4 and X3/X4, respectively, and all multiplied values are summed at the output.

To clarify a function of this circuit, we apply the simulation with the setting as; Vin1, Vin2 and Vin3 are sin signals of 5mV, 10mV and 15mV amplitude at 1kHz frequency. DAC1, DAC2 and DAC3 are set as the gains of the multipliers to be 3×, 2× and 1×, respectively. The simulation results are shown in Fig. 15(a). We can correctly observe 65mV amplitude at the output signal.

Next, we change the frequency of each input as; Vin1, Vin2 and Vin3 are sin signals of 10kHz, 5kHz and 1kHz frequencies, respectively. The other settings as same as in Fig. 15(a). Fig. 15(b) demonstrates the simulation results. Our perceptron circuit can output a complicated waveform, so that it has a potential for complicated machine learning.

IV. Conclusion

This paper presents a perceptron circuit applicable to a sensor analog front-end. We adopt a DAC-based multiplier in the perceptron circuit, where the gain of the multiplier is determined by only digital codes. It contributes to the precision without degrading the process-induced variation. As well, compared with a traditional transconductor-based multiplier, it has a wide input range and a good temperature dependency. The simulation result demonstrates a perceptron circuit with

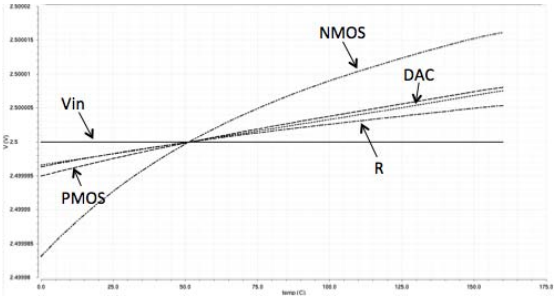

Fig. 12. Temperature dependency compared with traditional analog amplifier.

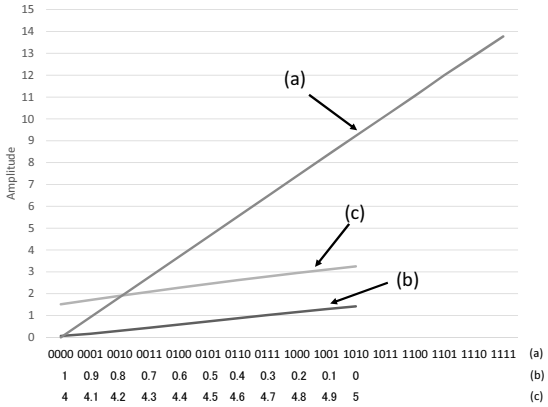

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Fig. 13. Input range compared with traditional analog amplifier. (a) digital code, (b) gate voltage of PMOS, (c) gate voltage of NMOS

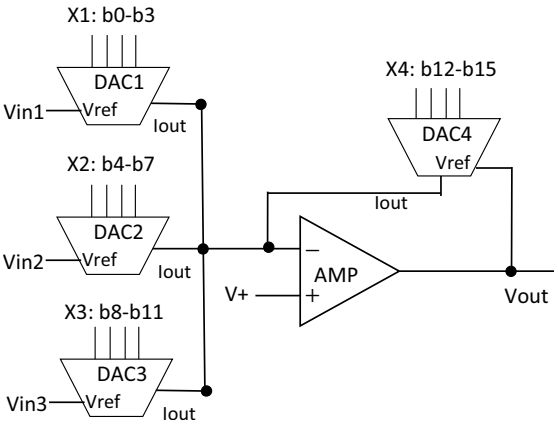
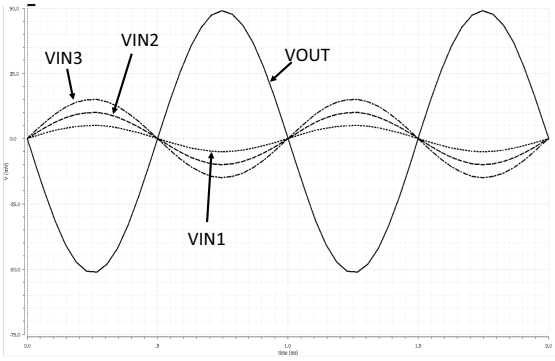


Fig. 14. Our perceptron circuit for three inputs.

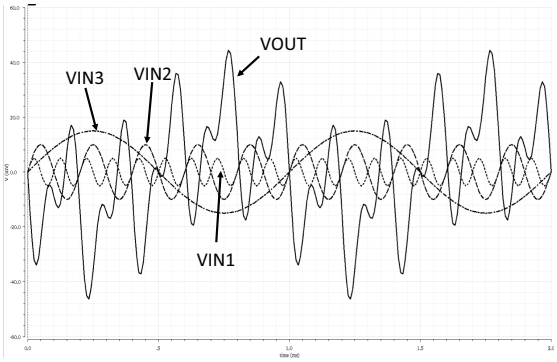
the DAC-based multiplier can combine smoothly multiple analog signals amplified by the digital codes.

REFERENCES

[1] S. M. Gowda, B. J. Sheu, J. Choi, *Design and characterization of analog VLSI neural network modules*, IEEE Journal of Solid-state Circuit, Vol.28, No.3, pp.301–313, 1993,



(a) Vin1: 5mV, 1kHz, Vin2: 10mV, 1kHz, Vin1: 15mV, 1kHz DAC1: 3×, DAC2: 2×, DAC3: 1×



(b) Vin1: 5mV, 10kHz, Vin2: 5mV, 1kHz, Vin1: 15mV, 1kHz DAC1: 3×, DAC2: 2×, DAC3: 1×

Fig. 15. Our perceptron circuit for three inputs.

[2] B. V. Essen, C. Macaraeg, M. Gokhale, R. Prenger, *Accelerating a Random Forest Classifier: Multi-Core, GP-GPU, or FPGA?*, IEEE 20th International Symposium on Field-Programmable Custom Computing Machines, pp.232–239, 2012.

[3] Qi Yu, Chao Want, Xiang Ma, Xi Li, Xuehai Zhou, *A Deep Learning Prediction Process Accelerator Based FPGA*, IEEE/ACM 2015 International Symposium on Cluster, Cloud and Grid Computing, pp.1159–1162, 2015.

[4] John Wynne, *Application Notes, AN-320A*, ANALOG DEVICES.

[5] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Education, 2000.

[6] Gunhee Han and Edgar Sanchez-Sinencio, *CMOS Transconductance Multipliers: A Tutorial*, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol.45, No.12, pp.1550–1563, 1998.

[7] J. Xu, S. Mitra, A. Matsumoto, S. Patki, C. V. Hoof, K. A. A. Makinwa, R. F. Yazicioglu, *A Wearable 8-Channel Active-Electrode EEG/ETI Acquisition System for Body Area Networks*, IEEE Journal of Solid-state Circuit, Vol.49, No.9, pp.2005–2016, 2014.

[8] C.-L. Goh, S. Nakatake, *A Sensor-Based Data Visualization System for Training Blood Pressure Measurement by Auscultatory Method*, IEICE Trans. on Information and Systems, Vol.E99-D, No.4, pp.936–943, 2016.