Experimental Body-input Three-stage DC offset Calibration Scheme for Memristive Crossbar

Charanraj Mohan[1], L.A. Camuñas-Mesa[1], Elisa Vianello[2], Carlo Reita[2], José Manuel de la Rosa[1], Teresa Serrano-Gotarredona[1] & Bernabé Linares-Barranco[1]

[1]Instituto de Microelectrónica de Sevilla IMSE – CNM (CSIC, Universidad de Sevilla), Sevilla, Spain,

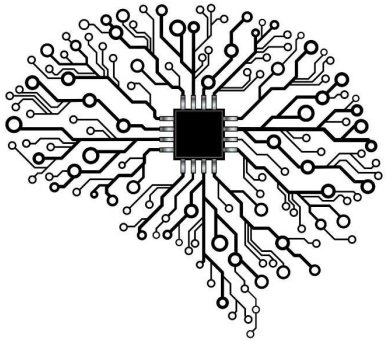
[2]CEA-LETI, Grenoble, France

2020 IEEE International Symposium on Circuits and Systems
Virtual, October 10-21, 2020

OUTLINE

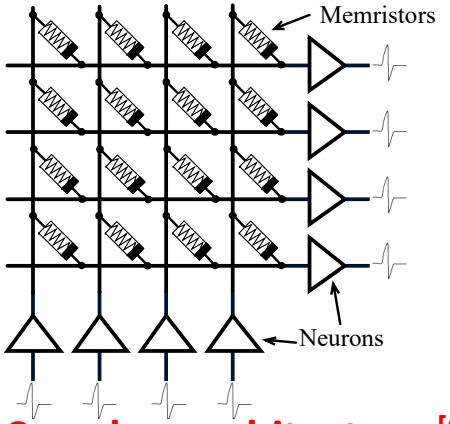
- Introduction (6 slides)
- Motivation of the work (1 slide)
- Bulk-based DC offset calibration scheme for crossbars- design (3 slides)
- Different views of the packed chip & its layout (2 slides)
- Experimental set-up (1 slide)
- Experimental results (1 slide)
- Conclusion & future work (1 slide)

Introduction

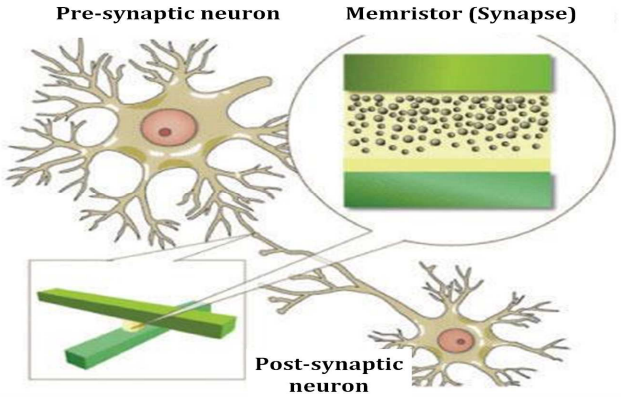


Brain-inspired computing [1]

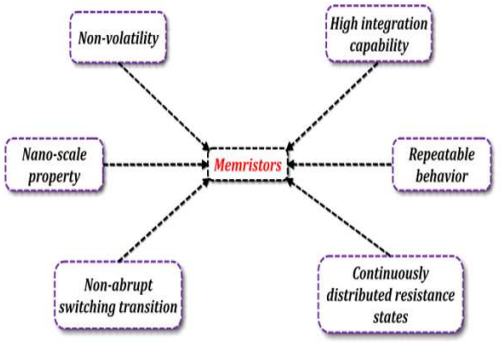
Pool of tech gaints & their neuromorphic chips [2, 3, 4, 5]



Crossbar architecture [6]



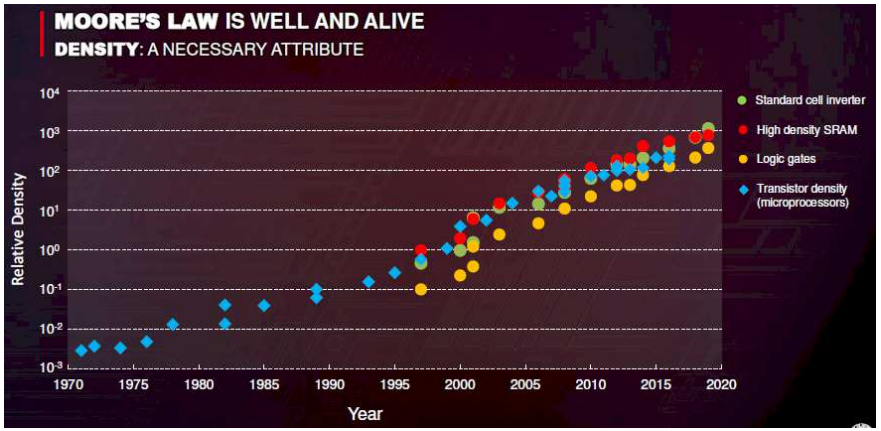
Memristors- a favourable synapse [7, 8]

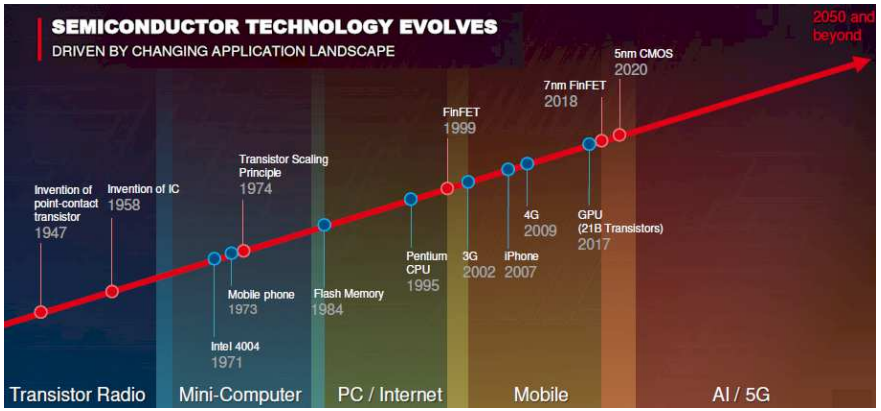


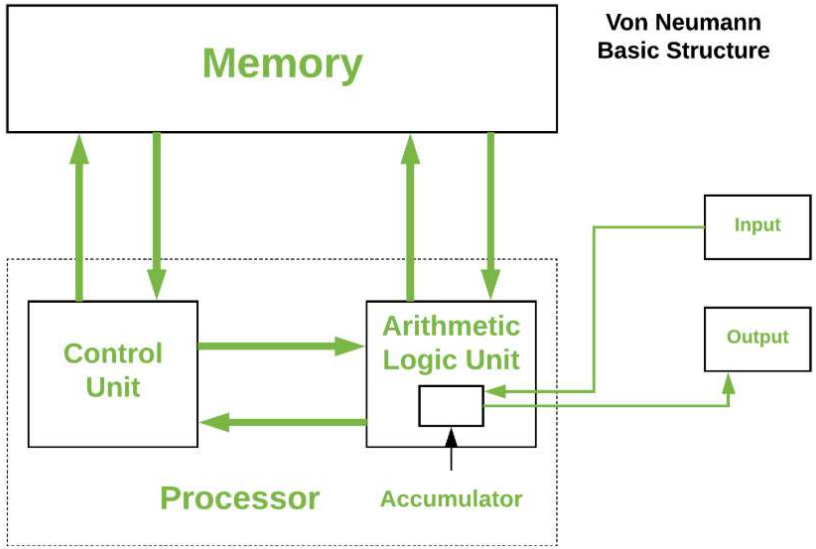
Properties of memristors

[1] Carver Mead, 'Analog VLSI and Neural Systems', Addison Wesley, 1989.
[2] www.web.stanford.edu/group/brainsinsilicon/neurogrid.html
[3] http://paulmerolla.com/merolla_main_som.pdf (Truenorth)
[4] www.brainscales.kip.uni-heidelberg.de/
[5] www.apt.cs.manchester.ac.uk/projects/SpiNNaker/
[6] O. Turel and K. Likharev, "Cross-nets possible neuromorphic networks based on nanoscale components", Int. J. Circuit Theory App., vol. 31, no. 1, pp. 37-53, January, 2003.
[7] L. Chua, 'Memristors-the missing circuit element', Circuit Theory, IEEE Transactions on, vol. 18, no. 5, pp. 507-519, 1971.
[8] D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, 'The missing memristor found', Nature, vol. 453, no. 7191, pp. 80-83, 2008.

Introduction (Contin.)







- **Paradigm shift: Parallel elements with memory & co-localized computation**
- **Memristors as synapse → didn't solve Von Neumann bottleneck**

Moore's Law [1]

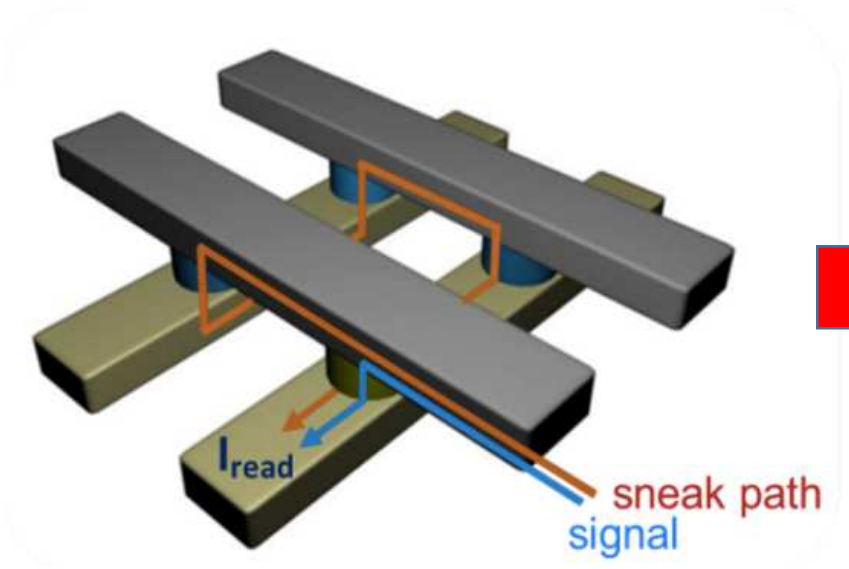
Von Neumann bottleneck [2, 3]

[1] Moore, Gordon E. (1965). "Cramming more components onto integrated circuits" (http://download.intel.com/museum/Moores_Law/Articles-Press_Releases/Gordon_Moore_1965_Article.pdf)(PDF). Electronics Magazine. p. 4. . Retrieved 2006-11-11.

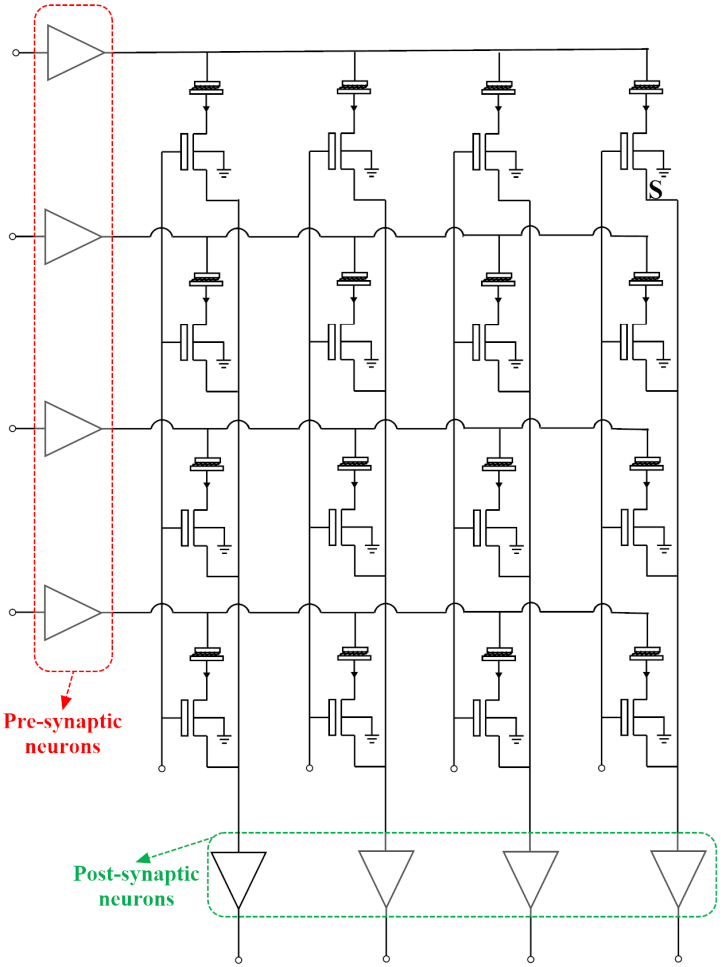
[2] James M. Feldman and Charles T. Retter. Computer Architecture: A Designer's Text Based on a Generic RISC. McGraw-Hill, Inc., New York, 1994.

[3] M. D. Godfrey and D. F. Hendry. The computer as von Neumann planned it. IEEE Annals of the History of Computing, 15(1):11{21, 1993.

Introduction (Contin.)



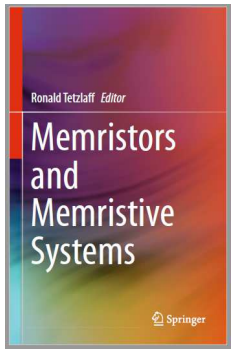
Sneak-path [1] in a selector-less crossbar

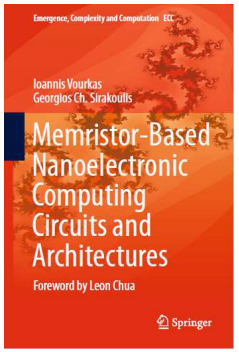


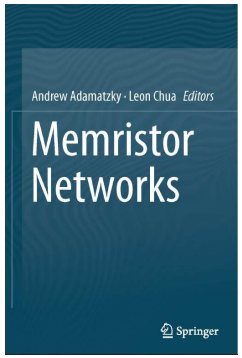
4 × 4 1T1R crossbar with pre & post synaptic neurons

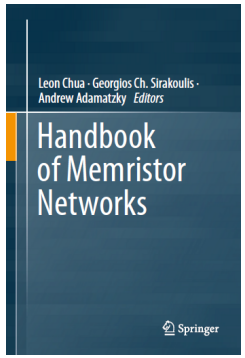
[1] Y. Cassuto, S. Kvatinsky and E. Yaakobi,"Sneak-path constraints in memristor crossbar arrays", Information Theory Proceedings (ISIT), 2013 IEEE International Symposium on.,10.1109/ISIT.2013.6620207, October 2013.

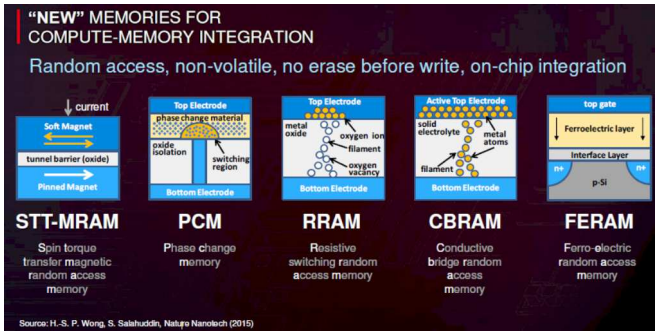
Introduction (Contin.)





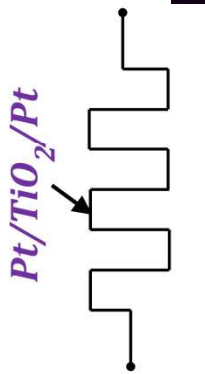


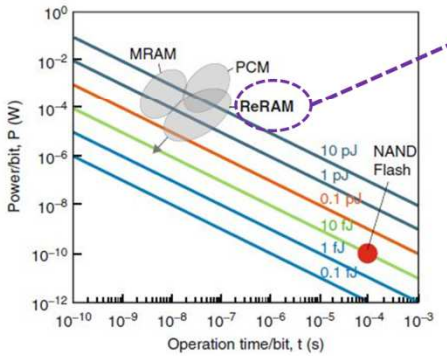




List of oxides used for memristive devices & their behavior [2]

Oxide	TE-BE	ON/OFF ratio	Switching speed	Retention time(s)	Endurance
Binary, bipolar					
CoO	Ta–Pt	10^3	20 ns	–	100
Cu_xO	Ti/TiN–Cu	10^2	50 ns	10^5 @ 90°C	600
$HfLaO_x$	TaN–Pt	10^6	10 ns	10^4 @ 27°C	10^4
HfO_x/TiO_x	TiN–TiN	10^3	5 ns	10^4 @ 200°C	10^5
TaO_x	Pt–Pt	10^1	10 ns	10^7 @ 150°C	10^9
TiO_2	Pt–TiN	10^3	5 ns	10^6 @ 85°C	10^6
ZrO_2	TiN–Pt	10^1	1 µs	10^4 @ 27°C	10^3
Binary, unipolar					
Gd_2O_3	Pt–Pt	10^6	–	10^5 @ 85°C	60
HfO_2	Pt–Pt	10^2	–	10^6 @ 27°C	140
Lu_2O_3	Pt–Pt	10^3	30 ns	10^6 @ 27°C	300
NiO	Pt–Pt	10^2	5 µs	10^7 @ 27°C	10^6
TaO_x	Cu–Pt	10^2	80 ns	10^6 @ 27°C	100
TiO_x	Pt–Pt	10^4	–	–	25
WO_x	TiN–W	4	300 ns	10^4 @ 100°C	10^7
ZnO	Pt–Pt	10^4	–	–	100
Perovskite, bipolar					
$Cr:Ba_{0.7}Sr_{0.3}TiO_3$	Pt–$SrRuO_3$	4	0.2 s	10^4 @ 27°C	10^4
$Pr_{0.7}Ca_{0.3}MnO_3$	Ag–$YBa_2Cu_3O_{7-x}$	10^2	8 ns	–	10^5
$Pr_{0.7}Ca_{0.3}MnO_3$	Al–Pt	10^2	20 µs	10^4 @ 125°C	10^3
$Cr:SrTiO_3$	Au–Au	10	1 ms	8×10^4 @ 27°C	10^3
$Nb:SrTiO_3$	Pt	10^2	50 µs	10^8 @ 125°C	10^7
$Cr:SrZrO_3$	Au–$SrRuO_3$	20	100 ns	10^7 @ 27°C	–
$Cr:SrZrO_3$	Al–$LaNiO_3$	10^2	500 µs	10^3 @ 85°C	–

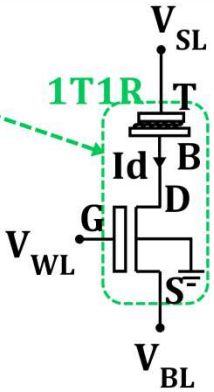




Comparison of switching energy performance for ReRAM, NAND flash, MRAM & PCM technologies [1]

TiO_2
HfO_2
NiO
Al_2O_3
Nb_2O_5
$SrTiO_3$
$Pr_{0.7}Ca_{0.3}MnO_3$
CuO_2
Ag_2S
$AgGeSe$

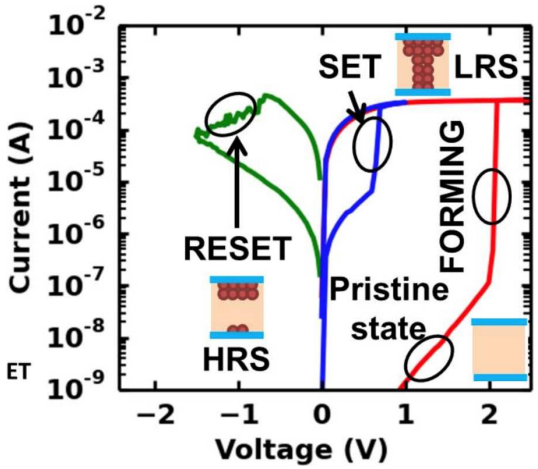
- Conductive filament
- Schottky barrier
- Charge trapping
- Electrochemical migration of point defects



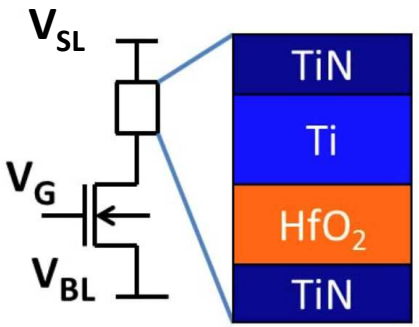
[1] B. Govoreanu, S. Kubicek, G. Kar, Y-Y, Chen, V. Paraschiv, M. Rakowski, R. Degraeve, L. Goux, S. Clima, N. Jossart et al., inExt. Abstr SSDM Conf., Nagoya, Japan, (*The Japan Society of Applied Physics*, 2011), p. 1005.

[2] S.D. Ha, S. Ramanathan, 'Adaptive oxide electronics: a review', *J. Appl. Physic*, 110, 071101 (2011).

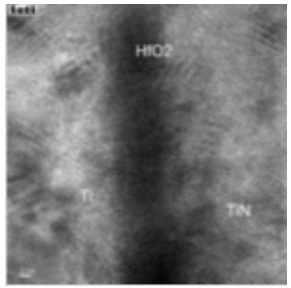
Introduction (Contin.)



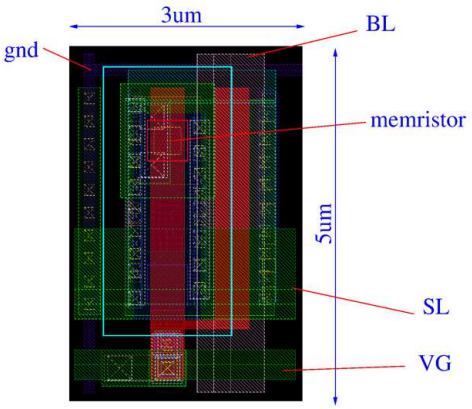
I-V characteristics of a 1T1R device



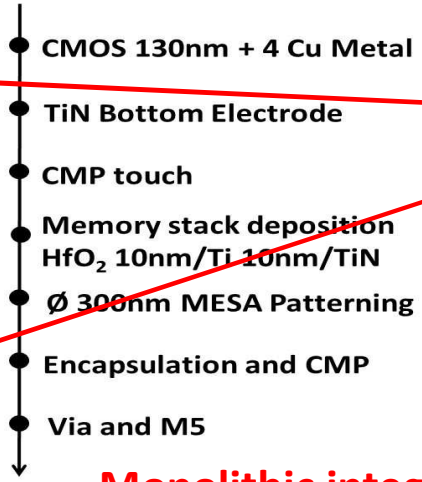
1T1R device [1, 2]

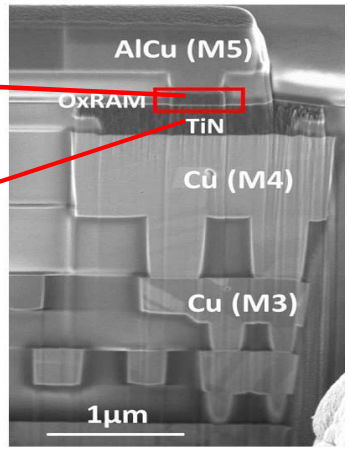


Microscopic view of Ti-HfO_2-TiN



Layout of 1T1R





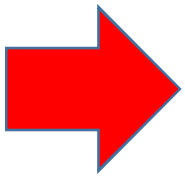
Monolithic integration based on hybrid CMOS & OxRAM

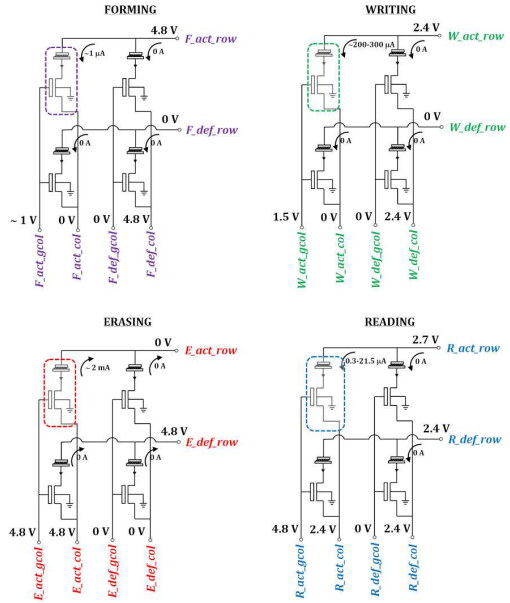
V_{FORM} = 4.8 V; V_G = 1 V; t_{FORM} = 10 µs; I_C = 1 µA

V_{ERASE} = 4.8 V; V_G = 4.8 V; t_{ERASE} = 100 ns

V_{WRITE} = 2.4 V; V_G = 1.5 V; t_{WRITE} = 100 ns

Various operations performed in 1T1R crossbar by choosing a device





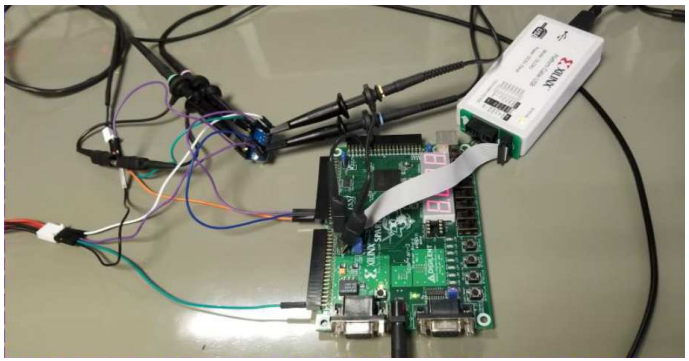
[1] D. Garbin et al., "Variability-tolerant Convolutional Neural Network for Pattern Recognition applications based on OxRAM synapses," 2014 IEEE International Electron Devices Meeting, San Francisco, CA, 2014, pp. 28.4.1-28.4.4.

[2] D. Garbin et al., "HfO2-Based OxRAM Devices as Synapses for Convolutional Neural Networks," IEEE Transactions on Electron Devices, vol. 62, pp. 2494–2501, August 2015.

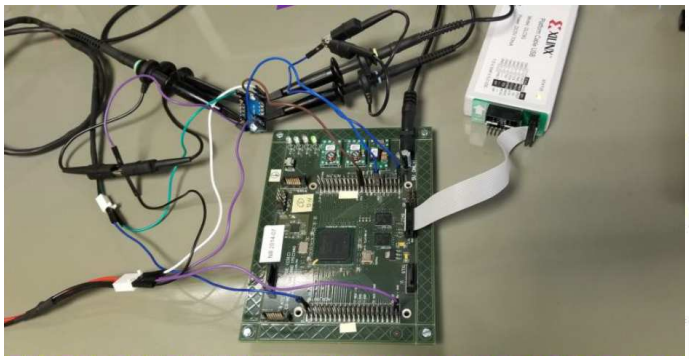
(Microscopic Image courtesy: CEA-Leti)

Introduction (Contin.)

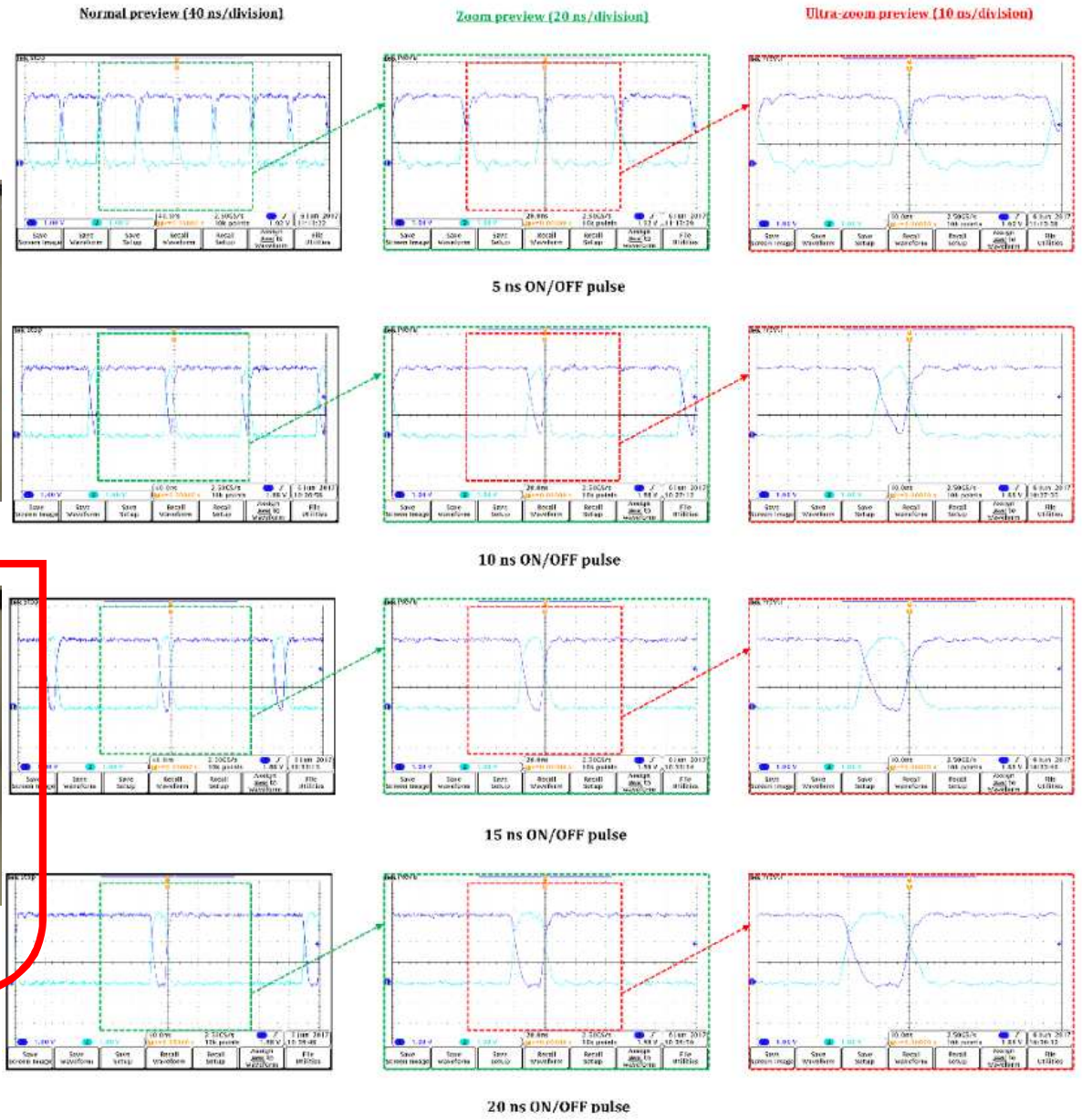
Driver board's fast pulses



SPARTAN 3 board

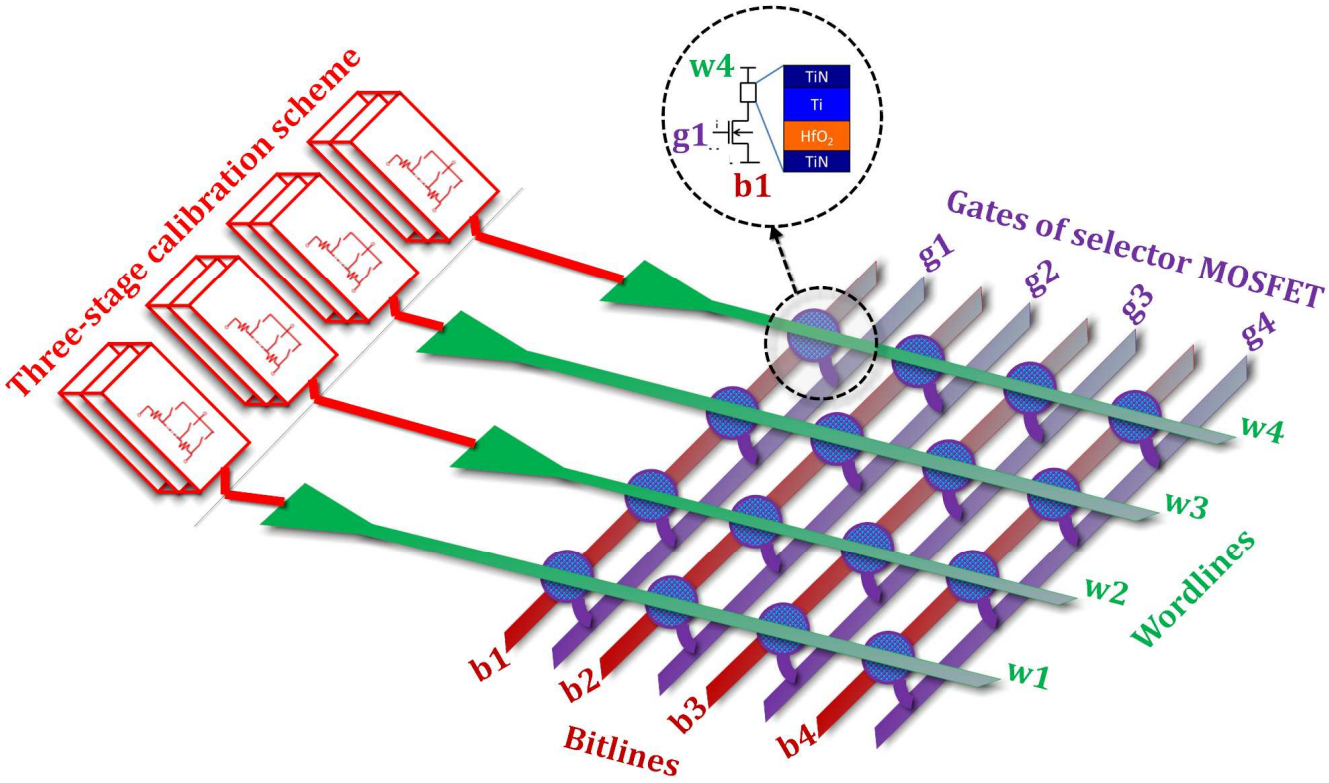


SPARTAN 6 board (node board) [1]



[1] http://www2.imse-cnm.csic.es/neuromorphs/index.php/AER-Vision-Processors

Motivation of the work



DC offset voltage

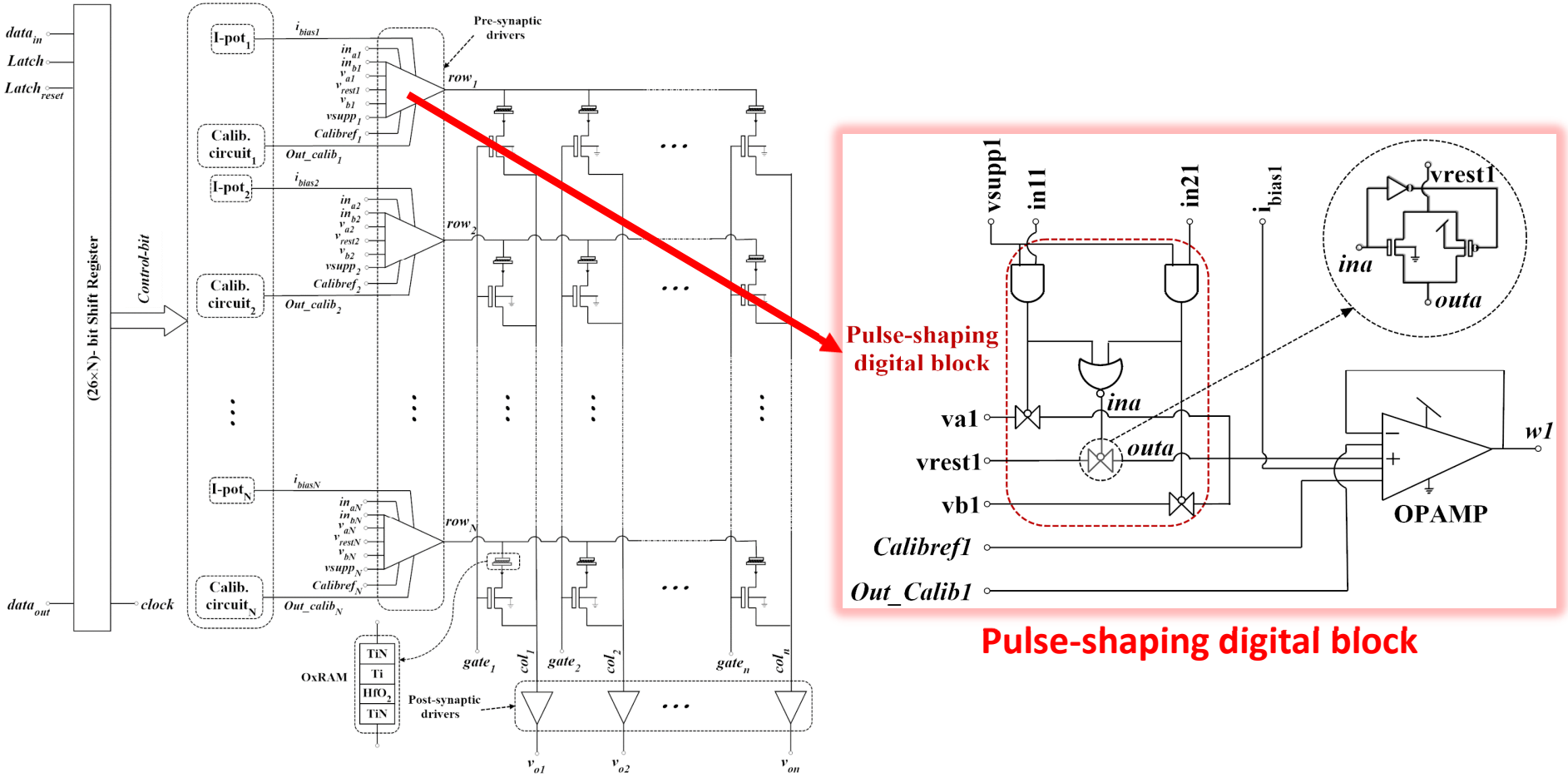
V_{read} = 0.3 V

V_{read} = 0.1 V

V_{read} = 0.02 V or below

Power consumption during inference

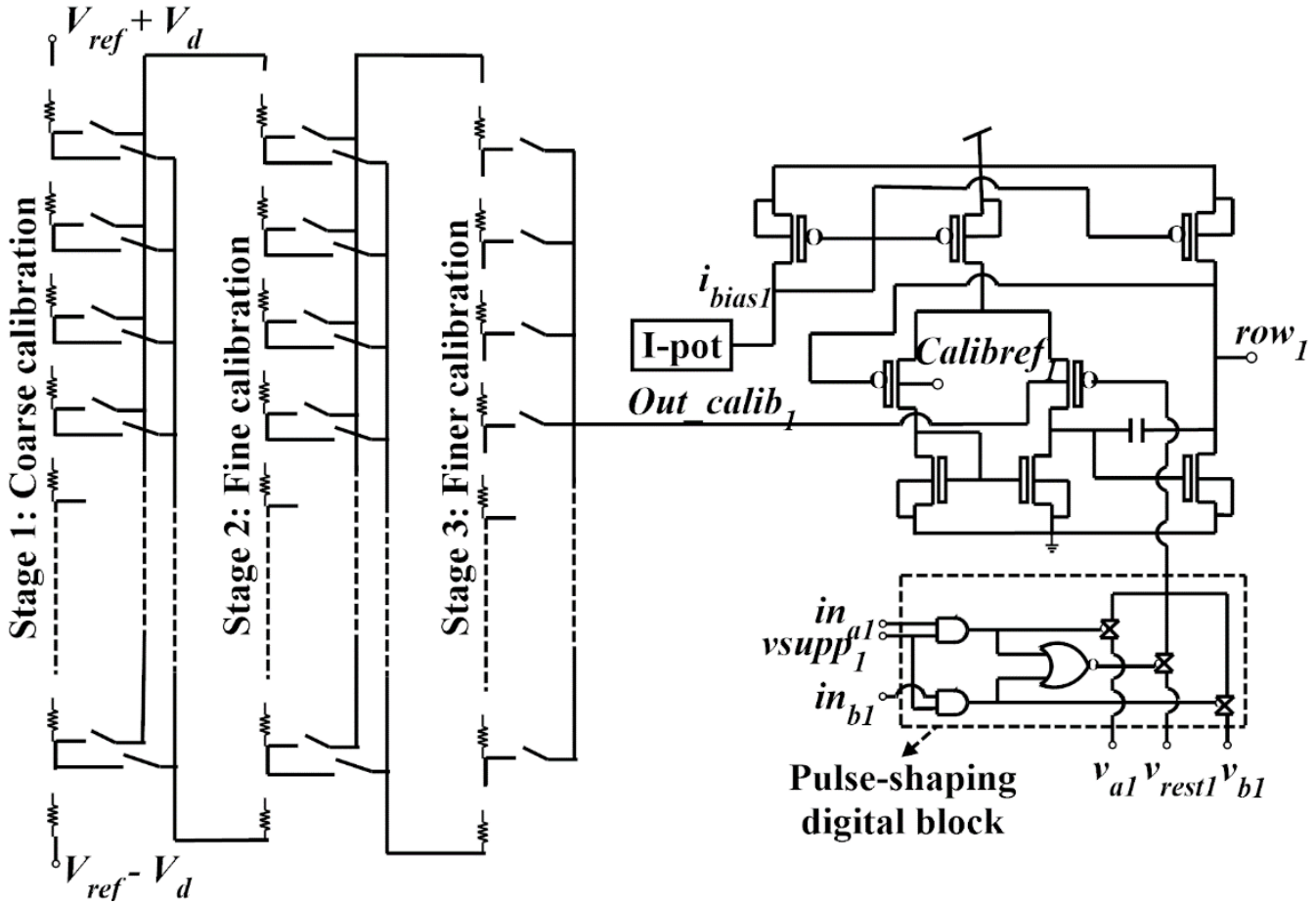
Bulk-based DC offset calibration scheme for crossbar- design



Pulse-shaping digital block

4 × 4 1T1R crossbar with calibration of DC offset

Bulk-based DC offset calibration scheme for crossbar- design (Contin.)

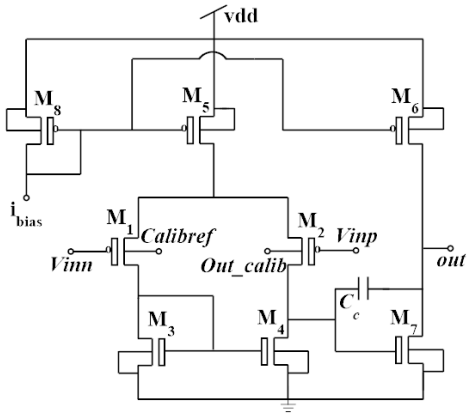


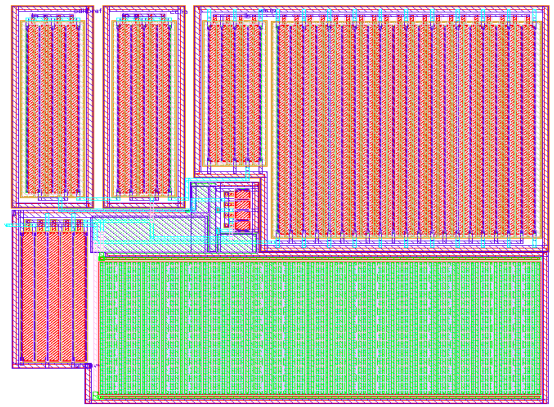
3 – stage calib. scheme [1] with opamp & I-pot [2]

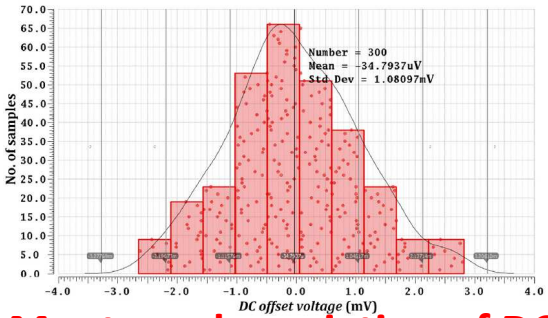
[1] C. Mohan, L.A. Camuñas-Mesa, E. Vianello, L. Perniola, C. Reita, J.M. de la Rosa, T. Serrano-Gotarredona and B. Linares-Barranco, “Calibration of offset via bulk for low-power HfO2 based 1T1R memristive crossbar read-out system”, Microelectronic Engineering, Elsevier, vol. 198, 15 October 2018, pages 35-47.

[2] R. Serrano-Gotarredona, L. A. Camuñas-Mesa, T. Serrano-Gotarredona, Juan.A. Leñero-Bardallo and B. Linares-Barranco,"The Stochastic I-Pot: A Circuit Block for Programming Bias Currents", IEEE Transactions on Circuits and Systems-II: Express Briefs., vol. 54, no. 9, pp. 760-764, September 2007.

Bulk-based DC offset calibration scheme for crossbars-design (Contin.)





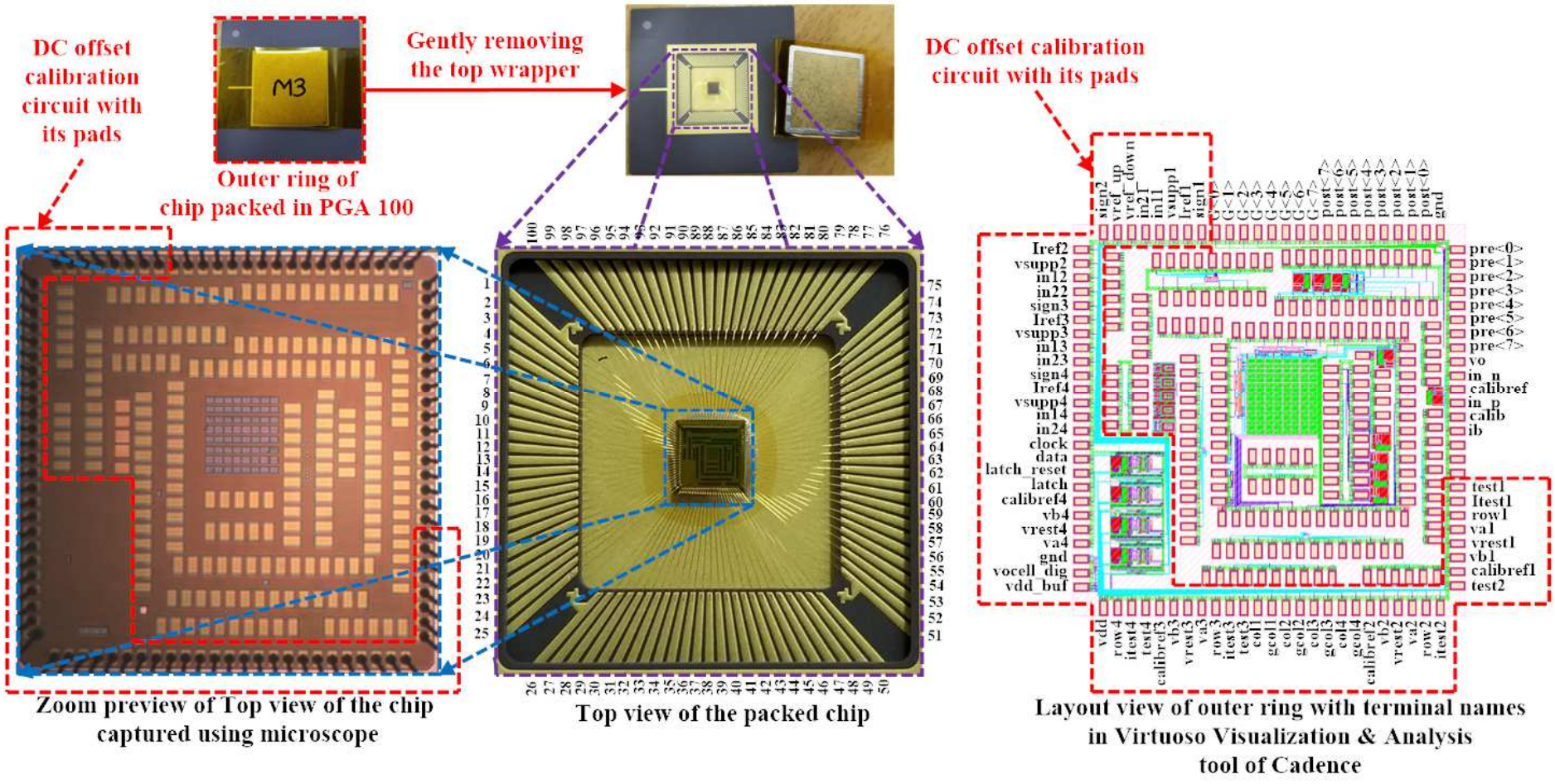


Monte carlo variation of DC offset voltage of the opamp

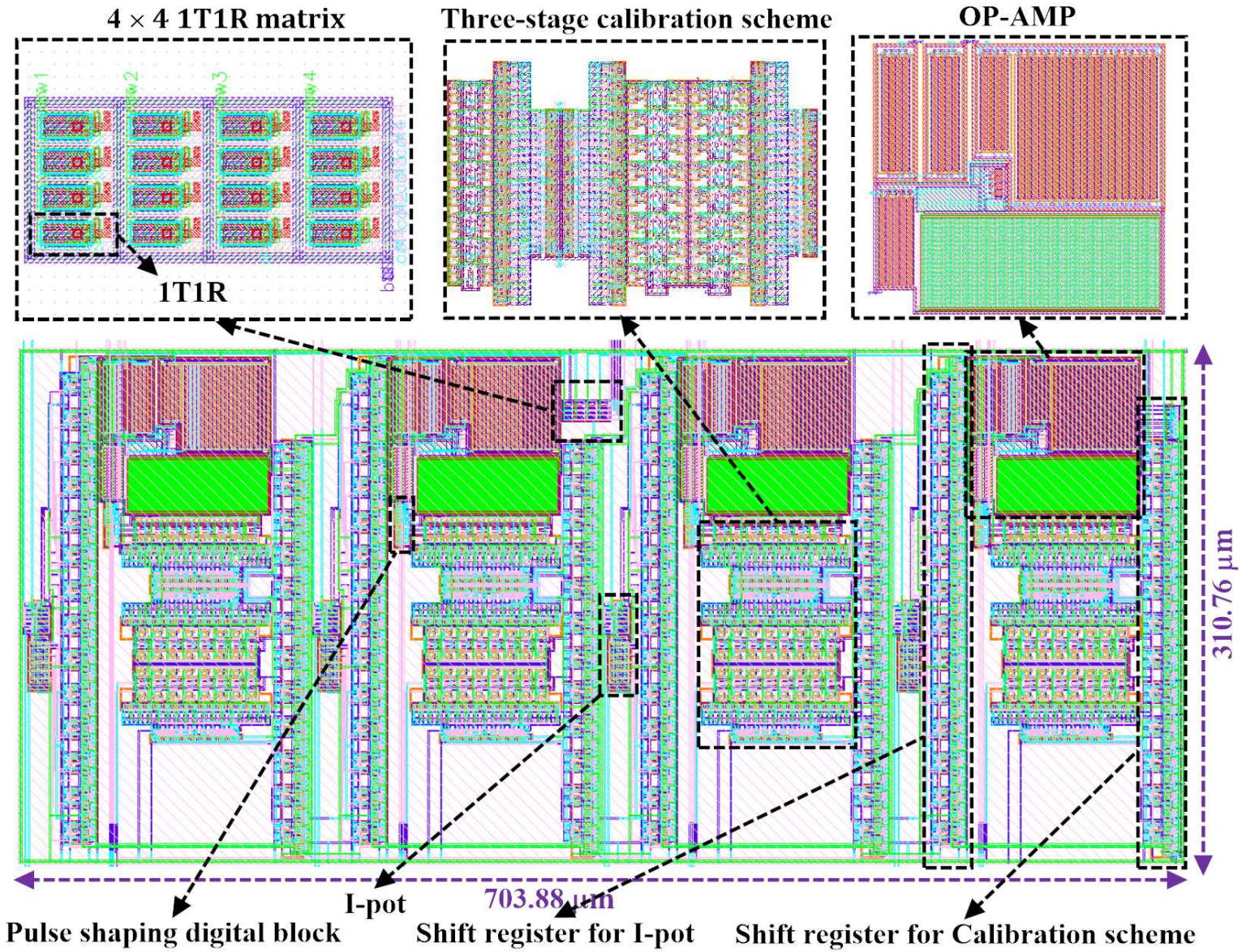
Specifications	Proposed values	Actual designed value			
		With C load	With RC load		
			R=2 kΩ	R=7 kΩ	R=225 kΩ
P-MOSFET Differential pair, $\left(\frac{W}{L}\right)_{1,2} = 80$	-	$\left(\frac{40\mu m}{2\mu m}\right)$ connected in 4 parallel numbers			
n-MOSFET Current mirror down to differential pair, $\left(\frac{W}{L}\right)_{3,4} = 2.5$	-	$\left(\frac{2.5\mu m}{2\mu m}\right)$ connected in 2 parallel numbers			
P-MOSFET Input current mirror, $\left(\frac{W}{L}\right)_{5,8} = 32.5$	-	$\left(\frac{32.5\mu m}{2\mu m}\right)$ connected in 2 parallel numbers			
Second stage P-MOSFET, $\left(\frac{W}{L}\right)_{6} = 497.5$	-	$\left(\frac{49.75\mu m}{2\mu m}\right)$ connected in 20 parallel numbers			
Second stage N-MOSFET, $\left(\frac{W}{L}\right)_{7} = 76.5$	-	$\left(\frac{30.6\mu m}{2\mu m}\right)$ connected in 5 parallel numbers			
Gain (Av) in dB	≥ 68	100.944	69.3312	79.6551	98.4536
Gain Bandwidth Product (GWB) in MHz	30	15.6501	13.2864	14.9	15.626
Phase Margin	60°	59.9955°	66.1448°	62.0176°	60.0652°
ICMR+ in V	4.3	4.5			
ICMR- in V	0.9	0.7			
Load Capacitor (CL) in pF	5	4.956			
Compensation Capacitor (CC) in pF	-	2.44181			
Slew rate (SR) in V/µs	20	15.53455	13.5063	14.7851	15.50825
Input current (I5) in µA	40	40.21154	40.21154	40.21154	40.21154
Second stage drain current (I6 or -I7) in µA	630-680	634.4841	623.7895	624.3674	631.2522
Total Power dissipation (Pdiss) in mW	≤ 4	3.2385	3.1872	3.18998	3.22303
DC component of the common mode voltage in AC analysis in µV	-	-14			
DC systematic offset from DC sweep analysis in µV	-	89.5937			
Parasitic capacitance reduction	-	para. capacitance Of 16 MOSFETs are reduced by 50 %			
DC offset by Monte carlo runs	-	Mean=-34.7937 µv Sigma=1.08097 mV for 300 runs	-	-	-
Total Input referred noise in V^2		8.34E-11			

Design specs of 2 – stage PMOS-based differential opamp with schematic & layout views

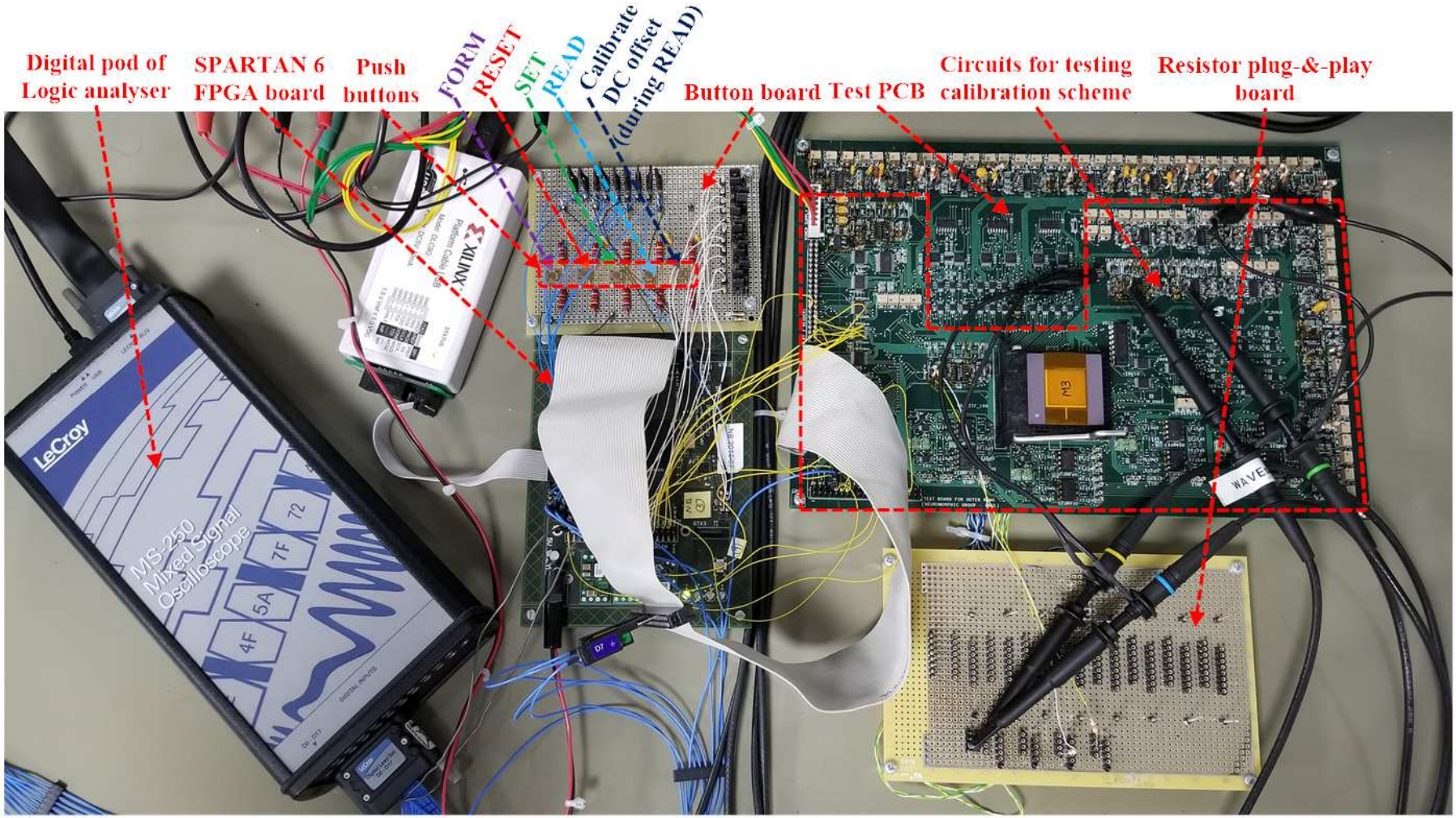
Different views of the packed chip & its layout



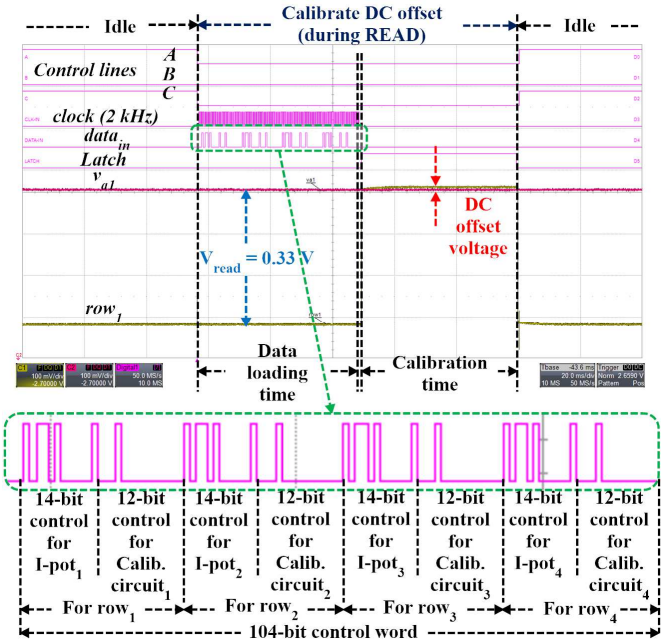
Different views of the packed chip & its layout (Contin.)



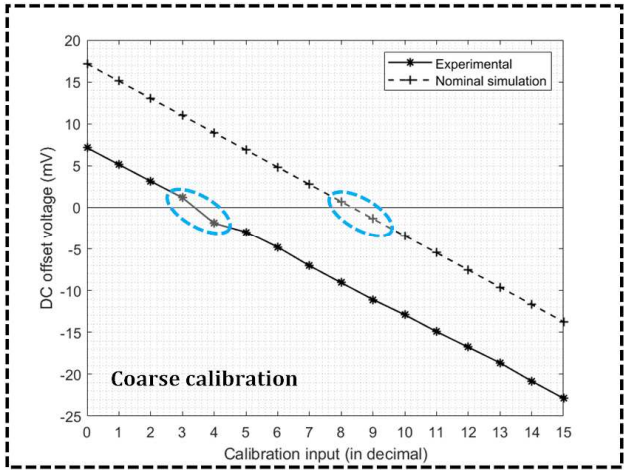
Experimental set-up

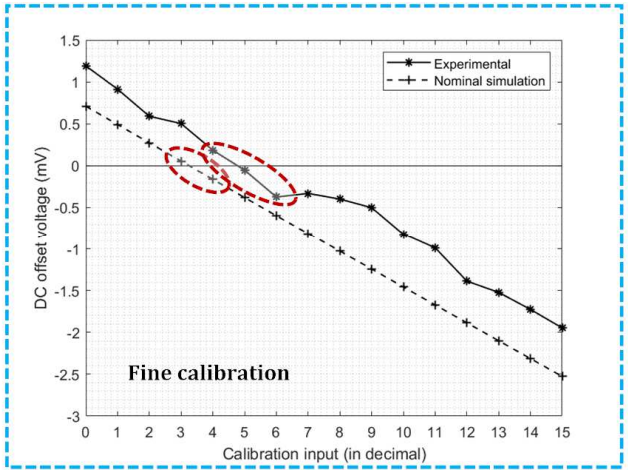


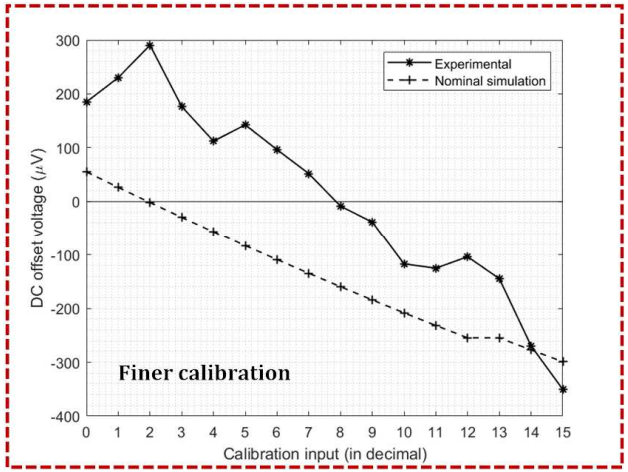
Experimental results



Digital and analog signals observed in oscilloscope during calibration







Experimental results of the 3 – stage calibration scheme [1]

Conclusion & Future work

- **Design of a 2 – stage PMOS- based differential pair opamp- used in buffer configuration for memristive crossbars.**
- **Bulk-based calibration of DC offset across rows of 1T1R crossbar-> Low power dissipation & scalability of crossbar.**