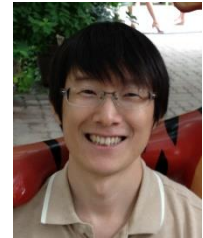


A 1280x960 Dynamic Vision Sensor with a 4.95- μm Pixel Pitch and Motion Artifact Minimization



Yunjae Suh, Seungnam Choi, Masamichi Ito, Jeongseok Kim, Youngho Lee, Jongseok Seo, Heejae Jung, Dong-Hee Yeo, Seol Namgung, Jongwoo Bong, Sehoon Yoo, Seung-Hun Shin, Doowon Kwon, Pilkyu Kang, Seokho Kim, Hoonjoo Na, Kihyun Hwang, Changwoo Shin, Jun-Seok Kim, Paul K. J. Park, Joonseok Kim, Hyunsurk Ryu and Yongin Park

Samsung Electronics, South Korea

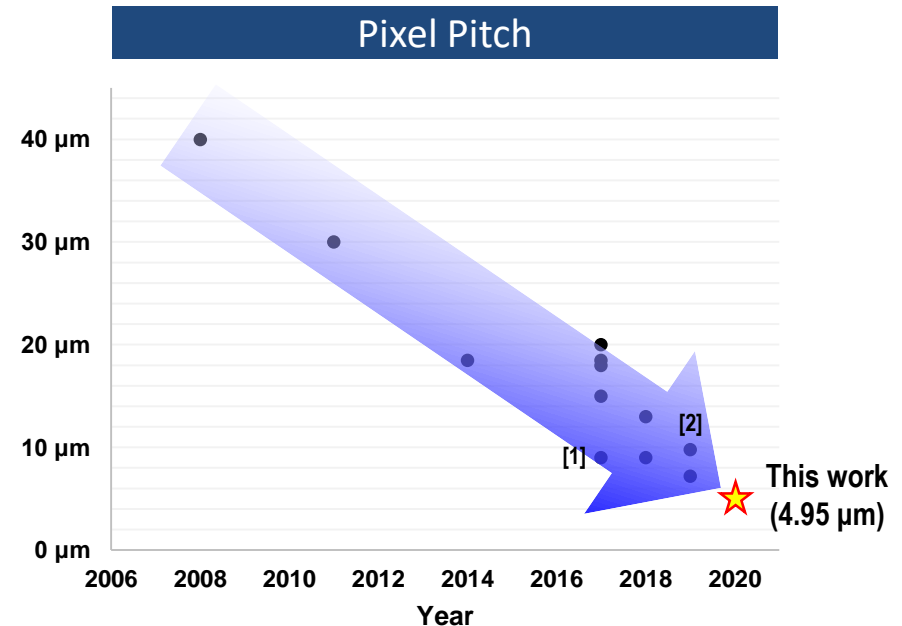
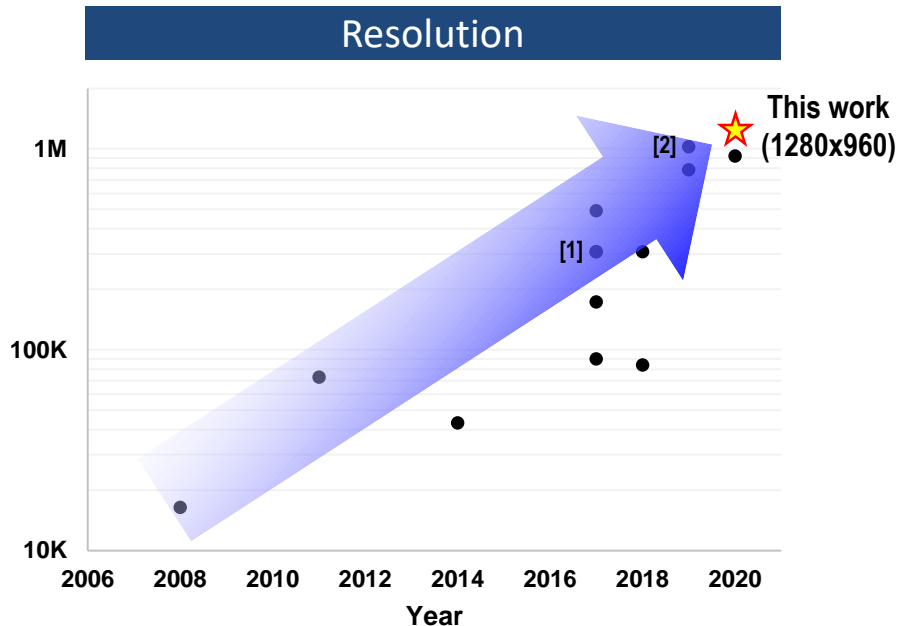
2020 IEEE International Symposium on Circuits and Systems
Virtual, October 10-21, 2020

Outline

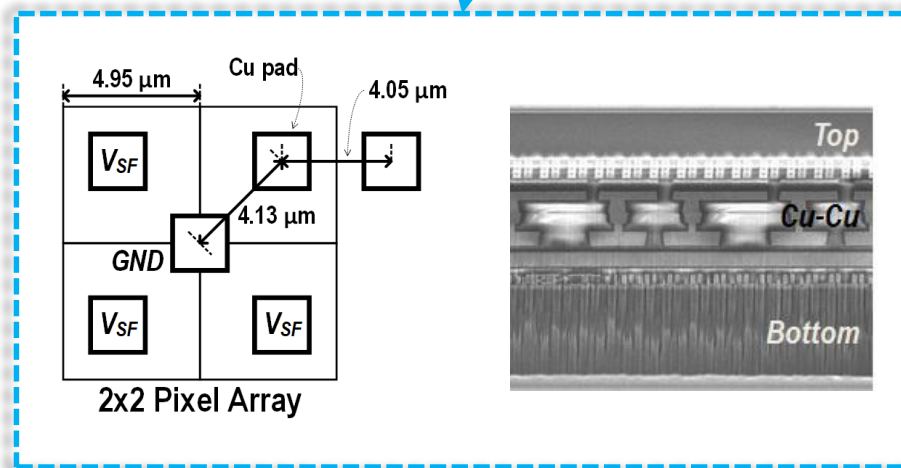
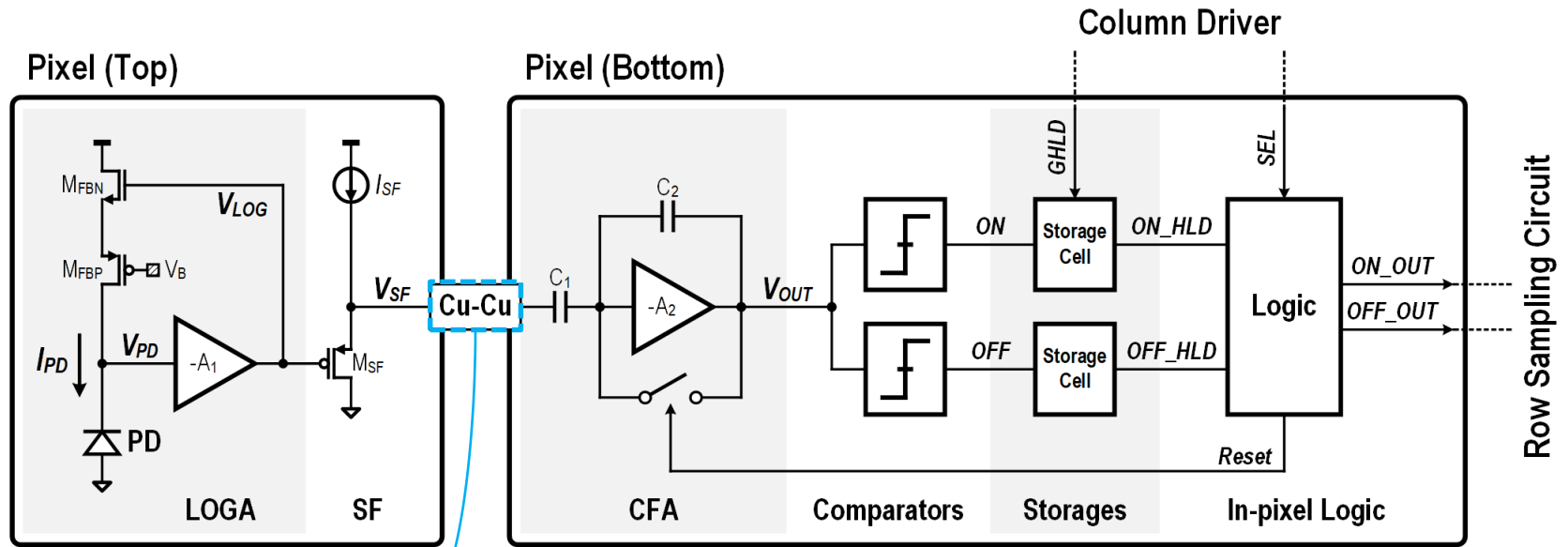
- ✓ Introduction
- ✓ Pixel Design
- ✓ Motion Artifact Minimization
- ✓ Performance Comparison
- ✓ Summary

Introduction

- **1280x960 (1.2M)** resolution and **4.95 μm** pixel pitch
- Pixel shrink is achieved by Cu-Cu wafer bonding technology.
- Side effects from scaled-down technology and motion artifacts are solved.



Pixel Structure w/ Cu-Cu bonding



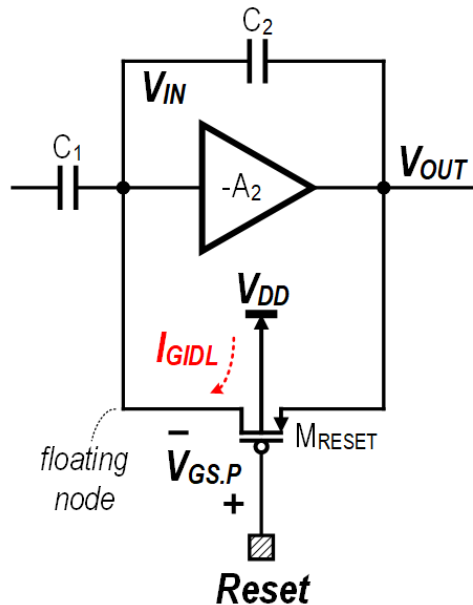
Pixel is composed of

- Photodiode (PD)
- Log Transimpedance Amplifier (LOGA)
- Source Follower (SF)
- Capacitive Feedback Amplifier (CFA)
- Comparators & Event Storages
- In-pixel Logic Circuitry

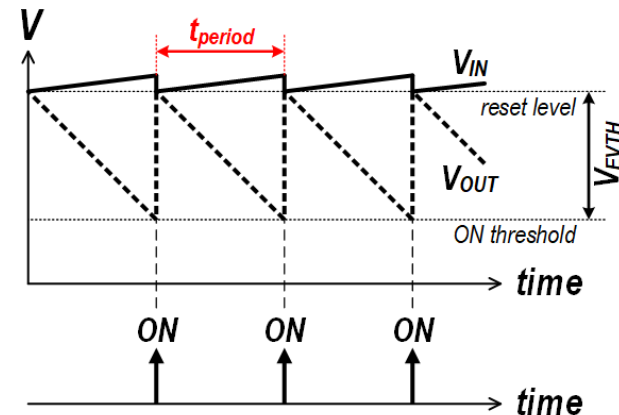
Periodic False Event Generation

- Leakage currents flowing into the floating node induces the periodic false event generation.
- GIDL of M_{RESET} is the dominant source of the leakage currents and it is derived from large $V_{\text{GS,P}}$ after reset operation finishes.

CFA w/ Conventional Reset Switch



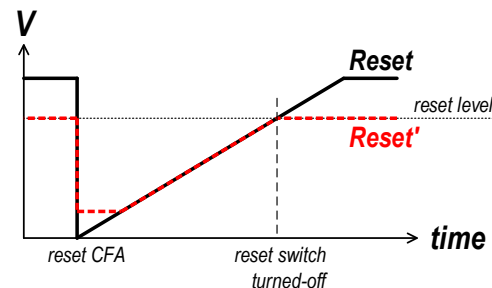
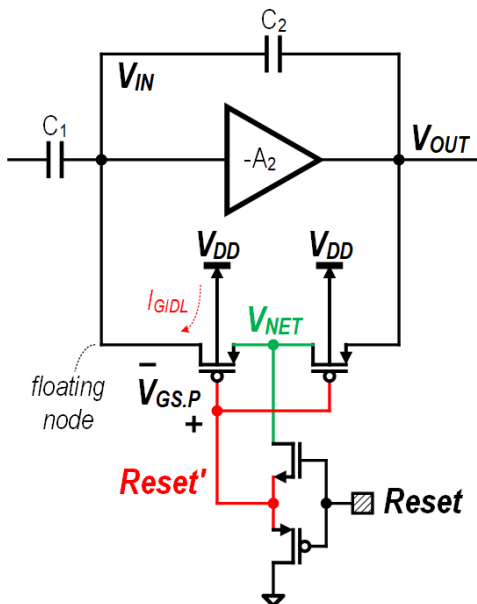
False ON-Event Generation



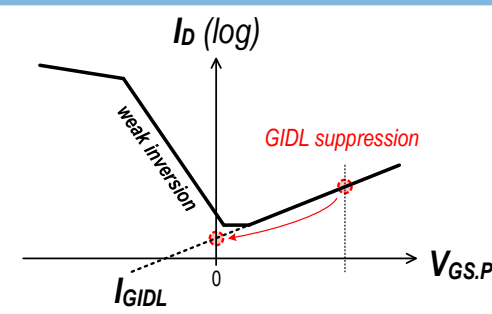
GIDL Suppression

- **GIDL-suppressed reset switch** is newly designed to avoid the periodic false event generation.
- The switch adaptively samples its reset voltage pixel-by-pixel and time-to-time.
- Zero $V_{GS,P}$ after the reset operation finishes decreases GIDL, thus suppresses periodic false events.

GIDL-suppressed Switch

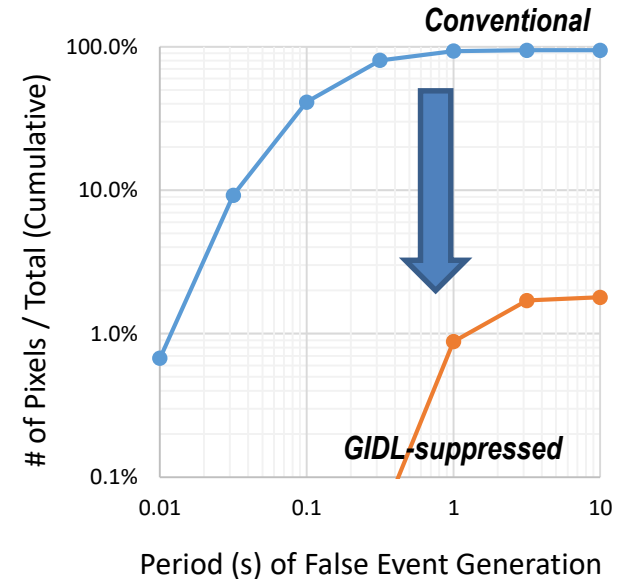


Timing Diagram at Reset



I-V Curve in Weak Inversion

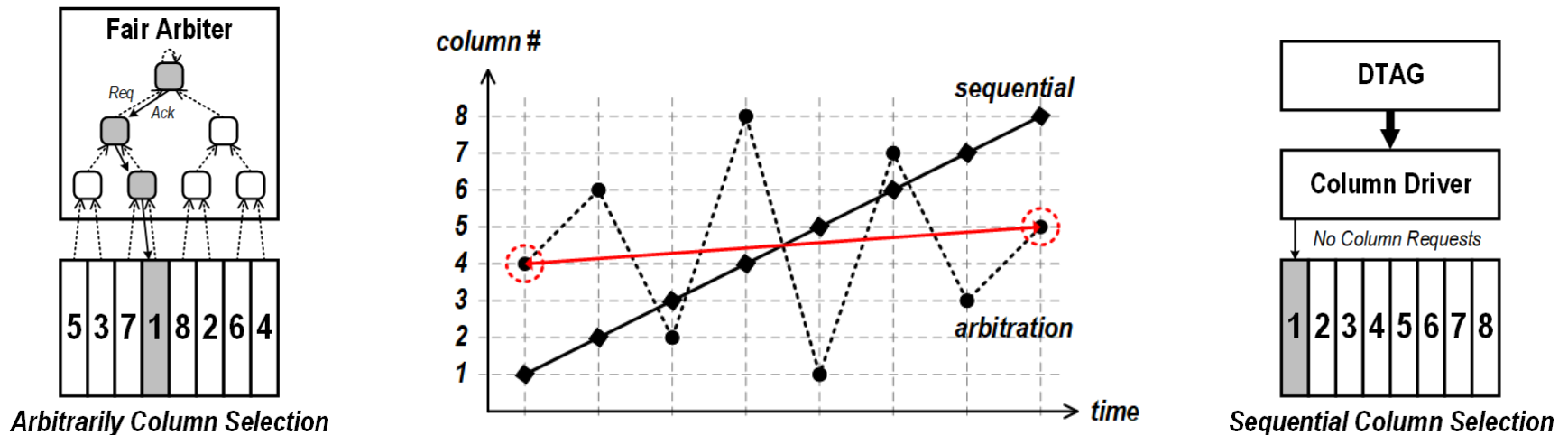
Measurement Result



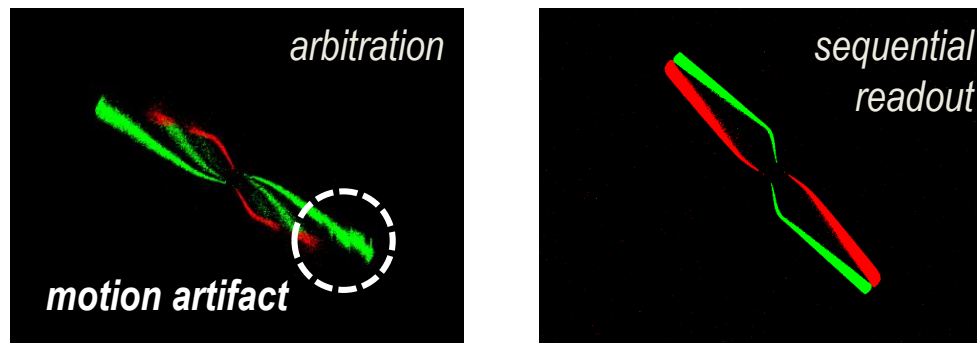
Motion Artifact Minimization (1/2)

- **Sequential Column Readout** is employed to avoid the motion artifact which is introduced by the event-handling order of fair arbiter.

Arbitration VS Sequential Readout



Captured Images (Rotating Fan)



- **Global Event-Holding Function** is implemented to avoid a jello effect.
- The cascaded structure of the in-pixel storage secures the sampled event voltage from the channel leakage.

[illegible]

The diagram consists of two vertically aligned plots sharing a common horizontal time axis.

Top Plot (Voltage V vs. time):

- The vertical axis is labeled V .
- A horizontal line at the top is labeled $GHL D$.
- A vertical line marks the start of a "holding event & reset CFA".
- A horizontal double-headed arrow indicates a duration of $>10\text{ ms}$.
- A solid black line labeled ON_HLD starts at a high level and remains constant during the holding event, then ramps down.
- A dashed red line labeled ON_HLD' starts at the same high level but ramps down linearly during the holding event, reaching a lower level than ON_HLD at the end of the event.

Bottom Plot (Current I vs. time):

- The vertical axis is labeled I .
- A solid black line labeled ON is at a low level during the holding event and then ramps up.
- A dashed red line labeled I_{LEAK1} is at a high level during the holding event and then ramps down.
- A dashed red line labeled I_{LEAK2} is at a high level during the holding event and then ramps down, following a similar path to I_{LEAK1} but at a lower level.

A dashed line connects the end of the ON_HLD ramp to the start of the I_{LEAK2} ramp. A note at the bottom states: I_{LEAK2} suppressed by the body effect of M_{N2} .

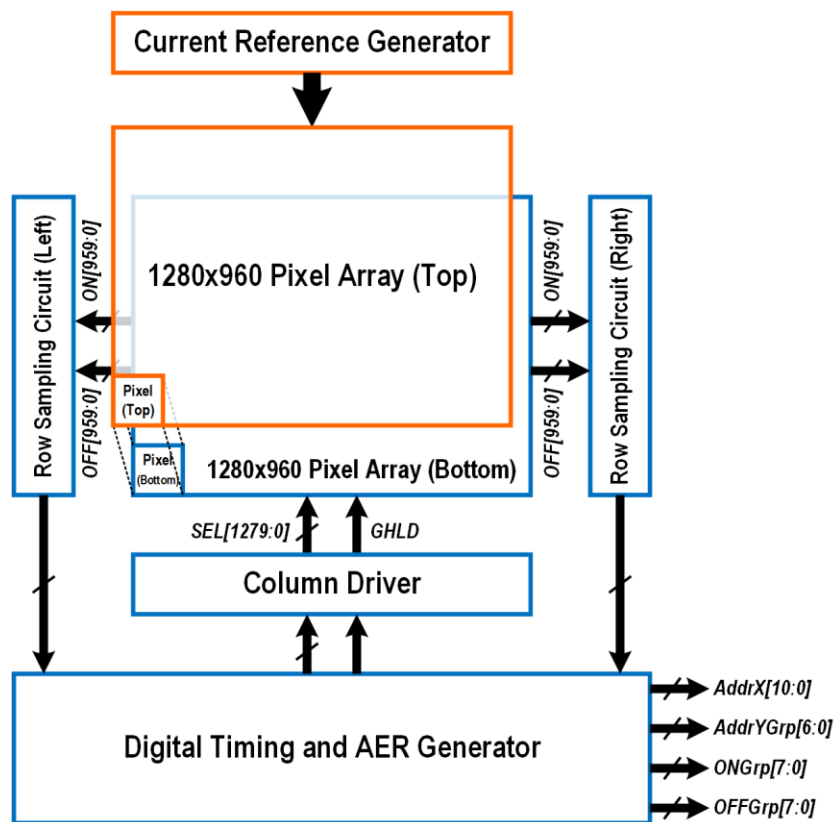
jello effect

w/ global event-holding

Top Block Diagram & Chip Photo

- Pixel array is divided into the top and the bottom wafers.
- 8.37 x 7.64 mm² sensor was fabricated in a 65 nm/28 nm stack process.

Top Block Diagram



Chip Photo

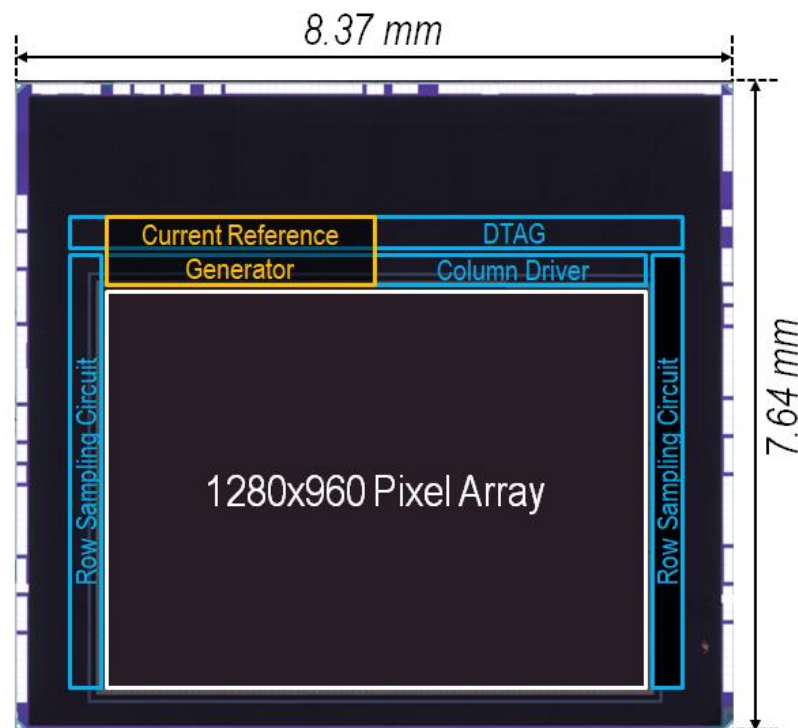
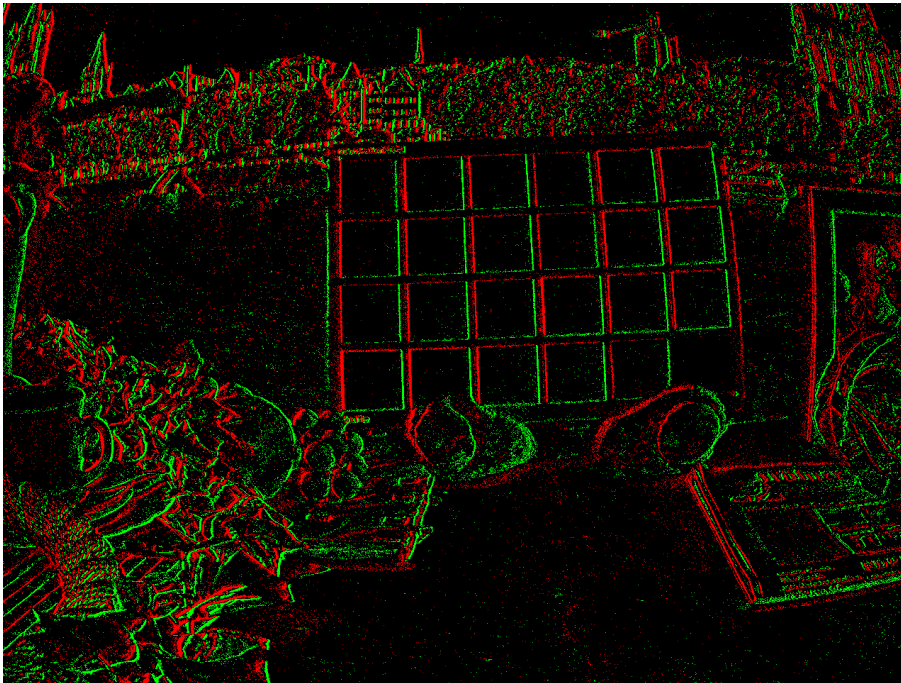


Image from Event Stream

- 1280x960 high-resolution image captured from event stream



A captured image from the event stream
(Green for ON event, Red for OFF event)



Original studio scene

Performance Comparison

- **The highest resolution** and **the highest event rate** were achieved.
- 2.5-Gbps 4-lane MIPI is integrated to transfer 1.3×10^9 events in a second.

		This work	ISSCC 2017 [1]	CVPR 2019 [2]	VLSI 2019 [6]	ISSCC 2020
Process		65 nm 1P6M BSI / 28 nm 1P7M	90 nm 1P5M BSI	65 nm CIS	65 nm 1P9M	90 nm BI CIS / 40 nm CMOS
Resolution		1280x960	640x480	1280x800	132x104	1280x720
Chip Area		8.37x7.64 mm ²	8.0x5.8 mm ²	-	2.0x2.0 mm ²	-
Pixel Pitch		4.95 μm	9 μm	9.8 μm	10 μm	4.86 μm
Fill Factor		22%	-	-	20%	>77%
Supply Voltages		2.8 V, 1.8V, 1.0 V	2.8 V, 1.2 V	-	1.2 V	2.5 V, 1.1 V
Power Consumption	Total ^a	150 mW ^c	50 mW ^d	400 mW ^c	4.9 mW ^d	84 mW ^d
	per Pixel ^b	122 nW	162 nW	391 nW	357 nW	91 nW
Max Event Rate		1.3 Geps	300 Meps	-	180 Meps	1.066 Geps
Readout		Sequential	Arbitration	-	Sequential	Arbitration
In-Pixel Storage		Yes	No	-	Yes	-
Interface		MIPI	MIPI	MIPI	Parallel	Parallel

a. At max event rate or under high activity condition

b. Normalized by resolution

c. Including power consumption at MIPI as I/O

d. Including power consumption at parallel interface as I/O

Summary

- 1280x960 resolution dynamic vision sensor
- 4.95- μm pixel pitch with in-pixel Cu-Cu bonding technology
- GIDL-suppressed switch
- Sequential column selection
- Global event-holding function
- The highest resolution (1.2Mpixels)
- The highest event rate (1.3 Geps)