A 16 × 16 Nonvolatile Programmable Analog Vector-Matrix Multiplier

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***Abstract*— In this paper, we present a 16 × 16 analog vector-matrix multiplier with analog electrically erasable and programmable read-only memories (EEPROM's) used as nonvolatile storage for the weight matrix values. Each weight matrix value is stored in an EEPROM transistor as a change of the threshold voltage, and the same EEPROM transistor is used for the multiplication by utilizing the square-law characteristic of the metal–oxide–semiconductor field-effect transistor. This allows a very simple circuit for the multiplier array with a size of about 1 × 1 mm^2. The vector-matrix multiplier has been fabricated in a 1.5-μm single-poly complementary metal–oxide–semiconductor/EEPROM technology and successfully tested.**

***Index Terms*— Analog memories, analog multipliers, erasable and programmable read-only memory (EPROM).**

I. Introduction

THE vector-matrix multiply operation is defined as sum of products, namely

$$Y_i = \sum_j W_{ij} X_j$$

with an input vector X_j, a matrix of stored weight values W_{ij}, and the output vector Y_i. This general function can be used in various signal-processing algorithms and in a large number of neural-network algorithms. Among the most typical are multiple one-dimensional convolution or correlation operations, which are useful in many applications in image processing.

The advantage of an analog implementation of the vector-matrix multiplier in comparison to a digital realization are small chip size and low power consumption. The analog multiplier occupies only a small silicon area, so that an array of multipliers operating in parallel can be realized. For analog input and output signals, analog/digital and digital/analog (D/A) conversions can be saved if the multipliers are implemented as analog devices.

Fig. 1 shows the schematic of a vector-matrix multiplier that is suitable for an implementation as an analog VLSI circuit, where the values X_j, Y_i, and W_{ij} are assumed to be voltages. The values of the input vector X_j are multiplied in each column by the stored weights W_{ij} and are summed in each horizontal row. The results are the output values Y_i, which are available in parallel in each row. The analog weight matrix values W_{ij} are stored at each multiplier site so that all multipliers in the array can multiply in parallel without the necessity to fetch the weight from an external memory. An alternative analog storage for the weight values are capacitors [1], [2], but these can store an analog voltage only for a short time. For this reason, the capacitors need a repeated signal refreshing using an additional digital memory, where the weight values are stored. In addition to this, a D/A-converter is required that generates the analog voltage for the capacitors.

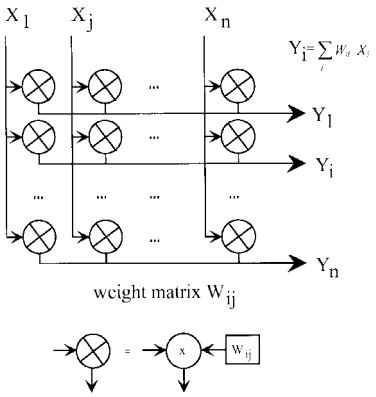

Fig. 1. Schematic of a vector-matrix multiplier.

For a nonvolatile storage of the weight values W_{ij}, analog electrically erasable and programmable read-only memory (EEPROM) devices can be used that do not need refreshing. EEPROM devices normally store digital values [3] and thus require relatively simple programming circuitry. Nevertheless, with a controlled programming of the EEPROM's, analog values can also be stored in EEPROM-based nonvolatile memory [4], [5]. The analog storage of a weight value in an EEPROM cell drastically reduces the occupied silicon area compared to a digital storage of just one bit for each EEPROM device. Some examples for applications of analog EEPROM's are represented by neural networks for weight storage [6], [7], trimming in analog circuits, cancellation of the amplifier offset [8], and calibration of image sensors [9].

Fig. 2 shows the cross section and the symbolic view of an EEPROM device with an injector gate in a single-poly CMOS technology. The device consists of a standard metal–oxide–semiconductor field-effect transistor (MOSFET) with a gate that is employed as a floating gate. The floating gate is completely isolated and coupled by two thin oxide capacitors to the control gate and the injector gate. The

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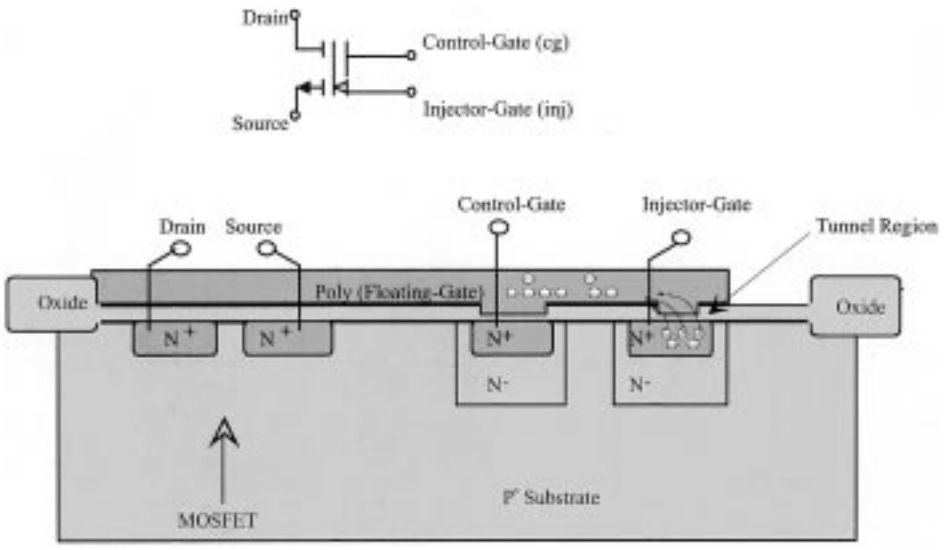


Fig. 2. Cross section and symbolic view of a single-poly EEPROM device.

control-gate/floating-gate capacitor $C_{\rm cg}$ is much greater than the injector-gate/floating-gate capacitor $C_{\rm inj}$. By applying a sufficiently high programming voltage between the control and injector gates, a high electrical field is generated in the tunnel region between the injector and floating gates. This electrical field yields a tunnel current that moves electrons to or from the floating gate and changes the threshold voltage of the MOSFET. The electrons remain at the floating gate even when the power supply is switched off. The EEPROM device allows an analog adjustment of the threshold voltage and thus can be used as an analog memory. The realized analog vector-matrix multiplier uses this effect for storing the matrix weight values W_{ij}.

II. Analog Multipliers with Nonvolatile Analog Storage

In this section, we will discuss possible implementations of vector-matrix multipliers based on analog EEPROM devices. It can be seen in Fig. 1 that the proposed vector-matrix multiplier is formed by the n^2 analog multipliers, each with an analog nonvolatile memory that determines the precision of the operation and the size of the whole circuit. A simple analog multiplier circuit that uses the triode region of a MOSFET [2], [10]–[12] is shown in Fig. 3. M1 and M2 are EEPROM devices of the same geometry size that store the analog matrix value W_{ij} as a change of the programmable threshold voltage V_{th}. To describe the operation let us assume that the threshold voltages of M1 and M2 are $V_{tho}+W_{ij}$ and V_{tho}, respectively. The input voltage vector X_j is applied at the drains of M1 and M2, and the multiplication is carried out by operating the two MOSFET's with $V_{gs}-V_{th} \gg V_{ds}$ in the triode region, so that their drain currents can be approximated as

$$I_1 = k\left[(W_{\rm ref} - V_{tho} - W_{ij})X_j - X_j^2/2\right]$$

and

$$I_2 = k\left[(W_{\rm ref} - V_{tho})X_j - X_j^2/2\right].$$

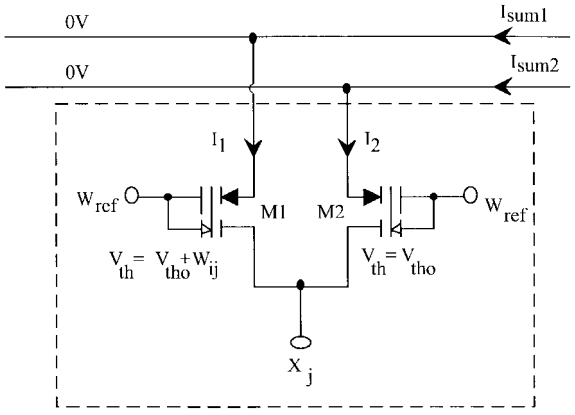


Fig. 3. A MOSFET triode multiplier with a floating gate for nonvolatile matrix value storage.

The second MOSFET M2 is required to cancel the nonlinear term in I_1 and I_2 so that the required product is obtained by subtracting the currents I_2 and I_1

$$I_2 - I_1 = k(W_{ij}X_j).$$

The sum of products can be readily obtained by summing the drain currents of the required number of multipliers. The disadvantage of the MOSFET triode multiplier is that the current-to-voltage converter that is required for summing of all drain currents ($I_{\rm sum1}$ and $I_{\rm sum2}$ in Fig. 3) and providing a voltage output must have a low input impedance within a very high input voltage range. Otherwise, a variation of the source potential at M1 and M2 would affect the drain-source voltage of M1 and M2 and thus influence the multiplication result.

An analog multiplier that does not require a low impedance at the input of its I/V-converter is represented by the modified Gilbert multiplier [1], [13]. The multiplier is built of four standard MOSFET's and two analog EEPROM's that store the weight value W_{ij} as the threshold voltage difference [6]. All transistors operate in saturation and produce a differential output current that is proportional to W_{ij} and the differential input voltage $X = X_j - X_{\rm ref}$.

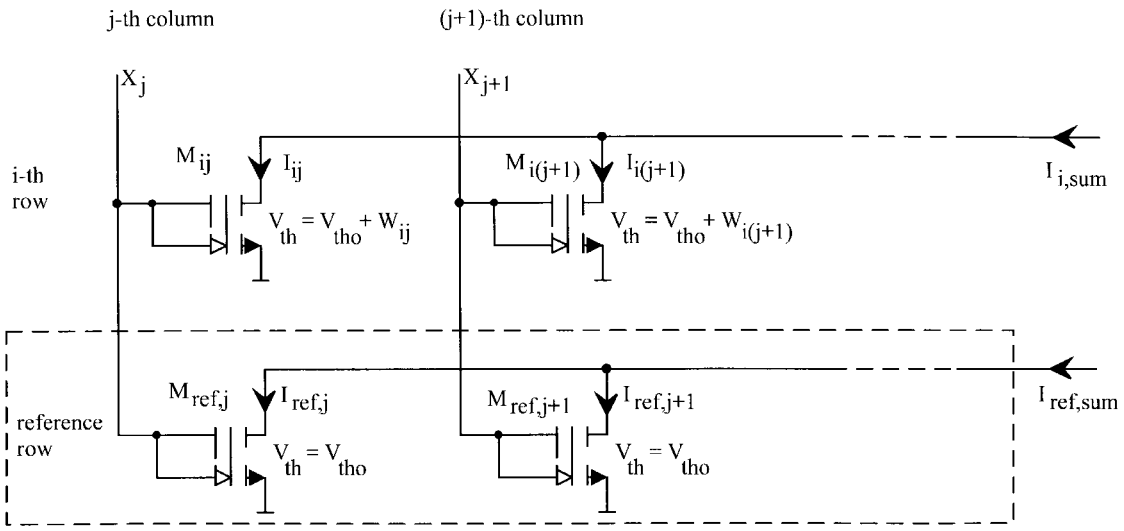


Fig. 4. Multiplier circuit for the vector-matrix multiplier with analog EEPROM's.

An alternative realization of multiplication can be implemented by using the "quarter-square algebraic identity" that can be written as

$$Y = \left[(X+W)^2 - (X-W)^2\right] = 4XW.$$

For this type of multiplication, we need first to add and subtract the two input signals X and W. Then, after squaring and finally subtracting the results, we obtain the product of X and W. The realization of such a multiplier is described in [14] and [15]. Its advantage is that it can be implemented using the square-law characteristic of MOS devices in saturation. However, it requires too many MOS transistors (at least 12 MOS transistors are used in [15]) and is thus not suitable for a multiplier array. Simple multiplier cells based on the quarter-square technique can be realized by using dual- or multiple-input floating-gate MOSFET's [16], [17] and promise a small silicon area. If the matrix value is stored in the EEPROM transistor as a change of the threshold voltage, the multiplication can be easily obtained by using the square-law characteristic of the MOSFET in saturation. A very simple multiplier circuit can be realized by using only two EEPROM transistors. Assuming that the threshold voltages of the matched EEPROM devices can store the weight W_{ij} in such a way that we obtain $V_{th} = V_{tho} + W_{ij}$ and $V_{th} = V_{tho} - W_{ij}$ and that both are in saturation, their drain currents are given by

$$\begin{aligned} I_1 &= k(X_j - (V_{tho} + W_{ij}))^2 \\ &= k((X_j - V_{tho}) - W_{ij})^2 \end{aligned}$$

and

$$\begin{aligned} I_2 &= k(X_j - (V_{tho} - W_{ij}))^2 \\ &= k((X_j - V_{tho}) + W_{ij})^2. \end{aligned}$$

The differential output current $I_2 - I_1$ now contains the product $X_j * W_{ij}$ because

$$I_2 - I_1 = 4k(X_j - V_{tho})W_{ij}.$$

To generate an output signal Y_i from the differential current $I_2 - I_1$, an I/V-converter is required, but with relaxed requirements on its input impedance because the transistors operate in saturation.

For the realized vector-matrix multiplier, we have further simplified the described multiplier circuit by using just a single EEPROM transistor for the nonvolatile storage and an additional reference EEPROM transistor that is needed only once for the whole column. The weight matrix value W_{ij} is stored in the EEPROM storage transistor, and the same EEPROM transistor is used for the multiplication by exploiting the square-law characteristic of the MOSFET. Fig. 4 shows the ith row and the reference row of the vector-matrix multiplier circuit. The EEPROM transistor M_{ij} stores the weight matrix value W_{ij} as $V_{th} = V_{tho} + W_{ij}$, while the threshold voltage of the reference transistor $M_{\mathrm{ref},j}$ is V_{tho}. For the multiplication in the ith row and jth column, the input value X_j is applied to the gates of the M_{ij} and $M_{\mathrm{ref},j}$. Hence, for both devices in saturation, the currents I_{ij} and $I_{\mathrm{ref},j}$ are given as

$$I_{ij} = k(X_j - V_{tho} - V_{ij})^2$$

and

$$I_{\mathrm{ref},j} = k(X_i - V_{tho})^2.$$

The difference current $\Delta I_{ij} = I_{\mathrm{ref},j} - I_{ij}$ is then defined as

$$\Delta I_{ij} = I_{\mathrm{ref},i} - I_{ij} = k\left(2X_jW_{ij} + 2V_{tho}W_{ij} - V_{ij}^2\right)$$

and this is proportional to the product of X_j and W_{ij}, although with an offset, that depends on V_{tho} and W_{ij}, i.e., $(2V_{tho}W_{ij} - W_{ij}^2)$. The sum of the current differences in the

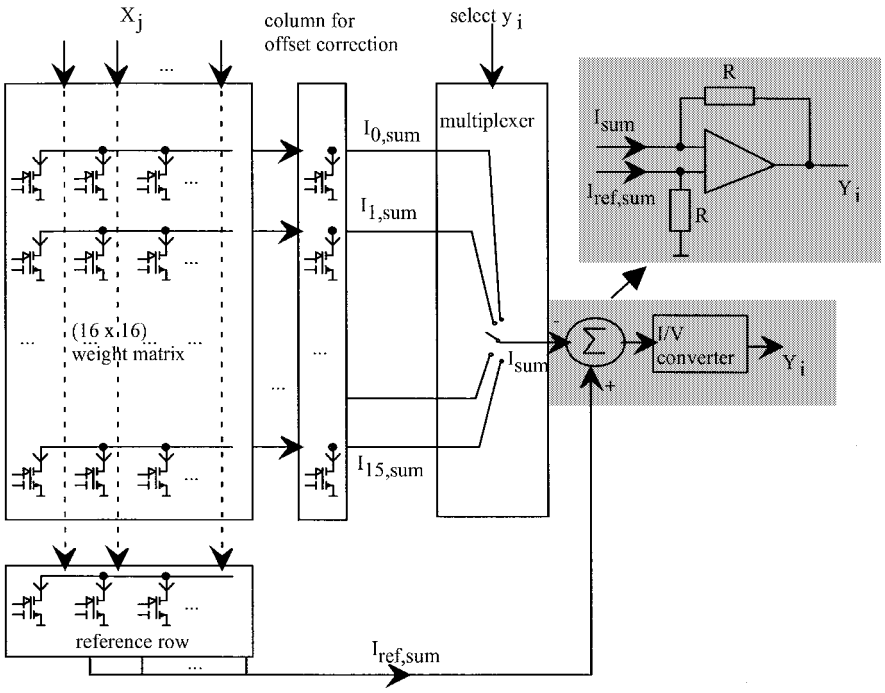


Fig. 5. Block diagram of the realized 16 × 16 vector-matrix multiplier.

ith horizontal row is

$$\begin{aligned}\Delta I_{i,\mathrm{sum}} &= I_{\mathrm{ref,sum}} - I_{i,\mathrm{sum}} \\ &= \sum_j I_{\mathrm{ref},j} - \sum_j I_{ij} \\ &= \sum_j \Delta I_{ij} \\ &= 2k \sum_j X_j W_{ij} \\ &\quad + \underbrace{2kV_{tho} \sum_j W_{ij} - k \sum_j W_{ij}^2}_{\text{OFFSET!}}.\end{aligned}$$

Thus the vector-matrix multiplication $2k\ \Sigma_j\ X_j W_{ij}$ exhibits an offset that is constant after all rows have been programmed to store their values of W_{ij}. This offset can be easily computed by applying $X_j =$ constant for all j, stored in a separate EEPROM column, and then subtracted from the output signal.

III. The Vector-Matrix Multiplier

Fig. 5 shows the simplified block diagram of the realized 16 × 16 vector-matrix multiplier. For the vector-matrix operation, the input values X_j are applied to the EEPROM gates of the weight matrix array and to the reference row. The currents in each row are summed together, including the sum current of the reference row, and converted into voltage to yield the output vector. Each row line has an additional analog memory that corrects the offset so that the offset at the output is zero. To reduce the number of I/O pads, an analog serial-to-parallel multiplexer is used for the input vector and a parallel-to-serial multiplexer for the output vector. The output values Y_i are read out in serial by accessing each row of the weight matrix and subtracting it from the reference row. For applications that need parallel readout of the Y_i values, the sum current of the reference row $I_{\mathrm{sum,ref}}$ can be copied by current mirrors. After calculating the difference of the currents $I_{\mathrm{ref,sum}} - I_{\mathrm{sum}}$, an I/V-converter is needed to produce the output signal Y_i as a voltage.

IV. The Programming of the Weight-Matrix Values

The programming of the EEPROM devices is done by the Fowler–Nordheim tunnelling that moves electrons to or from the floating gate and changes the threshold voltage of the EEPROM transistor if a sufficiently high programming voltage has been applied between the injector gate (inj) and the control-gate (cg). To store analog information in the EEPROM device, a controlled programming is needed that shifts the threshold voltage of the EEPROM transistor to the desired analog value. The EEPROM's can be programmed simply by repeated application of a finite number of constant pulses of the programming voltage at the gates [18]. After each application, the output must be read out in order to enable monitoring control: if the desired value has been reached, the application of the programming pulses is terminated. This programming method is slow because as the programming characteristic of the EEPROM is nonlinear, the pulse width of the programming voltage has to be very small to yield the minimum incremental change of the threshold voltage per pulse. Another disadvantage is the stressing of the tunnel oxide by pulsing voltage.

We have chosen an alternative method where the EEPROM's are programmed just by applying a single pulse that shifts the threshold voltage. A simple feedback circuit is used to cut off the programming voltage at the moment when the desired value has been reached. This programming method,

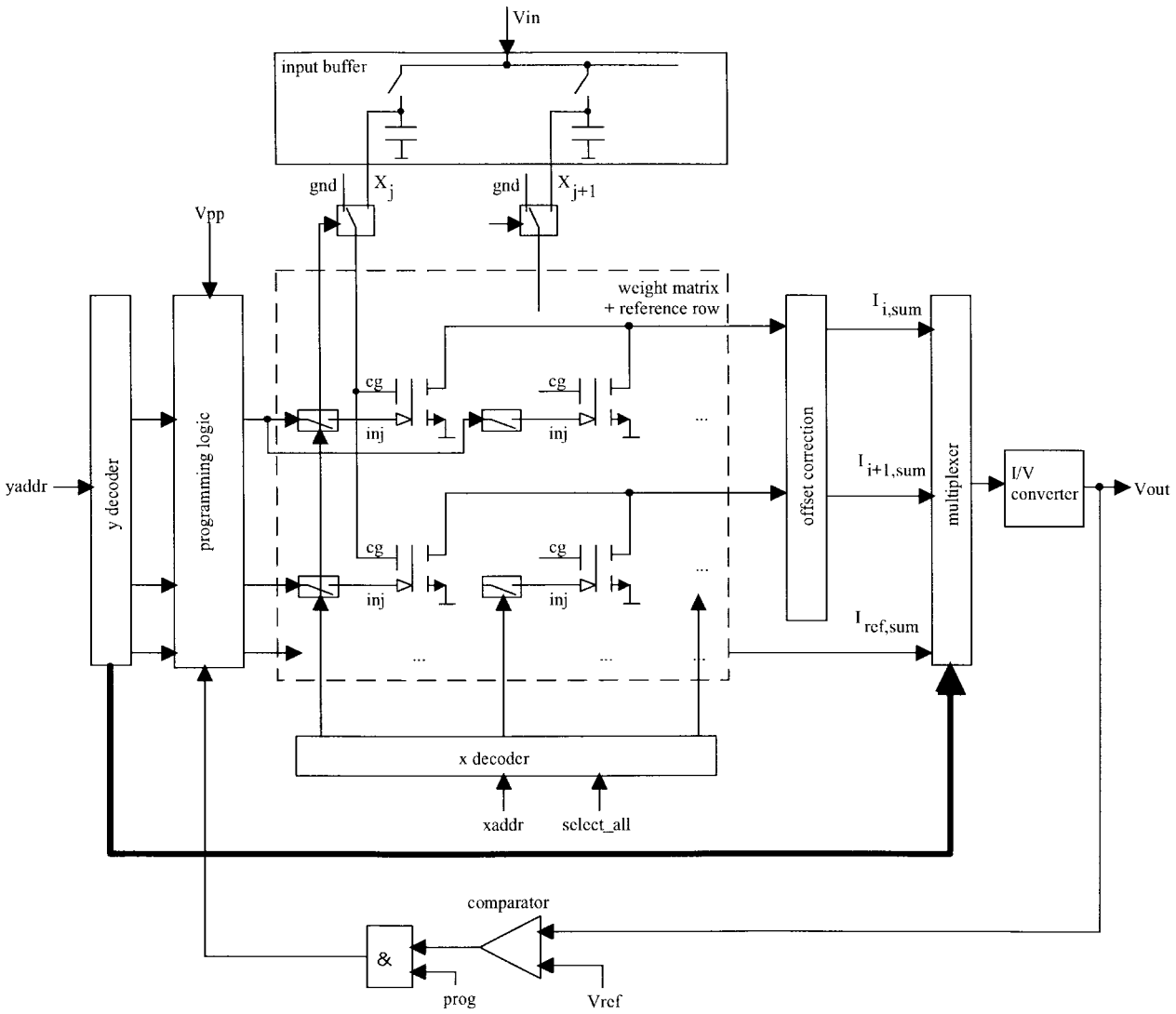


Fig. 6. Block diagram of the realized vector-matrix multiplier with the programming circuit.

however, can change the threshold voltage of the EEPROM only in one direction, which means that the cells have to be initialized first (by applying a sufficiently high programming pulse of V_{pp} at the control gates) before the programming begins. Fig. 6 shows the block diagram of the vector-matrix multiplier with the programming circuit. The cells of the weight matrix are very simple and contain only the EEPROM devices and select transistors at the injector gate (inj) that are controlled by the select signals $yaddr\langle 0:3\rangle$ and $xaddr\langle 0:3\rangle$ to apply the programming voltage V_{pp} to the EEPROM cells. The drain current of the selected EEPROM cell is read out by creating $I_{i,\mathrm{sum}}$. All unselected columns are switched off by grounding their control gates (cg) using the x *decoder*. The selected EEPROM cell receives the input value V_{in} at the control gate in correspondence to the matrix weight W_{ij}. The programming is started with a pulse at the input marked *prog*, and the programming logic applies the programming voltage V_{pp} to the injector gate (inj). It cuts off the programming voltage V_{pp} automatically when the output voltage V_{out} has reached a predefined value V_{ref}. After the programming is completed, the drain current $I_{i,\mathrm{sum}}$ is equal to a constant value $I_{d,\mathrm{ref}}$, i.e.,

$$I_{d,\mathrm{ref}} = k(V_{\mathrm{in}} + V_o - V_{th})^2$$

so that

$$V_{th} = V_{\mathrm{in}} + V_o - \sqrt{\frac{I_{d,\mathrm{ref}}}{k}}$$

and thus the applied input value V_{in} is stored in each EEPROM cell as a change of the threshold voltage V_{th}. First the threshold voltages of the reference EEPROM devices are programmed by applying $V_{\mathrm{in}} = V_{\mathrm{in}o}$. Then the EEPROM devices in the array are programmed by applying $V_{\mathrm{in}} = V_{\mathrm{in}o} + W_{ij}$. Due to the capacitive coupling between the floating gate and the injector gate, the drain current changes when the programming voltage is removed from the injector gate. This results in an additional offset voltage V_o between the applied voltage V_{in} and the programmed threshold voltage V_{th}. But this offset voltage is constant for all EEPROM devices in the array and also for the EEPROM devices in the reference row. So it does not affect the programmed matrix weight W_{ij}, because W_{ij} is the threshold-voltage difference of the reference EEPROM

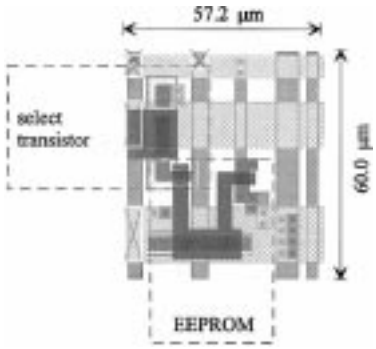


Fig. 7. Layout of the multiplier cell with nonvolatile storage.

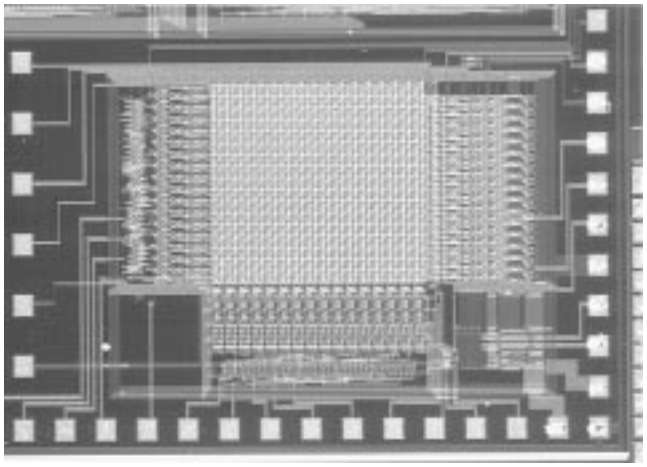


Fig. 8. Micrograph of the realized chip.

device and of the EEPROM device in the array. The storage of the weight values W_{ij} as voltage difference also compensates temperature effects during the programming.

For the programming of the analog offset correction, all columns of each row are selected by the signal *select_all*. With the input signal $X_j = X_{\text{ref}} = 2.5$ V, the offset correction EEPROM device is programmed to reach the desired sum current $I_{i,\text{sum}}$. The programming can be done the same way as for the matrix values using a feedback and controlling the output sum current during the programming. This will produce also an offset voltage V_o because of the capacitive coupling between the floating gate and the injector gate. The offset voltage is constant for all rows and can be easily compensated off the chip.

The 16 × 16 vector-matrix multiplier has been realized in a 1.5-μm single-poly CMOS/EEPROM technology. One multiplier cell consists of a single EEPROM device, and a select transistor and has a size of 57.2 × 60 μm^2 (Fig. 7). The size of the entire 16 × 16 array is 1 × 1 mm^2. The total size of the chip including the circuitry required for analog EEPROM programming is 2.9 × 2.1 mm^2 (Fig. 8).

V. Measurements

A. Programming the Matrix Weight Values W_{ij}

The threshold voltage V_{th} of the EEPROM's can be programmed in a range between $V_{th} = 0$ V and $V_{th} = 5$ V from which only a range of $V_{th} = 1.5$ V to $V_{th} = 2.5$ V has been used for the multiplication. Correspondingly, the range for W_{ij} was varied between -0.5 and 0.5 V. We have programmed the weight values with a programming voltage V_{pp} of 16 V and a programming time of 100 ms for each weight value. The measured programming error for W_{ij} was measured less than 10 mV.

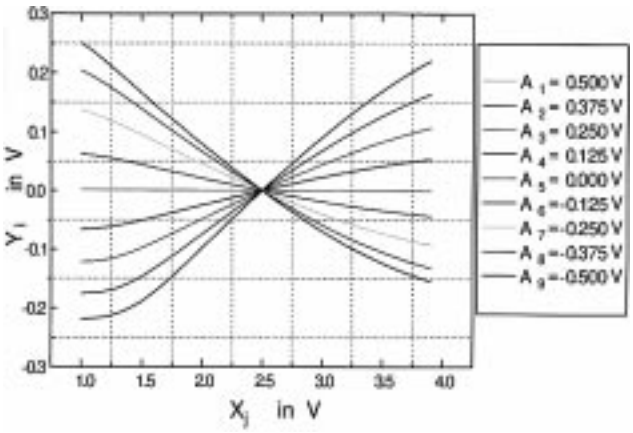


Fig. 9. Measured multiplier characteristic of the vector-matrix multiplier with differently programmed weight values.

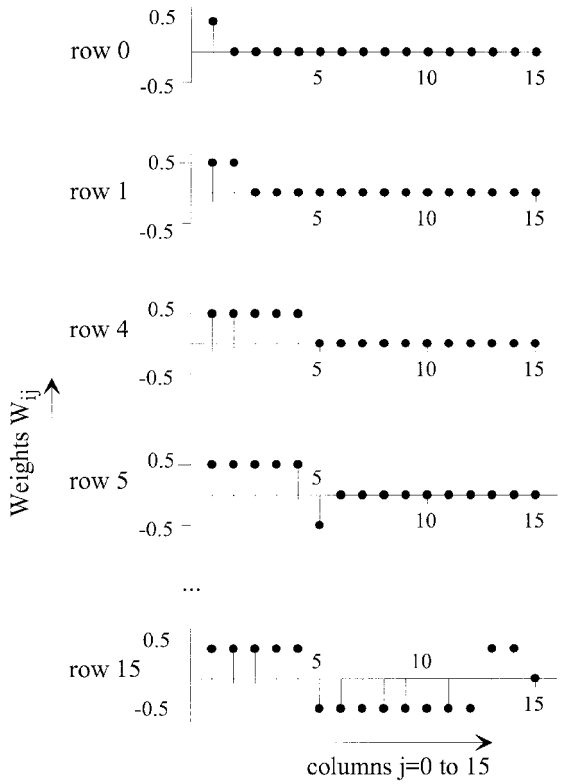
B. Multiplier Characteristic

Fig. 9 shows the measured multiplier characteristic of the vector-matrix multiplier for various programmed weight values of W_{ij}. The weight values are constant in all rows but differ from row to row with $W_{ij} = A_i$ (A_i was varied between -0.5 and 0.5 V) and the input vector X_j is varied from 1 to 4 V with values constant for each row. After an offset correction that was not carried out on the chip in this case, the result is the multiplication of the input vector X_j, with the sum of the stored weights in one row $Y_i = X_i * \Sigma\ A_i = 16 * X_i * A_i$. The resulting products exhibit different gradients that depend on the stored weight values. The maximum linearity error of the sum product for the input range from $X_j = 1.5$ to 3.5 V is $\Delta Y_i = 11.6$ mV (worst case) for the weight value $W_{ij} = 0.5$ V. This means a relative nonlinearity of less than 2.4% for a full-scale output swing of 500 mV.

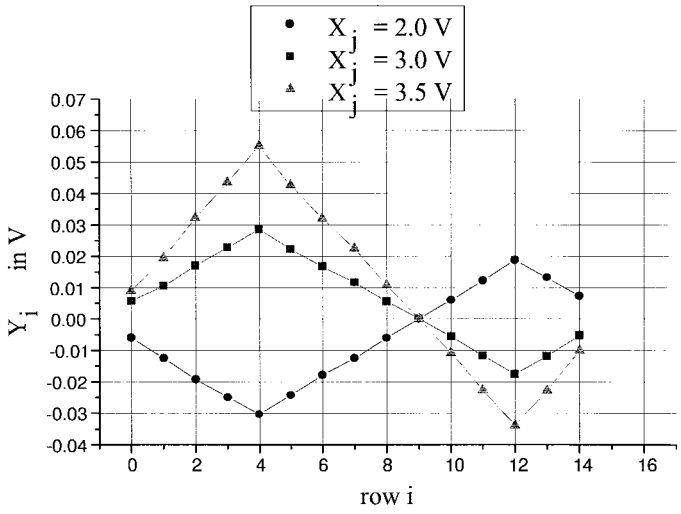
The total harmonic distortion (THD) of the output signal describes the nonlinearity of the multiplier. For a sine wave input signal $X_j = 1.0$ $V_{p\text{-}p}$ ($X_j = X_j - 2.5$ V) and $W_{ij} = 0.5$ V the calculated THD value is less than 1%.

C. Vector-Matrix Multiplication

To demonstrate the vector-matrix multiplication, weights corresponding to square-waves with constant amplitude but different periodicity have been programmed in each row [Fig. 10(a)]. The input vector X_j with constant column values but varying amplitudes is applied to the vector-matrix multiplier, and the output vector Y_i is measured. Fig. 10(b) shows the offset-corrected result of the vector-matrix multiplication. For $X_j > 2.5$ V, the Y_i increases from $i = 0$ to $i = 4$ because a positive weight is added in each row, and decreases for $4 < i \leq 12$ because negative weight values are programmed for $i \geq 5$. For $i \geq 13$, the value of Y_i again increases. For



(a)



(b)

Fig. 10. (a) Programmed weight values for the measurements shown in (b). (b) Measured Y_i values for different input values X_j after an offset correction.

$X_i < 2.5$ V, the plot exhibits the same dependence but with opposite signs.

We have measured a bandwidth of only $f = 60$ kHz for the analog vector-matrix multiplier although the simulation showed a bandwidth of more than 500 kHz. Since the chip can perform a 16×16 multiplication at once, that means about 15.36 million analog multiplications in one second at a frequency of $f = 60$ kHz. The measurements have revealed that it is the I/V converter that limits the speed. Thus, the multiplier bandwidth can be increased by improving the converter bandwidth.

TABLE I
TECHNICAL DATA

power supply	5 V
programming voltage	16 V
power consumption for vector-matrix multiplication	100 mW
maximum speed for vector-matrix multiplication	60 kHz
programming time for one weight value W_{ij}	100 ms
programming error for W_{ij}	$<$10 mV
storage time for W_{ij} (20 mV change at 85°C)	70 days
output noise (rms value)	540 μV
range for W_{ij}	-0.5 to 0.5 V
range for X_j	1 to 4 V
relative nonlinearity for the sum product	2.4%
fabrication process	1.5 μm single-poly CMOS/EEPROM

D. Retention Time for the Programmed Weight Values

For measurement of the retention time, the weight values W_{ij} have been programmed in the EEPROM's and the chip has been heated up in an oven with a temperature up to $T = 150$°C. After 86 h, the maximum change of the stored value was 20 mV. If we use an activation energy $E_a = 0.6$ eV for the floating-gate technology, the lifetime of 86 h at 150°C is equivalent to a lifetime of 71 days at 85°C.

The measured performance data of the realized vector-matrix multiplier are summarized in Table I.

VI. CONCLUSIONS

A 16×16 analog vector-matrix multiplier with analog EEPROM's has been realized in a 1.5-μm single-poly technology, and measurements are presented. In comparison to a digital realization, the analog vector-matrix multiplier drastically increases the storage density by storing the analog matrix value in a single EEPROM device. The multiplier array also allows 16×16 multiplication at the same time, which means more than 12 million multiplications in one second at a frequency of $f = 60$ kHz. By increasing the speed of the output I/V converter, the frequency can be increased to above $f = 500$ kHz.

The multiplier array size can be easily increased to a 64×64 array or more because the multiplier circuit is very simple. In comparison to other analog multipliers, the realized multiplier cell only uses a single EEPROM transistor for the nonvolatile storage of the matrix value and the analog multiplication. It has the same size as a full-featured EEPROM device with a select transistor. This yields an extremely simple analog multiplier, so that the total size of the 16×16 multiplier array with the analog nonvolatile memories is only 1 mm^2.

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Amer Aslam-Siddiqi (S'96), for a photograph and biography, see this issue, p. 1501.

Werner Brockherde (M'82), for a photograph and biography, see this issue, p. 1501.

Bedrich J. Hosticka (M'80–SM'84), for a photograph and biography, see this issue, p. 1501.