CHARGE AMPLIFIERS FOR PIEZOELECTRIC SENSORS

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Abstract. Research activities devoted to study and develop new piezoelectric tactile sensors for robotics show primary requirements of this class of sensor in terms of analog processing features. Charge amplifiers designed for this purpose are examined from the theoretical and experimental point of view evidencing performances and limits in their application. A new balanced circuit is proposed and analyzed in order to overcome the intrinsic disadvantages of the previous version of charge amplifiers. Several considerations from the measurement and hybrid microelectronic point of view complete the paper.

Introduction

New tactile sensors for robotic applications have been designed and built in the recent years to improve performances of robotic manipulators and introduce high level functions in industrial processes. Detailed studies have been performed in order to integrate the sensing capabilities and the processing electronics onto the same substrate using hybrid microelectronic techniques and PVDF sensing elements [1], [2], [5].

One of the most critical block in thisclass of sensors is represented by the analog processing circuit and in particular the charge amplifier introduced to reveal the small signal produced by the mechanical action. An in-depth analysis has been devoted to study problems related with this analog processing circuit and improve performances of the existing devices [3].

After the development of a classical configuration the authors began to study new and more sophisticated structures to process PVDF signals optimizing performances in respect of internal and external noises. The main purpose of the new configurations is to avoid typical problems introduced by FET gate currents and improve S/N ratio without introducing more processing elements.

The requirements of sensing elements based on PVDF thick-film technology are infact strictly correlated to the analog pre-processing structure and components and every change in the arrangement implies many times a sensible change in the system performances. This is the the reason for which an in-depth analysis has been performed on different structure of charge amplifiers in order to identify the effect of noise on the global device accuracy.

The reduction of noise in non-balanced structure, like the device presented in [4], is obtained by providing a correct choice of the JFETs and their driving circuits, after the definition of the optimal configuration of the charge amplifier.

The paper point out the attention to the extensive experimental activity performed on this type of circuits, describing theoretical characteristics and adopted in-field strategies to reduce parasitic elements. A statistical approch has been adopted in order to validate experimental results obtained testing a large number of devices. The experimental results obtained by testing the old and the new single-charge amplifier configuration show the benefits of adopting dedicated analog-processing structures for advanced piezoelectric sensors.

Following these research activities the authors propose a new and innovative configuration of charge amplifier devoted to the analog processing of signals provided by PVDF sensing elements. The structure, based on a differential-balanced configuration, reduces mainly both the effects of noises introduced by JFET and their driver circuits and the external noises.

Single-Structure Charge Amplifier: First Version

Tactile sensors based on piezoelectric active surfaces require efficient charge amplifiers or high-performance voltage follower circuits providing the highest S/N ratio to guarantee sufficient accuracy in the measurement process. In this way complex and advanced analog and also digital signal processing circuitry are developed on the same substrate of the sensing element in order to provide the best evaluation of the information resulting from the mechanical action of the manipulated object. Following a complete analysis of the hybrid structure and functionality of two previous realizations [1], [2], it is now possible to point out the attention on the performances reached designing and building the latest two version of analog processing blocks, properly optimized to enhance sensor performances.

As happened for the previous realizations the sensing area is realized using PVDF piezoelectric-film disposed on a ceramic substrate. The hybrid microelctronics for analog and digital signal processing is built near the active surface in order to reduce noise and interference created by the industrial environment in

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which the device is designed to work. The design of charge amplifiers is oriented to optimize the following A/D conversion block functionality in order to provide the highest accuracy in the analysis of force actions. The accuracy of measurement procedures depends infact by the development of particular circuit topologies providing a sufficient rejection of external and internal noises. In order to achieve this result two different charge amplifier circuits have been developed, built and experimented. A deep analysis of functionality and dynamic response of these systems under normal and limit conditions has been provided.

The electric design of the first prototype is shown in Fig. 1. After the first block performing real integrator functions (OA1) has been introduced a second block based on a derivative network (OA2). This arrangement cancel the pole of the first block introducing the ideal dominant pole of the system (1 Hz). A detailed description of the structure and design choices is presented in [3] and [4]. One of the first requirements evidenced in the design strategy is the improved accuracy in signal amplitude evaluation necessary to guarantee the best measurement performance for this type of sensing elements. This characterization can be only reached by means of a particular choice in the charge amplifier parameters: resistance, capacitance, parasitic values have to be selected in a proper way and noise sources reduced in order to reach optimal performances. All these task are related to the value of the feedback resistance in the first operational amplifier of the processing structure (real integrator). Increasing the value of R_1 global gain and SNR increments are obtained.

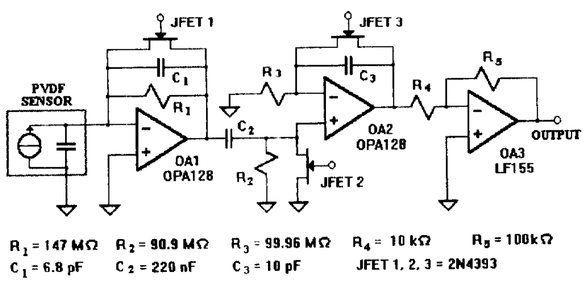

Fig. 1. The first version of the single-structure charge amplifier.

The upper limit in the choice of R_1 is defined by its enlarged physical dimension following an R_1 increasing; this means more surface unavailable in the thick-film structure and an increment in the time-constant value (that for design reason cannot be arranged greater then 1 ms). This parameter is also influenced by the capacitance C_1 connected in the feedback loop of the first operational amplifier (OA1). The choice of C_1 is strictly related to the JFETs introduced in the circuit to provide cyclic discharge of the capacitances. This function is implemented in order to neutralize the unwanted effects of bias currents and offset voltages of operational amplifiers and pyroelectric effect of PVDF-films.

The switching frequency of JFETs is also a control parameter for the global dynamical gain of the system, because it allows the extension of the measurement range of the sensor to higher values of force, leaving unchange the sensibility.

The main problem presented by JFETs working as switches is the noise transmission introduced in the analog processing circuits by switching waveform. The gate-source capacitance C_{gs} represents the coupling element between the switching signal on the gate and the analog signal generated by the PVDF element. In the first block during the ON-OFF transition (JFET 1) the charge injected by C_{gs} is transferred to C_1, inducing a voltage transient on the OA1 output. The amplitude of the injected charge (and consequently of the noise) depends on different causes. They can be resumed as:

1. The type of JFET driver adopted in the circuit;
2. The specific value of driving voltage required by the JFET to switch the device from ON to OFF state and therefore its pinch-off voltage;
3. The C_{gs} value;
4. The C_1 value.

For the example presented in Fig. 2 the noise introduced in the amplifier by the charge injection provided by C_{gs} is able to affect the output with a transient signal of maximum amplitude equal to V_{tr}. This amplitude is proportional to $(C_{gs}/C_1)\Delta V_{gate}$, where ΔV_{gate} is the gate voltage able to switch off the JFET. The time constant $t = R_1 C_{tot}$ defining the transient time is computed performing the parallel between C_1 and C_{feed}, where C_{feed} is the feedthrough capacitance introduced by the JFET [9].

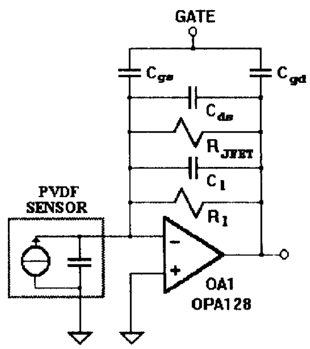

Fig. 2. Feedback-loop equivalent circuit showing coupling capacitances.

It is interesting to note that the necessary requirements for C_1 are in contrast each other:
- C_1 must be enough great to minimize the transient amplitude;
- C_1 must be enough small to reduce the transient time.

This leads to find a compromise between these two opposite characteristics. It is also necessary to choose JFETs characterized by small associated capacitances, especially for the input capacitance C_{gs}; in addition the design of JFET driver needs to be correctly provided in order to reduce its parasitic effect on the main circuit.

In the first version of the circuit JFET switching generates output pulses having maximum amplitude of 400 mV and duration of 4 ms (Fig. 3) in all the prototypes. These pulses restrict the switching frequency up to 250 Hz, and this fact sets the circuit bandwidth.

JFET 2 (Fig. 1) works without introducing significant noise in the output. The charge injection due to junction capacitances introduces voltage pulses having amplitude proportional to $(C_{gs}/C_2)\Delta V_{gate}$. Because C_{gs}/C_2 is small (20 10^{-3}), this noise is negligible in respect of JFET 1 switching effects.

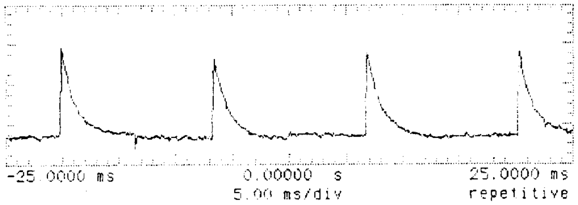

Fig. 3. Output switching noises due to JFET 1 (amplitude: 200 mV/div).

A different approach is required to examine switching noises introduced by JFET 3. This device presents the same charge injection through the capacitance C_3 during every ON-OFF change of state. Because the discharge process of C_3 is not possible by means of a resistive element, the charge can be only removed by the successive OFF-ON switching process. For this reason on the output of the second block a constant voltage, proportional to $(C_{gs}/C_3)\Delta V_{gate}$, can be revealed during the OFF state of JFET 3. This voltage level (about 400 mV in our experimental prototype) can be simply compensated by means of a dedicated hardware structure [2] or software procedure [4].

Single-Structure Charge Amplifier: Second Version

The second version of the analog circuit for the pre-processing of sensing element output signals has been developed after an extended and deep analysis of the noises introduced by switching processes in the first prototype. The design has been reviewed only optimizing passive components values and leaving unchanged microelectronic layout (Fig. 4). This solution guaranteed short manufacturing times, because allowed to use of the same mask to develop hybrid circuits.

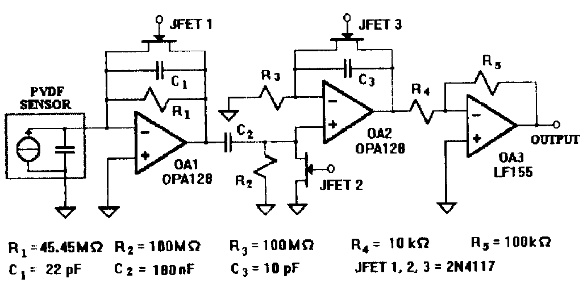

Fig. 4. The second version of the single-structure charge amplifier.

Because the amplitude of voltage pulses introduced by switching process of JFET 1 depends by the (C_{gs}/C_1) ratio, the second prototype design maximized C_1 accordingly to the limitations imposed by the time constant $t = R_1C_1$. The final choice was for a value of C_1 triple of the previous adopted value and consequently the resistance R_1 has been reduced to one third of its initial value. Even if there is an increase of the shot noise, the sensing accuracy is anyway defined up to 1 g.

A significant reduction of switching noise has be obtained in this second design changing the JFET adopted in the first design (switching application oriented) with devices built for linear applications. This family is characterized by lower capacitances ($C_{gs} = C_{gd}$ = 1.5 pF) and pinch-off voltage. A lower ΔV_{gate} can be applied to switch the device (2.5 V instead of 7.5 V for the first version). The channel resistance in the ON state of this JFET family is quite high (10 kΩ ca.) if compared with the previous devices (lower then 100 Ω). Nevertheless it is enough low to guarantee short time-constant in capacitance discharge (under 1 ms) in respect of JFET switching period (never under 1 ms).

Fig. 5 shows the switching noise detected at the output of the second operational amplifier during the JFET switching process. In the new version the maximum amplitude of this signal has been reduce to one third of the previous version: it is limited to 60 mV max in all the prototypes. At the same time there is a reduction in the time constant $t = R_1C_{tot}$ due to the decreased value in the feedthrough capacitance, C_{feed}, of the new JFETs. This fact leaded to measure the new mean transient time equal to 3 ms, that guarantees working conditions able to support a maximum switching frequency of 330 Hz.

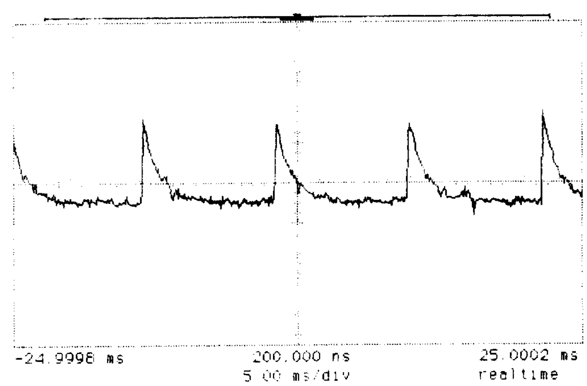

Fig. 5. Output switching noises due to JFET 1 (amplitude: 30 mV/div).

Differential-Structure Charge Amplifier

One of the main problems found in designing tactile sensors for robotics is to implement autonomous noise rejection capabilities in the device. Analog electronics must be able to cancel noise generated by external or internal environment from the output signal.

The sensor designed in our project is especially influenced by:
- the PVDF pyroelectric effect (due to temperature changes); and
- the input bias currents and output voltage offsets of operational amplifiers used to built the analog processing blocks.

The hybrid microelectronic technology emphasizes these problems because it cannot properly provide internal adjustable compensations able to be settle during the working life of the sensor. The search of solutions capable to cancel the effect of these noise sources led to introduce JFET switches in the first and second version of sensor prototypes. This adopted technique guarantees the dynamic control of the analog block gain and provides an efficient rejection of the above-mentioned noises. On the other hand the previous paragraphs show how these devices introduce transient noises related to the switching process. A well-developed design and proper choice of components can reduce their amplitude but not delete their effects.

In order to solve this essential problem a new and more efficient design of the analog block has been provided. The new circuit for the analog processing of PVDF signals allows the use of JFET switches without introducing the associated switching noises.

The new structure is built using a balanced configuration of the previous charge amplifier (Fig. 6). Two symmetrical and syncronized analog processing circuits provide the processing of PVDF signals; a final operational amplifier performs the algebric sum of their outputs. In this way all the external (temperature and interferences) and internal (switching process, bias currents, offset voltages) noises are cancelled if the analog components present the same characteristics. This technique is highly efficient to reject common-mode noise and allows to refer the final output to the ground.

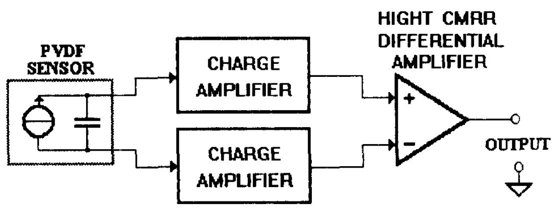

Fig. 6. The new balanced configuration for the charge amplifier.

The first design of this new balanced configuration is under development using the same basic structure of the charge amplifier described in the previous paragraph. Numerical simulations performed on the circuit show significant reduction of JFET switching noise in the final output and confirm theoretical expectations. In the prototype under development the maximum noise amplitude is assumed to be lower then few mV, even if passive component values are supposed to be affected by errors due to the tolerance band.

Concluding Remarks

The design, realization and experimental considerations connected to the development of new and advanced sensors built using hybrid microelectronic techniques indicated several limits in obtaining high-accuracy measurements using classical analog processing electronics. Starting from a sensor previously developed using this technology, the authors consider a new design based upon the specific requirements imposed by this particular application.

The overall design goal of this research is the analysis of practical performance limits of charge amplifiers for piezoelectric tactile sensor based on PVDF sensing elements and built using hybrid-microelectronic analog processing circuit. The sensing area, realized using PVDF piezoelectric-film, needs proper connections to the charge amplifier by means of output lines that pass through the ceramic substrate. Electronic circuits, which perform analog processing, find their best arrangement on the bottom side of the substrate. The benefits of using the same substrate to implement electrodes and electronics for analog processing appear especially in the drastic reduction of noises and in having smaller parasitic elements between the electrodes and amplifiers.

Particular attention is expecially given to enhancing the analog processing characteristics in terms of high S/N ratio. The single-structure processing configurations show their limits in presence of small signal amplitudes more influenced by internal noises (generated by JFET switching process) and external electromagnetic interferences. The significant improvement of performance reached in these analog processing systems by means of a proper choice of electronic components is the prerequisite for the global enhancement of the sensor characteristics.

A new balanced charge amplifier is develop and analyzed in order to overcome the limits presented by previous realizations. Performances defined by numerical simulations seem to be in accordance with theoretical expectations that present reduced influence of external and internal noises. The next experimental activities will be devoted to ascertain these assumptions.

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