Two-Stage Differential Charge and Transresistance Amplifiers

Marco Massarotto, Alfonso Carlosena, *Senior Member, IEEE*, and Antonio J. López-Martín, *Member, IEEE*

***Abstract*—A novel approach to the design of high-performance operational-amplifier-based differential charge and transresistance amplifiers is proposed. It is based on a two-stage topology: The first stage performs a differential measurement to single-ended signal conversion, providing a common-mode rejection that only depends on the matching between two resistors; the second stage filters the signal. Three novel topologies that are based on this technique are presented, analyzed, and measured, and design criteria are finally given. Their performance is compared with that of a state-of-the-art topology that is used as the benchmark, and it results in a better common-mode rejection ratio (CMRR).**

***Index Terms*—Accelerometer, charge amplifier, charge-to-voltage converter, charge-type sensor, current-to-voltage converter, current-type sensor, photodiode, piezoelectric sensor, transresistance amplifier.**

I. Introduction

CHARGE amplifiers are typically defined as transcapacitance circuits—they transform electrical charge into voltage by integration [1]–[3]. In data acquisition systems, they are the first natural conditioning stage to process the information carried by a charge signal coming from a sensor and to deliver it in a suitable form for further analog processing or digitalization. Desirable properties of charge amplifiers are negligible input and output impedance for optimum coupling with the generating element and the subsequent electronics, high sensitivity, and low noise to increase the signal-to-noise ratio (SNR).

According to its physical nature, the typical charge amplifier input signal can be represented by either charge or current sources. It can be single ended when only one terminal of the sensor at the input is available and the other is grounded, or it can be differential when both terminals are available. In any case, the information is encoded in the differential mode (Q_D, I_D), and it is always mixed with unwanted signals like, e.g., dc offset, interference, or thermal noise. Since charge-generating sensors are usually operated under virtual ground conditions (i.e., a zero voltage is forced between their terminals), these unwanted signals ideally only have an effect when they are in current form. If, as is sometimes the case, they appear as a common-mode current (Q_C, I_C), then the topologies with differential input offer a clear advantage.

The technical literature is scarce on differential circuits for charge- and current-type sensors. Either the counterpart of the well-known three-operational-amplifier (op-amp) instrumentation amplifier [Fig. 1(a)] or the simpler topology [4] [Fig. 1(b)] is almost the only available solution; however, it requires at least two matching conditions between resistances and between capacitors that can be practically hard to fulfill. In an attempt to fill this gap, this paper describes a design technique to obtain differential charge amplifiers based on a two-stage topology. Basically, the first stage rejects the common-mode input and performs a differential measurement to single-ended signal conversion, whereas the second one low-pass filters the signal. To validate the proposed technique, three novel topologies are designed, analyzed considering second-order effects and noise, implemented, and tested. With respect to the known topologies aforementioned, they only rely on the matching of two resistors to achieve a better common-mode rejection ratio (CMRR). A preliminary short version of this paper can be found in [1].

Last, it is noted that since current is defined as the derivative of charge, the proposed topologies are of application with charge and current sources (e.g., piezoelectric accelerometers and photodiodes [5]). Only some minor redesign is needed to cope with specific issues such as signal levels, noise shaping, and dc errors. Anyway, when a current input is applied, the circuit is better named transresistor or current-to-voltage converter. In the rest of this paper, this twofold application is taken into account, showing both the charge amplifier and transresistor results and peculiarities.

II. Theoretical Analysis

Differential circuits are routinely described by two transfer functions [6]: G_D is the ratio between the output and the differential input, with a null common-mode input; G_C is the ratio between the output and the common-mode input, with a null differential-mode input. Both parameters can refer to current or voltage output and to charge or current input, depending on the case. The CMRR is defined as the rate G_D/G_C. Ideally, it is desirable to obtain $G_C = 0$ (i.e., CMRR $= \infty$); however, component mismatch makes it unreachable. Hence, the aim of the design is to obtain circuits that, for the desired G_D, yield the highest CMRR. Therefore, dependence on a minimum set of matching conditions and critical components is a design goal.

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M. Massarotto is with the Department of Electrical and Electronic Engineering, Public University of Navarra, 31006 Pamplona, Spain, and also with the Dipartimento Elettronica per l'Automazione, Facoltá di Ingegneria, Universitá degli Studi di Brescia, 25123 Brescia, Italy (e-mail: massama@gmail.com).

A. Carlosena is with the Department of Electrical and Electronic Engineering, Public University of Navarra, 31006 Pamplona, Spain (e-mail: carlosen@unavarra.es).

A. J. López-Martín is with the Department of Electrical and Electronic Engineering, Public University of Navarra, 31006 Pamplona, Spain, and also with New Mexico State University, Las Cruces, NM 88003-8001 USA (e-mail: antonio.lopez@unavarra.es).

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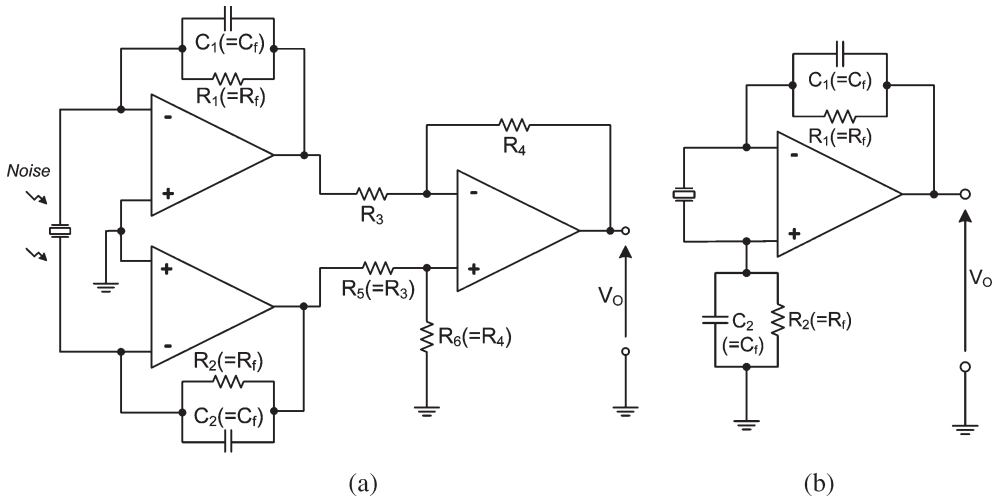

Fig. 1. Conventional differential charge amplifier topologies. (a) Three op-amp. (b) Reference [4]. Table I shows their basic features: Required matching conditions and ideal response with respect to current and charge.

The first way to obtain a differential charge amplifier is given by the counterpart of the popular three-op-amp differential amplifier [Fig. 1(a)] that has been proposed for photodiode [7] and charge sensors [8] and used with minor modifications in a number of applications [9]. Its first stage is a fully differential charge amplifier obtained by two ideally identical integrator topologies (or, alternatively, by an integrator based on a fully differential op-amp [10]). The second stage is the well-known difference amplifier, which provides differential to single ended voltage conversion. The CMRR of the circuit in Fig. 1(a) relies on the matching between resistors, capacitors, and even op-amps.

A much more compact solution [Fig. 1(b)] has been proposed in a recent patent [4]. This topology is obtained by adding to the common single-ended integrator another impedance equal to the feedback impedance and placed from the noninverting op-amp input to ground. To properly reject the common-mode input ($G_C = 0$), the circuit needs two matching conditions on resistors and capacitors. With respect to the circuit in Fig. 1(a), this alternative is very attractive because it requires fewer components and matching conditions; however, it is unbalanced and has the disadvantage that the common-mode voltage of the sensor is signal dependent and may induce some kind of nonlinearity in the op-amp.

A close look at the two above-presented circuits shows that their limitations mainly depend on the fact that common-mode rejection and integration are simultaneously accomplished by a pair of matched branches, which includes capacitance in addition to resistance. However, the basic functions that are required in these kinds of circuits (i.e., common-mode rejection, differential measurement to single-ended signal conversion, charge-to-voltage signal conversion or integration, and amplification) can be also implemented in a different way. Thus, the design technique here proposed (Fig. 2) allows the design of differential charge amplifiers, splitting the basic functions into two independent stages. The first one converts the differential-mode input into a single-ended signal and rejects the common-mode input, whereas the second one performs low-pass filtering and provides a single-ended output voltage. For the two stages

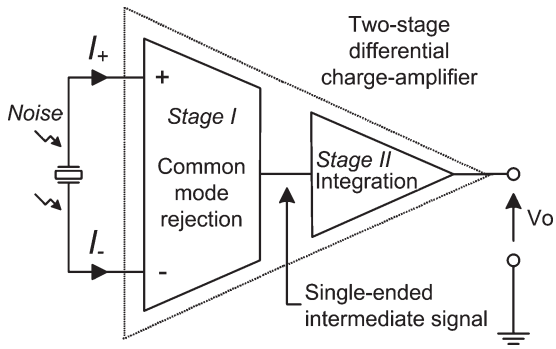

Fig. 2. General approach that is proposed to implement two-stage differential charge and transresistance amplifiers. The first stage provides common-mode rejection, performing a differential to single ended signal conversion. The second one integrates the resulting signal.

to be independent, the output impedance of the first one and the input impedance of the second one have to be properly chosen.

The general approach of Fig. 2 can be implemented in several alternative ways. The first example is given by the circuit in Fig. 3(a). Its first stage is derived from the typical difference amplifier, and it was formerly proposed for photodiode application [5], whereas the second stage is a standard lossy integrator. The circuit in Fig. 3(b) is nothing but a variation of that in Fig. 3(a); it uses a passive lossy integrator as the second stage instead of an active one. A completely different implementation is given by the circuit in Fig. 4. Its first stage is a variant of the so-called Howland circuit [11], whereas the second stage is a standard current integrator. This circuit is an improvement of the one proposed in [12] by the authors. It provides additional gain by just adding the resistor R_a to the topology (for $R_a = 0\ \Omega$, the circuit in [12] is obtained). The main difference between the two implementations of Figs. 3(a) and 4 is in the first stage, which yields an intermediate voltage or current mode signal, respectively.

In Table I, (22)–(45) summarize the basic features of all of the presented topologies so far: the matching conditions that are needed to obtain an infinite CMRR and the ideal

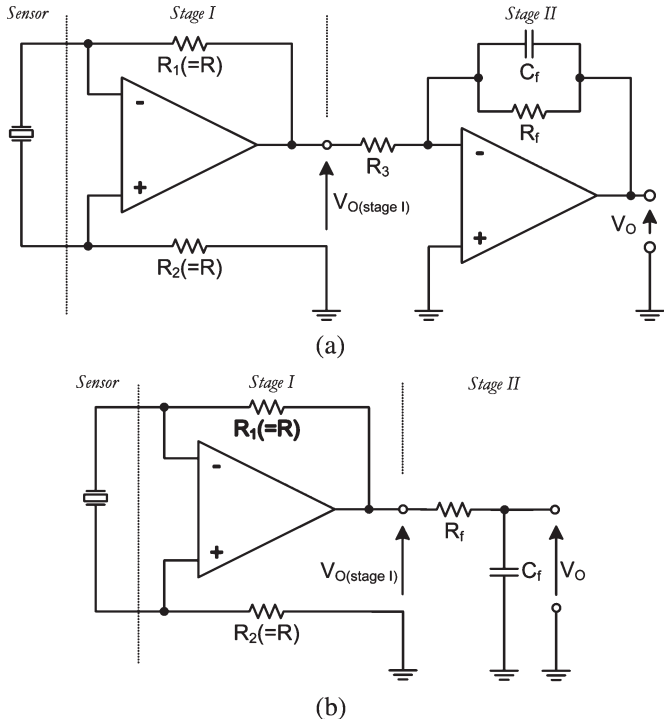

Fig. 3. Two-stage differential charge and transresistance amplifiers with (a) active and (b) passive second stage, proposed as first implementation of the general approach of Fig. 2. Table I shows their basic features.

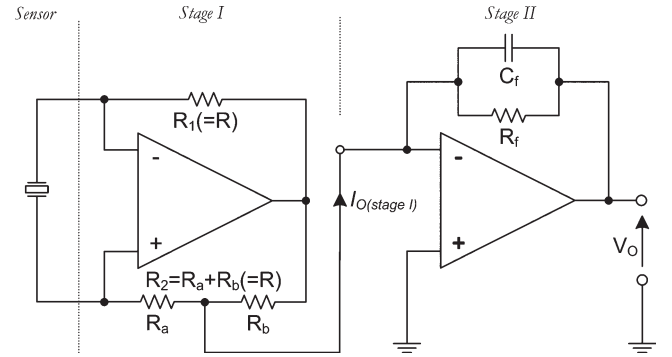

Fig. 4. Two-stage differential charge and transresistance amplifiers, proposed as second implementation of the general approach of Fig. 2. Table I shows their basic features.

transfer functions and sensitivities with respect to charge and current input. It is now clearer that the proposed circuits in Figs. 3 and 4 only need a single matching condition instead of the multiple ones that are required for the circuits in Fig. 1. Moreover, the required matching is easier to achieve because it only involves resistors and not capacitors that, particularly in a discrete implementation, often have quite wide tolerance values, which would result in worse matching, as compared to resistors.

Besides the number and type of matching conditions, the presented circuits can be also compared for their sensitivity (also summarized in Table I), the sensor common-mode voltage rejection, the output impedance, and the complexity. The circuits in Figs. 3(a) and 4, in comparison with that in Fig. 1(a), can feature the same sensitivity with lower component count, and their main drawback is the signal-dependent common-mode voltage of the sensor. The same circuits, with respect to that in Fig. 1(b), feature higher sensitivity, but at the expense of using additional components. Last, the circuit in Fig. 3(b), in comparison with that in Fig. 1(b), can reach higher sensitivity (if $R > R_f$) with the same component count; however, its output impedance is obviously worse.

The presented circuits can be used as charge or transresistance amplifiers with only minor redesign. Table I and Fig. 5 illustrate the different frequency responses (G_D) and sensitivities (S_Q, S_I) that are obtained from the same topology but considering either charge or current as input. The charge amplifier has a high-pass response, and its pole is usually placed at very low frequency to approximate an ideal integrator. The transresistance amplifier has a low-pass response, and the dominant pole is fixed to define the passband. In the first case, the sensitivity S_Q is mainly defined by the capacitance C_f that performs the charge-to-voltage conversion (the resistance R_f just sets the op-amp closed loop in dc), whereas in the second one, the sensitivity S_I mainly depends on the resistance R_f that performs the current-to-voltage conversion (the capacitor C_f, if kept, only serves to limit the bandwidth).

In the remainder of this paper, the attention is focused on the novel circuits in Figs. 3(a) and 4, which are compared with the topology of Fig. 1(b), chosen as the benchmark. Besides the results just presented, which are obtained assuming ideal active and passive devices, other relevant effects such as sensor parasitics, mismatch, op-amp limitations, and noise are studied in detail to optimize the design against their influence. Measurement results of the circuits are finally included.

A. Sensor Model

Before going over the analysis, it is necessary to take into account the nature of the typical sensors that are applied to the charge and transresistance amplifiers. For most practical purposes, a suitable model is shown in Fig. 6, where C_S represents the capacitive nature, R_S is the leakage resistance, I_D is the generated differential-mode current that carries the information provided by the sensor according to the measured physical magnitude, and I_C is the common-mode current typically due to interference from the environment (the authors found this latter problem, e.g., in sensors that are attached to metallic materials that are susceptible to strong electrostatic charge or discharge processes).

The model applies, for instance, to piezoelectric sensors [13], where, typically, C_S is in the order of hundreds of picofarads, and R_S is in the order of tens of megaohms, so that, in practice, it is often considered infinite. Moreover, the sensor also exhibits some kind of resonance, a typical characteristic of piezoelectric materials. Most of the time, it is avoided when the sensor is used as an accelerometer or pressure sensor, or exploited, such as, for instance, in ultrasonic receivers and transmitters. Thus, the resonance needs to be modeled when the overall transfer function from physical magnitude to voltage has to be predicted but is not required, in general, to optimize the charge amplifier.

TABLE I
BASIC FEATURES OF THE CONVENTIONAL CIRCUITS OF FIG. 1 AND THE PROPOSED CIRCUITS OF FIGS. 3 AND 4 (REQUIRED MATCHING CONDITIONS, IDEAL TRANSFER FUNCTIONS, AND SENSITIVITY WITH RESPECT TO CHARGE AND CURRENT INPUTS)

Circuit	Matching condition ($G_C = 0$, $CMRR = \infty$)	Transresistance amplifier		Charge amplifier	
		$G_D = V_O/I_D$	S_I	$G_D = V_O/Q_D$	S_Q
Figure 1a	$R_1 = R_2 = R_f$, $C_1 = C_2 = C_f$, $R_6/R_5 = R_4/R_3$ (22)	$\frac{2R_f}{1+sR_fC_f}\frac{R_4}{R_3}$ (23)	$2R_f\frac{R_4}{R_3}$ (24)	$\frac{2sR_f}{1+sR_fC_f}\frac{R_4}{R_3}$ (25)	$\frac{2}{C_f}\frac{R_4}{R_3}$ (26)
Figure 1b	$R_1 = R_2 = R_f$, $C_1 = C_2 = C_f$ (27)	$\frac{2R_f}{1+sR_fC_f}$ (28)	$2R_f$ (29)	$\frac{2sR_f}{1+sR_fC_f}$ (30)	$\frac{2}{C_f}$ (31)
Figure 3a	$R_1 = R_2 = R$ (32)	$\frac{2R}{R_3}\frac{R_f}{1+sR_fC_f}$ (33)	$\frac{2R}{R_3}R_f$ (34)	$\frac{2R}{R_3}\frac{sR_f}{1+sR_fC_f}$ (35)	$\frac{2R}{R_3}\frac{1}{C_f}$ (36)
Figure 3b		$-2R\frac{1}{1+sR_fC_f}$ (37)	$-2R$ (38)	$-2R\frac{s}{1+sR_fC_f}$ (39)	$-2R\frac{1}{R_fC_f}$ (40)
Figure 4	$\begin{cases}R_1 = R\\ R_2 = R_a + R_b = R\end{cases}$ with: $\begin{cases}R_a = (1-a)R\\ R_b = aR\\ 0 < a \le 1\end{cases}$ (41)	$\frac{2}{a}\frac{R_f}{1+sR_fC_f}$ (42)	$\frac{2}{a}R_f$ (43)	$\frac{2}{a}\frac{sR_f}{1+sR_fC_f}$ (44)	$\frac{2}{a}\frac{1}{C_f}$ (45)

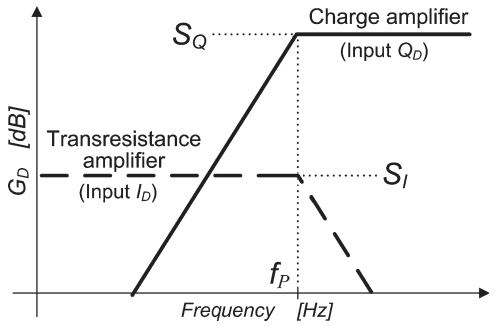

Fig. 5. Typical high-pass and low-pass frequency responses of charge and transresistance amplifiers. The passband is defined by the pole frequency f_P and the sensitivities by S_Q and S_I.

Because of the relationship between charge and current [$I(s) = sQ(s)$ in the s-domain], it is easy to swap between both equivalent sensor models of Fig. 6, allowing the study of the same circuit from different points of view. Anyway, the current model [Fig. 6(c)] is preferred to develop the mathematical analysis.

B. Second-Order Analysis

Because of the two independent stages topology, the second-order analysis of the circuits in Figs. 3 and 4 is better done stage by stage. The single-stage benchmark circuit in Fig. 1(b) is also studied.

1) Benchmark Circuit in Fig. 1(b): For this circuit, considering the ideal op-amp and the source of Fig. 6(c), the output is given by (1). It clearly shows that to obtain a complete common-mode rejection (CMRR $= \infty$), the double matching condition between resistances $R_1 = R_2 = R_f$ and capacitors $C_1 = C_2 = C_f$ is needed [Table I, (27)]. Applying them to (1), the ideal circuit response of (28)–(31) in Table I is obtained, i.e.,

$$V_O = \underbrace{-\frac{(R_1+R_2)+sR_1R_2(C_1+C_2)}{R_1R_2C_1C_2s^2+(R_1C_1+R_2C_2)s+1}}_{G_D} \times \left[I_D + \underbrace{\frac{(R_1-R_2)+sR_1R_2(C_2-C_1)}{(R_1+R_2)+sR_1R_2(C_1+C_2)}}_{1/\text{CMRR}} I_C \right]. \quad (1)$$

In practice, the matching conditions can only be approximated resulting in a finite CMRR. Considering component tolerances in the worst-case situation, given by $R_1 = R_f(1+t_R)$, $R_2 = R_f(1-t_R)$, $C_1 = C_f(1+t_C)$, and $C_2 = C_f(1-t_C)$, the minimum CMRR is given in the following, where R_f and C_f are the ideal component values, and t_R and t_C the component tolerances (e.g., $t_R = 0.01$ for 1% resistor):

$$\text{CMRR}_{\min} = \frac{1 - sR_fC_f\left(t_R^2-1\right)}{t_R + sR_fC_f\left(t_R^2-1\right)t_C} \begin{cases} \text{Pole } s = \frac{-t_R/t_C}{R_fC_f\left(t_R^2-1\right)} \\ \text{Zero } s = \frac{1}{R_fC_f\left(t_R^2-1\right)} \end{cases}. \quad (2)$$

It is noted from (2) that in dc (i.e., $s = 0$), $|\text{CMRR}_{\min}|$ is $1/t_R$, whereas at higher frequencies (i.e., $s \to \infty$), it is $1/t_C$. This means that $|\text{CMRR}_{\min}|$ is determined by resistance mismatch at low frequency and by capacitor mismatch at the higher ones. At intermediate frequencies, $|\text{CMRR}_{\min}|$ may exhibit three different behaviors, depending on the ratio t_R/t_C that determines the relative position of its pole and zero.

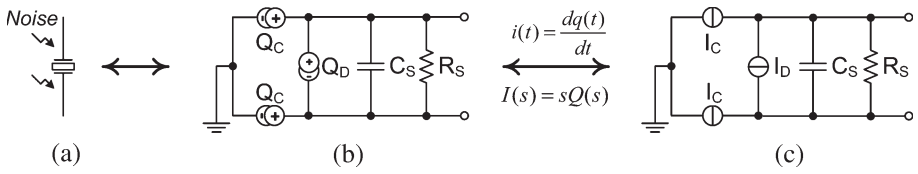

Fig. 6. (a) Typical sensor used in conjunction with charge and transresistance amplifiers can be represented by (b) its charge or (c) its current equivalent model.

For a discrete realization, the condition $t_C > t_R$ can be typically assumed, so that $|\text{CMRR}_{\min}|$ decreases with frequency.

The most critical matching is that between resistors because, in general, it is important to reject the common-mode input low-frequency components that often have the highest power levels.

2) Circuits in Fig. 3—Stage I: For this circuit, considering the ideal op-amp and the source of Fig. 6(c), the output is given by

$$V_{O(\text{Stage I})} = \underbrace{-(R_1+R_2)}_{G_D}\left(I_D + \underbrace{\frac{R_1-R_2}{R_1+R_2}}_{1/\text{CMRR}} I_C\right). \quad (3)$$

Assuming the matching condition $R_1 = R_2 = R$ [Table I, (32)], the ideal behavior is obtained: $G_D = V_{O(\text{Stage I})}/I_D = -2R$, and $\text{CMRR} = \infty$. In practice, it is affected by the mismatch and the actual op-amp response, as shown in the remainder of this section.

The theoretically infinite CMRR is practically limited by the resistor tolerances that yield mismatch. Substituting the worst-case condition $R_1 = R(1+t_R)$ and $R_2 = R(1-t_R)$ into (3), the minimum CMRR is obtained as given by

$$\text{CMRR}_{\min} = 1/t_R. \quad (4)$$

$|\text{CMRR}_{\min}|$ is inversely proportional to the resistor tolerance t_R, e.g., it is 40 and 60 dB for 1% and 1‰ resistors, respectively. Therefore, high-precision resistors are required to optimize the CMRR. It is also noted that to obtain a high CMRR, only $R_1 = R_2 = R$ is required; however, it is irrelevant how the resistor values differ from the ideal value R. If, e.g., $R_1 = R_2 = R(1+t_R)$, the gain corresponding to G_D is $-2R(1+t_R)$ instead of the ideal value $-2R$, but still, $\text{CMRR} = \infty$.

Now, perfect matching is considered, and the effects of the op-amp imperfections on G_D and CMRR are studied. At low frequency, it can be considered, with very good level of approximation, that the feedback action of the op-amp virtually shorts the sensor terminals; however, at higher frequencies, the op-amp open-loop gain rolls off, and a finite input error voltage exists. Therefore, despite its simplicity, this circuit has a two-pole frequency response that can be only explained by considering the real op-amp response and the dominant capacitive behavior of the sensor.

A detailed analysis is presented in the Appendix, leading to (15) and (16). Here, to provide an intuitive grasp of the main effects, typical approximations are applied to the results. The sensor leakage resistance R_S is considered infinite, and the op-amp is modeled with an output resistance $R_{OA} \ll 2R$ and a dc gain $A_0 \gg 1$. Therefore

$$G_D = \frac{V_{O(\text{Stage I})}}{I_D} = -2R\frac{1 - s\frac{R_{OA}}{2RA_0\omega_a}}{s^2\frac{1}{\omega_n^2} + s\frac{2\zeta}{\omega_n} + 1} \quad (5)$$

$$\zeta = \frac{1}{2}\frac{2RC_S\omega_a + 1}{\sqrt{2RC_SA_0\omega_a}} \quad \omega_n = \sqrt{\frac{A_0\omega_a}{2RC_S}} \quad (6)$$

$$\text{CMRR} = -2R\frac{A_0}{R_{OA}} \cdot \frac{1 - s\frac{R_{OA}}{2RA_0\omega_a}}{s^2\frac{2RC_S}{\omega_a} + s\frac{2RC_S\omega_a+1}{\omega_a} + 1}. \quad (7)$$

The location of the poles in (5) enforces stability; however, depending on the damping factor ζ, the circuit response can have an unwanted resonant peak at frequency ω_n [see (6)]. This is the case in typical application where C_S is of the order of hundreds of picofarads, and R is of the order of tens of kiloohms. The CMRR result, as (7) shows, is limited by the op-amp nonidealities, and it is proportional to R since increasing R increases G_D but not G_C. Anyway, this expression practically applies only at higher frequencies, where the op-amp open-loop gain rolls off. At lower frequencies, because of the good op-amp performance, the CMRR dominant limitation is a mismatch, as practically described by (4).

3) Circuit in Fig. 4—Stage I: The output current of this circuit, considering ideal op-amps and the source of Fig. 6(c), is given by

$$I_{O(\text{Stage I})} = \underbrace{-\frac{R_1 + (R_a+R_b)}{R_b}}_{G_D}\left[I_D + \underbrace{\frac{R_1 - (R_a+R_b)}{R_1 + (R_a+R_b)}}_{1/\text{CMRR}} I_C\right]. \quad (8)$$

Considering the matching condition (41) in Table I, the ideal behavior of the circuit is characterized by $G_D = I_{O(\text{Stage I})}/I_D = -2/a$, and $\text{CMRR} = \infty$. It is interesting to note that G_D only depends on the parameter named a. In practice, this ideal response is affected by the mismatch between the resistors and the op-amp nonidealities, as shown in the remainder of this section.

The mismatch analysis is identical to that described for the circuits in Fig. 3 by simply considering that the resistances to be matched are now R_1 and $R_2 = R_a + R_b$. Therefore, the resulting $\text{CMRR}_{\min}$ is given again by (4).

Now, perfect matching is considered, and only the effects of the op-amp limitations are studied. The complete analysis is presented in the Appendix, leading to (18)–(21). Here, some

typical approximations are introduced: R_S infinite, $R_{OA} \ll aR$, and $A_0 \gg 1$. The results are given by the following expressions:

$$G_D = \frac{I_{O(\text{Stage I})}}{I_D} = -\frac{2}{a}\frac{s\frac{1}{\frac{2}{a}A_0\omega_a}+1}{s^2\frac{1}{\omega_n^2}+s\frac{2\zeta}{\omega_n}+1} \tag{9}$$

$$\zeta = \frac{1}{2}\frac{RC_S(2-a)\omega_a+1}{\sqrt{RC_S(2-a)A_0\omega_a}} \qquad \omega_n = \sqrt{\frac{A_0\omega_a}{RC_S(2-a)}} \tag{10}$$

$$\text{CMRR} = \frac{2}{a}A_0\frac{s\frac{1}{\frac{2}{a}A_0\omega_a}+1}{s^2\frac{2RC_S}{\omega_a}+s\frac{2RC_S\omega_a+1}{\omega_a}+1} \tag{11}$$

$$Z_O = aR\frac{A_0}{\omega_a}\frac{s^2\frac{\omega_a}{\omega_n^2}+s\frac{2\zeta\omega_a}{\omega_n}+1}{\left(\frac{s}{\omega_a}+1\right)(s2RC_S+1)}. \tag{12}$$

It is concluded that the circuit is of order two [see (9)], and, depending on the damping factor ζ, it can have a resonance peak at the frequency ω_n (10), which is commonly found in typical applications. The CMRR is well described by (11) only at high frequencies; however, at low frequencies, mismatch dominates (4). Last, the output impedance (12), which is ideally infinite, is proportional to R. Therefore, the R value must be, in practice, high enough to obtain the desired high output impedance.

4) Circuits in Figs. 3(a), (b), and 4—Stage II: The second stages of these circuits are simple single-ended lossy integrators, with some minor differences depending on the case. Their ideal transfer functions are respectively given by $V_O/V_{O(\text{Stage I})} = -(R_f/R)/(1+sR_fC_f)$, $V_O/V_{O(\text{Stage I})} = -1/(1+sR_fC_f)$, and $V_O/I_{O(\text{Stage I})} = -R_f/(1+sR_fC_f)$; therefore, the pole is controlled by R_fC_f.

The integrator is active in Figs. 3(a) and 4 (with the advantage of amplification) and passive in Fig. 3(b) (with the advantage that no op-amp is needed, and the drawback of a worst output impedance). Moreover, the integrated magnitude is voltage for the circuits in Fig. 3 and current for the circuits in Fig. 4 (i.e., it also performs a current-to-voltage conversion).

C. Noise Analysis

This section focuses on the circuit's inherent noise due to its active and resistive components. Op-amp noise performance is routinely characterized by a voltage and two current equivalent input noise generators of spectral densities e_n, i_{np}, and i_{nn}, respectively [11]. Capacitors are considered noiseless. The thermal noise of a resistance R is described by a current equivalent noise generator of power density $i_{nR}^2 = 4kT/R$, where k is the Boltzmann constant, and T is the absolute temperature [11]. The sensor, which is represented by its model of Fig. 6(c), also suffers from thermal noise due to its internal resistance. To definitely clarify the model that we used for the noise analysis, the proposed circuits in Figs. 3(a) and 4 are also shown by Fig. 7(a) and (b), respectively, with the addition of the noise sources and assuming the matching conditions (32) and (41), respectively.

In low noise applications, it is of interest to know the total output ac noise of the circuit because it can be referred back to the input and compared against the useful signal to determine the SNR. This is defined by the ratio between the rms values of the useful signal and the input equivalent noise. Assuming that all the noise sources are uncorrelated, the total ac noise is given by the superposition principle as the rms sum of all the input-referred noise contributions.

Clearly, the SNR has to be maximized. Anyway, instead of analyzing the complicated global SNR expression, it is also efficient and easier to consider the SNRs corresponding to the isolated effect of each noise source. They are shown in (46)–(60) in Table II for both circuits in Fig. 7(a) and (b).

Each SNR has to be maximized in the passband, which depends on whether the circuit is used as a charge amplifier or transresistance (see Fig. 5). Consider, e.g., the particular SNR shown in (49) in Table II and I_D as the input. Hence, the SNR value in the passband (obtained for $s=0$) is $(R_S//2R)I_D/V_{n1}$, and, considering $R_S \approx \infty$ for a typical sensor, it is maximized by a high R value. Considering now Q_D as the input, the SNR passband value (obtained for $s \to \infty$) is Q_D/C_SV_{n1} and cannot be maximized by the design because C_S depends on the sensor.

Just applying similar analysis to all the SNRs of Table II and summarizing the results, the design criteria shown in the noise section of Table III are finally obtained. In addition, some general conclusion can be given. Equation (46) in Table II defines the reference SNR that cannot be improved by the design because the sensor-inherent noise is mixed with the useful signal. Obviously, low-noise op-amps increase the SNR, reducing the terms e_n, i_{nn}, and i_{np}. Finally, an optimization criterion results from the two-stage topology. An increase in the first-stage gain ($-2R$ for the circuit in Fig. 3; $-2/a$ for the circuit in Fig. 4) improves the global SNR because the relative weight of the second-stage noise sources is lowered.

D. Offset Analysis

The dc offset analysis can be easily accomplished, as usual [11], taking into account for the op-amps the typical bias I_B and offset I_{OS} currents and the offset voltage V_{OS}. Therefore, the dc output voltages of the circuits in Figs. 3(a) and 4 are, respectively, given by (13) and (14), where the numerical subscript stands for first or second stage, i.e.,

$$V_O|_{\text{dc}} = V_{OS2} - R_f\left(I_{B2} + \frac{I_{OS2}}{2} + \frac{V_{OS1}-V_{OS2}-RI_{OS1}}{R_3}\right) \tag{13}$$

$$V_O|_{\text{dc}} = V_{OS2} - R_f\left\{I_{B1}\left[R(1-a)-1\right] + \frac{I_{OS1}}{2}\left[R(a-1)+\frac{a-2}{a}\right] + \frac{V_{OS1}}{aR} + I_{B2} + \frac{I_{OS2}}{2}\right\}. \tag{14}$$

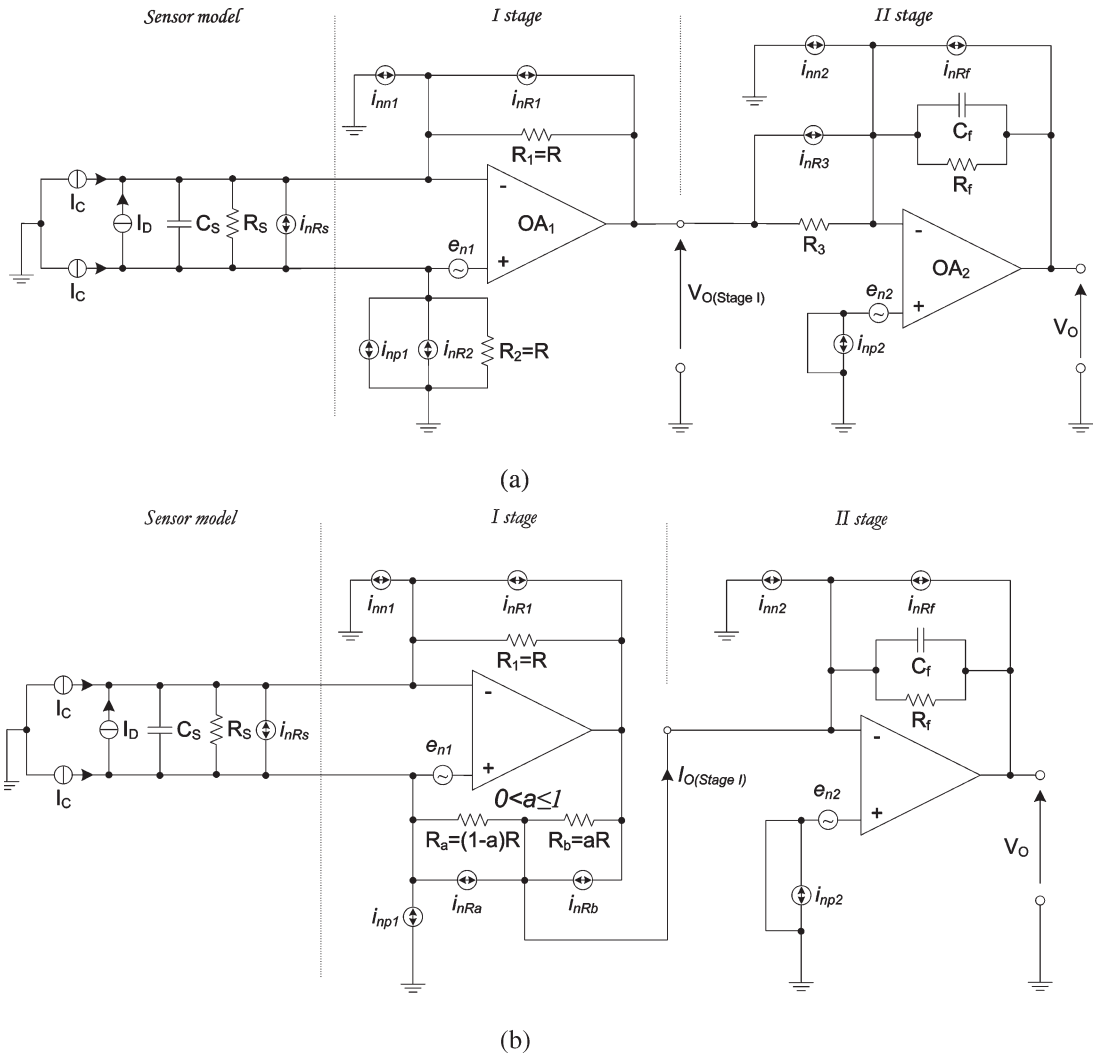

Fig. 7. Noise equivalent models for the circuit in (a) Fig. 3(a) and (b) Fig. 4. Matching conditions (32) and (41) of Table I and the sensor model of Fig. 6(c) are assumed.

Obviously, $|V_O|_{\rm dc}| < V_{CC}$ is assumed, where V_{CC} is the supply voltage. In practice, to meet this condition, field-effect-transistor (FET) input and low-offset op-amps are recommended, particularly in integrated realization where the voltage supply can be quite low. Anyway, if integration was intended to high-volume low-cost production, then a standard CMOS process would probably be the best compromise solution.

In a typical design with standard op-amps, I_B and I_{OS} are in the order of picoamperes, V_{OS} is in the order of a few millivolts, and R_f can be quite high. Therefore, for the circuit in Fig. 3(a), the dc operating point (13) is mainly set by V_{OS2}, and no practical problem arises. For the circuit in Fig. 4, the two-stage topology makes the dc output voltage (14) basically determined by V_{OS1}, so that, considering that a is usually kept small to increase sensitivity and that R_f can be high, a relatively high R value is required.

E. Best Design Criteria

The proposed circuits in Figs. 3(a) and 4 have been studied from different points of view (topology complexity, sensitivity, matching and CMRR, op-amp limitations and sensor parasitics, noise, and offset) and with respect to charge and current inputs. Table III summarizes the results, showing the recommended criteria to choose the values of every component with respect to every considered design aspect.

As a conclusion, the best design criteria to obtain high sensitivity and CMRR, low noise and offset, and proper passband and impedances between the two stages of the topology are given. For circuits in Figs. 3(a) and 4, and regardless of the input, the recommendations are as follows: high R and R_f values and low-noise and offset FET input op-amps. In addition, for the circuit in Fig. 3, the following are recommended: high-precision R_1 and R_2 matched resistors and a tradeoff value for R_3 that should be high to guarantee the proper high second-stage input impedance, as well as a tradeoff value for R_3 that should be low in order to not negatively affect sensitivity and noise attenuation. For the circuit in Fig. 4, high-precision R_1, R_a, and R_b matched resistors are recommended; a low value of a can be chosen to increase sensitivity.

Last, the optimum C_f value depends on the application. For charge amplifiers, a tradeoff arises. The very low pole frequency requirement suggests high R_f and C_f values; however, the high sensitivity and low noise requirements suggest a low

TABLE II
SNRs FOR THE PROPOSED CIRCUITS OF FIGS. 3(a) AND 4. THEY ARE CALCULATED BY THE SUPERPOSITION PRINCIPLE AS THE RATE BETWEEN THE USEFUL SIGNAL I_D AND EACH ONE OF THE NOISE SOURCES DETAILED IN FIG. 7(a) [FIG. 3(a)] AND FIG. 7(b) (FIG. 4)

Noise sources		SNRs (with respect to the input I_D)					
		Circuit of figure 7a (figure 3a)		*Circuit of figure 7b (figure 4)*			
Sensor	I_{nR_S}	$I_D/I_{nR_S}=\sqrt{R_S/4kT}\,I_D$	(46)				
I stage	I_{nn1}	$2I_D/I_{nn1}$	(47)				
	I_{np1}	$2I_D/I_{np1}$	(48)				
	V_{n1}	$\dfrac{R_S/\!/2R}{1+s\left(R_S/\!/2R\right)C_S}\dfrac{I_D}{V_{n1}}$	(49)				
	I_{nR_1}	$2I_D/I_{nR_1}=2\sqrt{R/4kT}\,I_D$	(50)				
	I_{nR_2}	$2\dfrac{I_D}{I_{nR_2}}=2\sqrt{\dfrac{R}{4kT}}I_D$	(51)	I_{nR_a}	$\dfrac{2}{\sqrt{1-a}}\dfrac{I_D}{I_{nR}}$	$2\dfrac{I_D}{I_{nR_2}}=$ $=2\sqrt{\dfrac{R}{4kT}}I_D$	(52)
				I_{nR_b}	$\dfrac{2}{\sqrt{a}}\dfrac{I_D}{I_{nR}}$		
II stage	I_{nR_3}	$2\dfrac{R}{R_3}\dfrac{I_D}{I_{nR_3}}=\dfrac{2R}{\sqrt{4kTR_3}}I_D$	(53)	x			
	I_{nn2}	$2\dfrac{R}{R_3}\dfrac{I_D}{I_{nn2}}$	(54)	$\dfrac{2}{a}\dfrac{I_D}{I_{nn2}}$			(55)
	I_{np2}	∞	(56)				
	V_{n2}	$2\dfrac{R}{R_3}\dfrac{R_3/\!/R_f}{1+s\left(R_3/\!/R_f\right)C_f}\dfrac{I_D}{V_{n2}}$	(57)	$\dfrac{2}{a}\dfrac{R_f}{1+sR_fC_f}\dfrac{I_D}{V_{n2}}$			(58)
	I_{nR_f}	$2\dfrac{R}{R_3}\dfrac{I_D}{I_{nR_f}}=2\dfrac{R}{R_3}\sqrt{\dfrac{R_f}{4kT}}I_D$	(59)	$\dfrac{2}{a}\dfrac{I_D}{I_{nR_f}}=\dfrac{2}{a}\sqrt{\dfrac{R_f}{4kT}}I_D$			(60)

C_f value. For transresistance amplifiers, the C_f value can be simply chosen to meet the passband requirement.

The last problem considered for the presented circuits concerns their first-stage frequency response, which can be resonant. This is concluded by substituting the typical design components values, which are obtained by the criteria presented above, in the damping-factor formulas (6) and (10).

A very low R value would imply no resonance; however, it is not recommended. Anyway, this observation suggests that the resonance peak can be attenuated by reducing the R value just before the resonance frequency by some bypass capacitors that are added to the first stage of the circuit. Relatively small capacitors are enough because R is recommended to be high and because of the contribution from op-amp parasitic capacities. For the first stage of the circuits in Fig. 3, the bypass capacitors are placed in parallel with R_1 and R_2; for the circuit in Fig. 4, the first is placed in parallel with R_1, and the second one is placed from the noninverting op-amp input to ground.

III. EXPERIMENTAL MEASUREMENTS (SETUP, RESULTS, AND DISCUSSION)

To verify the theoretical predictions and lead to more definite conclusions, the proposed circuits in Figs. 3(a) and 4 are experimentally compared with that in Fig. 1(b), taken as reference. The systems that are used to measure G_D and G_C are, respectively, shown in Fig. 8(a) and (b). They consist of a voltage signal generator, a voltage-to-current converter, and the circuit under test. Depending on whether G_D or G_C is measured, a differential-mode or common-mode current is applied to the circuit. The CMRR is indirectly obtained by calculating the ratio G_D/G_C.

The voltage-to-current conversion is obtained by a current conveyor and a resistance. The voltage $V_{\rm in}$ applied to the Y-input is copied to the X-input and results, by (trans)-resistance R_C, in a current that flows through the same input and is copied to the high-impedance output Z, yielding the output current $I_{\rm out}$. The resulting transfer function is $I_{\rm out}/V_{\rm in}=1/R_C$. In Fig. 8(a), R_C is shared to obtain the needed differential current, avoiding matching requirements. In Fig. 8(b), R_{C1} and R_{C2} are matched to obtain identical output currents, as required. In both cases, the circuits, which are built with *AD844* and $R_C=10$ kΩ ($1‰$), exhibit a passband of about 1 MHz with a resistive load of 10 kΩ (wider for lower loads).

The measurements are obtained by the vector signal analyzer *HP89410A* that provides the frequency response of the whole system. At up to 1 MHz, the entire system response is given by $V_{\rm out}/V_{\rm in}=TF/R_C$, where TF is the unknown response.

TABLE III
SUGGESTED CRITERIA TO CHOOSE THE COMPONENT VALUES FOR THE PROPOSED CIRCUITS OF FIGS. 3(a) AND 4 ARE SUMMARIZED. ALL THE DIFFERENT DESIGN ASPECTS STUDIED AND BOTH POSSIBLE INPUTS ARE TAKEN INTO ACCOUNT. LAST, THE BEST DESIGN CRITERIA ARE SYNTHETICALLY SHOWN

Circuit		***Figure 3a (figure 7a)***				***Figure 4 (figure 7b)***			
Components		R	R_3	R_f	C_f	R	a	R_f	C_f
Input		I_D/Q_D	I_D/Q_D	I_D/Q_D	I_D/Q_D	I_D/Q_D	I_D/Q_D	I_D/Q_D	I_D/Q_D
Considered design aspects	**High sensitivity**	H	L	H / x	x / L	x	L	H / x	x / L
	Proper pole frequency (passband)	x	x	x / H	x / H	x	x	x / H	x / H
	Proper impedance for two-stage independency	x	H	x	x	H	x	x	x
	High CMRR	*High-precision matching-resistors are recommended*							
	ac noise	H	L	H	x / L	H	L	H	x / L
		Low-noise op-amps are recommended							
	dc offset	x	x	x	x	H	x	x	x
		FET input and low offset op-amp are recommended							
Conclusion (Best design criteria)		***H***	***C***	***H***	***x / C***	***H***	***L***	***H***	***x / C***
		Are recommended: low-noise and offset, FET input op-amp; high-precision matching-resistors.							
Legend of the table		H – High value recommended. L – Low value recommended. x – Indifferent value. C – Compromise value required.				NOTE: Practical values depend on the desired performance. E.g. see section *III.A.*			

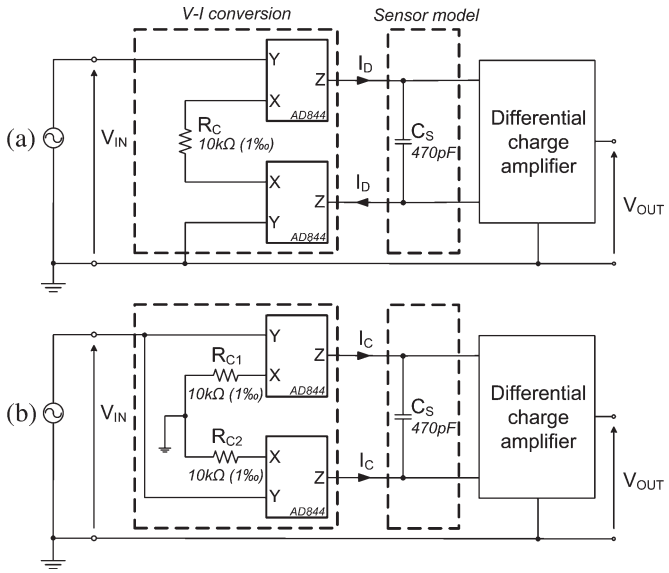

Fig. 8. Measurement system used to test the transfer functions (a) G_D and (b) G_C. It is composed of the test signal generation block that generates (a) differential-mode or (b) common-mode current, a capacitor, representing the sensor capacitance, and the circuit under test.

Therefore, TF is obtained with an attenuation given by R_C (for $R_C = 10$ kΩ, the attenuation is 80 dB).

The tested circuits are designed while taking into account the described criteria (Table III), as well as the need to make possible the comparison among topologies. The selected performance parameters are pole frequency $f_P = 79.6$ Hz and charge and current sensitivities $S_Q = 2 \times 10^9$ V/C (186 dB) and $S_I = 4 \times 10^6$ V/A (132 dB), respectively. Therefore, the benchmark circuit in Fig. 1(b) was built with $R_1 = R_2 = R = 2$ MΩ and $C_1 = C_2 = C = 1$ nF. The circuit in Fig. 3(a) was built with $R_1 = R_2 = R = 10$ kΩ, $R_3 = 5$ kΩ, $R_f = 1$ MΩ, and $C_f = 2$ nF. The circuit in Fig. 4 was built with $R_f = 1$ MΩ, $C_f = 2$ nF, $R_1 = R_2 = R = 200$ kΩ, and $R_a = R_b = 100$ kΩ ($a = 0.5$). The resistor and capacitor tolerances are 1% and 20%, respectively. The 2-MΩ, 200-kΩ, and 5-kΩ resistors and the 2-nF capacitors are made, depending on the case, by the series or parallel association of two equal components. The *TL054* enhanced junction-field-effect-transistor low-offset and noise op-amp is used.

For the circuit in Fig. 3(a), Fig. 9 shows the measured $|G_D|$ and |CMRR| versus frequency comparing different cases: 1) no stabilization ($C_1 = C_2 = 0$ F); 2) stabilization by only a feedback capacitor ($C_1 = 33$ pF, $C_2 = 0$ F); and 3) stabilization by two capacitors ($C_1 = C_2 = 33$ pF). The latter option, resulting in a more symmetrical topology, gives the best result for G_D and CMRR. Analogously to the previous case, the performance of the circuit in Fig. 4 is optimized, stabilizing it by two capacitors ($C_1 = C_2 = 15$ pF), placed as described before.

Last, to compare the obtained performance, Fig. 10 shows $|G_D|$ and |CMRR| versus frequency for the benchmark circuit in Fig. 1(b) and the novel circuits in Fig. 3(a) (stabilized with $C_1 = C_2 = 33$ pF) and Fig. 4 (stabilized with $C_1 = C_2 = 15$ pF). All the circuits have the same $|G_D|$ versus frequency response besides some minor differences at the higher

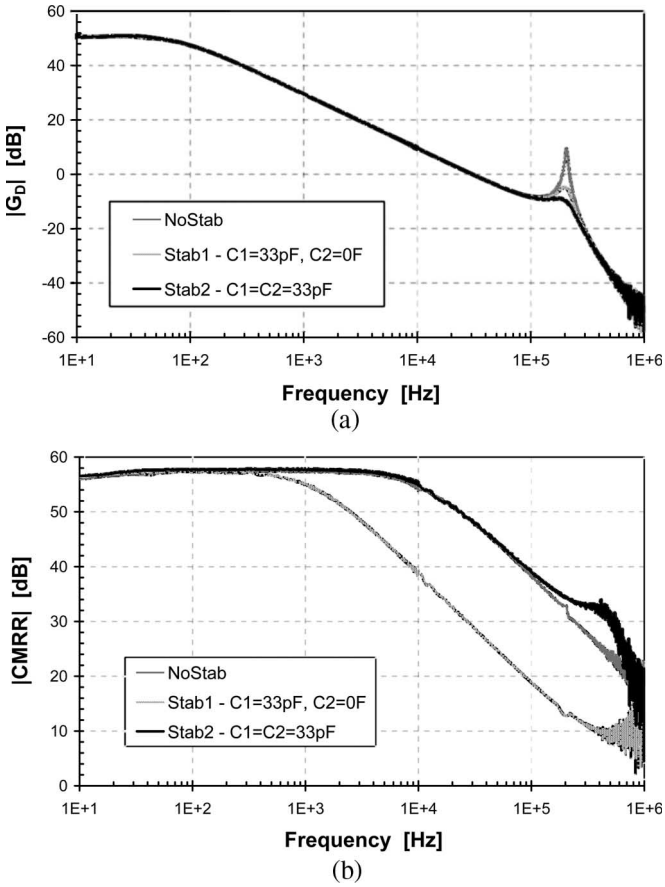

Fig. 9. (a) G_D and (b) CMRR versus frequency for the circuit in Fig. 3(a). The original responses (NoStab) are compared with the ones obtained by attenuating the G_D resonant peak by a single feedback capacitor (Stab1) or by two capacitors (Stab2). The best result is from this latter case.

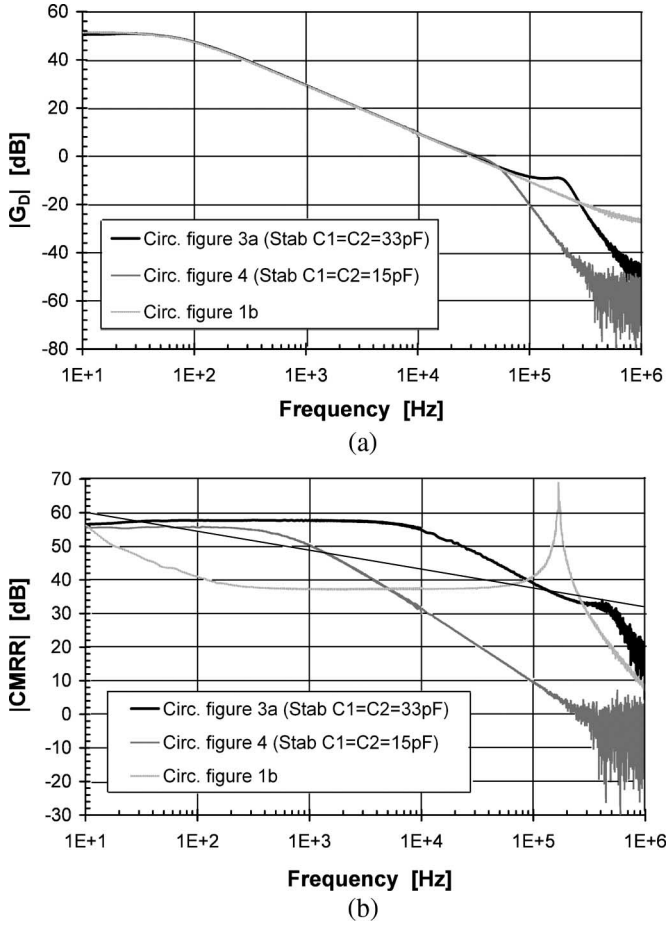

Fig. 10. (a) G_D and (b) CMRR versus frequency for the benchmark circuit in Fig. 1(b) and the circuits in Fig. 3(a) (stabilized with $C_1 = C_2 = 33$ pF) and Fig. 4 (stabilized with $C_1 = C_2 = 15$ pF).

frequency that are due to the op-amp limitations. The differences between the studied circuits mainly reflect in the CMRR versus frequency responses. The particular shapes are mainly due to the mismatch at low frequency and to the op-amp limitation at higher frequency. The measured CMRR is about 57 dB at 10 Hz for all the circuits. By (2) and (4), the $|\text{CMRR}_{min}|$ is 40 dB; therefore, the matching actually obtained from the test is better than the worst case.

For the benchmark circuit in Fig. 1(b), the CMRR falls at very low frequency since capacitor mismatch adds its effect to the resistor mismatch, as theoretically explained by (2). Contrarily, the novel circuits in Figs. 3(a) and 4 exhibit a higher CMRR because it depends only on resistor matching. The op-amp limitations, which are negligible at lower frequencies, are more important as the frequency increases and become dominant when they produce a drop in the CMRR that is higher than the one mismatch does. This corresponds to the corner frequencies that are located at about 700 Hz for the circuit in Fig. 4 and 11 kHz for the circuit in Fig. 3, whereas it corresponds to the resonance peak for the circuit in Fig. 1(b).

It is concluded that, for the same G_D, the novel circuits in Figs. 3(a) and 4 have a better CMRR than the benchmark circuit in Fig. 1(b) because only resistor matching is needed. In particular, the circuit in Fig. 3 has the best CMRR because the low-frequency value is maintained for a wider frequency band. At about 5.3 kHz, the CMRR of the circuit in Fig. 3 is 19 dB higher than the CMRR of the other circuits. These results validate the advantages of the design technique proposed.

IV. Conclusion

Differential charge amplifiers are widely used to interface differential charge-generating sensors because, with respect to the single-ended counterparts, they offer a double sensitivity with respect to the useful differential-mode input and reject the unwanted common-mode input. Anyway, the CMRR of most known topologies is practically limited because it relies on at least two matching conditions between resistors and capacitors. This is because the common-mode rejection and the charge-to-voltage conversion are both implemented by a single stage.

This paper has proposed a design technique to obtain two-stage differential charge amplifiers so that the common-mode input is rejected by the first stage, and the integration is separately implemented by the second one. From this technique, two novel circuits and some possible variants are proposed. As demonstrated by measurements and mathematical analysis, it is concluded that their CMRR is better than the conventional topologies because it only relies on a single resistor matching condition, which is easier to obtain in practice.

$$G_D = \frac{V_{O(\text{Stage I})}}{I_D} = \frac{R_S(R_{OA} - 2RA_0)}{2R + R_{OA} + R_S(A_0+1)} \frac{1 - s\frac{R_{OA}}{(2RA_0 - R_{OA})\omega_a}}{s^2\frac{1}{\omega_n^2} + s\frac{2\zeta}{\omega_n} + 1} \tag{15}$$

$$\zeta = \frac{1}{2}\frac{(1+\omega_a R_S C_S)(2R + R_{OA}) + R_S}{\sqrt{\omega_a R_S C_S (2R + R_{OA})\left[2R + R_{OA} + R_S(A_0+1)\right]}} \qquad \omega_n = \sqrt{\omega_a \frac{2R + R_{OA} + R_S(A_0+1)}{R_S C_S (2R + R_{OA})}} \tag{16}$$

$$\text{CMRR} = \frac{-R_S\left(\frac{2RA_0}{R_{OA}} - 1\right)}{2R + R_S} \frac{1 - s\frac{R_{OA}}{\omega_a(2RA_0 - R_{OA})}}{s^2\frac{2RR_S C_S}{\omega_a(2R+R_S)} + s\frac{2R(1+\omega_a R_S C_S) + R_S}{\omega_a(2R+R_S)} + 1} \tag{17}$$

The proposed circuits have been mathematically studied and compared with the existing ones, taking into account topology complexity, sensitivity, matching and CMRR, op-amp limitations and sensor parasitics, noise, and offset. A simple technique has been proposed to improve the proposed circuits' stability, and it has also been explained how these circuits apply as transresistance amplifiers for current-generating sensors. Last, as a suggestion for designers, best design criteria are given for charge and transresistance amplifiers.

APPENDIX
CIRCUITS OF FIGS. 3 AND 4—STAGE I, GENERAL ANALYSIS

To gain more insight about the first stage of the circuit in Figs. 3 and 4, the effects of the op-amp nonidealities and the interaction with the sensor parasitics are studied, considering the following: the sensor model of Fig. 6(c); the circuit matching conditions (32) and (41); and, for the op-amp, a finite output resistance R_{OA} and the dominant-pole approximation $A_{OL} = A_0/(1 + s/\omega_a)$ (where A_{OL} is the op-amp open-loop gain, A_0 is the dc open-loop gain, and ω_a is the -3-dB cutoff frequency).

For the first stage of the circuit in Fig. 3, in addition to the aforementioned hypothesis, the second-stage input impedance is considered infinite. Hence, (15)–(17) result, shown at the top of the page. From (15), it is clear that the circuit response is of order two due to the op-amp dominant pole and to the sensor capacitance C_S. The fact that all the characteristic polynomial coefficients have the same sign is a necessary and sufficient condition for the circuit to be stable. Anyway, depending on component values, G_D can be resonant as described by the damping factor ζ and the corresponding resonant frequency ω_n (16), calculated from (15). Expression (17) shows that, also, if the resistors are exactly matched, the CMRR is no longer infinite but decreases with frequency. The ideal situation is restored supposing $A_0 \to \infty$ or $R_{OA} = 0\ \Omega$ because of the term A_0/R_{OA}; therefore, limited op-amp gain and finite output resistance reduce the CMRR.

For the first stage of the circuit in Fig. 4, in addition to the aforementioned hypotheses, the second-stage input impedance is considered null. Hence, (18)–(20) result, shown at the bottom of the page.

The circuit response is of order two, is stable, and can have a resonance peak at the frequency ω_n, depending on the damping factor ζ (19). The circuit output impedance is given by

$$Z_O = aR\frac{R\left[2\left(1 + \frac{R_{OA}}{aR}\right) - a\right] + R_S\left(A_0 + 1 + \frac{R_{OA}}{aR}\right)}{\omega_a(2R + R_S)} \times \frac{s^2\frac{\omega_a}{\omega_n^2} + s\frac{2\zeta\omega_a}{\omega_n} + 1}{\left(\frac{s}{\omega_a} + 1\right)\left(s\frac{2RR_S C_S}{2R+R_S} + 1\right)}. \tag{21}$$

$$G_D = \frac{-R_S\left(1 + \frac{2}{a}A_0\right)}{R\left[2\left(1 + \frac{R_{OA}}{aR}\right) - a\right] + R_S\left(A_0 + 1 + \frac{R_{OA}}{aR}\right)} \frac{s\frac{a}{(a+2A_0)\omega_a} + 1}{s^2\frac{1}{\omega_n^2} + s\frac{2\zeta}{\omega_n} + 1} \tag{18}$$

$$\zeta = \frac{1}{2}\frac{R(1+\omega_a R_S C_S)\left[2\left(1 + \frac{R_{OA}}{aR}\right) - a\right] + R_S\left(1 + \frac{R_{OA}}{aR}\right)}{\sqrt{\omega_a R_S C_S R\left[2\left(1 + \frac{R_{OA}}{aR}\right) - a\right]\left\{R\left[2\left(1 + \frac{R_{OA}}{aR}\right) - a\right] + R_S\left(A_0 + 1 + \frac{R_{OA}}{aR}\right)\right\}}}$$

$$\omega_n = \sqrt{\omega_a \frac{R\left[2\left(1 + \frac{R_{OA}}{aR}\right) - a\right] + R_S\left(A_0 + 1 + \frac{R_{OA}}{aR}\right)}{R_S C_S R\left[2\left(1 + \frac{R_{OA}}{aR}\right) - a\right]}} \tag{19}$$

$$\text{CMRR} = \frac{R_S\left(1 + \frac{2}{a}A_0\right)}{\left(1 + 2\frac{R_{OA}}{aR}\right)(2R + R_S)} \frac{s\frac{a}{\omega_a(a+2A_0)} + 1}{s^2\frac{2RR_S C_S}{\omega_a(2R+R_S)} + s\frac{2R(1+\omega_a R_S C_S) + R_S}{\omega_a(2R+R_S)} + 1} \tag{20}$$

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Marco Massarotto was born in Brescia, Italy, in 1977. He received the M.Sc. degree (with honors) in electronic engineering and the Ph.D. degree in electronic instrumentation from the University of Brescia, in 2003 and 2007, respectively.

In 2003, he was a Visiting Scholar with the Polytechnic University of Catalonia, Castelldefels, Spain. From 2003 to 2007, he was a Researcher with the Public University of Navarra, Pamplona, Spain. He is currently with the Dipartimento Elettronica per l'Automazione, Facoltá di Ingegneria, University of Brescia. Within the electronic instrumentation and measurements fields, his main researches regard the design of fully differential and differential analog circuits (voltage filters, charge amplifiers) and the characterization of accelerometers.

Alfonso Carlosena (M'94–SM'05) was born in Navarra, Spain, in 1962. He received the M.Sc. (with honors) and Ph.D. degrees in physics from the University of Zaragoza, Zaragoza, Spain, in 1985 and 1989, respectively.

From 1986 to 1992, he was an Assistant Professor with the Department of Electrical Engineering and Computer Science, University of Zaragoza. In October 1992, he was an Associate Professor with the Public University of Navarra, Pamplona, Spain, where he had also served as Head of the Technology Transfer Office. Since March 2000, he has been a Full Professor with the same university. He was also a Visiting Scholar with the Swiss Federal Institute of Technology, Zurich, Switzerland, and New Mexico State University, Las Cruces, and spent a sabbatical leave (2004–2005) with Connection One, Arizona State University, Tempe. His current research interests are in the area of mixed signal system design, as it applies to instrumentation and communication problems, where he has published over 80 papers in international journals and a similar number of conference presentations. He is the holder of four patents in the field of coin validation mechanisms.

Antonio J. López-Martín (M'04) received the M.Sc. and Ph.D. degrees (with honors) from the Public University of Navarra, Pamplona, Spain, in 1995 and 1999, respectively.

He was a Visiting Professor with New Mexico State University, Las Cruces, and an Invited Researcher with the Swiss Federal Institute of Technology, Zurich, Switzerland. He is currently an Associate Professor with the Public University of Navarra and an Adjunct Professor with New Mexico State University. His current research interests include wireless transceivers and sensor interfaces with emphasis on low-voltage low-power implementations.

Dr. Lopez is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II and is also serving on the technical committees of various conferences. His is the recipient of the IEEE TRANSACTIONS ON EDUCATION Best Paper Award in 2005 and the Young Researcher Award in 2007 from the Complutense University of Madrid, Madrid, Spain.