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CAS

A 1/3-inch 1.12μm-Pitch 13Mpixel CMOS Image Sensor with Low-power Readout Architecture

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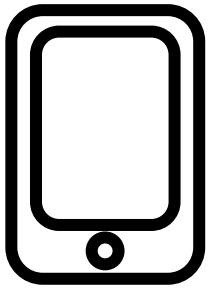
Motivation

High-resolution and High-frame-rate CIS

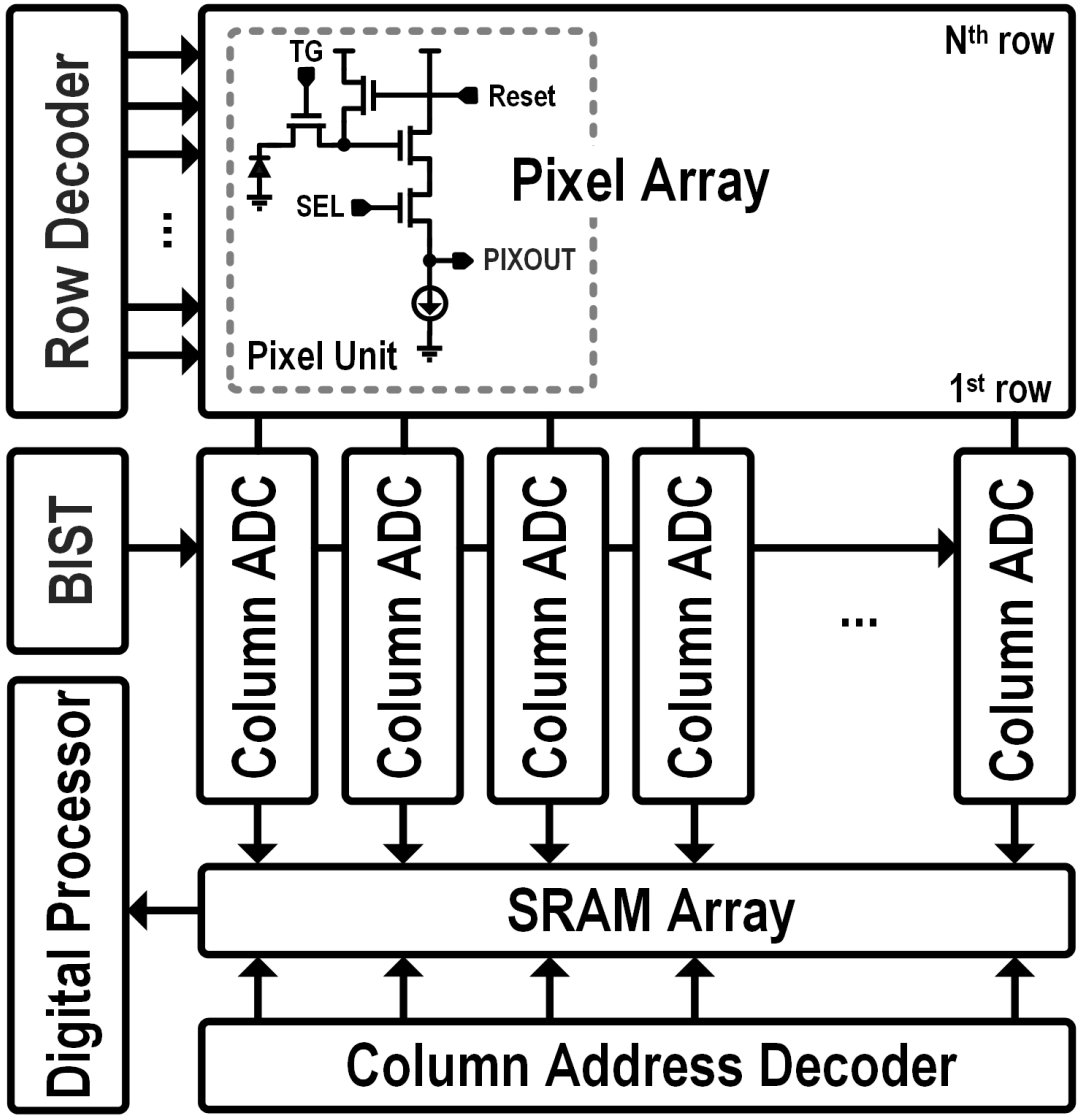


- Smartphone
- Medical device
- Automotive vehicle

Target Spec.	
Resolution	> 10 Mp
Frame rate	30 fps
Noise	< 5 e^-
Bit depth	10 bit
Power	**< 100 mW**

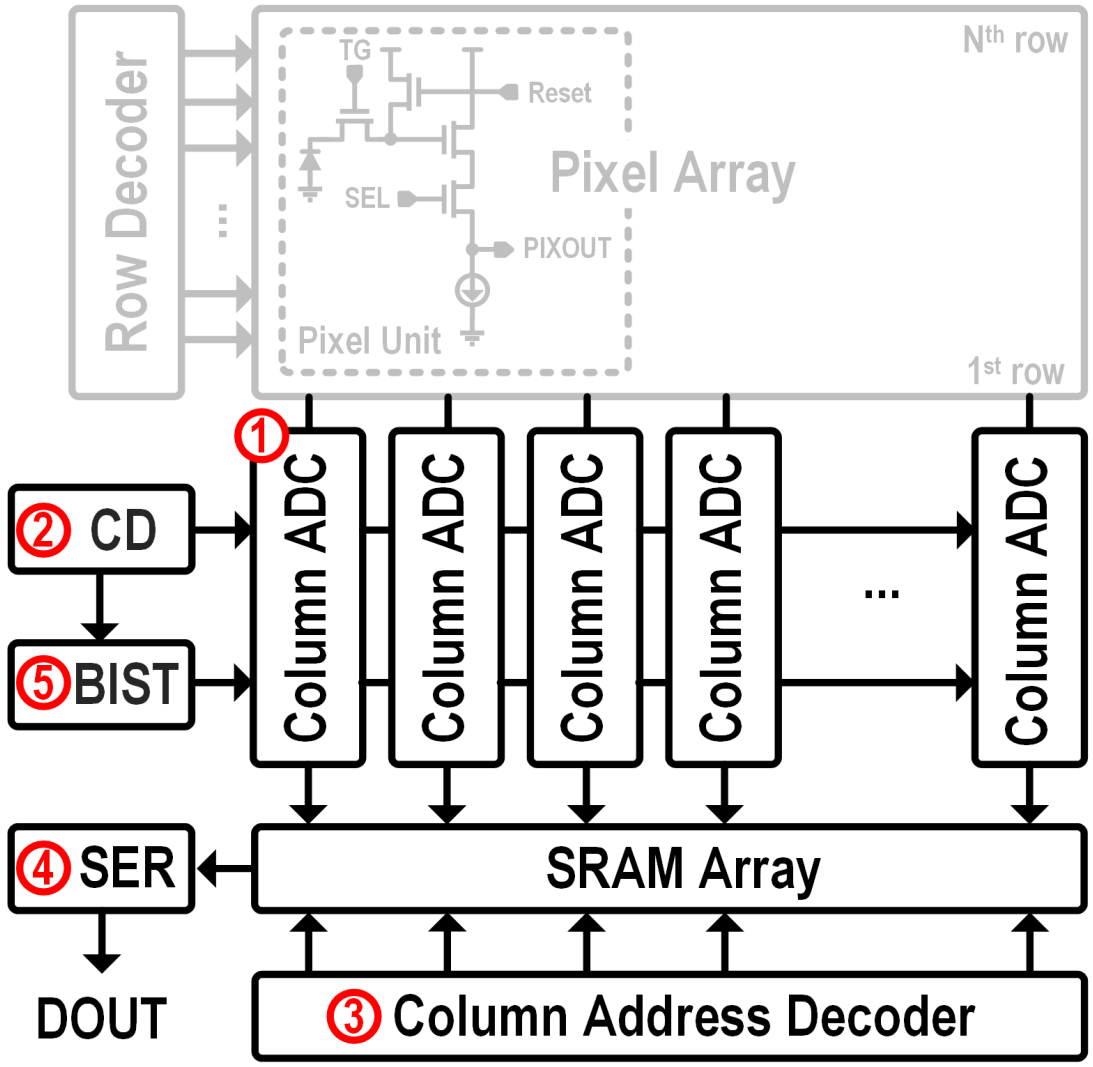
Requires energy-efficient CMOS Image Sensor

Block Diagram - CMOS Image Sensor



- Column parallel ADC structure
- **Single-slope ADC**
  - ⇒ Small Area ☺ & Low Noise ☺
  - ⇒ To maintain energy efficiency ☹
  - ⇒ Frame rate limit ☹
- Built-in self-test (BIST)
  - ⇒ For mass production

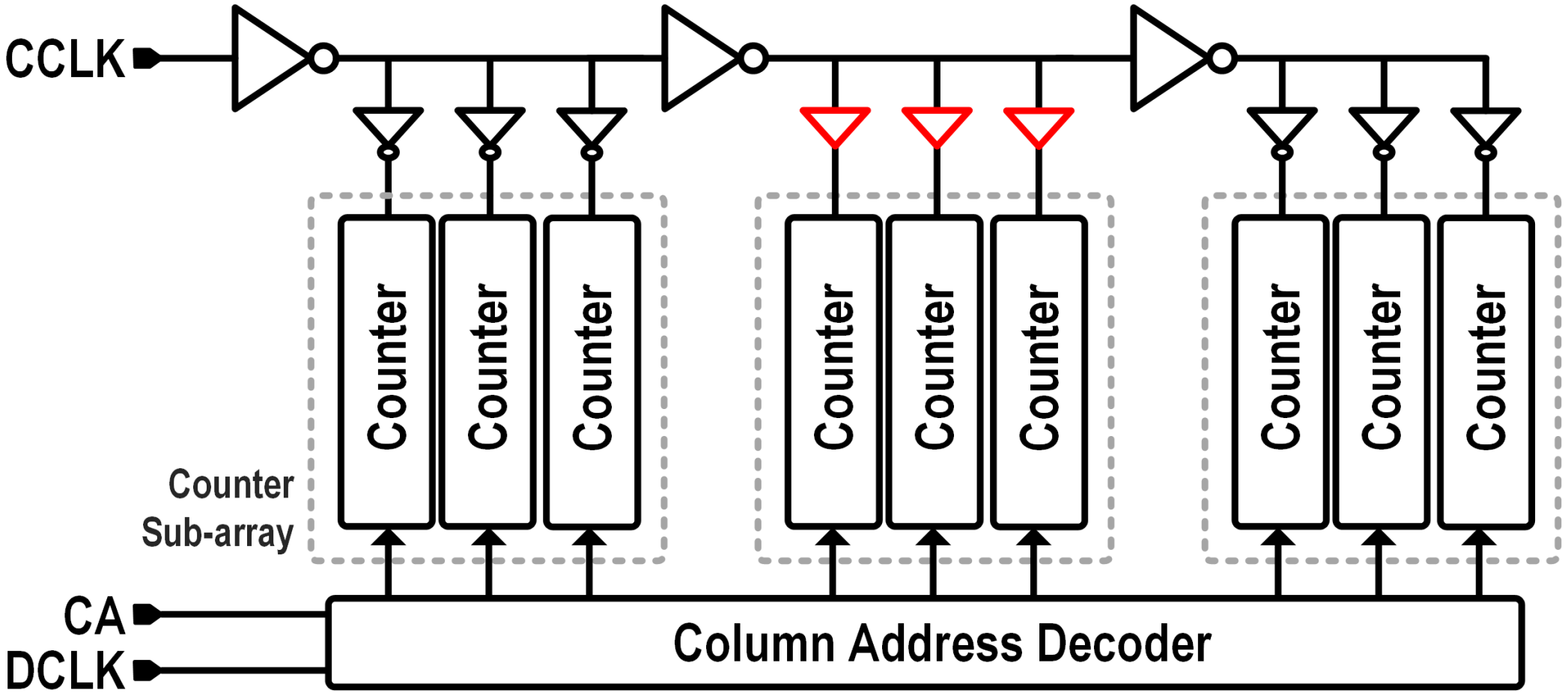
Proposed Architecture



- ① Ripple Counter ⇒ Gray Counter
- ② Clock Driver
  ⇒ Impedance matching technique
- ③ Address Decoder
  ⇒ Pre-decoder & Clock gating
- ④ Analog-level Serializer
- ⑤ Built-in self-test (BIST)
  ⇒ Only Two test patterns

Low-power Readout Architecture!

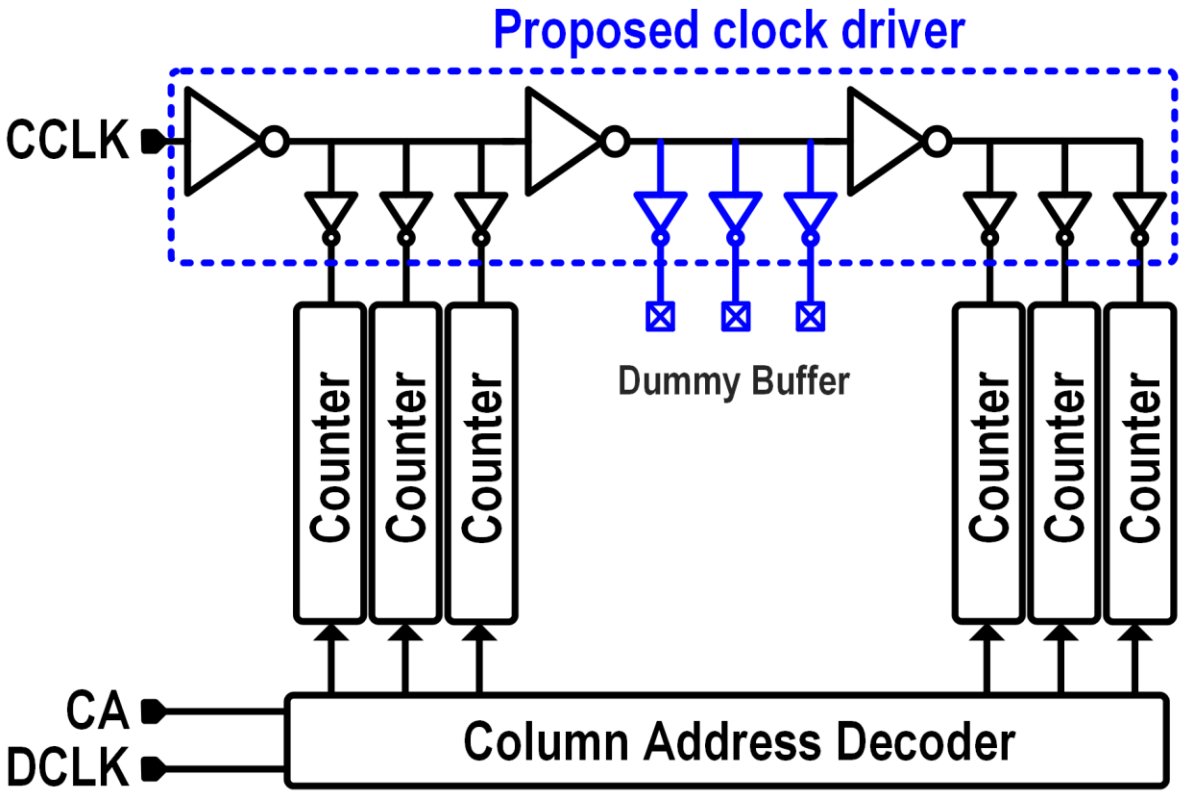
Conventional Clock Driver

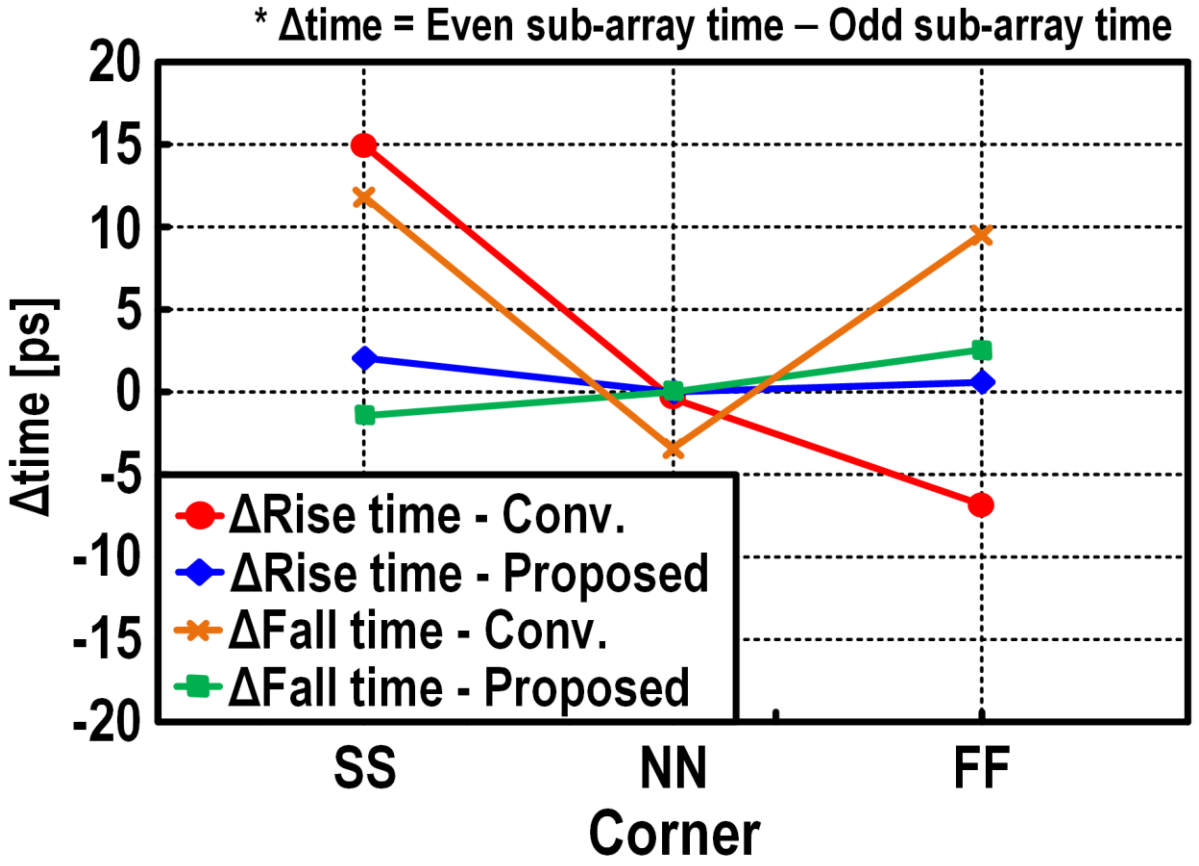


- Conventional Clock Driver

  ⇒ To avoid the large peak current ⇒ Inverter units

Proposed Clock Driver

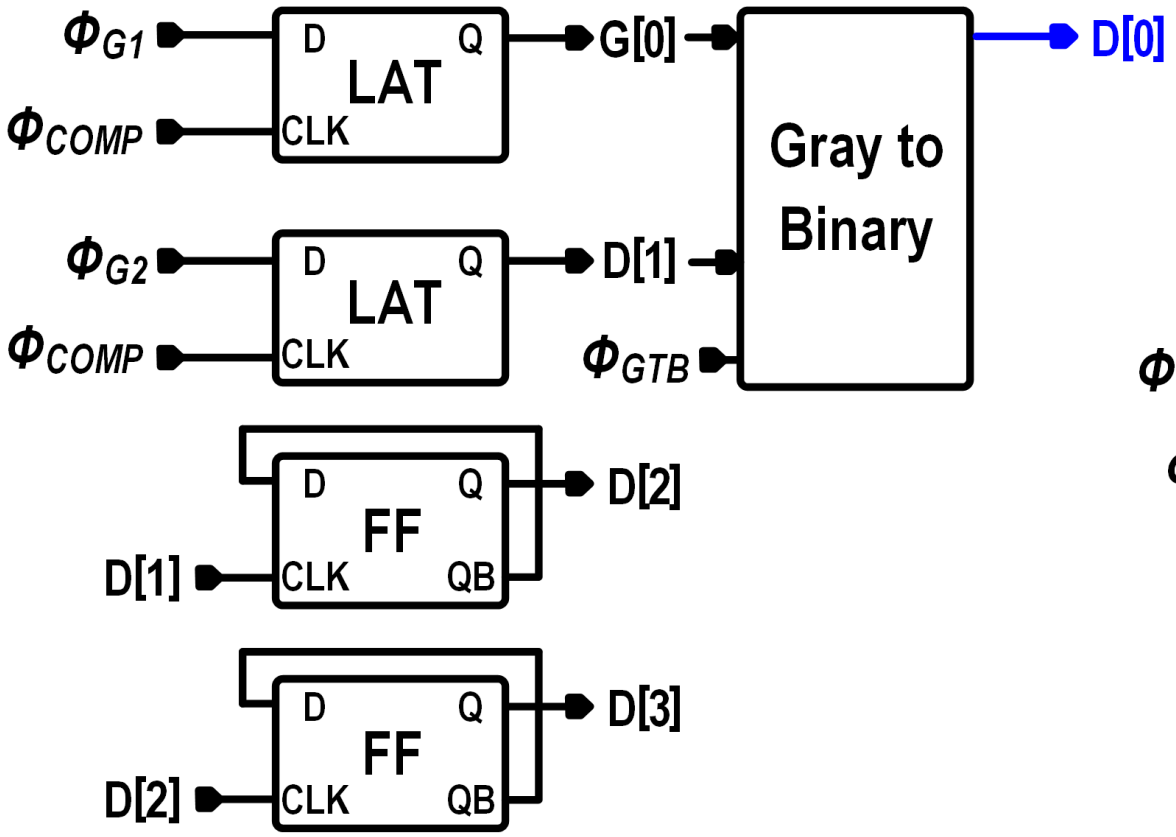


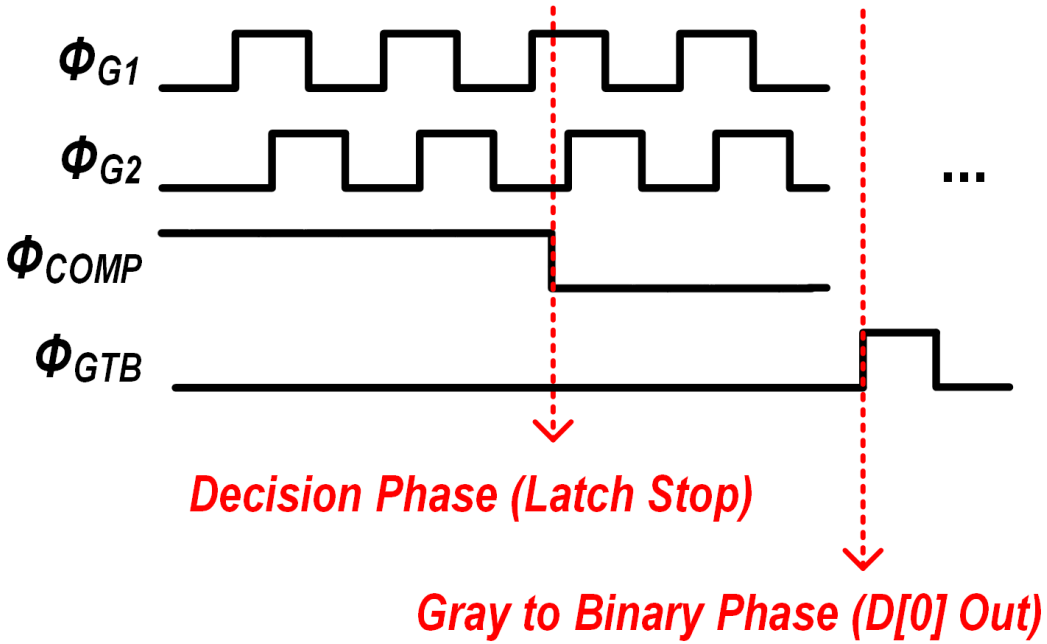


- Added dummy buffer: **Match the load impedance**

  ⇒ Rise / fall time mismatch: < 5 ps ⇒ Buffer size & power ↓ ☺

Proposed Counter Structure

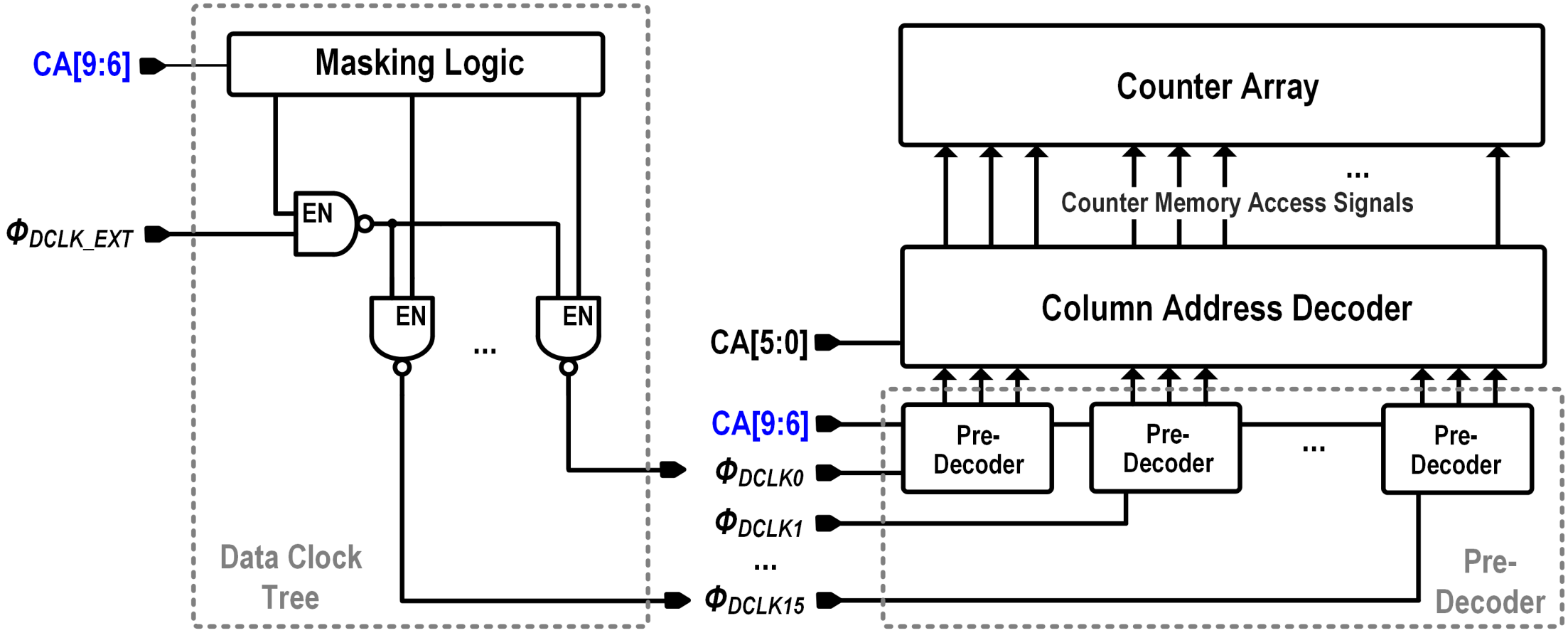




- **2-bit gray counter** + 9-bit ripple counter (+ MSB 1-bit for Overflow)

  ⇒ Power ↓ ☺ ⇒ Only 6.42 mW @ 720 MHz

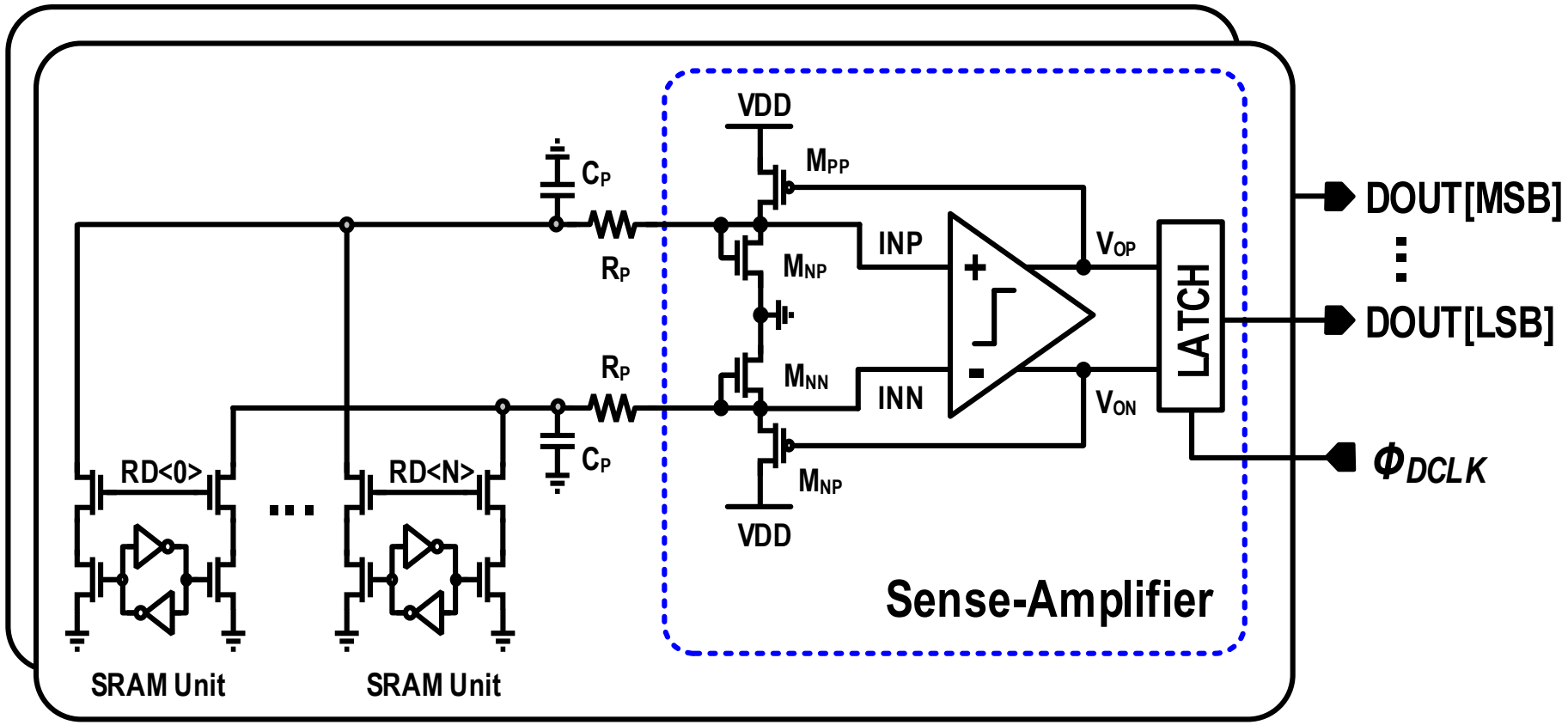
Proposed Address Decoder – Decoder



- Data clock masking + Pre-column address decoder

  $\Rightarrow$ Power $\downarrow$ ☺ $\Rightarrow$ Only 0.4 mW (@ 30 fps, 4240 Column)

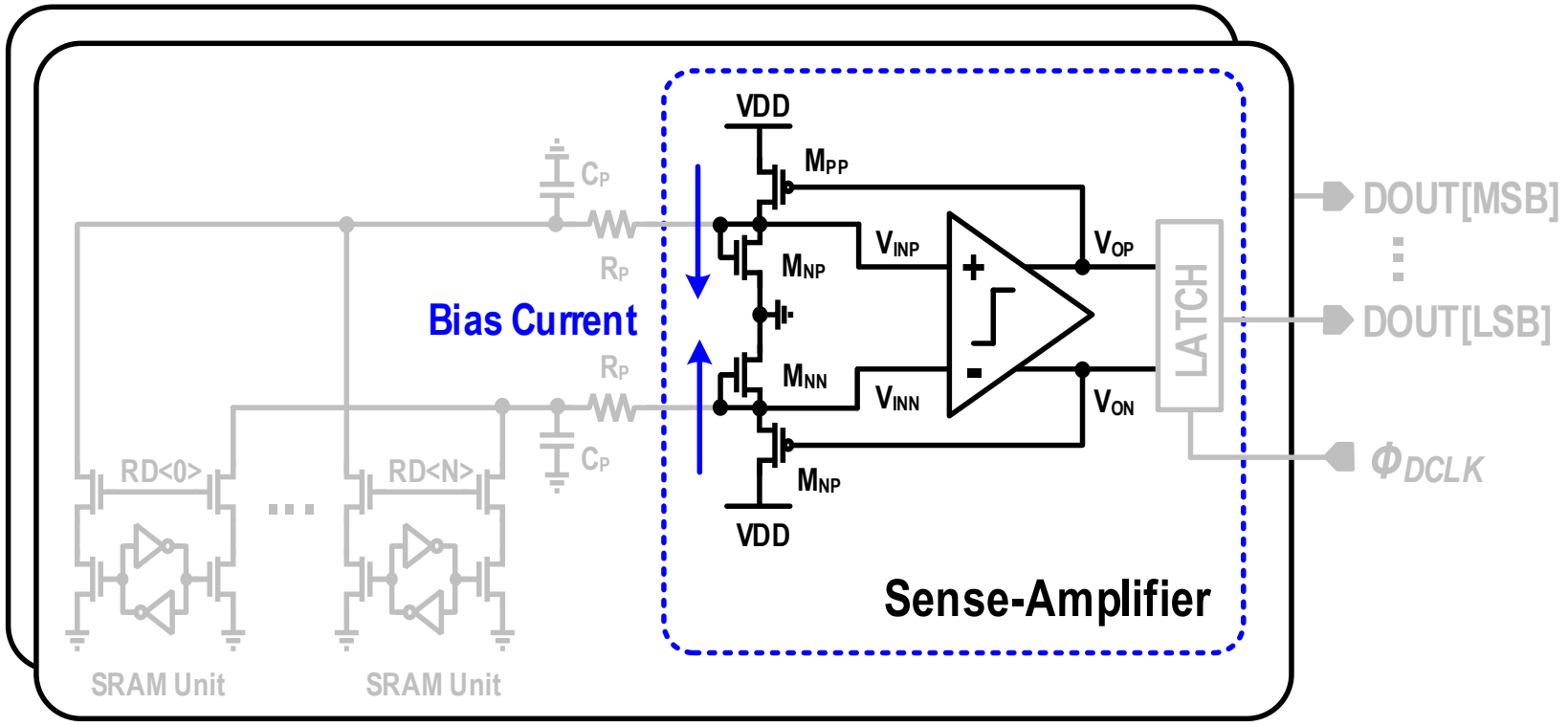
Proposed Serializer (1)

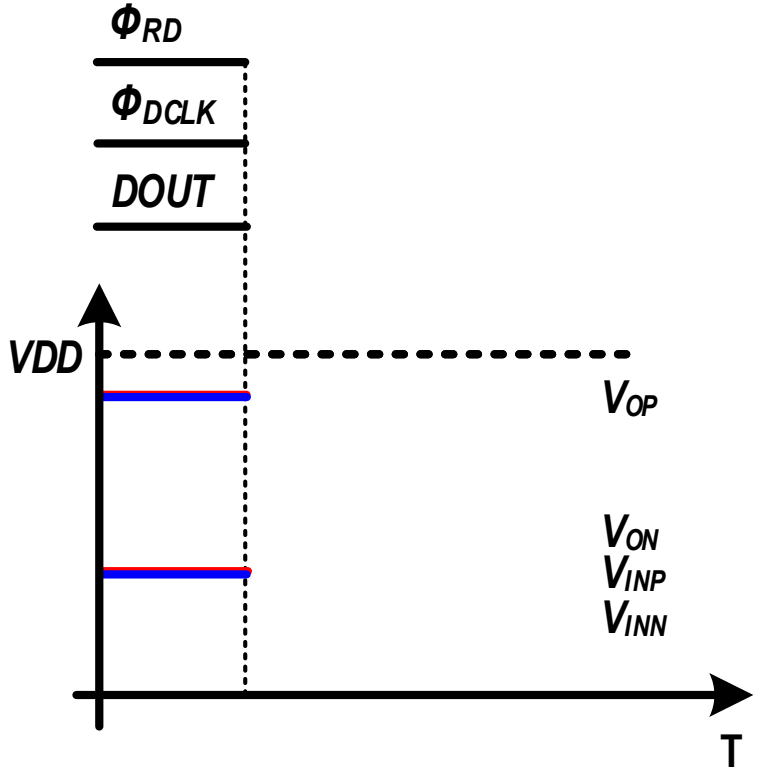


- **Analog-level Serializer**
  - Input Swing Limitation ⇒ Power ↓ ⇒ Only 4.03 mW @ 144 MHz ☺
  - Low Input Impedance ($g_{m,mn}$) ⇒ Speed ↑ ☺

Proposed Serializer (2)

Scheamtic of Analog Sense-Amplifier



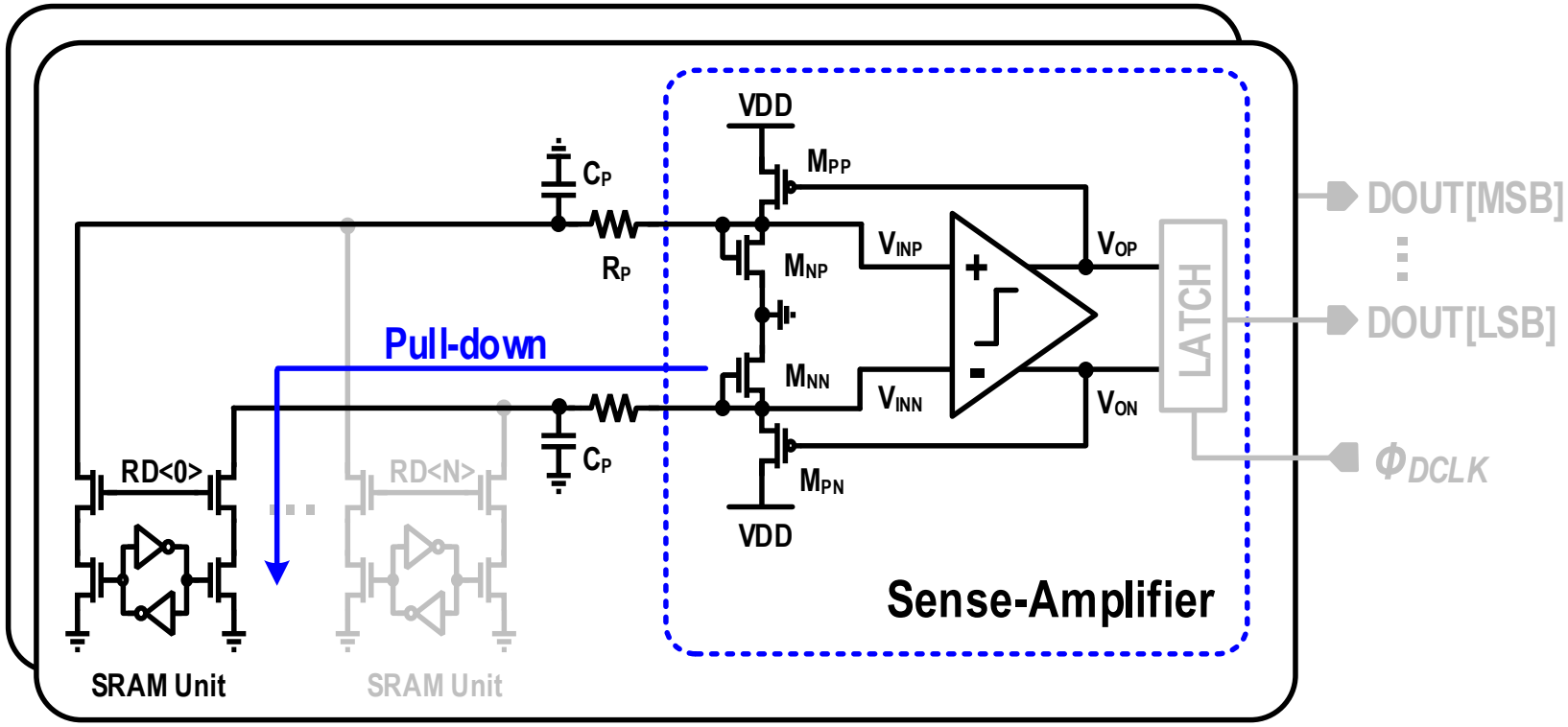


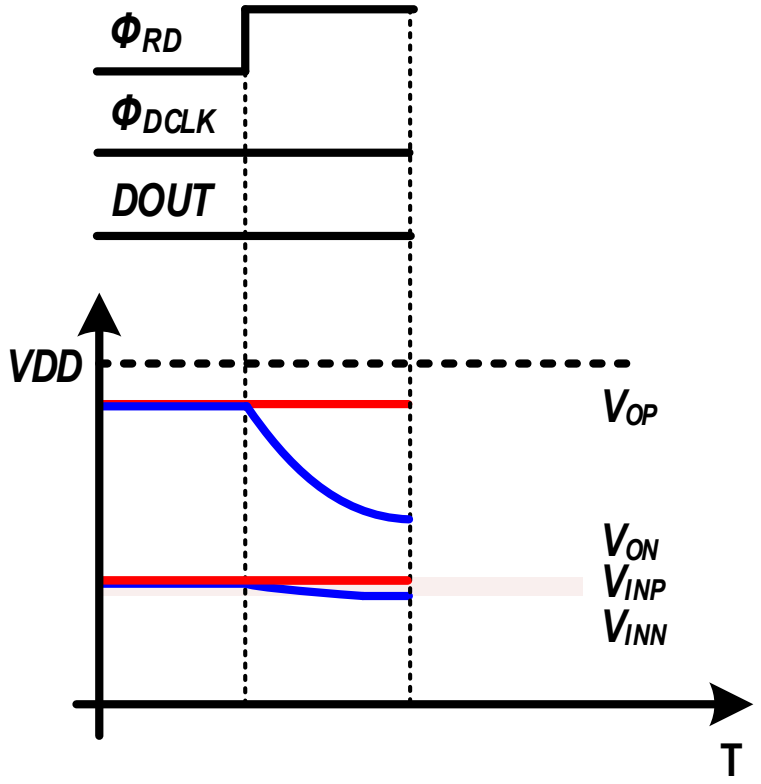
1. Reset Phase

⇒ Initial value of V_{IN} & V_O are determined by the feedback network

Proposed Serializer (3)

Scheamtic of Analog Sense-Amplifier



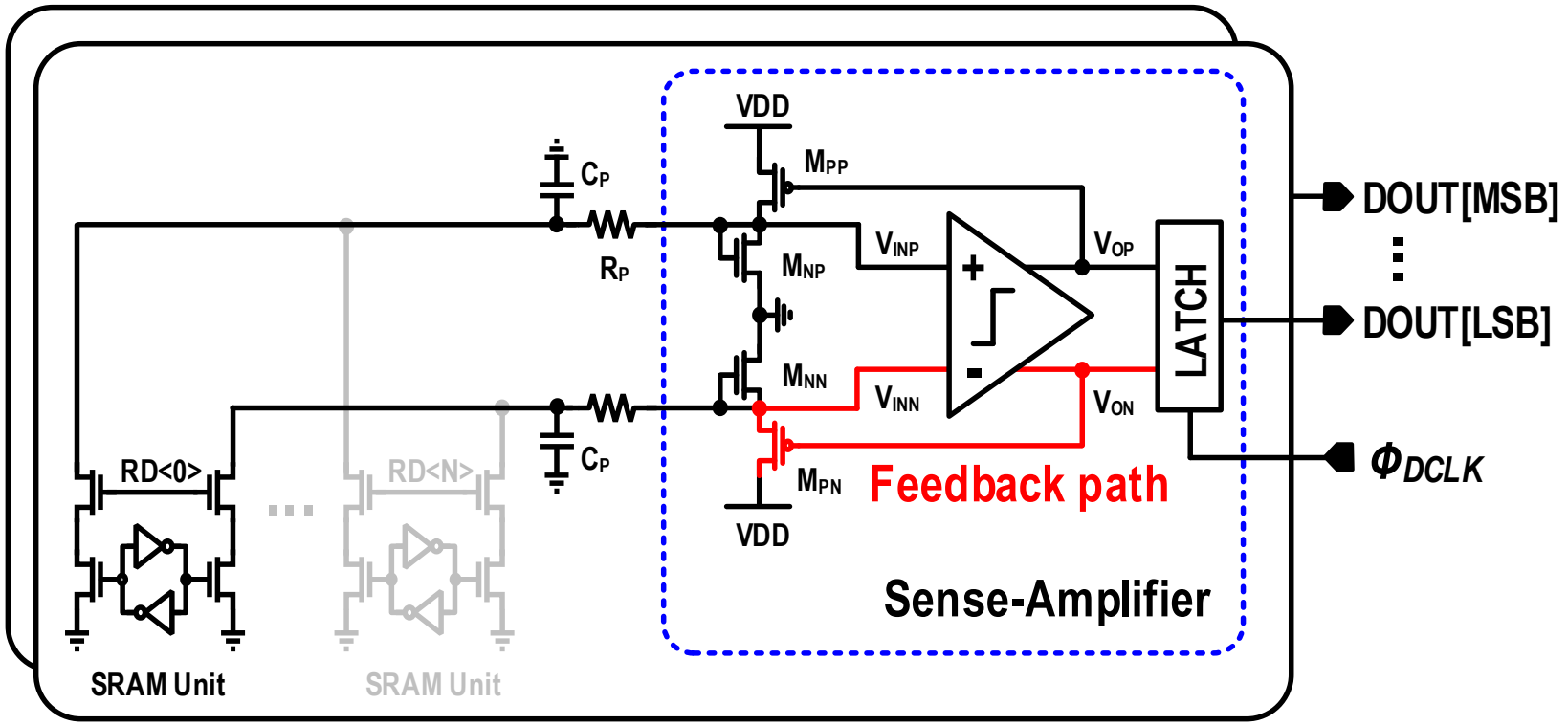


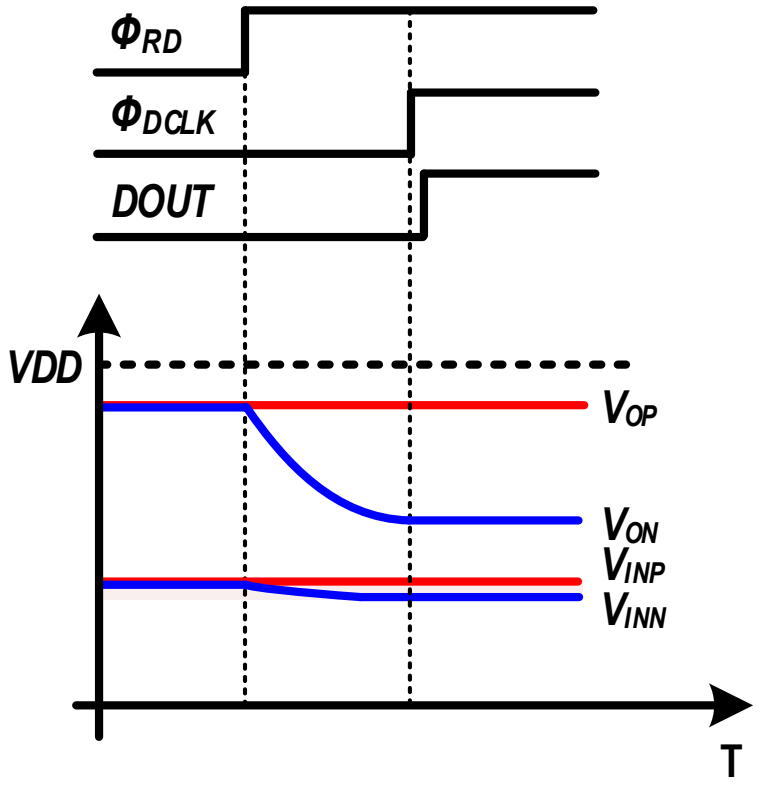
2. Amplification Phase

$\Rightarrow$ Pull-down current makes input voltage difference

Proposed Serializer (4)

Scheamtic of Analog Sense-Amplifier

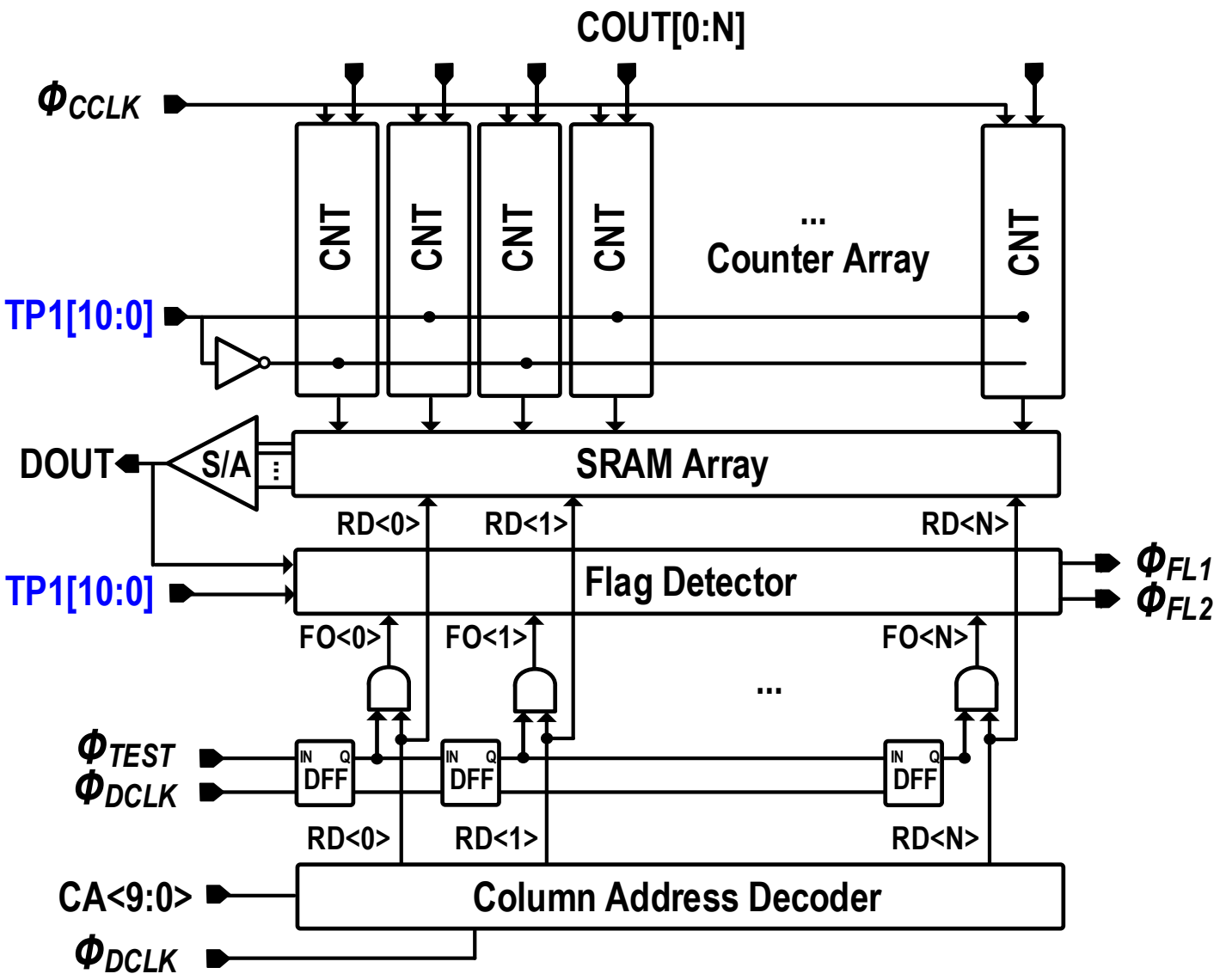




3. Decision Phase

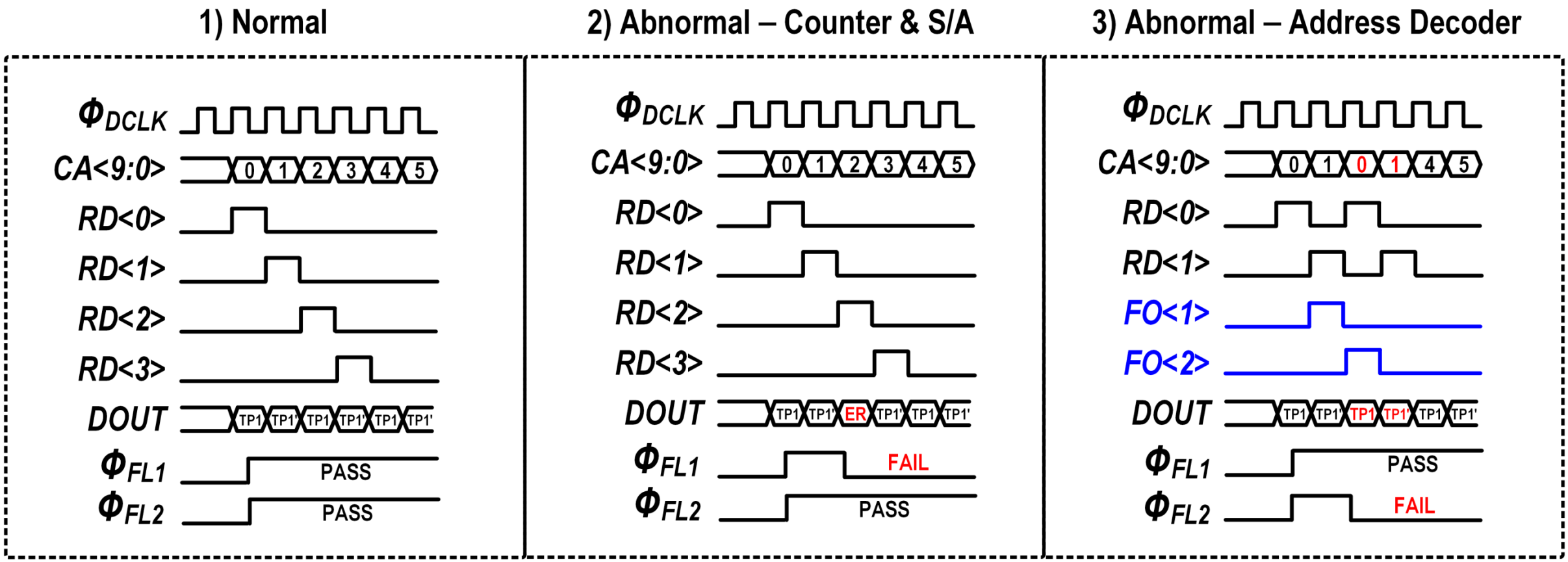
$\Rightarrow$ The $V_{IN,PP}$ is limited by feedback amplifier $\Rightarrow$ Output swing limitation

Proposed BIST Technique (1)



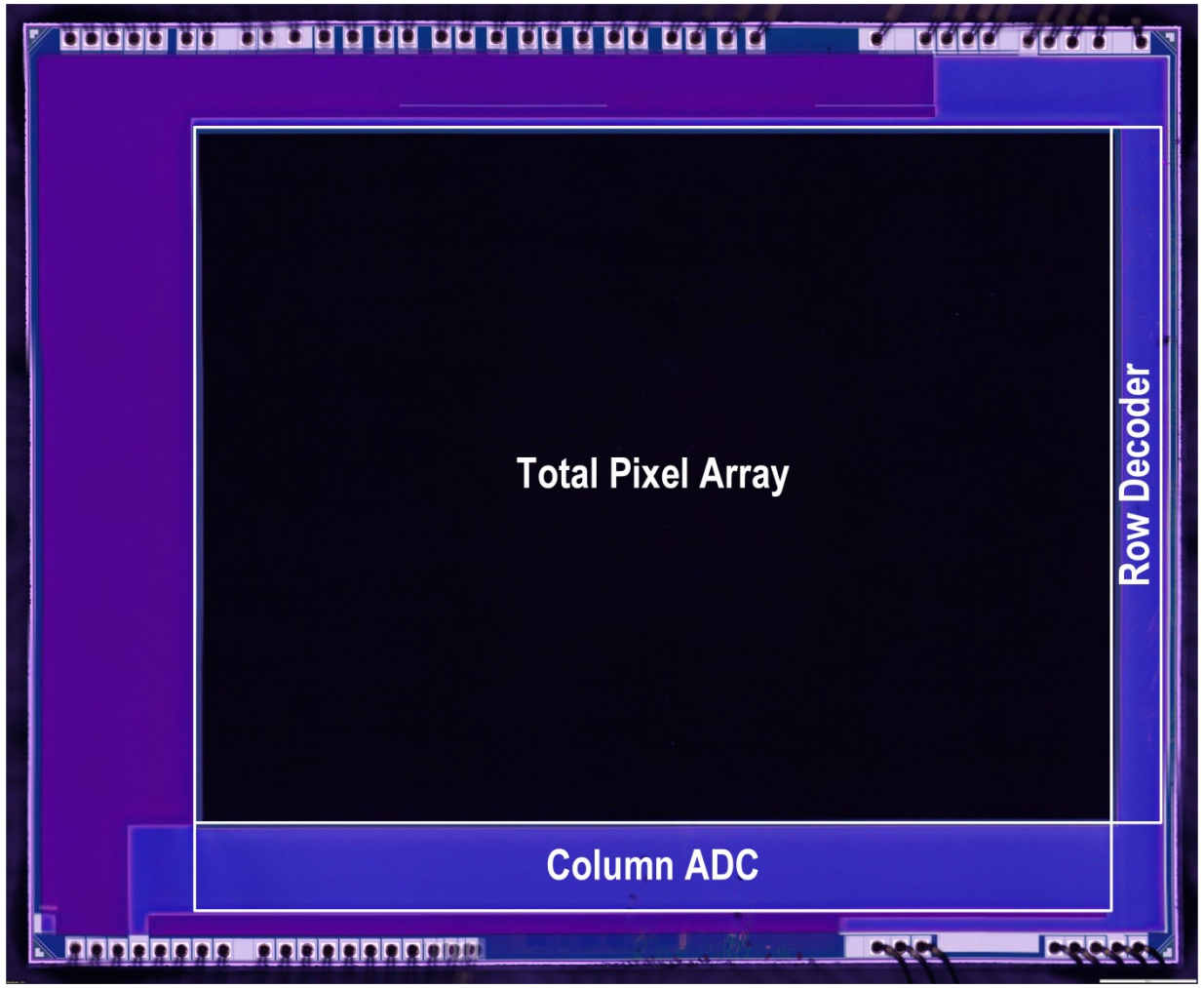
- ① Two test patterns
  - ⇒ TP1 & TP1’
  - ⇒ Test for worst case
- ② Shift register
  - ⇒ For address decoder test
- ③ Flag Detector
  - ⇒ Error Flag

Proposed BIST Technique (2)



- **Two error flags**
  - Error in Data output (FL1) and Memory access signals, RDs (FL2)

Implementation Result

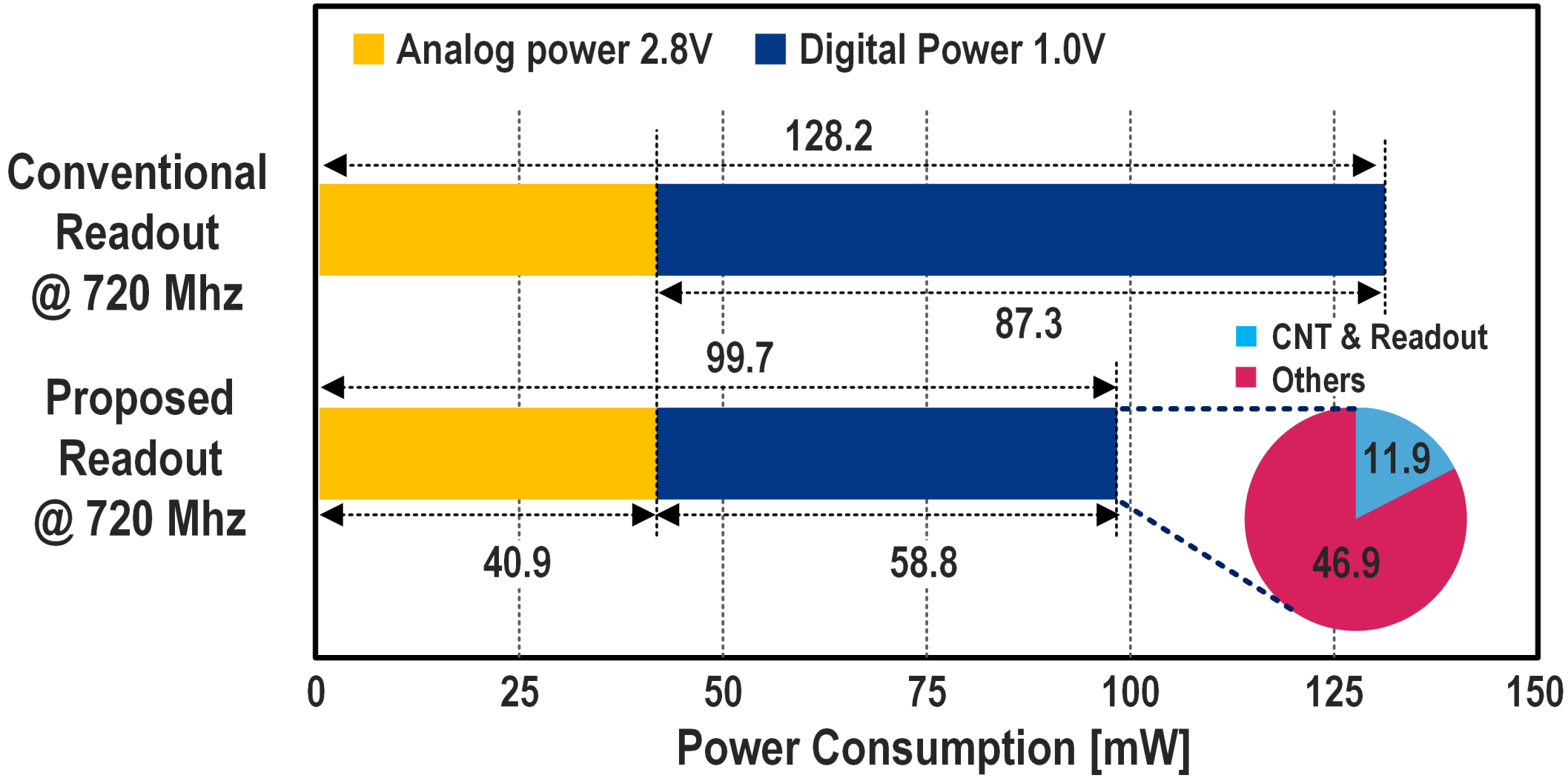


Process	65nm
Pixel Resolution	4240×3216
Pixel Pitch [μm]	1.12
Chip Size [mm²]	29.15
ADC Size [mm²]	2.54
Supply [V]	2.8 / 1
Frame Rate [fps]	30~120
A/D Clock Freq. [MHz]	720
ADC Resolution [Bit]	10
Analog Gain	1 ~ 16

Captured Image

- 30 fps
- 20 lux
- 33 ms exposure
- Macbeth Color Checker Chart

Power Breakdown



Readout power consumption 3.39× ↓ (40.4mW to 11.9mW)

Performance Comparison

Publication	This Work	JSSC'17 [6]
Process (nm)	65	35
Pixel pitch (μm)	1.12	5.86
FWC (e-)	5500	30,450
Conversion Gain (μV/e-)	124	30.4
# of Total Pixels (H×V)	4240×3216	4240×3216
Frame Rate (fps)	30 - 120	480
Power Consumption (mW)	99.7 (30 fps)	5,230 (480 fps)
Dynamic Range (dB)	65.2	76.3
Noise (e^-_{rms})	2	4.6
DNL (LSB)	0.26	-
INL (LSB)	0.18	-
†FoM [e^-·pJ/*DRU]	0.18	0.92

†FoM = (Power × Noise) / (Frame rate × fps × DRU)

††DRU = (FWC / Noise)

Conclusions

- A Low power 13Mp CMOS Image Sensor in 65-nm CMOS
  - **Energy efficient readout structure**
  - High frame rate (**Max 120 fps**) & Low power (**99.7 mW**)
  - State-of-the-art FoM : **0.18 e^{-}·nJ**
  - Built-in self-test for Mass production

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Thank you for your attention!