A 5.8 nW CMOS Wake-Up Timer for Ultra-Low-Power Wireless Applications

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***Abstract*—This work presents an ultra-low-power oscillator designed for wake-up timers in compact wireless sensors. In a conventional relaxation oscillator, a capacitor periodically resets to a fixed voltage using a continuous comparator, thereby generating an output clock. The reset is triggered by a continuous comparator and thus the clock period is dependent on the delay of the continuous comparator which therefore needs to be fast compared to the period, making this approach power hungry. To avoid the power penalty of a fast continuous comparator, a constant charge subtraction scheme is proposed in this paper. As a constant amount of charge is subtracted for each cycle, rather than discharging/charging the capacitor to a fixed voltage, the clock period becomes independent of comparator delay. Therefore, the high power continuous comparator can be replaced with a coarse clocked comparator, facilitating low-power time tracking. For precise wake-up signal generation, an accurate continuous comparator is only enabled for one clock period at the end of the specified wakeup time. A wake-up timer using the proposed scheme is fabricated in a 0.18 µm CMOS process. The timer consumes 5.8 nW at room temperature with temperature stability of 45 ppm/°C (-10 °C to 90 °C) and line sensitivity of 1%/V (1.2 V to 2.2 V).**

***Index Terms*—Low power, relaxation oscillator, subthreshold, timer, wireless sensor node.**

I. Introduction

THERE is a growing interest in the design of compact wireless systems with volumes of 1 cm^3 or less [1]–[3]. Such microsystems could benefit a wide range of application areas, including field of biomedical, military, and environmental investigation. However, the miniaturized size renders power consumption a critical factor in system design due to limited energy storage capacity. To address this issue, the system is often severely duty cycled. Even though the active power of the sensor or radio transmission is large, their average power consumption can be made negligible by having a long idle time between each operation. The idle time or ratio of the duty cycle should be adjustable depending on the target application. A wake-up timer with precise time tracking is useful in that sense as it can be used for scheduling and time-stamping each measurement, as well as synchronizing two different sensor nodes [3]. Since the wake-up timer is one of the few components that must remain on during standby mode, it becomes dominant in determining average power consumption. Therefore, it is vital to reduce wake-up timer power consumption while also maintaining accuracy to ensure proper time keeping.

Quartz crystals are the conventional choice for precision oscillators due to their excellent temperature and frequency stability. Recently, low-power operation of these oscillators has been reported [4], [5]. However, the requirement of an external component limits their usage in very compact wireless systems as they drive up system volume. Alternatively, MEMS-based oscillators have been introduced for integrated silicon-based solution [6], [7]. These works show small form-factor and high accuracy, but high power consumption ($>\mu$W) makes them unsuitable for wake-up timers.

Relaxation oscillators are preferred for their low-power operation and ability to be integrated entirely on-chip. However, they show inferior temperature and voltage insensitivity compared to crystal or MEMS-based oscillators. The basic operation of relaxation oscillators is shown in Fig. 1. A capacitor ($\mathrm{C_{INT}}$) is charged with a current source ($\mathrm{I_{REF}}$) and repeatedly reset. A continuous comparator is used for triggering the reset signal by comparing capacitor voltage ($\mathrm{V_{INT}}$) against a fixed voltage level ($\mathrm{V_{REF}}$). An inverter chain ensures sufficient reset time to fully discharge the capacitor. As this periodic operation continues, a sawtooth waveform and output clock are generated on the capacitor and comparator output, respectively. The output clock period can be expressed as follows:

$$T_{\mathrm{period}} = \frac{\mathrm{C_{INT}} V_{\mathrm{REF}}}{I_{\mathrm{REF}}} + 2t_d \tag{1}$$

where $\mathrm{t_d}$ is comparator and buffer delay. In this scheme, even if the charging time ($\mathrm{C_{INT}\ V_{REF}/I_{REF}}$) is perfectly compensated, temperature/supply dependent comparator and buffer delays ($\mathrm{t_d}$) impact the clock period. A simple way to address this issue is to make the comparator and clock buffer bandwidth high enough, making them negligible relative to the overall period. However, this incurs high power consumption.

Several methods have been introduced to increase tolerance of clock period against temperature and supply voltage variation. In [8] and [9], charging time sensitivity is reduced with a chopping technique to eliminate comparator offset. On the other hand, a replica circuit is used with a feedforward period control to remove comparator and buffer delay from the oscillation period [10]. An inverter-based RC oscillator [11] implements switching-point insensitive oscillation and regulates local supply voltage using a replica inverter. As a result, both charging time and delay are held constant. Also, compensation techniques using an external [12] or on-chip [13] clock reference have been proposed to suppress period

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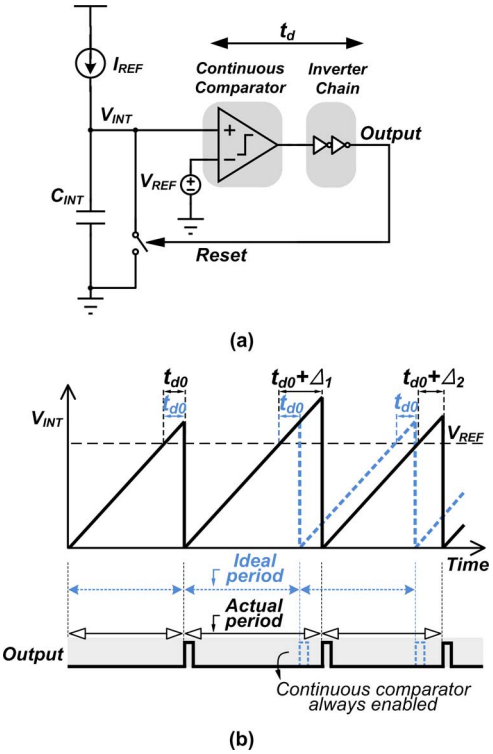


Fig. 1. (a) Basic structure and (b) concept of a conventional relaxation oscillator.

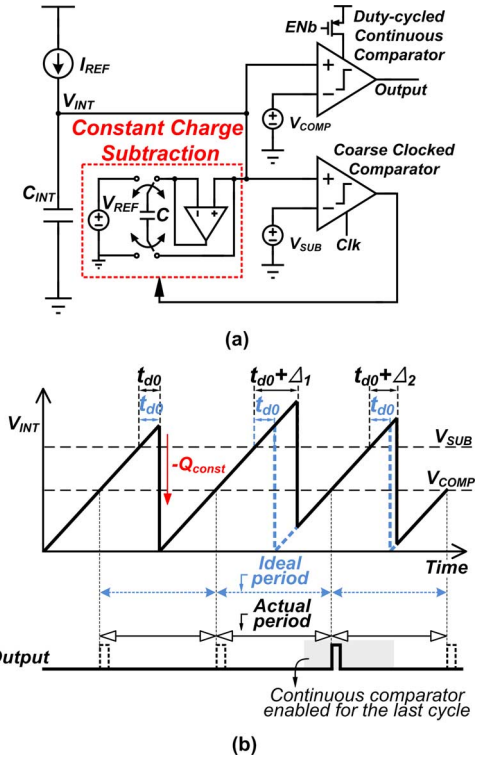


Fig. 2. (a) Basic structure and (b) concept of low-power operation using a constant charge subtraction scheme.

variations. Even though high accuracy (14 to 104 ppm/°C in the kHz range) is achieved with these techniques, their power consumption (120 nW to 4.5 μW) remains high compared to standby power in compact battery-powered systems. Further power reduction can be achieved by slowing the clock frequency, making comparator and buffer delays negligible. A small gate leakage is used as I_{REF} in [14], [15] to reduce clock frequency to Hz range. Alternatively, power consumption in generation of I_{REF} has been minimized with program-and-hold technique [16]. These oscillators consume sub-nW but are highly temperature sensitive ($\geq$ 375 ppm/°C) and offer poor supply stability (>40%/V), which is a critical drawback in battery-powered systems with often poor voltage regulation.

To avoid the fundamental trade-off between temperature-dependent comparator delay and comparator power, we introduce a constant charge subtraction scheme along with low-power time tracking topology that eliminates comparator delay from the clock period.

The remainder of the paper is organized as follows. Section II introduces the proposed low-power topology while Section III presents a detailed circuit description and analysis. Section IV describes measurement results of the test chip. Finally, Section V concludes the work.

II. Proposed Low-Power Topology

Fig. 2 shows a block diagram of the proposed oscillator and its operating concept. Instead of the conventional approach of fully discharging the integrating capacitor (C_{INT}), a constant amount of charge (CV_{REF}) is subtracted from C_{INT} through an amplifier. The power-hungry continuous comparator is replaced with a coarse, asynchronously clocked comparator to detect the subtraction point (V_{SUB}). While the actual subtraction point varies ($t_{d0} + \Delta_i$) due to the asynchronous operation of a clocked comparator, the constant charge subtraction creates a sawtooth waveform that always rejoins the ideal sawtooth waveform. Therefore, the exact subtraction time does not impact the sawtooth waveform and hence the clocked comparator can be slow and inaccurate, allowing its power to be reduced to ~100 pW. The sawtooth waveform period can be expressed as follows:

$$T_{\text{period}} = \frac{Q_{\text{Const}}}{I_{\text{REF}}} = \frac{C}{I_{\text{REF}}}\left(\frac{A}{A+1}V_{\text{REF}}\right) \qquad (2)$$

where A is finite amplifier gain. It can be seen that amplifier gain should be temperature-independent and also large to have temperature-insensitive output period.

While this approach requires an amplifier with high gain for accurate charge subtraction, its power consumption can be made very low since the bandwidth can be relaxed to match the oscillator frequency. The constant charge subtraction itself does not output a constant frequency as the interval between subtraction points is not constant. In order to generate a periodic signal, an auxiliary continuous comparator is required. The continuous comparator necessarily consumes high power to guarantee an ideal period as in the conventional scheme. However, since this work targets a wake-up timer rather than an oscillator, a low jitter high frequency clock is unnecessary. This allows the power hungry continuous comparator to be power-gated the vast majority of the time, which is not possible in conventional architectures since the continuous comparator is directly in the oscillation path. A counter is used to control the power-gate by

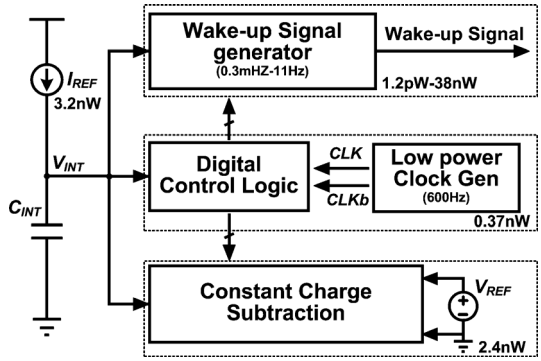


Fig. 3. Overall block diagram of the proposed timer.

tracking the number of subtraction cycles. As a result, the accurate continuous comparator is only triggered for the last cycle in order to generate a precise wake-up signal. With this scheme, an accurate wake-up signal is generated while the oscillator operates at ultra-low-power for all but the final clock period.

The constant charge subtraction scheme can be implemented in different ways, just as there are variants of the relaxation oscillator. The reference voltage, which is used as a threshold for the comparator, can be implemented in two ways; 1) applying a current across a resistor, or 2) directly using a voltage source. When resistor is used, charging time can be made independent of current by mirroring the same current that is used to charge the capacitor. As a result, charging time only depends on resistance and capacitance. Temperature dependence of metal-insulator-metal (MIM) or metal-oxide-metal (MOM) capacitors are negligible, while resistor temperature dependency can be minimized by combining two different types of resistor with opposite temperature coefficients [17]. On the other hand, when a voltage source is used, both voltage and current sources need to be compensated with respect to temperature. Considering that there is only one passive component rather than two active components that need to be temperature compensated, the former approach is preferable. However, the first approach requires a large resistance when targeting power budgets below tens of nW. Even with 100 mV of voltage swing on the capacitor, 100 MΩ is required to reduce the current to 1 nA, which is impractical for on-chip integration. This necessitates the use of both current and voltage sources, which makes the low-power design of a wake-up timer more challenging.

III. Circuit Description and Analysis

Overall block diagram of the proposed timer is shown in Fig. 3. The timer consists of current and voltage references, constant charge subtraction block, wake-up signal generator, digital control logic, and a low-power clock generator. As current reference charges $\mathrm{C_{INT}}$, digital logic observes node $\mathrm{V_{INT}}$ and controls charge subtraction. The digital logic also controls the generation of the wake-up signal, while the low-power clock generator provides clocks for the digital logic.

A. Constant Charge Subtraction

Fig. 4 describes the detailed operation of the constant charge subtraction method. The structure consists of two operational amplifiers (op-amps), namely the subtraction and charging amplifiers, and two capacitors; integration capacitor $(\mathrm{C_{INT}})$ and subtraction capacitor $(\mathrm{C_{SUB}})$. Initially, $\mathrm{C_{INT}}$ is reset to ground with switch configurations $\Phi_{1\mathrm{R}}$ and $\Phi_{2\mathrm{R}}$ rather than adding an additional device. This helps to reduce error arising from subthreshold leakage, which is not negligible in low frequency applications, particularly at high temperatures. For example, a minimum-sized I/O device at 80°C has 420 fA of subthreshold leakage, which leads to 0.51% error in timer period. Following an initial reset, the scheme cycles through two main phases; charge (Φ_1) and subtraction (Φ_2). In Φ_1, $\mathrm{C_{SUB}}$ is connected to a voltage reference $(\mathrm{V_{REF}})$ through the charging amplifier. $\mathrm{C_{SUB}}$ is charged to a fixed voltage $(\mathrm{V_{REF}})$ as the charging amplifier is configured as a unity-gain buffer. At the same time, the subtraction amplifier goes into a sampling phase where offset is stored on $\mathrm{C_{az1}}$ to remove offset and 1/f noise of the amplifier. The integration capacitor $(\mathrm{C_{INT}})$ is disconnected from the subtraction amplifier to reduce leakage. By introducing an additional switch for isolation, the number of off-state switches connected to the integration node $(\mathrm{V_{INT}})$ during Φ_1 is reduced. In a given period, it is preferable to maximize Φ_1 (i.e., minimize Φ_2) to reduce the leakage. However, there is a limit as certain amount of time is required for the subtraction to occur. In this work, Φ_1 has been designed to be 3 times longer than Φ_2. In simulation, this reduces leakage by 2.2× and improves timer error by 0.14%. In simulation, this reduces leakage by 2.2× and improves timer error by 0.14%. As the current source $(\mathrm{I_{REF}})$ charges up $\mathrm{C_{INT}}$, $\mathrm{V_{INT}}$ reaches the subtraction threshold voltage $(\mathrm{V_{SUB}})$, and the next phase (Φ_2) is triggered. During Φ_2, $\mathrm{C_{SUB}}$ is disconnected from the charging amplifier and connected to $\mathrm{C_{INT}}$ through the subtraction amplifier. The amplifier therefore subtracts charge in $\mathrm{C_{SUB}}$ from $\mathrm{C_{INT}}$. Simultaneously, the charging amplifier goes into a sampling phase and offset is stored on $\mathrm{C_{az2}}$ for the next phase. After subtraction, the phase reverts to Φ_1 when $\mathrm{V_{INT}}$ exceeds the reset voltage $(\mathrm{V_{RST}})$. Simultaneously, the voltage on $\mathrm{V_{INT}}$ is stored on $\mathrm{C_{offset}}$ for offset sampling of the subtraction amplifier during Φ_1.

A two-stage topology is used for both charging and subtraction op-amps. The amplifiers are designed to have a dominant pole at the second stage due to ∼ 10 pF of $\mathrm{C_{SUB}}$. Otherwise, a large compensation capacitor would be required, which is not preferable as it degrades amplifier bandwidth to the Hz range. Amplifier tail currents should be designed to meet required slew rates for charging/discharging operation. The subtraction amplifier must have sufficient current to pull down the output node at the beginning of Φ_2 and follow $\mathrm{V_{INT}}$ until the end of Φ_2, while the charging amplifier must be able to pull the discharged $\mathrm{V_{CAP}}$ up to $\mathrm{V_{REF}}$ within Φ_1. The subtraction amplifier tail current is boosted to 5.5 nA during Φ_2 to have fast response time and reduced to 500 pA during Φ_1 to save power. On the other hand, the charging amplifier tail current is fixed at 500 pA since Φ_1 is 3 times longer than Φ_2.

Input- and temperature-dependent amplifier offset and gain can lead to error in the resulting timer period. For the charging amplifier, input-dependent offset is not a concern as it always sees a fixed input voltage. However, due to the asynchronous operation of clocked comparators, the subtraction amplifier sees different values of $\mathrm{V_{INT}}$ at the end of Φ_2. Fig. 5(a) shows the

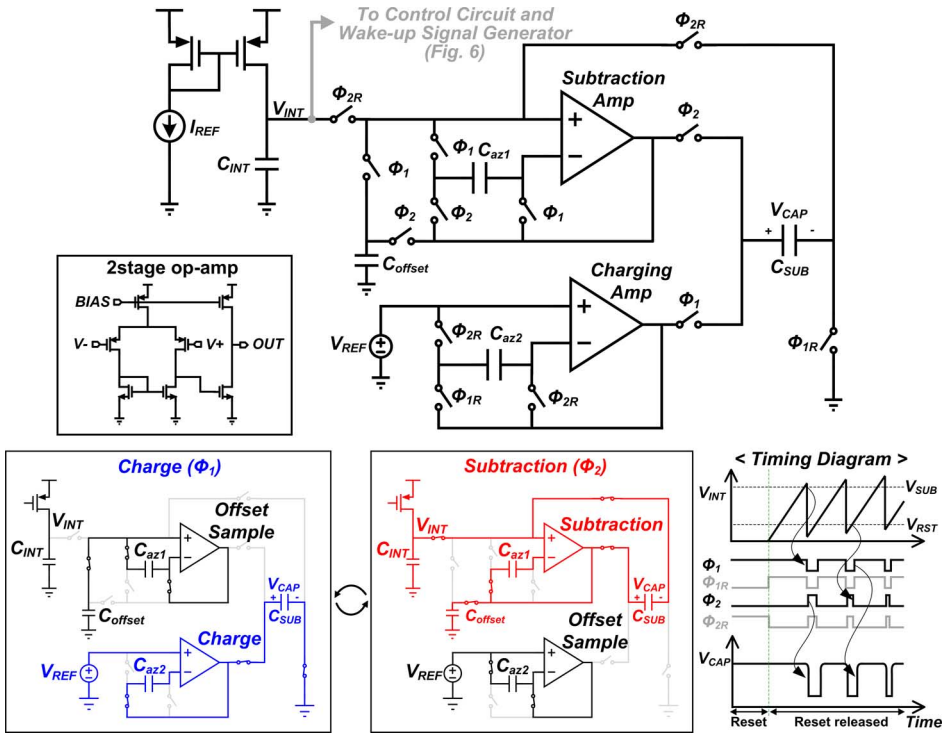


Fig. 4. Detailed structure of proposed constant charge subtraction scheme.

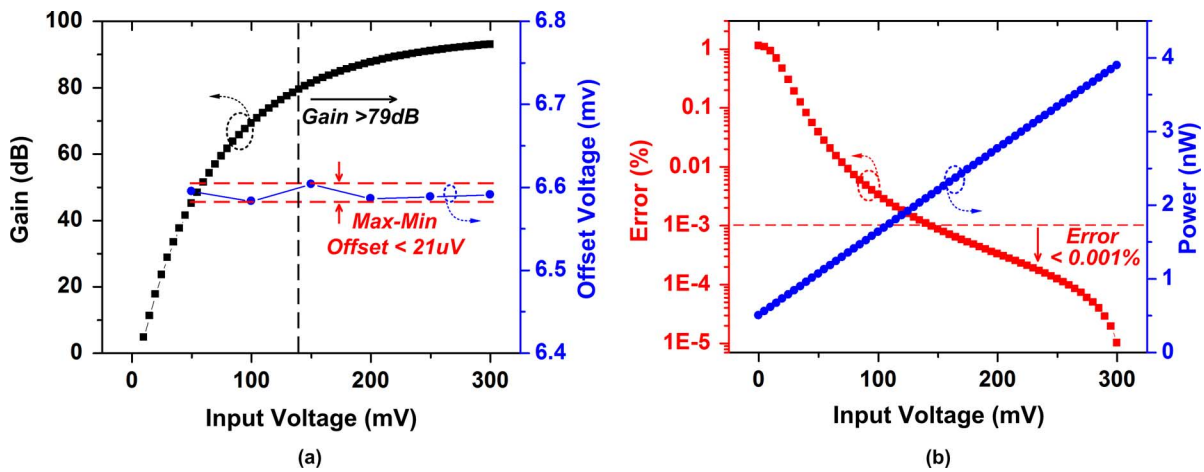


Fig. 5. (a) Simulated offset and gain of subtraction amplifier depending on input voltage and (b) its effect on timer frequency error and power.

dependency of offset and gain on the input level of the subtraction amplifier. It can be seen that while input offset dependency is negligible, the gain increases as the input voltage increases.

Differences in amplifier gain across temperature result in a varying amount of charge being subtracted. Therefore, the absolute value of gain should remain high across the targeted temperature range to minimize error. Simulation results on the frequency error and power consumption depending on input voltage level is shown in Fig. 5(b). The error decreases as input voltage increases, but at the expense of power consumption. Power consumption increases due to a longer subtraction phase (Φ_2). The results show that the subtraction amplifier input voltage should be higher than 140 mV at the end Φ_2 to maintain $<$0.001% error. This implies that there is a minimum frequency constraint for the clocked comparator to suppress the voltage variation. To achieve this, an ultra-low-power oscillator is used and its design and frequency dependency will be discussed in Section III-B. The reset voltage ($\mathrm{V_{RST}}$) that sets the input voltage of end of Φ_2 is designed to be $\sim$175 mV considering the worst case offset coming from the clocked comparator. In the targeted temperature range, both amplifiers are designed for open-loop gain of $>$78 dB with unity-gain bandwidth of 20 kHz.

B. Control Logic

Control logic is used to toggle switches in the charge subtraction scheme as well as to generate the power-gate signal (ENb). Fig. 6 provides a detailed schematic of this control logic. The 4T voltage reference [19] and PMOS diode stack are used to generate two reference voltages, $\mathrm{V_{SUB}}$ and $\mathrm{V_{RST}}$. Generated volt-

ages are then compared against V_{INT} with clocked comparators. Due to the low input range from near-ground to $V_{DD}/2$, the comparator uses a PMOS input stage for proper operation. A single-stage comparator uses a regenerative latch [20] for low-power operation. In order to minimize kickback, two comparators operate with opposite clock phases. The comparators show 3σ offset of 40 mV in simulation which is sufficient to keep the input voltage of the subtraction amplifier $>$140 mV.

The comparator clock is generated with a thyristor-based oscillator [21]. The frequency of the oscillator determines the input voltage difference on the subtraction amplifier between two consecutive cycles. The frequency of the oscillator also determines the voltage deviation of V_{INT} from the V_{SUB} at the subtraction point. The voltage deviation should be low enough to prevent V_{INT} being higher than V_{RST} after subtraction which would stop the oscillation. Maximum voltage difference occurs when the comparison is delayed by the entire comparator clock cycle. For example, a 600 Hz oscillator frequency can result in 10 mV voltage difference in worst case. Higher frequencies guarantee smaller voltage difference, but at the expense of power. Due to its leakage based operation, the oscillator output frequency shows high temperature sensitivity. As shown in Fig. 7, frequency and power increase by 100$\times$ in the targeted temperature range. Therefore, the minimum clock frequency must be set according to the lowest expected operating temperature. This will cause unnecessary power consumption, especially at high temperature.

To avoid undesired power consumption, the oscillator has been current starved with a reference current (described in Section III-D) using a current mirror to tolerate the temperature dependence. Simulation results show that biasing the oscillator with a current reference gives 16$\times$ of power savings at high temperature. Although the oscillator temperature sensitivity is reduced by 2.5$\times$, the oscillator frequency still varies by $\pm$39% across the targeted temperature range. However, overall timer period is not impacted due to the constant charge subtraction scheme. Overall the oscillator consumes 300 pW at an operating frequency of 700 Hz (25 °C).

C. Wake-Up Signal Generator

A 2-stage op-amp serves as an accurate continuous comparator for generating a wake-up signal in the last cycle. The continuous comparator consumes 25 nA (5$\times$ the current of the complete timer during all previous cycles), which leads to a comparator delay that is less than 0.1% of the period across the targeted temperature range. The reference current (I_{REF}) is used to bias the continuous comparator to maintain constant delay over temperature variations. A reconfigurable 16 bit asynchronous counter controls the interval between each wake-up. Since the counter runs at the speed of the subtraction cycles, its power consumption is dominated by leakage rather than dynamic power. In order to minimize leakage current, D-flip-flops are designed with high threshold voltage (HVT) devices. Fig. 8 provides a timing diagram for the generation of a wake-up signal. When reset is released, the counter counts subtraction cycles. When the counter reaches a preset value, which is equal to 8191 ($= 2^{13} - 1$) in this case, power gate (ENb) is released. As a result, the comparator is activated just before wake-up and generates a wake-up signal. The counter operates based on the trigger of reset (IN_2) rather than the trigger of subtraction (IN_1) to prevent false triggering of the continuous comparator during start up. Also, the continuous comparator is disabled after subtraction to prevent output glitching. At the same time, the counter resets to 0 and begins to count again for the next wake-up cycle.

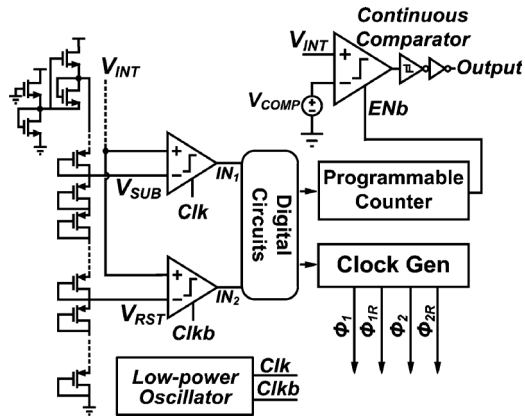


Fig. 6. Detailed schematic of control circuit for generating wake-up signal and clocks.

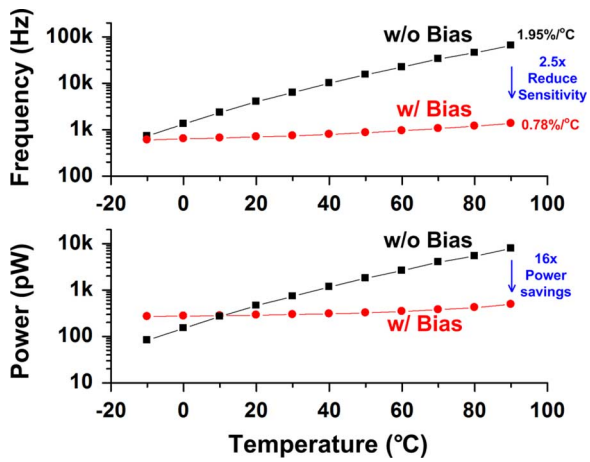


Fig. 7. Simulated frequency and power consumption of thyristor-based oscillator over temperature.

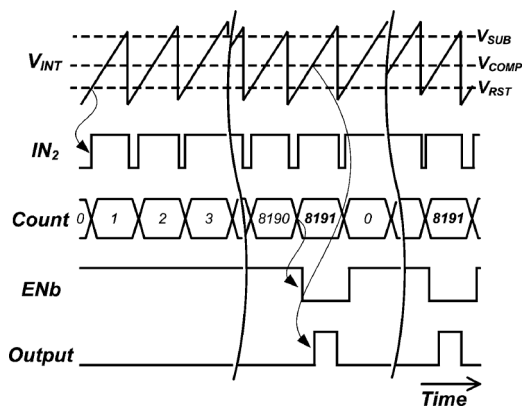


Fig. 8. A timing diagram that shows an example scenario of a wake-up signal generation with 13 bit counter configuration.

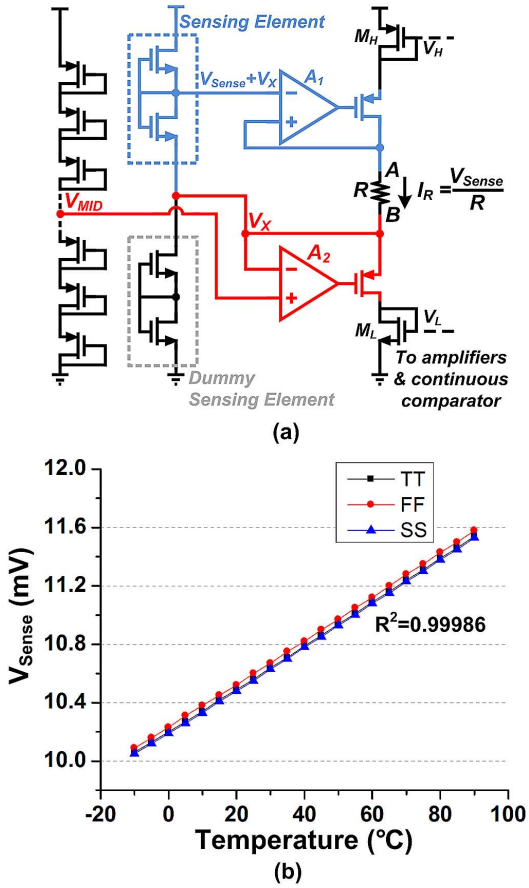


Fig. 9. (a) A reference current (I_{REF}) generator and (b) simulation results of the sensing element across different corners.

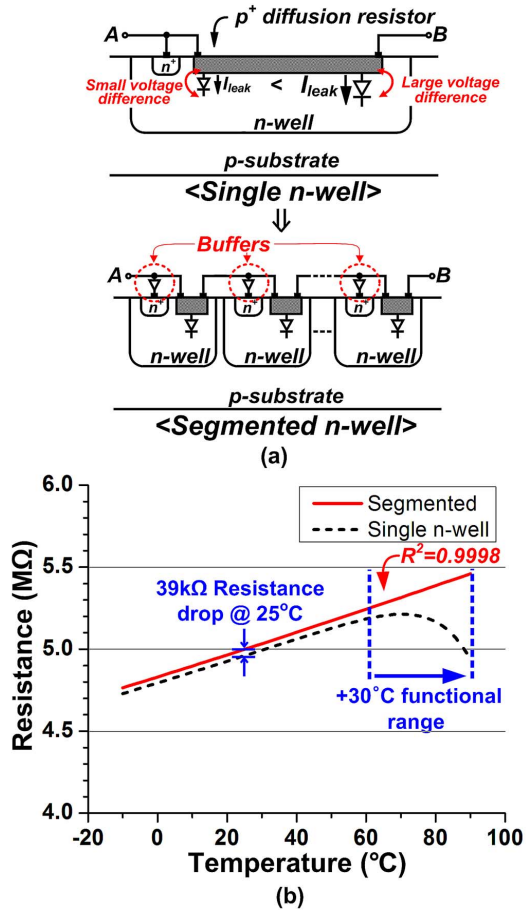


Fig. 10. (a) A segmented self-biased diffusion resistor and (b) its effect at high temperatures.

D. Reference Current and Voltage Generator

The reference current (I_{REF}) is generated with a temperature-to-voltage sensing element (V_{Sense}) along with a voltage to current (V-I) converter and a resistor [22] (Fig. 9(a)). The sensing element consists of two normal NMOS transistors and the output voltage shows a linear proportional to absolute temperature (PTAT) characteristic while consuming 11 pW. Temperature independent current can be generated by applying V_{Sense} across a resistor when the first-order temperature coefficients of the two are matched. Therefore, the sensing element has been sized to match the first-order temperature coefficient of the resistor. The output voltage of the sensing element must be kept $>3-4\ V_T$ to maintain highly linear behavior over temperature [22], generating temperature insensitive currents. In this work, the output voltage has been reduced to 10 mV for low-power operation at the expense of temperature insensitivity (8 ppm/°C of average degradation after 1 k Monte Carlo simulations). A negative feedback loop consisting of an amplifier (A_1) and PMOS transistor ensures that the voltage across the resistor tracks V_{Sense}. The second feedback loop along with the diode stack is used to boost output voltage of the sensing element by V_{MID} ($= V_{DD}/2$) to obtain effective common mode voltage of A_1. This also allows the inclusion of M_L at the bottom of the current generation path, enabling V_L to be directly generated from I_R. A dummy sensing element is added between node V_X and ground to provide a current path for the main sensing element. This helps to suppress undesired current in the main current generation path. The amplifiers use a 2-stage topology and are designed to have >100 dB of open-loop gain over the targeted temperature range while consuming 120 pW (simulated results). The resistor is a 5MΩ p+ diffusion resistor. In the chosen process, diffusion resistors show highly linear behavior against temperature, which enables accurate compensation. However, in low current applications, junction leakage in the resistor degrades linearity at high temperature. As only ~ 2 nA flows through the resistor nominally, the 10×

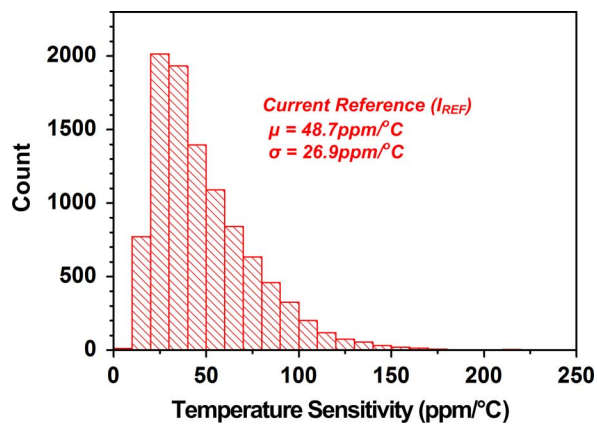


Fig. 11. Monte Carlo simulation results of reference current (I_{REF}).

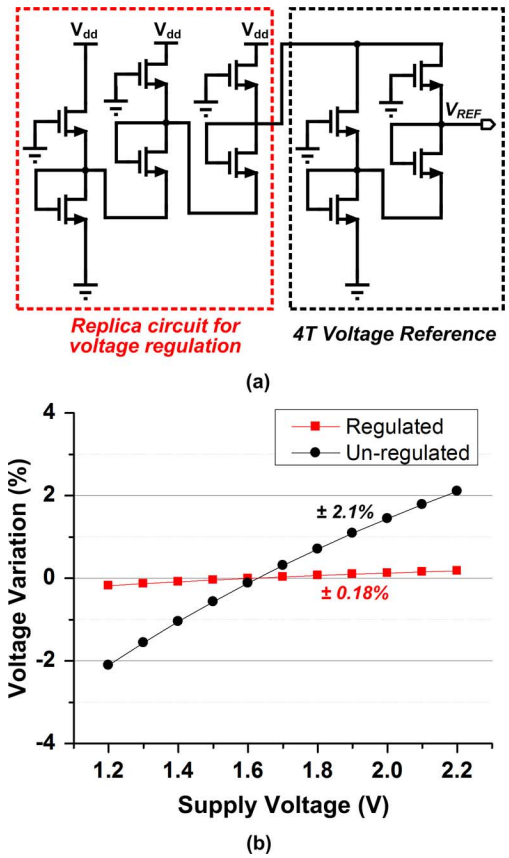


Fig. 12. (a) Voltage reference with locally regulated supply voltage and (b) its simulated line sensitivity.

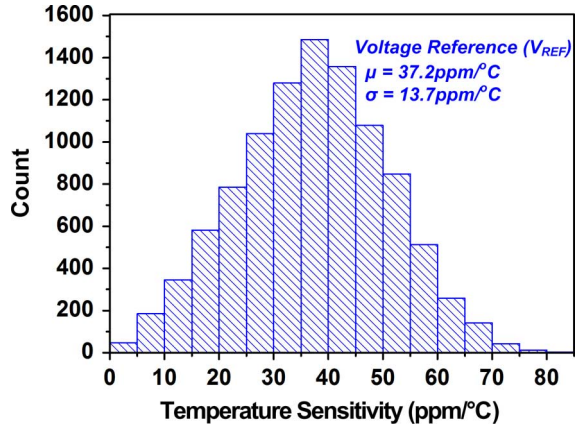


Fig. 13. Effect of process variations and mismatch on the reference voltage (V_{REF}) after 10 k Monte Carlo simulations.

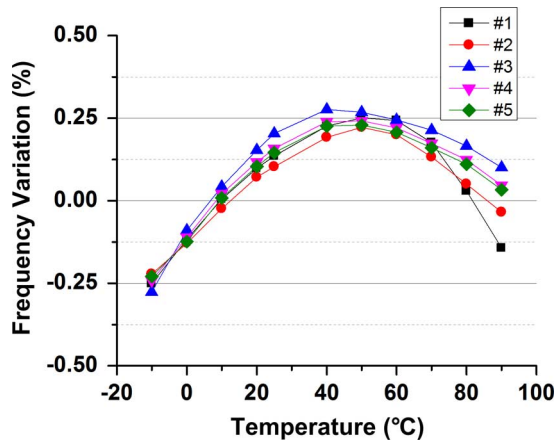


Fig. 14. Measured temperature stability of the timer.

increase in junction leakage from 25°C to 90°C (to 212 pA) causes a non-negligible change in total resistor current.

One way to reduce junction leakage is to minimize the voltage difference across the junction. In previous work, an n+ diffusion resistor is used in which the voltage difference cannot be controlled as it forms a junction with the p-substrate. We therefore use a p + diffusion resistor to segment the resistor into separate n-wells and tie them to intermediate points to minimize the voltage difference. This solves the leakage problem between two regions but raises a similar problem between n-well and p-substrate. Isolation of n-well to p-substrate leakage can be achieved through biasing segmented n-wells through buffers (Fig. 9(b)). Buffers are designed for 1 mV offset (10 k Monte Carlo simulations), limiting frequency error below 0.02%. Through this technique the functional temperature range increases from 0–60°C to 0–90° C at a 6.1% area penalty and 500 pW additional power from the well-biasing buffers (Fig. 10). It can be seen that even at room temperature junction leakages causes the effective resistance to be lower than the designed value. Based on 10 k Monte Carlo simulations, reference current I_{REF} shows an average temperature sensitivity of 48.7 ppm/°C with a standard deviation of 26.9 ppm/°C (Fig. 11).

The temperature-independent voltage source used in this work is shown in Fig. 12(a). Its architecture is based on a 4 T voltage reference [19]. The basic idea of this structure is to use opposite temperature coefficients of the threshold voltage (V_{th}) and the thermal voltage (V_T) to achieve a temperature-insensitive output voltage. In this work, native and I/O NMOS transistors are used to maximize threshold voltage difference. This helps to achieve required output voltage ($\sim$ 550 mV) with minimum number of 2 T voltage reference stacks. A conventional 4 T voltage reference shows $\pm$2.1% of supply voltage sensitivity across 1.2 V to 2.2 V in simulation (Fig. 12(b)). Major source of error is drain induced barrier lowering (DIBL) effect. The supply sensitivity can be improved by taking an advantage of its low-power operation. As only $\sim$ 50 pA is consumed in the voltage reference, a replica circuit can be designed to provide a regulated voltage to the original circuit while consuming only 300 pW. When a sufficient amount of current is supplied, there is negligible effect on the temperature characteristics. Line sensitivity improves by 11.7$\times$ after regulating the local supply voltage in this way. Fig. 13 shows the effect of process and mismatch on the temperature characteristics of the voltage reference. Based on 10 k Monte Carlo simulations, the average temperature coefficient is 37.2 ppm/°C with standard deviation of 13.7 ppm/° C.

IV. Measurement Results

The proposed wake-up timer is implemented in 0.18 μ m CMOS. Fig. 14 shows measured stability results across temperature. Operating at 11 Hz, measured temperature sensitivity is

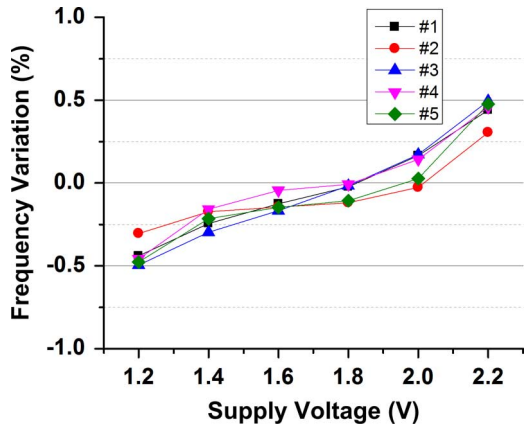


Fig. 15. Measured line stability of the timer.

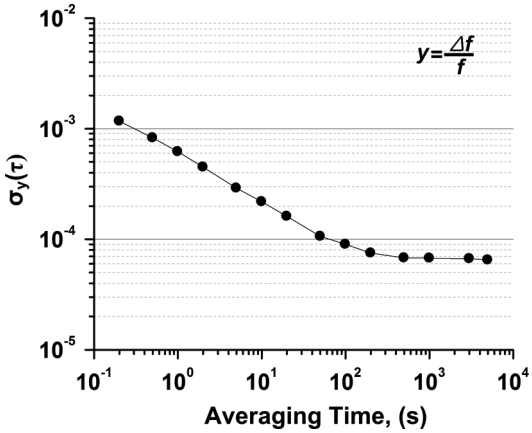


Fig. 16. Measured Allan Deviation of the timer.

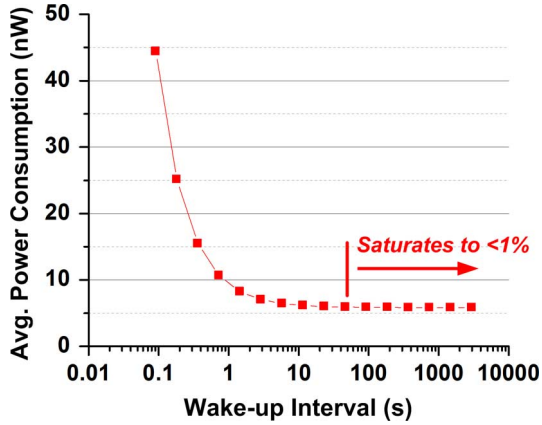


Fig. 17. Measured average power consumption with different wake-up intervals.

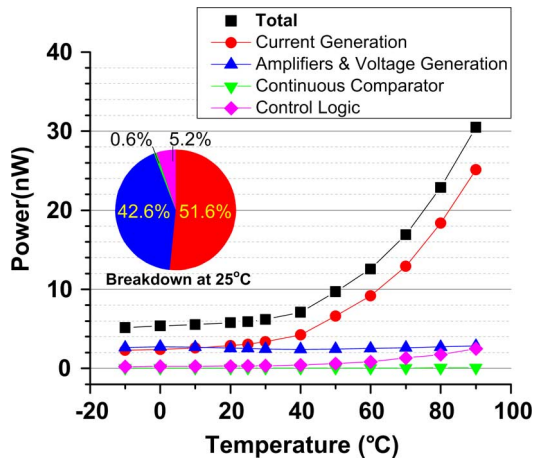


Fig. 18. Breakdown of average power consumption across temperature.

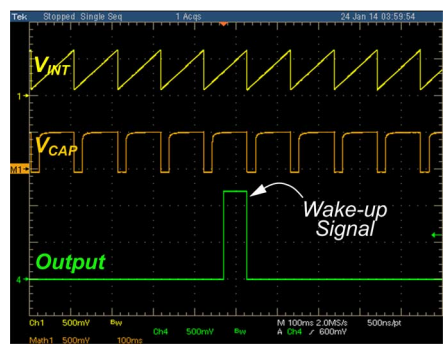
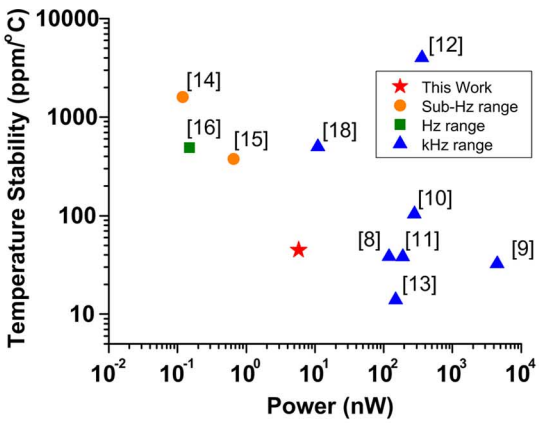


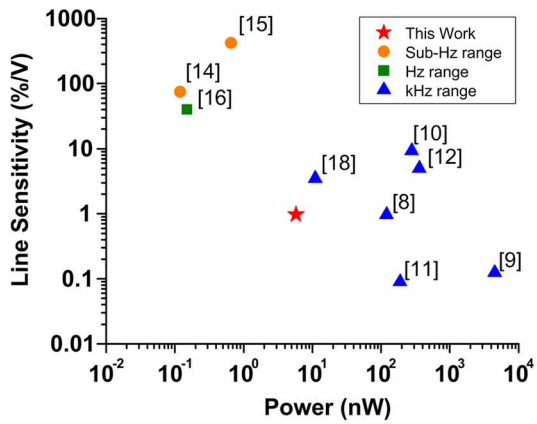
Fig. 19. Measured waveform of V_{INT}, V_{CAP} and Output signal.

45 ppm/° C from −10 to 90°C (48 ppm/°C average across the 5 dies). Fig. 15 shows the supply sensitivity of the output frequency from 1.2 V to 2.2 V. The variation is less than 1%/V. The sensing element in the reference current generator is the major source of error. Measured Allan deviation [23] demonstrates long-term stability (Fig. 16). As averaging time increases, frequency fluctuations decrease as white noise is averaged out until flicker noise dominates and timer performance saturates ($\sim$ 10 mins).

Average power consumption of the timer strongly depends on the wake-up interval of the accurate continuous comparator. Fig. 17 shows measured average power as a function of wake-up interval. As wake-up interval increases, average power consumption decreases rapidly. Even for wakeup intervals of just 1 s, average power remains below 10 nW and saturates within 1% of 5.8 nW after 50 sec. Fig. 18 provides a breakdown of power consumption across the measured temperature range (1.2 V supply, 12 minute wake-up signals). Due to the proposed approach, the continuous comparator power is a negligible portion of total average power consumption ($<$1%). Amplifiers and the continuous comparator show only a small increase in power with temperature due to the current reference (I_{REF}) biasing, while the reference current generator dominates power at high temperatures due to constant voltage biasing of amplifiers. Fig. 19 shows measured waveforms of V_{INT}, V_{CAP}, and timer output signal with a 10 bit counter configuration. It can be seen that subtraction and charging operation is well-performed without any stabilization issue. The die photo of the test chip is shown in Fig. 20 with an active area of 0.24 mm^2. Table I compares state-of-art low-power on-chip oscillators ($\leq$ kHz range, $<$10 μ W). The proposed timer occupies a portion of the design space that had not been previously reported. It can be seen that the timer achieves comparable temperature and voltage insensitivity to timers in the 100 nW range while consuming sub-10 nW.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH RECENTLY PUBLISHED LOW POWER TIMERS





	This Work	[14]	[15]	[16]	[18]	[8]	[13]	[11]	[10]	[12]	[9]
Technology	**0.18µm**	0.13µm	0.13µm	0.13µm	0.35µm	65nm	0.13µm	65nm	90nm	0.18µm	60nm
Area	**0.24mm²**	0.0005mm²	0.015mm²	0.02mm²	0.1mm²	0.032mm²	0.25mm²	0.015mm²	0.12mm²	0.016mm²	0.048mm²
Frequency	**11Hz**	0.08Hz	0.37Hz	11Hz	3.3kHz	18.5kHz	100kHz	33kHz	100kHz	31.25kHz	32.8kHz
Temperature Range	**-10-90°C**	0-80°C	-20-60°C	0-90°C	-20-80°C	-40-90°C	20-70°C	-20-90°C	-40-90°C	-45-80°C	-20-100°C
Temperature Coefficient	**45ppm/°C**	1600ppm/°C	375ppm/°C[1] (31ppm/°C[2])	490ppm/°C	<500ppm/°C	38.5ppm/°C	14ppm/°C	38.2ppm/°C	104ppm/°C	4000ppm/°C	32.4ppm/°C
Line Sensitivity	**1%/V @1.2-2.2V**	75%/V @0.4-0.5V	490%/V @1.15-1.25V 420%/V @0.65-0.75V	40%/V @0.55-0.6V	3.5%/V @1-2.5V	1%/V @1.5-3.3V	N/A	0.09%/V @1.15-1.45V	9.3%/V @0.725-0.9V	5%/V @N/A	0.125%/V @1.6-3.2V
Power Consumption	**5.8nW**	0.12nW	0.66nW[1] (N/A[2])	0.15nW	11nW	120nW	150nW	190nW	280nW	360nW	4.48µW

[1]Without a temperature sensor.
[2]With 10 point calibration using a temperature sensor. Power number with the sensor not available.

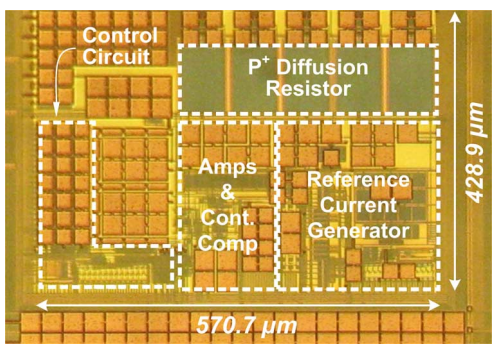


Fig. 20. Microphotograph of the test chip in 0.18 μ m CMOS.

V. CONCLUSION

This work describes a wake-up timer that can be used in compact wireless sensors. A low-power topology using a constant charge subtraction scheme is proposed. To avoid using a very large resistance, the proposed architecture uses voltage and current references in the architecture. Two op-amps act to repeatedly subtract a constant amount of charge. Since the generated sawtooth waveform is independent of subtraction time, a low-power clocked comparator is used for triggering the subtraction. The final precise wake-up signal is generated by triggering a higher power accurate continuous comparator. The proposed topology separates the continuous comparator from the oscillation path and activates it only for short period when it is required. As a result, both low-power tracking and generation of precise wake-up signal is made possible. The timer consumes 5.8 nW at room temperature from a 1.2 V supply voltage. Temperature sensitivity of 45 ppm/°C from −10 to 90°C and supply sensitivity of 1%/V from 1.2 V to 2.2 V is achieved.

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