# Circuit Techniques for Efficient Implementation of Memristor Based Reservoir Computing

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IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS

# Overview

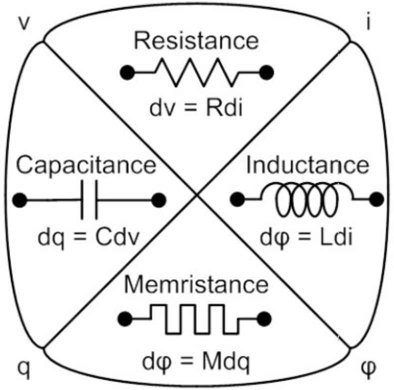
- Introduction
- Bi-Memristor Synapse
- Memristor based Reservoir Computing
- mrDANNA Architecture for Reservoir Implementation
- Memristive Crossbar with STDP Learning for Readout Layer
- Simulation Results
- Summary

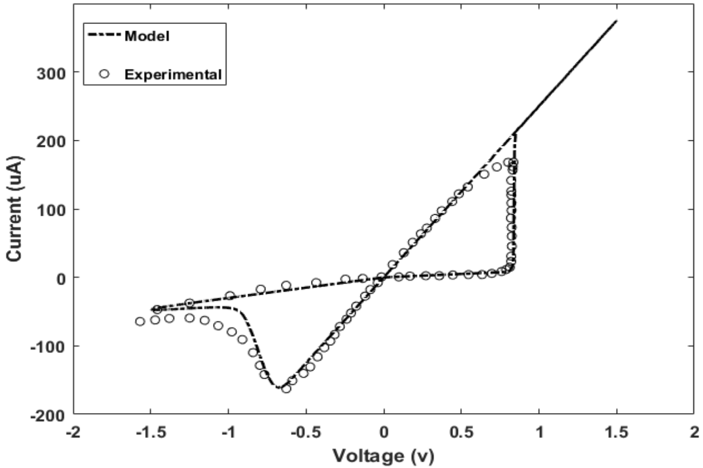
# Neuromorphic Systems

- Saturation of Moore's law for miniaturization
- von Neumann architecture facing the "wall":
  - Data Latency
  - High Power
- Neuromorphic Computing:
  - Paradigm shift in computing
  - Brain-inspired systems
  - High speed and low processing power
- Neuromorphic Components:
  - Neurons: CMOS circuits based
  - Synapses:
    - CMOS based: capacitive, resistive, RAM based
    - Emerging devices: Phase change memory, Spintronic devices, Memristors

# Memristor Overview

- Short form for “memory resistor”
- Named the “missing” circuit element by Chua in 1971[1]
- Physically demonstrated by HP in 2008
- I-V hysteresis

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1. L. Chua, “Memristor-the missing circuit element,” IEEE Transactions on circuit theory, vol. 18, no. 5, pp. 507–519, 1971.
2. Sayyaparaju, S. Amer, and G. S. Rose, “A bi-memristor synapse with spike-timing-dependent plasticity for on-chip learning in memristive neuromorphic systems,” in 2018 19th International Symposium on Quality Electronic Design (ISQED). IEEE, 2018, pp. 69–74.

# Bi-Memristor Synapse

- Two-memristors between a pre- and post-neuron
- Neurons' switches' positions change
- When post-neuron accumulates,

$$i = i_{M_p} - i_{M_n} = (G_p - G_n) V_{spike}$$

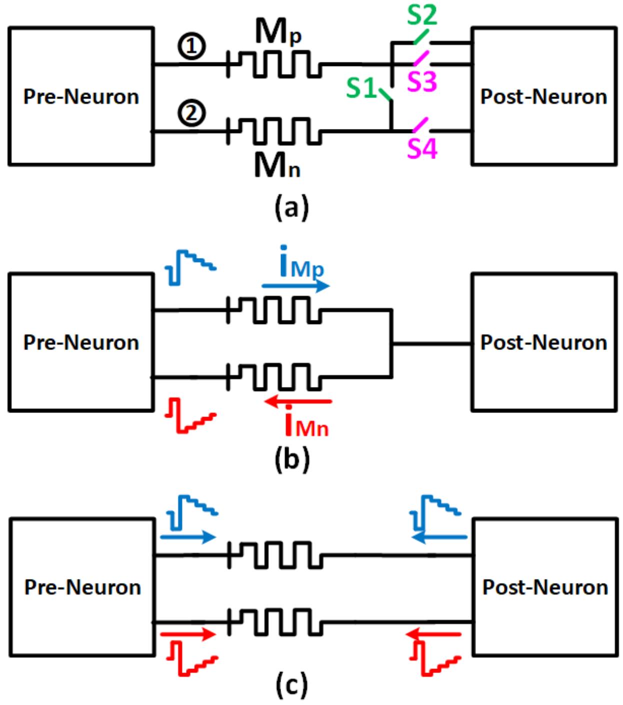
$$G_{eff} = G_p - G_n = \frac{1}{M_p} - \frac{1}{M_n}$$

- $M_p < M_n$ => positive weight and vice-versa

Schematic

Accumulation

Learning

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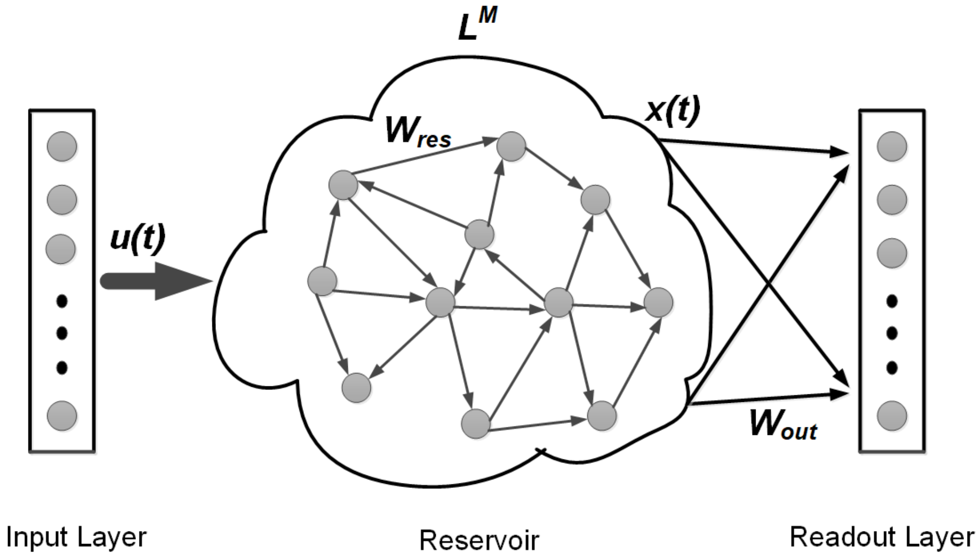
# Reservoir Computing

- A form of recurrent neural networks (RNNs)
- RNNs are tough to train: computational cost and slow convergence
- Reservoir Computing (RC) gets rid of training cost
- Contains 3 layers: input, reservoir and readout
- Only readout layer weights are trained
- Input and reservoir weights remain unchanged

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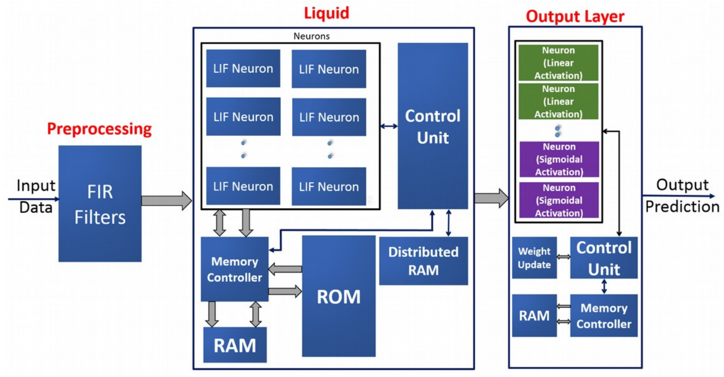
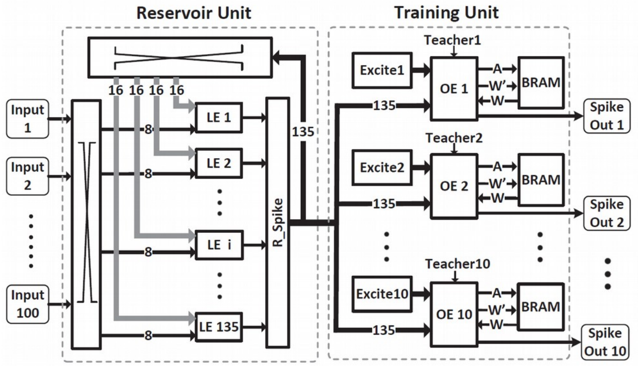
# Physical Reservoir Computing

- Two variants: echo state networks (ESNs) and liquid state machines (LSMs)
- ESNs use artificial neurons, LSMs use spiking neurons and are bio-inspired
- Prior work on Physical RC:




[1]



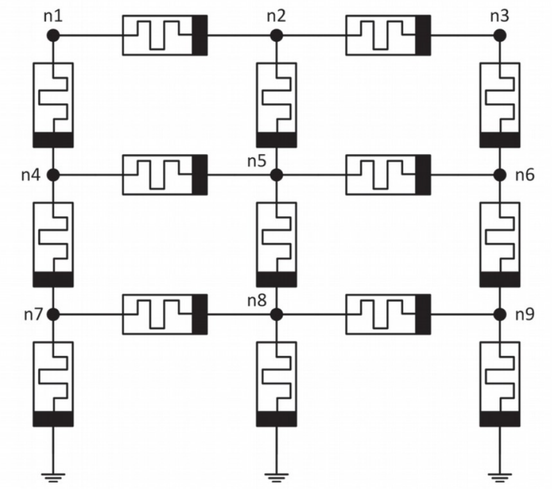

[2]

Digital implementations of RC.
Huge area overhead for weights and learning circuits

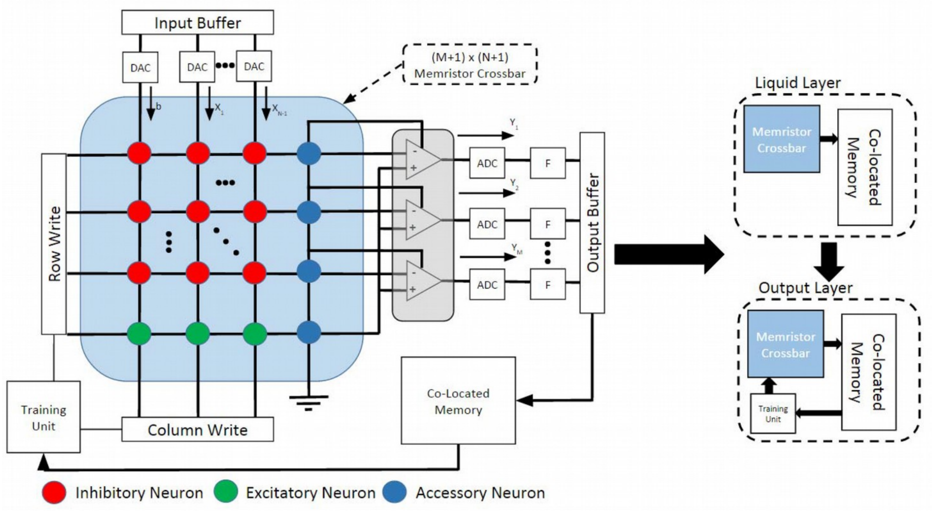

1. A. Polepalli, N. Soures, and D. Kudithipudi, "Reconfigurable digital design of a liquid state machine for spatio-temporal data," in Proceedings of the 3rd ACM International Conference on Nanoscale Computing and Communication. ACM, 2016, p. 15.
2. Q. Wang, Y. Li, and P. Li, "Liquid state machine based pattern recognition on fpga with firing-activity dependent power gating and approximate computing," in 2016 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2016, pp. 361–364

# Memristor-Based Reservoir Computing

- Prior work on memristor-based RC:




Mesh based structure.[1]
Not a neural network




LSM implemented with crossbar.[2]
Has “heavy” circuits for implementation and learning.

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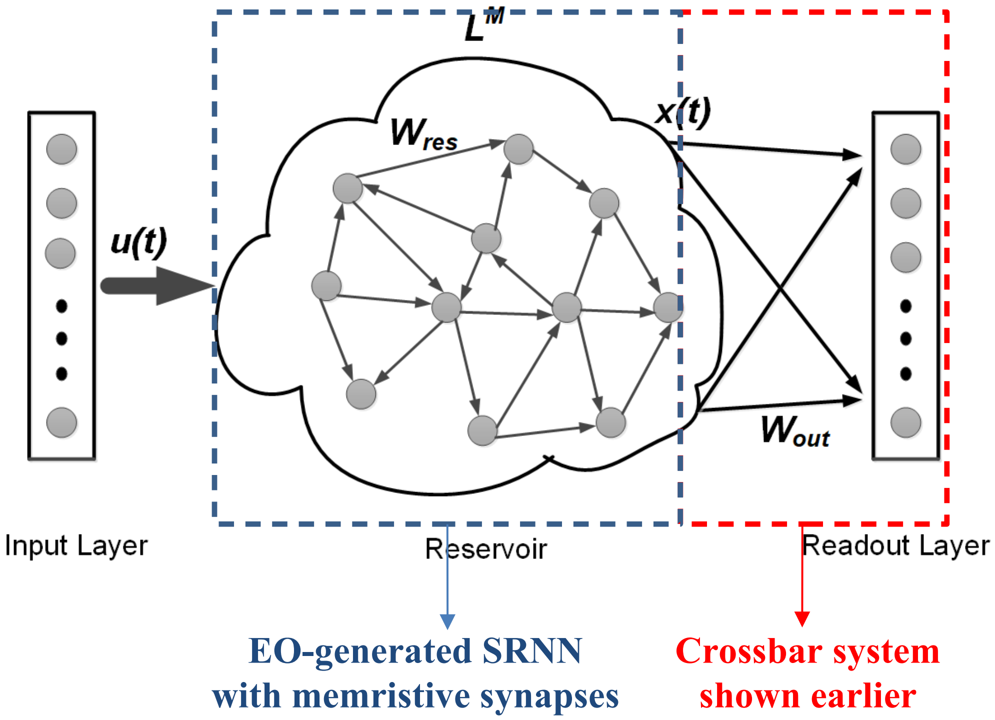
1. N. Soures, L. Hays, and D. Kudithipudi, “Robustness of a memristor based liquid state machine,” in 2017 international joint conference on neural networks (ijcnn). IEEE, 2017, pp. 2414–2420.
2. J. B¨urger and C. Teuscher, “Variation-tolerant computing with memristive reservoirs,” in Proceedings of the 2013 IEEE/ACM International Symposium on Nanoscale Architectures. IEEE Press, 2013,pp. 1–6.

# Proposed Memristor-Based RC

- Proposed system is an LSM
- Contains bi-memristor synapse and CMOS spiking neurons in reservoir
- Reservoir is a Spiking RNN (SRNN)
- Optimal reservoir for a given task generated through evolutionary optimization (EO)
- Readout layer implemented with crossbar presented earlier.
- Readout layer learning is through supervised STDP

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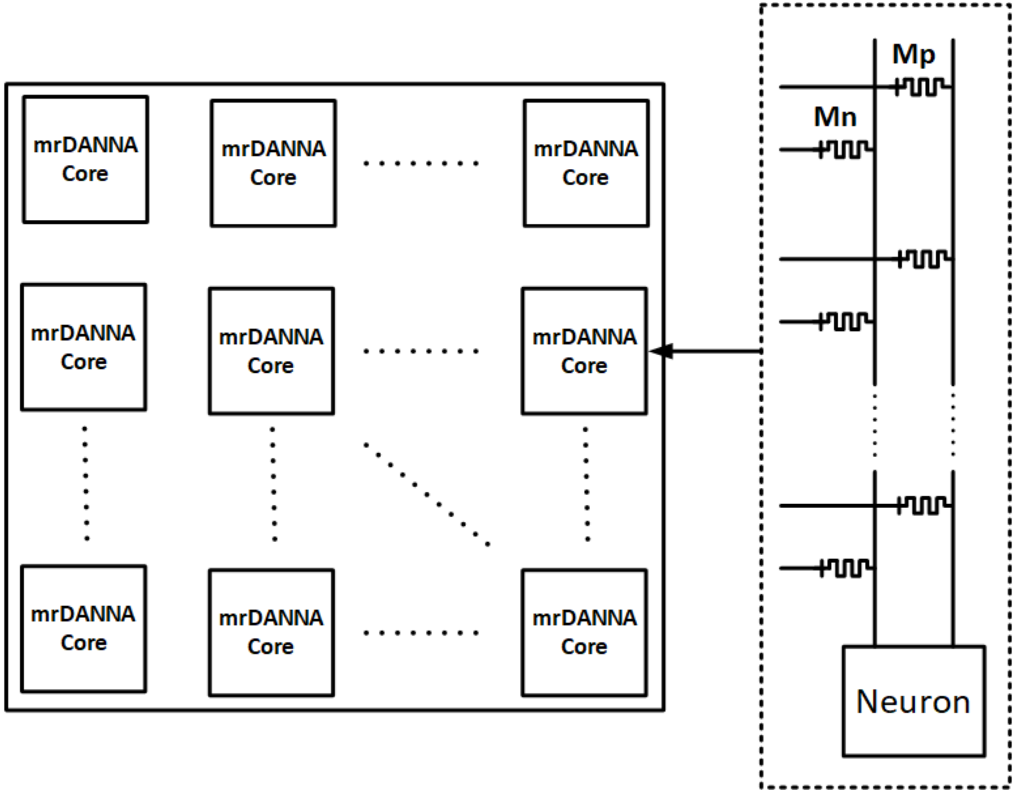
# RC Implementation – Reservoir

- Memristive Dynamic Adaptive Neural Network Array – mrDANNA
- Contains mrDANNA ‘cores’
- Each core has 1 neuron + some synapses
- Cores connected to form network
- Can implement a given network topology

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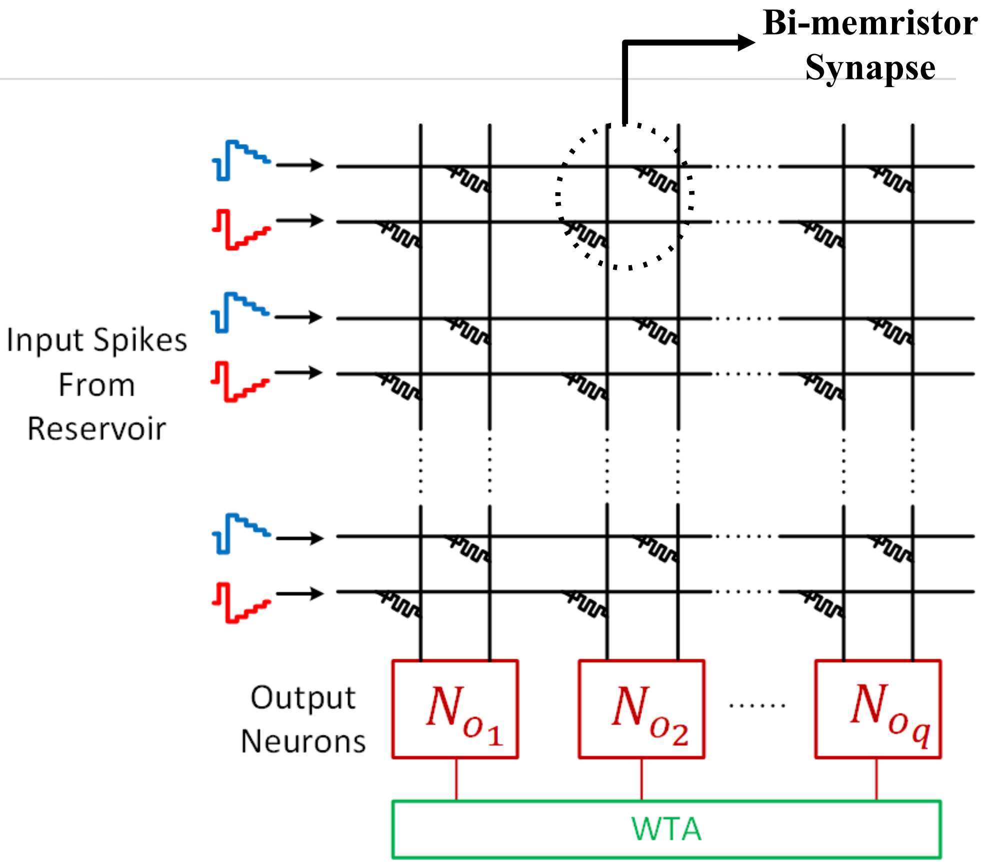
# Readout Layer

- Crossbar architecture for readout layer
- Two layers of neurons: input and output
- Input spikes lead to currents in synapse columns
- Leads to accumulation in output neurons
- “Winner takes all (WTA)” to decide the output neuron with highest accumulation
- Supervised STDP approach for learning

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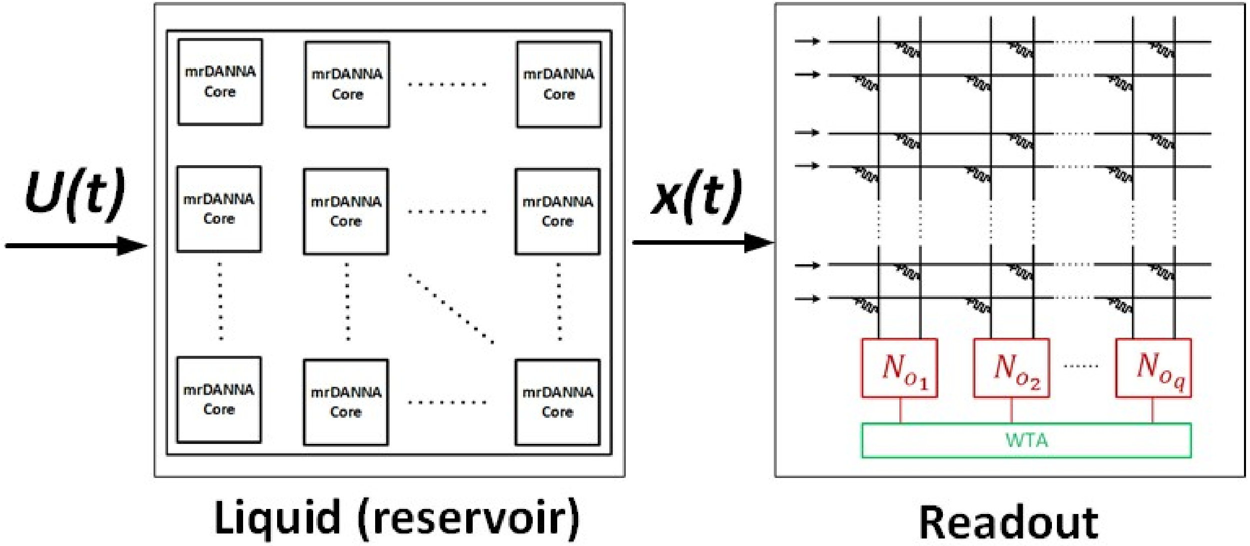
# RC Implementation Framework

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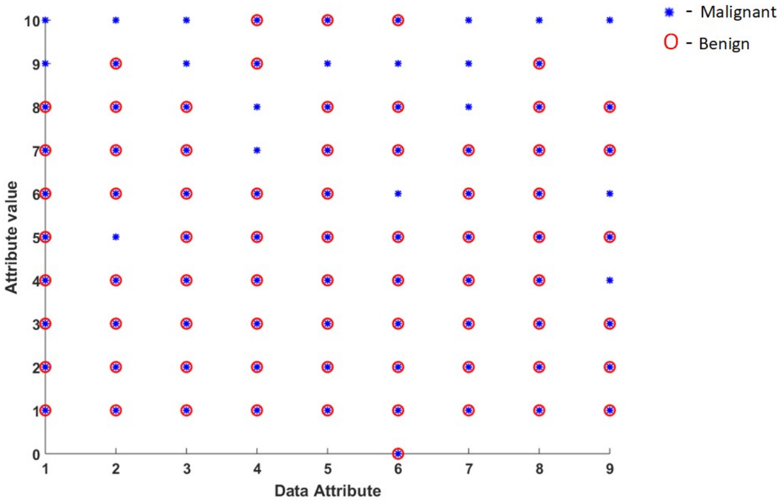
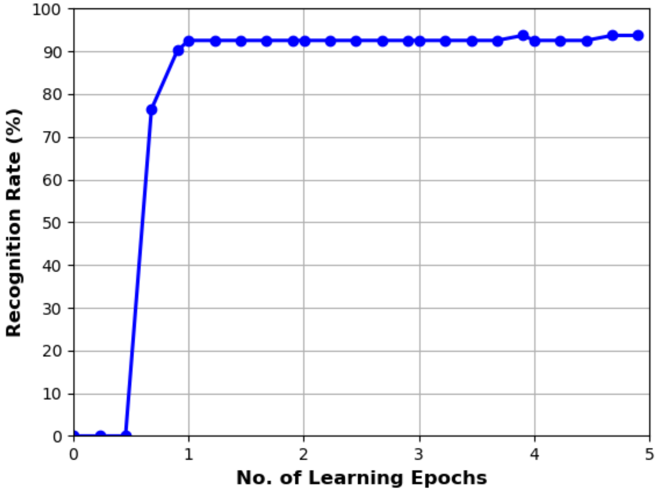
# Simulation Results

- Simulation using high level model
- Dataset – Wisconsin Breast Cancer (WBC)
- Reservoir generation using evolutionary optimization algorithm
- Readout layer based on crossbar based STDP online learning

**Dataset**




**Readout Layer Learning**

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# Advantages of Proposed Readout

- *Trade off between learning efficiency and hardware complexity must be considered for any required task at hand*
- STDP based crossbar:
  - STDP is ‘local’ weight update method
  - Hardware efficient for achieving weight update
  - More efficient for applications with pre-processed inputs such as reservoir computing
- For other popular techniques such as backpropagation, achieving weight update computation fully in hardware is complex

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# Summary

- Memristor based Reservoir Computing:
  - Reservoir Layer
    - Memristive spiking recurrent neural network
    - mrDANNA architecture for implementation
  - Readout Layer
    - Memristive crossbar based readout layer
    - STDP based learning

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# THANK YOU!