

Time-frequency pattern wake-up detector for low-power always-on sensing of acoustic events

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Abstract— In acoustic event detection scenarios, average power consumed for continuous monitoring can be lowered by an low-power always-on sensor interface, waking-up power-hungry signal sampling and processing circuitry only upon detection of the specific audio-pattern. We research on power consumption of such wake-up sensing (WUS) interface consisting of a multichannel programmable analog filtering bank, signal detectors, and a digital wake-up pattern detector circuit. Focusing on the pattern detector, this paper investigates a design performing wake-up upon matching a sequence of its multi-channel inputs against a digitally preset template of time-frequency states. We compare two hardware implementations of a proposed design: one exploiting a dedicated programmable sequential logic chip, and the other on a low-power 16-bit microcontroller (MCU). In most cases, experimental results generally demonstrate lower energy expenditure obtained by the MCU. Only 330 nW is required for always-on listening, and 1.27-1.71 μ J is spent for analysis of a 3-channel sequence consisting of 4 successive states, each lasting for 200-500 ms. Depending on the application scenario, proposed WUS interface enables for extension of sensor node's battery-lifetime up to 7.4 times, compared to continuous sampling and processing.

Keywords— *always-on acoustic monitoring, low-power sensor interfaces, wake-up sensing, pattern detection circuits, time-frequency analysis, template-matching*.

I. INTRODUCTION

In many application domains, acoustic monitoring is aimed at detection of rarely occurring events, exhibiting a distinctive time-frequency pattern (signature). Such are cases with biomedical monitoring of respiratory symptoms [1], sleep disorders [2], and with many assistive technologies: fall-detection [3], for hearing- [4] or locomotor impairments [5]. Also, such are many environmental monitoring scenarios, including detection of wildlife or pest vocalization [6], perimeter monitoring in security applications [7], structural health [8], urban traffic monitoring [9] etc.

Many of those scenarios require event detection carried out on an energy-constrained sensor node. However, acoustic event detection requires for continuous, uninterrupted, periodic sampling and digital processing of the signal at the multiple of its Nyquist-rate. Processing algorithms most typically implement classification from a set of features extracted from some of signal's time-frequency decomposition [10]-[11]. Algorithms' ever-increasing complexity limits the autonomy of the energy-constrained sensor node, due to significant share of time spent in active state. Aiming to decrease the sensor node's

average power by constraining the sampling and processing time only to the intervals when acoustic event actually happens, we investigate a concept of acoustic “wake-up sensing” (WUS, [7]-[8]). It envisions an always-on low-power wake-up sensor interface, performing rudimentary analog/mixed-signal event detection, and triggering the analog-to-digital converter (ADC) and the main digital signal processor (DSP) only in presence of a potential event candidate [12]-[15].

Going a step further from a simplistic audio wake-up based on time-domain magnitude/envelope level detection [15], already adopted within some commercial MEMS microphones [16] and stand-alone ICs [17], we investigate the power-budget of a more complex WUS interface, performing wake-up upon detection of a preset time-frequency pattern template.

A typical hardware architecture enabling such design is shown in Fig. 1. It consists of two major parts: 1) time-frequency features extraction circuit, and 2) wake-up pattern detector. An analog-domain implementation of the time-frequency features extraction circuit demonstrated in [18] comprises of a multichannel bank of low-power programmable band-pass filters, envelope detectors and comparators. Filters decompose the input signal into N discrete frequency bands (i.e. channels). Each channel's central frequency $f_1 \dots f_N$ and bandwidth $B_1 \dots B_N$ is programmed individually. Signal amplitude contained within each filter's pass-band is extracted by the envelope detector and finally, thresholded by the comparator. Each comparator outputs a time-continuous binary waveform, which localizes spectral content associated to each channel in time.

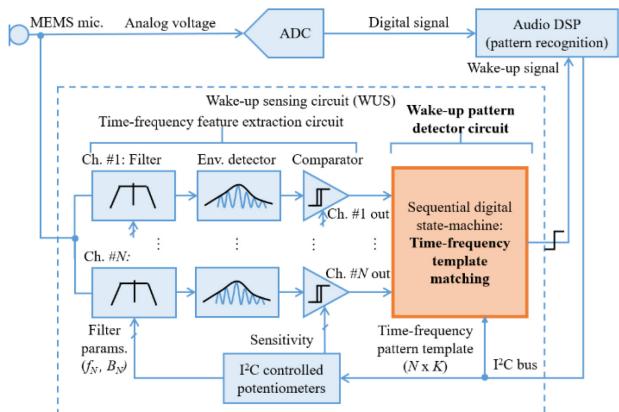


Fig. 1. WUS Hardware architecture consisting of a filter bank, channel detectors, and a classifier circuit (highlighted).

Encouraged by its power consumption of merely 10.5 – 13.5 μW per channel [18], in this work we complement the time-frequency feature extraction circuit with an accompanying wake-up pattern detector design. Detector is required to generate a wake-up signal upon finding a match between the feature extraction circuit's multi-channel output, and a preset acoustic time-frequency template (i.e. perform time-frequency template matching). Contextually closest literature approach includes a single-channel time-domain template matching circuit implementing dynamic time warping for wake-up of wearable inertial sensors, within 9 – 193 μW [19]. Also, an analog circuit for two-dimensional template matching of geometric handwritten patterns was shown in [20], however lacking any power consumption figures.

We contribute by analyzing two implementations of multi-channel time-frequency template matching concept, designed specifically for acoustic wake-up: one using a dedicated programmable logic chip and another on a low-power microcontroller. Both are programmable from the main DSP through an I²C interface. We analyze boundaries of the design's pattern detection errors, profile energy consumption for each implementation, and finally, estimate its effect on lifetime extension of a sensor node in a typical operating scenario.

The rest of the paper is organized as follows. Section II. shows the proposed design of a wake-up pattern detector, with II.A. describing its operating principle, and II.B. and II.C. showing implementations on a low-power microcontroller and a dedicated programmable logic chip, respectively. Experimental results are given in Section III. III.A. analyzes boundaries of its pattern detection accuracy and III.B. evaluates the circuit's energy-consumption. Finally, Section IV. concludes the paper.

II. WAKE-UP PATTERN DETECTOR DESIGN

A. Time-Frequency Template Matching Wake-up Concept

For the purpose of event detection, time-frequency signatures of many acoustical events are often represented by a concise set of two-dimensional time-frequency shapes or regions, serving as discriminatory features (see [1], [2], [9] and [10]). The proposed pattern detector wake-up circuit design envisions that signal's time-frequency signature is approximated by an ordered sequence of N -by- K rectangular regions, as shown by the example in Fig. 2a). N is total number of frequency bands (i.e. filtering channels) required to represent signal's frequency content ($N=3$ channels in Fig. 2). Each band's central frequency $f_1\dots f_K$ and bandwidth $B_1\dots B_K$ is preset by tuning the associated band-pass filter from the Fig. 1. Comparator's response in each channel from the Fig. 1 provides an information on intervals of activation (i.e. presence of signal) within each frequency band throughout time, as illustrated in Fig. 2b). Thus, time-frequency template is constructed by temporally delimiting responses of all N channels into K non-overlapping intervals ($K=7$ in Fig. 2) of individual durations $T_1\dots T_K$. Considering them a sequence of K temporal states, wake-up pattern detection is performed by a state-machine in Fig. 2c).

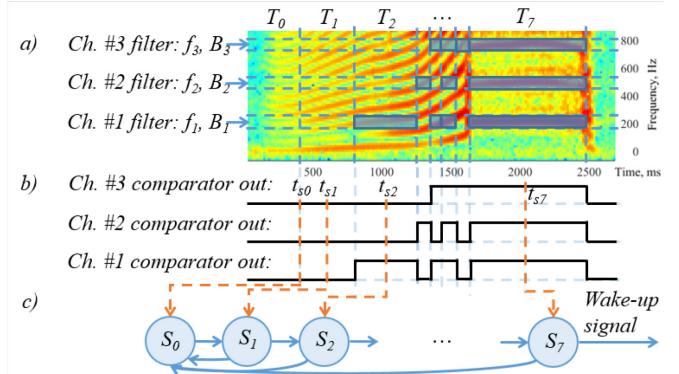


Fig. 2. Operating principle: a) spectrogram of an example signal, b) time-frequency feature extraction circuit's multi-channel response, and c) state-machine used for sequence analysis.

In each state $S_1\dots S_K$, the state-machine compares the comparators' N -channel binary output waveform pattern to the corresponding N -bit template. Once a complete sequence is matched, wake-up pattern detector raises a wake-up signal for the ADC and DSP to initiate signal sampling and processing. Detection of the sequence start (transition from S_0 to S_1) is asynchronous. From there on, during the sequence analysis, state-machine operates synchronously. Motivated by the minimization of the dynamic power, it samples the input channels only at the single sampling instant $t_{s1}\dots t_{sK}$ per state. Thus, sampling instants are non-equidistant, chosen to correspond to the midpoints of states durations $T_1\dots T_K$ in order to maximize the state detection probability w.r.t. possible non-idealities of the feature extraction circuit's output.

Next, we verify this concept experimentally on a low-power microcontroller (MCU) and a programmable logic chip, analyze its boundaries of sequence recognition accuracy, and compare the energy-cost. We constraint the design to an arbitrary (digitally configurable) 3-channel input sequences comprised of 3-10 states, each lasting from 100 ms to 10 s.

B. Software Implementation on Low-Power Microcontroller

Microcontroller version of the wake-up pattern detector was implemented on a low-power 16-bit MCU from the MSP430 family (MSP430F2013, Texas Instruments [21]), according to the diagram shown in Fig. 3. Upon power-on, MCU enters the configuration mode, enabling for preset of the wake-up pattern template over I²C. Once configured, MCU enters the least-consuming low-power mode, stopping its central processing unit (CPU) and the oscillator (i.e. mode LPM4 [21]). From there, it asynchronously listens its digital inputs for a combination signaling the beginning of sequence analysis (i.e. transition between states S_0 and S_1). During the wake-up sequence analysis (states $S_1\dots S_K$), digital input channels are sampled at non-equidistant instants $t_{s1}\dots t_{sK}$ defined by the wake-up pattern's template, using a single 16-bit timer. Timer is clocked by an RC oscillator at 22.22 kHz, with the CPU halted in the low-power mode (i.e. power mode LPM3 [21]).

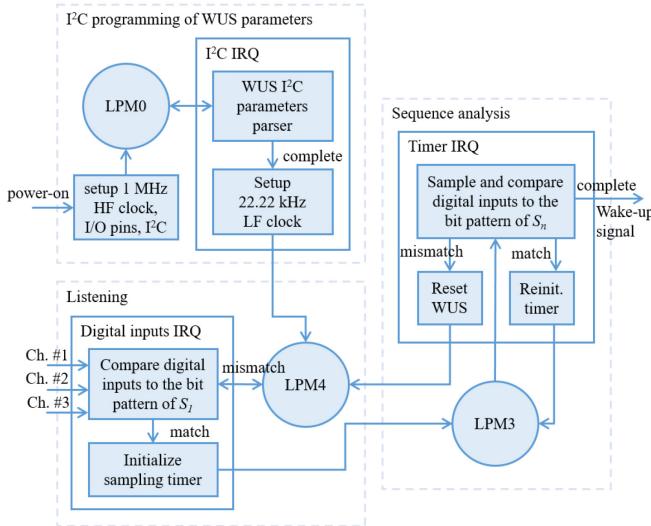


Fig. 3. MCU implementation of time-frequency pattern wake-up detector. Block-chart including power-states transitions.

Upon timer interrupt, CPU is awoken, digital inputs are simultaneously sampled, and based on outcome, state machine is either advanced to the next state S_{k+1} presetting the timer for $t_{s(k+1)}$, or rolled back into the listening state S_0 (MCU power-mode LPM4) in case of mismatch. Upon a successful progression through all K states, a digital wake-up output signal is generated.

C. Hardware Implementation on Programmable Logic Chip

Hardware version of the detector was implemented on the mixed-signal, one-time programmable sequential logic chip GreenPAK SLG46537V (Silego [22]), chosen for providing a minimal set of required functional blocks (look-up table combination logics, timers, 8-state asynchronous state-machine logics, and I²C slave controller) in combination with lower static power (0.83 μ W) than CPLD or FPGA (best case \sim 2 μ W [23]).

3x1 look-up table (LUT) combination logics blocks are used for sampling digital combinations of 3 inputs. Sequence analysis is asynchronously triggered with LUT S_0 output activating the state-machine sequential logics, which starts timers. They count at 25 kHz, and on runout, they trigger their LUTs $S_1 \dots S_K$. This way, each LUT is activated to sample inputs only at its respective absolute sampling instants $t_{s1} \dots t_{sK}$. LUTs' output are fed back to the asynchronous state-machine logic block, which in the final state S_K , in case of the positive outcome, generates the wake-up output signal for DSP. Wake-up pattern template is configured by altering the content of their truth tables and timer values using the I²C slave controller upon power-up (Fig. 4).

Silego's main limitation is the lack of memory blocks for storage of larger wake-up pattern templates. Consequently, this affects the circuit architecture, requiring the instantiation of as many individual LUTs and timers as there are states. With given constraints, proposed architecture enables for implementation of no more than 3 input channels, and 4 successive states within the single chip. Scalability is achieved only by chaining multiple chips together (not shown in Fig. 4).

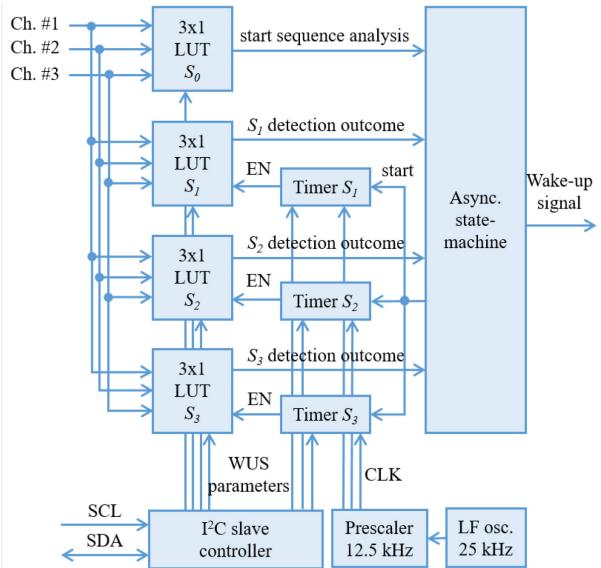


Fig. 4. Hardware implementation of the wake-up pattern detector using the Silego GreenPAK programmable logics.

III. EXPERIMENTAL RESULTS

A. Boundaries of Sequence Recognition Accuracy

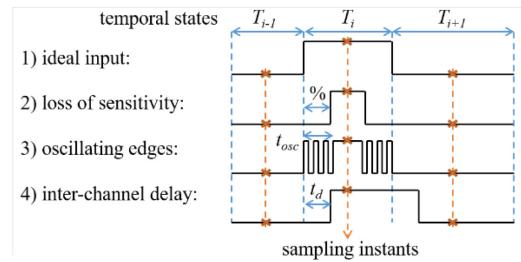
Due to single sampling point per each state, sequence recognition errors dominantly occur due to temporal mismatch between the expected sampling instants defined by a template, and the actual signal present at the inputs. Thus, to identify a design-subspace guaranteeing the maximal accuracy, we modelled sequence recognition probability parametrically against: (1) implementation-specific parameters (clock frequency), (2) input sequence parameters (state duration, number of channels, number of states), and (3) input sequence's non-idealities (poor sensitivity, oscillating edges, inter channel delay in Fig. 5a).

In order to enable for repeatable, parametric generation of such non-ideal output of a multi-channel time-frequency feature extraction circuit [18], test sequences were generated synthetically. For each set of the input sequence's parameters (i.e. number of states in a sequence, states' durations, percentage of simulated sensitivity loss, duration of oscillating edges, duration of inter channel delay), a test was repeated for 50 random sequence realizations, to enable for statistical analysis. Each sequence recognition test (producing a single binary outcome: positive/negative) comprised of inspection for a full sequence match between the non-ideal test signal and its idealized template, obtained at sampling instants defined by the sequence template.

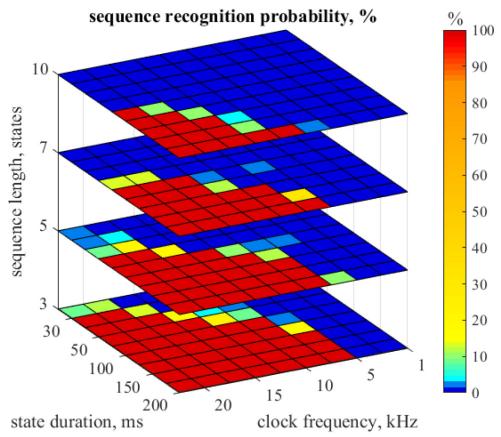
Following such methodology, accuracy of both pattern detectors implementations was experimentally evaluated. NI USB-6211 data acquisition card was used for three-channel input sequence generation and for acquisition of the wake-up pattern detector's output. Time-frequency templates were preset by I²C using the NI USB-8451. Whole measurement setup was controlled from Matlab.

Results in Fig. 5b) indicate that by running the sequence recognition at 25 kHz clock (typical case with MSP430 and Silego), fine-grain sequences containing very short states can be recognized (down to three successive 30 ms states, or even 10 states lasting for 100 ms each, as this error accumulates with number of states). In order to lower the power, operating frequency can be further scaled down to 10 kHz, still sufficing for reliable identification of up to 10 successive 200 ms states.

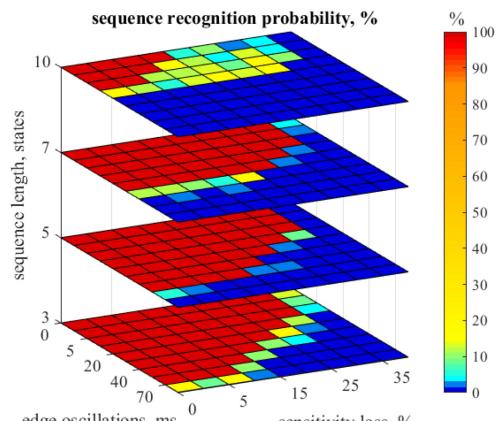
Resilience to non-idealities from Fig. 5a) in input's waveform at 10 kHz operating frequency are depicted in Fig. 5b). Problem scales with number of states. Thus, for very long sequences of up to 10 states, pattern detector is able mutually tolerating for 5% sensitivity loss and 15 ms edge oscillation. Robustness improves by increasing the timer's clock frequency.



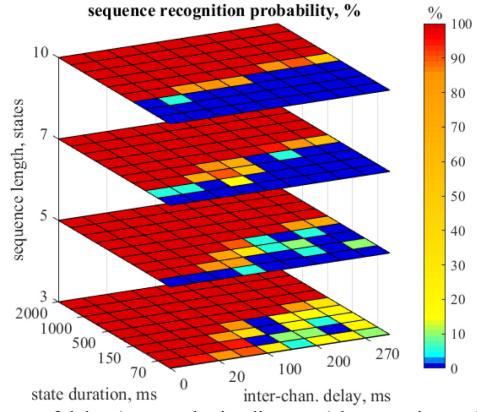
a) Non-idealities of time-frequency feature extractor circuit's output (i.e. input pattern for the wake-up pattern detector circuit).



b) Influence of the wake-up pattern detector's clock frequency.



c) Influence of input pattern's non-idealities.



d) Influence of delay (temporal misalignment) between input channels.

Fig. 5. Parametric analysis of sequence recognition probability for 3-ch. detector. Every outcome obtained for 50 random sequences.

Single sampling instant per state (Fig. 5a)) defines maximal theoretical tolerance to inter-channel delay of the time-frequency feature extraction circuit's output at exactly half of state duration. Accounting for finite operating frequency, Fig. 5d) shows that up to 100 ms of temporal mismatch is tolerated for sequences containing up to 10 states, each no shorter than 300 ms. This error also accumulates with number of states.

B. Energy Consumption

WUS pattern detector's energy consumption was evaluated in three steps: (1) power-profiling in characteristic operating states, (2) calculation of energy required for sequence analysis, and (3) estimation of sensor node's lifetime extension gained by utilization of the WUS featuring the proposed pattern detector.

In the first step, average powers were measured for 3 typical operating states: a) listening for sequence initiation, b) sequence analysis, and c) I²C programming (upload of time-frequency pattern's template). Powers were obtained from operating voltages and current consumption profiles measured by INA128 instrumentation amplifier on a 100 Ω high-side shunt connected in series to the Silego GreenPack programmable logics and the MSP430F2013 MCU chip respectively. Average steady-state currents were additionally verified with Fluke 45 multimeter and uCurrent Gold current probe.

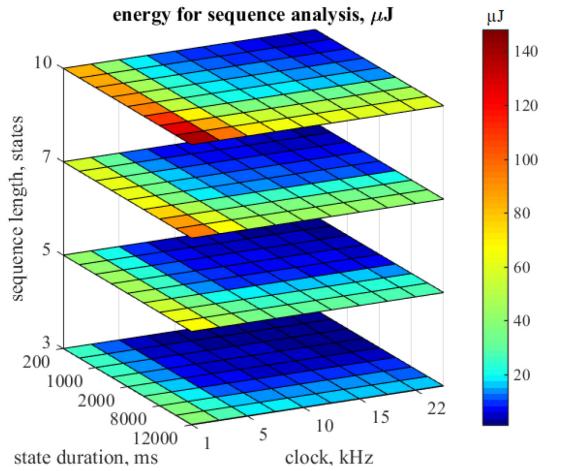
Results in Table I show that both pattern detector implementations exhibit listening powers below 1 μW (see power states P_1) when operating at equal supply voltages of 1.8 V, and clock frequencies matched as closely as possible. During the sequence analysis, Silego's power rises to the constant-value of 8.75 μW (power state P_2), required for continuous operation of its timer's 25 kHz clock oscillator. On the other hand, MCU's average sequence analysis power is optimized by operating the state-machine timer by a 22.22 kHz clock with the CPU halted in LPM3 (power state P_3 , 0.59 μW). Minimal intervals of CPU's active time are invoked only for digital inputs sampling and associated state-machine transitions (i.e. $P_2 = 104.14 \mu\text{W}$ for CPU clocked at 22.22 kHz). For reference, Table I also lists the consumption of remaining WUS subsystems: MEMS microphone [24] and the referent time-frequency features extraction circuit (analog filter, envelope detector [18]).

TABLE I. POWER STATES OF THE WAKE-UP PATTERN DETECTOR.

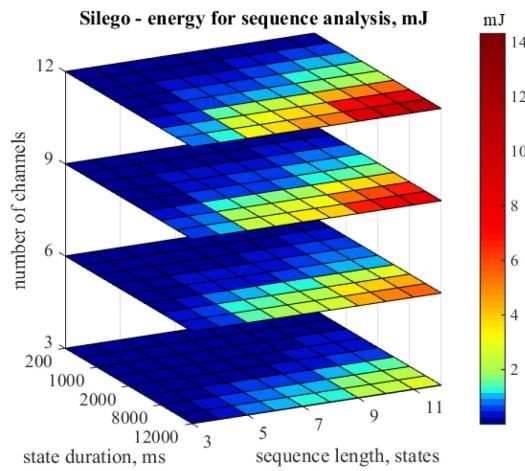
Wake-up pattern detector circuit		
Platform	MSP430	Silego
Operating voltage V_{CC} (V)	1.80	1.80
Clock frequency f_{clk} (kHz)	22.22	25.00
P_1 : Listening, oscillator OFF (μ W)	0.33	0.83
P_2 : Sequence analysis, Active (μ W)	104.14	8.75
P_3 : Sequence analysis, Sleep (μ W)	0.59	-
P_4 : I ² C programming (μ W)	113.27	8.75

Remaining subsystems of the WUS signal chain		
MEMS microphone (μ W) [24]	16.02	
WUS analog filter (μ W / channel) [18]	10.01	
WUS envelope detect. and comp. (μ W / channel) [18]	1.40	

In the second step, we modelled energy required for sequence analysis by both wake-up pattern detector implementations, parametrized w.r.t. number of states, state durations and number of channels. Simulation was based on measurements from Table I, fed into the Matlab model addressing the implementation-specifics of both classifier circuits. Results in Fig. 6 a) and b) generally demonstrate lower energy expenditure obtained by the MCU. Analysis of the typical sequence (i.e. 3-4 states, each lasting for 200-500 ms) requires only 1.27-1.71 μ J on the MCU, while on the Silego it takes 4.32-15.10 μ J.



a) Pattern detector implemented on the MCU: 1.27 to 148.05 μ J.



b) Pattern detector implemented on the Silego: 4.32 μ J to 14.31 mJ.
Fig. 6. Energy consumed for the wake-up pattern sequence analysis.

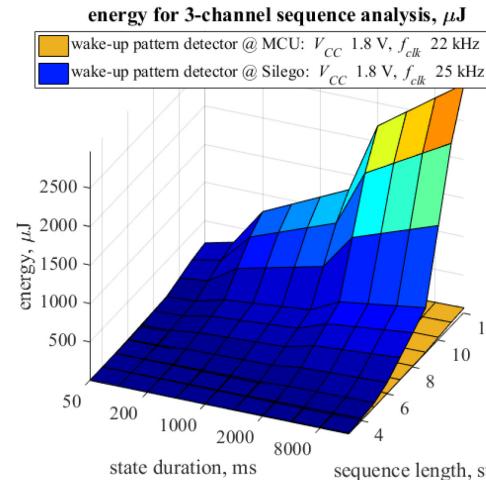


Fig. 7. Comparison of energy requirements for a 3-channel sequence analysis. MCU (orange) vs Silego (blue-to-red colorscale).

However, more detailed head-to-head comparison in Fig. 7 reveals 10-15% lower energy-cost of Silego, but only for limited cases of the shortest 3-channel sequences constrained to max. 4 states, lasting less than 100 ms each. Finally, in case of more complex time-frequency patterns requiring for a sequence of more than 4 states and/or more than 3 channels, MCU proves more scalable than Silego. In such case, Silego's energy spans over more than three orders of magnitude, as it is required to chain several programmable chips together.

Finally, we estimated the lifetime extension of a sensor node for acoustic event detection utilizing the WUS interface triggering the ADC and DSP, in comparison to the continuous (periodic) sampling and processing. Analysis is based on the use-case of a wearable sensor node for quantification of asthmatic symptoms, by detecting the intervals of asthmatic wheezing in respiratory sounds [1]. We modelled the sensor node featuring WUS interface with a MCU-implemented wake-up pattern detector. Detector's contribution to the sensor node's average power was modelled from the listening power (Table I) and sequence analysis energies (Fig. 6a), remaining WUS subsystems – filters, envelope detectors and comparators from [18], and the microphone from its datasheet [24] (see Table 1). ADC and DSP were chosen and modelled according to application-related parameters derived in [25]: once woken-up, 16-bit AD7684 ADC samples at 8 kHz. DSP performs identification and temporal tracking of intermittently appearing wheeze-frequency maxima in successive 512-point FFT spectra [1]. Two DSPs were analyzed: ARM Cortex M4 SoC CC2640, and the dedicated audio DSP C5355 [25]. Fig. 8 shows that the sensor node's lifetime extension is dominantly influenced by respective total powers consumed in the listening state. Audio DSP C5355 requires 220 μ W, while CC2640 SoC can implement listening at only 4.9 μ W [25]. Thus, CC2640 with smaller sleep current enables for higher energy savings, asymptotically reaching 7.4x w.r.t. continuous processing for case of a single wheezing-event appearing once per day, and C5355 up to 2.7x.

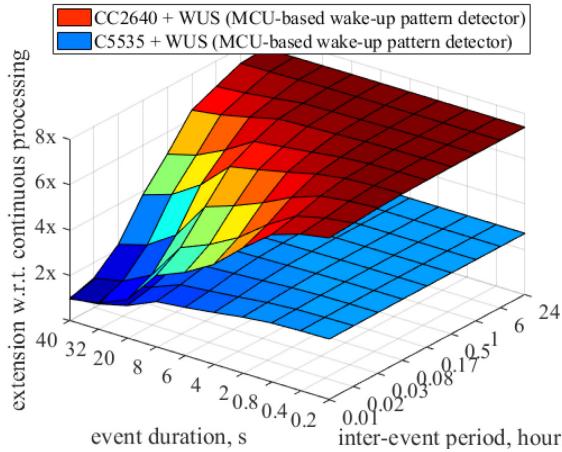


Fig. 8. Lifetime extension of an asthmatic wheeze detection sensor node utilizing WUS interface triggering the on-event processing.

IV. CONCLUSION

Designing the low-power always-on sensor interface for acoustic wake-up of an energy-hungry DSP, this paper showed the implementation of the low-power multi-channel digital sequence analyzer, used for template-matching of the preprogrammed time-frequency patterns. While posing limitations for fine-grain speech recognition, presented audio pattern detector is aimed at the rudimentary recognition of mechanistic sounds featuring time-frequency pattern discriminated by a finite sequence of discrete time-frequency states. Combined with the analog 3-channel time-frequency feature extraction circuit [18], this design enables implementation of the complete audio wake-up signal chain within only 35 μ W in listening mode. In the future work, we plan to integrate the demonstrated wake-up detector design with remaining WUS signal chain subsystems (microphone, bank of programmable filters and envelope detectors).

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