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High-Dynamic-Range Image Reconstruction from Pixel-Level Self-Reset ADC Samples

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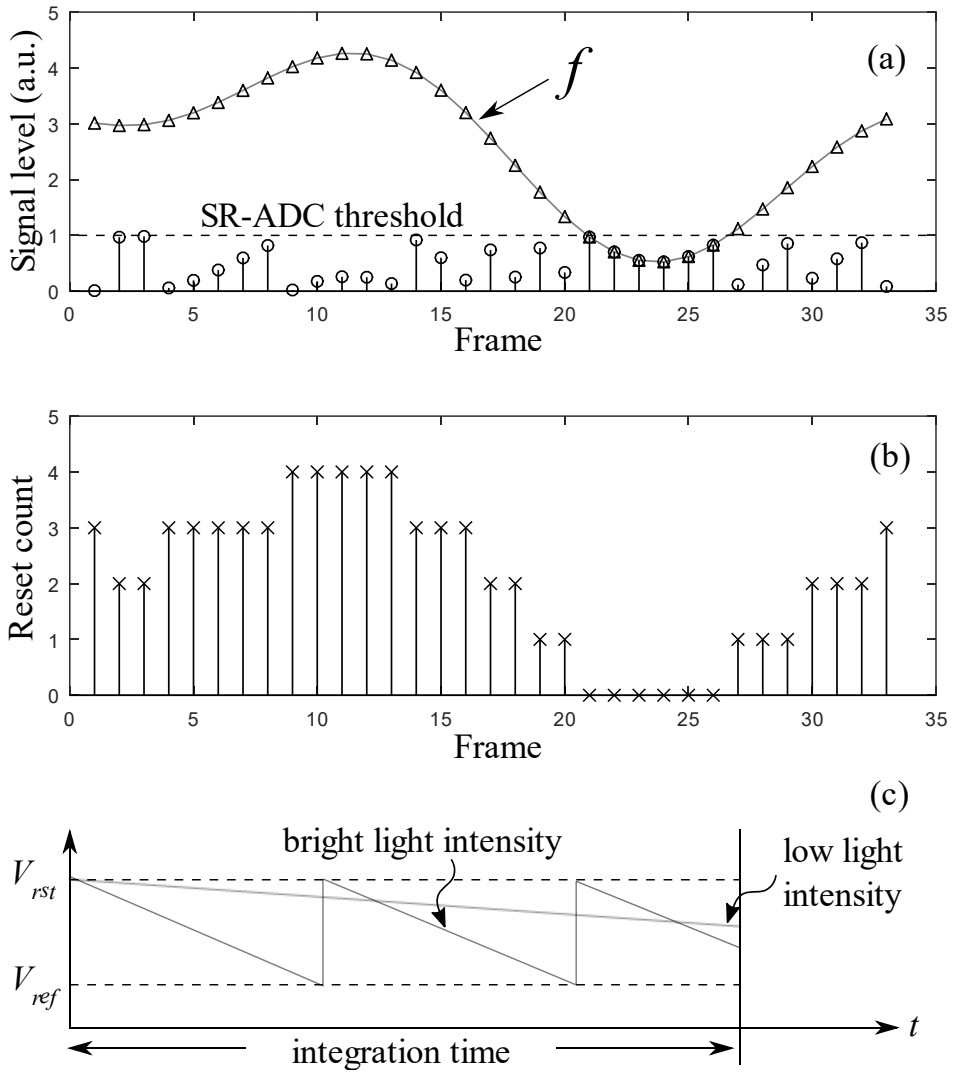
SENSORS WITH SENSE

Introduction

- HDR imaging is a technique that allows much larger range of luminosity to be expressed than the typical image sensor can capture.
- Full range of illumination in the real world is over 100 dB. Typical CMOS sensors can capture around 60 dB of dynamic range.
- One way to acquire HDR images is to combine multiple low-dynamic-range images, taken with different exposure times. Also special pixel types have been developed. **The aim of this work is to present a method to obtain HDR images in real time using typical commercial CMOS image technologies.**
- Utilizing self-reset ADCs, it is possible to achieve higher dynamic range within single integration period in CMOS technology (Wide dynamic range CMOS image sensor with pixel level ADC, J. Rhee *et. Al,* 2003).

Self-Reset ADC

- SR-ADC resets the image sensor every time the sensor's voltage crosses pre-defined threshold.
- Storing reset count in digital pixel readout takes additional area thus increasing the pixel area.
- Is it possible to construct an HDR image without knowing the reset count? Yes, using modular arithmetic.

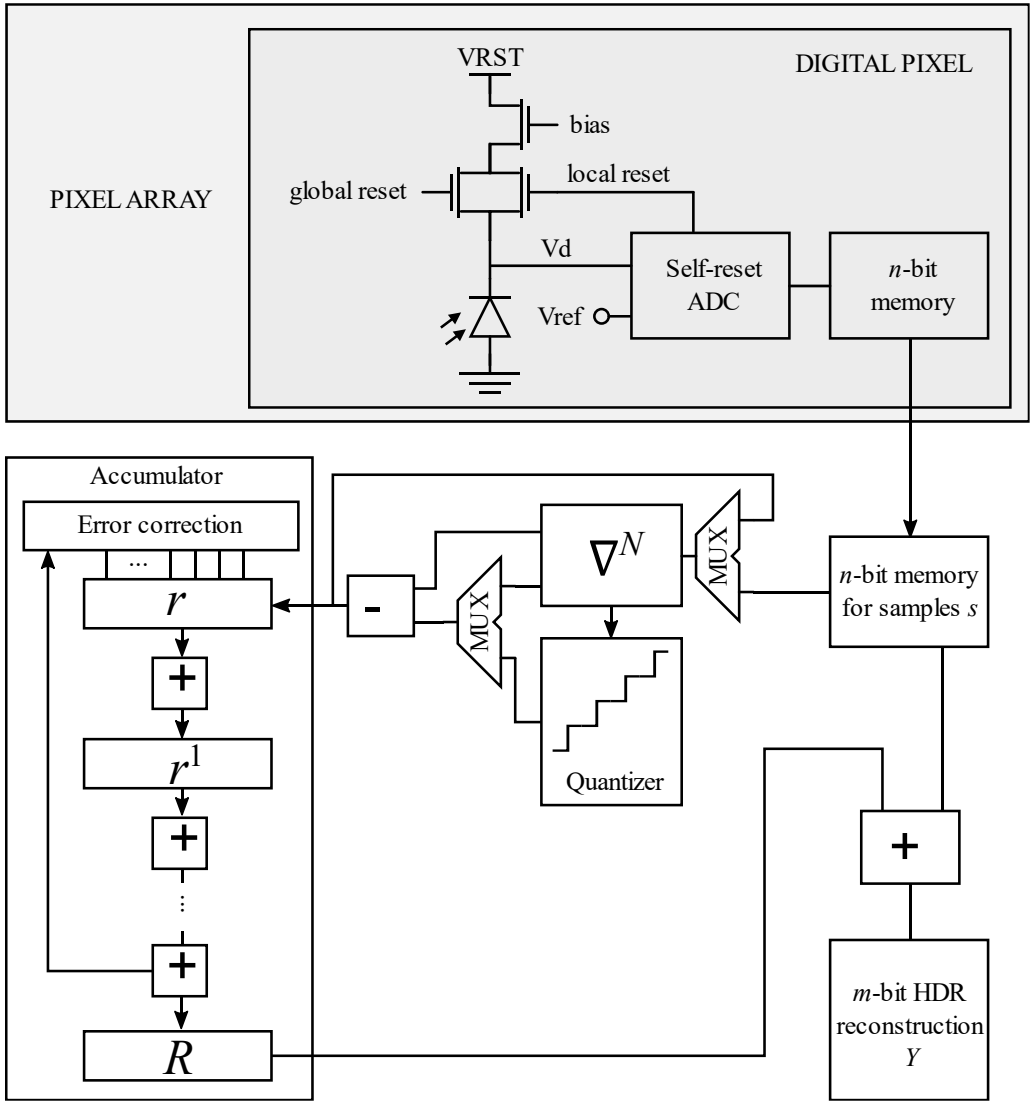


Constructing HDR Image without storing the reset count

- This paper is based on work "On unlimited sampling.” by Bhandari, A. *et. al*. *2017 International Conference on Sampling Theory and Applications (SampTA)*. IEEE, 2017.
  1. Signal must be bandlimited and zero-mean.
  2. Signal must be sampled at constant sampling rate, at least πe greater rate than Nyquist frequency.
  3. An estimate of the measured signal’s maximum amplitude must be known.
- In imaging applications the signal is not bandlimited or zero mean, the frame rate may vary and the maximum illumination level is unknown.
- Our work focuses on recovering (reconstructing) an HDR image from low dynamic range and low bit count samples. Due to the uncertainties listed above the reconstruction may be incorrect and some error correction mechanism is needed.

Circuit arrangement for HDR image reconstruction

- Digital pixel consists of global reset transistor, local reset transistor, SR-ADC that converts analog signal V_d into *n*-bit samples and an *n*-bit memory for storage.
- Reconstruction circuit arrangement consist of memory for SR-ADC samples *s*, an *N*-th order finite difference calculation unit, a quantizer, an accumulator unit and optional error correction unit.



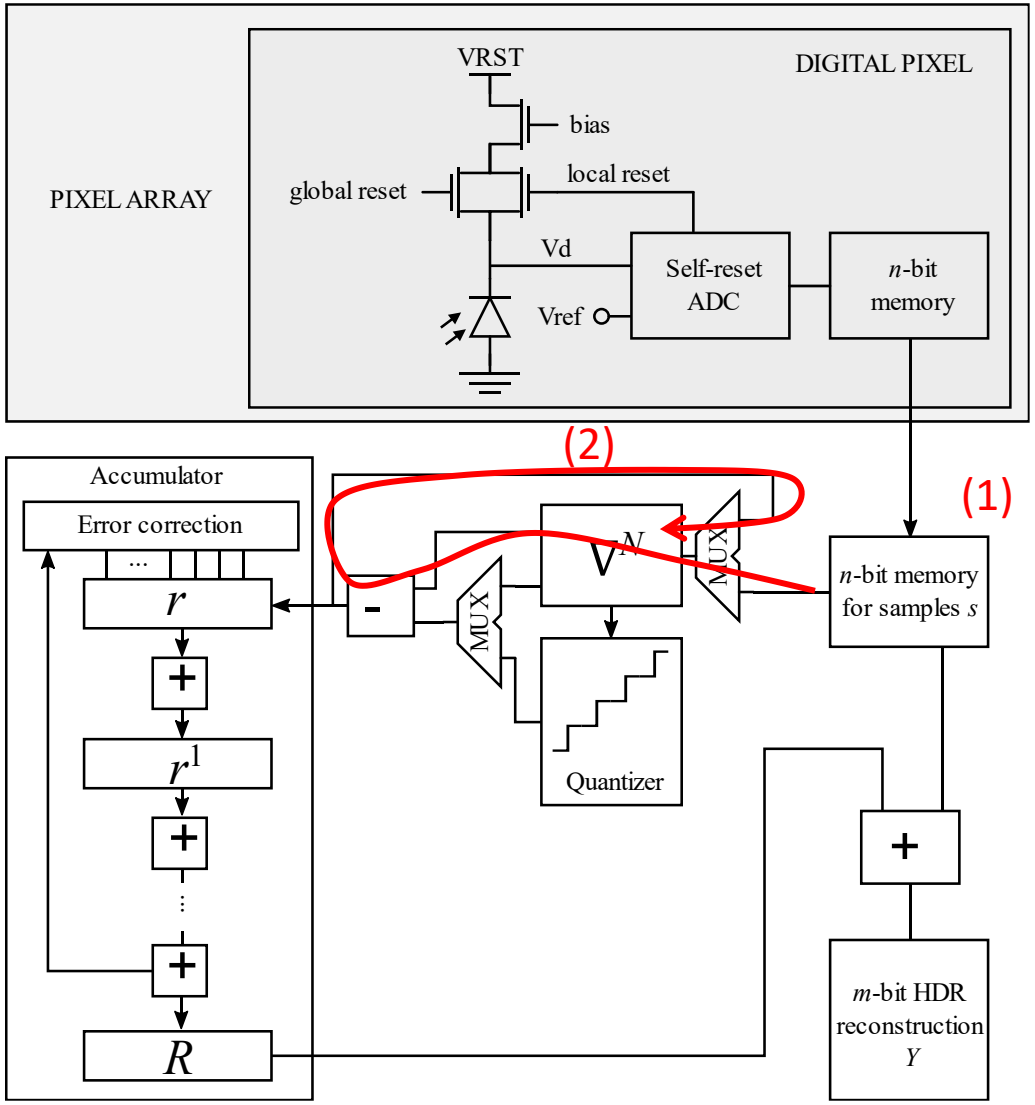
Circuit arrangement for HDR image reconstruction

- 1) Store at least N amount of *n*-bit samples s from SR-ADC into separate memory, where $N = 1,2,3, \ldots$ (more about the choice of *N* later)
- 2) Calculate N-th order finite differences $\nabla^N(s)$, such that

  $\nabla s[k] = s[k] - s[k-1]$

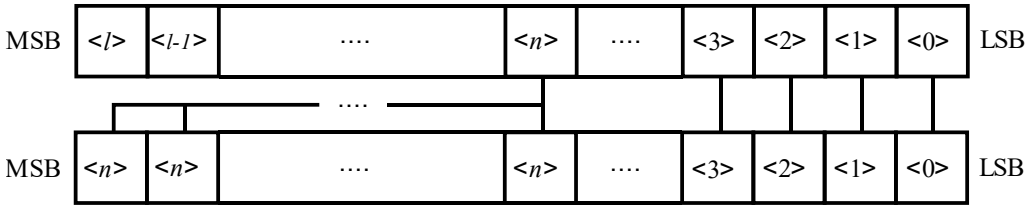
  and iteratively

  $\nabla^N s[k] = \nabla^{N-1} s[k] - \nabla^{N-1} s[k-1]$, where *k* denotes the index of the latest frame captured.



Circuit arrangement for HDR image reconstruction

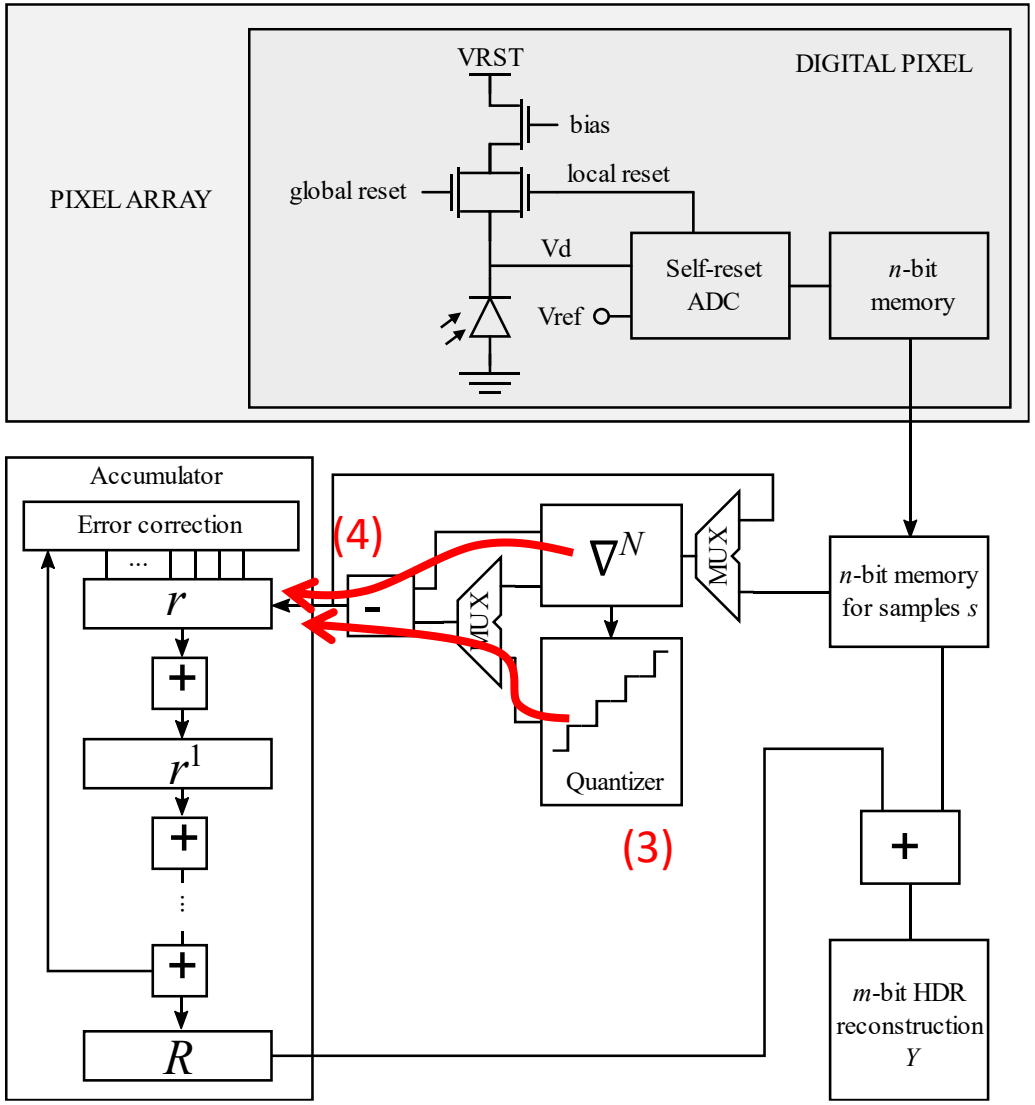
- 3) Quantize the result
  $Q: \nabla^N s[k]$
  $\rightarrow \{-2^{n-1}, -2^{n-1}+1, \ldots, 2^{n-1}-2, 2^{n-1}-1\}$



- 4) Calculate residue values r and store them into accumulator

$$r[k] = Q(\nabla^N s[k]) - (\nabla^N s[k])$$

Note! By definition *r* is some positive or negative multiple of 2^n.



Circuit arrangement for HDR image reconstruction

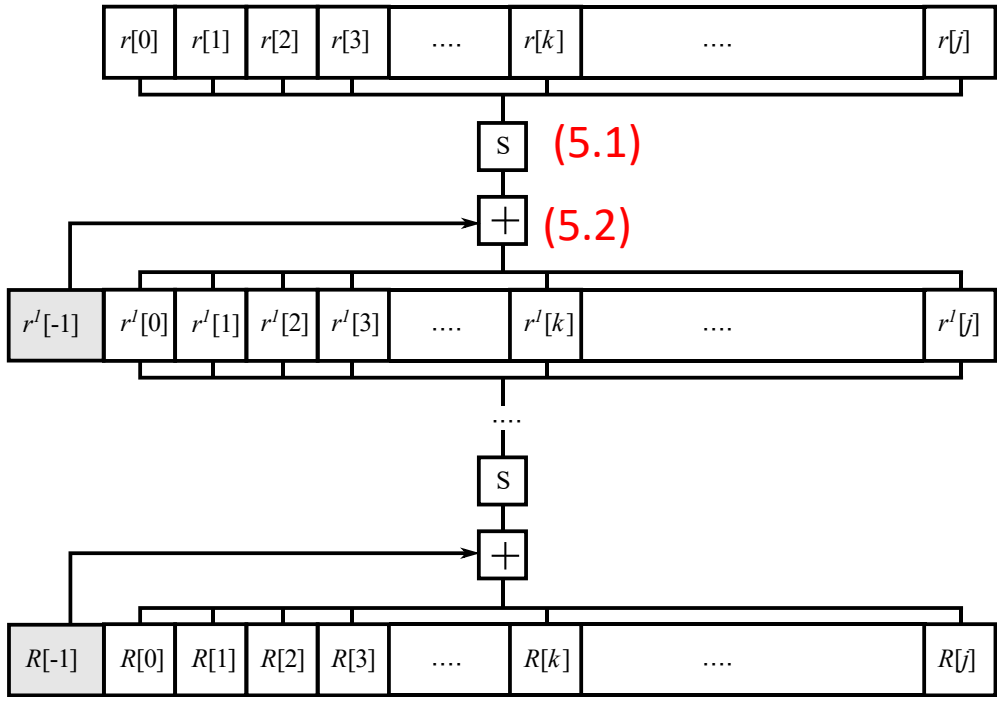
- 5) Accumulate the previous result *r*, *N*-times within the accumulator.
- 5.1) calculate cumulative sum from the partial sums r^i,

$$\{S(r[k])\}_{l=0}^{k} = \sum_{i=0}^{l} r[i], \text{ for i=0,1,2, … , } l$$

and compute the course bits *R* such that

$$R = S^N(r) = \underbrace{S(S(\dots S(r) \dots))}_{N-times}.$$

- 5.2) For each accumulation round *i*, add the value $r^i[-1]$ to the result of the cumulative sums. After accumulations, shift the memory contents left such that $r^i[-1] \coloneqq r^i[0]$.
- The final result *R*, should correspond to reset counts of conventional SR-ADC readout circuit.



Circuit arrangement for HDR image reconstruction

- 6) The result *Y* is the constructed *m*-bit HDR representation of measured *n*-bit signal

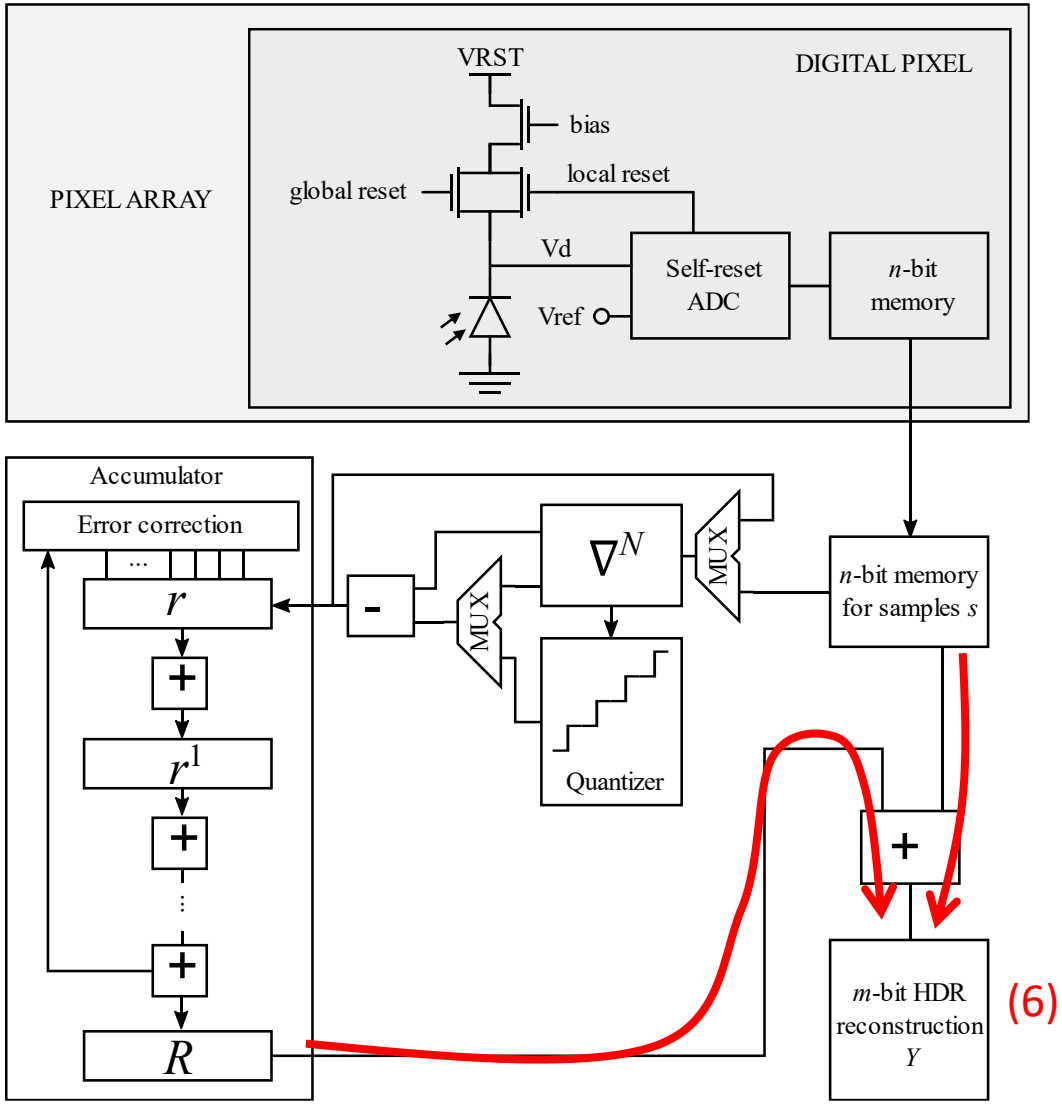
$$\mathrm{Y}[k] = s[k] + R[k].$$

- The reconstruction is correct if the following criteria is satisfied

$$-2^{n-1} \leq \nabla^N f \leq 2^{n-1} - 1.$$

  This may be unsatisfied due to many reasons such as quantization noise, abrupt changes in light illumination (signal is not bandlimited between frames), the amount of SR-ADC bits is too small, wrong choice of parameter *N* etc…

- Some error detection and correction mechanism is necessary.



Error detection and correction

- If we consider the true coarse bits $\hat{R}$ to be calculated from quantized detected signal f_q such that $\hat{R} = f_q - s$, we can calculate the true residues $\hat{r} = \nabla^N \hat{R}$.
- The reconstruction relies on recovering $\hat{R}$ from cumulative sums of r in presence of errors e, such that the $r = \hat{r} + e$.
- Fortunately, $\hat{r}, r, e$ are by definition negative or positive multiples of 2^n, and we know that $0 \leq Y \leq 2^m - 1$, and $0 \leq \hat{R} \leq 2^m - 2^n - 1$ thus $0 \leq R \leq 2^m - 2^n - 1$.
- Depending on the choice of *N*, the cumulative error grows extremely fast which is good for error detection. There is a trade-off, bigger *N* causes more errors to be present during reconstruction and smaller *N* needs more memory to detect the error. Practical values are $N < 5$ and the choice is highly application specific considering the limitations of the signal properties.
- If the error correction fails the reconstruction is permanently lost and only way to recover is to start the reconstruction from the beginning.

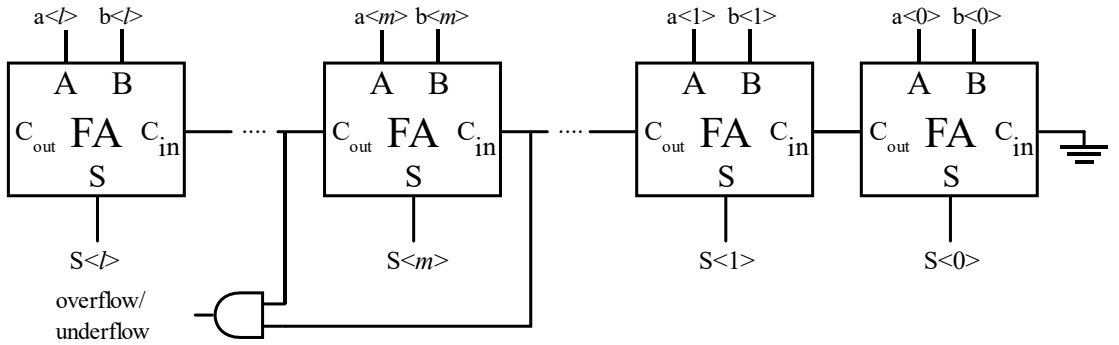
Error detection and correction

- Error detection is simply observing some flag bits in the last accumulation round.
- The magnitude of the cumulative error for some frame *j*

$$E[j]^N = \sum_{i=0}^{j} \binom{i+N-1}{N-1} e[j-i],$$

and for special case where there is only one error present

$$E[j]^N = \pm 2^n \frac{(j+N-1)!}{j!(N-1)!}.$$



Error detection and correction, an example

- If the system parameters are $n = N = 3$, and we want to recover 8-bit HDR image ($m = 8$) from 3-bits, in worst case scenario we need at least eight samples that we can be sure that our result is correct as $E[7]^3 = 288 > 2^8$.
- Briefly, if we observe $R[k] < 0$ or $R[k] > 2^m$, we know that an error is present for some *r*[*i*], where *i* = 0, 1, 2, . . . , *k*, and we start systematically setting $r[k] \coloneqq r[k] \pm 2^n$, until we find some $r[i] \coloneqq r[i] \pm 2^n$, that satisfies $0 \leq R \leq 2^m - 1$.

$$r = [-8,8,-8,0,0,16,-24,16].$$

$$S^3(r) = R = [72,64,48,24,-8,-32,-72,-112], \qquad \text{where } R[-1] = 80$$

< 0

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$$r = [-8, 8, -8, 0, +8, 16, -24, 16].$$

$$S^3(r) = R = [72, 64, 48, 24, 0, -8, -24, -32], \qquad \text{where } R[-1] = 80$$

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$$r = [-8, 8, -8, +8, 0, 16, -24, 16\ ].$$

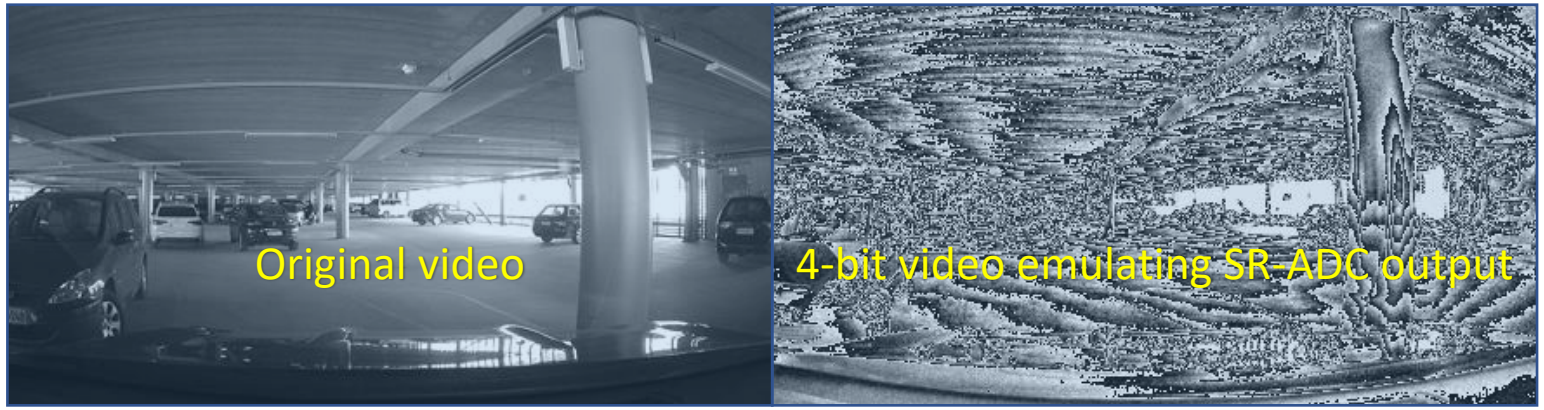
$$S^3(r) = R = [72, 64, 48, 32, 16, 16, 8, 8], \qquad \text{where } R[-1] = 80$$

> 0

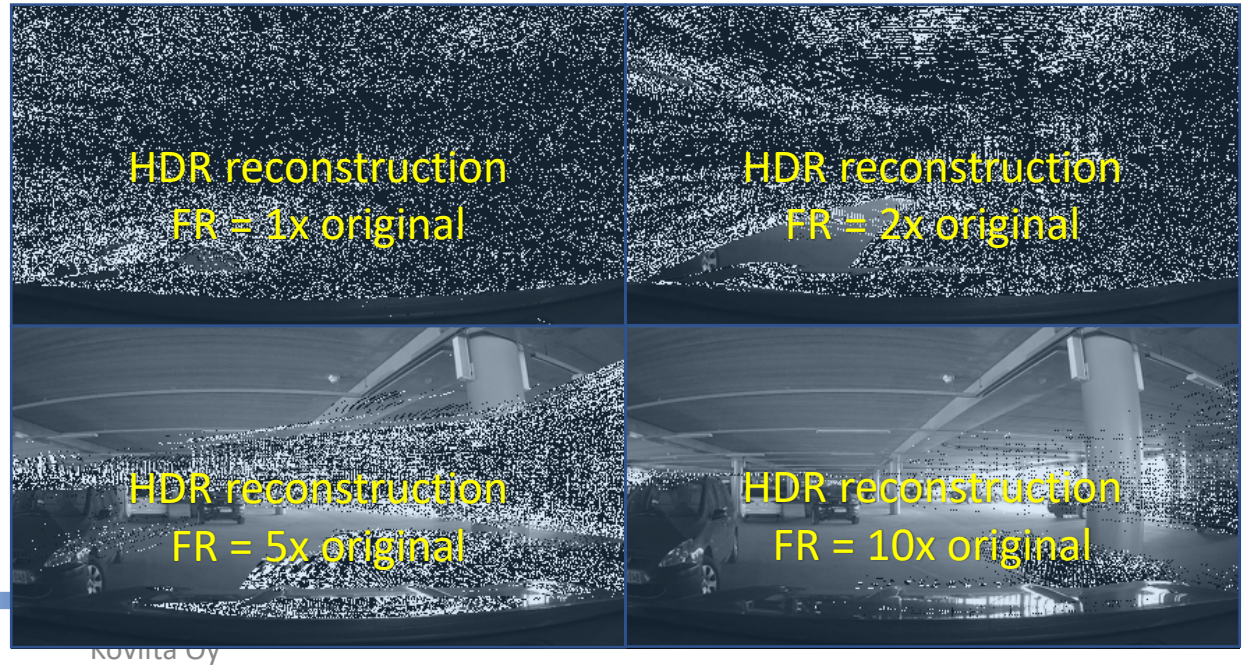
we can assume that our guess was correct thus $r = \hat{r}$.

Example video

- Car driving through parking garage during day (*video1*), **8-bit** grayscale video

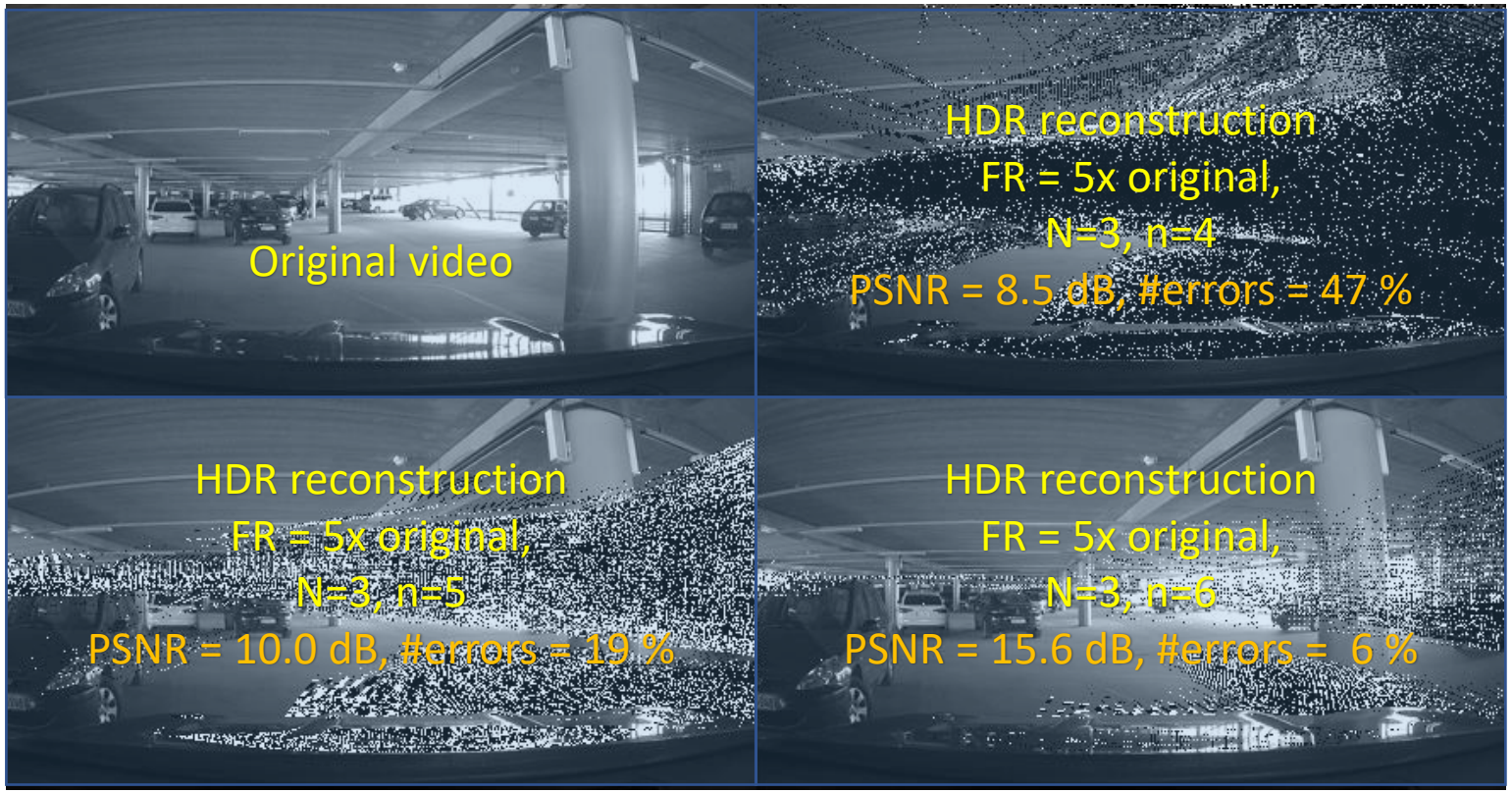


- Emulating the performance of 8-bit HDR reconstruction of different frames rates interpolated from original source video (*video2*)
- **Increased frame rate -> better reconstruction**
- No error correction used in these example videos



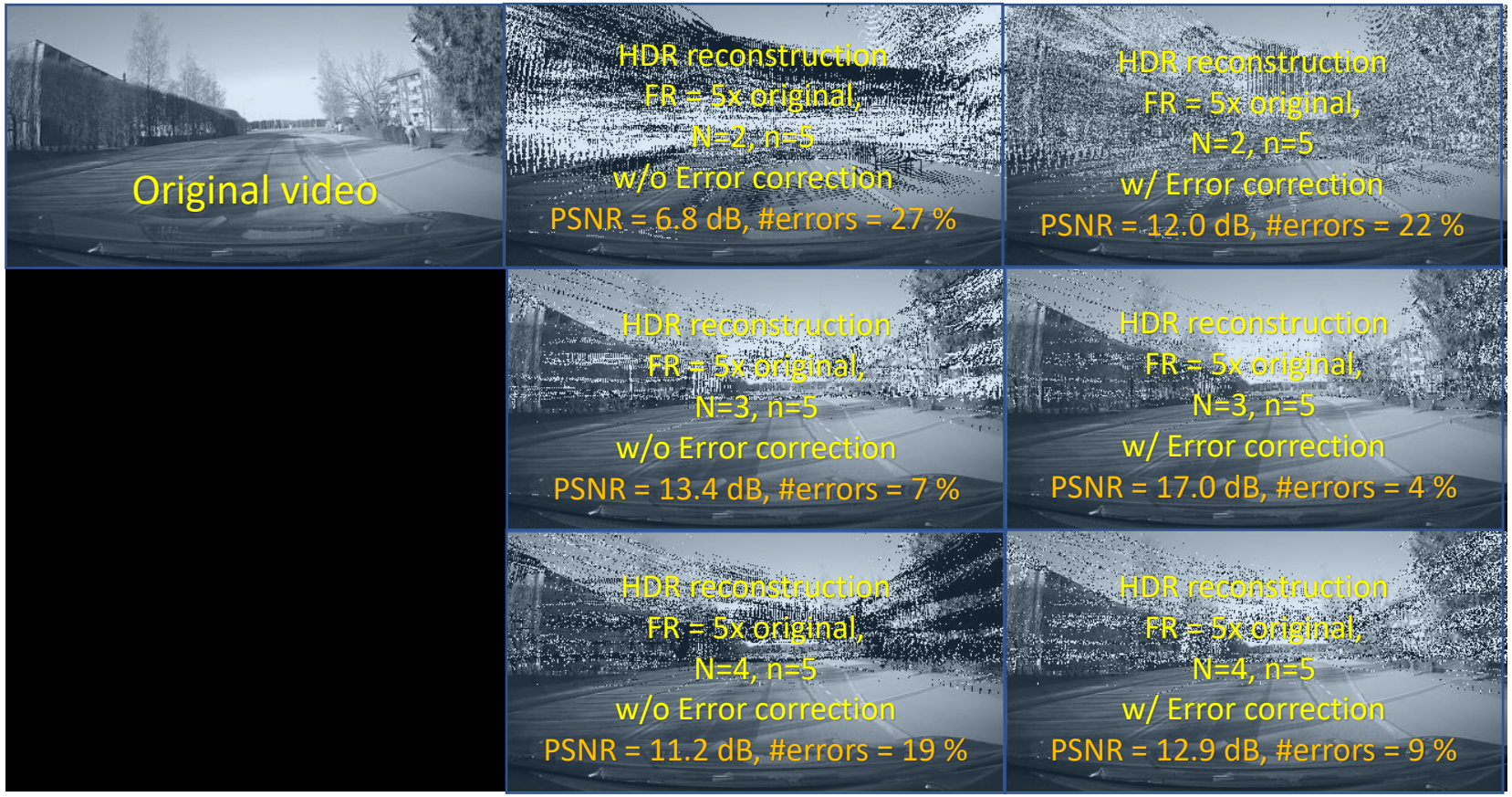
Example video

- Car driving through parking garage during day
- Performance of HDR reconstruction of different amounts of SR-ADC bits (n=4,5,6) (*video3*)
- **More SR-ADC bits -> better reconstruction**
- No error correction used in these example videos



Example video

- Car driving in city streets during day
- Performance of HDR reconstruction with and without error correction, also demonstrations of the choice of *N*=2,3,4 (*video4*)
- **Best performance when *N*=3 and using error correction.**



Conclusions

- We proposed an HDR reconstruction circuit arrangement for SR-ADC samples.
- No need for reset counter in digital pixel readout circuitry, all additional circuitry are outside the pixel array.
- Reconstruction consists of simple bit manipulations, additions and subtractions.
- Due to nonidealities in sampling, some (simple) error correction is needed for improving reconstruction.
- There are limitations of scaling this circuit arrangement.
  - Multiple frames within reconstruction unit must be stored for each individual pixel (if on-chip array parallel operation is considered). This takes additional silicon area thus < 1Mpixel arrays are probably suitable for practical on-chip implementations.
  - Although the reconstruction operations are simple additions/subtractions the actual silicon implementation takes many logical gates thus affecting area and power consumption.
  - The time that reconstruction takes should be faster than frame-rate. This shouldn't be a problem if parallel operation is considered even for very high frame-rates e.g. 1000 FPS.
- The focus of this presentation was to show a truly parallel on-chip circuit arrangement reconstruction. However, off-chip post-processing is also possible (the example videos were made that way).