Low Voltage Low Power CMOS Four-Quadrant Analog Multiplier for Neural Network Applications

Gianluca Colli, F. Montecchi*
Neural Network Design Group - Central R&D
SGS-THOMSON Microelectronics -Via Olivetti 2- Agrate Brianza MI (ITALY)
* Dept of Electrical Engineering - Universiy of Pavia (ITALY)

Abstract-A new low power CMOS four quadrant analog multiplier based on the operation of MOS transistors in linear region is presented. The simulated performances prove that it is possible to achieve an high input to supply ratio without a considerable amount of biasing current. Unlike almost all other designs of Four Quadrant Multiplier in literature, this circuit allows a very low power dissipation (6μW for cell) using both low biasing current (4μA) and a 1.5Vsupply. These properties make this circuit very suitable for ANN applications as a precise weighting synapse and for low power analog signal processing for portable applications.

The circuit achieves an high linearity (less than 40dB of Vina/b=1.5 Vpp@200KHz) and a small area occupied (94μmx88μm with bias section included).

I. INTRODUCTION

Four quadrant analog multiplier are important building blocks in the construction of many signal processing circuits such as correlators, convolvers, adaptive filters and function generators. They are also applied to modulation, frequency translation, PLL, and Automatic Gain Controlling (AGC). In these last years, this particular non linear analog building block has gained more an more importance, especially in the field of Artificial Neural Network as weighting synapse. There are many different approaches for implementing four quadrant analog multiplier in CMOS technology: some of these ones have been realised on a modified Gilbert cell [2], which was originally implemented with bipolar transistors [1], applying the variable trasconductance technique. Others are based on the square-algebraic identity [3,5] that can be easily performed using the square law characteristics of MOS devices working in saturation mode, or on the current-voltage characteristics of MOS devices working in triode region [4].Then other multipliers using the quarter square technique, pulse width modulation technique and Switched Capacitors technique are reported. Recently analog multipliers that take advantage of BiCMOS technology have been presented achieving very good performances in terms of high frequency operations and very low total armonic distortion [6,7]. The main disadvantages of the mentioned circuits, in the light of a possible application in ANN chips, are generally the single cell size and the stand by dissipated power in relationship with wide input range and output linearity, disadvantages that make the greater part of the proposed circuits useless in big synapses arrays in the design of neural network architecture. The new proposed circuital topology may be used, for its intrinsic characteristics, in any applications mentioned above, but, in this case, it has been designed specifically with the requirements for large scale integration, essential for neural networks. The main characteristics kept in mind in the designing has been the modularity, the single cell area, the dynamic range, speed and especially power dissipation. Even if it not important for ANN applications, a good linearity performance is achieved.

II. PRINCIPLE OF OPERATION AND DESIGN OF THE CMOS MULTIPLIER

The proposed multiplier is shown in Fig. 1.

The circuit uses as inputs differential signals [M1- M8] with the same common mode voltage, and the multiplying function is obtained by the difference of the output currents (Iout+ , Iout-).

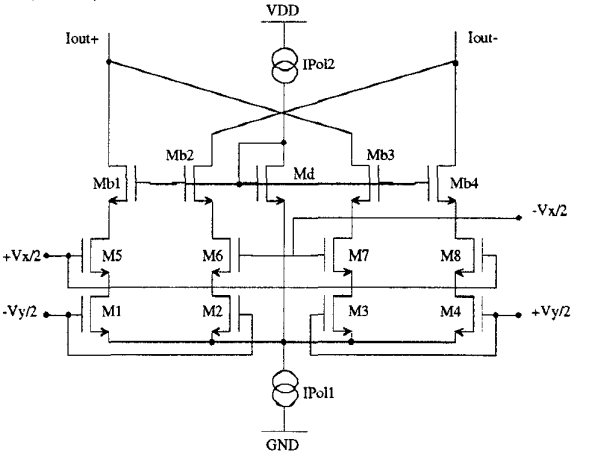

Fig. 1: Full circuit diagram of proposed circuit

It is a single trasconductance stage using four cross-coupled current branches, each one composed of three pipelined n-ch transistors, the first two devices are forced to operate in triode region by a n-ch transistor connected in diode configuration [Md], instead the third one has been sized to work in sub threshold region [Mb1-Mb4] to reduce as well as possible its overdrive voltage and, at the same

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time, to reduce the source impedance at very low current level with the aim to have good current buffers, in comparison with a device operating in saturation mode. The sum of Vds of the first two transistors is established by the overdrive voltage of the diode that is fixed by a biasing current: in this way drain-source voltage of the input transistors are kept ever less than the correspondent overdrive guaranteeing the linear region operation of the devices. To increase the dynamic range of the input devices, they have been sized with a channel length bigger than width. The principle of operation of the multiplier is based on the self-modulation of the Vds of the transistors working in linear region. This effect causes a variation of the equivalent trasconductance of each branch, with the result to achieve an output current from each current buffer depending from both inputs. The second and third order non linearity are removed, or became trascurable, by the mean of the output cross-coupling. Calculating the difference of the output currents, using the I-V equation for Mos transistor in triode, it possible to demonstrate the multiplying function of the circuit. In Fig. 2 a single branch of the multiplier is shown.

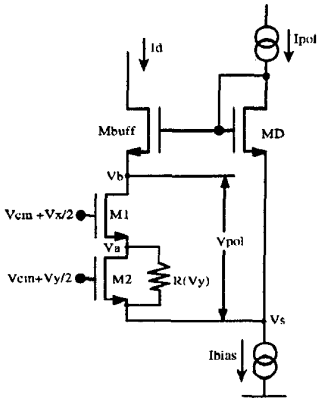

Fig. 2: Single Branch Multiplier schematic

The drain current of an nMOS transistor operating in linear region

$$Id = K\left[(Vgs - Vth)Vds - \frac{Vds^2}{2}\right] \qquad [1]$$

Where K, Vgs, Vds,and Vth are the trasconductance parameter, the gate-to-source voltage, the drain-to-source voltage and the threshold voltage, respectively.

Applying the equation (1) to the structure in Fig. 2, and neglecting the quadratic term (in fact the Vds of the devices, fixed by the overdrive voltage of the diode, results less of a factor 20 respect the corrispective overdrive voltage) results

$$Id = K_1\left[\left(Vcm + \frac{Vx}{2} - Vth - Va\right)(Vb - Va)\right] \qquad [2]$$

Where:

$$Va = Id * R + Vs \qquad Vb = Vpol + Vs$$

and

$$R(Vy) = \frac{1}{K_2\left(\frac{Vy}{2} + Vcm - Vs - Vth\right)} \qquad [3]$$

$$Vpol \approx Vov,\ Md = \sqrt{\frac{Ipol}{Kd}} \qquad [4]$$

Combining the equations (1,2,3,4) the output current of a single branch is obtained

$$Id = K_1 \frac{\left(Vcm + \frac{Vx}{2} - Vth - Vs\right)}{1 + \frac{K_1\left(Vcm + \frac{Vx}{2} - Vth - Vs\right)}{K_2\left(Vcm + \frac{Vy}{2} - Vth - Vs\right)}} \qquad [5]$$

where *Vcm is* input common mode voltage and *Vpol* is the overdrive of the diode. From eqn. (5), making the necessary simplifications and assuming $K_1 = K_2 = K$, and $Vd = Vcm - Vth - Vs$ = constant, the four output currents are derived

$$I\left(\frac{Vx}{2}, \frac{Vy}{2}\right) = K\frac{\left(\frac{Vx}{2} + Vd\right)\left(\frac{Vy}{2} + Vd\right)}{2Vd + \left(\frac{Vx}{2} + \frac{Vy}{2}\right)}Vpol \qquad [6]$$

$$I\left(\frac{Vx}{2}, -\frac{Vy}{2}\right) = K\frac{\left(\frac{Vx}{2} + Vd\right)\left(Vd - \frac{Vy}{2}\right)}{2Vd + \left(\frac{Vx}{2} - \frac{Vy}{2}\right)}Vpol \qquad [7]$$

$$I\left(-\frac{Vx}{2}, \frac{Vy}{2}\right) = K\frac{\left(-\frac{Vx}{2} + Vd\right)\left(\frac{Vy}{2} + Vd\right)}{2Vd + \left(-\frac{Vx}{2} + \frac{Vy}{2}\right)}Vpol \qquad [8]$$

$$I\left(-\frac{Vx}{2}, -\frac{Vy}{2}\right) = K\frac{\left(-\frac{Vx}{2} + Vd\right)\left(-\frac{Vy}{2} + Vd\right)}{2Vd + \left(-\frac{Vx}{2} - \frac{Vy}{2}\right)}Vpol \qquad [9]$$

The difference of the output currents results:

$$\Delta Iout = Iout^+ - Iout^- =$$

$$= \left[I\left(\frac{Vx}{2}, \frac{-Vy}{2}\right) + I\left(\frac{-Vx}{2}, \frac{Vy}{2}\right)\right] - \left[I\left(\frac{-Vx}{2}, \frac{-Vy}{2}\right) + I\left(\frac{Vx}{2}, \frac{Vy}{2}\right)\right] \qquad [10]$$

Substituting eq.(6,7,8,9) in eq. (10) the ΔIout value is obtained:

$$\Delta Iout = KVpol \frac{4Vd^3 - 2Vd\left(Vx^2 + Vy^2\right)}{16Vd^4 - 8Vd^2\left(Vx^2 + Vy^2\right) + \left(Vx^2 - Vy^2\right)^2}[4VxVy] \quad [11]$$

Considering that

$$8Vd\left(Vx^2 + Vy^2\right) >> \left(Vx^2 - Vy^2\right)^2 \quad [12]$$

is valid for every Vx and Vy in the respective input voltage range, and after some calculations and substitutions, the following equation demonstrates the multiplying operation of the proposed circuit:

$$\Delta Iout = K \frac{\sqrt{\frac{Ipol}{Kd}}}{4(Vcm - Vth - Vs)}(VxVy) \quad [13]$$

SIMULATION RESULTS

The proposed circuit has been simulated using the simulator ELDO version 4.1 with LEVEL3 models. The device sizes and bias condition are shown in Tab.1.

It is important to remark that n-ch low threshold devices has been used. Fig.3a plots the DC transfer characteristics of the multiplier with Vb as parameter and sweeping Va input in the 0-2.5 Vpp range. A similar characteristic is obtained with Va is used as parameter (Fig.3b).Fig.4 shows the Total Armonic Distortion (THD) as a function of a sinusoidal Input Voltage with 1.2Vpp amplitude, varying the other differential input (DC) in the range 0 - 2.5Vpp. The Fig.6 shows the simulation of the performance of the multiplier as a frequency doubler. The input signals are two in-phase 10KHz sine wave of 0.5 Vpp and the output is a sine wave of twice of input frequency. The fig.7 demonstrate the use of the multiplier as an amplitude modulator: in the simulation a 5khz sine wave is modulated by a 100khz sine wave. Also the simulated spectrum of the output signal is given. All these simulations has been done using a circuit bias with real current mirror.In Fig.5 the layout of the single cell plus Bias Circuitry is given. In conclusion in Tab.2 all the simulated performances of the new four quadrant analog multiplier are summarised.

Bias Conditions

Vsupply	1.5Vpp
Ibias_pol1	3.5μA
Ibias_pol2	500nA

Device Size

M1-M8	2.5/30
Mb1-Mb4	30/1
Md	5/5
Mpol1	30.8/5
Mpol2	10/2

Tab. 1: Bias Conditions and Device size

Performance of the Multiplier

Power Dissipated	6μW
Vsupply	1.5V
Area for cell	94μm x 64μm
Input Voltage Range	-2.5-2.5 Vpp
THD(at 200Khz)	-40dB
Banwidth for Vx and Vy	600Khz
Output Range(in current)	0-500nA

Tab.2: Performance

CONCLUSION

A new four quadrant analog multiplier for very low power, low voltage application, having a simple configuration, a small size area occupied (94μm x 64μm), and good performances in term of linearity and power comsuption, has been described. The circuit achieves also a wide input voltage range (from -2.5 to 2.5 Peak-to-Peak Voltage) thank to the input devices working in triode region.

The THD of the difference output current is less than -40dB for an 1.5Vpeak to peak sinusoidal input voltage (freq=200KHz) and the other at 1.2Vpp (DC), and the Total Power dissipation is 6μW for each cell with 1.5Vsupply. These properties with the high modularity and small size of the complete cell makes the circuit very suitable for Neural Network Application such as multilayer Perceptron and Hopfield' s network. The circuit has been integrated in a 0.7μm double metal, single poly CMOS process with n-ch and p-ch low threshold transistors.

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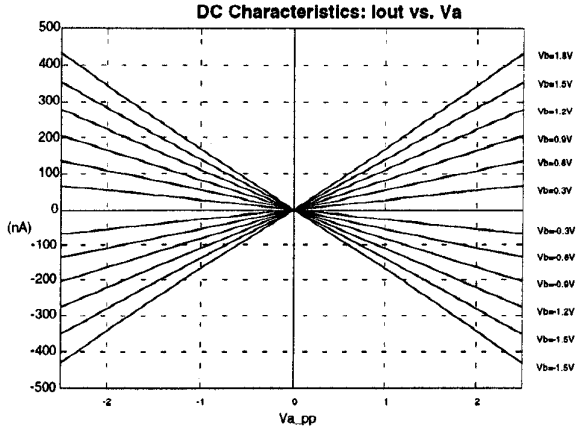

Fig.3a: DC transfert characteristics (Va sweeping in the range -2.5-2.5 Vpp and Vb at fixed values)

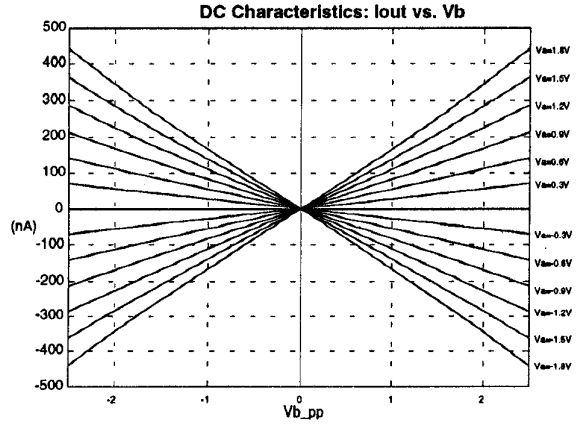

Fig.3b: DC transfert characteristics (Vb sweeping in the range -2.5-2.5 Vpp and Va at fixed values)

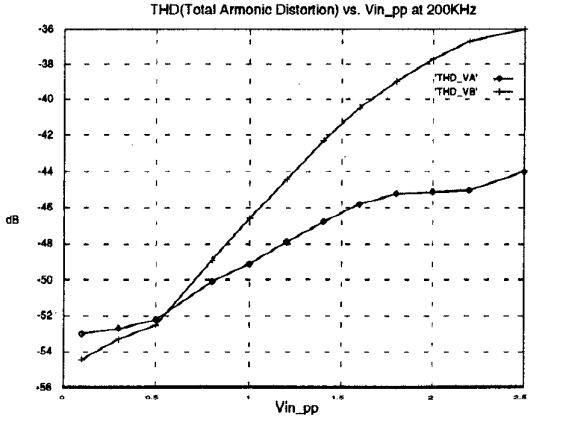

Fig.4:Total Harmonic Distortion Performances

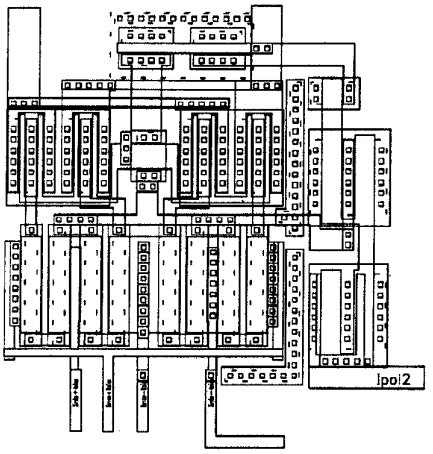

Fig.5: Layout analog Multiplier Cell plus Bias Circuitry

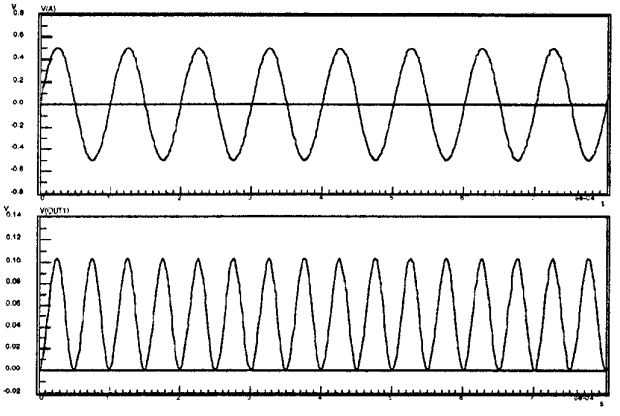

fig. 6 Frequency Doubler Operation (Fs=10KHz, Vpp,in=0.5V)

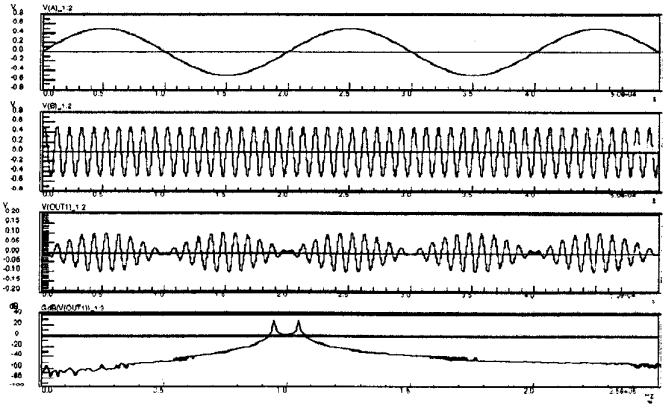

fig.7 AM modulation Example (Fcarry=5KHs, Fs=100KHz)