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# CMOS design of a low power and high precision four-quadrant analog multiplier

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ABSTRACT

In this paper, a novel current-mode Four-quadrant analog multiplier is proposed. The newly designed current squarer circuits and one current mirror which all operate in low supply voltage (2 V) are the basic building blocks in realization of the mathematical equations. The multiplier circuit is designed by using 0.35 μm standard CMOS technology and to validate the circuit performance, the proposed multiplier has been simulated in HSPICE simulator. The simulation results demonstrate a linearity error of 0.17%, a THD of 0.16% in 1 MHz, a −3 dB bandwidth of 485 MHz and a maximum power consumption of 0.232 mW while the static power consumption is 0.111 mW.



## 1. Introduction

Analog multiplier is an important building block for many applications such as adaptive filters, frequency doublers, modulators, neural networks, fuzzy logic controllers, etc. Due to the popularity of CMOS technology, MOS transistors are the first choice for the device fabrication. Therefore, many CMOS analog multipliers which exploit MOS transistors have been presented in the literature. Among the various available methods for implementing a continuous time current-mode analog multiplier, those who utilize transistors operating in saturation or linear [1–6] regions are more prevalent than those who are in sub-threshold [7–10] region. Although in the former method power consumption is higher, the other features like dynamic range of input and output currents, operating frequency and linearity are much better in comparison to the later method. Moreover, class AB current-mode cells are used as the other approach of the multiplier implementation [11,12] where the transconductance parameter of the PMOS and the NMOS transistors should be identical. Otherwise, the output current will not be multiplied correctly and consequently the total harmonic distortion can be a considerable shortcoming. On the other hand, having identical transconductance parameter is very difficult, because its value is strongly depended on the fabrication process and varies lot by lot [3]. By using saturated transistors, we can use the inherent square-law characteristic of MOS transistors in saturation region, which are utilized for construction of current-mode squarer and square root circuits. Thus, multipliers can take the advantage of either square root circuits [5,6,13–15] or squarer circuits [4,16–18] in their structures.

In this paper, squarer circuits have been used. Since the current squarer circuit is the core cell of the multiplier circuit, it is considered as the main element in determining of the multiplier functionality level. Hence, we present a low power, high speed and high precision four-quadrant current-mode analog multiplier circuit based on a newly designed current squarer circuit. The circuit works under supply voltage of VDD = 2 V. The squarer circuit has been designed based on the square-law characteristic of an MOS transistor operated in the saturation region. Proposed multiplier is composed of four squarer cells and a current mirror so that it has a symmetrical structure and results a low harmonic distortion. Simulations are performed by HSPICE simulator and results imply that high linearity, high speed, wide bandwidth and low power dissipation are the main advantages of proposed multiplier.

## 2. Circuit description

### 2.1. Current-mode squarer circuit

Squarer circuits are widely used in communication systems and measurements such as frequency doublers, peak amplitude detector and analog multipliers. Square circuits can be categorized into three groups proportional to the type of their input signals: voltage-mode [19,20], current-mode [3,4,16,21–23] and mixed signals [24]. One of the most effective methods in decreasing power dissipation is lowering supply voltage level, but designing in this situation is

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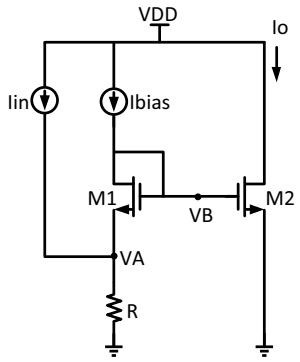


**Fig. 1.** Proposed current squarer circuit.

more difficult. Lowering the voltage level means limiting the output swing (range) which leads to a limited input range in its turn. Therefore, the utilized squarer should be capable of operating properly under the determined voltage level. Because of working in current-mode, at first we review some squarer circuits that have been presented in the previous works. Despite of working in a low level voltage (±0.7 V and 0.9 V) [21,23] operate in sub-threshold region and have a restricted input and output ranges [3,4,16] have an adequate input and output ranges, but their supply voltages are 5 V, 3.3 V and ±1.5 V, respectively. Ref. [22] suffers neither from small input and output ranges nor high supply voltage level, but it is comprised of 10 transistors which leads to a larger area and can confine the bandwidth whenever it is used in a multiplier structure. Fig. 1 illustrates the proposed current squarer circuit while the power supply is VDD = 2 V. This circuit consists of two transistors which both of them are in saturation region.

A suitable constant current passes through M1 (*Ibias*) so that any changes in the voltage of node (*A*) will occur in the voltage of node (*B*) as well. The current of *M*2 can be expressed as:

$$Io = K_2(V_B - V_{t2})^2 \quad (1)$$

where $K = 0.5\,\mu$ COX $(W/L)$ is transconductance parameter of transistor, $\mu$ is the electron mobility, COX is the gate oxide capacitance per unit area, $W/L$ is the transistor aspect ratio, $V_B$ and $V_{t2}$ are gate-source and threshold voltages of *M*2. Voltage of node (*A*) is given by

$$V_A = R(Iin + Ibias) \quad (2)$$

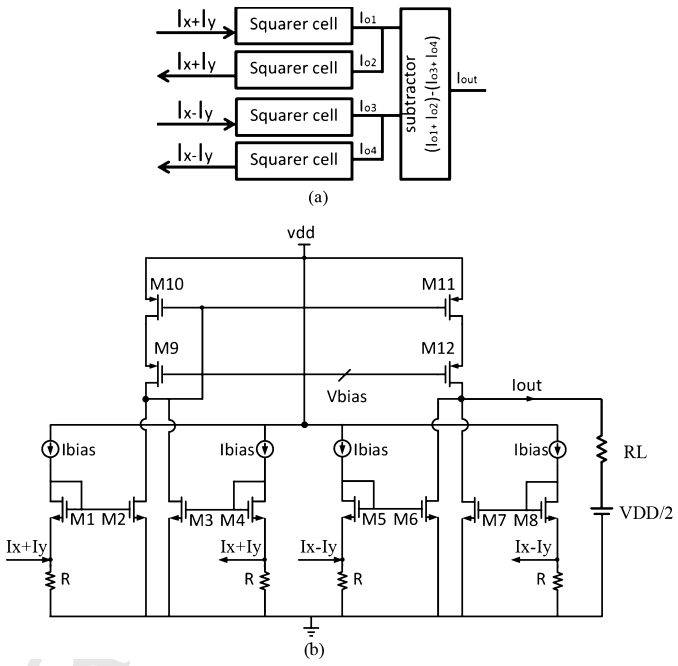


**Fig. 2.** Proposed multiplier structure (a) block diagram and (b) circuit level.

*Iin* is the current input signal and *Ibias* is a suitable constant current which sets the initial voltage of node (*B*) (i.e. $V_0$ when $Iin = 0$). Voltage of node (*B*) is

$$V_B = R(Iin + Ibias) + V_{t1} + \sqrt{\frac{2Ibias}{K1}} \quad (3)$$

$$V_0 = RIbias + V_{t1} + \sqrt{\frac{2Ibias}{K1}} \quad (4)$$

$$V_E = V_0 - V_{t2} \quad (5)$$

According to above equations, Eq. (1) will be changed into Eq. (6).

$$Io = k(RIin + V_0 - V_{t2})^2 = k(RIin + V_E)^2 \quad (6)$$

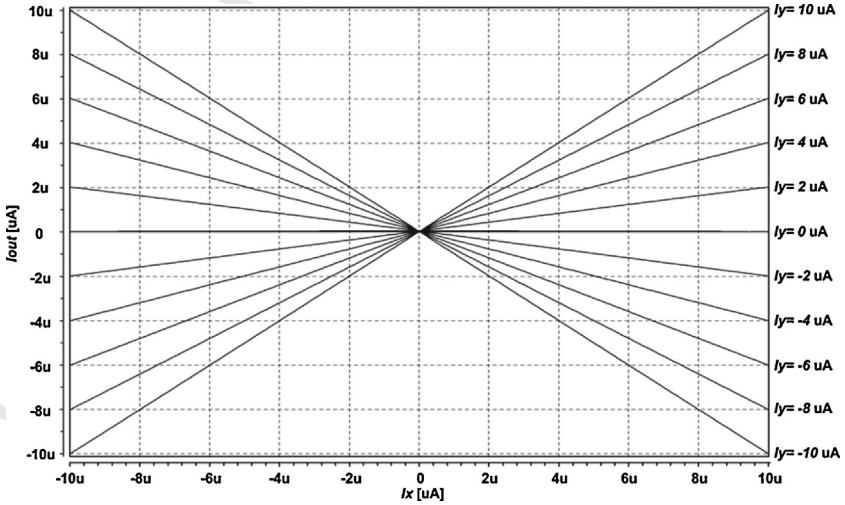


**Fig. 3.** DC transfer characteristic of proposed four-quadrant multiplier.

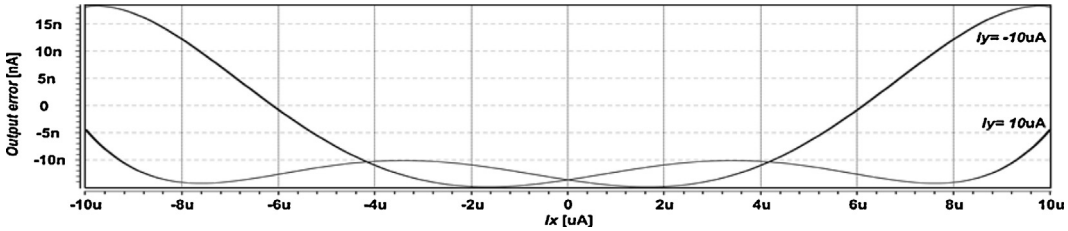


**Fig. 4.** Linearity error when $I_Y = \pm 10\,\mu A$.

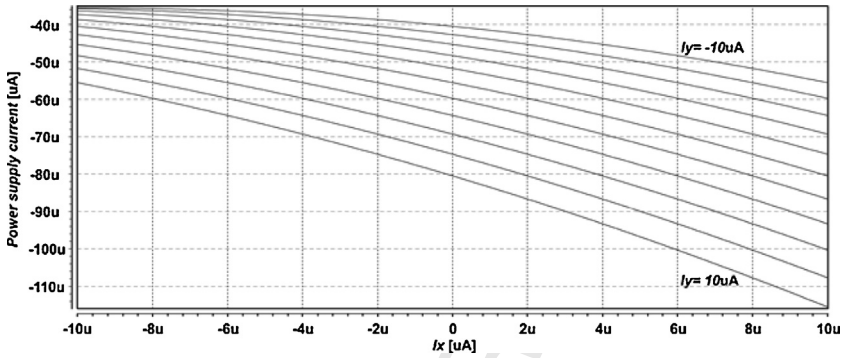


**Fig. 5.** Drained currents from power supply (VDD).

### 2.2. Multiplier circuit

To implement the proposed multiplier, four numbers of squarer cells are required in its structure. According to Eq. (6), if $I_X + I_Y$, $-(I_X + I_Y)$, $I_X - I_Y$ and $-(I_X - I_Y)$ are applied as their input currents, the output currents of these circuits will be

$$Io1 = k(R(I_X + I_Y) + V_E)^2 \tag{7}$$

$$Io2 = k(-R(I_X + I_Y) + V_E)^2 \tag{8}$$

$$Io3 = k(R(I_X - I_Y) + V_E)^2 \tag{9}$$

$$Io4 = k(-R(I_X - I_Y) + V_E)^2 \tag{10}$$

The output current of multiplier is given by subtracting the summation of $Io1$ and $Io2$ from summation of $Io3$ and $Io4$ as follows:

$$Iout = (Io1 + Io2) - (Io3 + Io4) = 8kR^2 I_X I_Y \tag{11}$$

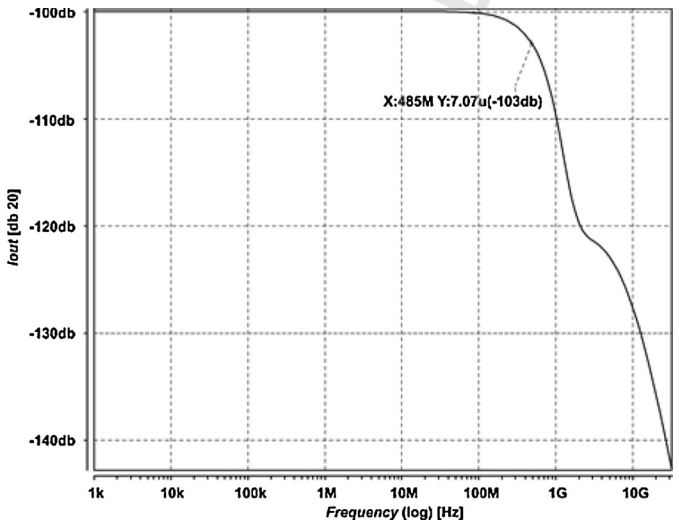


**Fig. 6.** AC characteristic of proposed multiplier.

This idea is shown schematically in the form of block diagram and transistor level structure in Fig. 2.

### 2.3. Analysis of the performance of multiplier

In this section, the effects of various mismatches which can be caused by process variations have been surveyed on the performance of proposed multiplier.

#### 2.3.1. Input current mismatch

Assume that both of the input currents ($I_X$ and $I_Y$) are different from the ideal desired value and are defined as follows:

$$I_X = I_{xidael} + \Delta I_{xidael} \tag{12}$$

$$I_Y = I_{yidael} + \Delta I_{yidael} \tag{13}$$

$$\Delta = \frac{n}{100} \tag{14}$$

Substituting Eqs. (12) and (13) into Eq. (11) results in

$$\begin{aligned} Iout &= 8kR^2(I_{xidael} + \Delta I_{xidael})(I_{yidael} + \Delta I_{yidael}) = 8kR^2 I_{xidael} I_{yidael} \\ &\quad + 8kR^2(I_{xidael}\Delta I_{yidael} + I_{yidael}\Delta I_{xidael} + \Delta I_{xidael}\Delta I_{yidael}) \\ &= 8kR^2(I_{xidael} I_{yidael} + I_{Error}) \end{aligned} \tag{15}$$

Whenever input signals are $I_{xidael} = I_{yidael} = A$, $I_{Error}$, will be

$$I_{Error} = \frac{2nA^2}{100} + \left(\frac{nA}{100}\right)^2 \tag{16}$$

In this equation the second term is much smaller than the first term and can be ignored, so for 1% mismatch ($n = 1$) the percentage of output error is

$$Error = \frac{I_{Error}}{Iout} \times 100 = 2n\% = 2\% \tag{17}$$

Note that obtained error is for the worst case when the mismatch of $I_X$ and $I_Y$ both are in a similar direction.

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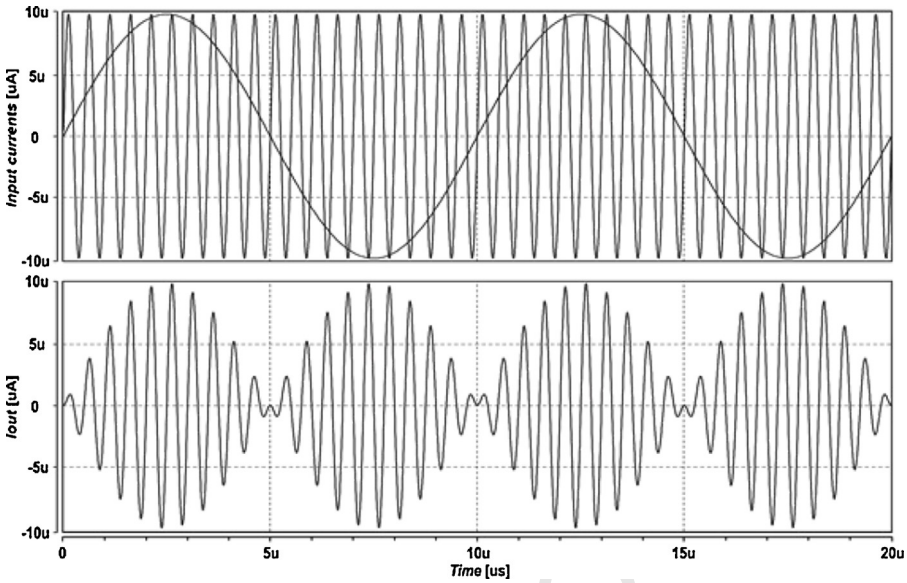


**Fig. 7.** Multiplier as a modulator.

### 2.3.2. Threshold voltage mismatch

According to Eq. (5), $V_E$ is a function of $V_{th}$. Thus, the variation of threshold voltage will change the value of $V_E$. $V_E$ is a common parameter for the squarer cells which are used in multiplier circuit. Consequently, by symmetrical structure of proposed multiplier $V_E$ is eliminated in Eq. (11) and will not appear in the output current. In addition, the threshold voltage variation changes the initial value of node ($B$) (i.e. $V_0$) as shown in Eq. (4). Therefore, to preserve the accuracy of output current in an acceptable level, the value of $V_0$ must be fixed in its initial value by adjusting the bias current value ($Ibias$) so that by increasing the threshold voltage, the bias current should be decreased and vice versa.

### 2.3.3. Transconductance parameter mismatch

In the ideal case, *M2, M3, M6* and *M7* have identical dimensions and are match. But now, assume that the transconductance for *M2* and *M7* is *K*2 and for *M3* and *M6* is *K*1 where

$$k2 = k1 + \Delta k1 \tag{18}$$

In this condition, the output current is obtained by Eq. (19).

$$\begin{aligned} Iout_{real} &= 4(k1 + k2)R^2 I_X I_Y = 4(2k1 + \Delta k1)R^2 I_X I_Y = 8k1R^2 I_X I_Y \\ &\quad + 4\Delta k1 R^2 I_X I_Y = 8k1R^2 I_X I_Y + \frac{4nK1}{100} R^2 I_X I_Y \\ &= Iout_{ideal} + I_{Error} \end{aligned} \tag{19}$$

According to Eq. (19), the percentage of output current error caused by transconductance mismatch can be calculated as follows:

$$Error = \frac{I_{Error}}{Iout} \times 100 = \frac{nI_X I_Y}{200 I_X I_Y} = \frac{n}{200}\% \tag{20}$$

For 1% mismatch ($n = 1$) the percentage of output error is 0.5%.

The low input and high output impedances cause good impedance conformity for current-mode circuits. The input and output impedances of proposed multiplier are

$$Rin = (R||\infty) = R \tag{21}$$

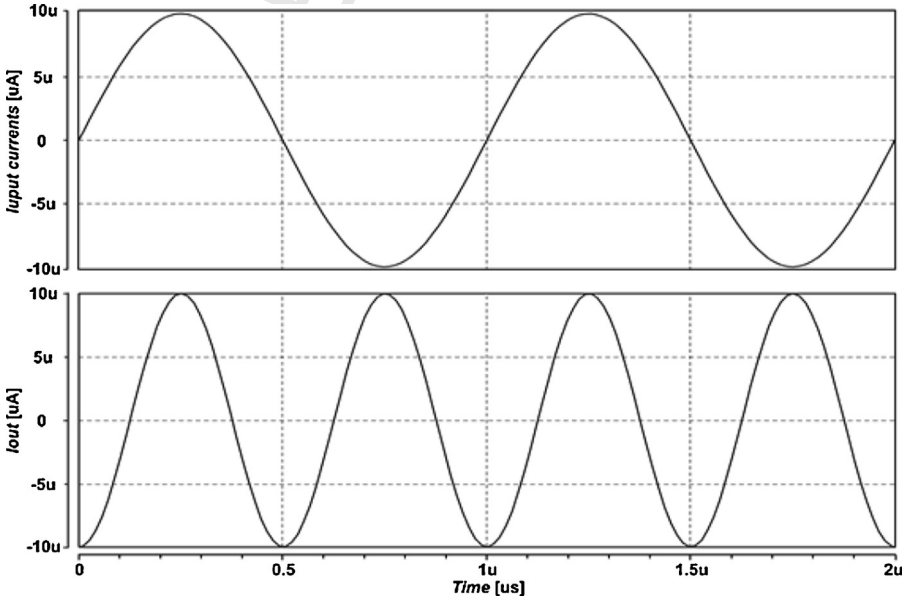


**Fig. 8.** Multiplier as a frequency doubler.

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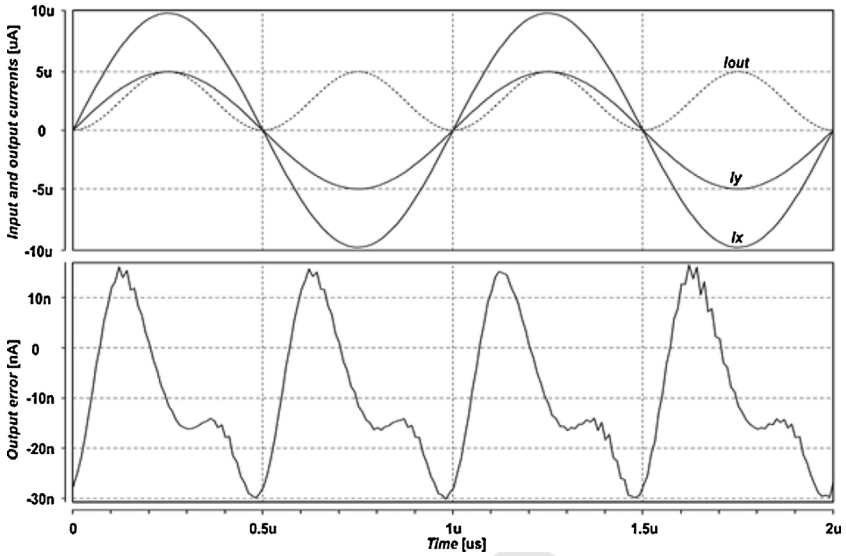


**Fig. 9.** Simulation of multiplier for transient error measurement.

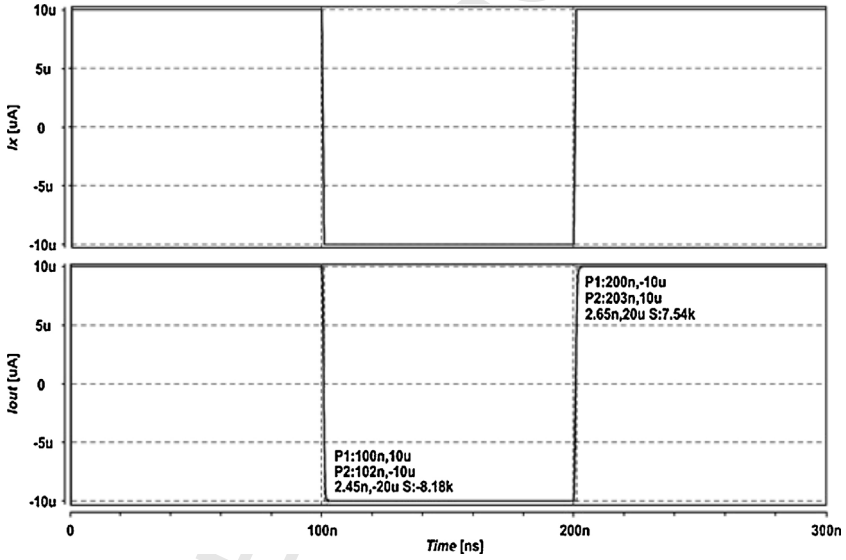


**Fig. 10.** Pulse response of multiplier.

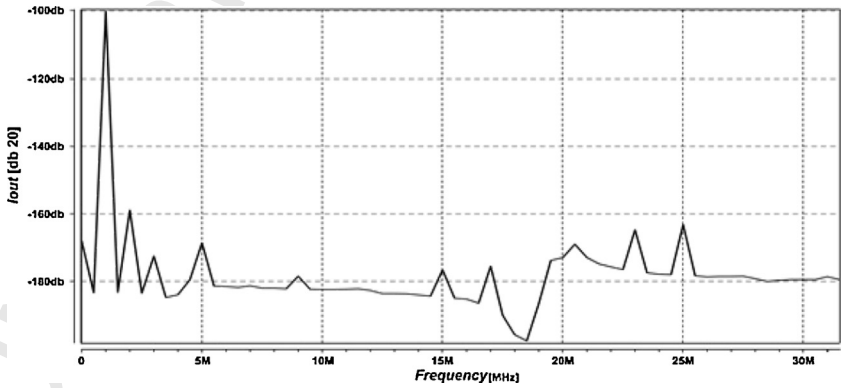


**Fig. 11.** Output spectrum of multiplier.

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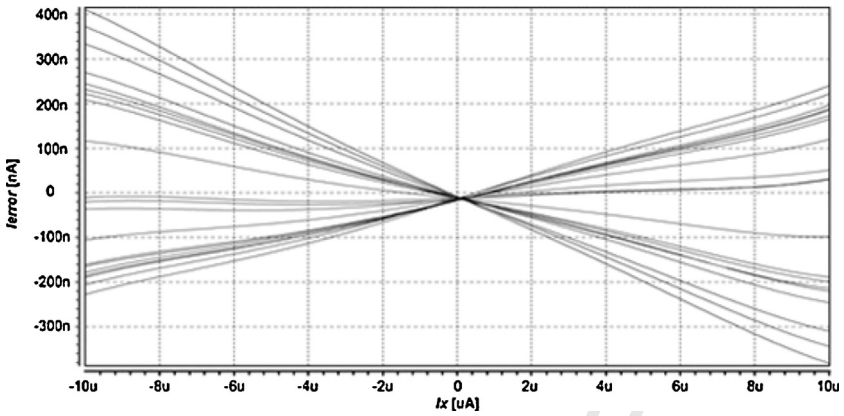


**Fig. 12.** Output error due to Monte Carlo analysis for transconductance parameter variations.

**Table 1**
Sizes of the transistors used in the proposed current-mode multiplier.

| Transistors | Aspect ratio $W/L$ (μm/μm) |
|---|---|
| M2, M3, M6, M7 | 1.4/1 |
| M1, M4, M5, M8 | 1/1 |
| M9, M10, M11, M12 | 6/0.5 |

**Table 2**
The total harmonic distortion (THD) versus input signal ($I_X$) peak to peak amplitude at different frequencies.

| Amplitude | 10 kHz | 100 kHz | 1 MHz | 10 MHz |
|---|---|---|---|---|
| ±5 μA | −61.5 db | −59.2 db | −56.8 db | −44.8 db |
| ±10 μA | −58.9 db | −56.9 db | −55.8 db | −43.7 db |
| ±15 μA | −46.8 db | −46.7 db | −46.5 db | −41.2 db |

$$Rout = (rds6||rds7) + rds12(1 + gm12\,rds11) \quad (22)$$

## 3. Simulation results

In this section, to validate the functionality of the proposed multiplier various kinds of simulations are performed. The simulation results are given using HSPICE with 0.35 μm CMOS parameters while power supply voltage VDD is 2 V. In squarer cell R and *Ibias* are 12 kΩ and 4.6 μA while RL is 1 kΩ. The aspect ratios of the transistors are inscribed in Table 1. Fig. 3 shows the simulated DC transfer characteristic of the multiplier when $I_X$ is continuously swept from −10 μA to 10 μA and $I_Y$ steps from −10 μA to 10 μA with 2 μA step size. Fig. 4 illustrates linearity error within the ±10 μA input range ($I_X$) when $I_Y = \pm 10$ μA and indicates that linearity error is less than 0.17% of full scale current (20 μA).

To study the power efficiency of proposed circuit, drained currents from VDD are shown in Fig. 5. According to Fig. 5, the maximum power dissipation is 232 μW when $I_X$ and $I_Y$ are 10 μA (drained current = 116 μA). However, the quiescent power consumption is 111 μW when $I_X$ and $I_Y$ are zero (drained current = 55.5 μA). The frequency characteristic of the multiplier where $I_Y$ is set to 10 μA DC and $I_X$ is the AC-varying signal with 10 μA magnitude, is shown in Fig. 6 and exhibits a −3 dB bandwidth of 485 MHz. Fig. 7 demonstrates the use of the multiplier as an analog amplitude modulator where $I_X$ is the sinusoidal modulating signal with magnitude equal to ±10 μA and frequency ($Fx$ = 100 kHz) while $I_Y$ is the sinusoidal carrier with amplitude equal to ±10 μA and frequency ($Fy$ = 2 MHz). Fig. 8 shows the use of the multiplier as a frequency doubler where both $I_X$ and $I_Y$ are sinusoidal signals with magnitude equal to ±10 μA and frequency ($F$ = 1 MHz).

In order to study the linearity error in a transient condition and to do an equitably comparison with [4,17], another simulation in which the input current are similar to the currents used in [4,17], was performed. The simulation result is displayed in Fig. 9 revealing a linearity error of 0.24% which is smaller than referred works. Fig. 10 shows the pulse response of multiplier where $I_Y$ is set to 10 μA and $I_X$ is a pulse with amplitude equal to ±10 μA and frequency ($Fx$ = 5 MHz). Proportional to the variation of $I_X$, the settling times are 2.65 ns and 2.45 ns for raising and falling edges, respectively. Fig. 11 shows the spectrum of the output current when $I_Y$ is fixed at 10 μA and $I_X$ is a 1 MHz sinusoidal with peak to peak amplitude of ±10 μA and indicates that the other harmonic components are about 60 dB below the fundamental component. Monte Carlo analysis is usually utilized to model random mismatches between different components due to process variation. Figs. 12 and 13

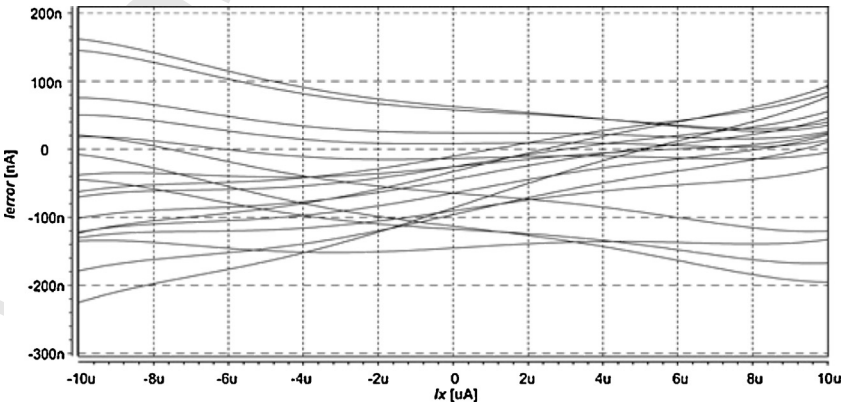


**Fig. 13.** Output error due to Monte Carlo analysis for threshold voltage variations.

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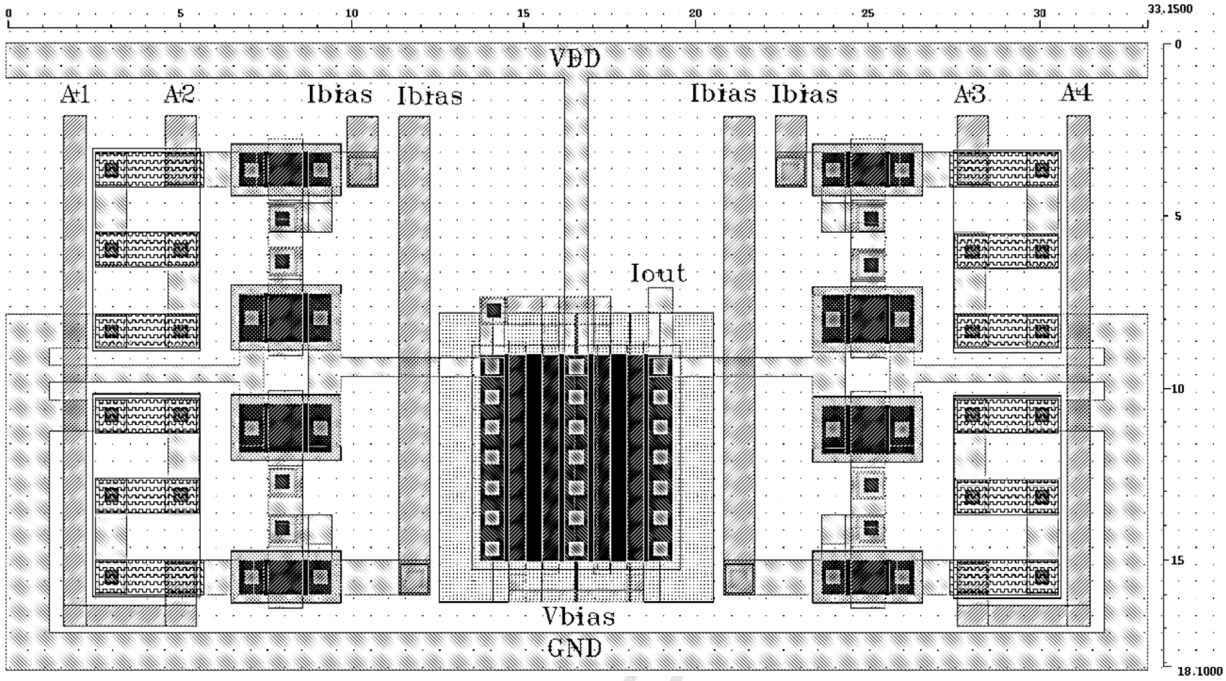


**Fig. 14.** Layout of proposed multiplier.

**Table 3**
Comparison between this work and previous works.

| Reference | Technology (μm) | Supply voltage (V) | Input range (μA) | Output range (μA) | Linearity error (%) | THD,1 MHz 20 μA (%) | Power consumption (μW) | Chip area ($\mu m^2$) | −3 db bandwidth (MHz) |
|---|---|---|---|---|---|---|---|---|---|
| [3] | 2 | 5 | ±20 | ±5 | 1.22 | 1.54 | 930 | – | 22.4 |
| [4] | 0.35 | 3.3 | ±10 | ±10 | 1.1 | 0.97 | 340 | 872 | 41.8 |
| [5] | 2.4 | 5 | 100 | 100 | 1.2 | 1 (10 kHz) | 700 | $32 \times 10^4$ | 12.3 |
| [14] | 0.35 | 3 | 10 | 20 | – | 0.14 | – | $10^4$ | 44 |
| [16] | 0.5 | ±1.5 | ±60 | ±7 | 3.9 | 4.485 | 720 | – | 31 |
| [17] | 0.25 | 3.3 | ±10 | ±10 | 0.56 | 0.96 | 214.5 | 234.9 | 533 |
| [25] | 0.5 | ±1.5 | ±20 | ±10 | 1.2 | 3.7 | 460 | – | 19 |
| [26] | 0.8 | 1.5 | ±15 | ±10 | – | 0.9 | (1 kHz) | 184 | 5.5 |
| [27] | 0.18 | 1.2 | 10 | 40 | 0.75 | – | 60 | 600 | 79.6 |
| [28] | 0.5 | ±1.5 | ±50 | ±25 | 0.9 | 0.44 (20 kHz) | 600 (static) | – | 205 |
| [29] | 0.25 | 1.5 | ±200 | ±40 | 0.8 | 0.25 | – | – | 154 |
| [30] | 0.35 | ±0.75 | ±20 | ±20 | – | 0.83 (10 MHz) | – | $186 \times 10^2$ | 140 |
| This work | 0.35 | 2 | ±10 | ±10 | 0.17 | 0.16 | 232 | 594 | 485 |

clarify that the maximum linearity error is less than 4% and 2% when the Monte Carlo analysis is performed for transconductance parameter and $V_{th}$, respectively. The total harmonic distortion (THD) versus input signal ($I_X$) peak to peak amplitude at 10 kHz, 100 kHz, 1 MHz and 10 MHz is shown in Table 2 when $I_Y$ is 10 μA. Table 2 makes it clear that the THD is much better in this work than the previous works. This THD improvement originates from the symmetrical structure of proposed multiplier.

A comprehensive comparison between the performance of multipliers reported in the previous works and proposed multiplier is presented in Table 3. Based on this comparison, especially with those works have been designed in a similar process (0.35 μm), features like small linearity error, low harmonic distortion, wide bandwidth, high speed and low power consumption can be cited as the advantage of proposed multiplier.

## 4. Conclusion

A current-mode four-quadrant multiplier based on a newly designed squarer circuit was proposed. The simulation results indicate that the symmetrical configuration of proposed circuit allows us to achieve a high linearity. The other advantages of proposed circuit were verified by various simulation results. The layout of this circuit which is depicted in Fig. 14 has been drawn by Cadence Virtuoso software and illustrates that the occupied area is about 594 $\mu m^2$.

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