A Low-Power CMOS Analog Multiplier

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***Abstract*—A multiplier is an important component for many analog applications. This paper presents a low power CMOS analog multiplier with performance analysis and design considerations. Experiments with SPICE simulation and results from chip testing show that this new structure has extremely low power consumption with comparable linearity and noise performance, making it very attractive for use in a variety of analog circuits.**

***Index Terms*—Analog integrated circuits, analog multipliers, CMOS, low-power design.**

I. Introduction

AN ANALOG multiplier is an important subcircuit for many applications such as adaptive filters and frequency modulators [1]–[10]. It is intended to perform a linear product of two continuous signals x and y, yielding an output $z = Kxy$, where K is a constant with suitable dimension. Driven by the early work of *Gilbert* [11], a variety of multipliers have been designed for different optimization objectives [3]–[10]. A general idea behind these designs is to use electronic devices to process the input signals, followed by a cancellation/minimization of errors caused by nonlinearity of the devices. Due to the popularity of advanced CMOS technology, MOS transistors are a natural choice for the devices, while differential circuit structure is widely used for nonlinarity cancellation [3], [13]. The readers are referred to [7] for recent survey on MOS multipliers.

In this paper, we present a new multiplier with CMOS structure with emphasis on low power consumption. We analyze various performance metrics of the multiplier and provide some design considerations. It is demonstrated in particular that this multiplier is much better than other structures in terms of power consumption, and is hence especially suitable for implementation of large-scale circuits.

II. Multiplier Structure

For CMOS analog multiplier design, most transistors are biased to operate in the saturation region where the drain current I_D of the device is given by [14]

$$I_D = \frac{1}{2}K(V_{\rm GS} - V_{\rm TH})^2(1 + \lambda V_{\rm DS}) \tag{1}$$

where $K = \mu_o C_{\rm ox} W/L$ is the transconductance parameter, $V_{\rm TH}$ the threshold voltage of the device, and λ the channel-length modulation effect for long channel devices. It can be seen that in the saturation region, low power consumption requires a small value of $V_{\rm GS}$ which leads to a reduced input range. By biasing the transistors to operate in the linear region instead, one can reduce the drain current while keeping a relatively large input range. The drain current in linear region is given by [14]

$$I_D = K\left[(V_{\rm GS} - V_{\rm TH})V_{\rm DS} - \frac{1}{2}V_{\rm DS}^2\right]. \tag{2}$$

Since $V_{\rm GS} - V_{\rm TH} > V_{\rm DS}$ in linear region, the overdrive voltage can be biased to increase the input range. The drain current can remain a proper value by decreasing $V_{\rm DS}$, keeping the power dissipation at same level. Considering the fact that pMOS transistors need less drain current with larger overdrive voltage $(V_{\rm GS} - V_{\rm TH})$ compared with nMOS transistors, pMOS transistors are preferably chosen in the input terminals for operations in either saturation or linear region.

Our basic idea in designing low-power multipliers is to fit most transistors into linear region and use pMOS devices to operate in saturation region. Fig. 1 shows the proposed CMOS multiplier structure which consists of 4 pMOS transistors ($P1$–$P4$) operating in saturation region and 8 nMOS transistors ($N1$–$N4$ and $M1$–$M4$) operating in linear region. Throughout the paper, the upper case letters, X and Y, represent common-mode (dc bias) components, while the lower case letters, x and y, represent small (input) signals. Assuming that all transistors in Fig. 1 are biased to operate in proper (linear or saturation) region, we can prove that this topology achieves multiplication, i.e.,

$$V_{01} - V_{02} \propto \frac{K_P}{K_N K_M}xy. \tag{3}$$

A potential advantage of this structure is that a larger input range can be obtained with only pMOS transistors in their saturation region. In other words, for the same input range, a lower supply voltage can be used. The transistors $P1$–$P4$ in saturation region reduce $V_{P1} - V_{P4}$, pushing up the input range for signal y.

For a given DC bias, the output range of the multiplier also depends on $K_P/(K_N K_M)$ which has a maximum value in order to keep $M1$–$M4$ and$N1$–$N4$ in linear region. While exhibiting the ability of canceling nonlinearity, the circuit still has a linearity error due to temperature, body effect of transistors $N1$–$N4$, and possible device mismatches.

The required bias conditions for Fig. 1 can be written as

$$V_P - |V_{\rm THP}| \le X \pm x \le V_{\rm DD} - |V_{\rm THP}|, \qquad \text{for } P1\text{–}P4 \tag{4}$$

$$Y \pm y \ge V_O + V_{\rm THN}, \qquad \text{for } N1\text{–}N4. \tag{5}$$

The bias voltage of $M1$–$M4$ is chosen to be $V_{\rm DD}$ in order to keep V_P as low as possible, allowing $P1$–$P4$ for a larger input

Manuscript received March 18, 2005; revised June 1, 2005. This work was supported in part by the National Sciences and Engineering Research Council of Canada (NSERC) under Grant 249499-02. This paper was recommended by Associate Editor T. Saito.

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Digital Object Identifier 10.1109/TCSII.2005.857089

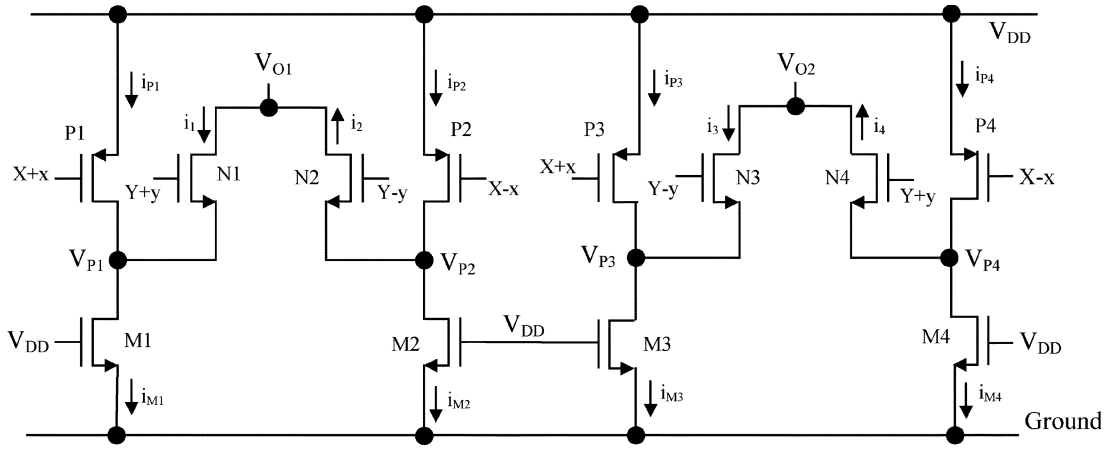

Fig. 1. Proposed multiplier topology.

range. Typical values to be used are: $V_{\rm DD} = 1.5$ V, $X = 0.5$ V, $Y = 1.5$ V, $V_{\rm THP} = 0.75$ V, and $V_{\rm THN} = 0.6$ V. For instance, when all transistors have same size of $W/L = 0.8\ \mu$m/0.35 μm with $x = y = 0$, both V_{O1} and V_{O2} turn out to be 16.1 mV.

III. Quantitative Analysis and Verification

The performance metrics for multipliers include linearity, input range, chip area cost, power consumption, frequency range, and noise. Depending upon applications, some of them can be more important than others. Also, it is not uncommon that some metrics need to be traded for others. For instance, as the power consumption of a multiplier is to be optimized, its linearity performance tends to get worse. This requires a reasonable tradeoff between the two. In this section, we give a quantitative analysis on power consumption and noise for the proposed multiplier, which is verified by the *Spectre Simulator* from the *Cadence* tool.

A. Power Consumption

Given a constant supply voltage, the power consumption of Fig. 1 can be estimated by looking at the total output current which is given by $i_{\rm total} = i_{P1} + i_{P2} + i_{P3} + i_{P4}$, i.e.,

$$\begin{aligned} i_{\rm total} &= \frac{1}{2}K_P(V_{\rm DD} - X - x - |V_{\rm THP}|)^2[1 + \lambda(V_{\rm DD} - V_{P1})] \\ &\quad + \frac{1}{2}K_P(V_{\rm DD} - X + x - |V_{\rm THP}|)^2[1 + \lambda(V_{\rm DD} - V_{P2})] \\ &\quad + \frac{1}{2}K_P(V_{\rm DD} - X - x - |V_{\rm THP}|)^2[1 + \lambda(V_{\rm DD} - V_{P3})] \\ &\quad + \frac{1}{2}K_P(V_{\rm DD} - X + x - |V_{\rm THP}|)^2[1 + \lambda(V_{\rm DD} - V_{P4})]. \end{aligned} \tag{6}$$

Since $V_{P1} \sim V_{P4}$ are very small compared with the input signals (if the circuit is properly biased), we have the following approximate result:

$$i_{\rm total} \propto 2K_P[(V_{\rm DD} - X - |V_{\rm THP}|)^2 + x^2]. \tag{7}$$

This indicates that the power consumption has nothing to do with signal y and dc bias Y for transistors N1–N4.

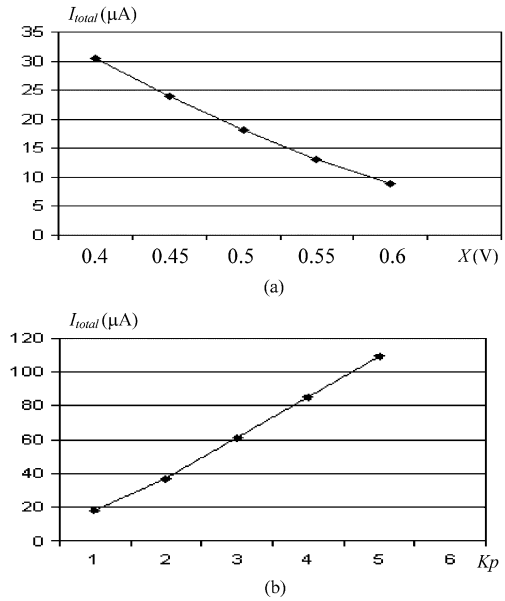

Fig. 2. Total current with respect to (a) X and (b) K_P (with $W/L = 0.8\ \mu$m/0.35 μm).

The simulation results for the total current in Fig. 1 with respect to X and K_P (with uniform transistor size of $0.8\ \mu$m/$0.35\ \mu$m) are shown in Fig. 2(a) and (b) with both x and y being 0.2 V.

B. Noise

Noise is another consideration in designing multipliers. The total output noise of Fig. 1 is given by

$$\begin{aligned} \overline{i_{n;o}^2} &= 8\overline{i_{n;\rm lin}^2} + 4\overline{i_{n;\rm sat}^2} \\ &= 16kTg_{\rm ds1}df + 16kTg_{\rm ds2}df + \frac{32}{3}kTg_m df \end{aligned} \tag{8}$$

where

$$g_{\rm ds1} = K_N(Y - V_O - V_{\rm THN}) \tag{9}$$

$$g_{\rm ds2} = K_M(V_{\rm DD} - V_P - V_{\rm THN}) \tag{10}$$

$$g_m = K_P(V_{\rm DD} - X - |V_{\rm THP}|). \tag{11}$$

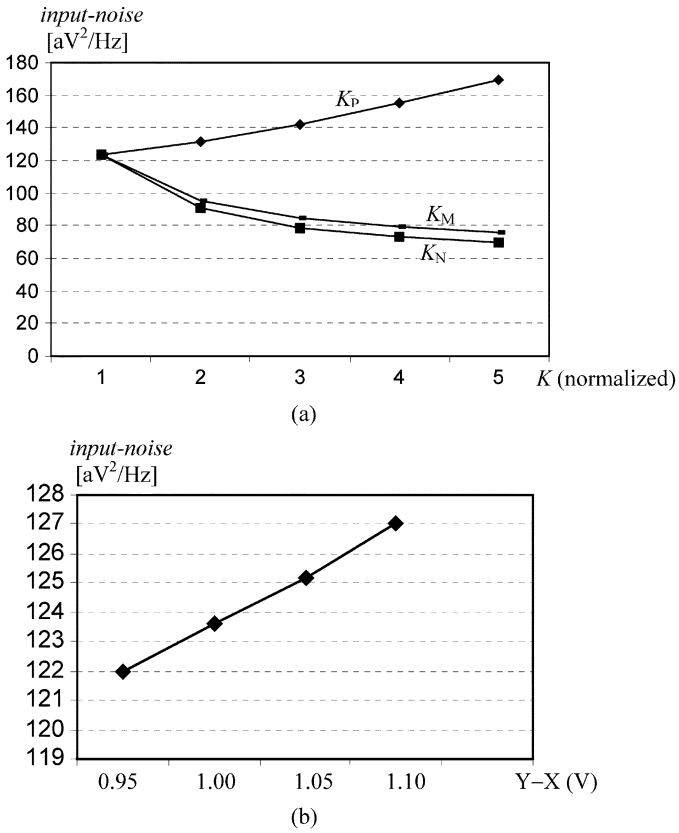

Fig. 3. Noise simulation results for Fig. 1. (a) Input-referred noise voltage of Fig. 1 versus K_P, K_M, and K_N. (b) Input-referred noise voltage of Fig. 1 versus $(Y - X)$.

The total input noise is

$$\overline{v_{n;i}^2} = 16kT\frac{K_P^2}{K_M^2}g_{\mathrm{ds1}}df + 16kT\frac{K_P^2}{K_N^2}g_{\mathrm{ds2}}df + \frac{32}{3}kT\frac{K_P^4}{K_M^2K_N^2}g_m df. \quad (12)$$

This suggests that K_M, K_N, and K_P should be well designed to improve the noise performance. Also, the input-referred noise depends on g_{ds} and g_m that vary with the value of $(Y-X)$. If we increase K_M or K_N while keeping other parameters the same, the input-noise will decrease. This is verified by experimental results in Fig. 3(a). The input noise increases with the value of $(Y - X)$, as shown in Fig. 3(b).

IV. Experiment and Comparison

In order to estimate the performance of the proposed structure, we conducted the experiments on linearity, power consumption and noise. To ensure a fair comparison, we also simulated the most recommended structure of eight multipliers provided in [7]. For convenience, this structure is redrawn in Fig. 4. For both circuits in Figs. 1 and 4, a standard 0.35-μm CMOS technology was used with the supply voltage of 1.5 V. Unless otherwise specified, all transistors use the identical size of $W/L = 0.8\ \mu$m/0.35 μm and the circuits are biased to have typical values (in Fig. 4, $X = 1.3$ V, and $Y = 1.0$ V were used) with the input range of ± 0.2 V for both x and y (i.e., $2x = 2y = 0.4$ V).

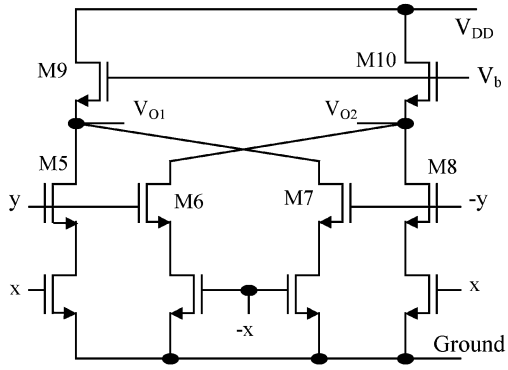

Fig. 4. Recommended multiplier structure by [7].

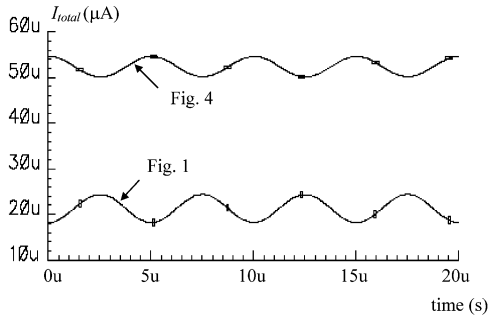

Fig. 5. Total current comparison for Figs. 1 and 4.

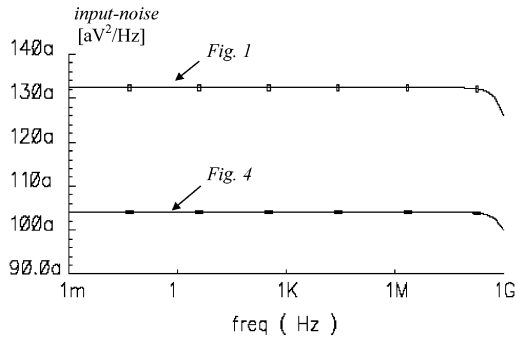

Fig. 6. Input-referred noise simulation results for Figs. 1 and 4.

A. Output Current

To compare the power consumption of Figs. 1 and 4, we used same power supply and input signals. Fig. 5 shows the total currents for these two structures with both x and y being a 100-kHz 0.2-V_{p-p} sinusoidal-wave. The circuit of Fig. 1 exhibits lower power consumption which is nearly one third of that in Fig. 4.

B. Noise

Noise comparison is given in Fig. 6. Our experiment shows that the structure in Fig. 1 has a little higher input-referred noise compared with the structure of Fig. 4 when applied with similar input signal level.

C. Linearity

We look at the DC transfer characteristics of $(V_{o1} - V_{o2})$ versus x and y for Fig. 1 with $X = 0.5$ V and $Y = 1.5$ V. The results are plotted in Fig. 7(a) and (b) where the linearity gets worse as x and y increase. In particular, when $x = y = 0.2$ V,

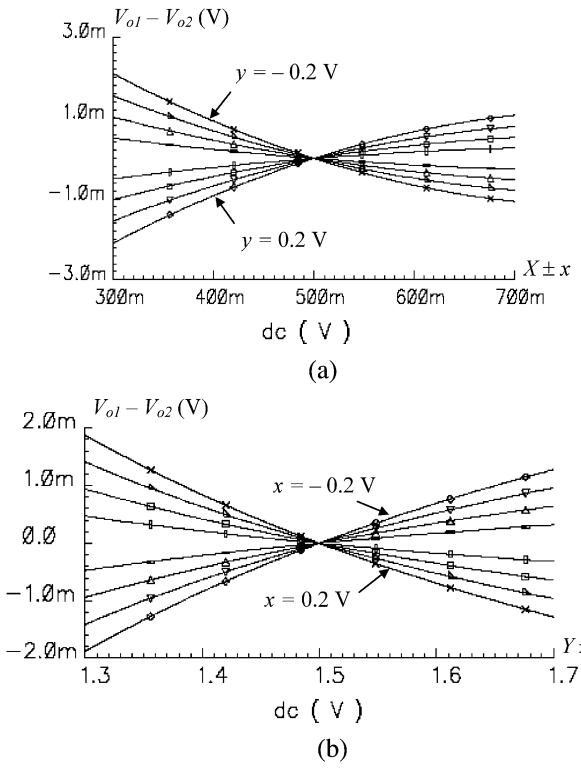

Fig. 7. The dc transfer characteristics of Fig. 1. (a) $V_{o1} - V_{o2}$ versus x. (b) $V_{o1} - V_{o2}$ versus y.

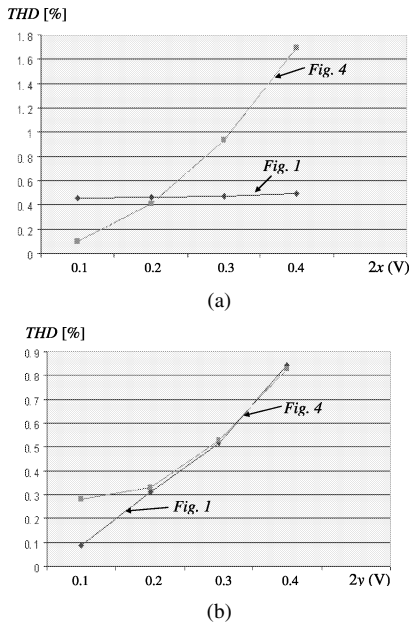

Fig. 8. THD for Figs. 1 and 4. (a) THD of signal x with $2y = 0.4$ V. (b) THD of signal y with $2x = 0.4$ V.

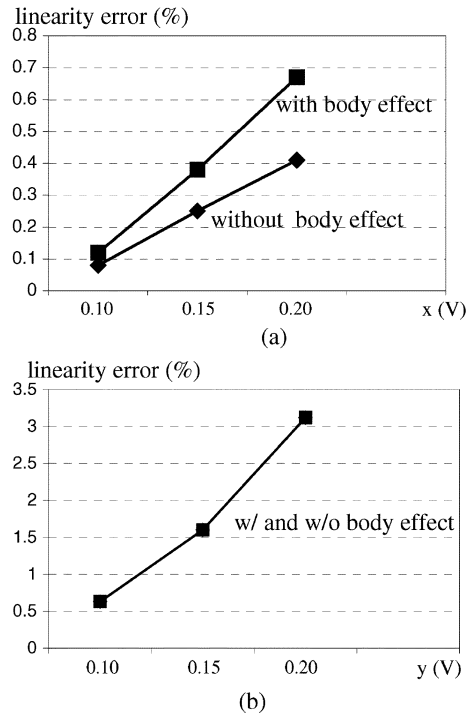

Fig. 9. Linearity errors with and without body effects. (a) Linearity error versus x (when $y = 0.2$ V). (b) Linearity error versus y (when $x = 0.2$ V).

the linearity error is measured to be 2.7%. From our simulation, the linearity error of Fig. 4 reaches 5.3% for same x and y, which is almost twice as much as in Fig. 1. Fig. 8(a) and (b) show the total harmonic distortion (THD) when a constant dc voltage (0.2 V) is applied to x (or y) while a 100-kHz 0.2 $V_{\mathrm{p-p}}$ sinusoidal-wave is applied to y (or x). It can be seen that the THD (when $2x = 2y = 0.4$ V) of signal x for Fig. 1 is much less than that for Fig. 4. With signal y, two structures have the comparable THD.

Body effect may be another source of linearity errors. We show that the structure of Fig. 1 has less body effect than that of Fig. 4. Indeed, for the transistors $N1$–$N4$ in Fig. 1, V_p is normally very low and the value of their V_{sb} is very small. The transistors $P1$–$P4$ and $M1$–$M4$ have no body effect as their source terminals are connected to V_{DD} and the ground, respectively. Fig. 9 shows the linearity comparison with and without body effect for signal x and y($x = 0$–0.2 V when $y = 0.2$ V or $y = 0$–0.2 V when $x = 0.2$ V). The curves in Fig. 9(b) overlap, implying that the body effect has no impact on the linearity error due to signal y.

In summary, experimental results have shown that the proposed multiplier structure consumes much less power compared with the existing structures. The total supply current can be further reduced by some design considerations such as using a smaller value of $(Y - X)$ and bigger size for transistors $P1$-$P4$. The proposed multiplier was sent to the Canadian Microelectronics Corporation (CMC) for fabrication with 0.35-μm CMOS technology. Fig. 10 shows its layout diagram. We performed the post-layout simulation for Fig. 10 and also tested the fabricated chip. The comparison is shown in Table I, where the post-layout simulation results are very close to pre-layout simulation shown before (see Sections IV-A and IV-C). In this table, the linearity error of x (or y) is measured when a 100-kHz 0.2-$V_{\mathrm{p-p}}$ sinusoidal-wave is applied, while the total current and power consumption are measured with $x = y = 0$ V, $X = 0.5$ V, $Y = 1.5$ V, and $V_{\mathrm{DD}} = 1.5$ V. We see that the overall performance of the real chip is much worse than simulation results. We believe this is mainly due to the added pads for chip fabrication since the core area of proposed multiplier (i.e., Fig. 10) is just a very small portion (less than 5%) of the whole chip.

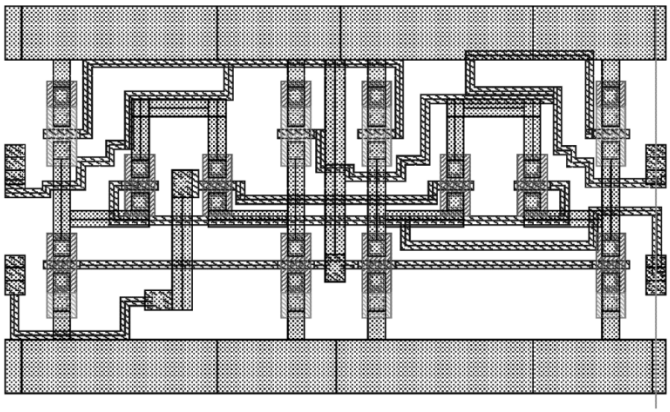

Fig. 10. Physical layout of Fig. 1.

TABLE I
COMPARISON OF POST-LAYOUT SIMULATION AND TESTING RESULT

	post-layout simulation	*testing*
Linearity error of x	0.7%	1.09%
Linearity error of y	3.2%	4.52%
Total current (μA)	21	30
Power consumption (μW)	32	45
Bandwidth (GHz)	1.98	1.02

Layout of these pads was changed by the CMC to meet some requirements (such as final design rule check—DRC) for fabrication, and thus not available for full post-layout simulation. Other factors such as process variations and parasitic parameters may also contribute to the significant difference between simulation results and measurements shown in Table I.

V. CONCLUSION

A low-power CMOS analog multiplier has been proposed. Several important performance metrics have been analyzed. A significant power reduction has been achieved by both well-designed structure and fine-tuned parameters. The results from simulation and chip testing have shown the desirable performance of the multiplier, which makes it very suitable for use in low power implementation of large-scale analog circuits.

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