A Buffered Single-Supply Charge Amplifier for High-Impedance Piezoelectric Sensors

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***Abstract*— This paper presents a differential-input, differential-output charge amplifier topology built with discrete, commercial components. The amplifier is designed to interface high-impedance ultrasonic sensors made of piezoelectric polymer, with a required bandpass of at least 100 kHz to 1 MHz, and needs to operate from a single 5-V supply. The performance and tradeoffs of the proposed topology are evaluated analytically and using a circuit simulator, showing a charge-to-voltage conversion gain in excess of 240 dB[V/C], while maintaining an input impedance lower than 100 Ω. Simulations and measurements of a prototype implementation are presented.**

***Index Terms*— Analog circuits, charge amplifiers, differential amplifiers, preamplifiers, ultrasonic sensors.**

I. Introduction

CHARGE-MODE amplification of capacitive sensors is a signal conditioning approach useful in certain measurement setups, where the impedance of the sensor is high and the cabling is such that its stray capacitive loading becomes comparable with the sensors' own capacitance [1].

Designing a charge amplifier using commercial components, however, turns into a challenge when pursuing bandwidths above hundreds of kilohertz in reduced supply voltage systems, since, in this range, commercial operational amplifiers start to present severe tradeoffs that impact the overall performance of the circuit.

The target application considered in this paper is guided-wave ultrasound structural health monitoring (SHM) systems adopting custom broadband piezoelectric sensors made of piezoelectric polymer films (polyvinylidene fluoride (PVDF)], and operating in the 100-kHz–1-MHz bandwidth [2]. When compared with piezoceramic materials, PVDF has a very low relative dielectric constant ($\epsilon_r = 10$–12) that results in our sensors having a capacitance in the 10^1–10^2-pF range and generally inferior overall performance compared with their ceramic counterparts [3]. Despite this, piezoelectric sensors made of polymers benefit from material elasticity and flexibility, which represents an important characteristic in SHM applications that require installing them on structures that are uneven and/or subject to strain.

As reported in [2], the capacitance of piezopolymer sensors for SHM lies in hundreds of picofarads range, and decreases steadily as the frequency grows. At the same time, cables used to connect those sensors to the front-end electronics may exhibit conductor-to-conductor capacitances in the order of 100 pF/m. Therefore, as the length of the cables increases, sensor loading will result in smaller signals at the preamplifier inputs. A charge-mode preamplifier, which ideally presents itself as a short-circuit to the transducer, can reduce the effect of capacitive sensor loading if its input impedance is lower than the cable's shunt impedance [1]. Charge amplifiers have been successfully used to interface piezoelectric polymer sensors in different applications, including tactile sensors [4] and PVDF-based piezoelectric wafer active sensors (PWAS) for Lamb-wave reception [5].

The adoption of charge amplifiers in ultrasound imaging has been lately revamped with the emergence of capacitive ultrasonic micromachined transducers (CMUTs), and a literature exists on the subject [6], [7]. Unfortunately, the requirements and integrated implementations of charge amplifiers for CMUTs have generally little in common with the proposed application, even though some research has been performed on the adoption of CMUTs for SHM [8].

In general, SHM systems can be deployed in noisy electromagnetic environments (industrial, automotive, aerospace, and so on), and can thus greatly benefit from the noise immunity provided by differential signal conditioning electronics. That was the main rationale behind adopting a fully differential circuit architecture in this paper.

A differential-input, single-ended output charge amplifier design can be found in [9]. Although its requirements are quite different from those sought by the authors in terms of bandwidth, and therefore a direct performance comparison with the amplifier proposed in this paper is not possible, it is nonetheless an interesting circuit topology alternate to the one hereby presented.

Many differential charge amplifiers presented in the literature have been designed with a symmetrical two-op-amp topology that requires both to be high-performance

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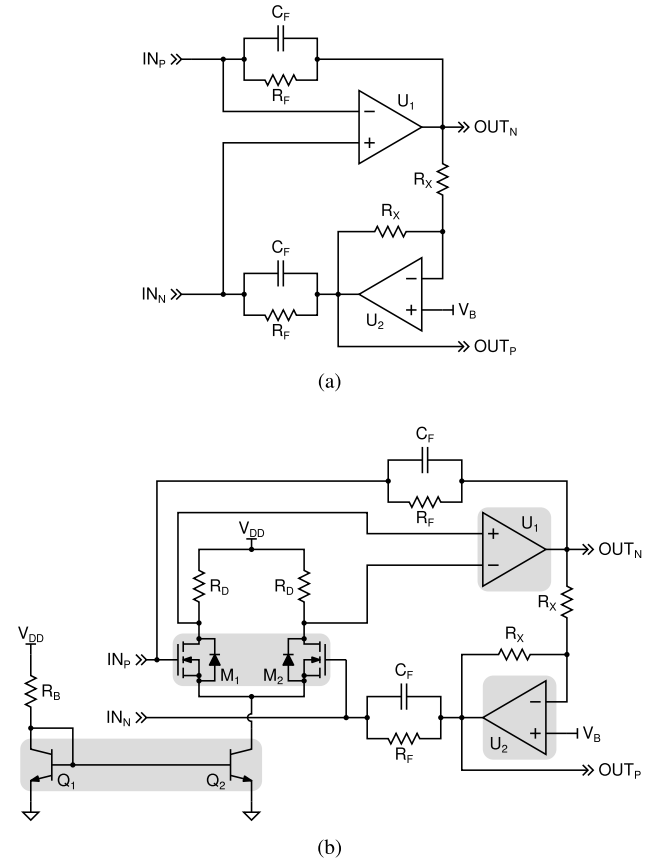

Fig. 1. (a) Original differential input and differential output charge amplifier topology. (b) Improved, single-supply topology with additional differential input stage and biasing current mirror.

devices [10], [11]; the base topology adopted in this paper needs only one of the two op-amps to provide high open-loop gain and wide bandwidth. Other designs have been attempted using a single fully differential amplifier, but their performance is limited by other technology-related tradeoffs (input bias current, open-loop gain lower than regular bipolar op-amps) [12].

In this paper, an improved charge amplifier design based on discrete components that circumvents the limitations imposed by the interplay of op-amp technology, speed, and bias requirements is presented, detailing the design and tradeoffs of the new topology. Simulations performed with SIMetrix (SIMetrix Technologies Ltd, Thatcham, U.K.) and the measurements of a prototype implementation are then reported and discussed, with an emphasis on the evaluation of common-mode and differential-mode responses of the amplifier.

II. Improving Charge Amplifiers

Generally speaking, charge amplifier topologies based on operational amplifiers, like the one shown in Fig. 1(a), have a differential input impedance that depends on the feedback impedance of the circuit and on the open-loop gain of the op-amp: increasing the closed-loop gain (i.e., the charge conversion gain) requires increasing the feedback impedance, resulting in a higher input impedance, while increasing the open-loop gain of the op-amp U_1 (A_{OL}) does the opposite [1]. The expression of the differential input impedance of the circuit in Fig. 1(a) is

$$Z_{\mathrm{IN}} = \frac{2Z_F}{1+2A_{\mathrm{OL}}}$$
$$Z_F = R_F \parallel \frac{1}{sC_F}. \tag{1}$$

While the charge conversion gain is a design parameter that can be set by changing the value of the feedback components, the open-loop gain of the op-amp can usually only be changed by changing the component itself. It is also strongly dependent on the semiconductor technology and supply voltage.

The amplifier topology presented by Giannelli *et al.* [1], which followed the schematic of Fig. 1(a), adopted a high-speed, FET-input operational amplifier (a Texas Instruments OPA657) in place of U_1 that ensured a large open-loop gain (70 dB typical), but required a supply of at least 8 V.

When operating in single-supply 5-V systems, the choice of wide-bandwidth, high open-loop gain op-amps is mainly composed of bipolar devices. One problem of using bipolar op-amps in charge amplifiers is their high-input bias current ($\sim$10 μA or more are common), which, combined with capacitive sources that do not provide a dc path for biasing the inputs, results in conflicting requirements. That of input biasing was a nonissue in the previous charge amplifier design, as the FET inputs of the OPA657 conducted an insignificant current that could flow through the high-resistance paths provided by R_F without affecting circuit operation. In the case of bipolar devices, simply adding dedicated biasing resistors to the op-amp inputs should be avoided, because they can either shunt the input signal or, most importantly, introduce significant offsets that can shift the operating point of the op-amps outside of their specified common-mode voltage range.

To solve the input biasing problem and successfully use high-speed bipolar op-amps, we propose the introduction of an additional differential input stage to the charge amplifier topology described in [1] [shown in Fig. 1(a)], obtaining the circuit shown in Fig. 1(b).

The additional differential pair, made by the two matched nMOS devices M_1 and M_2 (Advanced Linear Devices ALD1101A), serves the vital purpose of buffering the input bias current of the high-speed op-amp U_1 (a Texas Instruments LMH6629) and provides additional amplification, thus increasing the combined open-loop gain of the two cascaded stages. Hereinafter, A_{COL} will be used to indicate the combined open-loop gain of the charge amplifier that is the product between the differential pair gain and the open-loop gain of U_1.

The proposed topology has been devised specifically for a discrete component realization to overcome some of the tradeoffs associated with commercially available bipolar operational amplifiers. Consequently, many integrated circuits' techniques generally adopted to improve the performance of differential pairs have been excluded from this design to keep the number of components (and, therefore, the total area of the circuit) to a minimum.

A. Amplifier Design

An implementation of the proposed charge amplifier topology was designed to obtain a rather large charge conversion gain. As in the classical charge amplifier, the midband charge-to-voltage conversion ratio is inversely proportional to the feedback capacitance C_F. The differential midband charge-to-voltage conversion gain can be calculated as follows when a purely differential charge signal Q_{DM} is fed to the inputs. In the Laplace domain, the time derivative of the input charge corresponds to the differential-mode input current $I_{\mathrm{DM}} = s\,Q_{\mathrm{DM}}$. Assuming a virtual short circuit at the charge amplifier inputs, I_{DM} will flow through the series of feedback capacitances C_F (the midband region corresponds to Z_F being dominated by C_F), resulting in a differential output voltage equal to $V_{\mathrm{OUT,DM}} = 2\ Z_F I_{\mathrm{DM}} = 2\ Q_{\mathrm{DM}}/C_F$. The midband charge conversion gain can thus be defined as $A_{\mathrm{DM}} = V_{\mathrm{OUT,DM}}/Q_{\mathrm{DM}} = 2/C_F$.

Our design adopted two 1-pF precision thin-film capacitors as feedback capacitances, thus attaining a nominal differential midband gain of $A_{\mathrm{DM}} = 2\ TV/C$ (246 dB[V/C]). Those capacitors, manufactured by AVX Corporation, Fountain Inn, SC, USA, had a nominal capacitance tolerance of ± 0.02 pF, one of the tightest available on the market.

The feedback capacitance, together with the total capacitance appearing across the input terminals of the amplifier (C_{SRC}), sets the equivalent voltage gain of the circuit, that is the gain with respect to the voltage that would be developed across the source capacitance of a charge-output sensor if it was left open-circuit. This gain is defined as the ratio $A_{V,\mathrm{DM}} = 2\ C_{\mathrm{SRC}}/C_F$ for a differential charge amplifier. The importance of this parameter lies not only in allowing the comparison of signal gain between charge amplifiers and high-input impedance voltage-mode amplifiers but also on the effect that it has on the noise of the charge amplifier itself, as will be shown later in this paper.

Resistors R_F, together with C_F, set a pole in the charge conversion transfer function of the amplifier, determining the lower end of the passband. Two 4.7-MΩ metal electrode leadless face resistors were used as R_F in our design, setting the high-pass cut frequency at

$$f_{\mathrm{HP}(-3\,\mathrm{dB})} = \frac{1}{2\pi\, R_F C_F} \approx 34\ \mathrm{kHz}. \tag{2}$$

The upper bandwidth of the proposed charge amplifier was primarily limited by the performance of the gain blocks (i.e., the high-frequency roll-off of A_{COL}). The following paragraphs, however, highlight how the presence of additional components at the amplifier inputs affected the transfer function of the circuit in certain situations.

The schematic in Fig. 2 shows a simplified equivalent input circuit, including the series resistance of the input multiplexer R_{series}, the blocking capacitors C_{dc}, and two shunting capacitors: C_{stray} and C_{shunt} (the origin and purpose of this network will be explained in Section II-E). The differential input impedance of the amplifier was defined as $Z_{\mathrm{IN}} = (V_{\mathrm{IN},P} - V_{\mathrm{IN},N})/I_{\mathrm{IN}}$.

In the simplest case, R_{series} and C_{stray} can be used to calculate the main low-pass pole in the conversion gain of

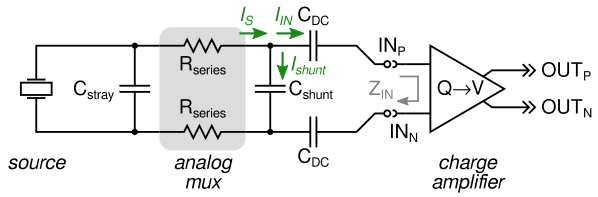

Fig. 2. Simplified input network of the charge amplifier prototype, including the parasitic components. The analog multiplexer used to swap the inputs is a Texas Instruments TS5A23157.

the charge amplifier, provided their values are known and that the impedance seen at the outputs of the analog multiplexer can be approximated as resistive (R_{IN})

$$f_{\mathrm{LP}(-3\,\mathrm{dB})} = \frac{1}{2\pi\,(2R_{\mathrm{series}} + R_{\mathrm{IN}})C_{\mathrm{stray}}}. \tag{3}$$

However, in our case, C_{stray} included many parasitic components belonging to the cables, the analog multiplexer, and the transducer itself, some of them difficult to predict at the design stage; moreover, the input impedance of the charge amplifier is not purely real, making this calculation widely inaccurate unless R_{series} dominates the two.

An interesting effect of the input network worth investigating was the interplay between C_{shunt}, C_{dc}, and Z_{IN}. As shown in Fig. 2, those components formed a current divider and the actual differential input current of the amplifier (I_{IN}) could be represented in the Laplace domain as in

$$\frac{I_{\mathrm{IN}}}{I_S} = \frac{1}{\left(1 + 2\frac{C_{\mathrm{shunt}}}{C_{\mathrm{dc}}}\right)\left(1 + \frac{s Z_{\mathrm{IN}} C_{\mathrm{dc}} C_{\mathrm{shunt}}}{C_{\mathrm{dc}} + 2C_{\mathrm{shunt}}}\right)}. \tag{4}$$

In the denominator of (4), the factor to the left shows that the ratio $C_{\mathrm{shunt}}/C_{\mathrm{dc}}$ defines an attenuation of the input signal of the amplifier, suggesting that $C_{\mathrm{dc}} \gg C_{\mathrm{shunt}}$ to obtain the maximum charge flow inside the amplifier inputs.

The factor to the right, on the other hand, is frequency-dependent but can be simplified by making certain assumptions on Z_{IN}. Equation (6) shows that, as will be explained later, within the intended passband of the charge amplifier, Z_{IN} behaves like a capacitance. Thus, by replacing Z_{IN} with $1/(sC_{\mathrm{IN}})$, (4) can be rewritten into

$$\frac{I_{\mathrm{IN}}}{I_S} \simeq \frac{1}{\left(1 + 2\frac{C_{\mathrm{shunt}}}{C_{\mathrm{dc}}}\right)\left(1 + \frac{1}{C_{\mathrm{IN}}} \cdot \frac{C_{\mathrm{dc}} C_{\mathrm{shunt}}}{C_{\mathrm{dc}} + 2C_{\mathrm{shunt}}}\right)}. \tag{5}$$

Therefore, while the approximation of Z_{IN} as a capacitance holds, the rightmost factor of the denominator also causes a broadband attenuation of the input signal. In this case an increase of either C_{dc} and C_{shunt} would determine a net signal reduction, while C_{IN} should be as large as possible to counteract the effect. As expected, in the ideal case where $Z_{\mathrm{IN}} = 0$, the rightmost factor disappears entirely.

Considering that the effect of finite bandwidth of the amplifier A_{COL} caused Z_{IN} to lose the capacitive behavior at the onset of open-loop gain roll-off (as shown in Fig. 3, the input impedance starts growing again after $\sim$1 MHz), (5) had limited validity and the two capacitances C_{dc} and C_{shunt} still introduced a high-frequency pole in the transfer function of the charge amplifier.

B. Additional Differential Stage

The differential pair formed by M_1 and M_2 was designed to buffer the input bias current of U_1, at the same time increasing the combined open-loop gain (A_{COL}) of the charge amplifier.

Biasing conditions for the differential pair FETs were imposed by the required operating conditions of U_1: the dc voltage at the output of U_1, set through V_B in Fig. 1(b), needed to be fixed at midsupply rail (i.e., 2.5 V) to avoid output distortion from the op-amp. This turned into having 2.5-V dc forced at the gates of M_1 and M_2 as well.

Additionally, the inputs of U_1 needed to remain within their specified common-mode input range. Since they both were directly cascaded to the outputs of the differential pair, this requirement further restricted the feasible biasing range of the two FETs.

Ultimately, the differential pair tail current I_{C,Q_2} was set at 15 mA, with transistor Q_2 operating at $V_{CE,Q_2} = 0.11$ V, and the drain terminals of the differential pair biased at 2.9 V. The resulting FET small-signal transconductance was around $g_m \approx 7$ mS. The actual gain of the differential pair, however, was not only determined by $R_D = 270\ \Omega$ alone, i.e., $A_d = g_m R_D (\approx 5.5$ db), but also by the loading introduced by the input impedance of U_1. Simulations performed using the SPICE macromodel of op-amp U_1 as load showed that the actual differential gain was $A_d \approx 4.7$ dB.

Being the transconductance so low, the Miller multiplication of the FETs gate–drain capacitance was not the major limiting factor of the differential stage bandwidth. In fact, the culprit was again to be found at the differential pair outputs, where U_1 introduced a capacitive load made up of two different contributions: its intrinsic input capacitance (4 pF according to the datasheet) and, most importantly, the Miller multiplication of capacitance C_M (see Fig. 5). As closed-loop stability issues were expected from the cascading of the differential pair and op-amp U_1, it seemed at first that the Miller multiplication of C_M could provide a way to reduce the bandwidth or compensate the charge amplifier; this, however, turned out to be an impractical solution with discrete components because of the large open-loop gain of U_1.

C. Amplifier Differential Input Impedance

The formula for calculating the differential input impedance of the proposed amplifier is similar to that used for the original topology of Fig. 1(a), reported above in (1), with the only difference being that the open-loop gain appearing at the denominator is now the combined gain of the discrete differential stage and U_1 (i.e., A_{COL}), as shown in

$$Z_{\mathrm{IN}} = \frac{2Z_F}{1 + 2A_{\mathrm{COL}}}. \tag{6}$$

For frequencies above the first pole (2), C_F dominates the feedback impedance of the amplifier, meaning that Z_{IN} exhibits a capacitive behavior until the roll-off of A_{COL} begins. A plot of the simulated input impedance of the proposed topology is shown in Fig. 3. Contributions of the additional input components used in the prototype, described in Section II-E, are not included.

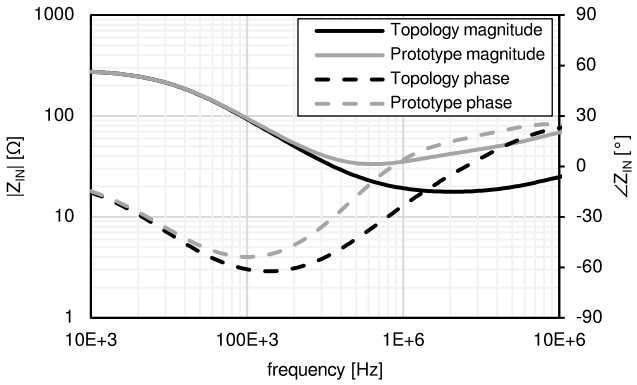

Fig. 3. Simulated input impedance of the proposed amplifier topology, together with a simulation of the prototype, including frequency compensation (see the text). These plots do not account for the additional impedance introduced by the components present at the amplifier inputs (like the analog multiplexer).

As a comparison baseline, the circuit design of Fig. 1(a), presented in [1], had an input impedance almost an order of magnitude greater than the proposed design within the 100-kHz–1-MHz band, if configured with the same Z_F.

Fig. 3 also includes the simulation results showing the effect of frequency compensation used in the prototype circuit (stability is discussed in Section II-F). The compensation technique used to attain stability acted directly on A_{COL}, reducing the open-loop gain bandwidth and, therefore, degrading the input impedance of the charge amplifier.

D. Effects of Passive Component Mismatch

A discrete implementation of a charge amplifier should expect a certain degree of component mismatch to arise from board and packaging parasitics, even when adopting high-precision passives. In our case, it is useful to distinguish the impact of stray capacitances between those that affect the closed-loop differential conversion gain and those that cause a degradation of the common-mode rejection performance.

Mismatch of the differential pair described in Section II-B, the input stage of U_1, and the feedback resistors of U_2 mostly leads to a degradation of the common-mode rejection ratio (CMRR) of the amplifier, as they primarily affect the circuit balance.

Mismatch and stray loading of the feedback impedances Z_F, as expected, result in a direct and measurable effect on the closed-loop differential gain of the charge amplifier. In particular, the resistors R_F and the board interconnections of Z_F introduce two kinds of stray capacitances: a shunt capacitance across Z_F and a capacitance between the component terminations and ground. While the latter can be seen as an additional loading at the inputs and at the outputs of the charge amplifier, the former directly influences the closed-loop gain. Chip resistors present a shunt capacitance that depends on their size and is generally of the order of some tens of femtofarads, and this additional capacitance increases the total amount of C_F, decreasing the conversion gain A_{DM}. In general, adopting

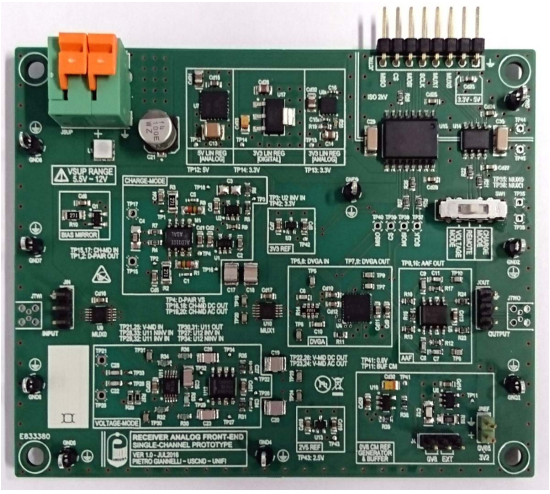

Fig. 4. Prototype analog front end for piezoelectric sensors, including the proposed charge amplifier. A partially assembled version of the circuit shown here was used to perform all the measurements presented in this paper.

smaller passives will result in lower shunt capacitance, leading to a smaller gain error [13].

E. Prototype-Related Input Circuitry

The equivalent input network shown in Fig. 2 was not an intrinsic part of the topology, even though some of its elements represented actual parasitic components of the circuit.

The prototype implementation of the proposed charge amplifier, which was also used to perform all the measurements presented in this paper, was part of the custom analog front end for piezopolymer transducers shown in Fig. 4. In that circuit, the proposed amplifier was placed side by side with an instrumentation amplifier, so that they could be swapped in the analog signal chain.

Dual-channel analog multiplexers were added at both the inputs and outputs of the two preamplifiers to select the signal path. The input terminals, which were switched using a Texas Instruments TS5A23157, ended up requiring the additional blocking capacitors C_{dc} to prevent the multiplexer and preamplifiers from affecting each other's bias points.

The multiplexer introduced the two series resistances shown in Fig. 2 ($R_{\mathrm{series}} \approx 10\ \Omega$) and contributed to the shunt and stray capacitances with ~17.5-pF nominal per terminal.

The presence of multiplexer resistance in series with the inputs had the obvious drawback of raising the total input impedance, while its effect on the frequency response of the amplifier was negligible.

F. Stability and Frequency Compensation

Despite the differential nature of the proposed amplifier, with two separate feedback branches, the topology itself provided a way to easily define a single-loop gain and evaluate the stability using a classical phase/gain margin criterion. With reference to the circuit of Fig. 5, where capacitor C_M is not present for the reasons discussed in Section II-B, the topology can be opened with a single cut at the output of op-amp U_1 to define the loop gain G_{LOOP}.

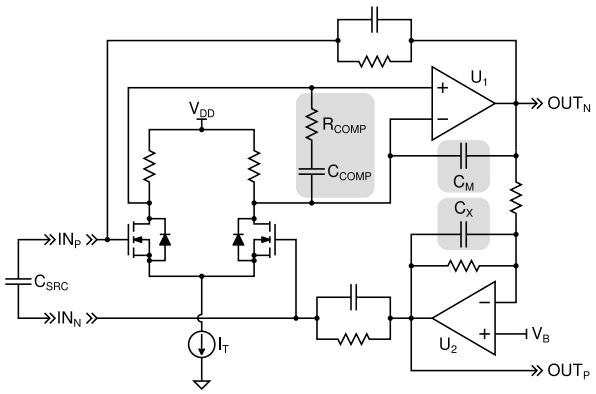

Fig. 5. Schematic showing the frequency compensation components considered for the proposed amplifier topology. The final design included all of them except capacitance C_M.

Given the complexity of the topology, with multiple gain blocks affecting the high-frequency behavior of the loop gain, the stability of the proposed amplifier was evaluated using the simulator and compensated using the series *R-C* network $Z_C = R_{\mathrm{COMP}} + 1/(sC_{\mathrm{COMP}})$ and capacitor C_X shown in Fig. 5. A simplified analysis is nonetheless given below to highlight the main stability issues. An expression of G_{LOOP} can be constructed by introducing several simplifying assumptions on the behavior of the topology. First of all, the gain stages are all assumed to display a single-pole response: for the differential pair determined by its load, for U_1 determined by the dominant pole of A_{OL}, and for U_2 determined entirely by the local feedback network. All other loading effects are neglected. By inspecting the feedback loop under those hypotheses, one can obtain the approximate loop-gain expression (7), where ω_{pd} is the differential pair pole and ω_{p1} is the dominant pole of U_1. Note that Z_C is not included in

$$G_{\mathrm{LOOP}}(s) = -2\frac{A_d}{1+s/\omega_{\mathrm{pd}}}\frac{A_{\mathrm{OL},0}}{1+s/\omega_{p1}}\frac{1+sC_XR_X/2}{1+sC_XR_X} \cdot \frac{1+sR_FC_F}{1+sR_F\,(2C_{\mathrm{SRC}}+C_F)}. \quad (7)$$

The low-frequency behavior of (7) is determined by the rightmost term of the expression, which presents a low-frequency pole followed by a zero. The influence of C_{SRC} on the pole frequency suggested that the unity gain crossover of G_{LOOP} would shift to lower frequency with growing source capacitance, increasing the stability margin. Therefore, as a first approximation, the worst-case stability condition was expected in conjunction with the minimum source capacitance.

The ordering of the remaining poles and zeros was as follows (from low to high frequency): ω_{p1} of op-amp U_1, the pole-zero pair of the inverting buffer (which was set by design), and finally ω_{pd} of the differential pair. The combined phase shift contributed by poles and zeros resulted in the $-180°$ phase crossover of G_{LOOP} being ultimately defined by ω_{pd}, which was the highest of all poles due to the very low gain of the differential pair [in our design $\omega_{\mathrm{pd}}/(2\pi) \approx$ 150 MHz].

Operating under these assumptions, a compensation strategy was enacted on the differential pair stage by adding Z_C as an output load, thus introducing a zero-pole pair and pushing

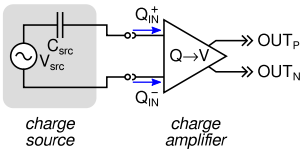

Fig. 6. Schematic of the ideal charge source and differential charge amplifier used to define the common-mode and differential-mode charge signals.

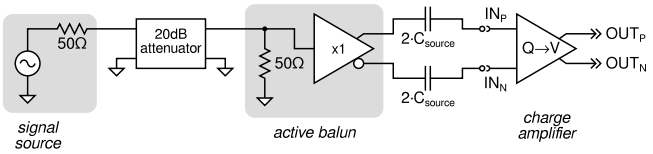

Fig. 7. Schematic of the differential charge source used to characterize the charge amplifier differential amplification.

ω_{pd} to higher frequency. The resulting effects on G_{LOOP} were to move the gain crossover point to lower frequency, at the same time moving to higher frequency the phase lag associated with ω_{pd}. This compensation technique came at the cost of degrading the input impedance of the charge amplifier, as introducing a pole-zero pair within the amplifier passband determined a reduction of the combined open-loop gain A_{COL}.

From a practical standpoint, the prototype design presented in this paper had a minimum source capacitance imposed by the additional input circuitry shown in Fig. 2: compensation was thus performed for the case with no source connected to the inputs. The component values used in the prototype to obtain ~70° of phase margin were $R_{COMP} = 249\ \Omega$, $C_{COMP} = 470$ pF, and $C_X = 47$ pF (the resistor in parallel with C_X was $R_X = 499\ \Omega$).

III. Prototype Characterization

Measurements on the prototype required the design of a custom setup with charge source emulators capable of generating input signals in hundreds of femtocoulomb range.

Simulations of the CMRR of the proposed charge amplifier suggested that the best way to characterize the differential and common-mode gain was designing two specific charge sources that could maximize either and attempt a direct measurement. The common-mode gain proved to be especially problematic to measure due to the influence of the two factors.

1) Large Differential Gain: With certain simulations showing more than 80 dB of CMRR, it was expected that even very small residual differential inputs would have resulted in their amplified output largely overshadowing any common-mode-related output.

2) Amplifier Unbalance: The proposed amplifier had differential inputs and outputs but lacked circuital symmetry. This resulted in an intrinsic unbalance of the single-ended input impedances that unevenly loaded the common-mode source, causing the introduction of an uncontrolled differential-mode input signal. It should also be added that this input impedance unbalance was not constant with frequency.

A. Charge Signal Definitions

The definitions of common-mode charge (Q_{CM}) and differential-mode charge (Q_{DM}) used throughout this paper are reported in (8), with reference to Fig. 6

$$Q_{CM} = Q_{IN}^+ + Q_{IN}^-$$
$$Q_{DM} = \frac{Q_{IN}^+ - Q_{IN}^-}{2}. \quad (8)$$

The corresponding common-mode and differential-mode charge-to-voltage transfer functions are indicated as A_{CM} and A_{DM}, respectively, where the input signal is either Q_{CM} or Q_{DM}, and the output signal is the differential output voltage ($V_{OUT,P} - V_{OUT,N}$).

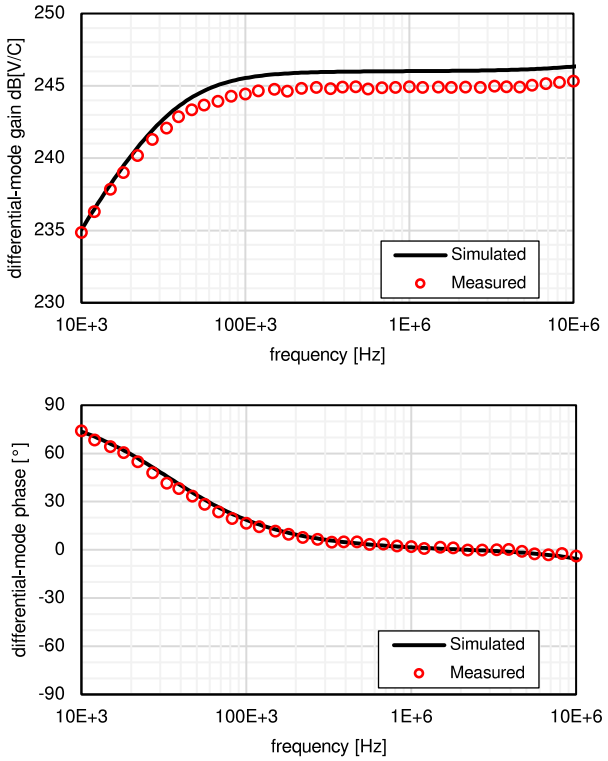

Fig. 8. Simulated and measured differential-mode charge conversion transfer function of the proposed charge amplifier (A_{DM}).

B. Differential-Mode Source and Gain Measurements

The differential charge source consisted of an active balun made with a wideband fully differential amplifier (a Texas Instruments LMH6552) in series with two capacitors. Fig. 7 shows the simplified schematic of the differential source. The actual $C_{source} = 1.65$ pF seen at the inputs of the charge amplifier was half the value of the capacitors used (3.3 pF); these two capacitors were used to retain circuit balance.

The adoption of a single-ended-to-differential converter allowed the direct measurement of the charge amplifier differential conversion gain A_{DM}, shown in Fig. 8 together with the simulation results.

C. Common-Mode Source and Gain Measurements

The common-mode charge source, shown in Fig. 9, consisted of a wideband closed-loop buffer (a Texas Instruments BUF602) feeding two capacitors in parallel to source the same

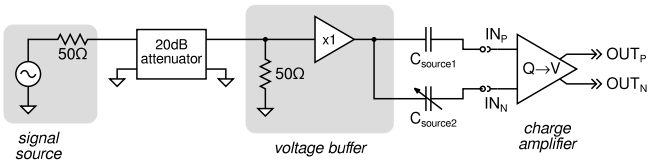

Fig. 9. Schematic of the common-mode charge source used to characterize the charge amplifier common-mode amplification. The common-mode calibration circuit is not shown.

charge signal to both the positive and negative inputs of the charge amplifier. $C_{source2}$ was actually a network of capacitors, including one trimmer, specifically designed to allow a fine adjustment of ∼100 fF around the tolerance range of $C_{source1}$.

Ideally, the two source capacitances ($C_{source1}$ and $C_{source2}$) would need to be identical to eliminate the differential signal injected along with the common-mode signal. However, the single-ended input impedance unbalance of the charge amplifier also played a role in generating a spurious differential mode; perfectly trimming $C_{source1} = C_{source2}$ would have resulted in a spurious differential input signal arising from the input impedance mismatch.

However, circuit unbalance was not completely unpredictable, and a reasonable source calibration procedure was found by exploiting the very large differential gain of the charge amplifier itself as an indicator of the presence of a spurious differential mode, adjusting $C_{source2}$ until the output was minimized, so that the remaining signal would be closer to pure common mode. Unfortunately, this procedure also had a dangerous pitfall, as trimming $C_{source2}$ could result in the introduction of an uncontrolled, out-of-phase differential signal canceling out the common-mode output, thus resulting in an erroneously high CMRR. A way to avoid such occurrence was found by analyzing the common-mode gain of the amplifier (A_{CM}) via Monte Carlo simulations that accounted for component tolerances. The simulation results, partially reported in Fig. 10, showed that in all the cases the common-mode gain started to collapse above ∼1 MHz, narrowing down to a gain of ∼185 dB and a phase of about −90° at 10 MHz. This point of convergence was used as reference to calibrate the common-mode source at 10 MHz.

The common-mode measurements performed with the calibrated source, also shown in Fig. 10, were then used to extrapolate the CMRR shown in Fig. 11. It is worth noting that the simulations predicted the presence of an antiresonance in A_{CM}, with characteristics strictly connected to the interplay of Z_F tolerances; this explains the measured CMRR peak shown in Fig. 11.

While the proposed calibration approach did not provide strictly accurate results for characterization purposes, as the input impedance unbalance varied with frequency, it could nonetheless give a rough estimate of the prototype amplifier CMRR.

D. Output Noise Measurements

The output noise spectral density of the charge amplifier was measured with discrete capacitors of increasing size connected across the inputs to highlight the effect of sensor capacitance.

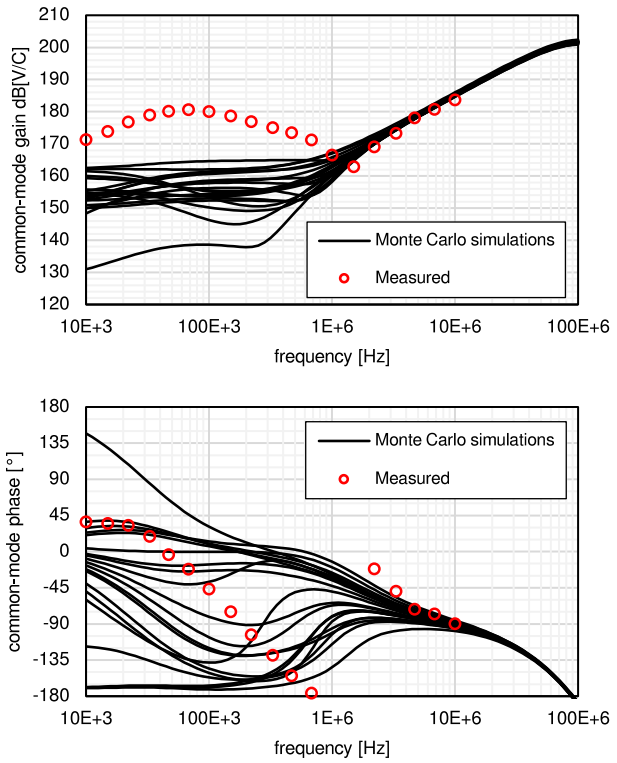

Fig. 10. Monte Carlo simulations and measurement of the common-mode charge conversion transfer function of the proposed charge amplifier (A_{CM}).

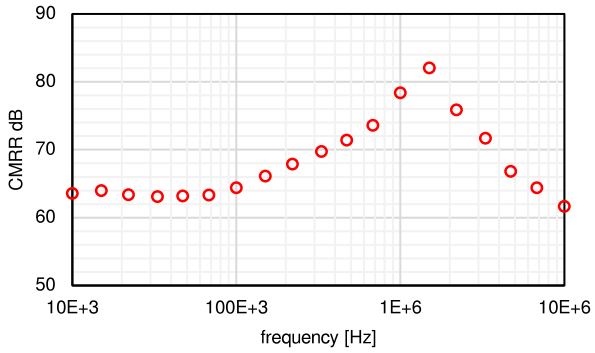

Fig. 11. CMRR measured on the prototype charge amplifier.

As with the classical charge amplifier, the closed-loop voltage gain of the proposed topology depended on the ratio between the source and the feedback capacitances. A larger source capacitance thus resulted in a larger contribution of the input noise voltage to the total output noise of the amplifier.

The output noise was measured with a spectrum analyzer using the circuit shown in Fig. 12, where a passive balun based on a Coilcraft TTWB2010L transformer was adopted to convert the differential output to a single-ended signal.

Fig. 13 shows the noise spectral density measured within the 100-kHz–1-MHz frequency range connecting additional source capacitances of 4.7, 47, and 470 pF. A measurement performed with the inputs left open is also shown, to highlight the noise floor determined by the parasitic capacitances of the analog multiplexer. As expected, the output noise grows with increasing source capacitance, suggesting that an increased

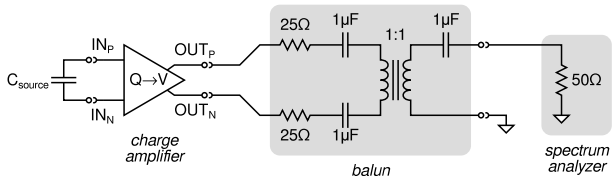

Fig. 12. Schematic of the setup used to characterize the charge amplifier output noise spectral density.

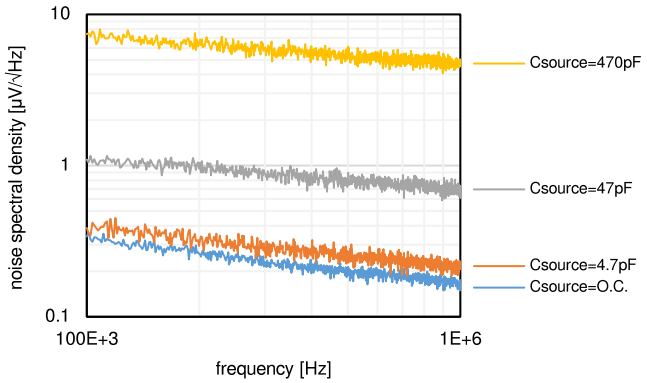

Fig. 13. Output noise spectral density of the charge amplifier measured using a spectrum analyzer with different source capacitances. The values shown in the legend are in addition to the parasitic capacitances already present at the amplifier inputs; the open-circuit trace accounts for those parasitic capacitances.

cable loading at the inputs will degrade the noise performance of the amplifier.

E. Output Range and Distortion

The nominal full-scale (FS) output range of the proposed charge amplifier was defined as ±2-V peak–peak differential. Given the midband gain of the device (2 TV/C), this translated to a maximum specified differential charge input of about ±1 pC. Since the measurements of Fig. 8 showed that the prototype exhibited −1 dB of gain with respect to the theoretical expectations, the charge input required to obtain an FS output had to be increased to ±1.1 pC.

The total harmonic distortion (THD) at 500 kHz was measured at FS and at −1-dB FS using the setup shown in Fig. 12, with the differential charge source of Fig. 7 (which had a $\mathrm{THD}_{\mathrm{SRC}} \approx 0.05\%$ at the specified measurement conditions). The resulting distortion was $\mathrm{THD}_{\mathrm{FS}} = 0.13\%$ and $\mathrm{THD}_{-1\,\mathrm{dB\,FS}} = 0.12\%$.

IV. Conclusion

This paper has presented a differential-input, differential-output charge amplifier topology for the signal conditioning of piezopolymer ultrasonic transducers.

The proposed circuit was devised to improve the performance of a previous design, namely, decreasing the input impedance and the supply voltage, by using only commercially available discrete components.

This paper can be compared with [9] by observing that both the circuits have differential inputs but only the one hereby presented retains a differential output. This fundamental difference prevented addressing the problem of matched feedback capacitances with the solution proposed in [9], that is by moving the integration to a second, single-ended stage. However, contemporary passive technology has reached a point where capacitor tolerances have become sufficiently tight to attain a large CMRR.

While the design succeeded in attaining the expected improvements, several criticalities arose from the analysis of the circuit and the measurements.

The gain bandwidth of the active components was the main factor defining the upper cutoff frequency of the amplifier transfer function, as the latter could only be properly controlled by introducing a resistance in series with the inputs, which increased the input impedance as well. Thus, it is advisable to perform low-pass filtering with a cascaded signal conditioning stage, if needed.

Closed-loop stability of the topology was also strictly dependent on the high-frequency behavior of the gain blocks, requiring the adoption of a circuital simulator for proper evaluation and compensation.

While the proposed amplifier had a sufficiently low input impedance to shunt the stray capacitances at its inputs (e.g., those due to cabling), the same stray capacitance was also shown to increase the output noise and possibly cause a midband gain loss.

The proposed topology has been developed for adoption in guided-wave ultrasound SHM systems. It is going to be included in a multichannel analog front end and used to receive signals propagated over composite structures with different experimental setups and transducers, and compared with other preamplifiers (e.g., instrumentation amplifiers). Those tests will highlight the scenarios, where the proposed amplifier provides the most significant advantages.

References

[1] P. Giannelli, A. Bulletti, and L. Capineri, "Charge-mode interfacing of piezoelectric interdigital Lamb wave transducers," *Electron. Lett.*, vol. 52, no. 11, pp. 894–896, 2016.

[2] P. Giannelli, A. Bulletti, and L. Capineri, "Multifunctional piezopolymer film transducer for structural health monitoring applications," *IEEE Sensors J.*, vol. 17, no. 14, pp. 4583–4586, Jul. 2017.

[3] K. S. Ramadan, D. Sameoto, and S. Evoy, "A review of piezoelectric polymers as functional materials for electromechanical transducers," *Smart Mater. Struct.*, vol. 23, no. 3, p. 033001, 2014.

[4] L. Pinna and M. Valle, "Charge amplifier design methodology for PVDF-based tactile sensors," *J. Circuits, Syst. Comput.*, vol. 22, no. 8, p. 1350066, Sep. 2013.

[5] B. Lin and V. Giurgiutiu, "Modeling and testing of PZT and PVDF piezoelectric wafer active sensors," *Smart Mater. Struct.*, vol. 15, no. 4, p. 1085, 2006.

[6] M. Sautto, A. S. Savoia, F. Quaglia, G. Caliano, and A. Mazzanti, "A comparative analysis of CMUT receiving architectures for the design optimization of integrated transceiver front ends," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 64, no. 5, pp. 826–838, May 2017.

[7] S. Y. Peng, M. S. Qureshi, P. E. Hasler, A. Basu, and F. L. Degertekin, "A charge-based low-power high-SNR capacitive sensing interface circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 1863–1872, Aug. 2008.

[8] D. A. Hutchins, D. R. Billson, R. J. Bradley, and K. S. Ho, "Structural health monitoring using polymer-based capacitive micromachined ultrasonic transducers (CMUTs)," *Ultrasonics*, vol. 51, no. 8, pp. 870–877, Dec. 2011.

[9] M. Massarotto, A. Carlosena, and A. J. Lopez-Martin, "Two-stage differential charge and transresistance amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 2, pp. 309–320, Feb. 2008.
[10] Y. Shen, N. Xi, U. C. Wejinya, and W. J. Li, "High sensitivity 2-D force sensor for assembly of surface MEMS devices," in *Proc. IEEE/RSJ Int. Conf. Intell. Robots Syst. (IROS)*, vol. 4, Sep. 2004, pp. 3363–3368.
[11] Z. Chen, K.-Y. Kwon, and X. Tan, "Integrated IPMC/PVDF sensory actuator and its validation in feedback control," *Sens. Actuators A, Phys.*, vol. 144, no. 2, pp. 231–241, 2008.
[12] M. Biroth, P. Achenbach, E. Downie, and A. Thomas, "A low-noise and fast pre-amplifier and readout system for SiPMs," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 787, pp. 185–188, Jul. 2015.
[13] R. S. Johnson, C. Wakeman, and W. Cuviello, "Frequency response of thin film chip resistor," in *Proc. 25th CARTS USA*, 2005, pp. 1–5.

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