A Portable Switching Bi-Phasic Stimulator with Level-Shifting Inverter for Functional Electrical Stimulation operating under a 6V Supply Voltage

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***Abstract*— This paper presents a compact architecture of portable functional electrical stimulator (*FES*) together with a level-shifting digital inverter. The presented architecture is composed of boost converter block with compact limiter circuit. The bi-phasic pulse generation is made from H-bridge switches with the boosted voltage from the boost converter block. The H-bridge switches are controlled by a level-shifting inverter which is composed of only four MOSFET devices with two capacitors. The clocking scheme for minimize power consumption is also a key point for reducing average power consumption in this work. The simulation results from LTSpice IV show that the presented stimulator can generate stimulating bi-phasic pulses with approximately +/-21V amplitude in voltage and constantly supply +/-19.2mA current to the load. The simulated bi-phasic pulse has pulse width of 326μs with frequency of 28.6Hz. The presented system can be operated under a single 6V supply voltage and the average power consumption is 117mW at stimulating frequency of 28.6Hz which can continuously operate under two CR2032 batteries for more than 11 hours. With this level of power consumption, the presented work is very suitable for using as a portable stimulator.**

Keywords— Functional Electrical Stimulation, FES, Muscle Stimulation, Portable Electrical Stimulator, Bi-phasic pulse generator

I. INTRODUCTION

Functional Electrical Stimulator is one of an important medical device for rehabilitation and help patients with drop-foot problem to recover their walking function. Restoring Lost motor activity can be done by applying a stimulating pulse via the nerves to shrink the targeted muscle in order to make organ movement with the same manner of ordinary motor function.

The implementation of the stimulator can be both implanted stimulator and external device. For an external device, the stimulating signal penetrates to the target nerves via surface electrode on human skin in a pulse manner which maybe monophasic pulse or bi-phasic pulse. The monophasic pulse transfers stimulating charges to the nerve in a very short pulse period. This approach, however, gives the stimulated cells a long time to recover after that which results in muscle fatigue [1]. On the contrary, the bi-phasic pulse with zero net charge approach drastically reduce charge build up and it offers charge balancing between positive portion and negative portion of the bi-phasic pulse. Hence, it takes longer time for patients to get fatigue with this approach and then the patient can use the stimulator device for longer time.

The stimulating pulse has three key parameters which are amplitude, frequency and duty cycle. According to previous studies, we found that the pulse pattern of frequency around 20-100Hz with pulse width of 25-800μs is good enough for FES pattern [2]-[3]. The body load impedance has an equivalent network of a resistor serially connected to a parallel circuit of a capacitor and a resistor which is so called "Electrode-Electrolyte Model" as shown in Fig. 1 [4][5]. The stimulating pulse can be current pulse with amplitude in the range of 5mA to 100mA [5].

A previous work presented the use of two fly-back power converters and a push pull current stage which requires double high voltage supply of +150V and -150V [6]. An alternative work presented a bi-phasic solution with supply voltage of 80V [7]. There is a work presented compensation network approach [5] and claimed to be the highest power efficiency but there is no any circuit detail and any explanation about its power usage in error amplifier, and driver. A digital-controlled universal approach [1] seems to be well designed and it provides high flexibility of pulse adjustment due to its digital approach. It, however, requires complex digital control system and it is not easy to implement. Previous simple system with monophasic approach [8] can be operated under a single battery but the system consumes too high power by draining all charges during off-pulse mode. It obviously cannot be used in portable device even it can operate with a single battery.

This paper presents an alternative solution which does not require any of high-voltage supply or even complex digital control system. The system in this paper can be operated under a standalone 6V supply voltage without wasting energy during off-pulse period which is very suitable for a portable stimulator.

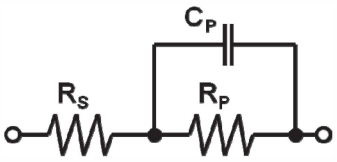

Fig.1 Electrode-Electrolyte Model for the stimulating nerve

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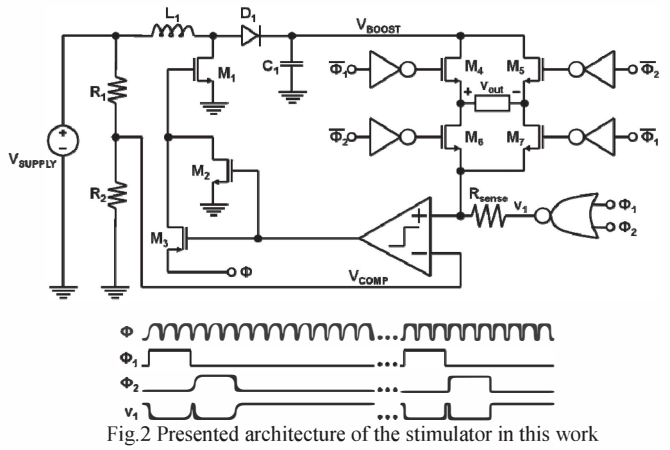

Fig.2 Presented architecture of the stimulator in this work

The next section presents architecture of the presented bi-phasic stimulator based on switching boost converter. Section III explains the level-shifting inverter as a driver for H-bridge switches to generate proper bi-phasic pulse. Simulation results and conclusion are summarized in the section IV and section V respectively.

II. Presented Architecture of Bi-Phasic Stimulator

In order to increase power efficiency, the switching boost converter approach is the most appropriate way to provide output voltage higher than its supply voltage. The boost converter, however, cannot be used alone without any voltage limiting control loop. The circuit may blown up due to infinite voltage increment of boost converter mechanism.

A compact architecture for stimulator is presented in Fig. 2 which is modified from previous work [5] to eliminate the usage of error amplifier.

V_{COMP} is generated by resistive voltage divider from the supply voltage as a reference level for determining upper limit of the boost converter.

Firstly, both of controlling clocks (Φ1 and Φ2) are low which makes output of the NOR gate to be high and the comparator output is high at this time. Then, the NMOS switch M2 is turned on to connect gate of the M1 to ground. No clock is fed to the boost converter block.

When the Φ1 or Φ2 is high, the NOR gate output is low and the comparator output is also low. At this time, the PMOS switch M3 is turned on while the M2 is off. The boosting clock signal (Φ) passes to gate of M1 and then the boost converter runs its switching mechanism to generate high output voltage at V_{BOOST}.

It is cleared that there is no switching clock fed to the boost converter when both of the stimulating clock Φ1 and Φ2 are low. Hence, there is no power consumption occurred in the boost converter. The boost converter only operates when the stimulation is required. This clocking scheme is helpful to minimize power consumption which is appropriate for a portable application.

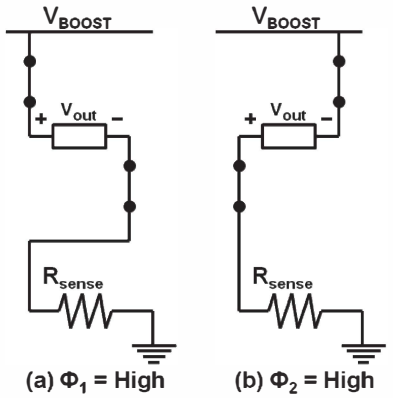

Fig.3 Bi-phasic pulse generation of the H-bridge switches

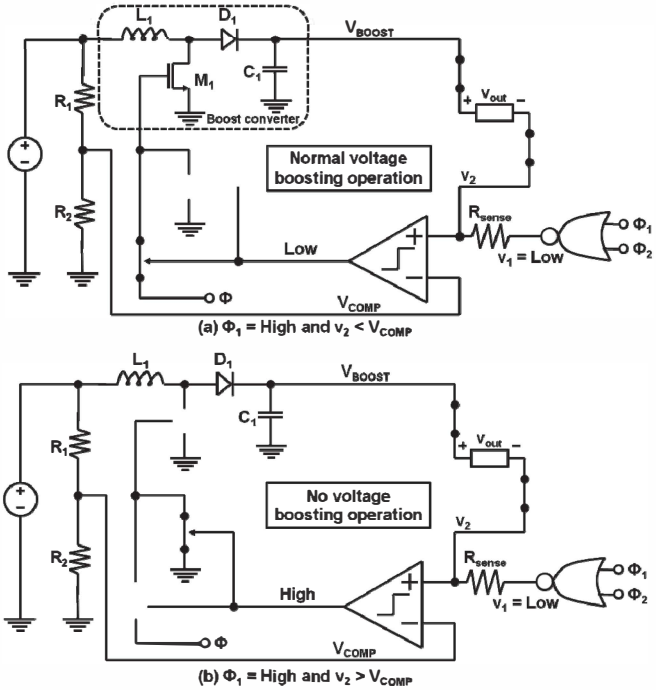

Fig.4 Voltage limiting mechanism for the boost converter

Bi-phasic stimulating pulse can be generated by H-bridge switches. The H-bridge switches are turned on or off based on their controlling clock signals. The load is connected to V_{BOOST} in two manners as shown in Fig. 3. When Φ1 is high, the load is connected in positive way between the boosted voltage and the sensing resistor (R_{sense}). The plus node is connected to the boosted voltage and the minus node is connected to the sensing resistor. When Φ2 is high, the load is connected in negative way which the minus node of the load is now shorted to the boosted voltage while the plus node is connected to the sensing resistor. The operation of this switching scheme generates a bi-phasic pulse to the load which is the nerve system.

While the H-bridge switches are operating, the boosted voltage is divided by the load and the sensing resistor. If the divided boosted voltage across the sensing resistor is higher than V_{COMP}, the comparator output turns to high and then M2 is turned on. Then, the boost converter stops its boosting operation since no clock is further supplied to the boost converter. The boost converter operates well only when the voltage across the sensing resistor is lower than V_{COMP}. Thus, the boosted voltage is clearly limited by setting a proper voltage level of V_{COMP} without any of further complex circuit required. Fig. 4 shows the voltage limiting mechanism of this architecture when the Φ1 is high. The same operation is also valid in the case that Φ2 is high.

This architecture requires two controlling clocks (Φ1 and Φ2) with small duty cycle for stimulation and one boosting clock (Φ) with much higher frequency than the previous two clocks for high voltage generation in the boost converter block. These clock signals, however, can be easily made from an ordinary timer circuit such as 555 timer IC or crystal oscillator with some digital circuits for timing adjustment.

III. Level-Shifting Inverter

According to Fig. 2, the H-bridge switches are directly connected to the boosted voltage, especially M4 and M5. Both switches can be implemented by NMOS. When turning the switches off, it can be easily done by connecting gate of NMOS to ground but it is not possible to turn the switches on by connecting gate of NMOS to the supply voltage which is lower than the boosted voltage. Still, the gate-source voltage of the switches is negative and the switches cannot be on. Thus, a level-shifting driver is necessary for the H-bridge switches in this case.

Fig. 5 is the circuit diagram of the using level-shifting inverter. When the input is low, M_d is off while gate of M_c is on. Then, the output is pulled to V_{DD}. On the contrary, when the input is high, M_d is on and the output is pulled to ground. Now, gate of M_b is also connected to ground and then it turns the M_b on. The V_{DD} is connected to the capacitor C_b and electric charges flow into the capacitor until the voltage across the capacitor reaches V_{DD}-V_{IN}. During this charging phase, M_a is also on since the voltage across C_b is still lower than V_{DD} which means the capacitor C_a is also charged at the same time.

After all of the capacitors are fully charged, M_a and M_c are turned off which results in stable output at low level when the input is high.

With the above explanation, the output at high level has the same voltage of VDD and the output at low level has the same voltage as ground. The input side, however, is completely different from the output side. The input at low level equals to ground level but the input at high level can be any voltage that is lower than V_{DD}.

Therefore, it is possible to use this level shifting inverter to connect with low-supply voltage digital logic circuit at input side while connect V_{DD} to higher voltage in order to obtain high-voltage digital output. It is clear that this circuit can be used as an inverting driver for the H-bridge switches as well.

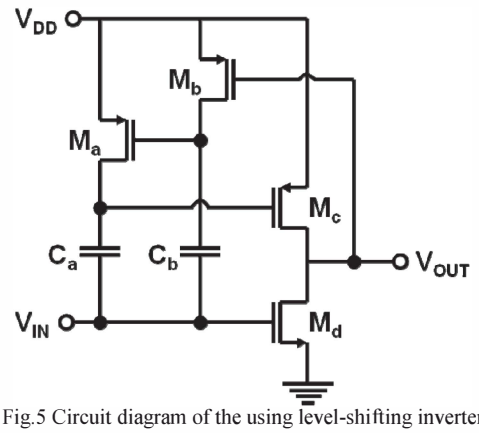

Fig.5 Circuit diagram of the using level-shifting inverter

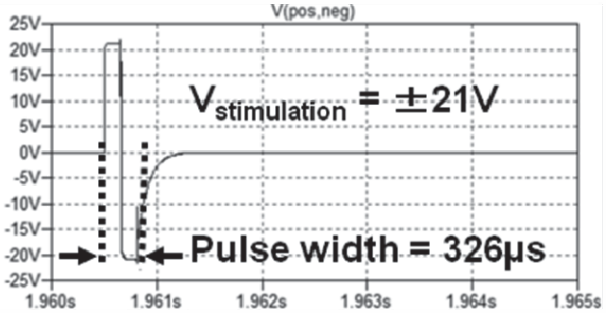

Fig.6 Simulated bi-phase pulse of the stimulator in this work

IV. Simulation Results

With the combination of the architecture in section II and the level-shifting inverter in section III, the whole system can be constructed as an actual functional electrical stimulator with bi-phasic stimulating pulse.

The controlling clocks (Φ1 and Φ2) are set to frequency of 28.6Hz with duty cycle of 0.43% which equals to pulse width of 150µs.

The boosting clock (Φ) is set to 20kHz (period of 50µs) with duty cycle of 90% in order to minimize latency of the stimulator.

In this paper, LTSpice IV is used for simulation. Fig. 6 shows the simulated bi-phasic voltage pulse with approximately 21V in amplitude. The exponential decay of the pulse in negative portion comes from discharging of the capacitor in the Electrode-Electrolyte Model. In this simulation, the load is composed of a 100Ω resistor serially with the parallel of a 1kΩ resistor and a 0.1µF capacitor.

The positive portion, however, is not completely decayed due to negative switching of the H-bridge switches in order to create the bi-phasic pulse. For the negative portion, it has plenty of time to finish its decay. With two controlling clocks of Φ1 and Φ2 together with the H-bridge switches, the stimulating pulse becomes bi-phasic pulse with the pulse width of 326µs.

TABLE I. COMPARISON OF THIS WORK WITH PREVIOUS WORKS

Item	[1]	[5]	[6]	[7]	This work
Supply voltage of output stage	---	---	±150V	+80V	+24.6V
Control method/ Control unit	Complex Digital Control	Analog control with error amplifier	Complex Digital Control	Complex Digital Control	Analog control without error amplifier
Dry-cell battery	---	---	Not mentioned	9V Battery	Two CR2032 batteries (+6V)
Battery lifetime	---	---	N/A	N/A	11 hours for continuous usage
Pulse type	Bi-phasic	Monophasic	Bi-phasic	Bi-phasic	Bi-phasic
Stimulating pulse (Voltage/Current)	0.5mA - 125mA	20mA	0 - 140mA	0 - 200mA	±21V / ±19.2mA

Although the voltage pulse shape is not so constant with some decaying period during the negative portion, the stimulating current holds around +/-19.2mA during the stimulating interval and runs off to zero during the decaying period of the voltage pulse.

Average power consumption of the stimulator in this paper is 117mW per one stimulating period at frequency of 28.6Hz and operating under a 6V supply voltage. Only two CR2032 batteries are sufficient to operate this system and it can prolong continuous usage for more than 11 hours since two CR2032 batteries supply energy at level of 1.32Wh.

Table I shows the comparison of this work among some of selected previous works. Although the previous work [5] provides the similar method, the stimulating pulse is monophasic and an error amplifier is required. This work provides a simple analog control solution for generating bi-phasic stimulating pulse without any error amplifier required.

Comparing with other digital-control works [1][6][7], these works provides more flexibility due to the digital control system but the power consumption seems to be too high for long-time continuous usage. On the other hand, this presented work is compact and consumes low-enough power for long-time usage. Hence, any patient with drop-foot problem can use this work in their daily life due to long battery lifetime.

V. CONCLUSION

This work presents a simple architecture of functional electrical stimulator which is compact and easy to implement. The presented system does not require any of complex building block. The presented architecture generates bi-phasic stimulating pulse via the H-bridge switches which must be operated together with the level-shifting inverter. The presented level-shifting inverter is also compact and allows practical implementation of the presented stimulator. Besides, the boost converter consumes power only when the stimulating pulse is required due to the clocking scheme. The system can be operated under a 6V supply voltage and the average power consumption is 117mW at operating frequency of 28.6Hz with the pulse width of 326µs. The presented work can continuously operate under two CR2032 batteries for more than 11 hours. At this level of power consumption, the presented work is very suitable for using as a portable functional electrical stimulator.

VI. FUTURE WORK

Since this work has results based on simulation tool, it is necessary to verify the result with actual test. Hardware of the presented circuit will be implemented and tested with the actual sample in the next phase.

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