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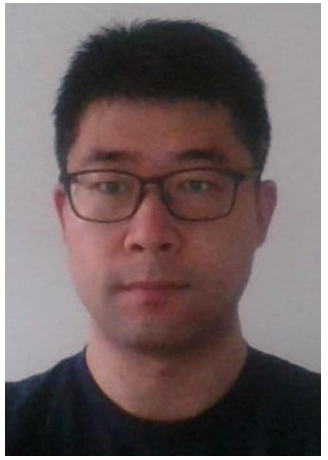

PointNet on FPGA for Real-Time LiDAR Point Cloud Processing

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WPI

Overview

- Introduction
- PointNet Structure
- Optimization
- Hardware Architecture
- System Building
- Conclusion

Introduction

- LiDAR widely used in autonomous robots and vehicles
  - Robust to lighting condition
  - Small number of data

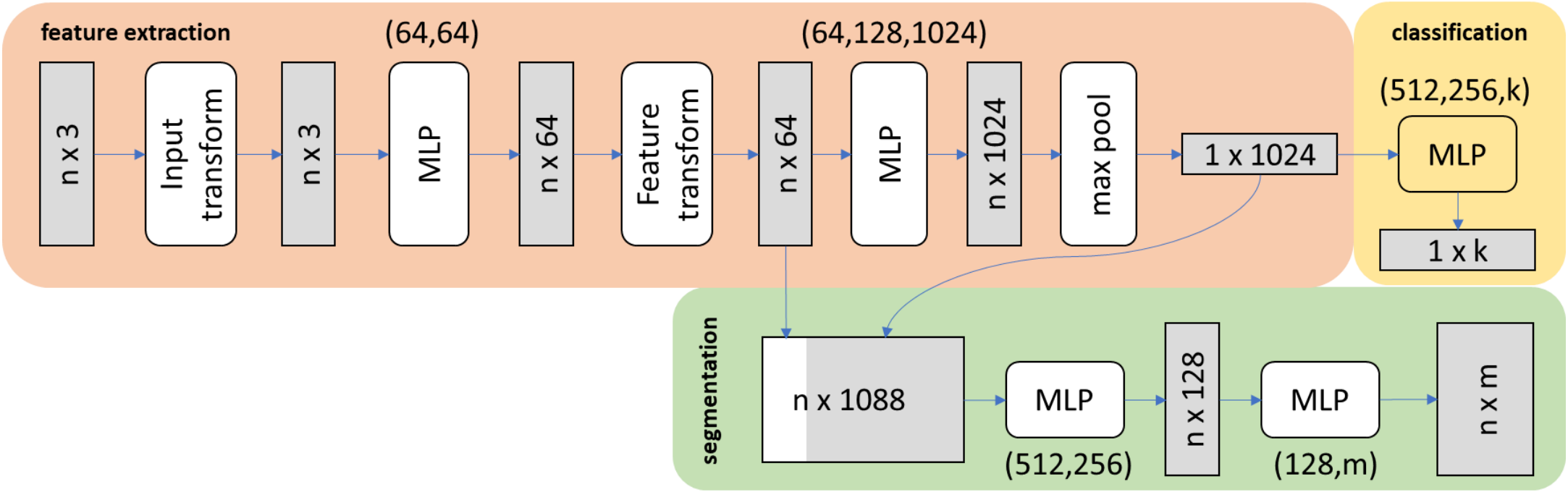
    LiDAR
    - 28.8K pixels ~ VLP-16
    - 133.33K pixels ~ HDL-64E

    Image
    - 777.6K pixels ~ 720p
    - 2M pixels ~ 1080p

Image source: https://www.vox.com/2017/11/29/16712572/general-motors-gm-new-self-driving-autonomous-cruise-car-future

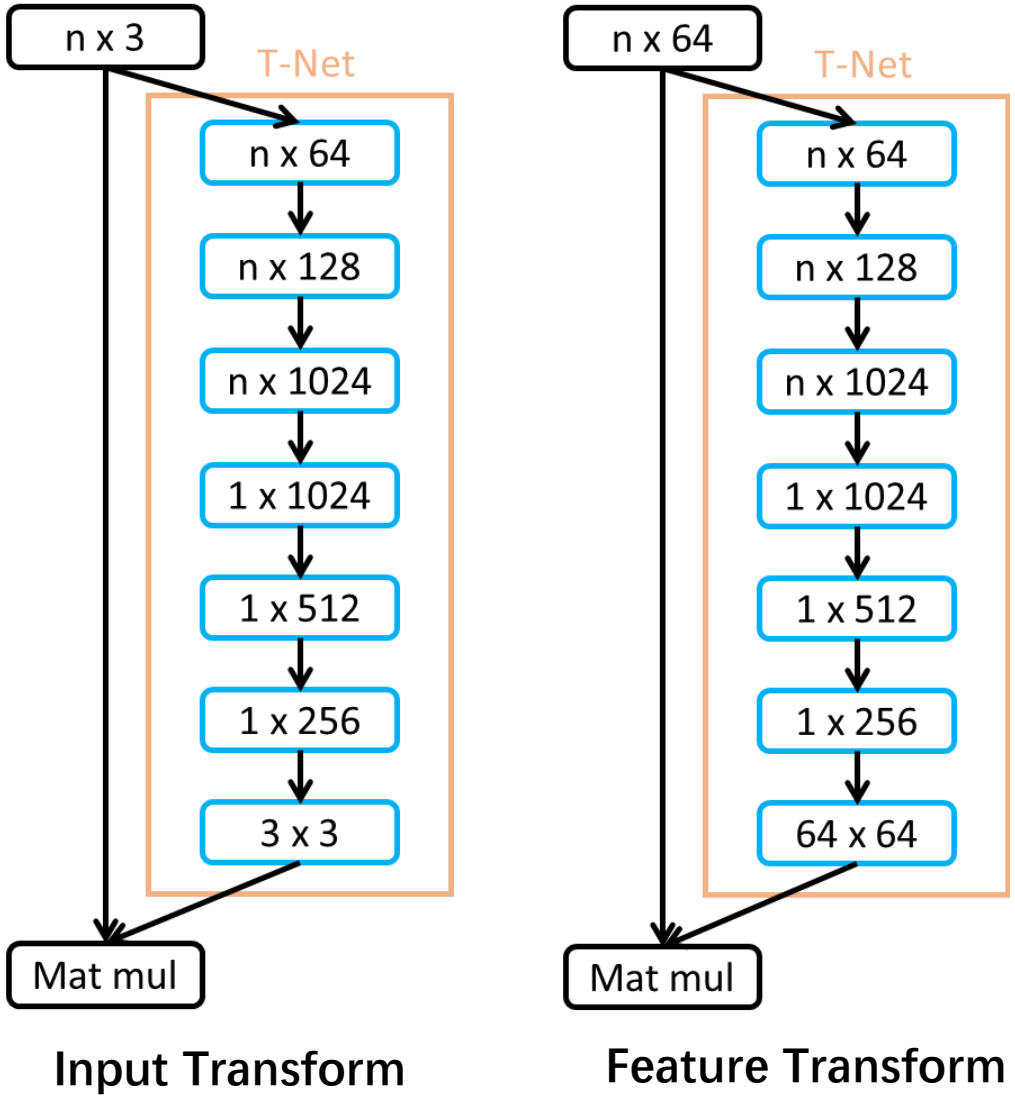
PointNet Structure

- Simple: all MLP, no convolution
- Robust: not affected by point could order, transformation



PointNet Structure

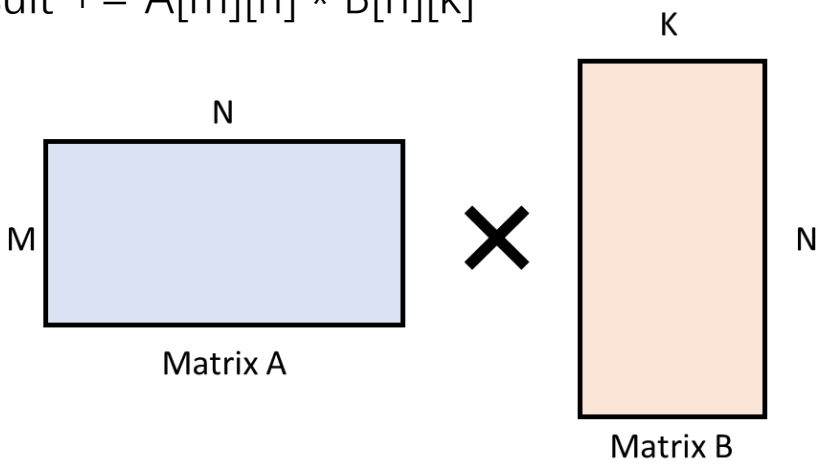
- Guarantee transformation (rotation, tarnation) invariant
- All fully connected layer (matrix multiplication)

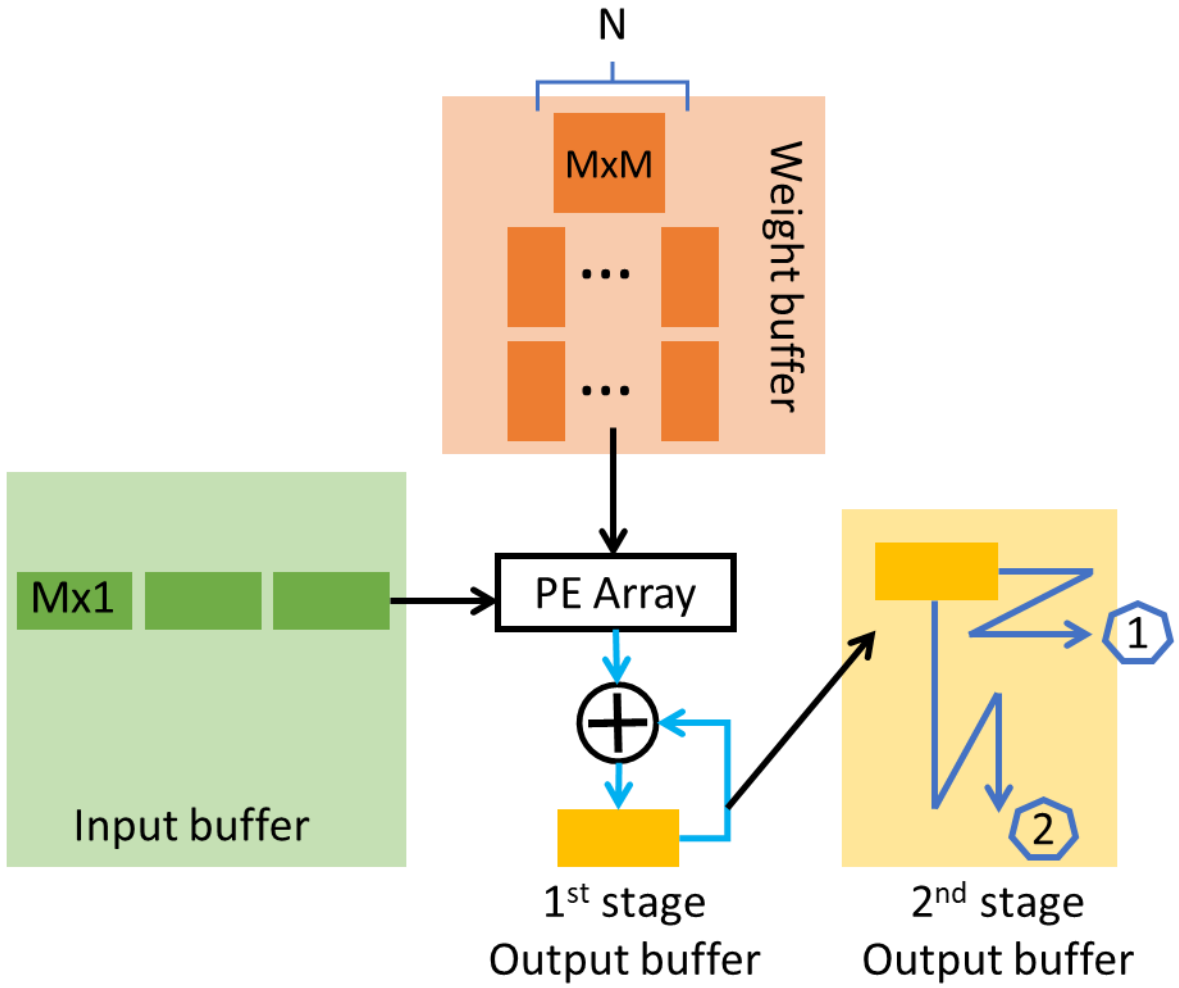


Optimization for Hardware

- Loop optimization
- Quantization

```
for m = 1:M                          -- loop-1
    for k = 1:K                      -- loop-2
        for n = 1:N                  -- loop-3
            result += A[m][n] * B[n][k]
```





Hardware Architecture

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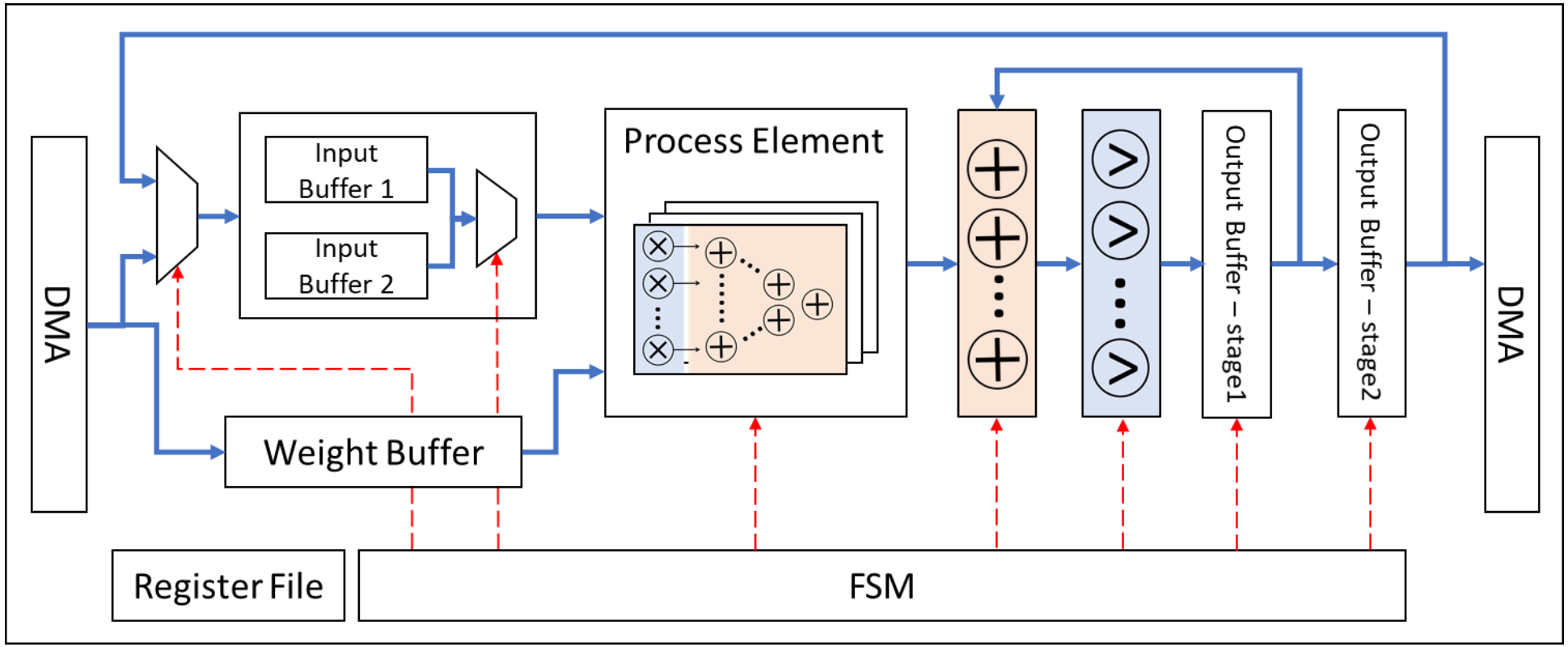
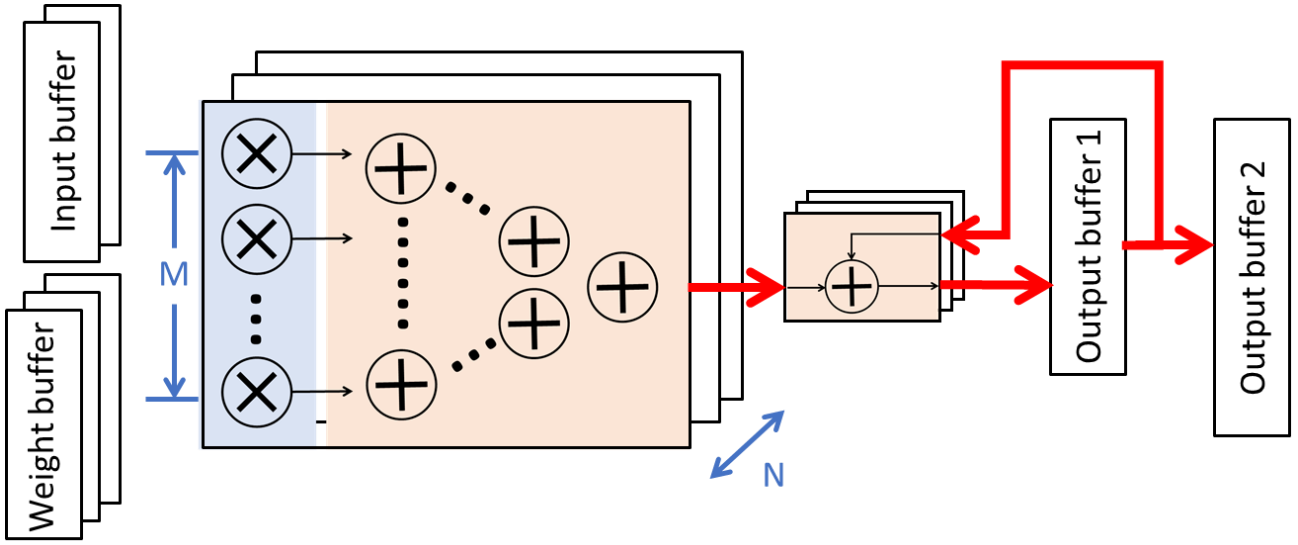
- SIMD structure



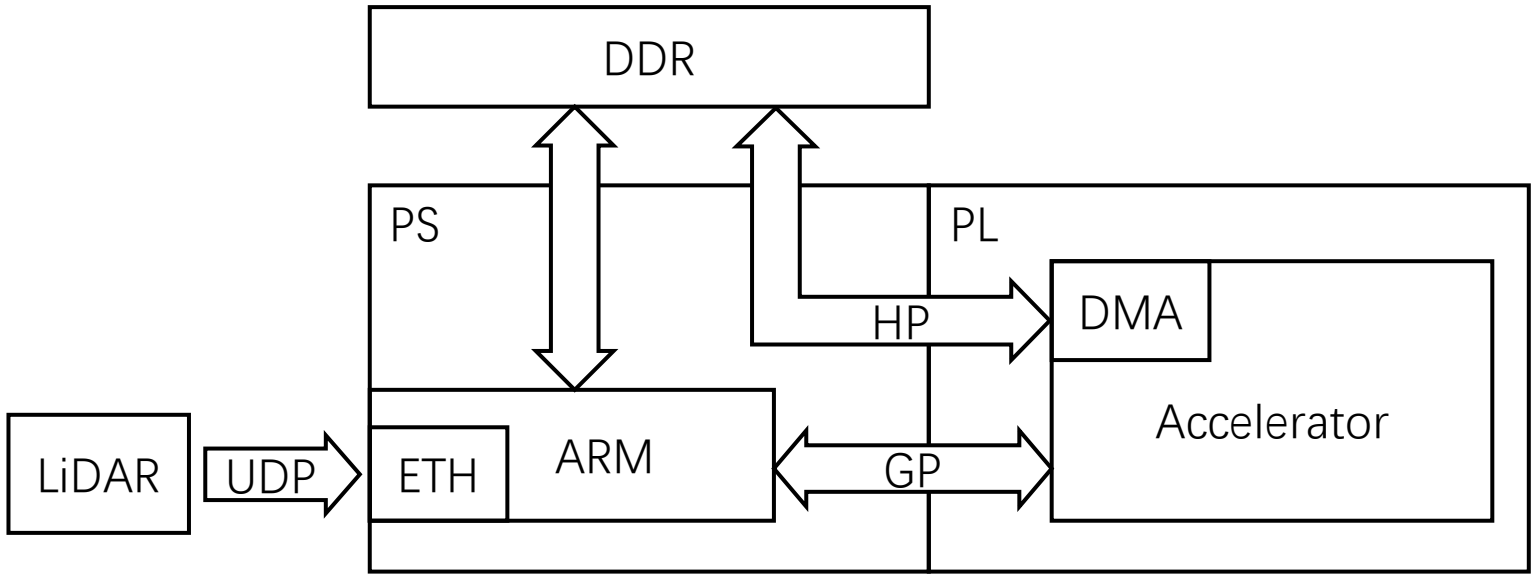
Hardware Architecture

- SIMD structure
- Two-stage buffer
  - Less accuracy loss
  - Less on-chip memory consumption



System Building

- VLP-16 connects to ZCU104 via Ethernet
- Velodyne driver is implanted into PS side (22-23 ms/set)
- DDR buffers point cloud



Performance and Results

Performance comparison

Networks	Processing Time	
	INT8	INT16
PointNet-classification	19.8 ms	27.8 ms
PointNet-segmentation	34.6 ms	42.6 ms

Resource consumption (Xilinx ZCU104)

Bit Width	LUT	FF	DSP	BRAM	URAM
INT8	19530 (8%)	36010 (8%)	1026 (60%)	114 (37%)	48 (50%)
INT16	30933 (13%)	60412 (13%)	1026 (60%)	123 (39%)	96 (100%)

Image source: https://www.xilinx.com/products/boards-and-kits/zcu104.html#:~:text=Product%20Description,)%2C%20drones%20and%20medical%20imaging.

Thank you!