Review on Event-Driven Wake-Up Sensors for Ultra-Low Power Time-Domain Design

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***Abstract*— This paper introduces a review of event-driven wake-up sensors detection approaches and investigates time domain injection-locked oscillator design solutions to reduce power consumption. Threshold-based sensing, digital classification and analog feature extraction method are presented. To overcome the power consumption limits provided by state of the art threshold detection methods, a novel threshold detection method based on injection-locked oscillator time-domain comparator is proposed and designed in a FDSOI 22 nm process. Simulations show a power consumption of 790 pW for an input full scale signal of 320 mV with a frequency of 1 kHz.**

Keywords — Internet-Of-Things (IoT), Event-Driven interfaces, Feature Extraction, Injection-Locked-Oscillator (ILO), Time domain Comparator, Unattended Sensors, Wake-Up Sensor.

I. INTRODUCTION

Internet-of-things (IoT) devices are more and more present in a lot of domains of our daily life, such as communication, security, automotive, or biomedical monitoring. They have to be context-aware systems able to measure environment parameters with the help of sensors interfaces. IoT applications require ultra-low power consumption circuits, in order to work as autonomous systems supplied with small batteries or energy harvesters. It is especially true for unattended sensors networks, as presented in the N-Zero program of DARPA [1], which have to consume less than 10 nW to reach a lifetime in the order of 10 years.

In order to reduce the power consumption of sensor interfaces, a standard way to process is to shut down a part of the circuit and only supply it when needed. It may be done with wake-up sensors (WUS) architectures. A few types of WUS exist, such as radio [2], timer [3] or optical WUS [4]. Another way to wake-up a system is to consider on-demand wake-up architectures. These are called event-driven WUS (EDWUS). An EDWUS sends a wake-up signal only when a relevant event in its environment is detected.

EDWUS may be realized with multiple approaches. This paper introduces different methods to extract events parameters from the signal to be detected. Thereafter, a time domain comparator will be proposed to be a solution in a threshold based feature extractor for ultra-low power applications, benefiting of the supply voltage reducing availability.

Section II reviews EDWUS implementation approaches. Section III proposes injection-locked oscillator (ILO) strategies to overcome presented power consumption limits, especially in introducing a time domain comparator design. Afterwards, system performances will be compared with existing circuits.

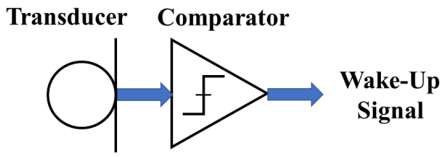

Fig. 1. Comparator based event detector.

II. EDWUS REALIZATION APPROACHES

EDWUS can be implemented in several ways, depending on application field. For sparse signals, threshold-based methods are used [5]. For a low bandwidth signal, digital acquisition and processing are used [6],[7]. For high bandwidth signal, feature extraction circuits, such as spectrum analyzer circuits are used. The next subsection introduces threshold based detection circuits.

A. Threshold-based Detecting Approaches

Threshold detection can be directly achieved in the analog domain by using an analog programmable threshold comparator [5]. Circuit architecture for such detector is depicted in Fig. 1.

The physical signal of the event is converted into electrical domain with the help of a context aware transducer. The amplitude of the signal is compared to a defined threshold which represents the detection threshold. This is a simple method to detect some sparse unattended event. A contemporary implementation of this method can be found in [5], and demonstrates a power consumption lower than 300 pW for a 10 Hz input signal. It is a suitable method to detect some sparse signals which do not need to be classified.

Main limitation of threshold based method is that it is restricted to very low bandwidth signals. They are also prone to false detection of signals that have sufficient amplitude to overpass comparator's threshold. Thus, more complex architectures with spectral classification are needed to avoid false detections.

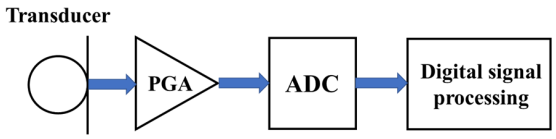

Fig. 2. Digital-based EDWUS

B. *Digital-Based EDWUS*

Another method which can be used to process a signal in an EDWUS is the classical amplifying – filtering and digital converting, acquisition circuit. The architecture of such circuit is depicted in Fig. 2. The transducer converts physical signasl to the electrical domain. This signal is then amplified and converted to digital domain by an ADC. Digital data is processed in a digital signal processing unit, and event classification is done. Such systems have been implemented in [6] ,[7] for unattended ground sensors application. The event can next be classified by analyzing the spectral components of the signal in the digital domain. Digital-based methods have demonstrated some ultra-low power consumption results, on the order of the nW, especially when using some optimized sub-threshold ADC architectures [8].

However, the bandwidth of detected signal is still limited to some hundredth of hertz to keep a power consumption on the order of nW. Sampling a wider bandwidth should imply an increase of the working frequency of these architectures, which, in turn, should dramatically increase the power consumption.

C. *Analog Feature Extraction to Higher Bandwidth*

Physical signal that have a higher bandwidth than 10-Hz and are usually more complex to classify. For instance, a spectrum from 20 Hz to 20 kHz needs to be covered to detect the entire information contained in audio signals. Spectral components of the analyzed signal can be extracted in the analog domain with analog-to-information techniques as proposed in [9]. The architecture of an analog feature extractor is presented in Fig. 3.

The feature extractor of [9] is made of amplifiers, bandpass filters and envelope detectors. The input signal is amplified and filtered by a bank of bandpass filters each centered on a particular frequency. The resulting signal is rectified by an envelope detector which gives a DC component which represents a signal parameter. Signal parameters are the information extracted from components of the input signal. This technique allows signal analysis in the analog domain, which optimizes signal recognition because only relevant information is extracted, unlike classical ADC architectures which converts whole signal bandwidth. These parameters can contribute in the classification of the input signal in the occurrence of relevant event with the help of decision trees [10].

Pattern recognition is a novel technique for reconfigurable systems that paves the way to the realization of new systems able to learn new patterns automatically [11], and becoming more and more context adapted.

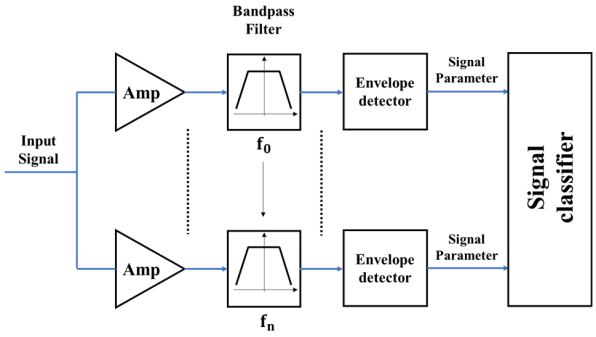

Fig. 3. Analog feature extractor.

To the best of our knowledge, state-of-the-art EDWUS based on analog feature extractor have a power consumption in the order of 10 µW. This value seems large compared to nW power consumption presented in previous section. Therefore, power consumption of these systems have to be reduced. Classical sub-threshold design can be adopted [9] to reduce power consumption of amplifying blocks. Another way to reduce power consumption is to reduce supply voltage. However, standard analog blocks cannot work with too small supply voltage. To be aware of that, time domain architectures can be adopted for signal acquisition and processing. Next paragraph introduces these structures.

D. *Time Domain Feature Extractor Architectures*

Time domain architectures for signal processing are composed of amplifiers, time encoders and time domain signal processing units. Temporal encoding of signals can be obtained by pulse width modulation, pulse density modulation or pulse position modulation. An architecture of time encoder for speech reconstruction is shown in [12] for cochlear implant. Inspired architecture is shown in Fig. 4.

This architecture is also based on a feature extractor, the difference is that the features are processed in the temporal domain. Advanced techniques of time domain signal filtering, using non-linear ring oscillators, and sorting are shown in [13] and [14]. These architectures can benefit from reduced supply voltage and become more power efficient.

III. DESIGN STRATEGIES FOR ILO BASED ARCHITECTURES

In this section we show how ILO can be used to reduce power consumption in time domain architecture. This architecture is proposed to be designed in a 22 nm FDSOI process.

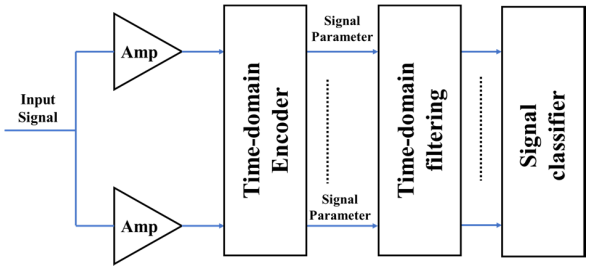

Fig. 4. Time domain feature extractor.

A. RS-Based ILO Circuit implementation

Theoretical principia of ILOs have been studied [15]. This kind of oscillators can lock to the frequency of an injection signal. Schematic of the proposed circuit is given in Fig. 5.

The oscillator works as follows: if we consider that $Q = 1$ and $\bar{Q} = 0$ for initial conditions, then transistor P1 is ON and N1 is OFF. I_{BIAS} charges the capacitor C_1. When C_1 voltage overpasses the threshold voltage of the inverters, the state of R is equal to 1 and the new state of $Q = 0$ and $\bar{Q} = 1$. The bias current is now directed to C_2 and charges it. The charge of C_2 inverts the state and begins the oscillation. P_1 and P_2 transistors switch the bias current source alternatively to each C_1 or C_2 capacitor and allow the use of only one bias current source. Its free running frequency f_0 can be expressed as follows:

$$f_0 = \frac{I_{\mathrm{BIAS}}}{2CV_{\mathrm{thINV}}} \quad (1)$$

Where I_{BIAS} is the bias current of the oscillator, $C = C_1 = C_2$ are capacitance value, and V_{thINV} is the threshold voltage of the inverters.

Injection current I_{INJ} is pushed and pulled into C_1 and C_2 thanks to switching inverter-based current injection circuit controlled by V_{INJ} and allows ILO output signal to be locked on injection frequency. A phase shift of output signal depending on f_0 and injection frequency f_{INJ} is introduced by injection locking, and will be studied in the next part.

Two ILO-based architectures are proposed to contribute to EDWUS architectures: an ultra-low power phase shifter which can be used in time domain ADC application, and an ultra-low power time domain comparator for threshold based applications.

B. ILO-Based Phase Shifter

An ILO can be used as a phase shifter, thanks to its frequency locking property. Output phase shift properties have been demonstrated in [16] for this kind of oscillator structure. A control signal V_{CTRL} is applied on the back-gate of FDSOI

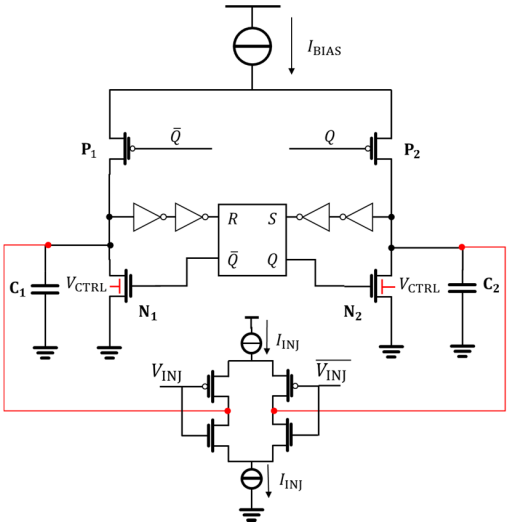

Fig. 5. Proposed ILO architecture.

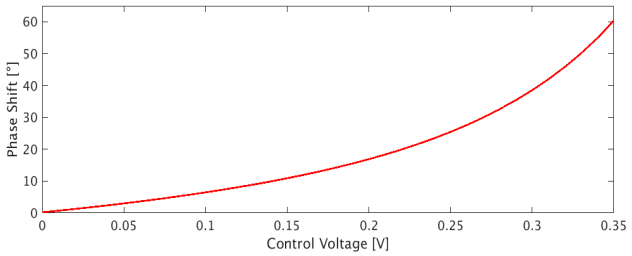

Fig. 6. ILO phase shift in function of control voltage.

MOS switches N_1 and N_2 to control f_0, as demonstrated in [17]. Although ILO output frequency is still locked on f_{INJ}, phase of output signal is shifted in function of the amplitude of V_{CTRL}. Phase shift introduced by this structure is presented in Fig. 6.

The injection current is up to 250 pA, which leads to a locking range of 8 KHz. The frequency of V_{CTRL} is 1 KHz. Measured phase shift spans 60° for control voltages between 0 mV and 320 mV. This property is suitable for time domain ADC as a voltage-to-time converter. This has been demonstrated in [16] for high temperature application. For EDWUS applications, phase shift characteristics can be used for time domain comparators, in charge to detect a relevant event. This will be studied in next subsection.

C. Time Domain ILO Comparator

State-of-the-art comparator for threshold based sensing method is presented in [5]. This comparator demonstrates a 270 pW power consumption for a 100µV, 10 Hz input signal. This structure is very interesting for ground sensors applications applications that require architectures that have high sensitivity over a low-bandwidth. The power consumption will increase for high frequency signals and has to be harnessed to be compatible with ULP applications.

An architecture of ultra-low power time domain comparator is presented in Fig. 7. Phase shift between an input signal and a reference signal is compared. The input signal V_{CTRL} is compared to the threshold V_{REF}. The asynchronous D Flip-Flop (DFF) works as a lead/lag comparator, which determines the sign of the phase shift between both signals. This architecture allows the comparison of two analog signals in the time domain thanks to ILO phase shifter properties, and only takes into account the power consumption of two ILOs and a DFF.

Time domain comparator has been simulated a 22 nm FDSOI process. Input signal amplitude is about 160 mV, which represents a full scale output amplitude of a ULP physical-to-voltage sensor interface. The circuit power supply is 0.4V and ILOs are synchronized on a 16 KHz frequency. This span allows getting some programmable thresholds. The comparator architecture is realized to make the time domain comparator.

Result of the comparison with a 0.2V threshold voltage is shown in Fig. 7. Power consumption of the time domain comparator is 790 pW for a 1 KHz 320 mV input signal. A peak overshoot of 100 mV appears, due to the charge and discharge of parasitic capacitances. This result has to be compared with the comparators shown in [5].

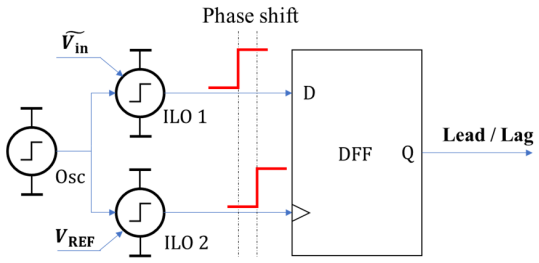

Fig. 7. Proposed time domain ILO-based comparator.

This performance can be seen in terms of energy per cycle. [5] presents an energy per cycle of 2nJ/cycle for programmable threshold from 27 to 46 mV, while the proposed ILO-based time domain comparator performance is 790 fJ/cycle for a 320 mV input. Performances and comparison with existing analog comparators are shown in Table I.

IV. Conclusion

This paper reviewed architectures of Ultra-Low Power EDWUS. These circuits can be achieved by threshold based sensing circuits for sparse signature events. Feature extraction allows the analysis of more complex signals and recognition of its spectral signature. Time domain architectures can be implemented to decrease power consumption, by lowering supply voltage.

The use of ILO as phase shifter or as comparator seems to be a promising way towards the reduction of the power consumption of time domain architecture of EDWUS. In particular, an ILO based time domain comparator has been implemented and tested for threshold sensing. Its power consumption is 790 pW for a 1 KHz input frequency, for a 0.2V threshold.

This time domain architecture may be the beginning of a time domain EDWUS.

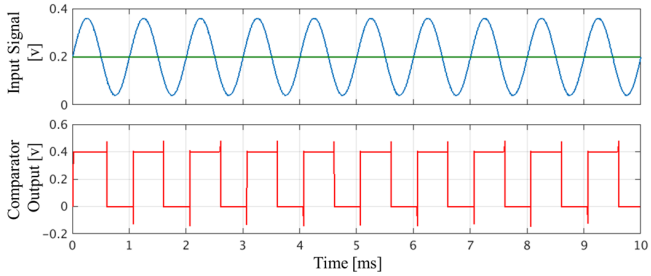

Fig. 8. Time domain comparator simulation.

TABLE I. Comparator perofrmances comparison

	[18]	[5]	This Work
Technology	9HP BiCMOS	65nm CMOS	22nm FDSOI
Architecture	Analog	Analog	Time Domain
Power	684 pW	24 nW	790 pW
Vthreshold	0 -30 mV	17 -46.5 mV	0-320 mV
Fmax	160KHz	1KHz	1KHz
Energy/cycle	nc	2nj/cycle	790 fJ/cycle

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