

## Module - 5

Topics to be covered :-

- ① Number System and Conversion
- ② Boolean Algebra
- ③ Logic Gates
- ④ Boolean Diagram Analysis
- ⑤ Boolean Expression Minimization
- ⑥ Arithmetic Circuits
  - Half adder
  - Full adder
  - Half subtracter
  - Full subtracter
  - Multipliers

- ⑦ K-map
- ⑧ Sequential Circuits
  - Flip-flop
  - Mux - Demux
  - Encoders - Decoders

### Number Conversions :-

- Binary to decimal
- Binary to octal
- Binary to Hexadecimal
- Octal to decimal conversion
- Octal to binary
- Octal to hexadecimal
- Decimal to binary
- Decimal to octal
- Decimal to hexadecimal
- Hexadecimal to binary
- Hexadecimal to decimal
- Hexadecimal to octal

Binary :  $(0,1) \rightarrow (0110)_2$

Decimal :  $(0-9) \rightarrow (7934)_{10}$

Octal :  $(0-7) \rightarrow (5642)_8$

Hexadecimal :  $(0-9) \rightarrow (98AC)_{16}$

$0 = 0000$	$6 = 0110$	$8 \ 4 \ 2 \ 1 [R_u_4]$
$1 = 0001$	$7 = 0111$	$(2^3) \ (2^2) \ (2^1) \ (2^0)$
$2 = 0010$	$8 = 1000$	$1 \ 0 \ 0 \ 0$
$3 = 0011$	$9 = 1001$	$1 \ 0 \ 0 \ 1$
$4 = 0100$	$A = 1010$	$E = 1110$
$5 = 0101$	$B = 1011$	$F = 1111$
$6 = 0110$	$C = 1100$	$D = 1101$
$7 = 0111$	$D = 1101$	$S \ S \ S \ O$
$8 = 1000$		$S \ S \ O \ O$

Binary to Decimal Conversion :-

$$(2^2 \ 2^0 \ 2^4 \ 2^5 \ 2^2 \ 2^0 \ 2^1 \ 2^3 \ 2^5 \ 2^7 \ 2^9) \Rightarrow ( )_{10}$$

$$(3 \times 2^{12}) + (3 \times 2^{11}) + (1 \times 2^9) + (1 \times 2^7) + (3 \times 2^6) + (1 \times 2^4) + (3 \times 2^2) + (3 \times 2^1) + (1 \times 2^{-2}) + (3 \times 2^{-5}) + (3 \times 2^{-7}) + (3 \times 2^{-8})$$

$$= 4096 + 2048 + 512 + 128 + 64 + 36 + 4 + 2 + 0.25 + 0.125 \\ 0.03325 + 0.0078125 + 0.00390625$$

$$= 6870.45796875$$

Binary to Octal Conversion :-

$$(031 | 050 | 105 | 051 | 105 | 050 | 111 | 015)_{2} \\ 3 \quad 2 \quad 5 \quad 3 \quad 5 \quad 2 \quad 7 \quad 3 \\ (32535.273)_{8}$$

Binary to Hexadecimal Conversion :-

$$(1110 | 1011 | 1011 | 0010 | 1010 | 1101 | 0000)_{2} \\ E \quad B \quad B \quad 2 \quad A \quad D \quad 0 \\ (EBB2.A00)_{16}$$

Decimal to Binary Conversion :-

$$(152.25)_{10}$$

$$0.25 \times 2 = 0.5 (0)$$

$$0.5 \times 2 = 1.0 (1)$$

$$(10011000.01)_{2}$$

2	152	
2	76	— 0
2	38	— 0
2	19	— 0
2	9	— 1
2	4	— 1
2	2	— 1
2	1	— 0

### Decimal to Octal Conversion :-

$$(152.25)_{10}$$

$$0.25 \times 8 = 2.0$$

8	152
8	19 — 0
2	— 3

$$(230.2)_8$$

### Decimal to Hexadecimal Conversion :-

$$(152.25)_{10}$$

$$0.25 \times 16 = 4.0$$

$$16 \mid 152$$

$$\begin{array}{r} 9 \\ - 8 \\ \hline \end{array}$$

$$(98.4)_{16}$$

### Octal to Decimal Conversion :-

$$(7652.865)_8$$

$$8^3 \ 8^2 \ 8^1 \ 8^{-1} \ 8^{-2} \ 8^{-3}$$

$$\begin{aligned}
 &= (7 \times 8^3) + (6 \times 8^2) + (5 \times 8^1) + (2 \times 8^0) + (3 \times 8^{-1}) + (6 \times 8^{-2}) \\
 &= 3584 + 384 + 53 + 2 + 0.875 + 0.09375 + 0.009765 \\
 &= 3983.478525
 \end{aligned}$$

### Octal to Binary Conversion :-

$$(5643.256)_8$$

$$256 \downarrow \quad \quad \quad 256 \downarrow \quad \quad \quad 256 \downarrow$$

$$0SD \quad 0SD \quad 0SD$$

$$[5643]$$

$$(SOS\ SD\ SOD\ OSS. OSD\ SOSS\ SD)_2$$

### Octal to Hexadecimal Conversion :-

$$(5643.256)_8$$

↪ Convert to Binary [SGP-5]

↪ Convert to Hexadecimal [SGP-3]

8	2	8	2	2	1	7	1	7	2	1	0
10	5	10	5	10	5	10	5	10	5	10	5
9	1	10	3	1	5	1	7	1	0	0	0

$$7(8) : 6(4)$$

$$(BA3.570)_{16}$$

## Hexadecimal to Decimal Conversion :-

$$\begin{aligned}
 & \left( 9786.5476 \right)_{16} \\
 &= (9 \times 16^3) + (7 \times 16^2) + (8 \times 16^1) + (6 \times 16^0) + (5 \times 16^{-1}) \\
 &\quad + (4 \times 16^{-2}) + (7 \times 16^{-3}) + (6 \times 16^{-4}) \\
 &= 36864 + 2792 + 24 + 6 + 0.8125 + 0.015625 + \\
 &\quad 0.000709 + 0.000091 \\
 &= 38686.329925
 \end{aligned}$$

## Hexadecimal to Binary Conversion :-

$$\begin{array}{c}
 (A D E 9 8 . 7 9 C 5)_{16} \\
 \downarrow \quad \downarrow \\
 1010 \ 1100 \ 1101 \ 1000 \ 0101 \ 1100 \ 0101 \ 0101 \\
 [A D E 9 8] \\
 (1010110011011000.0101110011000101)_2
 \end{array}$$

$$(1010110011011000.0101110011000101)_2$$

## Hexadecimal to Octal Conversion :-

$$(A D E 9 8 . 7 9 C 5)_{16}$$

Convert to Binary [Step - I]

Convert to Octal [Step - II]

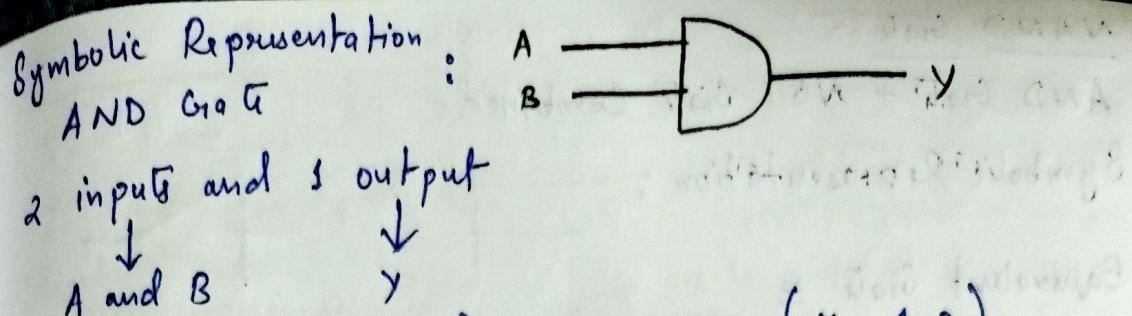
$$\begin{array}{c|c|c|c|c|c|c|c|c|c}
 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 \\
 1 & 2 & 6 & 6 & 3 & 0 & 3 & 6 & 3 & 4 & 2 \\
 1010110011011000.0101110011000101 & & & & & & & & & & \\
 (326630.3634)_8
 \end{array}$$

## Boolean Algebra :-

### Logical Gates :-

They are classified into three types :-

- ① Basic Logic Gates — AND, OR, NOT (Invert) Gates
- ② Universal Logic Gates — NOR Gate and NAND Gate
- ③ Advanced Logic Gates — XOR Gate and XNOR Gate



The Boolean Expression for AND Gate =  $(Y = A \cdot B)$

Truth Table :-

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Observation : If any one of the input is 0, then the output is 0. If both inputs are 1, output is high (1).  
0 = low  
1 = high

OR Gate :-

Symbolic Representation :

Boolean Expression :  $(Y = A + B)$

Truth Table :-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Observation : Any one of the input is high, output is high. If both inputs are low, the output is low.

NOT Gate :-

Symbolic Representation : A ——————→ Y

Boolean Expression :  $(Y = \bar{A})$

There's only one input and output



Truth Table :-

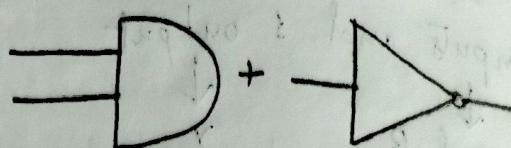
A	Y
0	1
1	0

Observation : If the input is low, the output will be high and vice-versa.

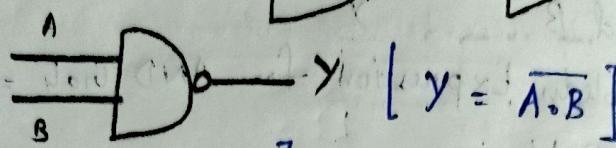
## NAND Gate :-

AND Gate + NOT Gate Combined

Symbolic Representation :



Equivalent Gate =



[ Inverse of the AND Gate ]

Truth Table :-

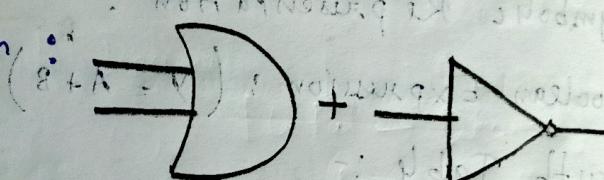
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Observation : If both the inputs are low, the output is high, vice-versa and if one of the inputs is high, the output is high.

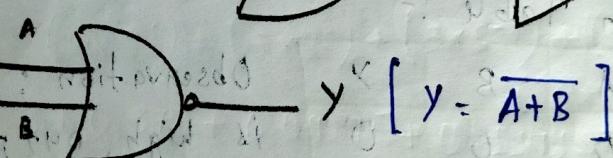
## NOR Gate :-

NOT Gate + OR Gate Combined

Symbolic Representation :



Equivalent Gate =



[ Inverse of the OR Gate ]

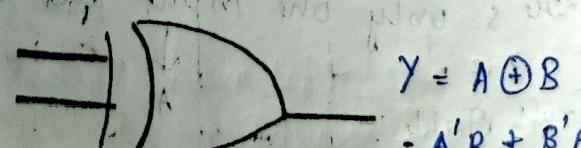
Truth Table :-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Observation : If both the inputs are low, the output is high, vice-versa and if one of the inputs is low, the output is low.

## XOR-Gate :-

Symbolic Representation :



Truth Table :-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

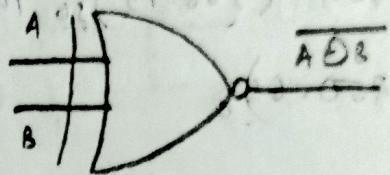
Observation : Low output for equal inputs otherwise high output.

X-NOR Gate :-  
 XOR Gate + NOT Gate Combined  
 $y = \overline{A \oplus B} = \overline{A'B + B'A}$

Truth Table :-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Observation : High output for equal inputs otherwise low output overall.  
 Symbolic Representation :



H.W. #

a) Convert  $(11100000101.001001000)_2$  into decimal.  
 [Binary  $\rightarrow$  Decimal]

$$\begin{aligned}
 & (11100000101.001001000)_2 \\
 &= (1 \times 2^9) + (1 \times 2^8) + (1 \times 2^7) + (1 \times 2^6) + (1 \times 2^5) + (1 \times 2^4) + \\
 &\quad (1 \times 2^3) + (1 \times 2^2) + (1 \times 2^1) + (1 \times 2^0) + (0 \times 2^{-1}) + (0 \times 2^{-2}) + \\
 &\quad (0 \times 2^{-3}) + (0 \times 2^{-4}) + (0 \times 2^{-5}) + (0 \times 2^{-6}) \\
 &= 537 + 256 + 128 + 64 + 32 + 16 + 8 + 4 + 2 + 1 + 0.125 + 0.0625 + 0.03125 + 0.015625 \\
 &= 905.575875
 \end{aligned}$$

b) Convert  $(11100000101.001001000)_2$  into octal.

$$\begin{array}{cccc|cc}
 2^7 & 2^6 & 2^5 & 2^4 & 2^3 & 2^2 & 2^1 & 2^0 \\
 1 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \\
 \hline
 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0
 \end{array} \quad (\text{Binary} \rightarrow \text{Octal})$$

$$(1605.130)_8 \quad 0210 \quad 0110 \quad 0100$$

c) Convert  $(11100000101.001001000)_2$  into hexadecimal.

$$\begin{array}{cccc|cc}
 2^7 & 2^6 & 2^5 & 2^4 & 2^3 & 2^2 & 2^1 & 2^0 \\
 1 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \\
 \hline
 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0
 \end{array} \quad (\text{Binary} \rightarrow \text{Hexadecimal})$$

$$\begin{array}{cccc|cc}
 2^7 & 2^6 & 2^5 & 2^4 & 2^3 & 2^2 & 2^1 & 2^0 \\
 1 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \\
 \hline
 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0
 \end{array} \quad (\text{Binary} \rightarrow \text{Hexadecimal})$$

$$(3.85.2C0)_{16}$$

Q) Convert  $(368.75)_{10}$  into Binary. [Decimal  $\rightarrow$  Binary]

Multiply after decimal digit repeatedly by 2 → Track integer part

168	
84	
42	
21	
10	
5	
2	
1	

$0.75 \times 2 = 1.5$  Until fractional part becomes zero.

$0.5 \times 2 = 1$

$\rightarrow 0.55$

$(10101000.55)_2$

a) Convert  $(568.75)_{10}$  into Octal. [ Decimal  $\rightarrow$  Octal ]

$$(250.6)_8 \quad 0.75 \times 8 = 6 \quad \begin{array}{r} 8 \\ \hline 8 & 21 \\ - & 2 \\ \hline 0 & 5 \end{array}$$

9) Convert  $(568.75)_{10}$  into Hexadecimal. [Decimal  $\rightarrow$  Hexadecimal]

$$(A8.c)_{sl} \quad 0.75 \times 16 = 12 \quad = c \quad \begin{array}{r} 16 \\ \hline 168 \\ 16 \\ \hline 8 \end{array}$$

9) Convert  $(8743.866)_8$  into Decimal. [Octal  $\rightarrow$  Decimal]

$$(7^3 \ 7^2 \ 7^1 \ 7^0 \cdot 7^{-1} \ 7^{-2} \ 7^{-3})_8$$

$$= (7 \times 8^3) + (7 \times 8^2) + (4 \times 8^1) + (8 \times 8^0) + (3 \times 8^{-1}) + (6 \times 8^{-2}) \\ + (6 \times 8^{-3})$$

$$= 3584 + 498 + 82 + 3 + 0.375 + 0.09375 + 0.01575875 \\ = (4087.48046875)_{10}$$

Q) Convert  $(7743.366)_8$  into Binary. [Octal  $\rightarrow$  Binary]

(7 7 4 3 . 3 6 6)8  
↓ ↓ ↓ ↓ ↓ ↓ ↓  
0551 0553 0500 0555 0550 0550

( sssssss 3000ss. 0ssssss )<sub>2</sub>

Q) Convert  $(7743.366)_8$  into Hexadecimal [Octal  $\rightarrow$  Hexadecimal]

( 7743.366 ) 8

↳ Convert to Binary

→ Convert to Hexadecimal

$\begin{smallmatrix} 1 & 2 & 2 & 2 & 2 \\ 1 & 2 & 2 & 2 & 2 \end{smallmatrix}$	$\begin{smallmatrix} 3 & 3 & 3 \\ 0 & & \end{smallmatrix}$	$\begin{smallmatrix} 0 & 0 & 1 & 1 \\ 5 & & & \end{smallmatrix}$	$\begin{smallmatrix} 0 & 1 & 1 & 1 \\ 5 & 5 & 5 & 5 \end{smallmatrix}$	$\begin{smallmatrix} 3 & 0 & 3 & 1 \\ 2 & 2 & 2 & 2 \end{smallmatrix}$
15 (P)	34 (E)	3	7	31 (B)

(FE3.7B)cc

8) Convert (8942.6846) into Decimal

$$\left( \begin{smallmatrix} 16^1 & 16^2 & 16^1 & 16^0 & 16^{-1} & 16^{-2} & 16^{-3} \\ 8 & 9 & 4 & 2 & 6 & 8 & 4 \\ 6 & 6 & 6 & 6 & 6 & 6 & 6 \end{smallmatrix} \right)_{36}$$

[ Hexadecimal  $\rightarrow$  Decimal ]

$$= (8 \times 36^3) + (9 \times 36^2) + (4 \times 36^1) + (2 \times 36^0) + (6 \times 36^{-1}) + \\ (8 \times 36^{-2}) + (4 \times 36^{-3}) + (6 \times 36^{-4})$$

$$= 32768 + 2304 + 64 + 2 + 0.375 + 0.03325 + \\ 0.0009765625 + 0.00009155273$$

$$= (35138.407818555),_0$$

q) Convert  $(8942.684)_ {16}$  into Binary [Hexadecimal  $\rightarrow$  Binary]

( 8 9 4 2 . 6 8 4 6 )<sub>S6</sub>

↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓

1000 1001 0110 0011 0110 0100 0101 0110

↓    ↓    ↓    ↓    ↓    ↓    ↓    ↓

08 09 04 02 . 06 08 04 06

$$(1000100101000010.01101000010001)_2$$

q) Convert  $(8942.6846)_{16}$  into Octal [Hexadecimal  $\rightarrow$  Octal]

(8942.6846) 36

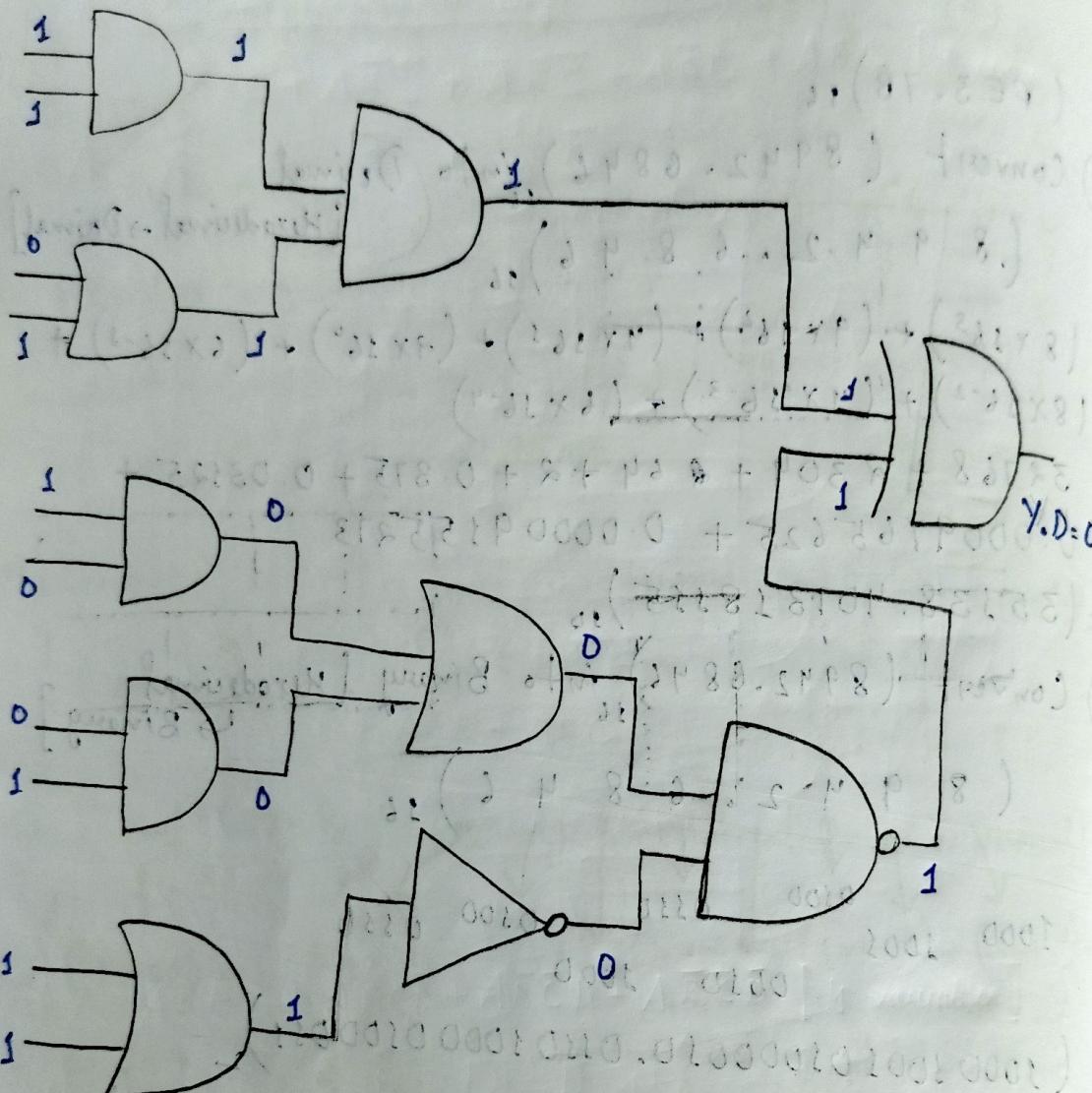
↳ Convert to Binary

Convert to Octal

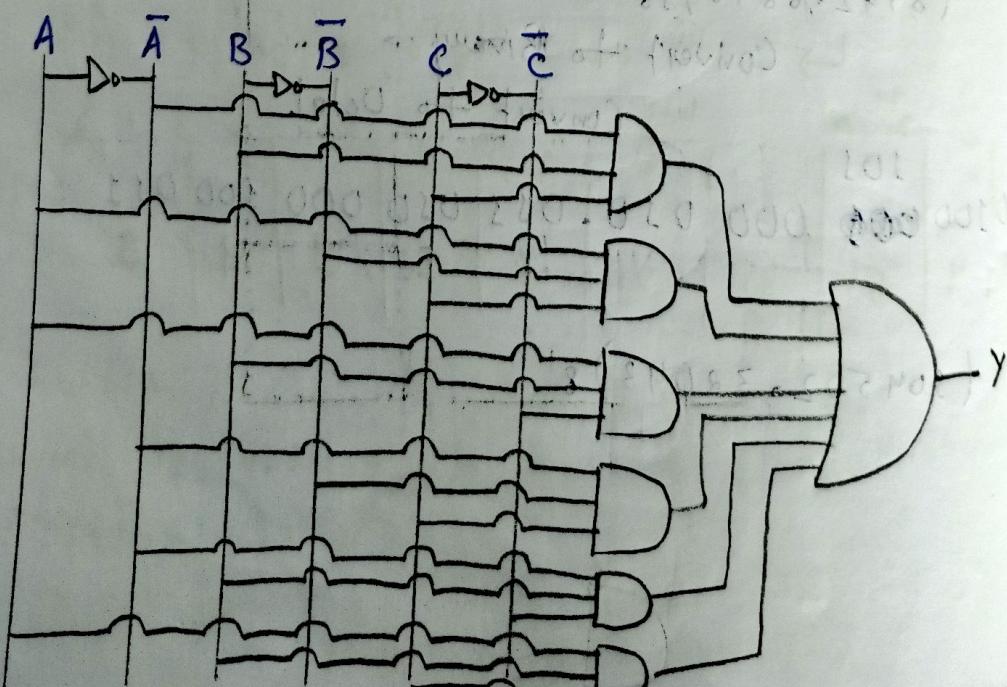
Convert to Octal									
2 <sup>20</sup>		2 <sup>18</sup>		2 <sup>16</sup>		2 <sup>14</sup>		2 <sup>12</sup>	
1000	100	100	000	050	051	051	050	000	100
10	4	5	0	2	3	2	0	4	3

(304502.32043) 8

## Boolean Algebra :-



$$\overline{ABC} + A\overline{B}C + AB\overline{C} + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C} + ABC = Y$$



## K-Map :-

Used to minimize the Boolean Expression.  
Maximum minimization can be achieved.

3  
4 } Variable

$$Y = \sum (0, 1, 2, 3, 5, 7)$$

A\BC	00	01	11	10
0	1	1	1	1
1	0	1	1	0

$$\begin{aligned} 2^0 &= 1 \\ 2^1 &= 2 \\ 2^2 &= 4 \\ 2^3 &= 8 \\ 2^4 &= 16 \end{aligned}$$

Priority  
bottom  
to top

Value given in que. → 1  
Not given in que. → 0

A\BC	00	01	11	10
0	1	1	1	1
1	1	1	1	1

A\BC	00	01	11	10
0	1	1	1	1
1	1	1	1	1

$$Y = \bar{A}B + \bar{B}\bar{C} + A\bar{C} + A\bar{B}C$$

Groups of 1 are made according to priority.  $Y = C + B$

4 pair — 1 variable

2 pair — 2 variables

1 pair — 3 variables

Boolean

Expression

## 4-Variable :-

$$Y = \{0, 3, 2, 5, 6, 8, 9, 12, 13, 14, 15\}$$

AB\CD	00	01	11	10	11	10
00	1	0	1	1	0	1
01	0	1	1	1	1	0
11	1	1	1	0	1	1
10	1	1	0	1	1	1

Interchange

$$Y = AC + \bar{C}D + \bar{B}\bar{D} + ABD + \bar{A}C\bar{D}$$

2 1's comb. — 3 vars.

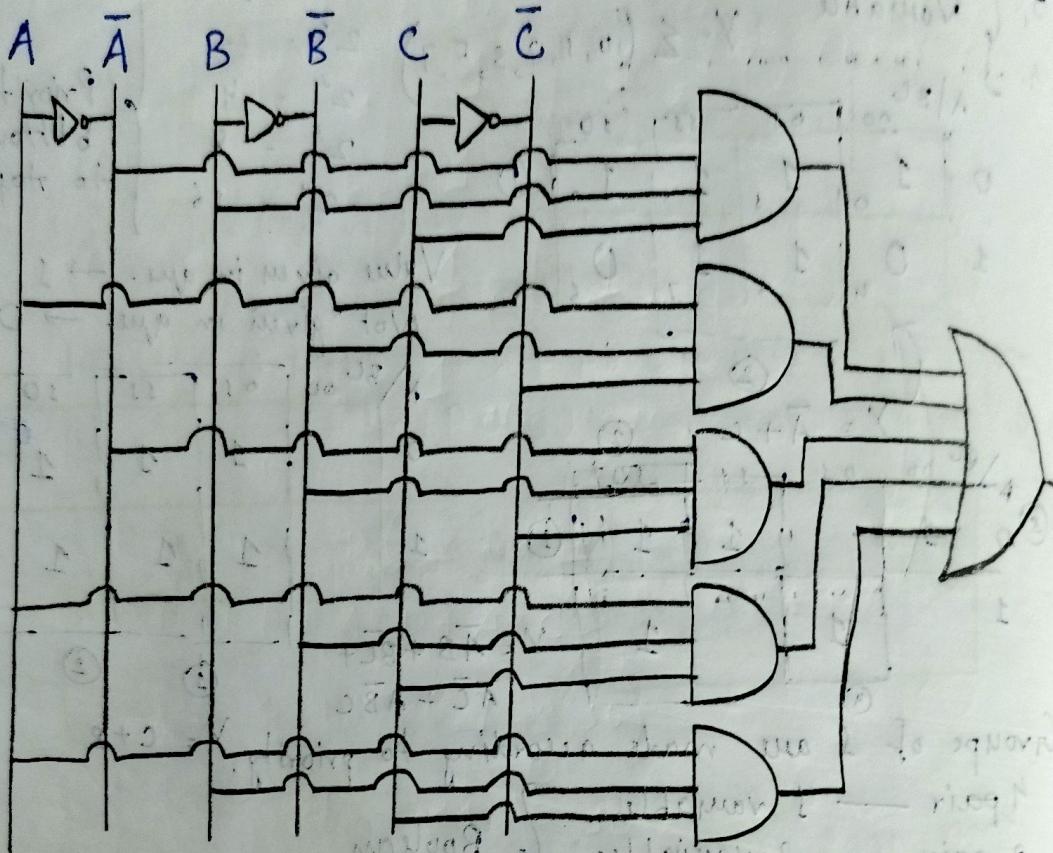
4 1's comb. — 2 vars.

8 1's comb. — 1 var.

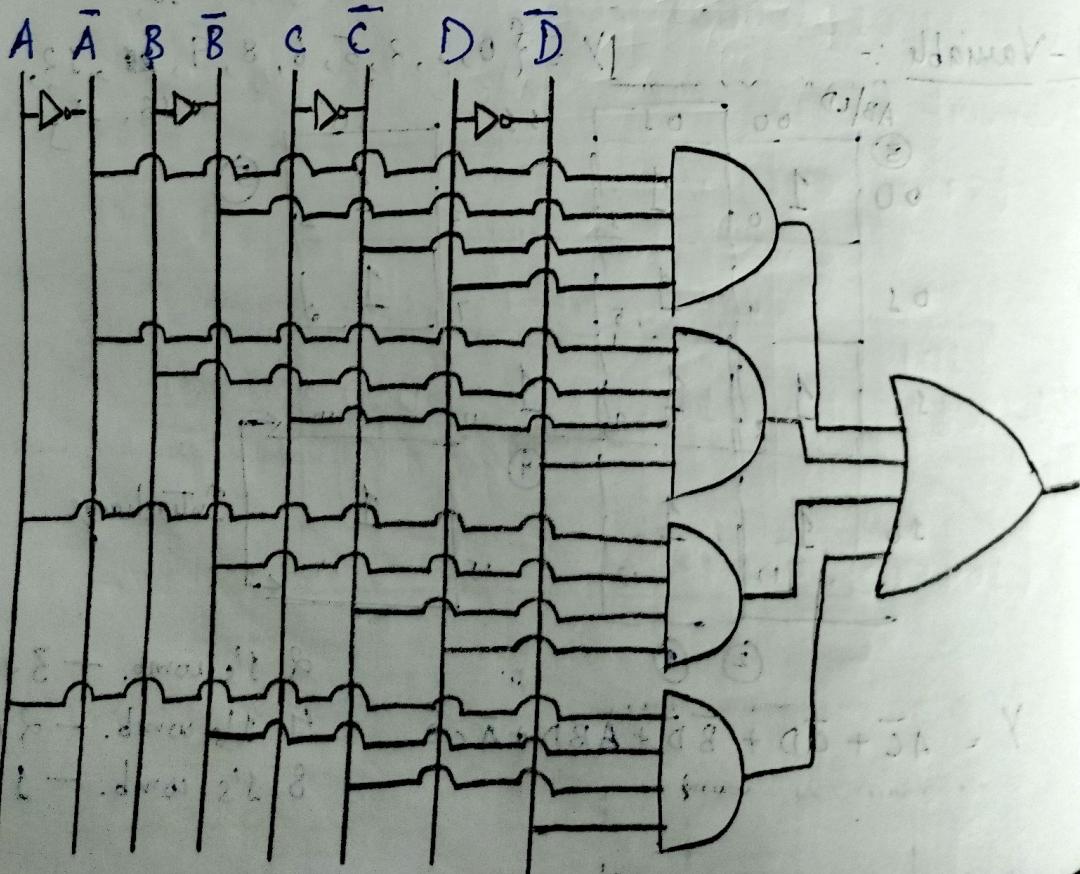
H.W 15

## Boolean Expression to Logic Gates :-

①  $Z = \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$  [3 variables]



②  $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D}$  [4 variables]



K-Map :- [ 3 variables ]

①  $y = \sum (0, 3, 4, 6, 7)$ :

	00	01	11	10
0	1 <sub>0</sub>	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>
1	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>

No. of Groups = 2 ( $\text{II}$  and  $\text{I}$ )

$$y = ① + ②$$

$$y = \bar{C} + AB$$

②  $y = \sum (1, 3, 4, 5, 6, 7)$ :

	00	01	11	10
0	0	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>
1	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>

No. of Groups = 2 ( $\text{II}$  and  $\text{V}$ )

$$y = ③ + ②$$

$$y = C + A\bar{C}$$

$$= A(A + A\bar{B}) + C(C + C\bar{A}) = A + C$$

③ ②

③  $y = \sum (1, 2, 3, 4, 5)$ :

	00	01	11	10
0	0	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>
1	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>

No. of Groups = 3 ( $\text{II}$  only)

$$y = ① + ② + ③$$

$$y = A\bar{B} + \bar{A}C + \bar{A}B$$

$$= \bar{A}B + \bar{A}(B+C)$$

③

④  $y = \sum (0, 1, 2, 4, 7)$ :

	00	01	11	10
0	1 <sub>0</sub>	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>
1	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>

No. of Groups = 4 ( $\text{II}$  and  $\text{I}$ )

$$y = ① + ② + ③ + ④$$

$$y = \bar{A}\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B} + ABC$$

④

⑤  $y = \sum (0, 1, 2, 3, 5)$ :

	00	01	11	10
0	1 <sub>0</sub>	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>
1	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>

No. of Groups = 2 ( $\text{II}$  and  $\text{I}$ )

$$y = ① + ②$$

$$y = \bar{A} + \bar{B}C$$

K-Map :- [ 4 variables ]

①  $Z = \sum (0, 2, 3, 7, 11, 13, 14, 15)$

		CD				
		00	01	11	10	①
AB	00	1	0	1	1	1
	01	4	5	1	7	6
AB	11	12	13	1	15	14
	10	8	9	1	11	10
		CD				②
		00	01	11	10	③
		00	1	1	1	1
		01	1	1	1	1
		11	12	13	15	14
		10	18	9	11	15, 10
		CD				④
		00	01	11	10	⑤

No. of groups = 4 ( ④ and ② )

$$Z = CD + \bar{A}\bar{B}\bar{D} + ABD + ABC$$

②  $Z = \sum (1, 3, 4, 5, 6, 7, 8, 10)$

		CD				
		00	01	11	10	①
AB	00	0	1	1	2	-
	01	1	1	1	1	1
AB	11	12	13	15	14	-
	10	18	9	11	15, 10	②
		CD				③
		00	01	11	10	④
		00	1	1	1	1
		01	1	1	1	1
		11	12	13	15	14
		10	18	9	11	15, 10
		CD				⑤
		00	01	11	10	⑥

No. of groups = 3 ( ② and ③ )

$$Z = ① + ② + ③$$

$$Z = \bar{A}D + \bar{A}B\bar{D} + A\bar{B}\bar{D}$$

③  $Z = \sum (0, 2, 5, 7, 9, 11, 13, 14)$

		CD				
		00	01	11	10	①
AB	00	1	0	②	1	1
	01	4	15	1	6	-
AB	11	12	14	15	1	14
	10	8	19	11	③	10
		CD				④
		00	01	11	10	⑤
		00	1	0	②	1
		01	4	15	1	6
		11	12	14	15	1
		10	8	19	11	③
		CD				⑥
		00	01	11	10	⑦

No. of groups = 4 (II only)

$$Z = \textcircled{1} + \textcircled{11} + \textcircled{12} + \textcircled{13}$$

$$Z = \bar{A}\bar{B}\bar{D} + \bar{A}BD + A\bar{B}\bar{D} + A\bar{B}D$$

④  $Z = \sum (0, 1, 2, 3, 5, 7, 8, 10, 13, 15)$

AB		CD	Z	
00	01	00	01	10
00	01	10	11	11
1 <sub>0</sub>	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>	1 <sub>11</sub>
1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>	
1 <sub>12</sub>	1 <sub>13</sub>	1 <sub>15</sub>	1 <sub>14</sub>	
1 <sub>8</sub>	1 <sub>9</sub>	1 <sub>11</sub>	1 <sub>10</sub>	

No. of Groups = 3 (II only)

$$Z = \textcircled{1} + \textcircled{11} + \textcircled{13}$$

$$Z = \bar{A}D + BD + \bar{B}\bar{D}$$

⑤  $Z = \sum (0, 1, 2, 5, 6, 8, 9, 10, 12, 13)$

AB		CD	Z	
00	01	00	01	10
00	01	10	11	11
1 <sub>0</sub>	1 <sub>1</sub>	1 <sub>3</sub>	1 <sub>2</sub>	1 <sub>11</sub>
1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>	1 <sub>13</sub>
1 <sub>12</sub>	1 <sub>13</sub>	1 <sub>15</sub>	1 <sub>14</sub>	
1 <sub>8</sub>	1 <sub>9</sub>	1 <sub>11</sub>	1 <sub>10</sub>	

No. of Groups = 4 (II and IV)

$$Z = \textcircled{1} + \textcircled{11} + \textcircled{13} + \textcircled{15}$$

$$Z = \bar{B}\bar{D} + A\bar{C} + \bar{C}D + \bar{A}C\bar{D}$$

## Arithmetic Circuits :-

- ① Adders — Half Adder and Full adder
- ② Subtractors — Half subtracter and full subtracter
- ③ Multipliers —  $(2 \times 3)$ ,  $(2 \times 4)$ ,  $(3 \times 2)$ ,  $(3 \times 3)$ ;  $(4 \times 2)$ ,  $(4 \times 4)$ ,  $(3 \times 4)$ .

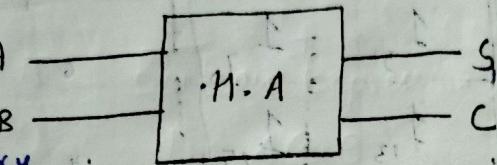
### Half-Adder Circuit :-

2 inputs  $\rightarrow$  2 outputs

Inputs : A and B

Outputs : S and C

S = Sum ; C = Carry



### Truth Table :-

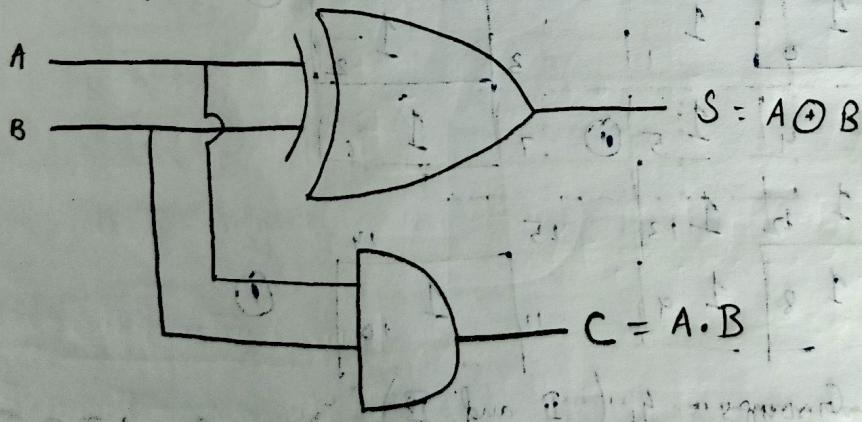
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean Expression :-

$$S = A \oplus B = A'B + B'A$$

$$C = A \cdot B$$

### Boolean Logic Diagram :-



### Full-Adder Circuit :-

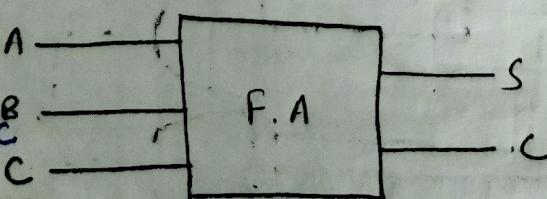
3 inputs  $\rightarrow$  2 outputs

Inputs : A, B; A and C

Outputs : S and C

S = Sum

C = Carry



Truth Table :-

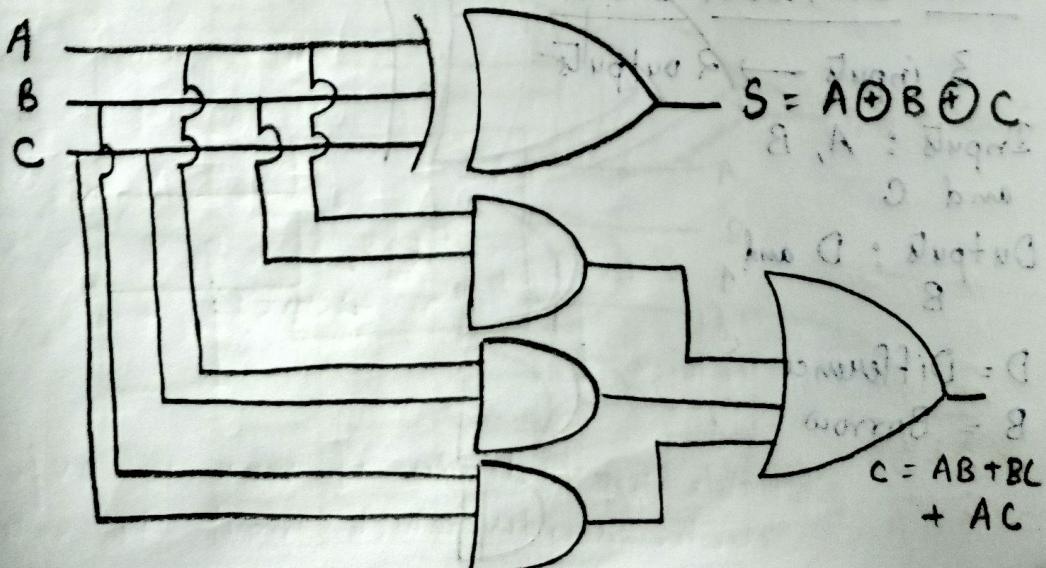
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression :-

$$S = \begin{array}{|c|c|c|c|} \hline & A'BC & AB'C & ABC' \\ \hline 0 & 00 & 01 & 10 \\ \hline 1 & 1 & 1 & 1 \\ \hline \end{array} = A'B'C + A'BC' + ABC' + ABC = A \oplus B \oplus C$$

$$C = \begin{array}{|c|c|c|c|} \hline & A'BC & AB'C & ABC' \\ \hline 0 & 00 & 01 & 11 \\ \hline 1 & 1 & 1 & 1 \\ \hline \end{array} = AC + AB + BC$$

Boolean Logic Diagram :-



## Half-Subtractor Circuit :-

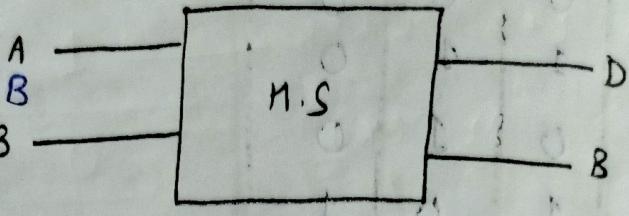
2 inputs  $\rightarrow$  2 outputs

Inputs : A and B

Outputs : D and B

D = Difference

B = Borrow



Truth Table :-

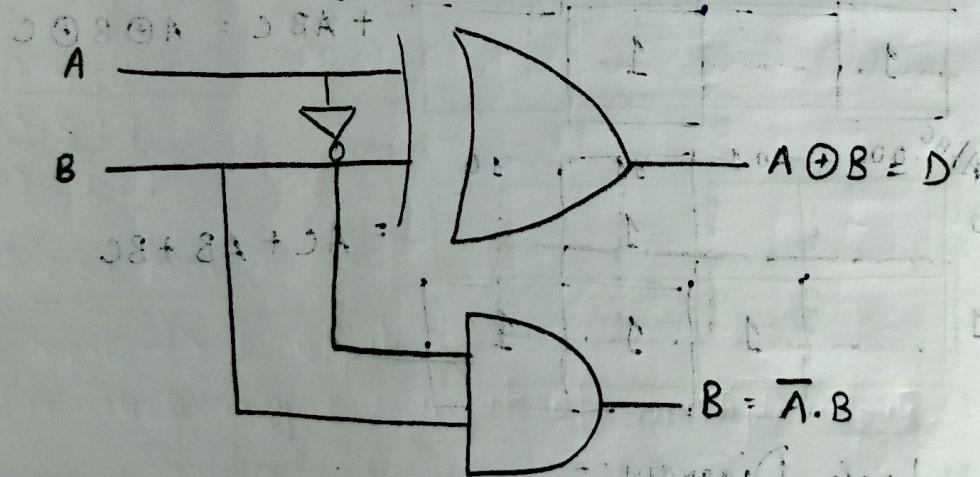
A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Boolean Expression :-

$$D = A \oplus B$$

$$B = \bar{A} \cdot B$$

Boolean Logic Diagram :-



## Full-Subtractor Circuit :-

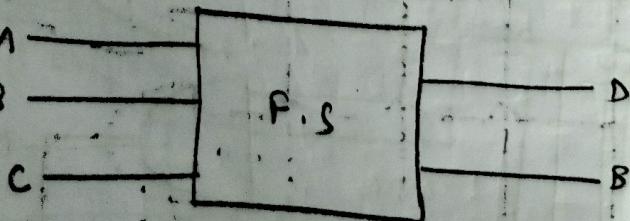
3 inputs  $\rightarrow$  2 outputs

Inputs : A, B  
and C

Outputs : D and B

D = Difference

B = Borrow



Truth Table :-

A	B	C	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Boolean Expression :-

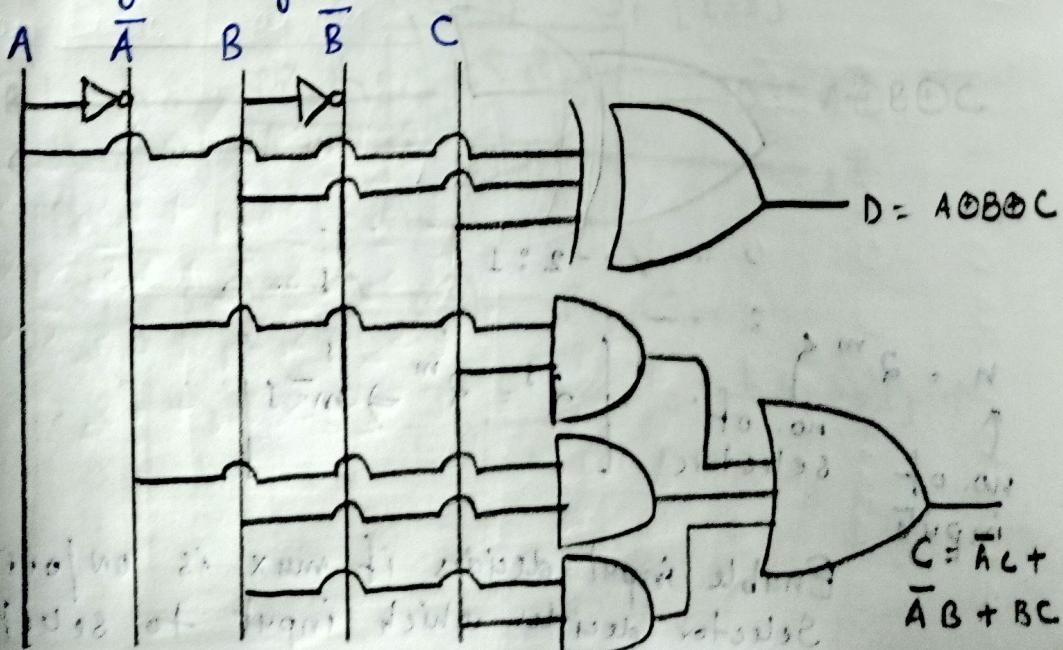
		00	01	11	10
		0	1	1	1
B =					
1				1	

$$= \overline{AC} + \overline{AB} + BC$$

		00	01	11	10
		0	1	1	1
D =					
1		1	1	1	

$$= AB'C' + A'B'C + ABC + A'BC' = A \oplus B \oplus C$$

Boolean Logic Diagram :-



## Multiplexers :-

$$\begin{array}{r} 1 \ 1 \ 0 \\ 1 \ 1 \\ \hline \end{array} \quad 2^2 + 2^3 = 4 + 2^3 = 6$$

$$\begin{array}{r} 1 \ 1 \\ 1 \ 1 \\ \hline \end{array} \quad 2^3 + 2^0 = 2 + 1 = 3$$

$$\begin{array}{r} 0 \ 1 \ 1 \ 0 \\ 0 \ 1 \ 1 \ 0 \\ \hline \end{array} \quad 6 \times 3 = 18$$

$$\begin{array}{r} 0 \ 1 \ 1 \ 0 \\ 0 \ 1 \ 1 \ 0 \\ \hline \end{array}$$

$$\begin{array}{r} 1 \ 0 \ 0 \ 1 \ 0 \\ 1 \ 0 \ 0 \ 1 \ 0 \\ \hline \end{array} \quad 2^4 + 2^3 = 16 + 2 = 18$$

## Combination Circuits :-

The present output is depending upon the present input, then its called combination circuits.

### ① Multiplexers (Mux) :-

Types of muxes :-

(i) 2 : 1

(ii) 4 : 1

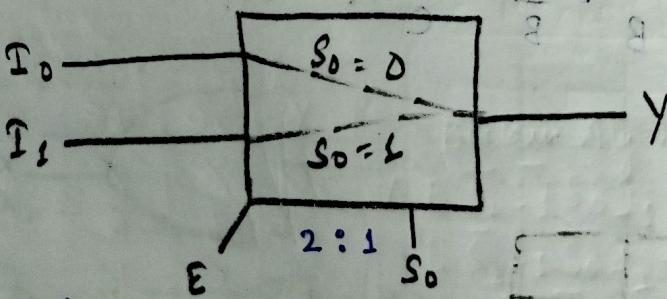
(iii) 8 : 1

(iv) 16 : 1

(v) 2 : 1 Mux

2 input  $\rightarrow$  1 output

Mux selects only one input of multiple inputs.



$n = 2^m$   
 $\uparrow$   
 no. of inputs      no. of selectors

$$2^s = 2^m \Rightarrow m = s$$

Enable input decides if mux is ON/OFF.  
 Selector decides which input to select.

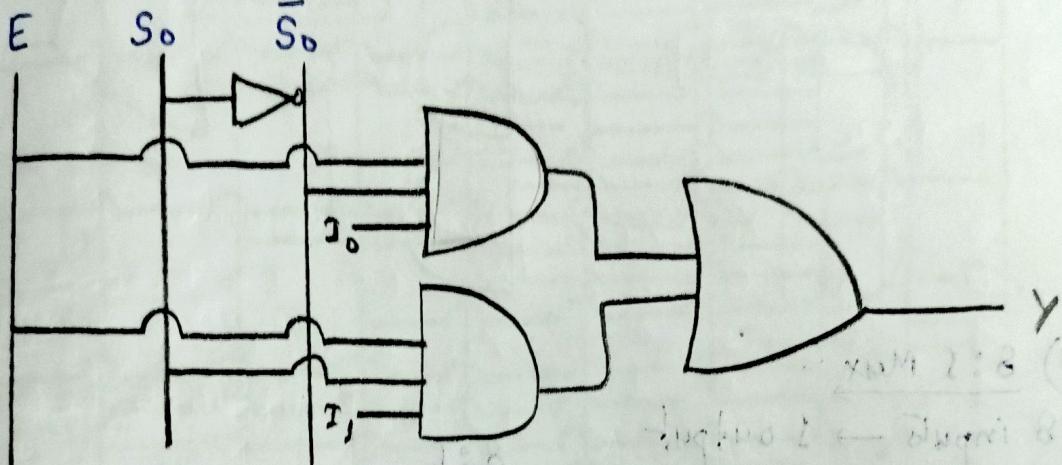
Truth Table :-

E	S <sub>0</sub>	Y
0	X	0
1	0	I <sub>0</sub>
1	1	I <sub>1</sub>

Boolean Expression :-

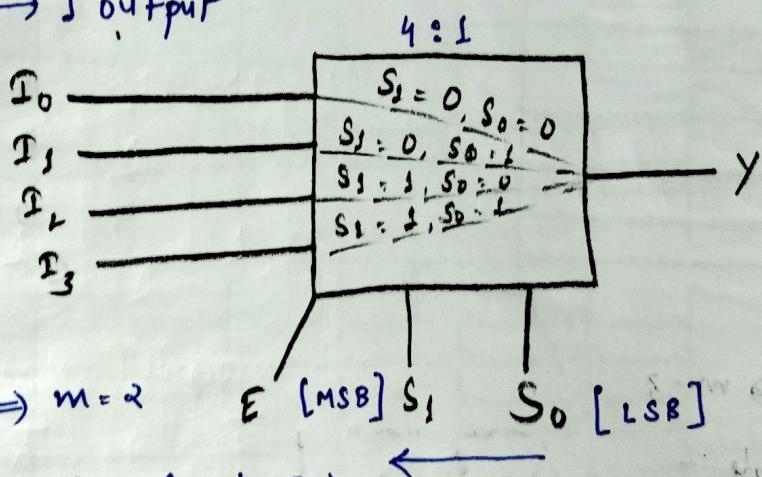
$$Y = E \cdot \bar{S}_0 \cdot I_0 + E \cdot S_0 \cdot I_1$$

Boolean Logic Diagram :-



(II) 4:1 Mux :-

4 inputs  $\rightarrow$  1 output



LSB : Least Significant Bit

MSB : Most Significant Bit

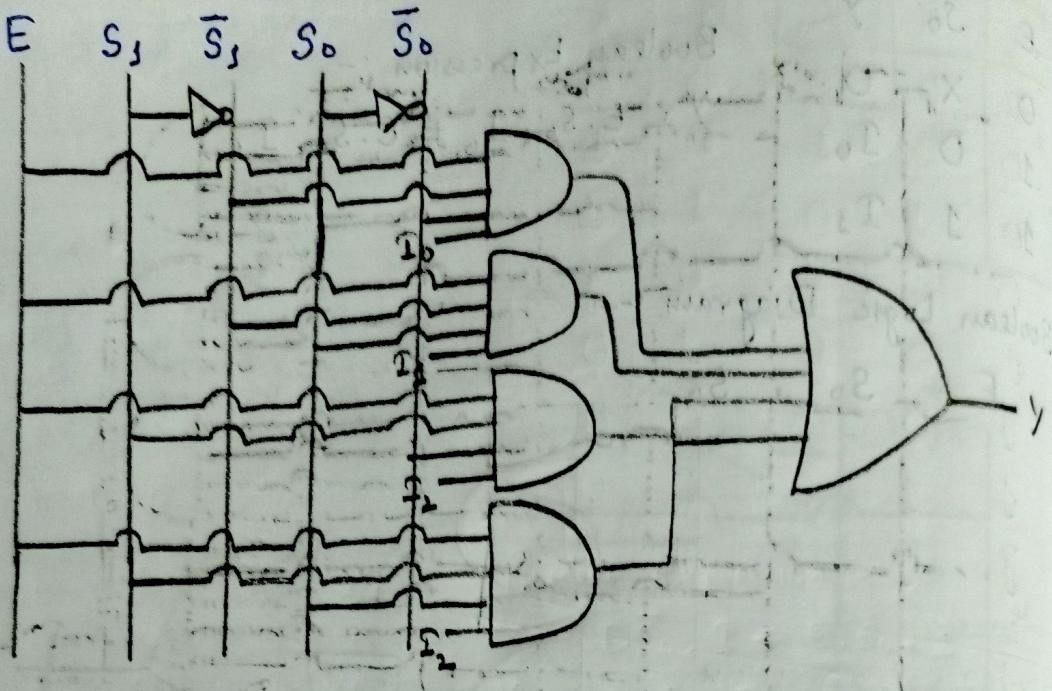
Truth Table :-

E	S <sub>1</sub>	S <sub>0</sub>	Y
0	X	X	0
1	0	0	I <sub>0</sub>
1	0	1	I <sub>1</sub>
1	1	0	I <sub>2</sub>
1	1	1	I <sub>3</sub>

Boolean Expression :-

$$Y = E \bar{S}_1 \bar{S}_0 I_0 + E \bar{S}_1 S_0 I_1 + E S_1 \bar{S}_0 I_2 + E S_1 S_0 I_3$$

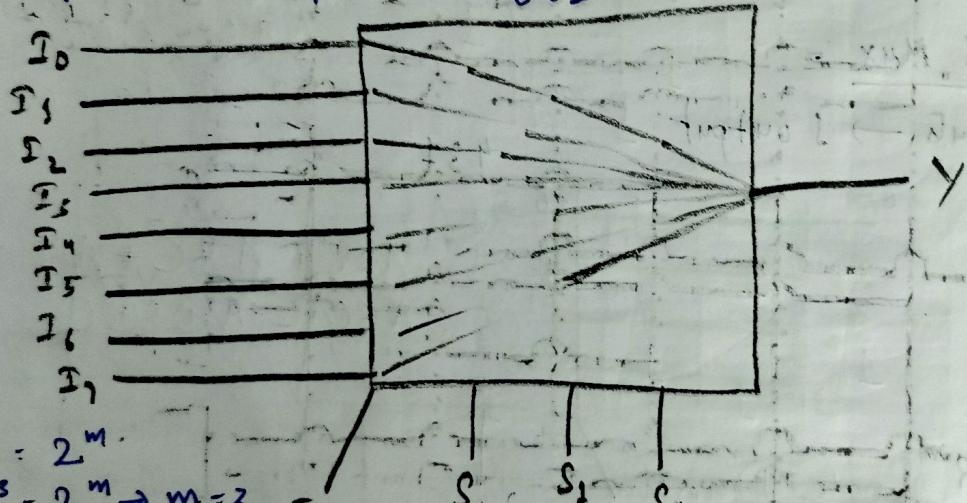
# Boolean Logic Diagram :-



(III) 8:1 Mux

8 inputs  $\rightarrow$  1 output

8:1



$$8 = 2^m$$

$$2^3 = 2^m \Rightarrow m = 3$$

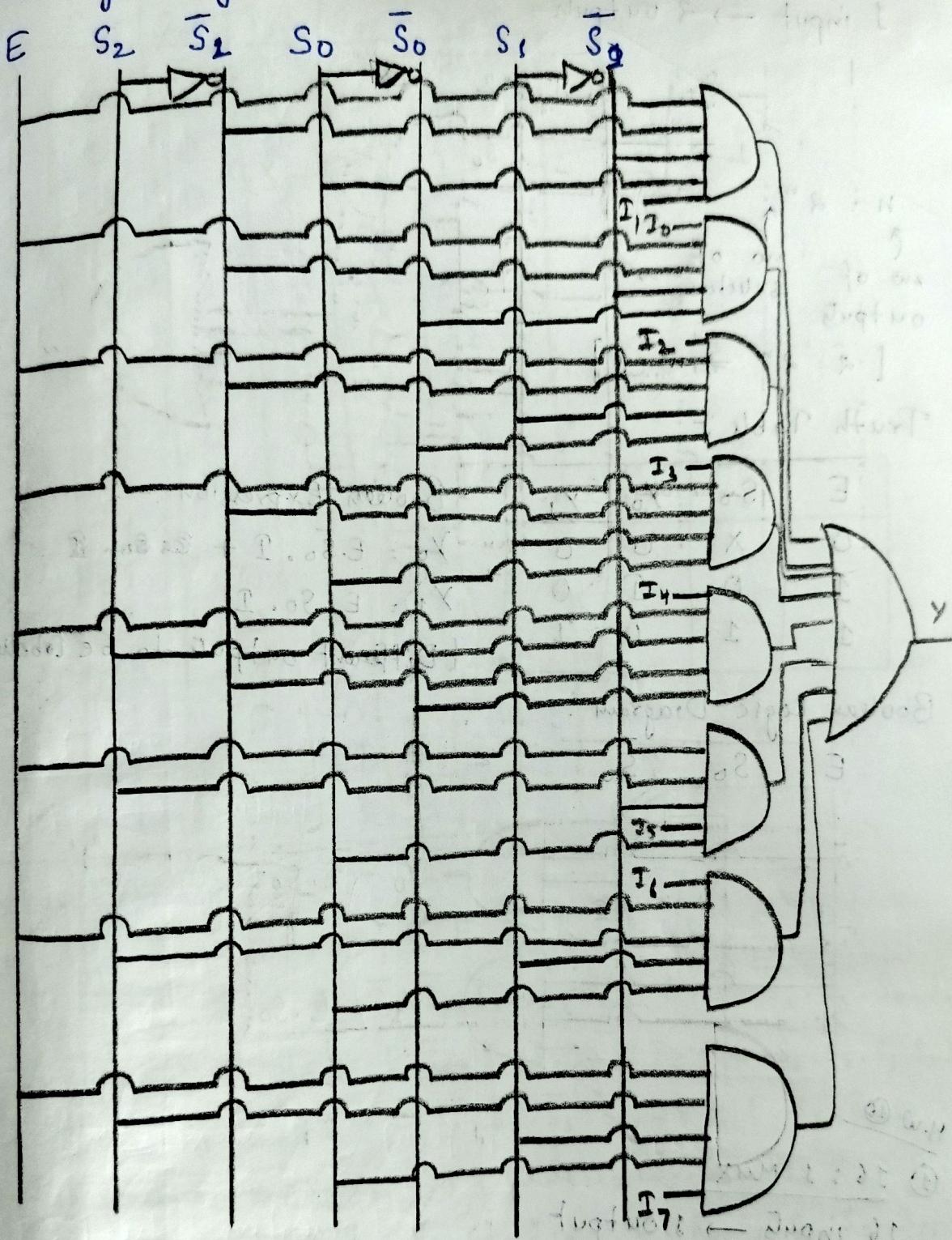
Truth Table :-

E	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Y
0	X	X	X	0
1	0	0	1	I <sub>1</sub>
1	0	1	0	I <sub>2</sub>
1	0	1	1	I <sub>3</sub>
1	1	0	0	I <sub>4</sub>
1	1	0	1	I <sub>5</sub>
1	1	1	0	I <sub>6</sub>
1	1	1	1	I <sub>7</sub>

Boolean Algebra :-

$$Y = E \bar{S}_2 \bar{S}_1 \bar{S}_0 I_3 + E \bar{S}_2 \bar{S}_1 S_0 I_0 + E \bar{S}_2 S_1 \bar{S}_0 I_2 + E \bar{S}_2 S_1 S_0 I_3 + E S_2 \bar{S}_1 \bar{S}_0 I_4 + E S_2 \bar{S}_1 S_0 I_5 + E S_2 S_1 \bar{S}_0 I_6 + E S_2 S_1 S_0 I_7$$

Boolean Logic Diagram :-



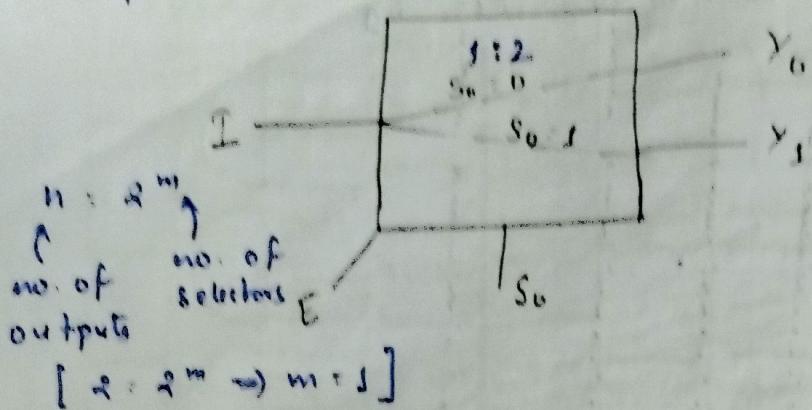
## ② Demultiplexer (Demux) :-

Types of demuxes :-

- (i) 1 : 2
- (ii) 1 : 4
- (iii) 1 : 8
- (iv) 1 : 16

# 1) 3:2 Demux :-

1 input → 2 outputs



Truth Table :-

E	S <sub>0</sub>	Y <sub>0</sub>	Y <sub>1</sub>
0	X	0	0
1	0	1	0
1	1	0	1

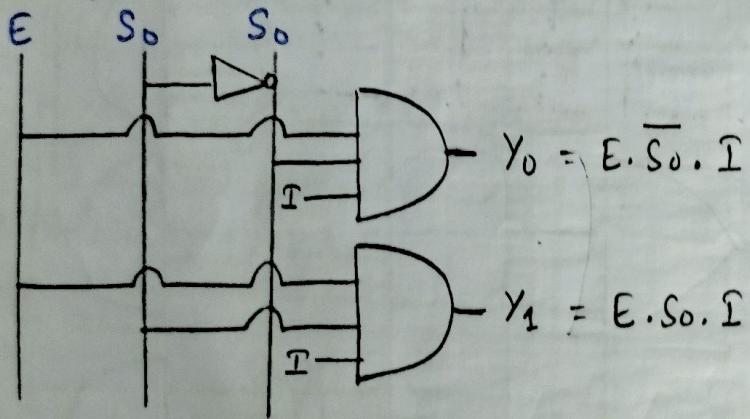
Boolean Expression :-

$$Y_0 = E \cdot \bar{S}_0 \cdot I \leftarrow 0000 \cdot 0$$

$$Y_1 = E \cdot S_0 \cdot I$$

| Different outputs to be labelled

Boolean Logic Diagram :-



H.W ①

## ① 16:4 MUX

16 inputs → 4 output

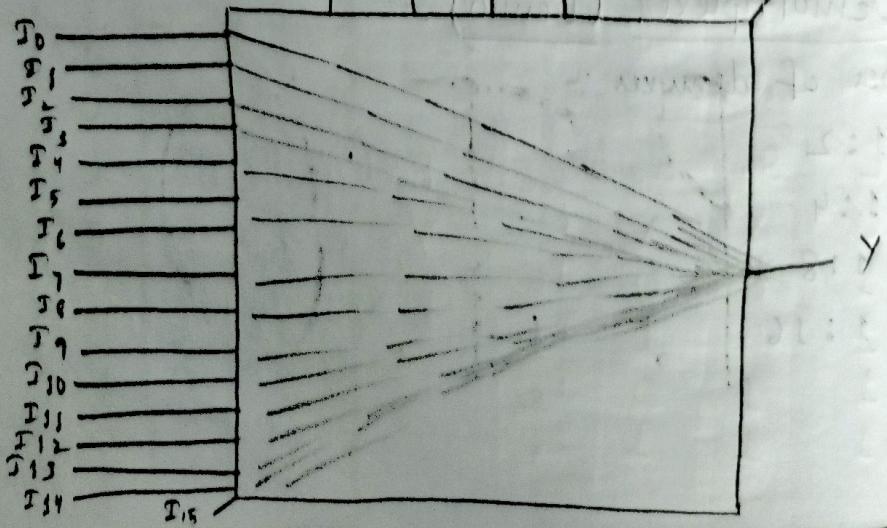
S<sub>3</sub> S<sub>2</sub> S<sub>1</sub> S<sub>0</sub>

$$16 = 2^m$$

$$2^4 = 2^m$$

$$m = 4$$

(selectors)



Truth Table :-

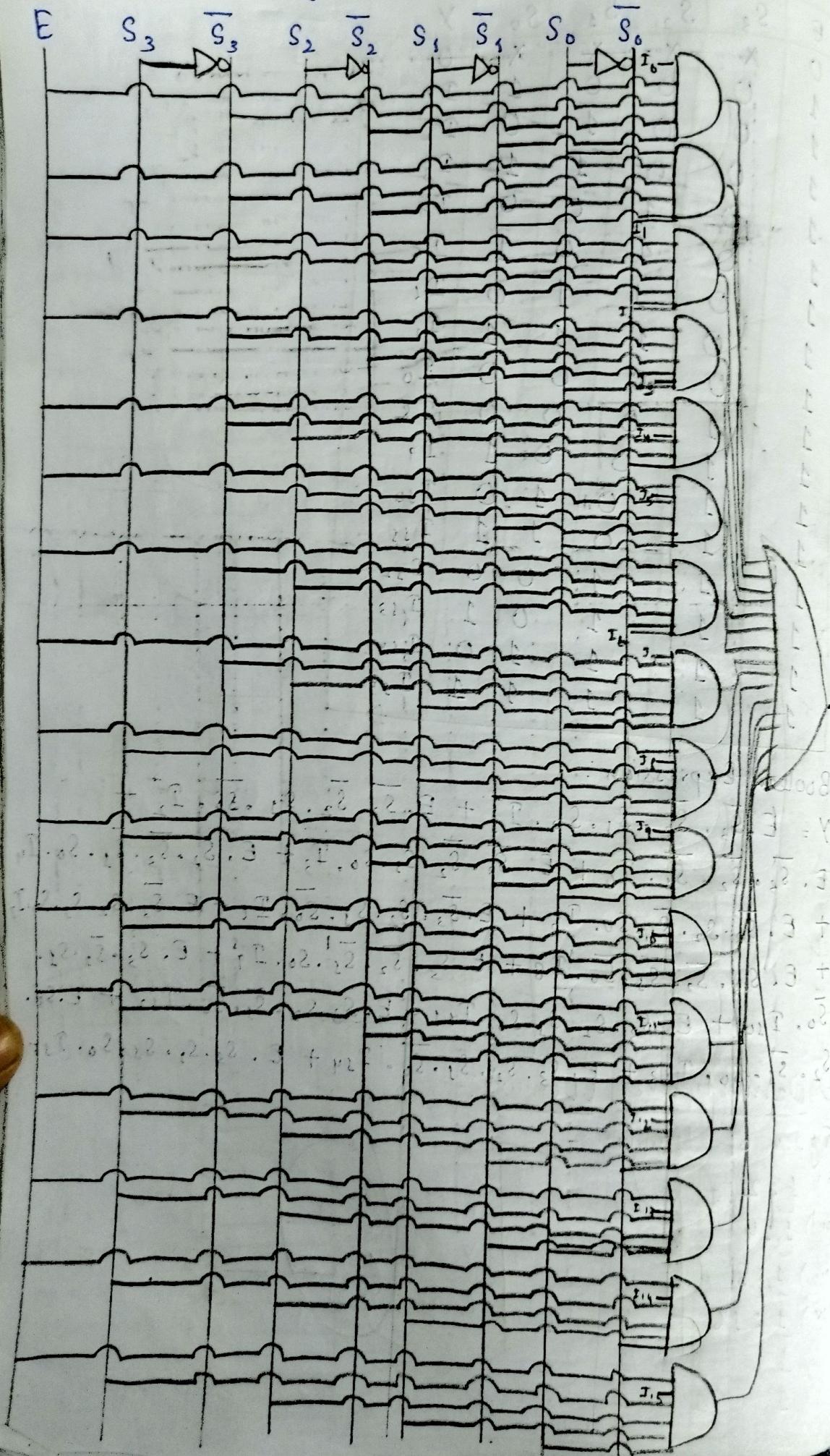
E	$S_3$	$S_2$	$S_1$	$S_0$	Y
0	X	X	X	X	0
1	0	0	0	1	$I_1$
1	0	0	1	0	$I_2$
1	0	0	1	1	$I_3$
1	0	1	0	0	$I_4$
1	0	1	0	1	$I_5$
1	0	1	1	0	$I_6$
1	0	1	1	1	$I_7$
1	0	0	0	0	$I_8$
1	1	0	0	0	$I_9$
1	1	0	1	0	$I_{10}$
1	1	0	1	1	$I_{11}$
1	1	1	0	0	$I_{12}$
1	1	1	0	1	$I_{13}$
1	1	1	1	0	$I_{14}$
1	1	1	1	1	$I_{15}$

Boolean Expression :-

$$\begin{aligned}
 Y = & E \cdot \bar{S}_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot S_0 \cdot I_1 + E \cdot \bar{S}_3 \cdot \bar{S}_2 \cdot S_1 \cdot \bar{S}_0 \cdot I_2 + \\
 & E \cdot \bar{S}_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot I_0 + E \cdot \bar{S}_3 \cdot \bar{S}_2 \cdot S_1 \cdot S_0 \cdot I_3 + E \cdot S_2 \cdot \bar{S}_3 \cdot \bar{S}_1 \cdot \bar{S}_0 \cdot I_4 + \\
 & E \cdot \bar{S}_3 \cdot S_2 \cdot \bar{S}_1 \cdot S_0 \cdot I_5 + E \cdot \bar{S}_3 \cdot S_2 \cdot S_1 \cdot \bar{S}_0 \cdot I_6 + E \cdot \bar{S}_3 \cdot S_2 \cdot S_1 \cdot S_0 \cdot I_7 + \\
 & E \cdot S_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot \bar{S}_0 \cdot I_8 + E \cdot S_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot S_0 \cdot I_9 + E \cdot S_3 \cdot \bar{S}_2 \cdot S_1 \cdot \bar{S}_0 \cdot I_{10} + \\
 & E \cdot S_3 \cdot \bar{S}_2 \cdot S_1 \cdot S_0 \cdot I_{11} + E \cdot S_3 \cdot S_2 \cdot \bar{S}_1 \cdot \bar{S}_0 \cdot I_{12} + E \cdot S_3 \cdot S_2 \cdot \bar{S}_1 \cdot S_0 \cdot I_{13} + \\
 & E \cdot S_3 \cdot S_2 \cdot S_1 \cdot \bar{S}_0 \cdot I_{14} + E \cdot S_3 \cdot S_2 \cdot S_1 \cdot S_0 \cdot I_{15}
 \end{aligned}$$

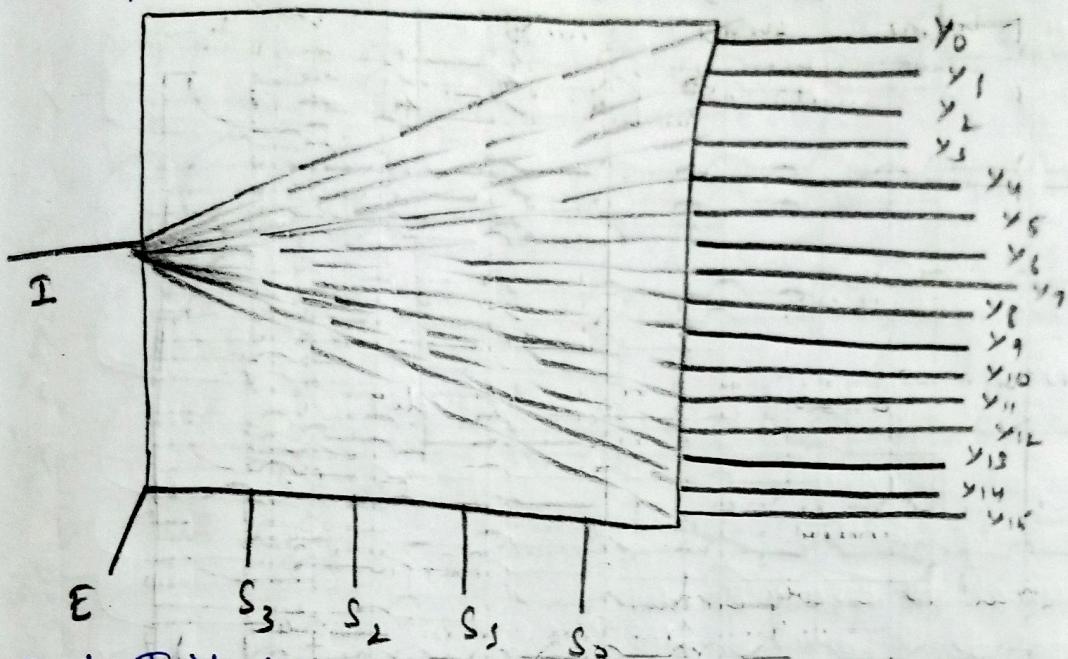
P.T.O

# Boolean Logic Diagram :-



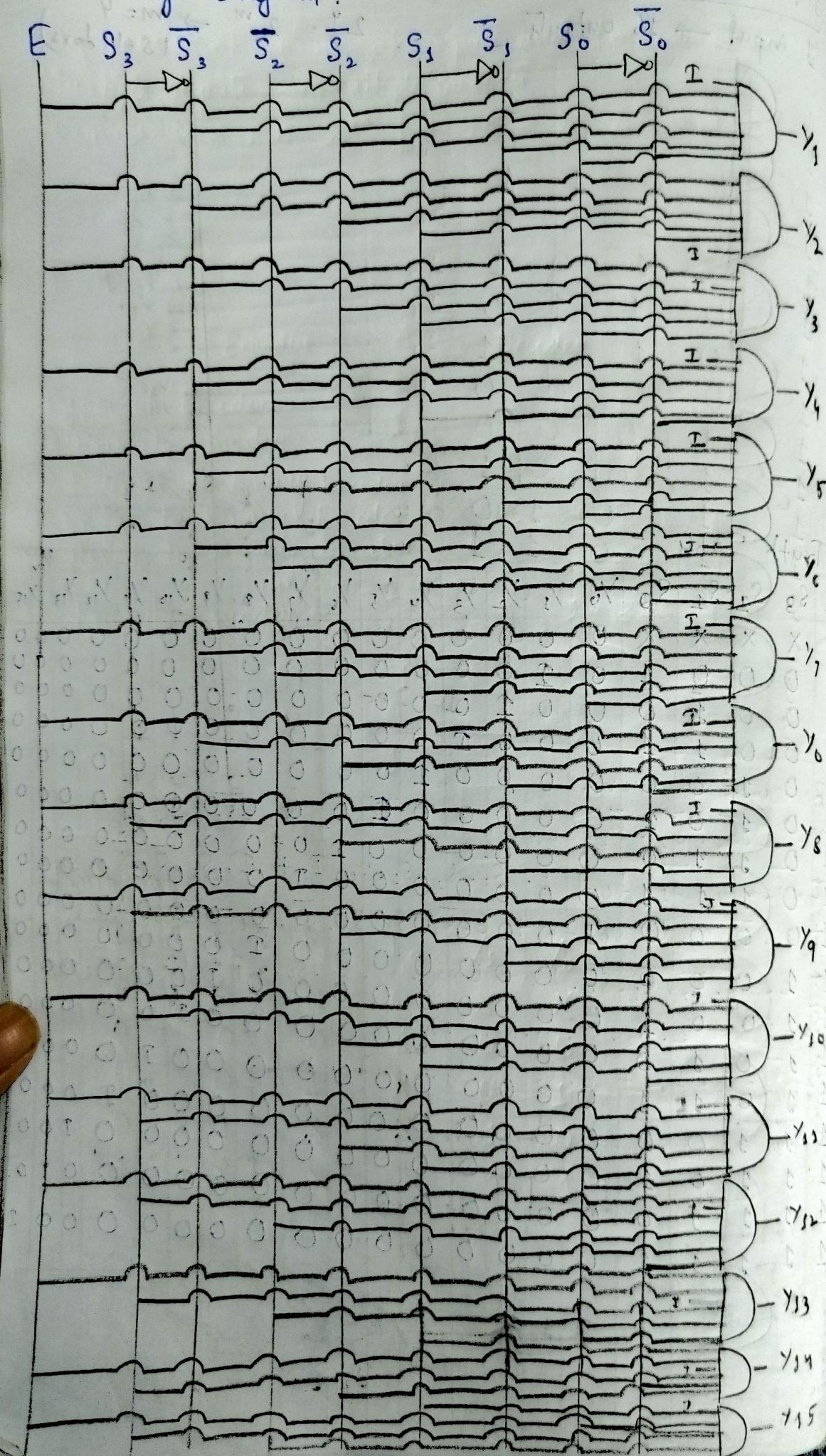
② 1 : 36 Demux :-  
1 input → 36 outputs

$$2^4 = 2^m \Rightarrow m = 4 \\ (\text{se 4 fatores})$$



## Truth Table :-

## Boolean Logic Diagram :-



### Boolean Expressions :-

$$y_0 = E \cdot \bar{S}_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot \bar{S}_0 \cdot I$$

$$y_1 = E \cdot \bar{S}_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot S_0 \cdot I$$

$$y_2 = E \cdot \bar{S}_3 \cdot \bar{S}_2 \cdot S_1 \cdot \bar{S}_0 \cdot I$$

$$y_3 = E \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot S_1 \cdot S_0 \cdot I$$

$$y_4 = E \cdot \bar{S}_3 \cdot S_2 \cdot \bar{S}_1 \cdot \bar{S}_0 \cdot I$$

$$y_5 = E \cdot \bar{S}_3 \cdot S_2 \cdot \bar{S}_1 \cdot S_0 \cdot I$$

$$y_6 = E \cdot \bar{S}_3 \cdot S_2 \cdot S_1 \cdot \bar{S}_0 \cdot I$$

$$y_7 = E \cdot \bar{S}_3 \cdot S_2 \cdot S_1 \cdot S_0 \cdot I$$

$$y_8 = E \cdot S_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot \bar{S}_0 \cdot I$$

$$y_9 = E \cdot S_3 \cdot \bar{S}_2 \cdot \bar{S}_1 \cdot S_0 \cdot I$$

$$y_{10} = E \cdot S_3 \cdot \bar{S}_2 \cdot S_1 \cdot \bar{S}_0 \cdot I$$

$$y_{11} = E \cdot S_3 \cdot \bar{S}_2 \cdot S_1 \cdot S_0 \cdot I$$

$$y_{12} = E \cdot S_3 \cdot S_2 \cdot \bar{S}_1 \cdot \bar{S}_0 \cdot I$$

$$y_{13} = E \cdot S_3 \cdot S_2 \cdot \bar{S}_1 \cdot S_0 \cdot I$$

$$y_{14} = E \cdot S_3 \cdot S_2 \cdot S_1 \cdot \bar{S}_0 \cdot I$$

$$y_{15} = E \cdot S_3 \cdot S_2 \cdot S_1 \cdot S_0 \cdot I$$

③ Design a 16:1 mux circuit using two 8:1 muxes and one 2:1 mux.

Sol:- To design mux = 16:1  
 $n_3 = 16$

To use first mux = 8:1

$$n_2 = 8$$

To use second mux = 2:1

$$n_3 = 2$$

$$\therefore \frac{n_3}{n_2} = \frac{16}{8} = 2 \Rightarrow \frac{2}{n_3} = \frac{1}{2} = \begin{matrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 1 & 0 \end{matrix}$$

Required : 2 (8:1) and 1 (2:1) muxes.

LEVEL-1

[Level-1]

[Level-2]

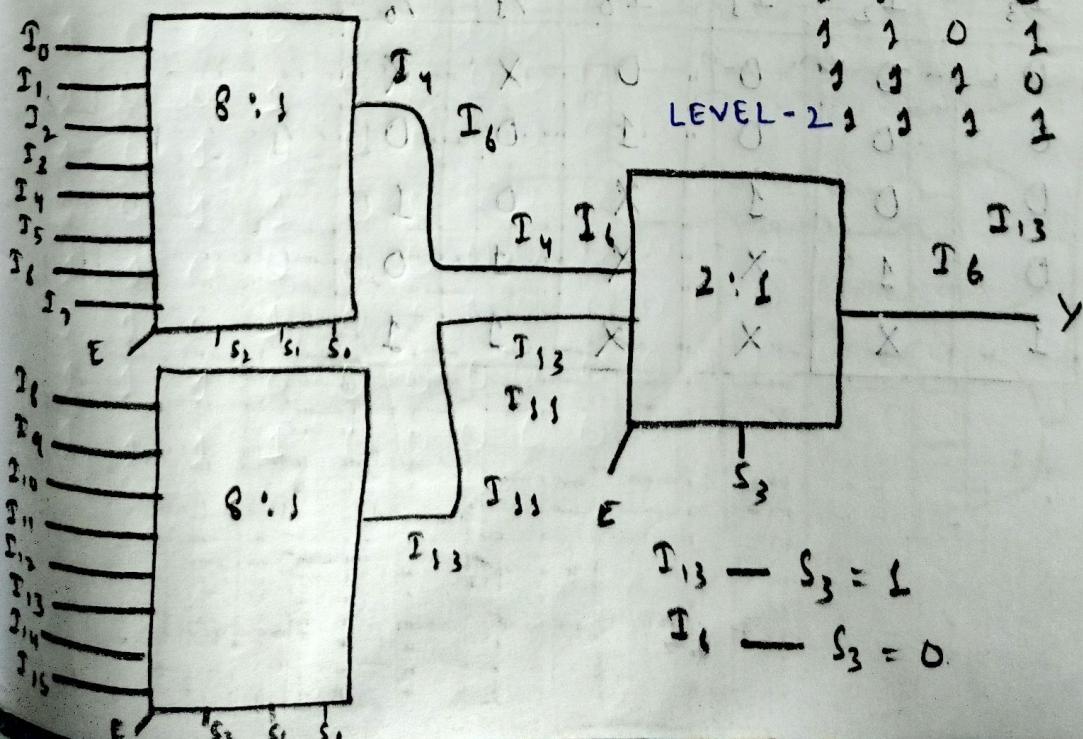
1 0 1 1

1 1 0 0

1 1 0 1

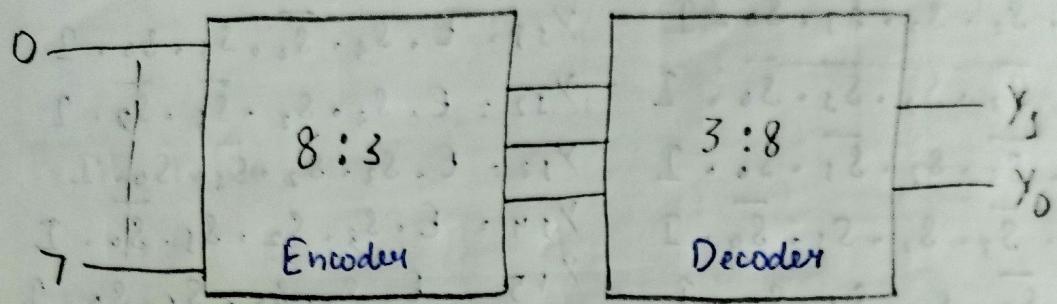
1 1 1 0

1 1 1 1



## Encoders :-

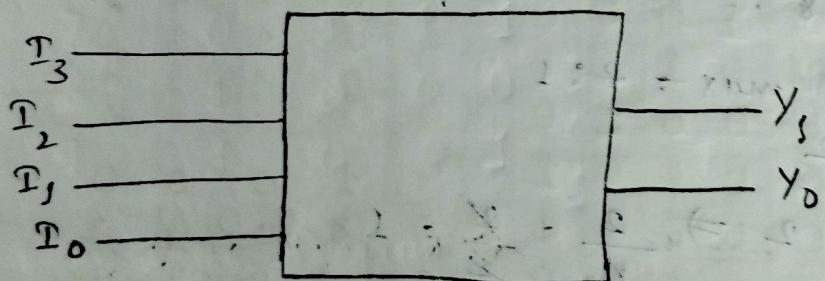
They consist of 'n' no. of inputs and 'm' no. of outputs.  
 Multiple inputs  $\rightarrow$  Multiple outputs.  
 formula used :  $n = 2^m$  [  $4 = 2^2 \Rightarrow 2^2 = 2^m \Rightarrow m = 2$  ]



Types of Encoders :-

- ① Priority Encoder
- ② Decimal to Binary Encoder
- ③ Octal to Binary Encoder
- ④ Hexal to Binary Encoder

(1) Priority Encoder :-



Truth Table :-

I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Y <sub>1</sub>	Y <sub>0</sub>
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

Boolean Expression :-

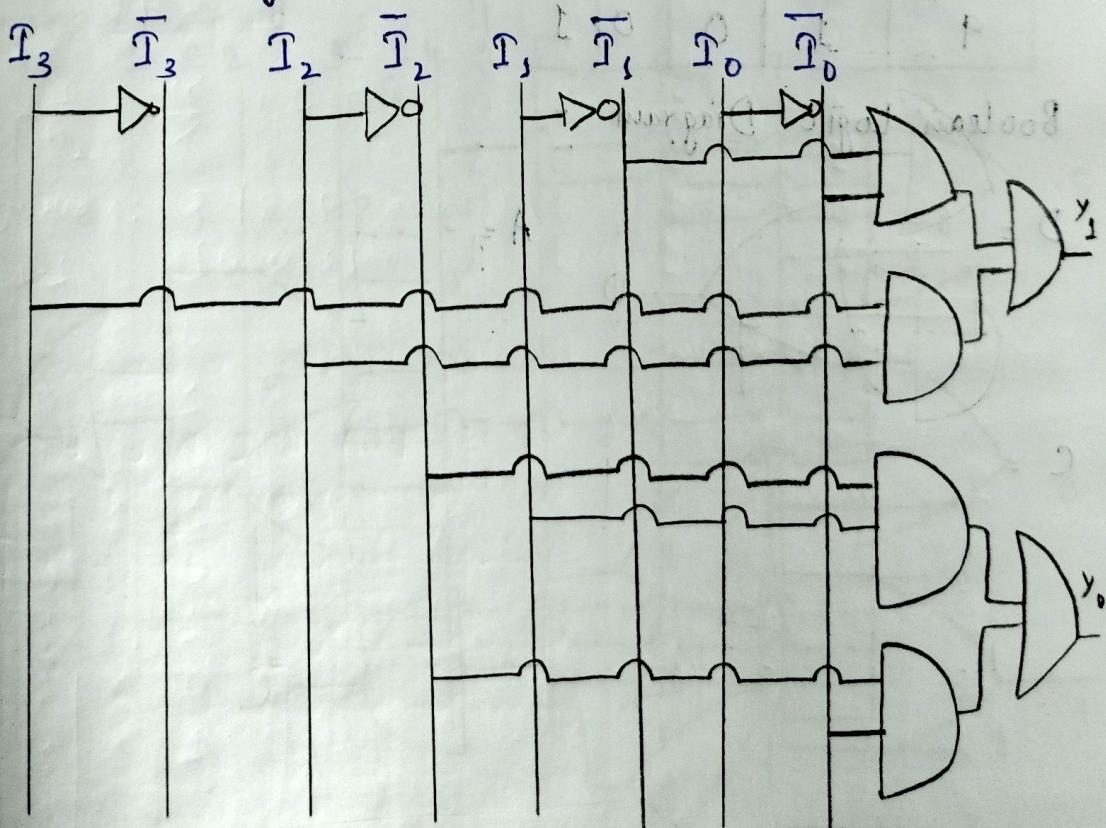
	$I_3, I_2$	$I_1$	$I_0$
$I_3, I_2$	00	01	10
00	X	0	0
01	1	1	1
11	1	1	1
10	1	1	1

$$y_3 = I_3 + I_2 + \bar{I}_1 \bar{I}_0$$

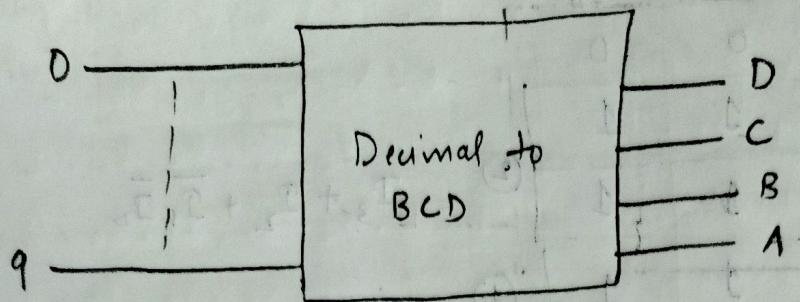
	$I_3, I_2$	$I_1$	$I_0$
$I_3, I_2$	00	01	11
00	X	0	1
01	0	0	0
11	1	1	1
10	1	1	1

$$y_0 = I_3 + \bar{I}_2 I_1 + \bar{I}_2 \bar{I}_0$$

Boolean Logic Diagram :-



# (11) Decimal to Binary-coded Decimal Encoder :-



Truth Table :-

Deci	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Boolean Expression :-

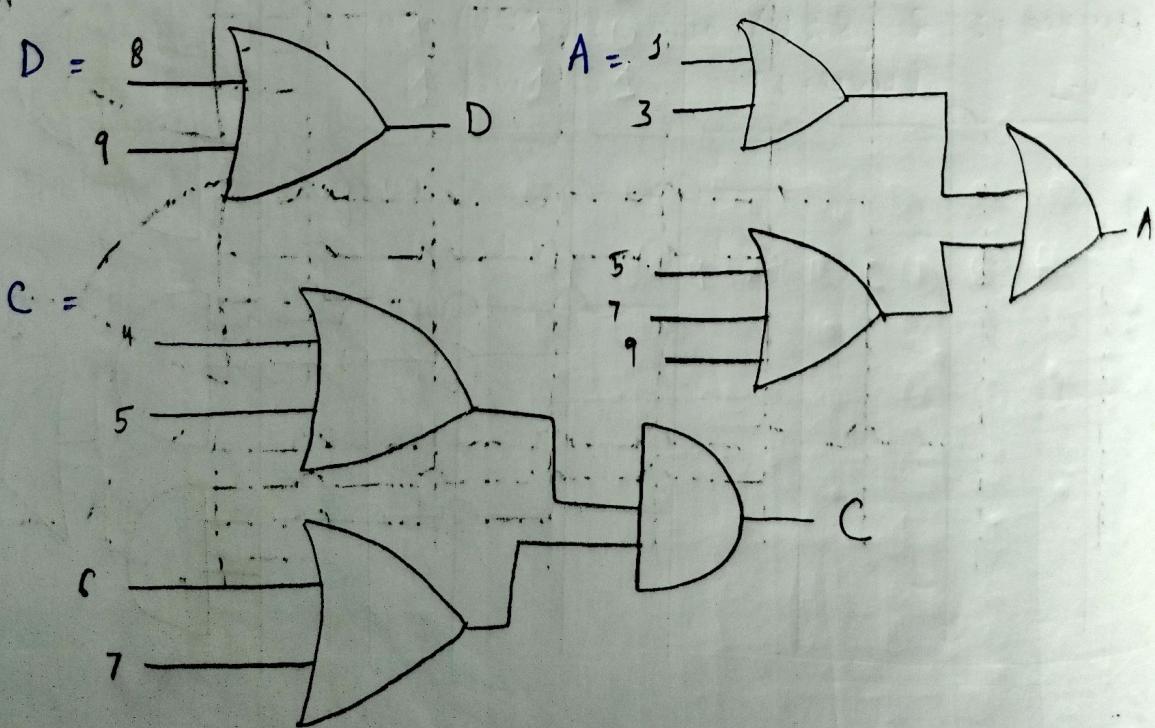
$$D = 8 + 9$$

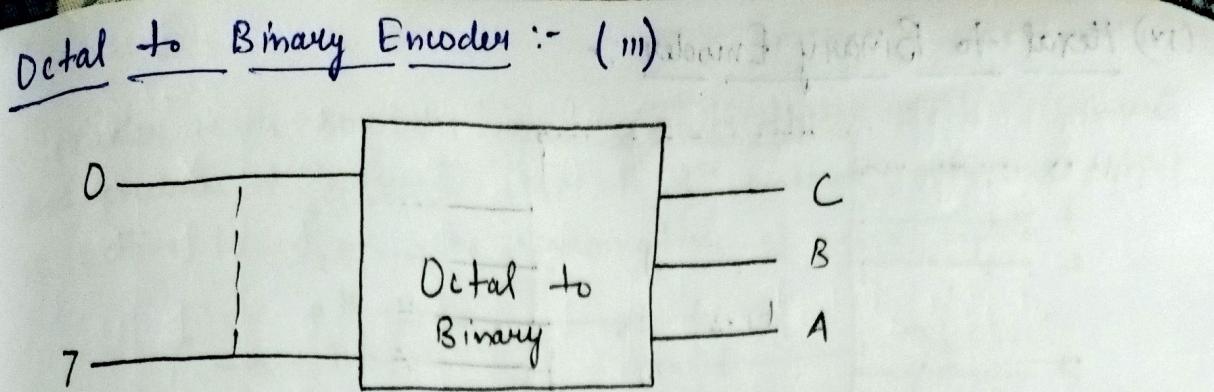
$$C = 4 + 5 + 6 + 7$$

$$B = 2 + 3 + 6 + 7$$

$$A = 1 + 3 + 5 + 7 + 9$$

Boolean Logic Diagram :-





Truth Table :-

Oct.	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

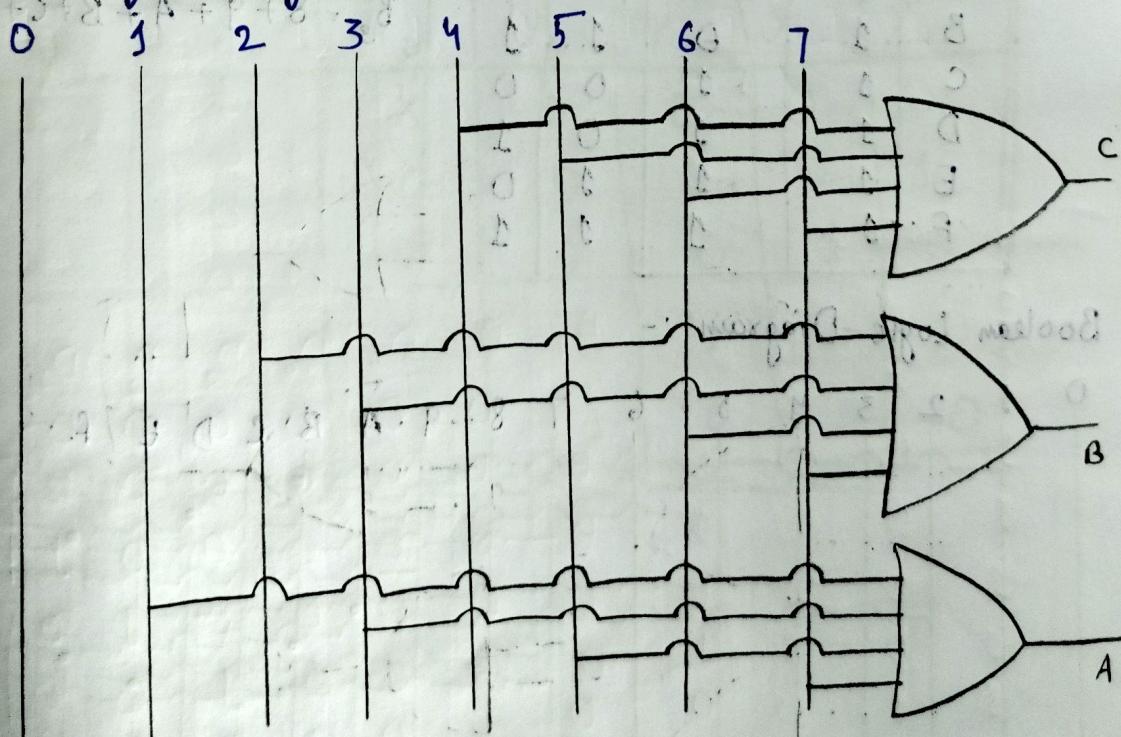
Boolean Expression :-

$$C = 4 + 5 + 6 + 7$$

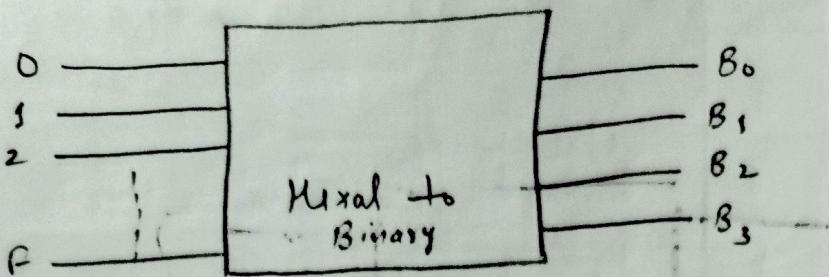
$$B = 2 + 3 + 6 + 7$$

$$A = 1 + 3 + 5 + 7$$

Boolean Logic Diagram :-



(iv) Hexal to Binary Encoder :-



Truth Table :-

Hex.	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	0	1	1	1

Boolean Expression :-

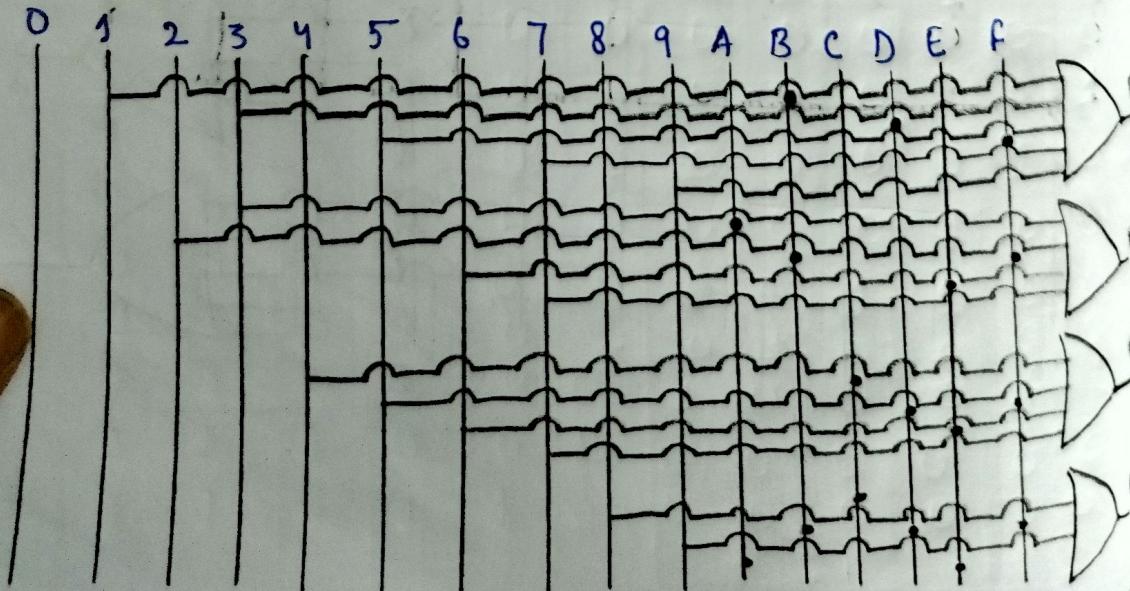
$$B_0 = 1 + 3 + 5 + 7 + 9 + 8 \\ D + F$$

$$B_1 = 2 + 3 + 6 + 7 + A + B + \\ E + F$$

$$B_2 = 4 + 5 + 6 + 7 + C + D +$$

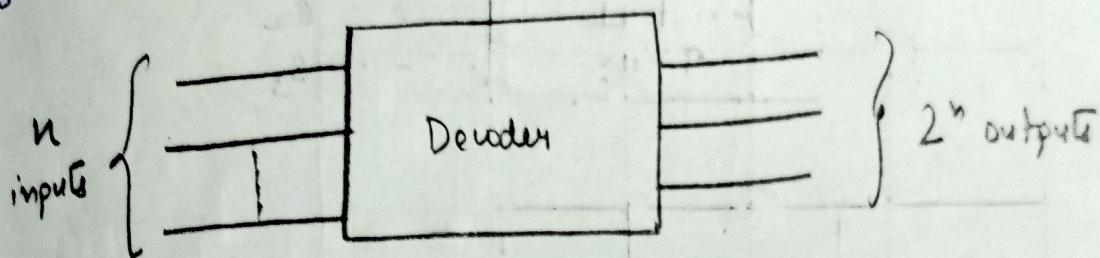
$$B_3 = 8 + 9 + A + B + C + D +$$

Boolean Logic Diagram :-

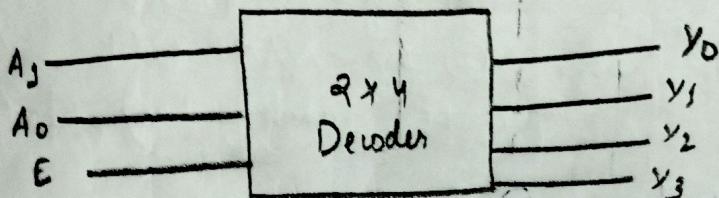


## Decoder :-

- Decoder is a combinational circuit that accepts 'n' inputs and produces  $2^n$  outputs. Out of  $2^n$  outputs, only one output is active based on the combination of each inputs.



## (1) $2$ to $4$ Decoder / $2 \times 4$ Decoder :-



- Out of these four outputs, only one output is high for each combination of inputs when enable input.

## Truth Table :-

E	A <sub>1</sub>	A <sub>0</sub>	y <sub>3</sub>	y <sub>2</sub>	y <sub>1</sub>	y <sub>0</sub>
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

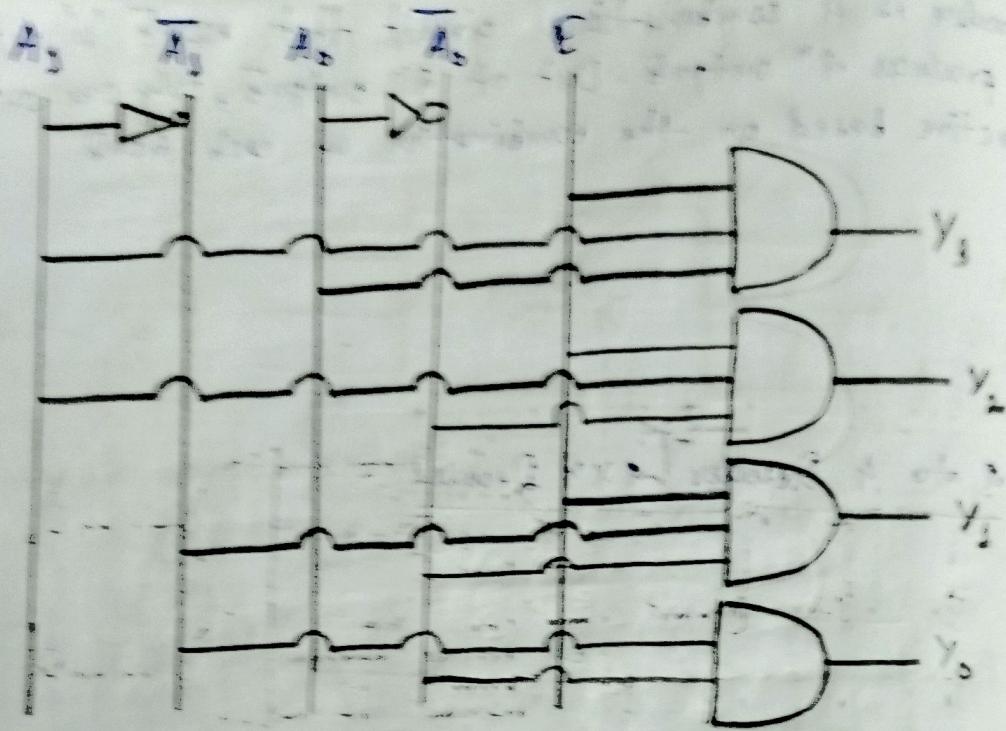
## Boolean Expression :-

$$y_3 = EA_1A_0$$

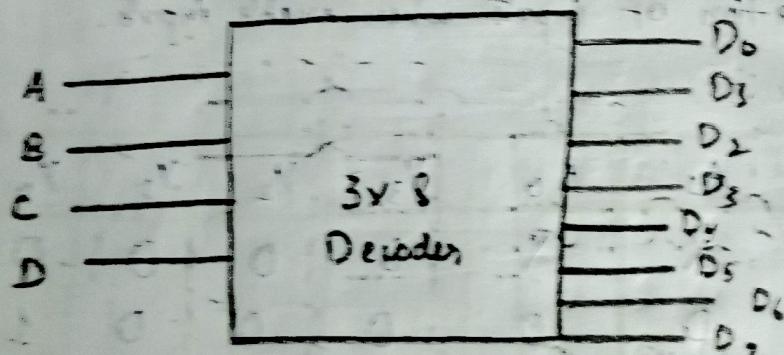
$$y_3 = EA_1\bar{A}_0$$

$$y_3 = E\bar{A}_1\bar{A}_0$$

# Boolean Logic Diagram :-



(ii)  $3 \rightarrow 8$  Decoder /  $3 \times 8$  Decoder :-



Truth Table :-

$E$	$A$	$B$	$C$	$D_7$	$D_6$	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Date \_\_\_\_\_

Boolean Expression :-

$$D_0 = \overline{A} \overline{B} \overline{C}$$

$$D_1 = \overline{A} \overline{B} C$$

$$D_2 = \overline{A} B \overline{C}$$

$$D_3 = \overline{A} B C$$

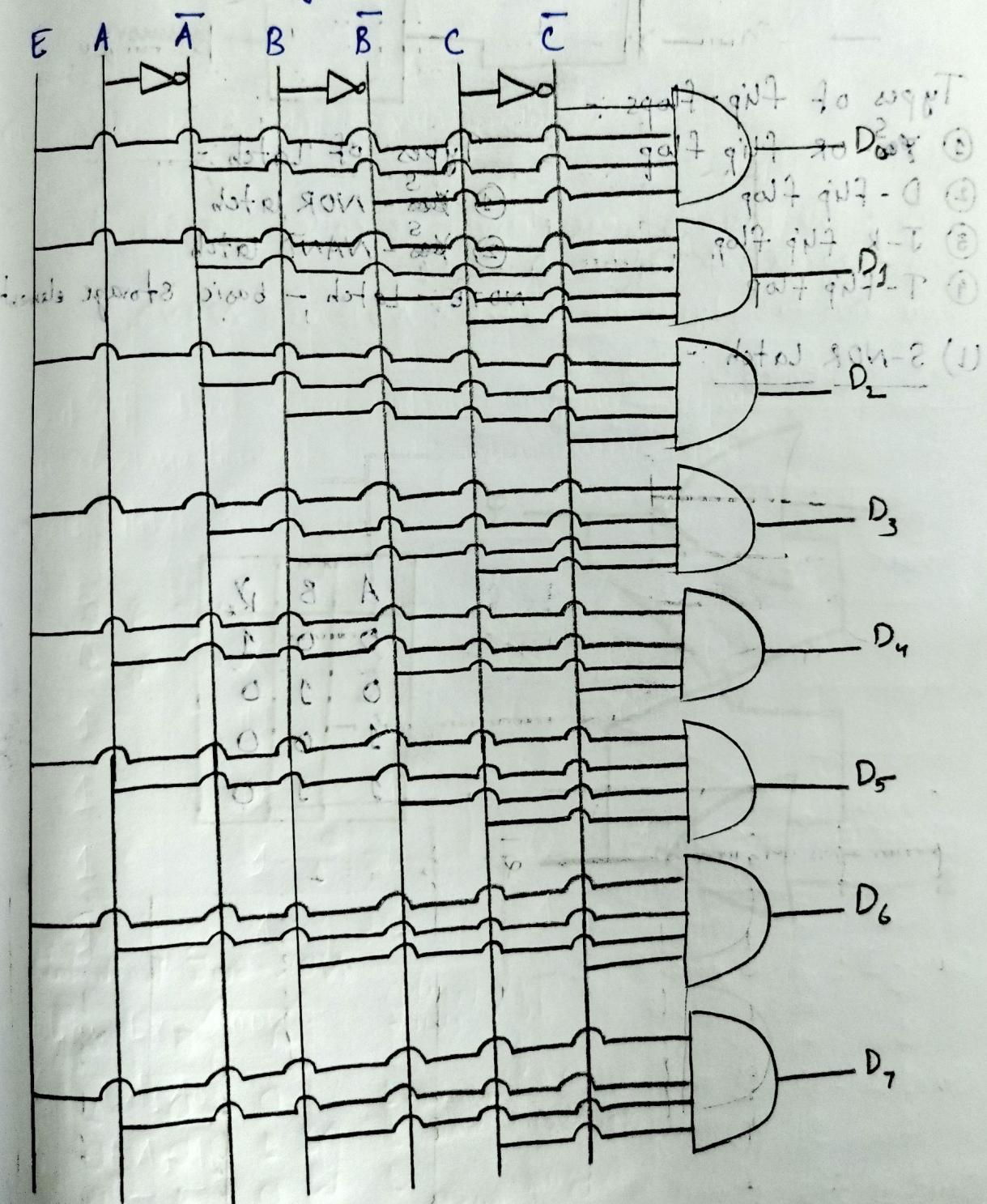
$$D_4 = A \overline{B} \overline{C}$$

$$D_5 = A \overline{B} C$$

$$D_6 = A B \overline{C}$$

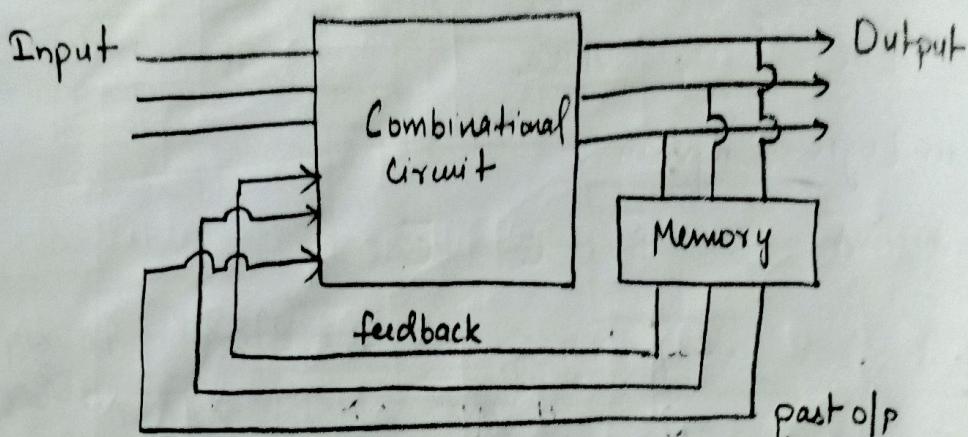
$$D_7 = A B C$$

Boolean Logic Diagram :-



## Sequential Circuits :-

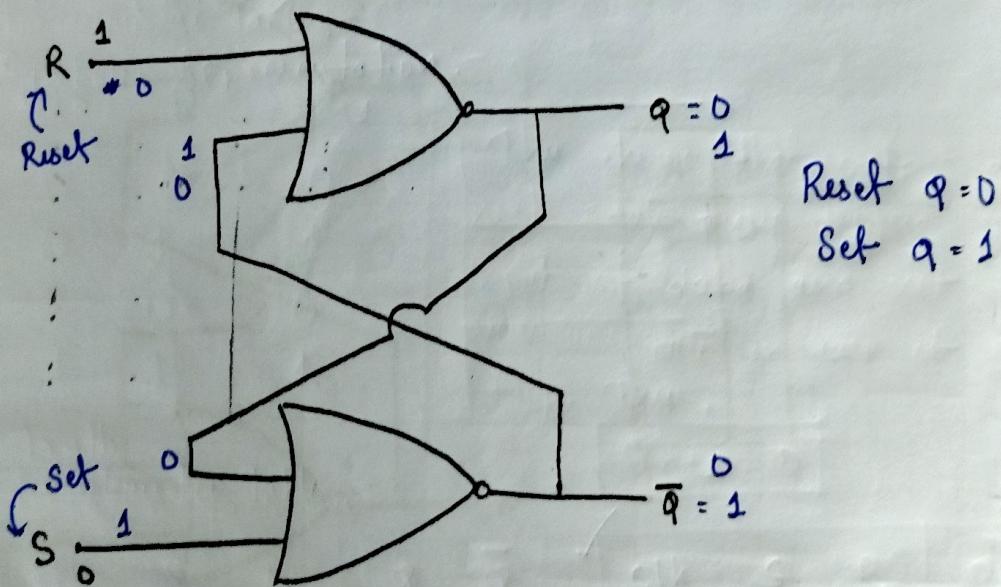
In sequential circuits, the present output depends on the present input as well as output/outputs.



Latch : The basic storage element is called LATCH. As the name suggests it latches '0' or '1'.

There are two types of Latch : NOR and NAND.

### NOR SR-Latch :-



Case - I :  $S = 0$  and  $R = 1$  }  
 $Q = 0$  and  $Q' = 1$  } First check

Case - II :  $S = 0$  and  $R = 0$  }  
 $Q = 0$  and  $Q' = 1$  } Memory state

Case - III :  $S = 1$  and  $R = 0$  }  
 $Q = 1$  and  $Q' = 0$  } gives memory state

Case - IV :  $S = 1$  and  $R = 1$  }  
 $Q = 0$  and  $Q' = 0$  } Invalid state

NOR-Gate Truth Table

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

Characteristics Table :-

S	R	Q	$\bar{Q}$
0	0	Memory	
0	1	0	1
1	0	1	0
1	1	Invalid	

Elaborating case (iv),

$S = 1, R = 1 ; Q = 0 \text{ and } \bar{Q} = 0$  (not possible)

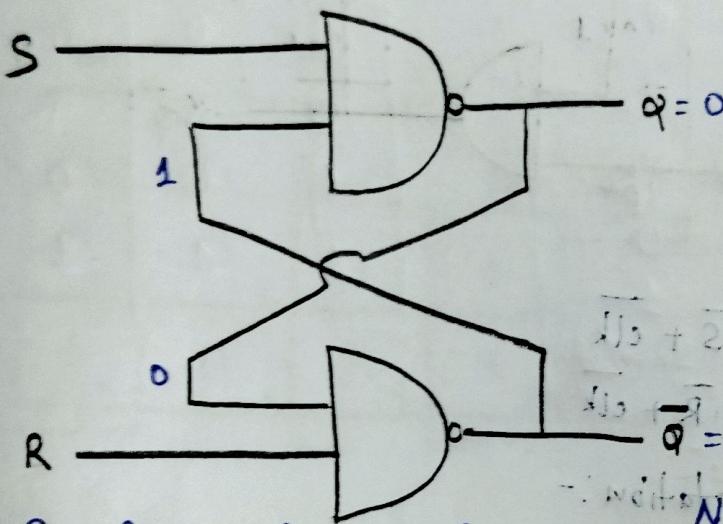
Starting from,  $Q = 0 \text{ and } \bar{Q} = 1 - 0$

$\bar{Q} = 0$  we get,  $\hookrightarrow$  start point

$Q = 1$  and  $\bar{Q} = 0 - (ii)$

(i)  $\neq$  (ii)

NAND-SR latch :-



Case-I :  $S = 1$  and  $R = 0$   
 $Q = 0$  and  $\bar{Q} = 1$  } first checking

Case-II :  $S = 1$  and  $R = 1$  ] Memory  
 $\bar{Q} = 1$  and  $Q = 0$  ] 8 state

Case-III :  $S = 0$  and  $R = 1$

$Q = 1$  and  $\bar{Q} = 0$

Checking for memory state,

$\therefore S = 1$  and  $R = 1$   $\Rightarrow$

$\bar{Q} = 0$  and  $Q = 1$

Characteristics Table :-

S	R	Q	$\bar{Q}$
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	Memory	

$$\overline{S} \cdot \overline{R} + \overline{S} = (\overline{S}, \overline{R}) = 1$$

$$\overline{S} \cdot \overline{R} = (\overline{S}, \overline{R}) = 1$$

NAND-Gate Truth Table :-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Case-IV :  $S = 0$  and  $R = 0$

$Q = 1$  and  $\bar{Q} = 1$  (wrong)

Also,  $S = 1$  and  $R = 1$

$Q = 0$  and  $\bar{Q} = 0 - (ii)$

Starting from  $\bar{Q} = 1$ ,

$Q = 0$  and  $\bar{Q} = 1 - (ii)$

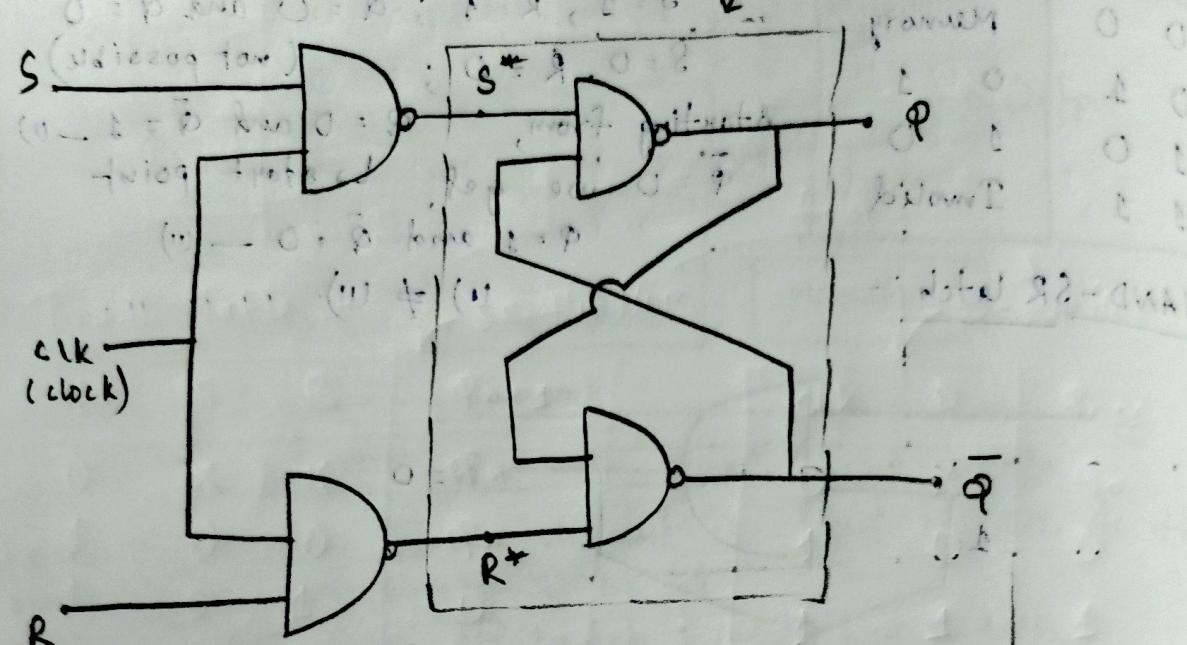
(i)  $\neq$  (ii)

$$P = \alpha \cdot \beta$$

$$\text{Total } P = \alpha \cdot \beta$$

$$\text{Total } P = \alpha \cdot \beta$$

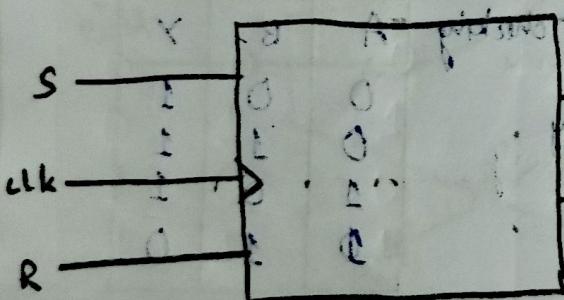
## SR-Flip Flop :-



$$S^* = (\overline{S} \cdot \overline{\text{clk}}) = \overline{S} + \overline{\text{clk}}$$

$$R^* = (\overline{R} \cdot \overline{\text{clk}}) = \overline{R} + \overline{\text{clk}}$$

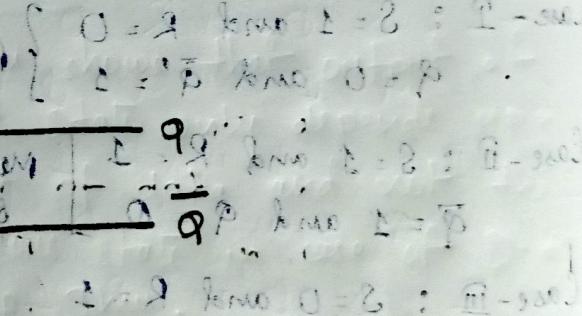
Symbolic Representation :-



Truth Characteristics Table :-

CLK = S = R =	Q & $\bar{Q}$
0	X X
1	0 0
1	1 1
1	0 1
1	1 0
1	1 1

Memory  
Memory  
0 1  
1 0  
Invalid



clk = S = R =	Q <sub>n+1</sub>
0	X X
1	0 0
1	1 1
1	1 0
1	0 1
1	1 1

Q<sub>n</sub> → Present state  
Q<sub>n+1</sub> → Next state

When,  
 $Q_{n+1} = Q_n$  (memory state)

Characteristics Table :-

$Q_n$	S	R	$Q_{n+1}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Excitation Table :-

$Q_n$	$Q_{n+1}$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

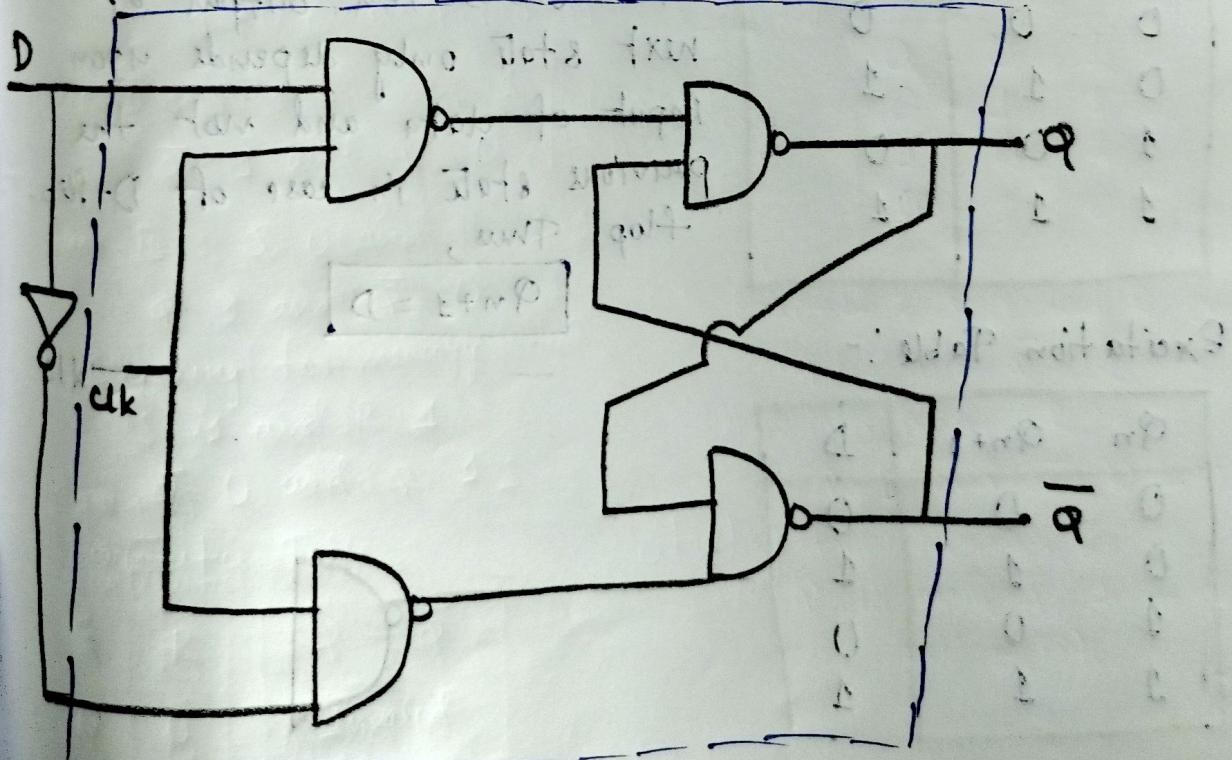
$Q_n$	SR	00	01	11	10	T
0	0	0	0	X	1	①
1	1	1	0	X	1	②

$$Q_{n+1} = \textcircled{1} + \textcircled{2}$$

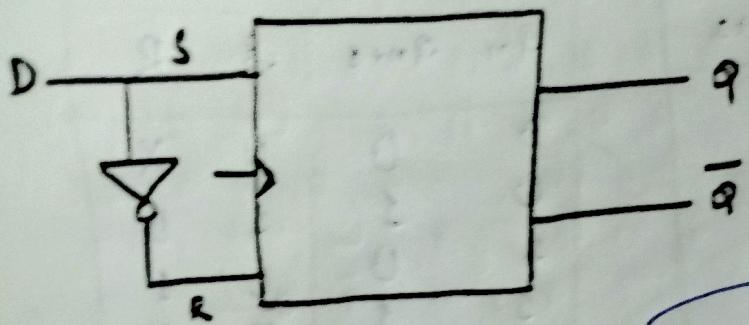
$$\textcircled{1} = S + Q_n \bar{R}$$

D-flip flop :-

SR - Fip flop



## Symbolic Representation :-



Truth Table :-

clk	S	R	$q_{n+1}$
0	X	X	$q_n$
1	0	0	$q_n$
1	0	1	0
1	1	0	1
1	1	1	Invalid

SR-flip flop

from

D-flip flop

clk	D	$q_{n+1}$
0	X	$q_n$
1	0	0
1	1	1

Characteristics Table :-

$q_n$	D	$q_{n+1}$
0	0	0
0	1	1
1	0	0
1	1	1

This shows that output of next state only depends upon input of data and not the previous state, in case of D-flip flop. Thus,

$$q_{n+1} = D$$

Excitation Table :-

$q_n$	$q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1