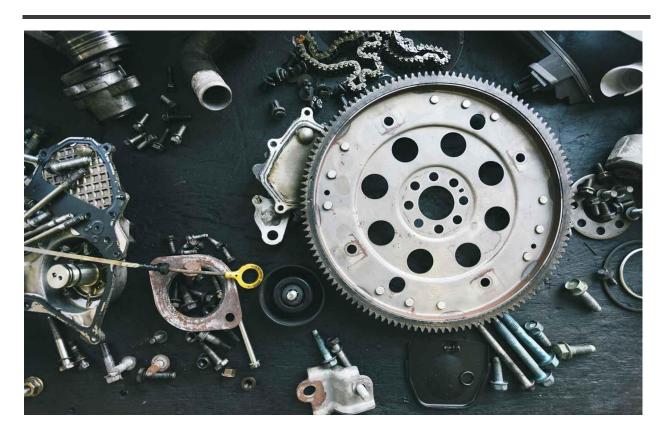
# NSWC CRANE PCB PROGRAM

## X-Force Created

August 14th, 2020

### **USER MANUAL**



All about the creation of the PCB script generator and how to use and update the program!

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#### **Abstract**

The National Security Innovation Network (NSIN) is an unrivaled problem-solving network that adapts to the emerging needs of those who serve in the defense of our national security. They are dedicated in bringing together defense, academic and entrepreneurial innovators to solve national security problems in new ways. Their main goal is to create a new alliance between the United States defense teams, academic students, and others in the community to help keep our national security safe. One way they allow this to happen is by hosting the X-Force Program. This program is an opportunity for students, technologists, and entrepreneurs to serve their country by solving real problems given by the United States military and the Department of Defense. During June 1<sup>st</sup>, 2020 – August 14<sup>th</sup>, 2020, students worked with the Naval Surface Warfare Center in Crane Indiana to create a program that sped up adding new high pin count devices to printed circuit boards.

#### **Introduction**

The Naval Surface Warfare Center (NSWC) tests electronic devices to determine their ability to handle radiation events whether natural or man-made. In addition, they also analyze devices from a security aspect. As industry pushes boundaries on more complex integrated circuits (IC'S) with higher pin counts capable of doing so much more than previous generations, NSWC too wants to leverage such technologies in next generation Department of Defense systems. In order to test these IC's, they need printed circuit boards (PCBs) allowing them to interface with the devices. Their design team is small, only about one to two people at a time. They want to be more efficient with their time.

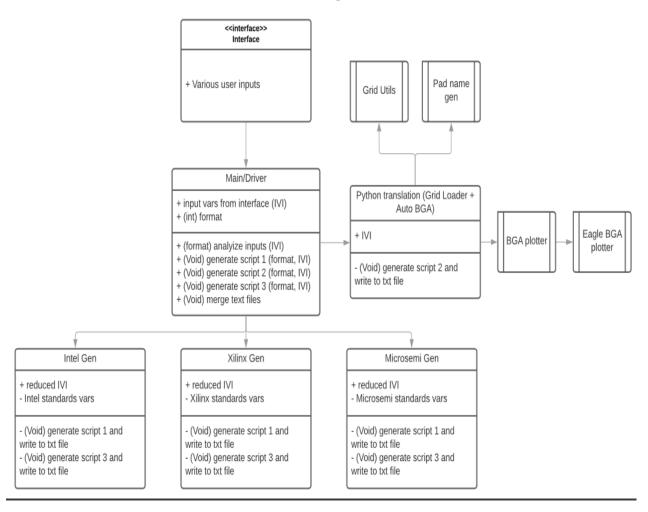
NSWC Crane uses a printed circuit board CAD program now owned by AutoDesk, Eagle 7.2.0. The software takes in a Schematic Symbol script, a Physical Footprint Layout script, and a Connection script. These come together and create a blue print for the scripted circuit board. Those three scripts are generated by a program that NSWC Crane has created, however the program has been redeveloped by X-Force fellows. The NSWC Crane program had two MATLAB files that created the Symbol script and the Connection script, and a Python File that generated the Footprint script. They have asked the X-Force fellows to create a single application, that is user friendly and scalable.

#### **Problem Statement**

As complex IC's get larger and use higher pin-count interfaces, the development time needing to add such components to Printed Circuit Board (PCB) CAD software libraries also increases. The scripting ability within the CAD software enables the user the ability to "automate" the step of adding the component to the PCB CAD software library. Design and create a program which will generate scripts that may be executed within the PCB CAD Software environment to expedite the process of adding new high pin count devices.

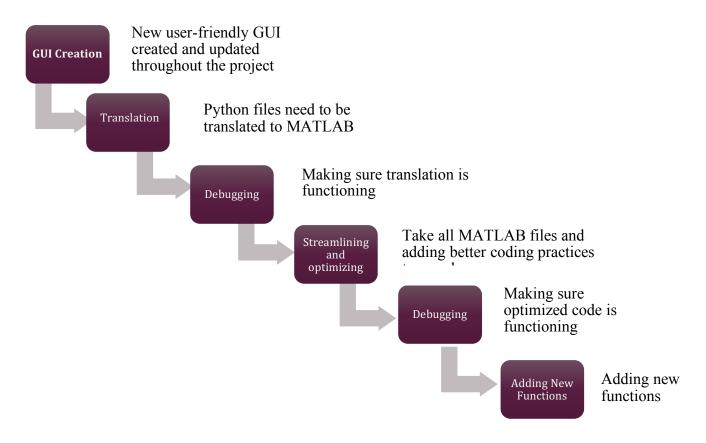
#### **Technical and Operational Details**

#### **UML Diagram**



*Figure 1:* The above figure is the UML Diagram created by Violet Todd, X-Force fellow.

#### **Project Procedures**



<u>Figure 2:</u> The above figure shows the steps taken to create a fully functioning program. This figure was created by Ivana Louis.

**GUI Creation:** The GUI was recreated to allow the user to have more control over the entire generation process. The user inputs the text file in the appropriate box, selects the manufacturer, adds an image to be processed, and fills out the foot print definition. Once all the information is filled out, the user clicks on "Confirm and generate" and a footprint grid pops up. This is then confirmed for use, and the scripts are generated and stored in your files. <u>Figure 3</u> shows the changes between the first GUI created by NSWC Crane and the new GUI.

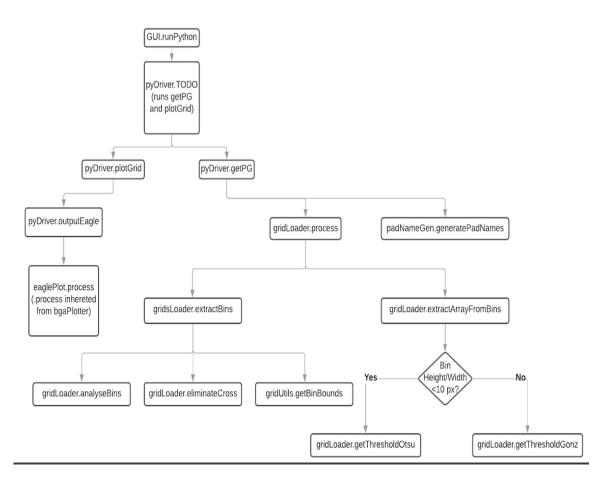
Old GUI  GXM EAGLE BGA  Script Generator							
User Inputs							
File Path							
Manufacturer Xillinx ▼							
Part Name							
Part #							
YES NO							
Headers							

	New GUI								
	GXM Eagl	e Script Generator							
Inputs file (.tx	ct, .xls, or .xlsx)	Browse files	0 100 Progress						
Part name	Imaç	ge file  Browse files	No Rerun? Yes						
Desired Pin Lim	nit per Bank: 30		Manufacturer						
Footprint Definition	on		Microsemi						
# of pins Pitch (mils)	0	# pads X dim 0  # pads Y dim 0	NAVEEA						
Pad diameter	0	Pack width 0	WARFARE CENTERS CRANE						
Pin A1 location	NW ▼	Pack height 0	CHANE						

<u>Figure 3:</u> The above figure shows the old GUI versus the New GUI. The new GUI allows the user full control over the script generation.

*Translation:* Once the GUI was complete the process moved on to code translation. The main goal was to create a program using a single platform. That platform was chosen to be MATLAB. All the Python files that were provided to the X-Force fellows were translated to MATLAB. From there, debugging was done to make sure that the files were working in their MATLAB form.

#### Flow Chart of Python Code



<u>Figure 3:</u> The above figure is a flow chart used to help understand the process of translating the python files and adding in a fully functioning image processing section. This figure was created by Violet Todd.

**Streamlining and optimizing:** The biggest complaint of the older code was running time. The files created took a large amount of time to parse. It was requested for the parsing to be optimized and streamlined to lower run time. This was done by going through the files and removing repeated and unnecessary code that was prolonging run time. Debugging was then redone to assure functioning code.

**Adding New Functions:** New functions were added to update the amount of options given to the user. These functions include image processing, the ability for the user to add pins in layers, and to edit input files to better suit their needs.

#### **How to use the Program**

#### **Formatting Xilinx Input Files**

For the various Xilinx families, you must first verify that the input is formatted correctly. The proper format should be a line which resembles "Device/package..." with some additional information following, the header line(s) (if present), followed by the data. It is possible for there to be a blank line present as well. The following is a properly formatted example from the Artix 7 family:

```
Device/Package xc7a15tftg256 10/31/2014 13:15:29
Pin Pin Name
                                  Memory Byte Group Bank VCCAUX Group Super Logic Region I/O Type No-Connect
H10 DONE 0
                                                          NΑ
                                                                        NΑ
                                                                                            CONFIG
                                                                                                     NΑ
                                                    0
K8 DXP 0
                                                                        NΑ
                                                                                           CONFIG
                                                                                                     NΑ
                                  NΑ
                                                    0
                                                          NΑ
G7 GNDADC_0
                                  NΔ
                                                    0
                                                          NΔ
                                                                        NΔ
                                                                                            CONFIG
                                                                                                     NΔ
G8
    VCCADC 0
                                  NΔ
                                                    0
                                                          NΔ
                                                                        NΔ
                                                                                            CONFIG
                                                                                                     NΔ
J8 VREFP 0
                                  NΔ
                                                    a
                                                          NΔ
                                                                        NΔ
                                                                                            CONFIG
                                                                                                     NΔ
                                                                                            CONFIG
J7 VN_0
                                                          NA
                                                                                                     NA
```

```
# (c) Copyright 2016 Xilinx, Inc. All rights reserved.
#
# This file contains confidential and proprietary informati
# of Xilinx, Inc. and is protected under U.S. and
# international copyright and other intellectual property
| laws.
#
# DISCLAIMER
# This disclaimer is not a license and does not grant any
# rights to the materials distributed herewith. Except as
```

However, some files have a large amount of information prior to the headers which should not be kept when running the program. The following is an example of file from Artix 7 which is not formatted properly, showing only the first few lines of many to the left.

To format this file properly, you will need to scroll down to extract certain information. The part with the information needed looks like this:

```
# ASCII Pinout File
#
# Device : xc7s50ftgb196
# Date : 12/5/2017 14:55:55
# Revision : 1.2
# Status : Production
#
# These package specifications are released coincident with production
# release of a particular device. Customers receive formal notification
# of any subsequent changes.
```

The information needed is that after "Device" and "Date". For the above example, we would want to type that information into a line which reads "Device/Package xc7s50ftgb196 12/5/2017 14:55:55". Place this line at the top of the file like this:

```
Device/Package xc7s50ftgb196 12/5/2017 14:55:55

# (c) Copyright 2016 Xilinx, Inc. All rights reserved.

# This file contains confidential and proprietary information

# of Xilinx, Inc. and is protected under U.S. and

# international copyright and other intellectual property

# laws.

# DISCLAIMER

# This disclaimer is not a license and does not grant any

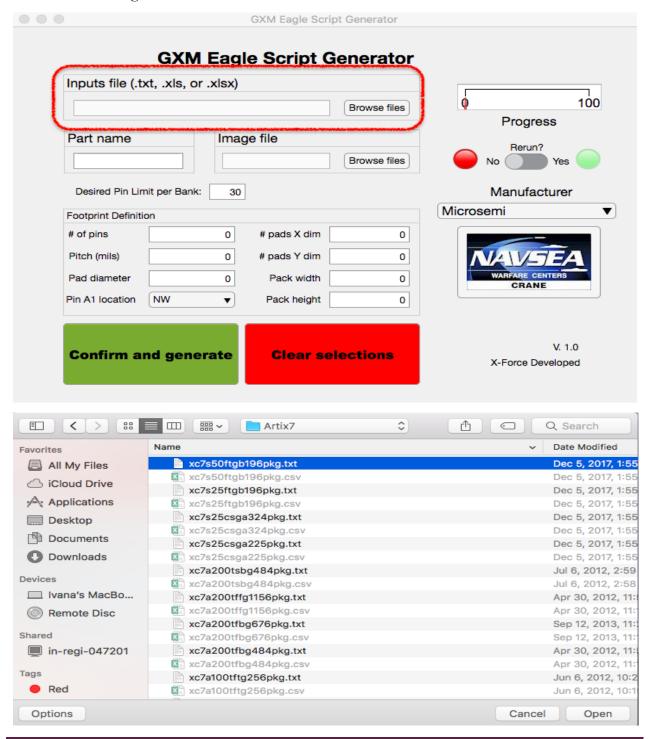
# rights to the materials distributed herewith. Except as
```

Next, delete all of the lines in the long introduction down until the headers, if present, or the first line of data, if there are no headers. Make sure there is one blank line between the "Device/Package..." line and the headers or data, resulting in the following:

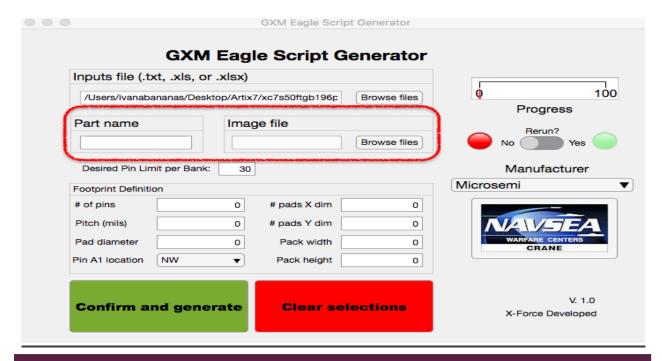
Device/Package xc7s50ftgb196 12/5/2017 14:55:55										
Pin	Pin Name	Memory Byte Group	Bank	VCCAUX Group	Super Logic Region	I/O Type	No-Connect			
P9	DONE_0	NA	0	NA	NA	CONFIG	NA			
J8	DXP_0	NA	0	NA	NA	CONFIG	NA			
F7	GNDADC_0	NA	0	NA	NA	CONFIG	NA			
F8	VCCADC_0	NA	0	NA	NA	CONFIG	NA			

Save the edited .txt file and then it will be ready to run through the program.

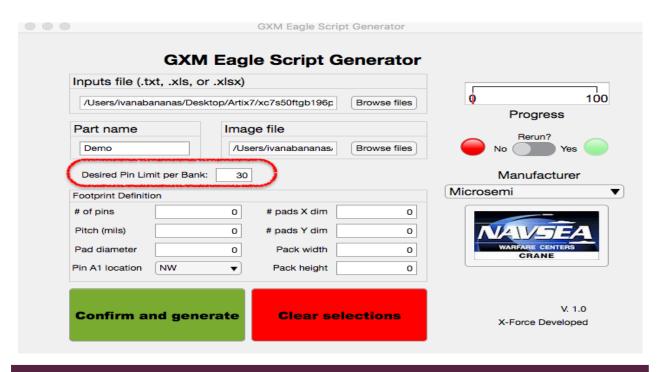
#### **Basic Run Through**



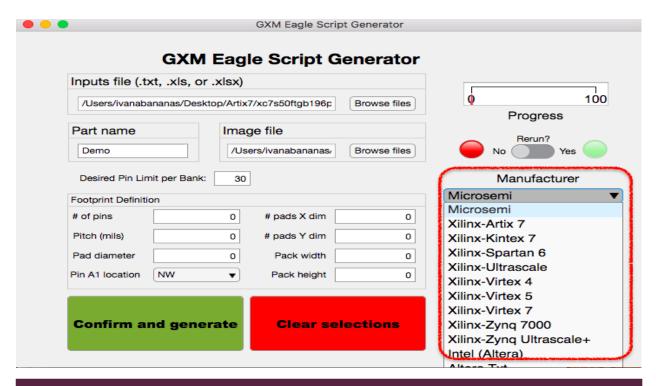
1. Begin by browsing your files for the text or excel file you will be working with. For this example, we will be using an Artix 7 file.



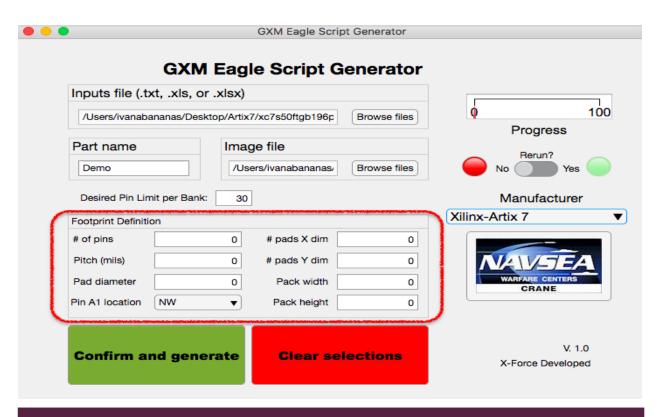
2. Add a name for your part so that the scripts can be saved and choose an image file if possible for the footprint.



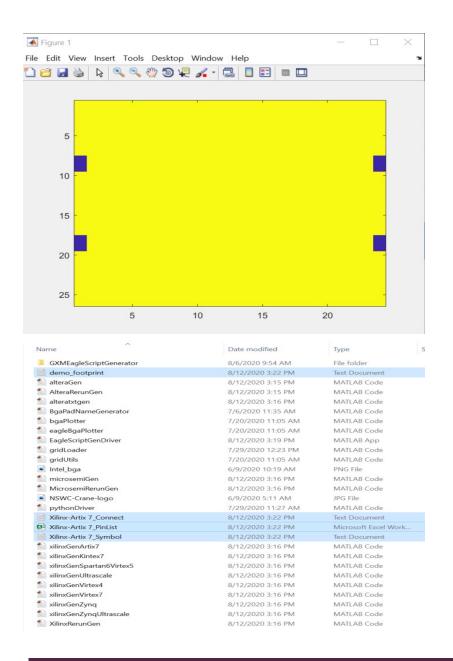
3. Add a desired pin limit per bank for your files. The desired pin limit is automatically set to 30, however it can be modified to your needs. If a pin limit is not desired, input 0.



4. Select a manufacturer. In this case, we are using Xilinx-Artix 7.



5. Fill out the footprint definition and hit the "Confirm and generate"

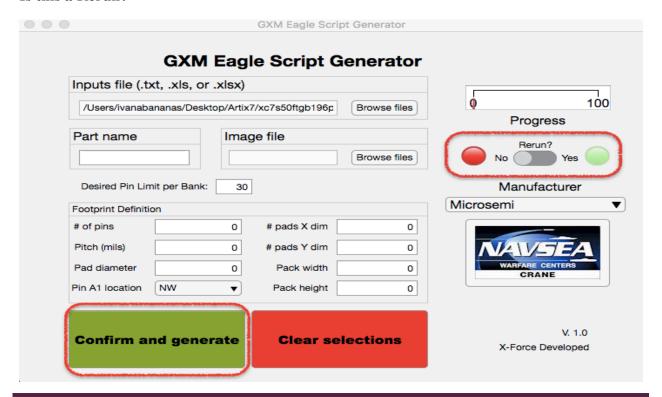


6. This pop up screen should pop up matching your image inserted in step two. If the display doesn't represent your image, you can click and change the incorrect boxes.

7. All of the generated scripts should be in created.

**Note:** After hitting "Confirm and generate," if running a file from Microsemi or Intel (Altera), a pop-up window will appear. Since both of these manufacturers, use Excel files with multiple tabs, you will need to type the name of the tab into the appropriate box in the window. If working with an Intel (Altera) file, there will be two additional boxes to complete, where you must indicate which columns you are using for the pin names and pads in your PCB generation. Simply enter in the number of the column, starting with 1 for the farthest left, 2 in the next column over and so on. Intel (Altera) files vary widely in terms of which columns they use and often will have multiple PCBs on one sheet in an Excel file distinguished by which column they are located in.

#### Is this a Rerun?



When running an input file from a manufacturer, the "Rerun?" switch should be turned off. If, after running the program, you decide that you wish to switch around which banks the pins are located on, use the \_PinList.xlsx file to edit the banks to resemble your desired configuration. Upon completing this, save the \_PinList.xlsx file and use it as the input in the GUI. Flip the "Rerun?" to "on" and click "Confirm and generate."

#### **NAVSEA Logo**



When clicking on the NAVSEA logo, you will be redirected to the NAVSEA Crane website!