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|  |  |
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| Class: | Engr M20/L – Moorpark College |
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Lab 5: Second Order Circuits

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| Lab Partners: | Roland Terezon  Daniel Alaya |

**Objective**

Analyze second-order circuits using standardized methods and PSPICE, and compare the theoretical results with those found in the lab experiment.

**Theory**

Note: Theories, concepts, and proofs heavily quoted from “Fundamentals of Electric Circuits” 5th edition & Wikipedia.

**Second-Order Circuits**

A circuit which is characterized by a second-order differential equation. It consists of resistors and the equivalent of two energy storage elements.

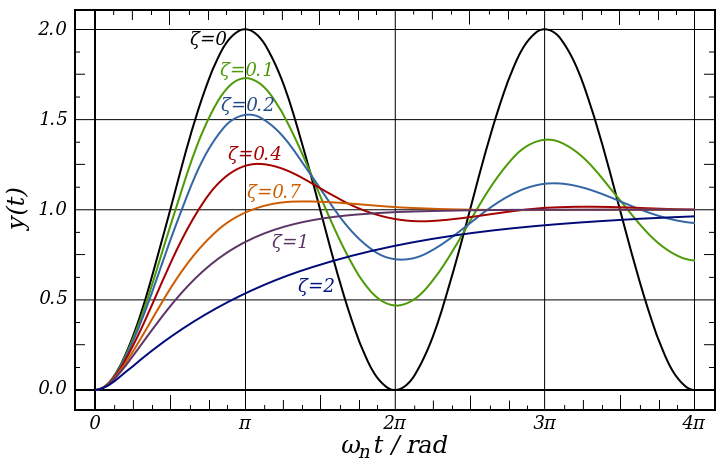
**Capacitor, C**

Device used to store an electric charge, consisting of one or more pairs of conductors separated by an insulator. The voltage across a capacitor in respect to time: , and the current in respect to time: .

**Inductor, L**

Device that stores energy in a magnetic field when electric current flows through it. An inductor typically consists of an insulated wire wound into a coil around a core. The voltage across an inductor in respect to time: , and the current in respect to time: .

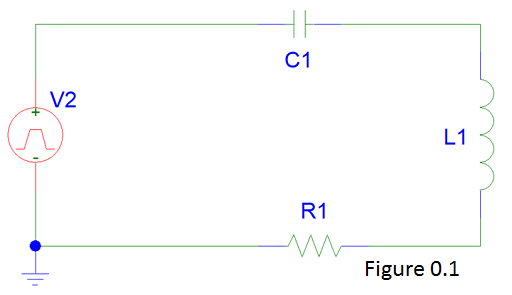
**Damping Ratio**

Dimensionless measure describing how oscillations in a system decay after a disturbance. The value is denoted by ζ (zeta, z), which can vary from undamped (z=0), underdamped (z<1), critically damped (z=1), and overdamped (z>1).

Damping is caused by the resistance in the circuit. It determines whether or not the circuit will resonate naturally (that is, without a driving source). Circuits which will resonate in this way are described as underdamped and those that will not are overdamped.

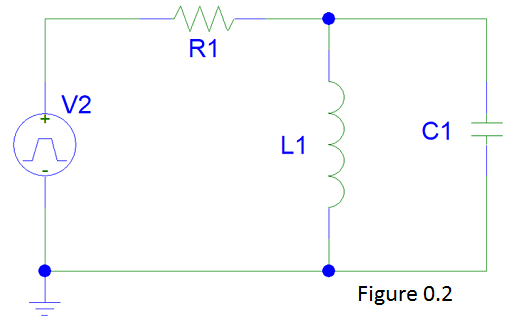
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| --- | --- | --- |
|  | | |
|  |  |  |
|  |  | **EQ 0.1** “Critical Damping” |
|  |  |  |
|  |  | **EQ 0.2** “Over-Damped’ |
|  |  |  |
|  |  | **EQ 0.3** “Under-Damped” |
|  |  |  |
|  |  | **EQ 0.4** “Un-Damped” |

**Capacitor and Inductor in Series**

The circuit shown in Figure 0.1 is analyzed in this lab. In this circuit, a capacitor, inductor, and resistor are in series. A square wave pulse is used for the input voltage. The pulse’s high and low times are large enough to allow a complete charge and discharge of the system over the course of one period. The voltage across the resistor is derived below. Note that the waveform will depend upon the damping ratio as seen in EQ 1.4.

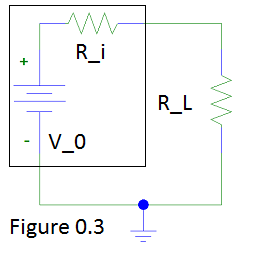
|  |  |  |
| --- | --- | --- |
|  |  | KVL |
|  |  |  |
|  |  | EQ 1.1 |
|  |  |  |
|  |  | Take Derivative. |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  | EQ 1.2 |
|  |  |  |
|  |  | EQ 1.3 |
|  |  |  |
|  |  | Because right side of ‘=’ is constant 0. |
|  |  |  |
|  |  | Differential Equations. (DE) |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  | **EQ 1.4** |
|  |  |  |
|  |  | Quadratic Equation. |
|  |  |  |
|  | | |
|  | | |
|  |  |  |
|  | | |
|  |  |  |
|  |  | Solve in terms of V across R |

**Capacitor and Inductor in Parallel**

The circuit shown in Figure 0.2 is analyzed in this lab. In this circuit, a capacitor and inductor in parallel. A square wave pulse is used for the input voltage. The pulse’s high and low times are large enough to allow a complete charge and discharge of the system over the course of one period. The voltage across the capacitor is derived below. Note that the waveform will depend upon the damping ratio as seen in EQ 2.4.

|  |  |  |
| --- | --- | --- |
|  |  | KCL |
|  |  |  |
|  |  | EQ 2.1 |
|  |  |  |
|  |  | Take Derivative. |
|  |  |  |
|  |  | EQ 2.2 |
|  |  |  |
|  |  | EQ 2.3 |
|  |  |  |
|  |  | Because right side of ‘=’ is constant 0. |
|  |  |  |
|  |  | Differential Equations. (DE) |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  | **EQ 2.4** |
|  |  |  |
|  |  | Quadratic Equation. |
|  |  |  |
|  | | |
|  | | |
|  |  |  |
|  | | |
|  |  |  |
|  |  | Solve in terms of V across L |

**Internal Resistance of Power Supply (Square Wave Generator)**

The square wave generator used in Figures 0.1 and 0.2 has an internal resistance. This resistance can be found by sampling the voltage across the generator when no load is present, and then again when a load is present. It’s easiest to picture the internal resistance as a resistor in series with the voltage source, which Figure 0.3 illustrates. This is mere voltage division, where V0 is the voltage with no load, and VL is the voltage across the added load, RL. The internal resistance, Ri, is derived below.

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| --- | --- | --- |
|  |  | Voltage Division |
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|  |  |  |
|  |  |  |
|  |  | **EQ 3.1** |

**Procedure**

**Part 1:**

**Data & Calculations**

**Calculation 1.1**

**Discussion of Results**

**Part 1:**

**Appendix**

