Ivan Cordoba

(602) 369-4423 | <u>ivanc95@email.arizona.edu</u> 4937 W Krall St, Glendale, AZ 85301

Education

Bachelor of Science, Electrical and Computer Engineering University of Arizona, Tucson, AZ 85719 Anticipated Graduation - May 2017 | Expected GPA: 3.3

Technical Skills

Experience with:

- Web Design, Object-Oriented Design, Agile Development
- Android Development
- Computer architecture and RISC processor design, testing on FPGA boards
- Logic Design using HLS and RTL while taking into account optimizations and tradeoffs
- Theories of Circuits and Signals
- Working in a lab designing, building, and testing circuits
- Programming Micro-controllers/Microprocessors, Communication Protocols (I2C, SPI, UART)
- Semiconductor Design and Processing
- Computer Networks and Protocols (TCP, UDP), Network Security (Cryptography, Protocols)
- Data Analysis (Graph Theory, Linked Lists)

Programming - Node, Python, Java, C/C++, HTML, CSS, PHP, Javascript, SQL, DOM, JSON, AJAX, Git (VCS), Verilog, MIPS, Assembly

Environments - Vivado, Xilinx ISE, Windows/Mac OS X, Linux, Xcode, Visual Studio, Eclipse, Matlab, Android Studio, MPLabX, Arduino

Lab Skills - Oscilloscope, Function Generator, Multimeter, Micro-controllers, Soldering, Wire Wrapping, Safety Protocols

Projects

CAT Autonomous Vehicle Project:

Created ROS software components, which are then prototyped using Simulink toolboxes. Final design is used on the CAT autonomous vehicle at the University of Arizona.

Line Following Car:

Used a microprocessor and an IR array along with various other components to design a small car that can follow a black line on the floor. Design recognized for completing given test track the fastest.

Dynamic Website:

Created a dynamic website that allows user to search IMDB's database. Project was completed using HTML, CSS, PHP, and JavaScript utilizing DOM and AJAX.

General Purpose Processor:

Designed and implemented a general purpose RISC processor that implements Pipelining with Forwarding and Hazard Detection. This processor was synthesized onto an FPGA board to verify it's functionality.

Senior Project/Anti-drone Device:

Worked in a team of 6 Engineers from different disciplines to design and create a device that can immobilize an incoming drone. Design process includes creating various documents and presentations (PDR, CDR, TRR, etc). Design utilizes a Raspberry pi and some Python code to take down a drone.

Verilog Code Generation:

C++ net-list files are parsed. Force Directed Scheduling is used to optimize for minimum resource usage before being converted to a proper Verilog file. Graph theory played a large role in this project.

Other Skills/Personal Achievements

- Received award for academic distinction from the College of Engineering at the University of Arizona
- Great leadership abilities: Student Government President in High School
- Spanish Speaker Minimum Professional Proficiency