University of California Riverside
EE/CS120A-Logic Design-2021 Fall
Instructor: Jia Chen

Homework 2

Submission deadline: Nov. 17th, Wednesday

Problem 1: Manipulate a circuit in Figure 1 so that it uses only NAND gates

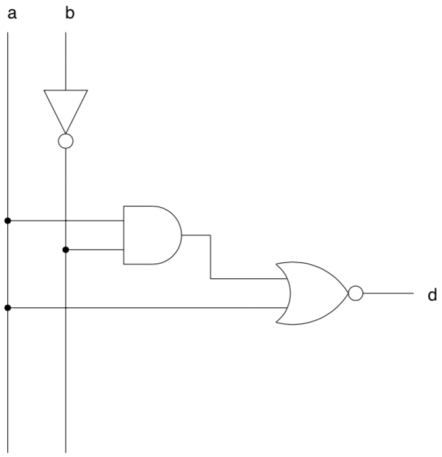


Figure 1

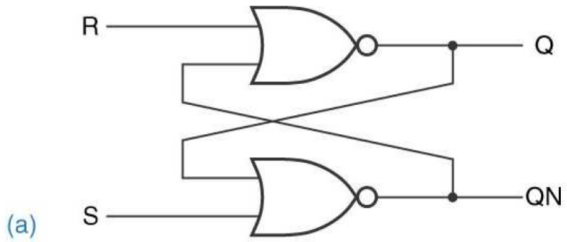
Problem 2: Using Karnaugh Maps, find a simplest SOP expression for each of the following functions.

1) $F = \Sigma_{X,Y,Z}(1,3,5,6,7)$;
2) $F = \Sigma_{W,X,Y,Z}(0,1,6,7,8,9,14,15)$;
3) $F = \Pi_{W,X,Y}(1,4,5,6,7)$

Problem 3: Using Karnaugh Maps, find a simplest POS expression for each of the following functions.

1) $F=\Sigma_{W,X,Y,Z}(0,1,6,7,8,9,14,15)$;
2) $F=\Pi_{W,X,Y}(1,4,5,6,7)$

Problem 4: Sketch the outputs (Q and QN) of an SR-Latch (the basic latch) of the type shown in Figure 4 for the input waveforms shown below Figure 4. Assuming that initially Q=0 and QN=1.

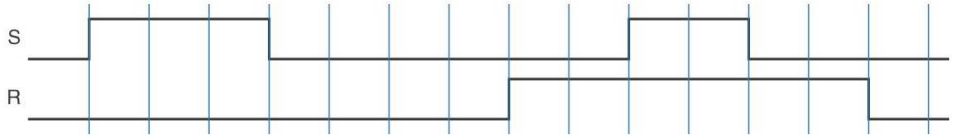


(a)

(b)

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

Figure 4: Circuit (a) and characteristic table (b) of SR-Latch



Problem 5: Sketch the Output of a Master-Slave D Flip-flop for the input waveforms shown below. Assuming that initially Output=0.