## **QUESTION 3**

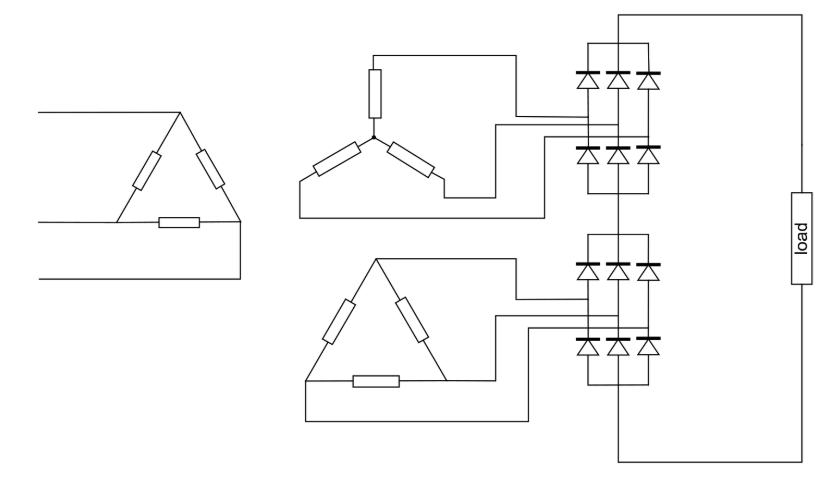


Figure 1: 12 pulse uncontrolled series connected bridge rectifier

Figure 1 shows a 12-pulse uncontrolled series connected bridge rectifier. Primary delta leads the secondary wye by 30o, hence secondary delta leads secondary wye by 30o as well. Therefore; the three-phase voltages supplying bridges are displaced by 30° resulting in 12 peaks per period of 20ms in the output voltage waveform.

12 pulse rectifiers can be obtained by half-wave (Figure 2) and parallel connected bridge (Figure 3) topologies. [1]

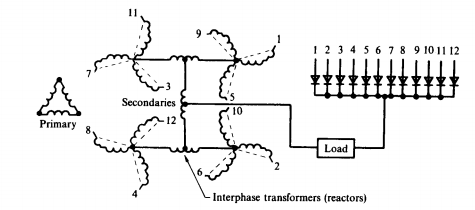


Figure 2: 12 pulse uncontrolled half-wave rectifier

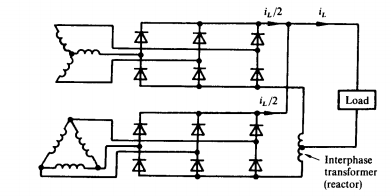


Figure 3: 12 pulse uncontrolled parallel connected bridge rectifier

In Figure 2, four wye connected secondary side windings are interconnected with reactors to give phases 30° apart from each other. 12 pulse uncontrolled parallel connected bridge rectifier works in the same fashion with its series version.

As the number of pulses increases output voltage waveform gets closer to dc form, whereas line current reaches to a sinusoidal form. Therefore, advantages of this rectifier are reduced THD level (Only 11th,13th harmonics) and voltage ripple output, increased output voltage. Thanks to these advantages high pulse rectifiers are used in HVDC transmission. The main disadvantage is the size of the equipment. [2] Also, frequency is doubled for 12 pulse rectifier so switching losses become larger.

There are 18-pulse, 24-pulse, 48-pulse and higher variations of this rectifier topology as well. Harmonics of these topologies can be found by (1) where n is the number of pulses.

18 pulse rectifier topology adds one more secondary windings and one rectifier in 12 pulse topology. Using phase shifting transformers 20o shift is displaced between pulses. [3]. 24 pulse rectifier uses 15o shifts between phases in Figure 5, whereas 48 pulse rectifiers has 7.5o shifts.

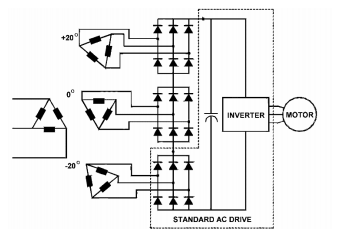


Figure 4: 18 pulse uncontrolled rectifier

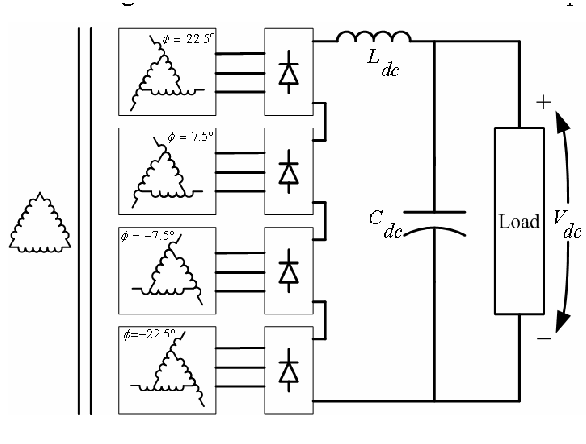


Figure 5: 24 pulse uncontrolled rectifier (Retrieved from [www.semanticscholar.org](http://www.semanticscholar.org))

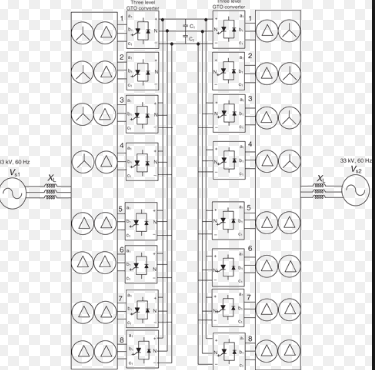


Figure 6: 48 pulse uncontrolled rectifier (Retrieved from www.degruyter.com)

b) Peak values of the output voltage are given by (2) and mean of the output voltage is found by (3) and (4).

(2)

We know that mean output voltage of a three-phase full bridge diode rectifier is given by (5) whereas 12-pulse rectifier’s is (4).

Therefore, we must choose 12 pulse bridge rectifier supply as **Vll =200V** so that both topologies produce the same average output voltage and average load current. To simulate 12 pulse rectifier Simulink topology in Figure 7 is used. Unfortunately, with this simplified topology phase currents in the primary side windings cannot be observed. However, 3rd, 5th, and 7th harmonics of the line current is eliminated resulted in a lower input THD level. Figure 8 and 9 show load current and voltage waveforms of 12 pulse and 6 pulse rectifiers, respectively. FFT analysis of these output voltage waveforms suggests **540V** dc components. As it can be seen, another advantage of 12 pulse rectifier is reduced input voltage.

Output ripple is 19V for 12 pulse rectifier and 75V for 6 pulse rectifier. Also, frequency is doubled which means smaller time constants for capacitors. Therefore; capacitor sizes decrease as the number of pulses increases. As switching frequency is increased, so do switching losses.

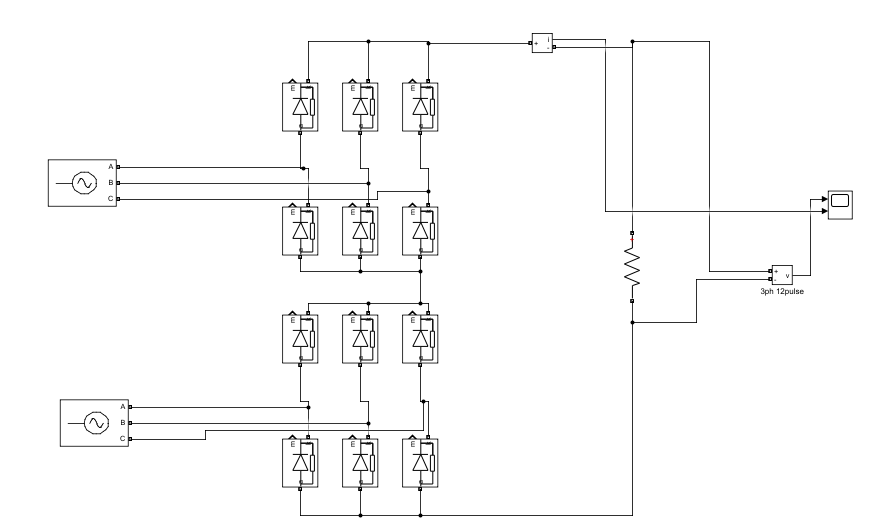


Figure 7: Simulink topology of 12 pulse uncontrolled series connected bridge rectifier

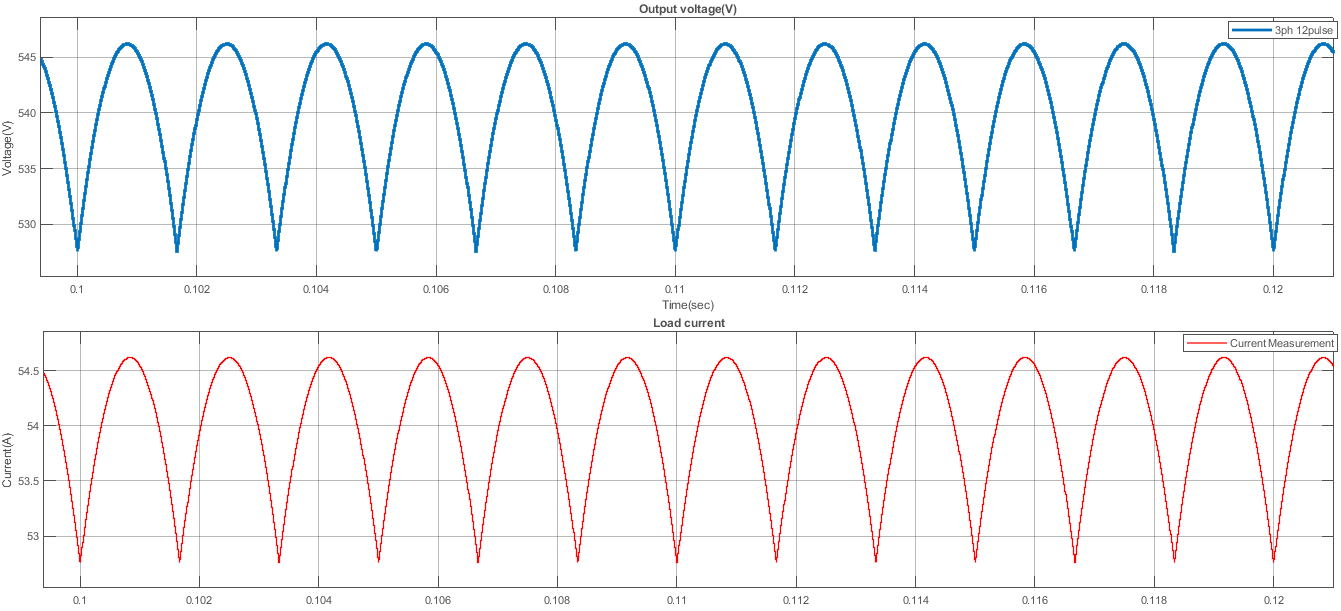


Figure 8:Output waveforms of 12 pulse uncontrolled series connected bridge rectifier

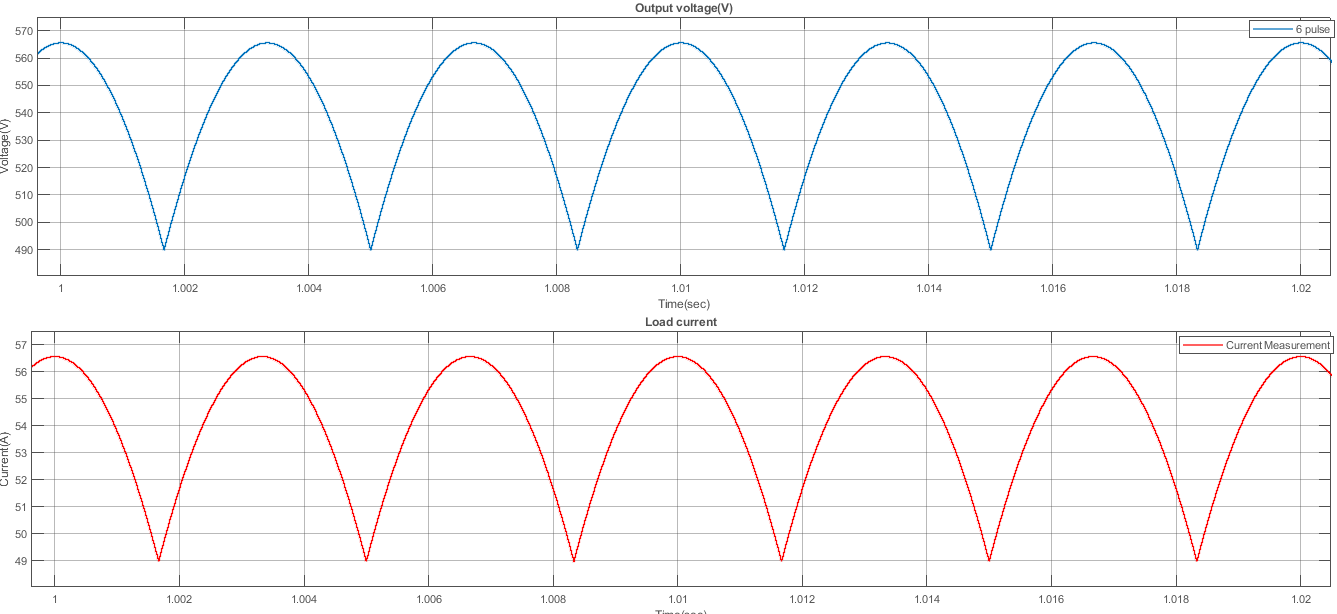


Figure 9: Output waveforms of 6 pulse uncontrolled series connected bridge rectifier

**[1] lander**

**[2]** siemens [**https://w3.siemens.no/home/no/no/sector/industry/marine/pages/12\_pulse\_system\_configuration.aspx**](https://w3.siemens.no/home/no/no/sector/industry/marine/pages/12_pulse_system_configuration.aspx)

**[3]**

**https://adfpowertuning.com/images/pdfs/Comparing\_Harmonics\_Mitigation\_Techniques\_2col\_REV3.pdf**