Intern Project Report
未來之星實習計畫專題成果報告
FPGA to perform BIOS seamless update (as a SPI Master)

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wistron

Outline

Outline

- Background
  - Coyote BIOS Seamless Update Topology
- Target
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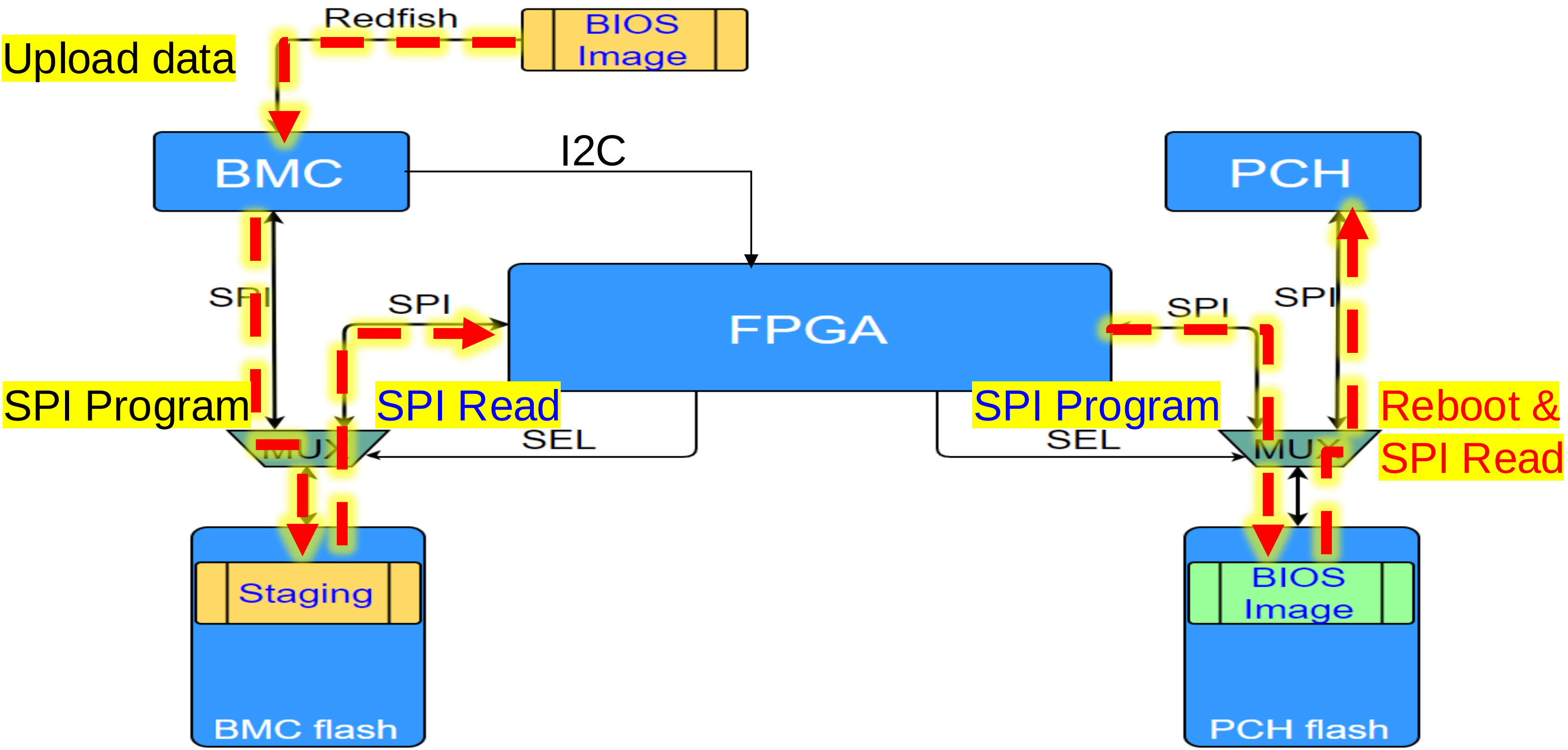
  - Schedule
- System architecture
- Verification
  - Simulation
  - Board level
- Conclusion
  - Future work
  - Conculusion

Background

Coyote BIOS Seamless Update Topology

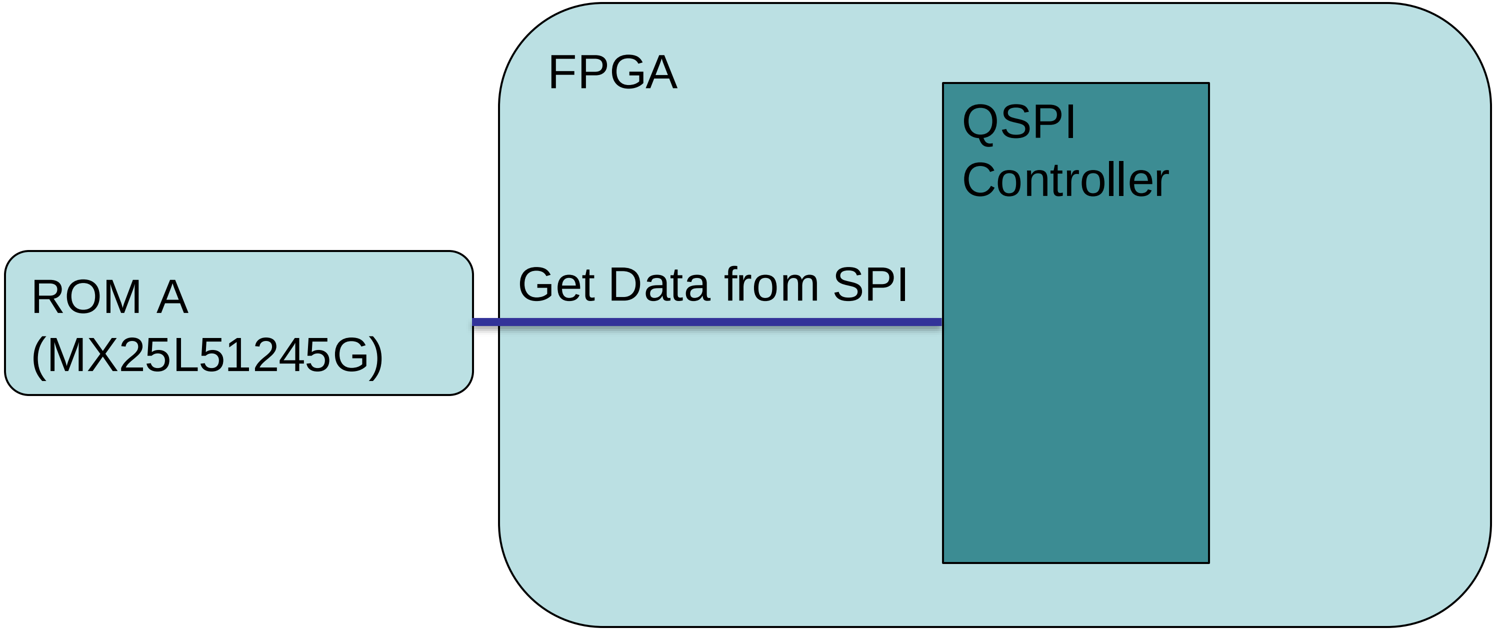


Target

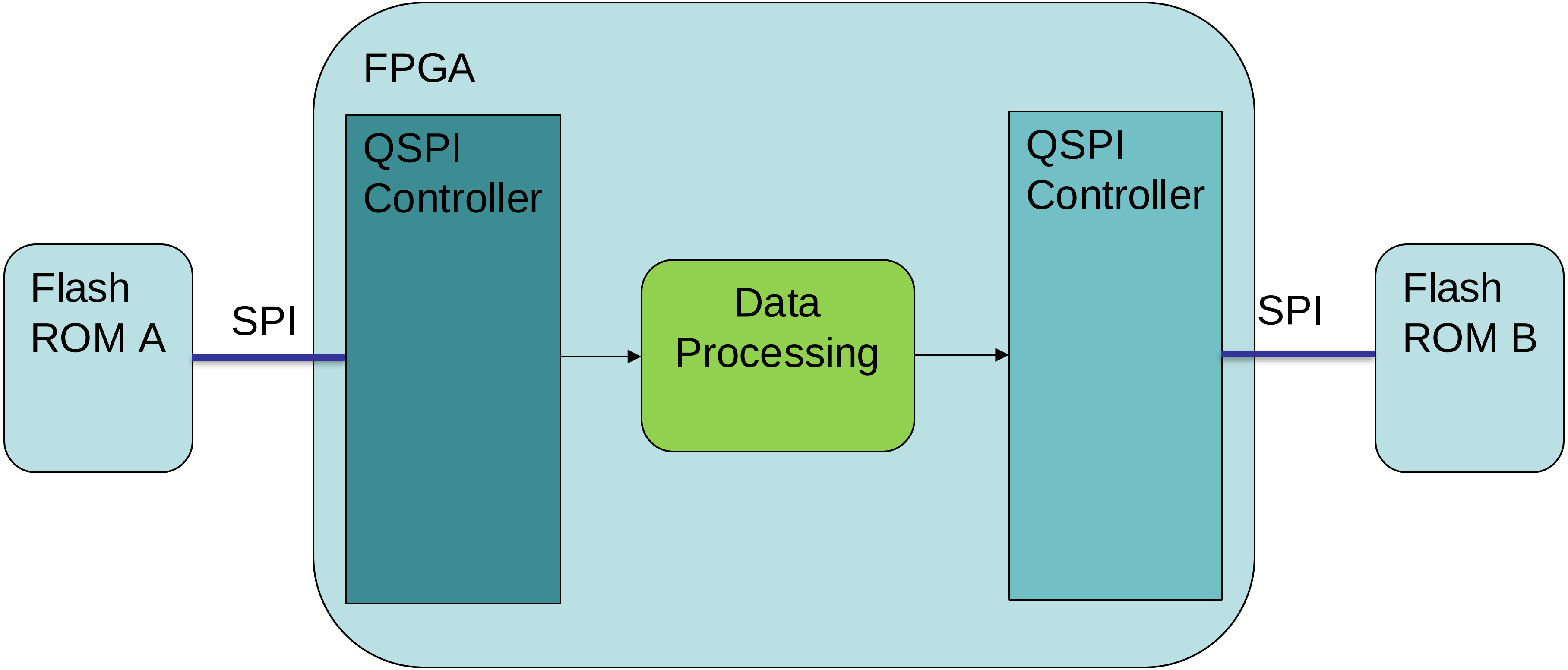
Project Target(1/3)

- First stage
  - –FPGA read data from Flash ROM A
- Second stage
  - –FPGA read data from Flash ROM A
  - –FPGA write data to Flash ROM B

Project Target(2/3)

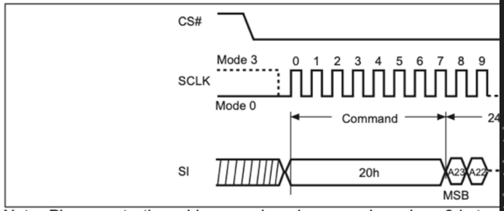


Project Target(3/3)



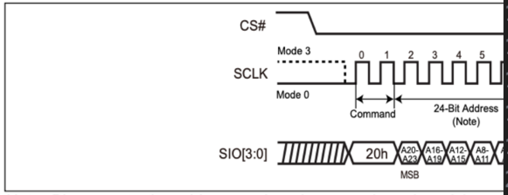
Schedule

Figure 80. Sector Erase (SE) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte a
address cycles will be increased.

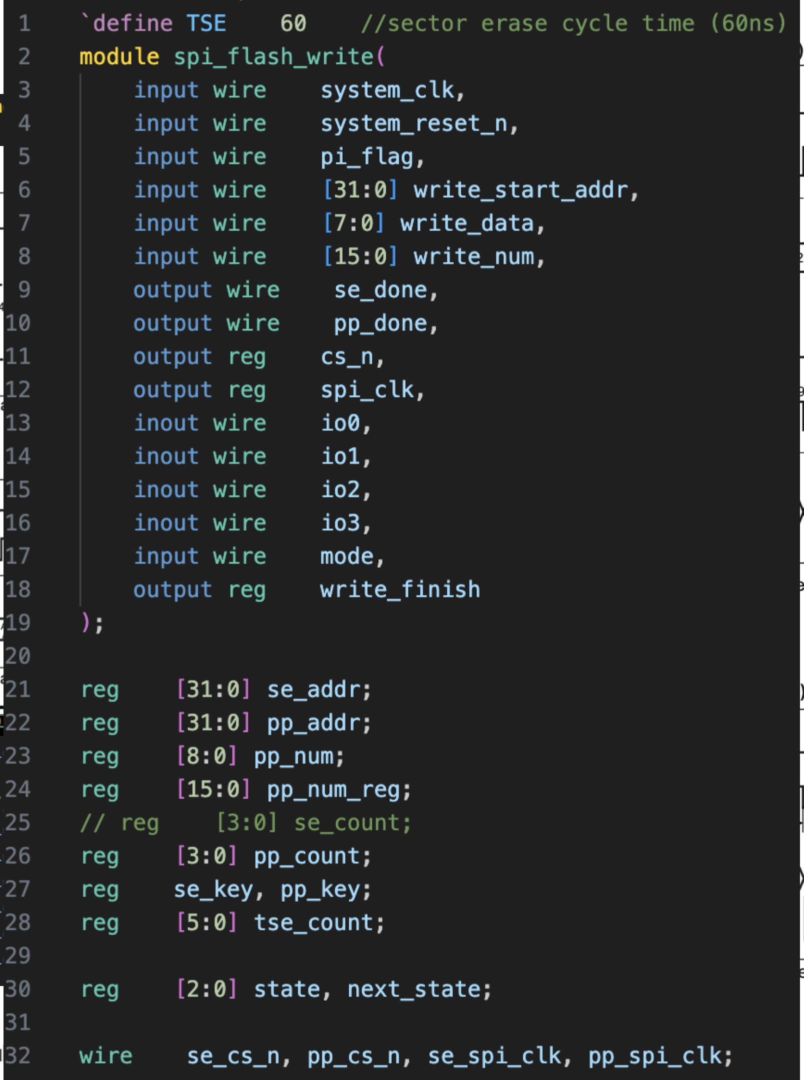
Figure 81. Sector Erase (SE) Sequence (QPI Mode)



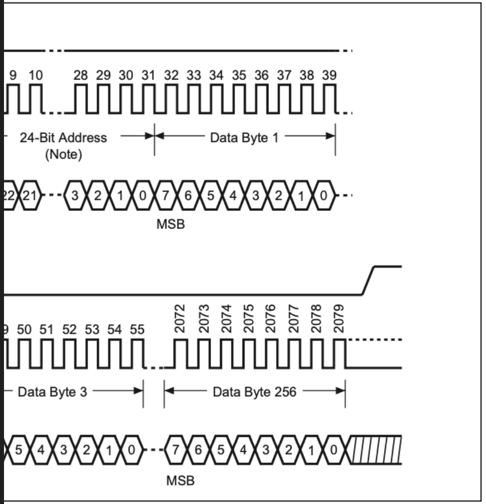
Note: Please note the address cycles above are based on 3-byte a
address cycles will be increased.

/top_read_vlg_tst/uut/s1/qspi_ctrl4read/byte_cnt 9

Earse cmd & Page Progra (Sector earse,Standard,Qua
Earse & Page cmd coding
Final Verification & Debug
Presentation Final stage

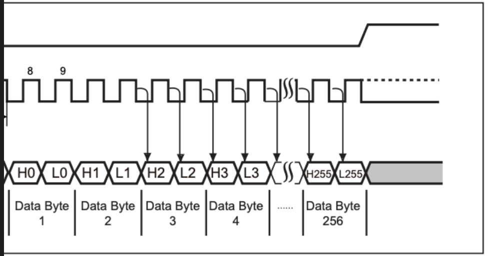


```
`define TSE    60    //sector erase cycle time (60ns)
module spi_flash_write(
    input wire    system_clk,
    input wire    system_reset_n,
    input wire    pi_flag,
    input wire    [31:0] write_start_addr,
    input wire    [7:0] write_data,
    input wire    [15:0] write_num,
    output wire    se_done,
    output wire    pp_done,
    output reg    cs_n,
    output reg    spi_clk,
    inout wire    io0,
    inout wire    io1,
    inout wire    io2,
    inout wire    io3,
    input wire    mode,
    output reg    write_finish
);

reg    [31:0] se_addr;
reg    [31:0] pp_addr;
reg    [8:0] pp_num;
reg    [15:0] pp_num_reg;
// reg    [3:0] se_count;
reg    [3:0] pp_count;
reg    se_key, pp_key;
reg    [5:0] tse_count;

reg    [2:0] state, next_state;

wire    se_cs_n, pp_cs_n, se_spi_clk, pp_spi_clk;
```



ed on 3-byte address mode. For 4-byte address mode, the

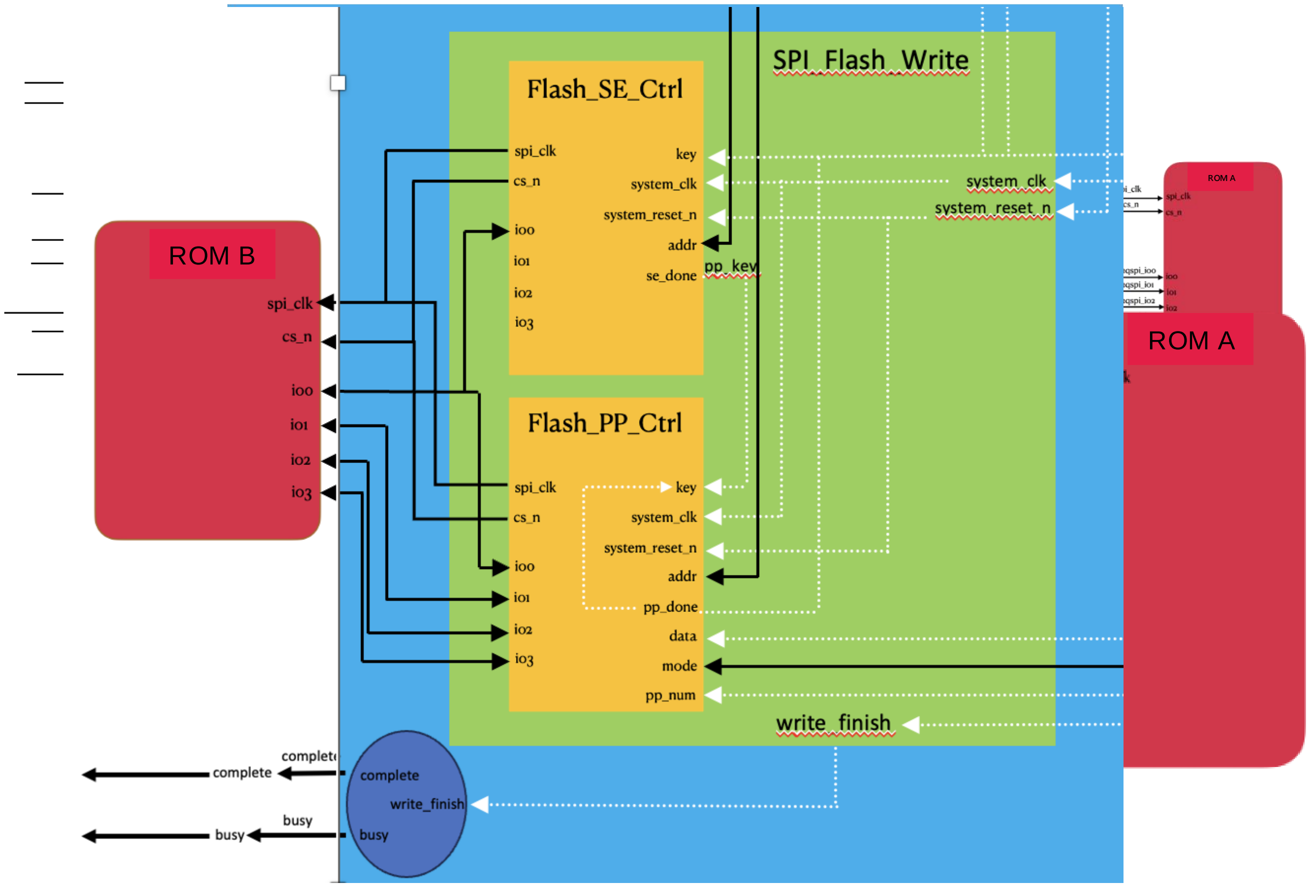
)



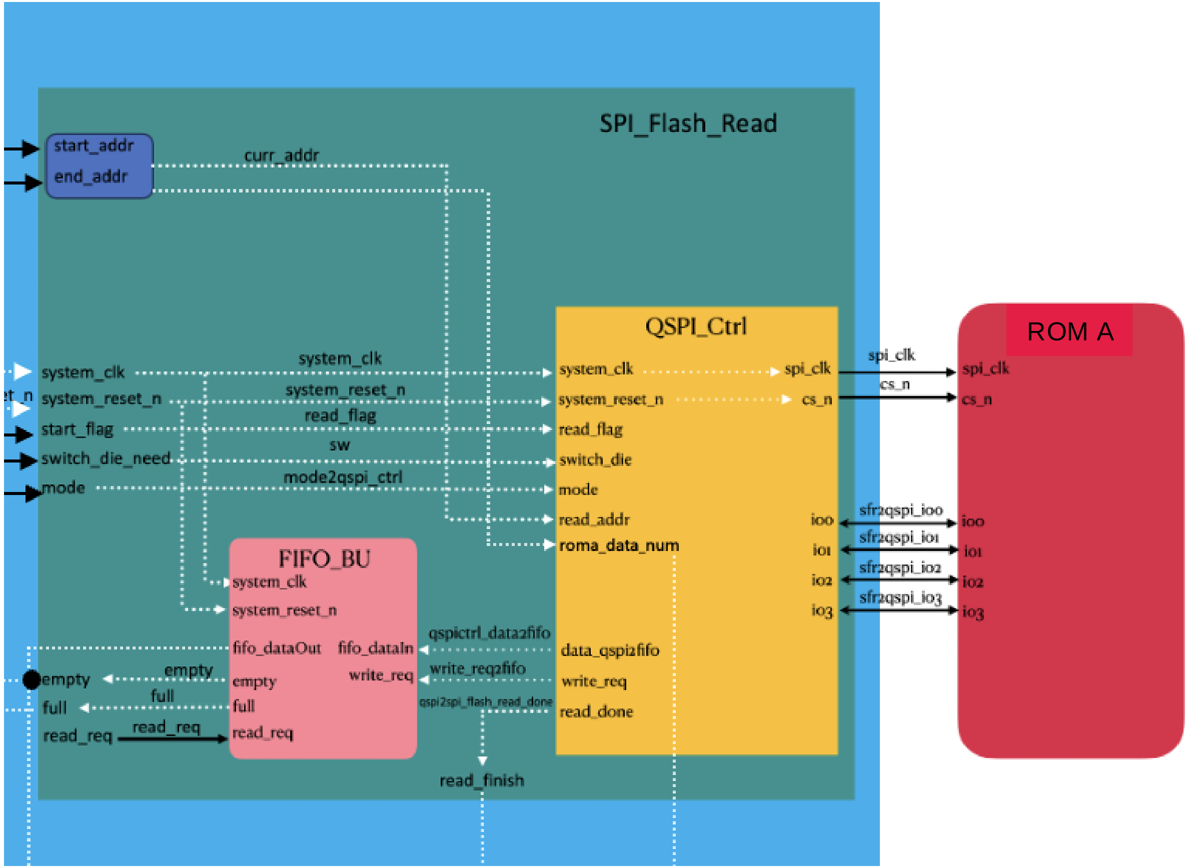
ed on 3-byte address mode. For 4-byte address mode, the

System architecture

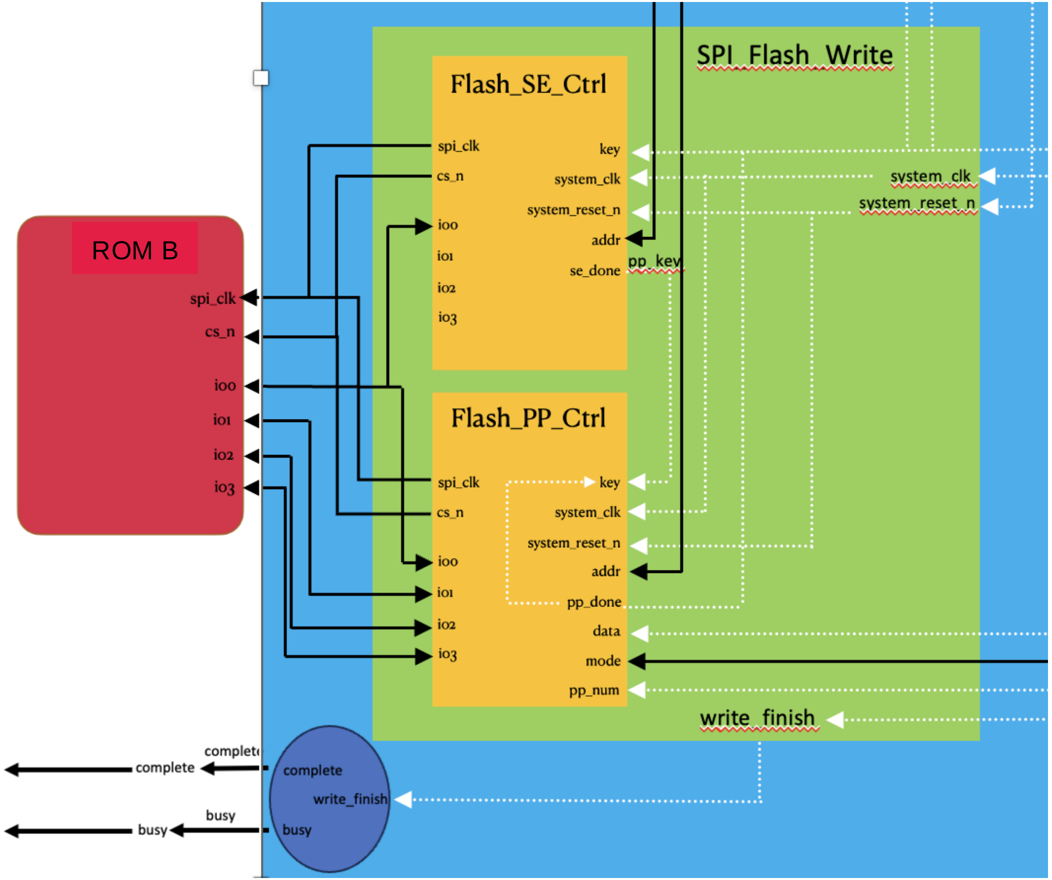
System Architecture



System Architecture

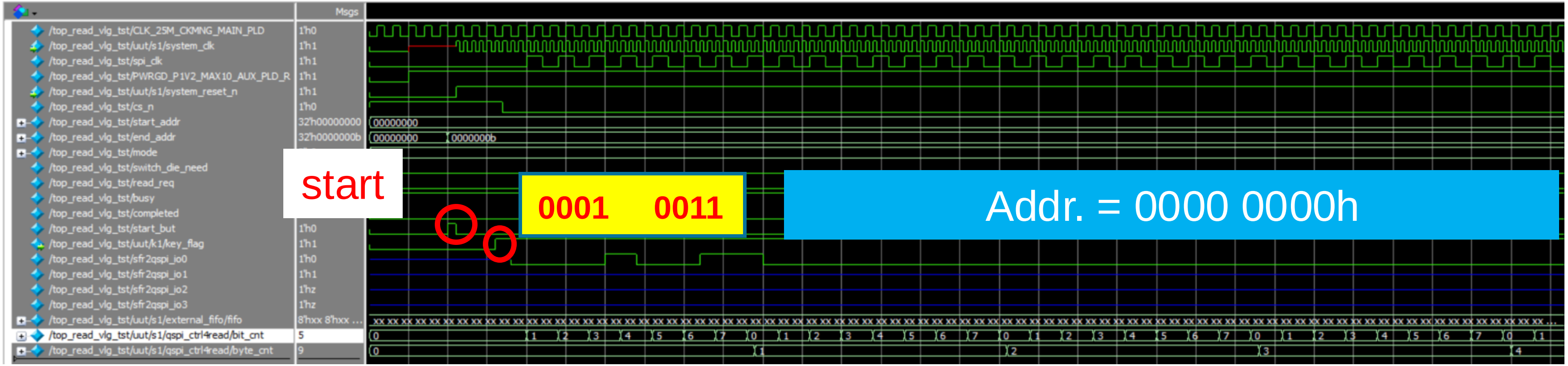


System Architecture



Verification

Simulation(1/4)-Standard read(13h)

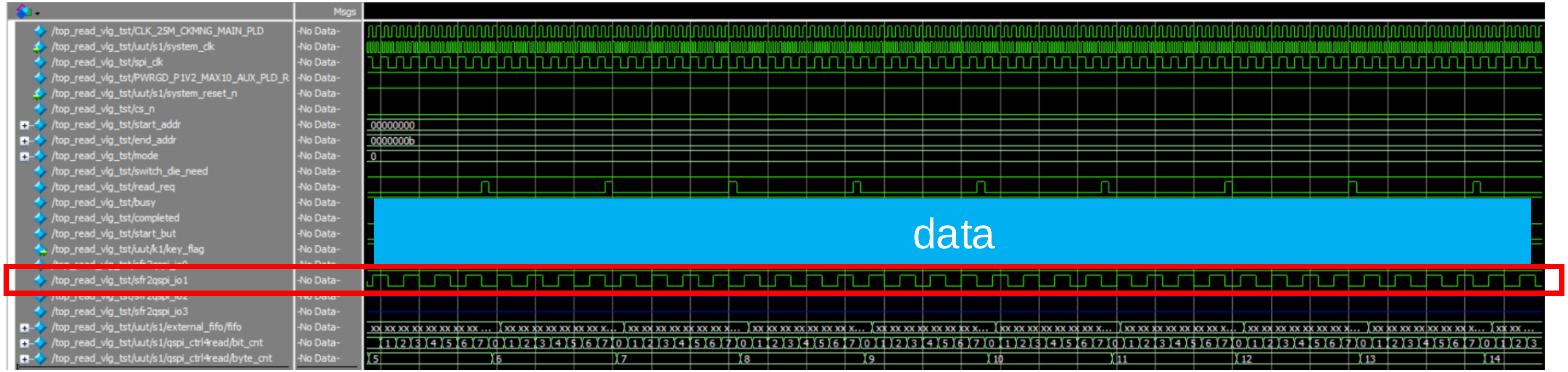


```
                                                   Msgs
/top_read_vlg_tst/CLK_25M_CKMNG_MAIN_PLD           1'h0
/top_read_vlg_tst/uut/s1/system_clk                1'h1
/top_read_vlg_tst/spi_clk                          1'h1
/top_read_vlg_tst/PWRGD_P1V2_MAX10_AUX_PLD_R       1'h1
/top_read_vlg_tst/uut/s1/system_reset_n            1'h1
/top_read_vlg_tst/cs_n                             1'h0
/top_read_vlg_tst/start_addr                       32'h00000000
/top_read_vlg_tst/end_addr                         32'h0000000b
/top_read_vlg_tst/mode
/top_read_vlg_tst/switch_die_need
/top_read_vlg_tst/read_req
/top_read_vlg_tst/busy
/top_read_vlg_tst/completed
/top_read_vlg_tst/start_but                        1'h0
/top_read_vlg_tst/uut/k1/key_flag                  1'h1
/top_read_vlg_tst/sfr2qspi_io0                     1'h0
/top_read_vlg_tst/sfr2qspi_io1                     1'h1
/top_read_vlg_tst/sfr2qspi_io2                     1'hz
/top_read_vlg_tst/sfr2qspi_io3                     1'hz
/top_read_vlg_tst/uut/s1/external_fifo/fifo        8'hxx 8'hxx ...
/top_read_vlg_tst/uut/s1/qspi_ctrl4read/bit_cnt    5
/top_read_vlg_tst/uut/s1/qspi_ctrl4read/byte_cnt   9
```

start

0001 0011

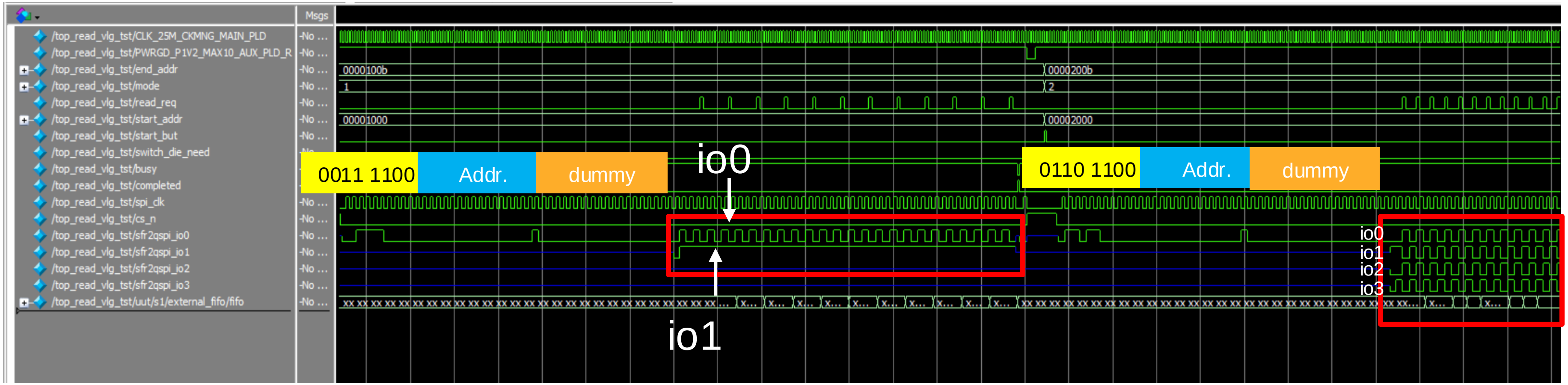
Addr. = 0000 0000h



```
                                                   Msgs
/top_read_vlg_tst/CLK_25M_CKMNG_MAIN_PLD           -No Data-
/top_read_vlg_tst/uut/s1/system_clk                -No Data-
/top_read_vlg_tst/spi_clk                          -No Data-
/top_read_vlg_tst/PWRGD_P1V2_MAX10_AUX_PLD_R       -No Data-
/top_read_vlg_tst/uut/s1/system_reset_n            -No Data-
/top_read_vlg_tst/cs_n                             -No Data-
/top_read_vlg_tst/start_addr                       -No Data-
/top_read_vlg_tst/end_addr                         -No Data-
/top_read_vlg_tst/mode                             -No Data-
/top_read_vlg_tst/switch_die_need                  -No Data-
/top_read_vlg_tst/read_req                         -No Data-
/top_read_vlg_tst/busy                             -No Data-
/top_read_vlg_tst/completed                        -No Data-
/top_read_vlg_tst/start_but                        -No Data-
/top_read_vlg_tst/uut/k1/key_flag                  -No Data-
/top_read_vlg_tst/sfr2qspi_io0                     -No Data-
/top_read_vlg_tst/sfr2qspi_io1                     -No Data-
/top_read_vlg_tst/sfr2qspi_io2                     -No Data-
/top_read_vlg_tst/sfr2qspi_io3                     -No Data-
/top_read_vlg_tst/uut/s1/external_fifo/fifo        -No Data-
/top_read_vlg_tst/uut/s1/qspi_ctrl4read/bit_cnt    -No Data-
/top_read_vlg_tst/uut/s1/qspi_ctrl4read/byte_cnt   -No Data-
```

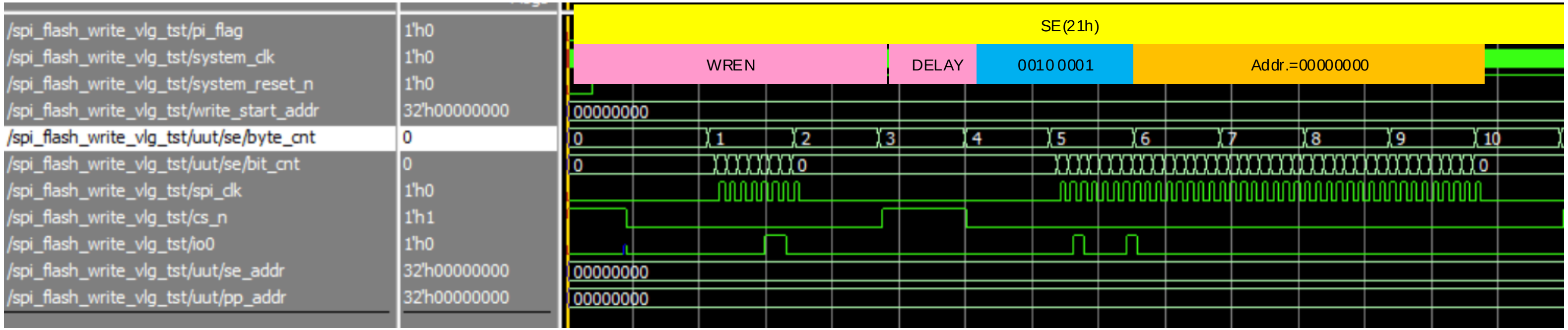
data

Simulation(2/4)-Dual (3Ch)& Quad(6Ch) mode

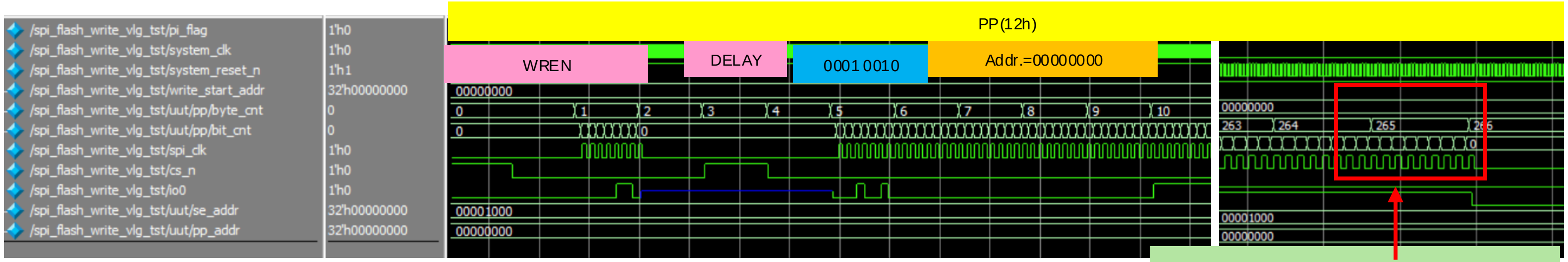


```
Msgs
/top_read_vlg_tst/CLK_25M_CKMNG_MAIN_PLD      -No ...
/top_read_vlg_tst/PWRGD_P1V2_MAX10_AUX_PLD_R  -No ...
/top_read_vlg_tst/end_addr                    -No ...   0000100b   0000200b
/top_read_vlg_tst/mode                        -No ...   1          2
/top_read_vlg_tst/read_req                    -No ...
/top_read_vlg_tst/start_addr                  -No ...   00001000   00002000
/top_read_vlg_tst/start_but                   -No ...
/top_read_vlg_tst/switch_die_need             -No ...
/top_read_vlg_tst/busy
/top_read_vlg_tst/completed
/top_read_vlg_tst/spi_clk                     -No ...
/top_read_vlg_tst/cs_n                        -No ...
/top_read_vlg_tst/sfr2qspi_io0                -No ...
/top_read_vlg_tst/sfr2qspi_io1                -No ...
/top_read_vlg_tst/sfr2qspi_io2                -No ...
/top_read_vlg_tst/sfr2qspi_io3                -No ...
/top_read_vlg_tst/uut/s1/external_fifo/fifo   -No ...
```

Simulation(3/4)-Standard write



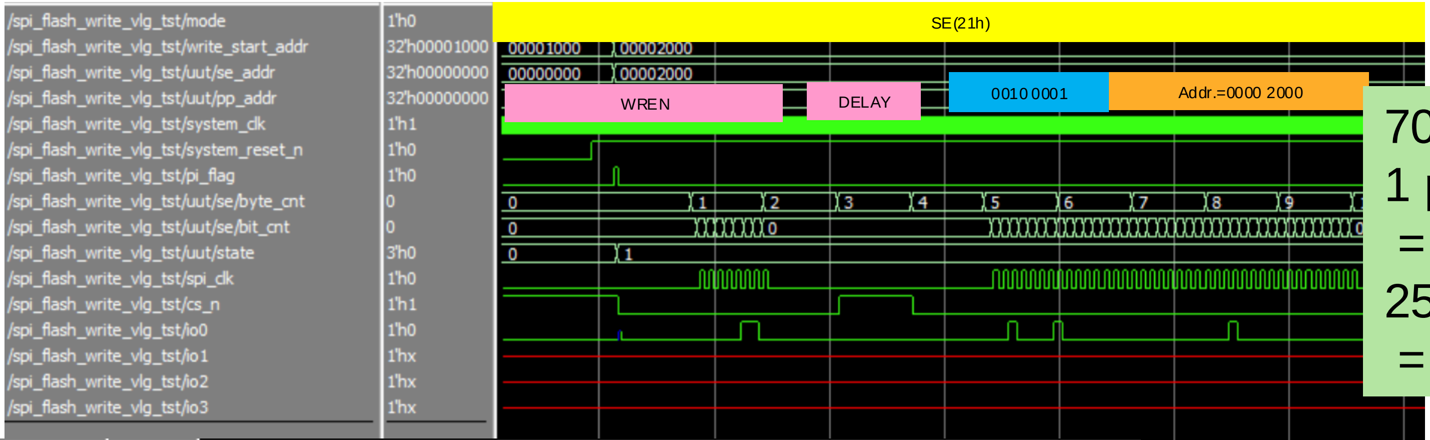
Signal	Value
/spi_flash_write_vlg_tst/pi_flag	1'h0
/spi_flash_write_vlg_tst/system_clk	1'h0
/spi_flash_write_vlg_tst/system_reset_n	1'h0
/spi_flash_write_vlg_tst/write_start_addr	32'h00000000
/spi_flash_write_vlg_tst/uut/se/byte_cnt	0
/spi_flash_write_vlg_tst/uut/se/bit_cnt	0
/spi_flash_write_vlg_tst/spi_clk	1'h0
/spi_flash_write_vlg_tst/cs_n	1'h1
/spi_flash_write_vlg_tst/io0	1'h0
/spi_flash_write_vlg_tst/uut/se_addr	32'h00000000
/spi_flash_write_vlg_tst/uut/pp_addr	32'h00000000



Signal	Value
/spi_flash_write_vlg_tst/pi_flag	1'h0
/spi_flash_write_vlg_tst/system_clk	1'h0
/spi_flash_write_vlg_tst/system_reset_n	1'h1
/spi_flash_write_vlg_tst/write_start_addr	32'h00000000
/spi_flash_write_vlg_tst/uut/pp/byte_cnt	0
/spi_flash_write_vlg_tst/uut/pp/bit_cnt	0
/spi_flash_write_vlg_tst/spi_clk	1'h0
/spi_flash_write_vlg_tst/cs_n	1'h0
/spi_flash_write_vlg_tst/io0	1'h0
/spi_flash_write_vlg_tst/uut/se_addr	32'h00000000
/spi_flash_write_vlg_tst/uut/pp_addr	32'h00000000

265-10=255byte
1 page = 256byte

Simulation(4/4) – Quad write



```
/spi_flash_write_vlg_tst/mode                 1'h0
/spi_flash_write_vlg_tst/write_start_addr     32'h00001000
/spi_flash_write_vlg_tst/uut/se_addr          32'h00000000
/spi_flash_write_vlg_tst/uut/pp_addr          32'h00000000
/spi_flash_write_vlg_tst/system_clk           1'h1
/spi_flash_write_vlg_tst/system_reset_n       1'h0
/spi_flash_write_vlg_tst/pi_flag              1'h0
/spi_flash_write_vlg_tst/uut/se/byte_cnt      0
/spi_flash_write_vlg_tst/uut/se/bit_cnt       0
/spi_flash_write_vlg_tst/uut/state            3'h0
/spi_flash_write_vlg_tst/spi_clk              1'h0
/spi_flash_write_vlg_tst/cs_n                 1'h1
/spi_flash_write_vlg_tst/io0                  1'h0
/spi_flash_write_vlg_tst/io1                  1'hx
/spi_flash_write_vlg_tst/io2                  1'hx
/spi_flash_write_vlg_tst/io3                  1'hx
```

SE(21h)

WREN

DELAY

0010 0001

Addr.=0000 2000

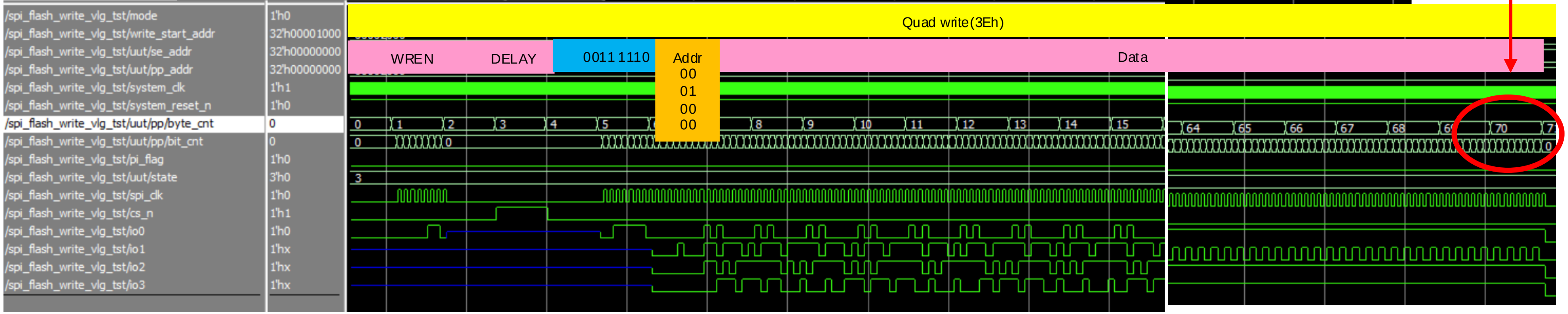
70-7=63byte

1 page

= 256byte

256/4

= 64 byte



```
/spi_flash_write_vlg_tst/mode                 1'h0
/spi_flash_write_vlg_tst/write_start_addr     32'h00001000
/spi_flash_write_vlg_tst/uut/se_addr          32'h00000000
/spi_flash_write_vlg_tst/uut/pp_addr          32'h00000000
/spi_flash_write_vlg_tst/system_clk           1'h1
/spi_flash_write_vlg_tst/system_reset_n       1'h0
/spi_flash_write_vlg_tst/uut/pp/byte_cnt      0
/spi_flash_write_vlg_tst/uut/pp/bit_cnt       0
/spi_flash_write_vlg_tst/pi_flag              1'h0
/spi_flash_write_vlg_tst/uut/state            3'h0
/spi_flash_write_vlg_tst/spi_clk              1'h0
/spi_flash_write_vlg_tst/cs_n                 1'h1
/spi_flash_write_vlg_tst/io0                  1'h0
/spi_flash_write_vlg_tst/io1                  1'hx
/spi_flash_write_vlg_tst/io2                  1'hx
/spi_flash_write_vlg_tst/io3                  1'hx
```

Quad write(3Eh)

WREN

DELAY

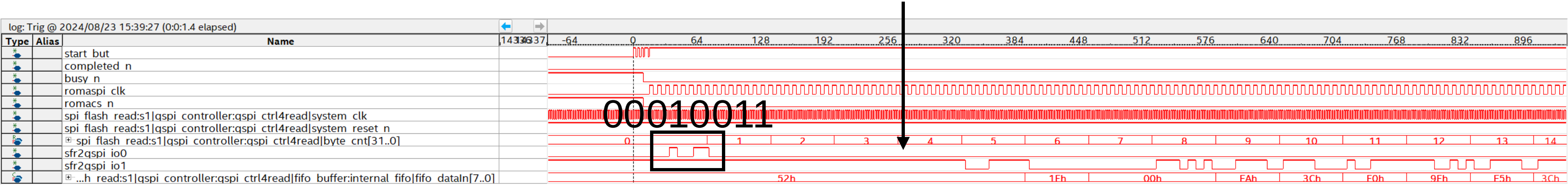
0011 1110

Addr
00
01
00
00

Data

Board Level(1/2)-read

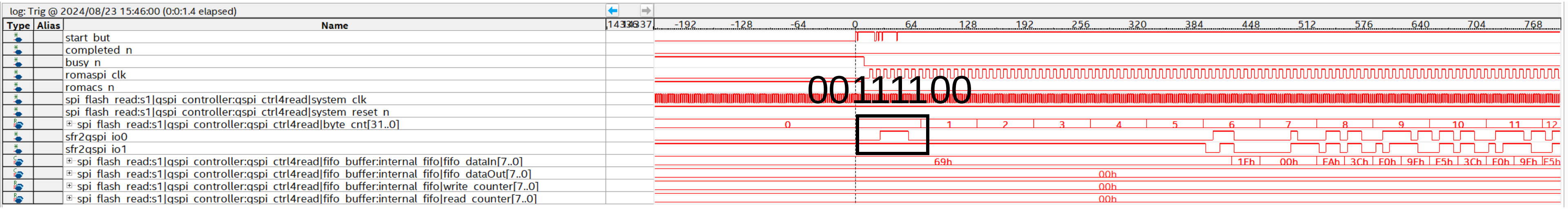
Addr.=00000000



log: Trig @ 2024/08/23 15:39:27 (0:0:1.4 elapsed)

```
Type Alias Name
start_but
completed_n
busy_n
romaspi_clk
romacs_n
spi_flash_read:s1|qspi_controller:qspi_ctrl4read|system_clk
spi_flash_read:s1|qspi_controller:qspi_ctrl4read|system_reset_n
⊞ spi_flash_read:s1|qspi_controller:qspi_ctrl4read|byte_cnt[31..0]
sfr2qspi_io0
sfr2qspi_io1
⊞ ...h_read:s1|qspi_controller:qspi_ctrl4read|fifo_buffer:internal_fifo|fifo_dataIn[7..0]
```

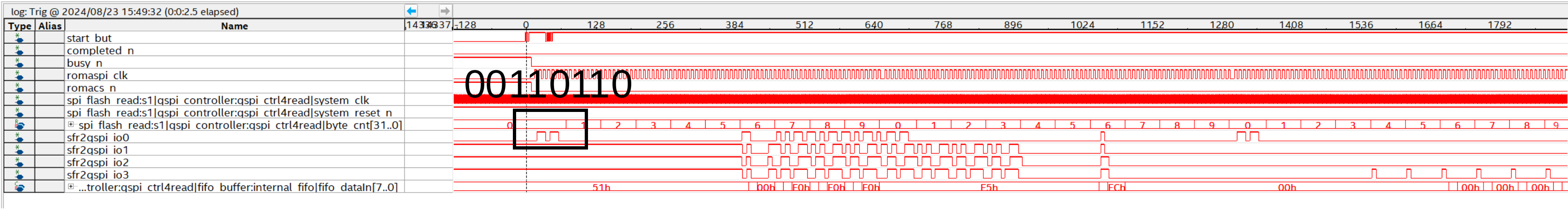
00010011



log: Trig @ 2024/08/23 15:46:00 (0:0:1.4 elapsed)

```
Type Alias Name
start_but
completed_n
busy_n
romaspi_clk
romacs_n
spi_flash_read:s1|qspi_controller:qspi_ctrl4read|system_clk
spi_flash_read:s1|qspi_controller:qspi_ctrl4read|system_reset_n
⊞ spi_flash_read:s1|qspi_controller:qspi_ctrl4read|byte_cnt[31..0]
sfr2qspi_io0
sfr2qspi_io1
⊞ spi_flash_read:s1|qspi_controller:qspi_ctrl4read|fifo_buffer:internal_fifo|fifo_dataIn[7..0]
⊞ spi_flash_read:s1|qspi_controller:qspi_ctrl4read|fifo_buffer:internal_fifo|fifo_dataOut[7..0]
⊞ spi_flash_read:s1|qspi_controller:qspi_ctrl4read|fifo_buffer:internal_fifo|write_counter[7..0]
⊞ spi_flash_read:s1|qspi_controller:qspi_ctrl4read|fifo_buffer:internal_fifo|read_counter[7..0]
```

00111100



log: Trig @ 2024/08/23 15:49:32 (0:0:2.5 elapsed)

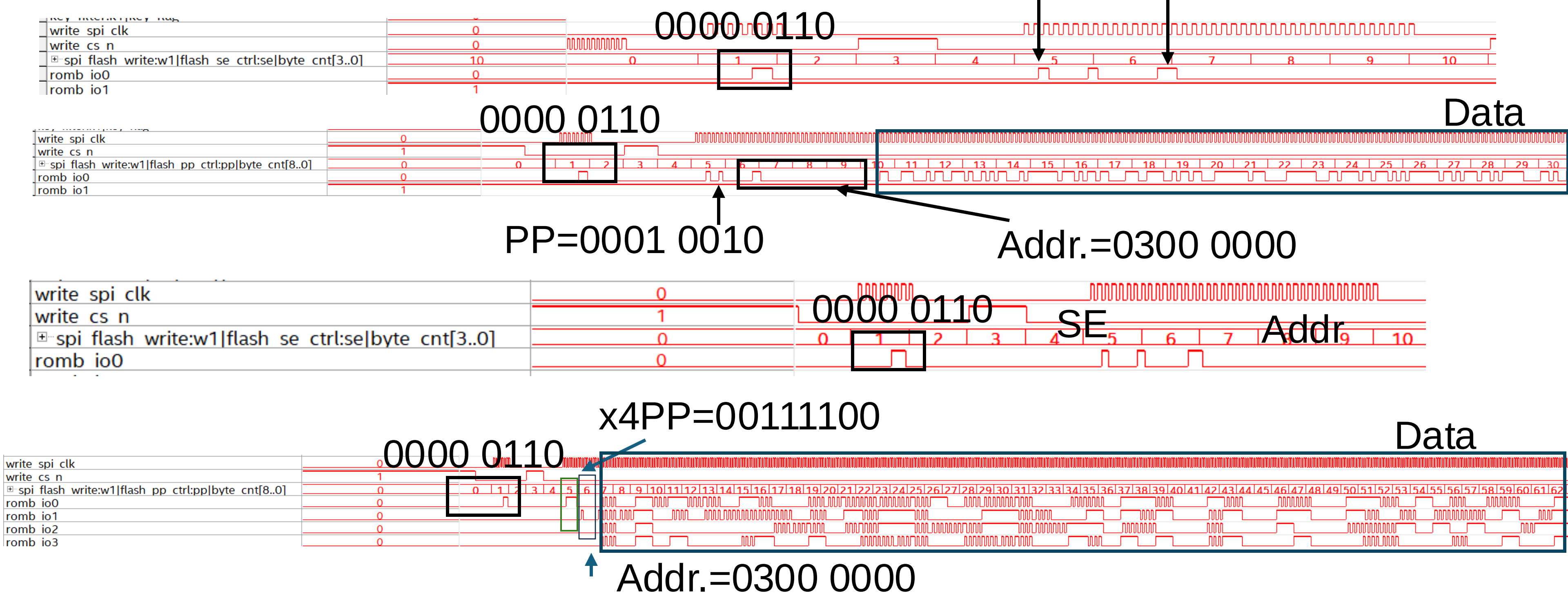
```
Type Alias Name
start_but
completed_n
busy_n
romaspi_clk
romacs_n
spi_flash_read:s1|qspi_controller:qspi_ctrl4read|system_clk
spi_flash_read:s1|qspi_controller:qspi_ctrl4read|system_reset_n
⊞ spi_flash_read:s1|qspi_controller:qspi_ctrl4read|byte_cnt[31..0]
sfr2qspi_io0
sfr2qspi_io1
sfr2qspi_io2
sfr2qspi_io3
⊞ ...troller:qspi_ctrl4read|fifo_buffer:internal_fifo|fifo_dataIn[7..0]
```

00110110

Board Level(2/2)-write

SE=0010 0001

Addr.=0300 0000



Conclusion

Future work

- Parallel Read and Write operations.

- CRC Verification

Conclusion

- Learned about SPI protocol and how to implement read and write control.

- Completed the entire process from reading the datasheet to design, simulation, board verification and testing.

Thank You!