ET5302701

Homework Assignment # 1

Date: September 13, 2024. **Instructor: M. B. Lin**

Due Date: October 11, 2024.

Homework is due at the beginning of class. Please note that **NO late homework** will be accepted. Working together on homework is encouraged, but copying assignments will not be allowed.

1. Consider the following switching function:

$$f(x,y,z) = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

   (a) Realize the above switching function using a 0/1-x/$\bar{x}$-tree network with nMOS switches, assuming that the output voltage need not be full-ranged.

   (b) Realize the above switching function with a 0/1-tree network in which f_Y^0 is implemented with nMOS switches and f_Y^1 is implemented with pMOS switches. Your answer must be derived by using Shannon's expansion theorem analytically.

2. (Physical layout of an Inverter)

   (a) Draw the transistor-level (i.e., circuit) schematic of an inverter.

   (b) Use HSPICE to verify the functionality of the inverter. What is the maximum propagation delay?

   (c) Plot a stick diagram of the inverter.

   (d) Draw the physical layout of the inverter.

   (e) Use HSPICE to verify the functionality of the resulting physical layout and estimate the maximum propagation delay. Compare the result with (b).

3. Considering a full adder, answer each of the following questions:

   (a) Derive the truth table of a full adder and find its minimal output expressions.

   (b) Draw a transistor-level schematic of each minimal output expression. How many transistors are required in the schematic?

   (c) Use HSPICE to verify the functionality of the full adder. What is the maximum propagation delay?

   (d) Plot a stick diagram of the full adder.

   (e) Draw the physical layout of the full-adder.

   (f) Use HSPICE to verify the functionality of the resulting physical layout and estimate the maximum propagation delay. Compare the result with (c).