ET5302701

Homework Assignment # 2

Date: October 11, 2024. **Instructor: M. B. Lin**

Due Date: November 1, 2024.

Homework is due **at the class beginning.** Please note that **NO late homework** will be accepted. Working together on homework is encouraged, but copying assignments will not be allowed.

1. Consider the switching function of XOR gate: $f(x,y) = \bar{x}y + x\bar{y}$.
   (a) Prove that $f(x,y) = \overline{\overline{x+y} + xy}$.
   (b) Realize it using a CMOS logic circuit. Your design must be limited to use 10 transistors at most.
   (c) Use HSPICE to verify the functionality of the resulting circuit. What is the maximum propagation delay of the resulting circuit?
   (d) Draw the pMOS and nMOS logic graphs and find the Euler paths.
   (e) Design and carry out a physical layout.
   (f) Use HSPICE to verify the functionality and estimate the maximum propagation delay of the resulting physical layout.
2. Consider the switching function of the XNOR gate: $f(x,y) = xy + \bar{x}\bar{y}$.
   (a) Prove that $f(x,y) = \overline{\overline{xy} \cdot (x+y)}$.
   (b) Realize it using a CMOS logic circuit. Your design must be limited to use 10 transistors at most.
   (c) Use HSPICE to verify the functionality of the resulting circuit. What is the maximum propagation delay of the resulting circuit?
   (d) Draw the pMOS and nMOS logic graphs and find the Euler paths.
   (e) Design and construct a physical layout.
   (f) Use HSPICE to verify the functionality and estimate the maximum propagation delay of the resulting physical layout.