M11215075 資工碩二 胡劭

1. Consider the following switching function:

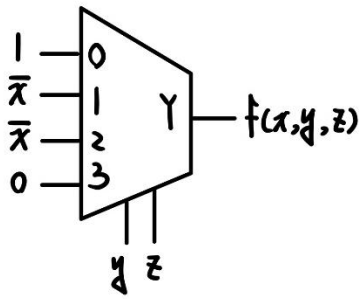
$$f(x,y,z) = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

(a) Realize the above switching function using a 0/1-$x/\bar{x}$-tree network with nMOS switches, assuming that the output voltage need not be full-ranged.

Ans.:

$$f(x,y,z) = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$
$$= \bar{y}(\bar{x} + \bar{x}\bar{z} + \bar{z}) + y(\bar{x}\bar{z})$$
$$= \bar{y}(\bar{x} + \bar{z}) + y(\bar{x}\bar{z})$$
$$= \bar{y}\left[\bar{x}(1+\bar{z}) + x\bar{z}\right] + y\left[\bar{x}\bar{z} + x(0)\right]$$
$$= \bar{y}(\bar{x} + x\bar{z}) + \bar{x}y\bar{z}$$

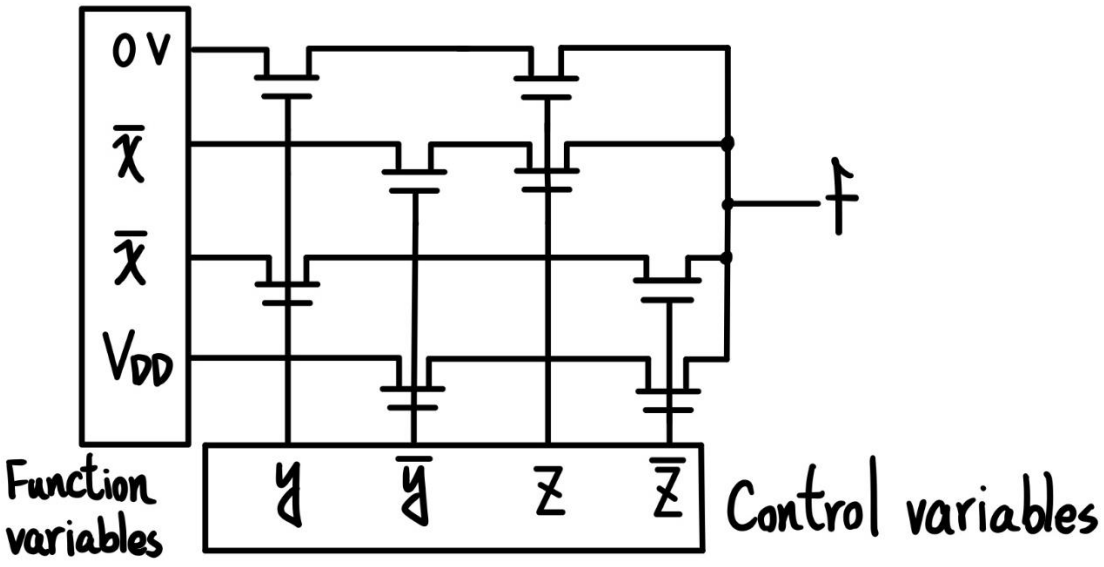
x \ yz	00	01	10	11
0	⓪	①	②	3
1	④	5	6	7
	↑ 1	↑ $\bar{x}$	↑ $\bar{x}$	↑ 0



$f_Y^0 = yz$

$f_Y^1 = \bar{y}\bar{z}$

$f_Y^{\bar{x}} = \bar{y}z + y\bar{z}$



(b) Realize the above switching function with a 0/1-tree network in which f_Y^0 is implemented with nMOS switches and f_Y^1 is implemented with pMOS switches. Your answer must be derived by using Shannon's expansion theorem analytically.

Ans.:

$$f(x,y,z) = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}$$

$$= \overline{x+y} + \overline{x+z} + \overline{y+z}$$

$$= \bar{x}(\bar{y}) + x(0) + \bar{x}(\bar{z}) + x(0) + \bar{y}(\bar{z}) + y(0)$$

$$= \bar{x}(\bar{y}\cdot 1 + y\cdot 0) + x(\bar{y}\cdot 0 + y\cdot 0) + \bar{x}(\bar{z}\cdot 1 + z\cdot 0) + x(\bar{z}\cdot 0 + z\cdot 0) + \bar{y}(\bar{z}\cdot 1 + z\cdot 0) + y(\bar{z}\cdot 0 + z\cdot 0)$$

$$= \bar{x}\bar{y}\cdot 1 + \bar{x}y\cdot 0 + x\bar{y}\cdot 0 + xy\cdot 0 + \bar{x}\bar{z}\cdot 1 + \bar{x}z\cdot 0 + x\bar{z}\cdot 0 + xz\cdot 0 + \bar{y}\bar{z}\cdot 1 + \bar{y}z\cdot 0 + y\bar{z}\cdot 0 + yz\cdot 0$$

$$\Rightarrow f_Y^1 = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z} = f(x,y,z)$$

$$f_Y^0 = \bar{x}y + x\bar{y} + xy + \bar{x}\bar{z} + x\bar{z} + xz + \bar{y}z + y\bar{z} + yz$$

$$= \bar{x}y + x(\bar{y}+y) + \bar{x}\bar{z} + x(\bar{z}+z) + \bar{y}z + y(\bar{z}+z)$$

$$= \bar{x}y + x(1) + \bar{x}\bar{z} + x(1) + \bar{y}z + y(1)$$

$$= (x+y) + (x+z) + (y+z)$$

$$f(x,y,z) = \bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z} = f_Y^1 \quad \text{(OR)}$$

$$g = \bar{f} = \overline{\bar{x}\bar{y} + \bar{x}\bar{z} + \bar{y}\bar{z}} \quad \text{(AND)}$$

$$= \overline{\overline{\bar{x}+y} + \overline{x+z} + \overline{y+z}}$$

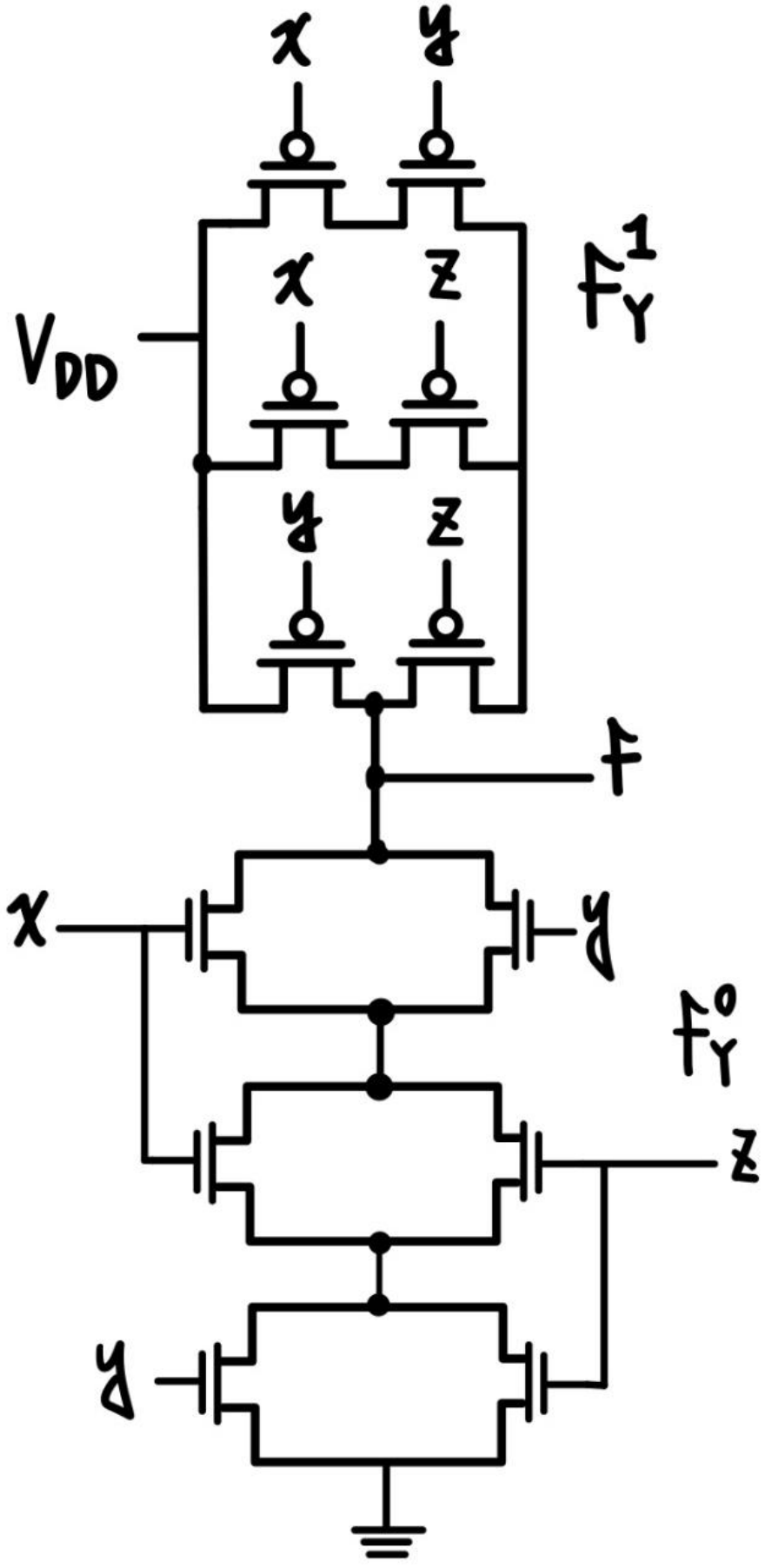
$$= \overline{\overline{(x+y)(x+z)(y+z)}}$$

$$= (x+y)(x+z)(y+z) = f_Y^0$$

x \ yz	00	01	11	10
0	1	1	0	1
1	1	0	0	0

$f_Y^0(x,y,z)$

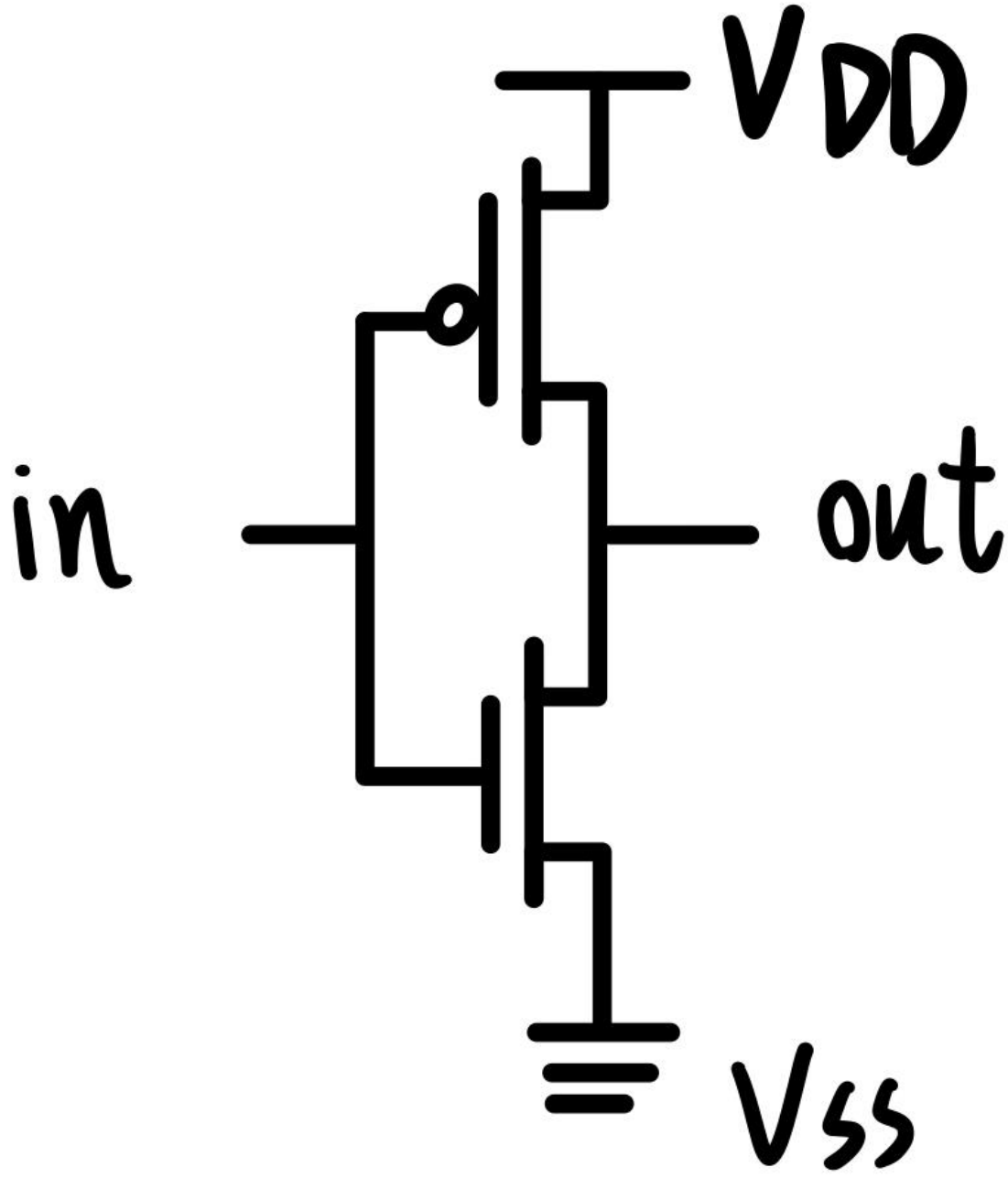
$f_Y^1(x,y,z)$


x
y
x
z
V_{DD}
f_Y^1
y
z
f
x
y
f_Y^0
z
y

2. (Physical layout of an Inverter)

(a) Draw the transistor-level (i.e., circuit) schematic of an inverter.

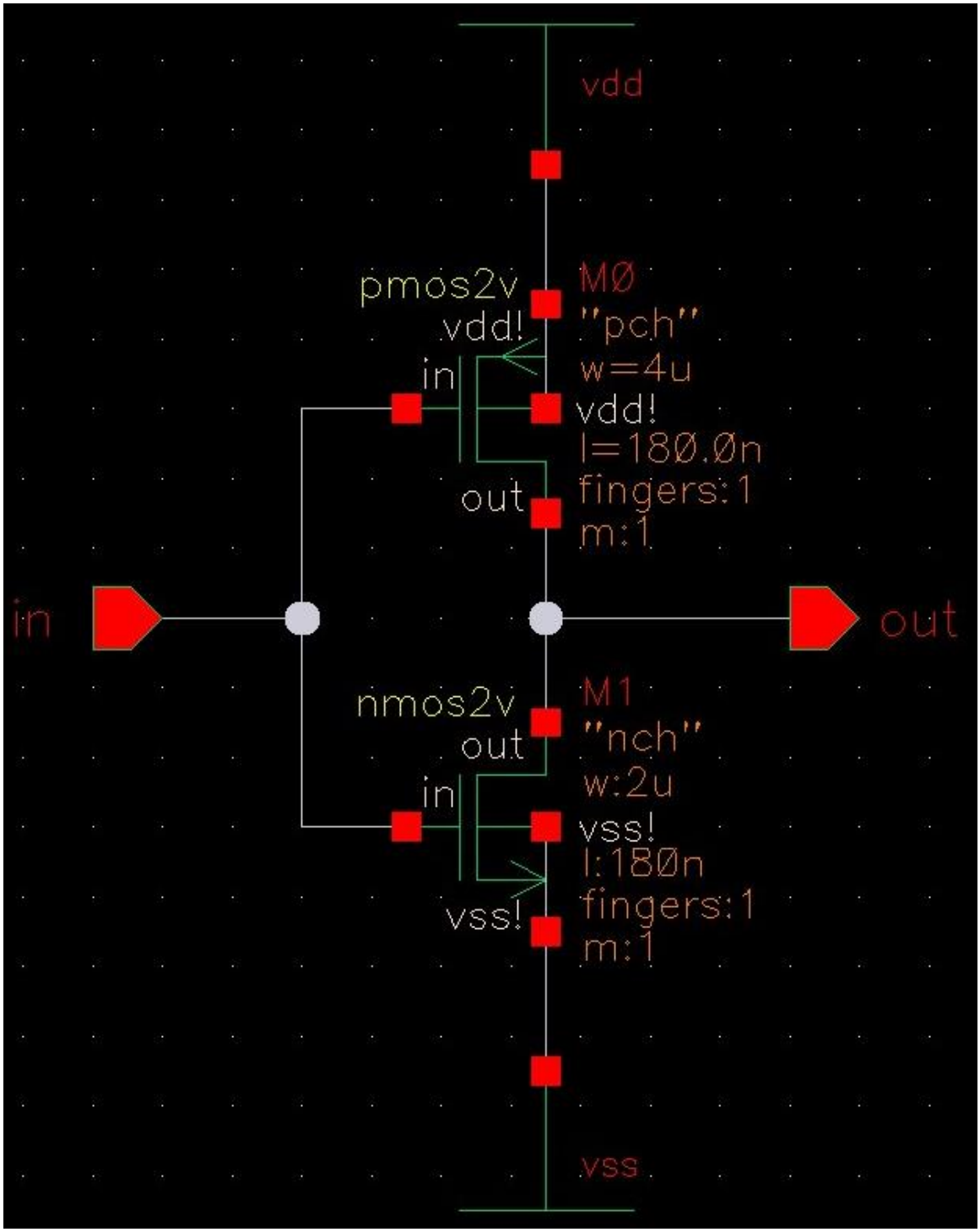
Ans.:

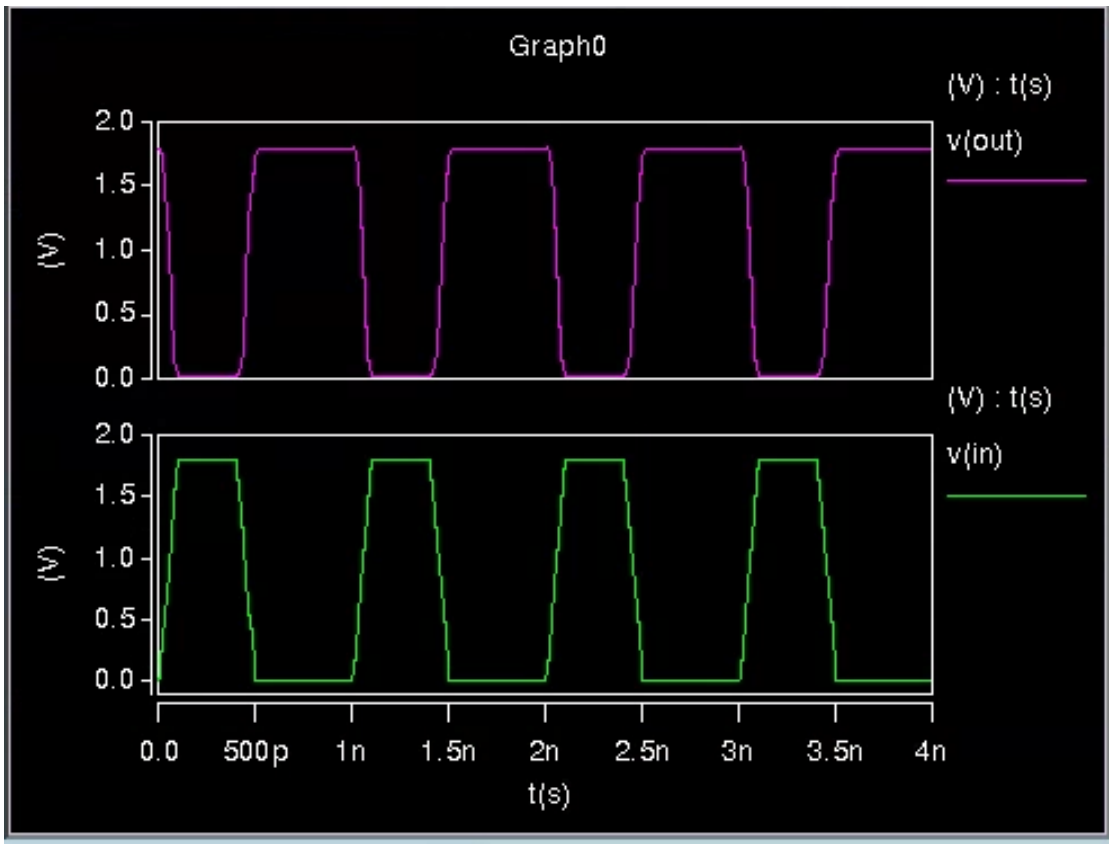


使用 Virtuoso Schematic 的 Circuit 跟 HSPICE(B)放在一起

(b) Use HSPICE to verify the functionality of the inverter. What is the maximum propagation delay?

Ans.:

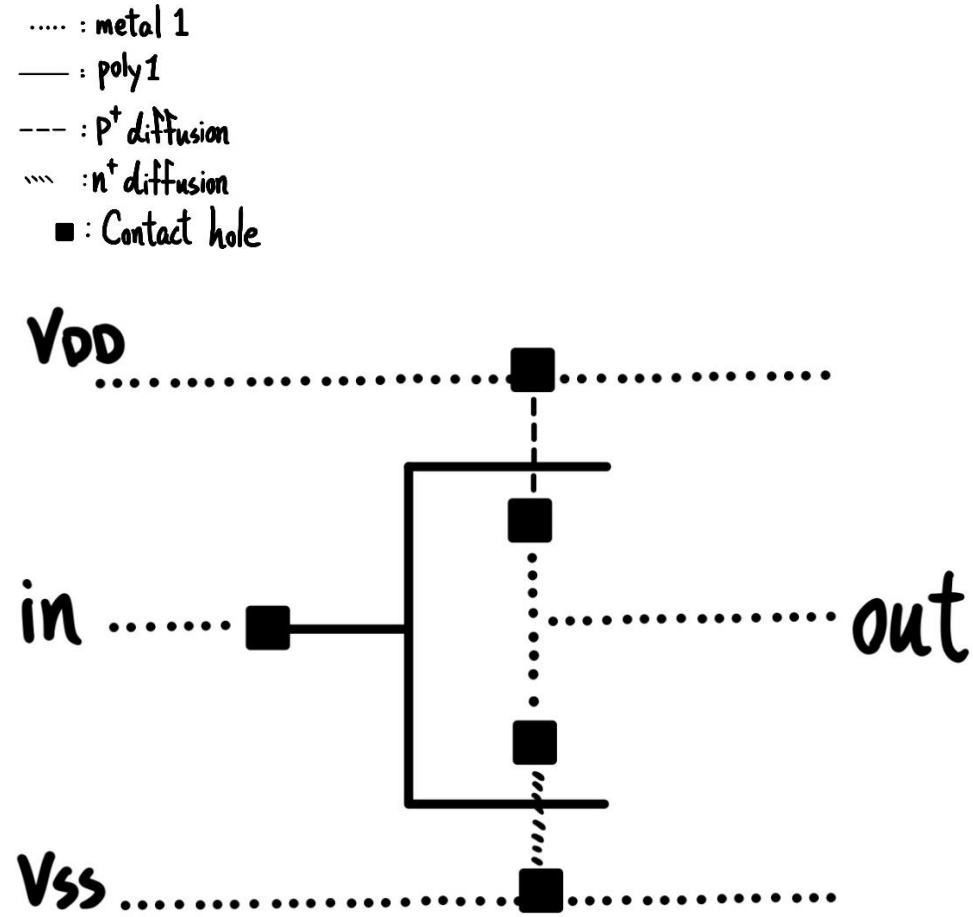




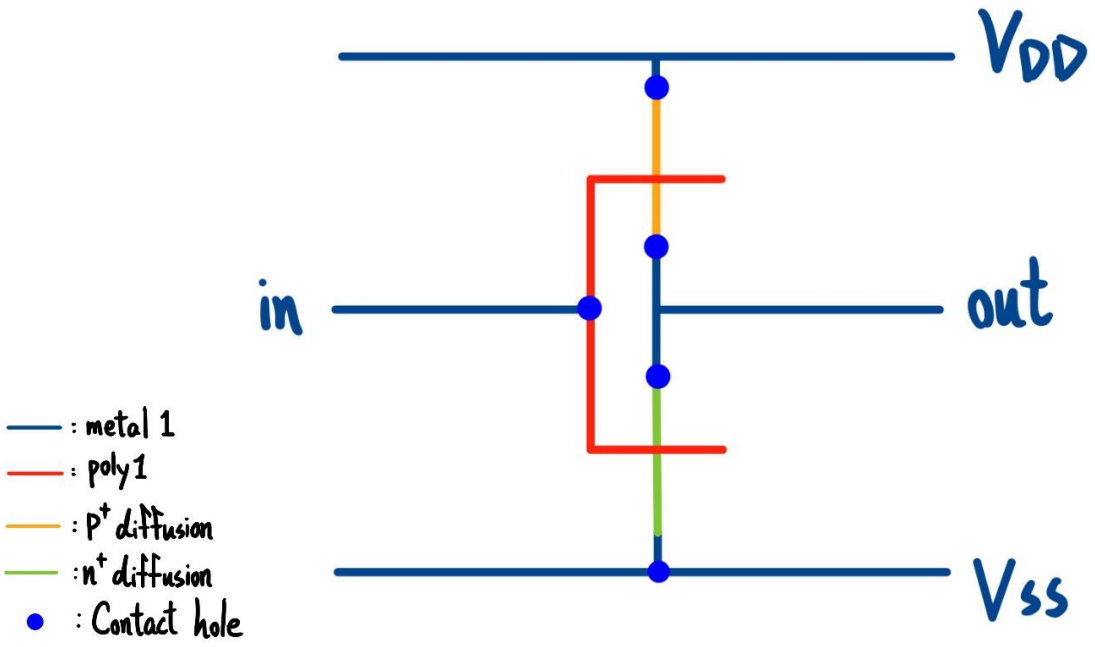

```
  ******  Measured values for the netlist  **********
tplh=  7.3563e-12    targ=  1.4574n trig=  1.4500n
tphl=  6.0684e-12    targ=  1.0561n trig=  1.0500n
tpd=  6.7123e-12     6.712e-12


 ***************************

Resource Usage for Transient Analysis
CPU Time     0.01 sec
Peak Memory  698.01 Mb

Wall Time Statistics:
  Transient Wall time                   = 0.0091
  Transient Wall time per timestep      = 5.9856e-05
  Transient Wall time per timestep-node = 8.5508e-06
  Total CPU time                        = 0.0100
  Total CPU time per step               = 6.5789e-05
```

(c) Plot a stick diagram of the inverter.

Ans.:

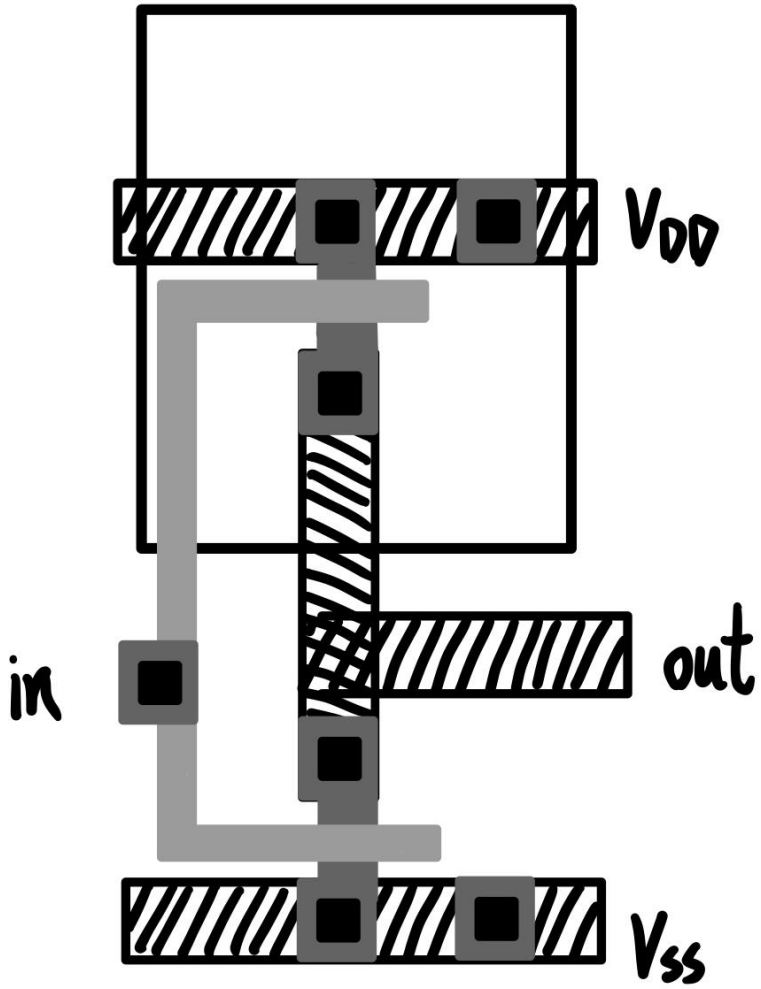


另一種版本:

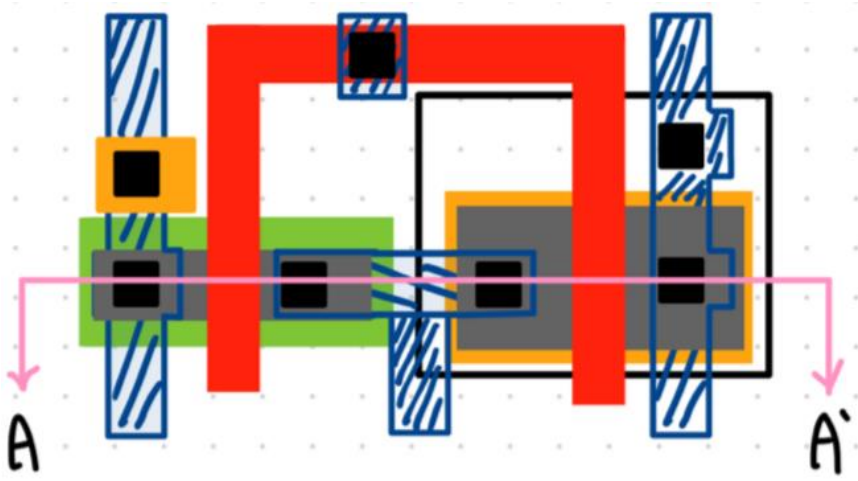


(d) Draw the physical layout of the inverter.

Ans.:



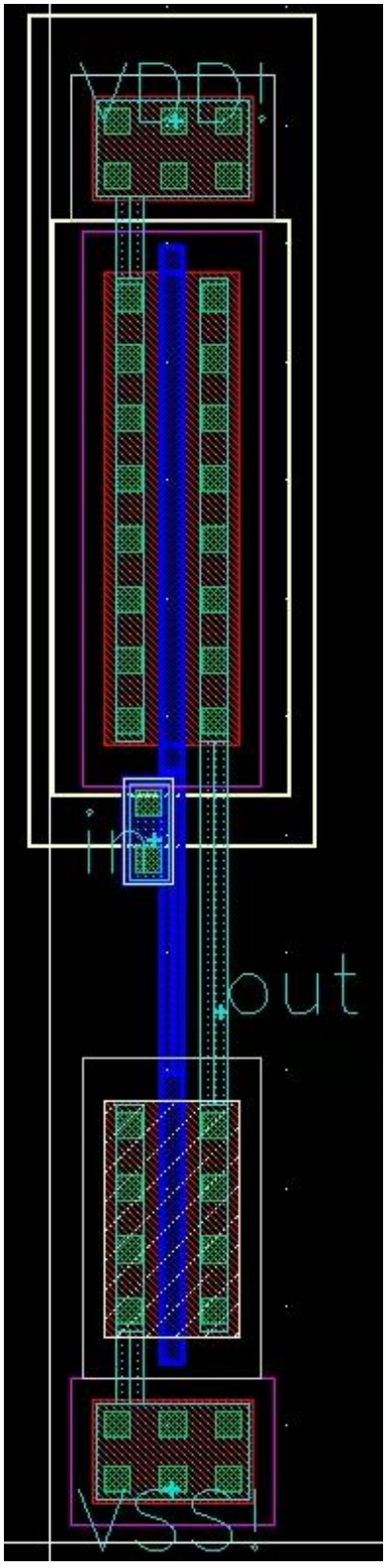
另一種版本:



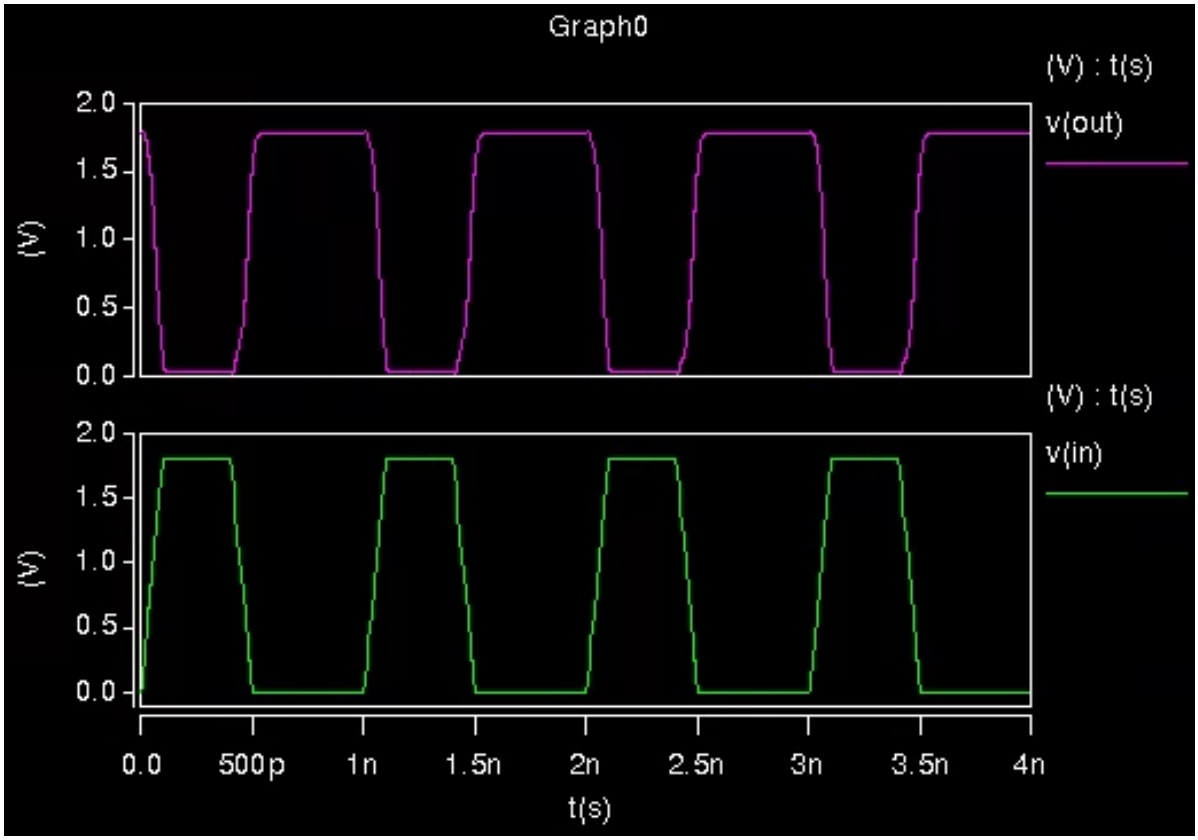
使用 Virtuoso Layouyt 的圖跟 HSPICE 以及 DRC LVS PEX 放在一起(e)

(e) Use HSPICE to verify the functionality of the resulting physical layout and estimate the maximum propagation delay. Compare the result with (b).

Ans.:




```
REPORT FILE NAME:          inv.lvs.report
LAYOUT NAME:               /home/vlsi24f/m11215075/Desktop/cic018/inv.sp ('inv')
SOURCE NAME:               /home/vlsi24f/m11215075/Desktop/cic018/spfile/inv.sp.bak ('inv')
RULE FILE:                 /home/vlsi24f/m11215075/Desktop/cic018/_Calibre.lvs_
CREATION TIME:             Mon Sep 23 01:16:47 2024
CURRENT DIRECTORY:         /home/vlsi24f/m11215075/Desktop/cic018
USER NAME:                 m11215075
CALIBRE VERSION:           v2021.1_33.19    Mon Mar 1 16:10:01 PST 2021


                    OVERALL COMPARISON RESULTS

                        #      ##################
                      #        #                #      ∓   ∓
                    #   #      #    CORRECT     #       |
                     # #       #                #      \___/
                      #        ##################
```




```
  ******  Measured values for the netlist  **********
 tplh=  2.5220e-11    targ=  1.4752n trig=  1.4500n
 tphl=  1.8437e-11    targ=  1.0684n trig=  1.0500n
 tpd=  2.1828e-11     2.183e-11


 ***************************

Resource Usage for Transient Analysis
CPU Time     0.04 sec
Peak Memory  707.28 Mb

Wall Time Statistics:
  Transient Wall time                    = 0.0300
  Transient Wall time per timestep       = 0.0002
  Transient Wall time per timestep-node = 4.1372e-06
  Total CPU time                        = 0.0400
  Total CPU time per step               = 0.0002
```

3. Considering a full adder, answer each of the following questions:

(a) Derive the truth table of a full adder and find its minimal output expressions.

Ans.:

令 Input : x, y, C_{in}

Output : C_{out}, S

#1 Truth Table

x	y	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

#2

$$S = x\bar{y}\overline{C_{in}} + \bar{x}\bar{y}C_{in} + \bar{x}y\overline{C_{in}} + xyC_{in}$$

$$= \overline{C_{in}}(x\bar{y} + \bar{x}y) + C_{in}(\bar{x}\bar{y} + xy)$$

$$= \overline{C_{in}}(x \oplus y) + C_{in}\overline{(x \oplus y)}$$

$$= C_{in} \oplus (x \oplus y)$$

$$= C_{in} \oplus x \oplus y$$

$$C_{out} = \bar{x}yC_{in} + x\bar{y}C_{in} + xy\overline{C_{in}} + xyC_{in}$$

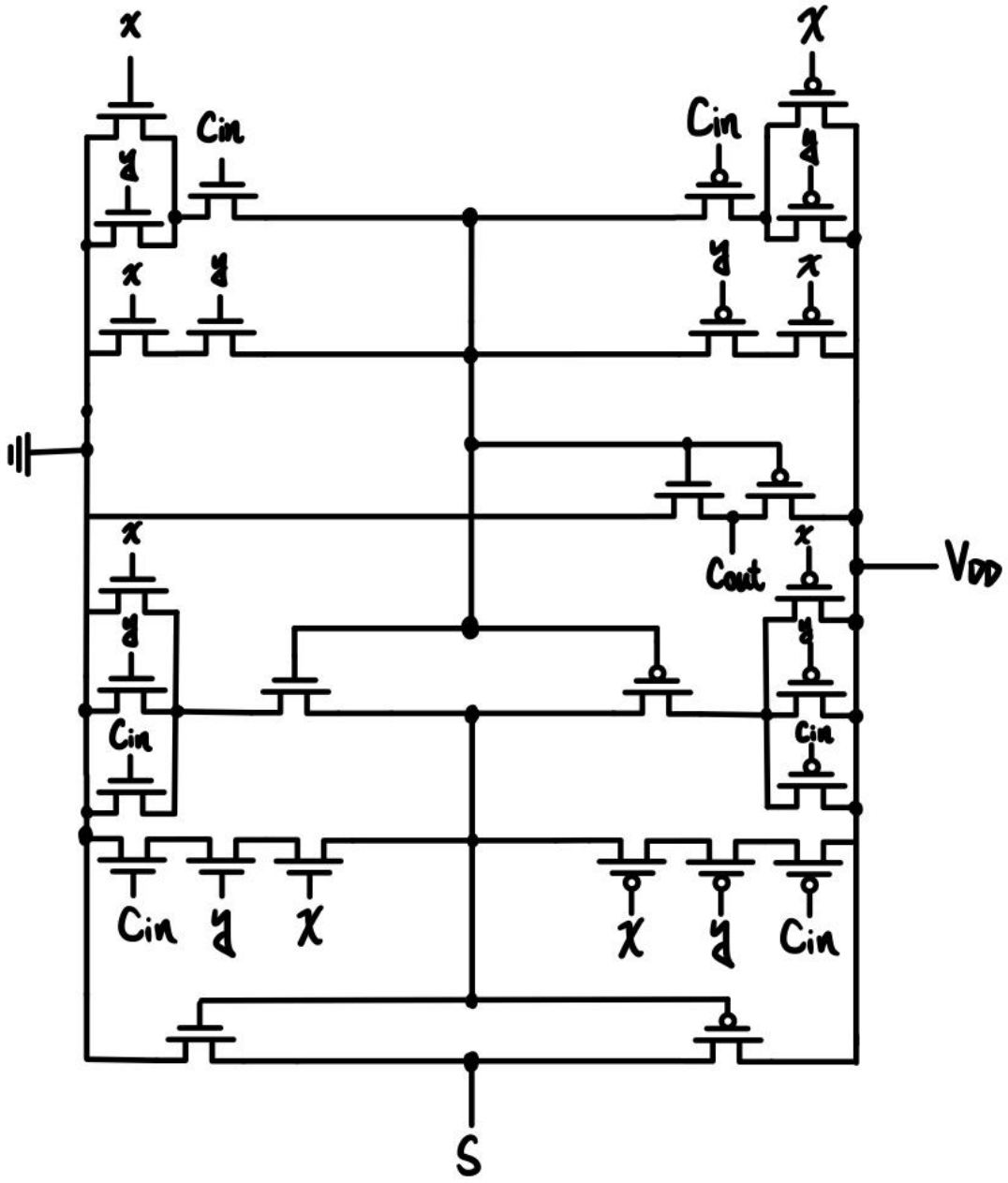
$$= C_{in}(\bar{x}y + x\bar{y}) + xy(\overline{C_{in}} + C_{in})$$

$$= C_{in}(x \oplus y) + xy$$

#

(b) Draw a transistor-level schematic of each minimal output expression. How many transistors are required in the schematic?

Ans.:

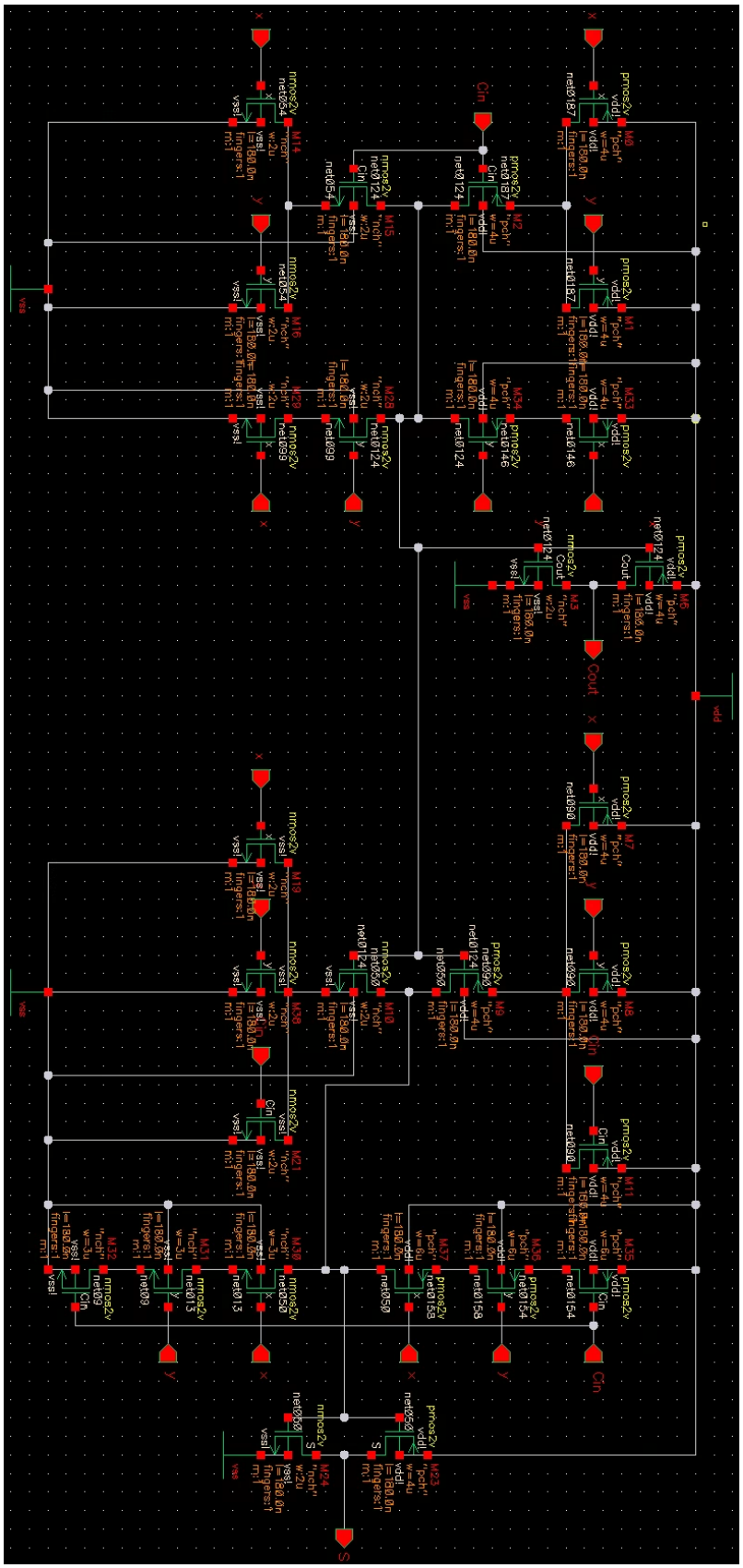


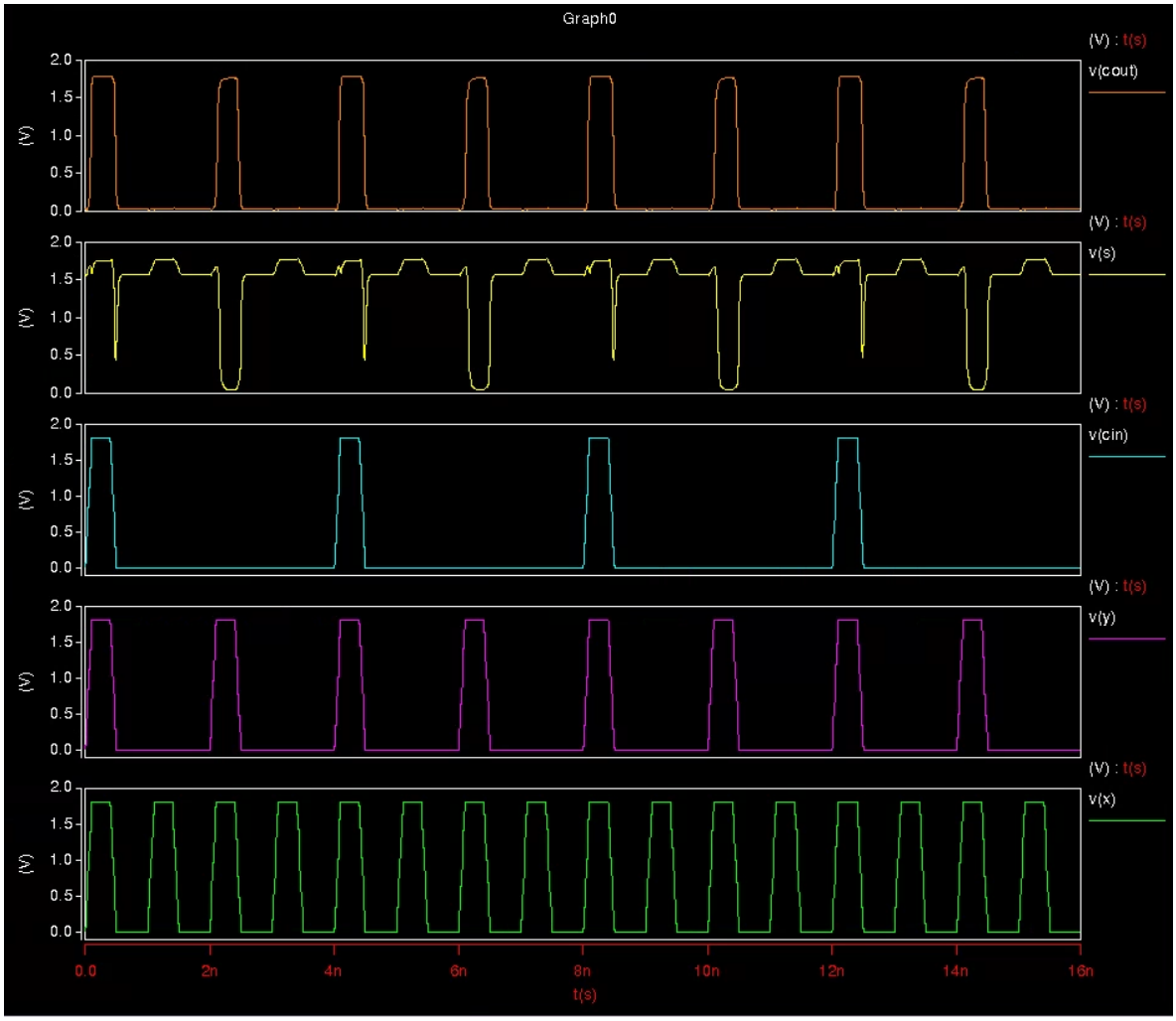
Total:Transistors 有 28 個

使用 Virtuoso Schematic 的 Circuit 跟 HSPICE(C)放在一起

(c) Use HSPICE to verify the functionality of the full adder. What is the maximum propagation delay?

Ans.:

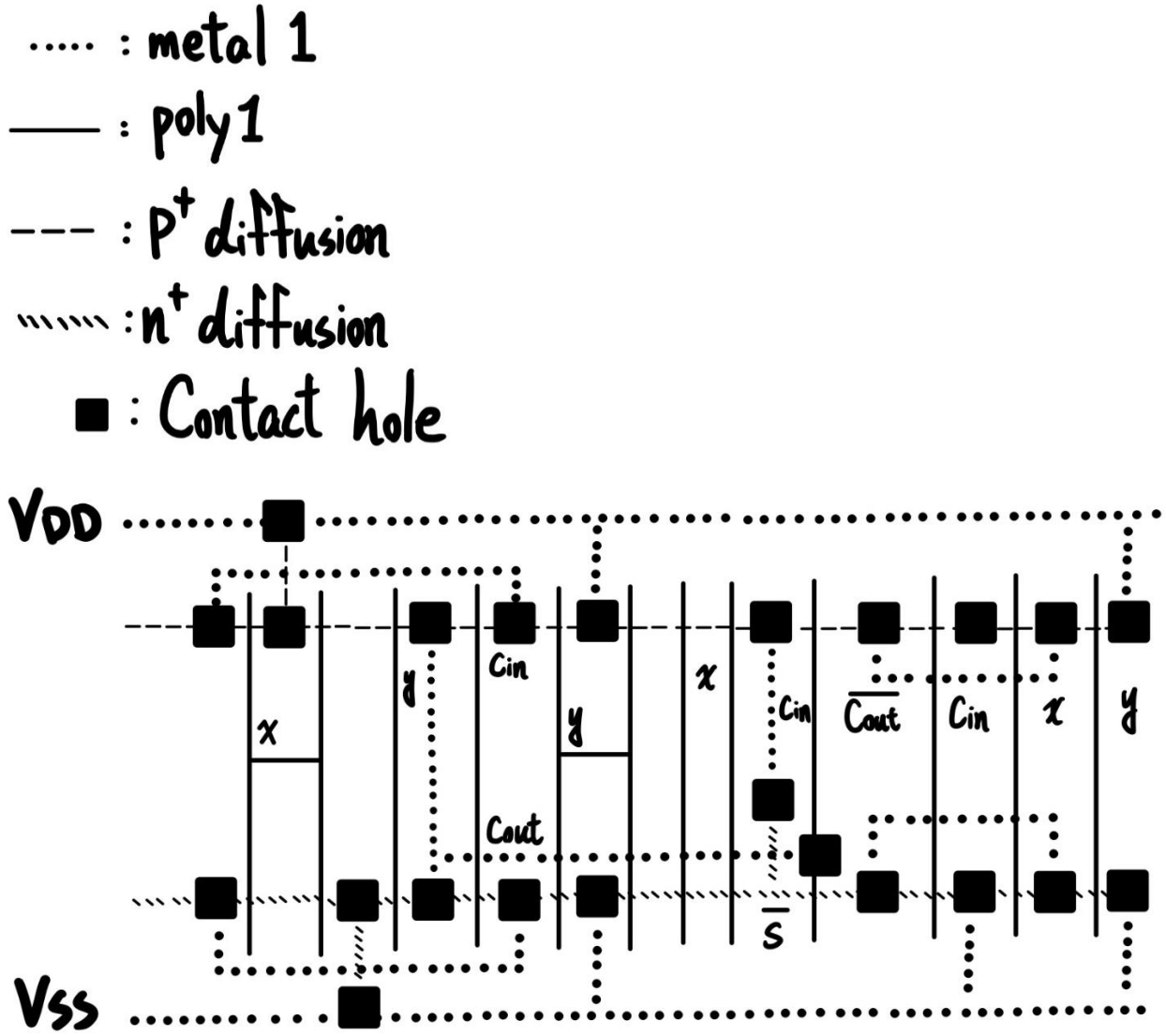





```
 ******  Measured values for the netlist  ********************
tplh_s_cin=  -1.9474e-09    targ=  2.5026n trig=  4.4500n
tplh_s_x=  1.0526e-09    targ=  2.5026n trig=  1.4500n
tplh_s_y=  5.2630e-11    targ=  2.5026n trig=  2.4500n
tplh_cout_cin=  -2.3333e-09    targ=  2.1167n trig=  4.4500n
tplh_cout_x=  6.6675e-10    targ=  2.1167n trig=  1.4500n
tplh_cout_y=  -3.3325e-10    targ=  2.1167n trig=  2.4500n
tphl_s_cin=  -1.8931e-09    targ=  2.1569n trig=  4.0500n
tphl_s_x=  1.1069e-09    targ=  2.1569n trig=  1.0500n
tphl_s_y=  1.0691e-10    targ=  2.1569n trig=  2.0500n
tphl_cout_cin=  -1.5808e-09    targ=  2.4692n trig=  4.0500n
tphl_cout_x=  1.4192e-09    targ=  2.4692n trig=  1.0500n
tphl_cout_y=  4.1921e-10    targ=  2.4692n trig=  2.0500n
tpd_s_cin=  -1.9202e-09    -1.920e-09
tpd_s_x=  1.0798e-09     1.080e-09
tpd_s_y=  7.9771e-11     7.977e-11
tpd_cout_cin=  -1.9570e-09    -1.957e-09
tpd_cout_x=  1.0430e-09     1.043e-09
tpd_cout_y=  4.2981e-11     4.298e-11
```

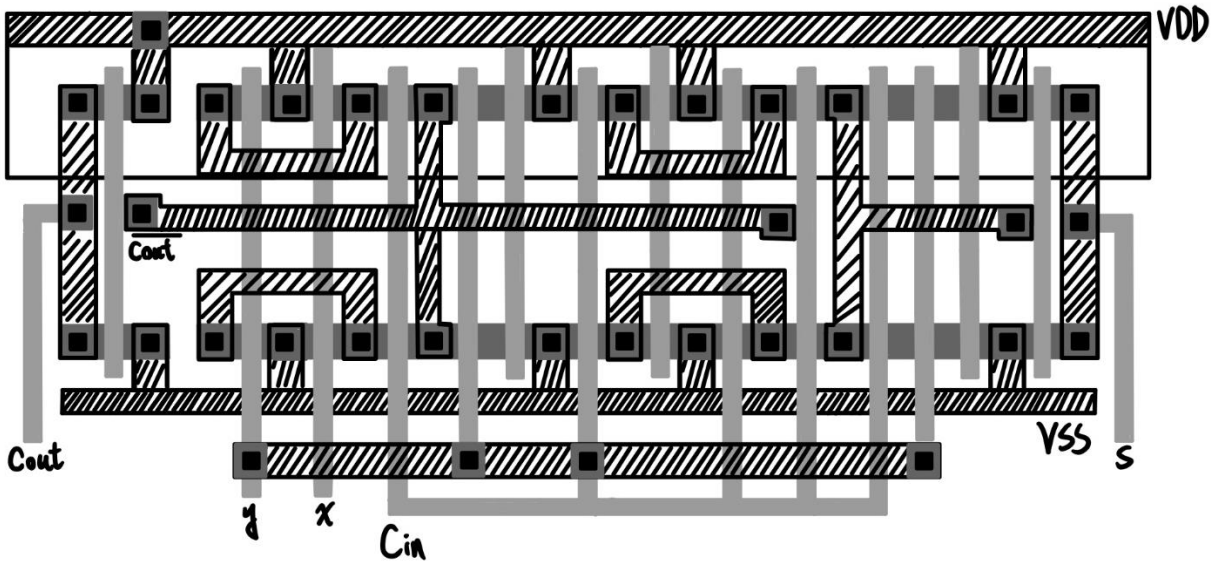
(d) Plot a stick diagram of the full adder.

Ans.:



(e) Draw the physical layout of the full-adder.

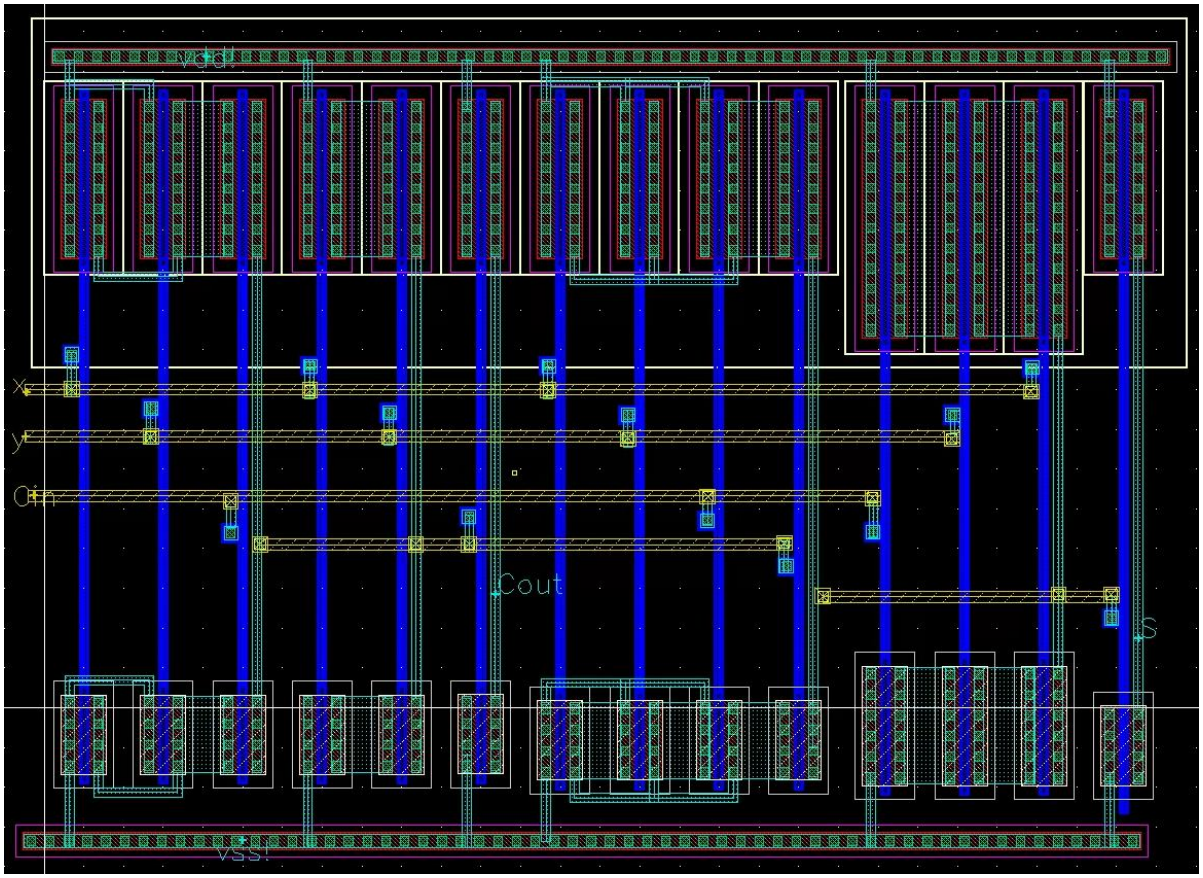
Ans.:



使用 Virtuoso Layouyt 的圖跟 HSPICE 以及 DRC LVS PEX 放在一起(f)

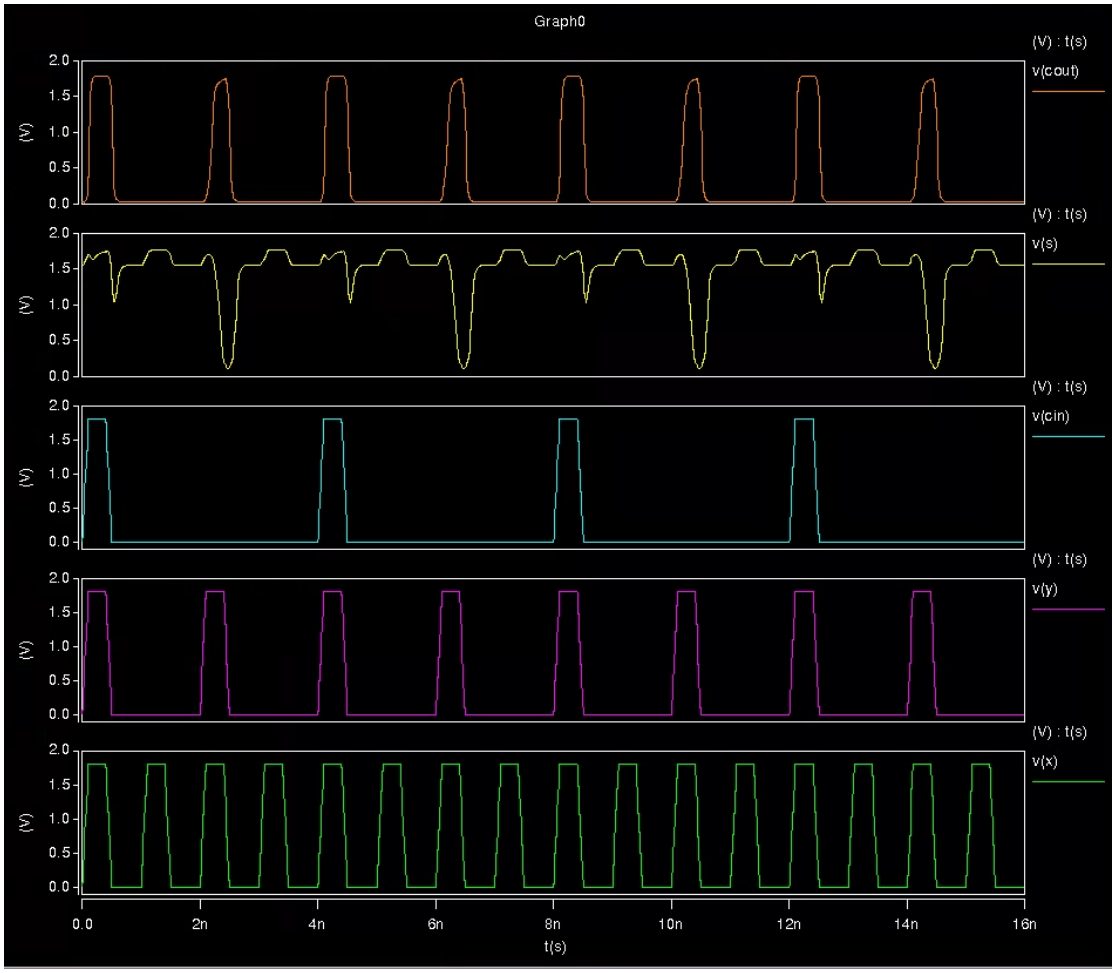
(f) Use HSPICE to verify the functionality of the resulting physical layout and estimate the maximum propagation delay. Compare the result with (c).

Ans.:



Cell full_adder Summary (Clean)

```
                    CELL COMPARISON RESULTS ( TOP LEVEL )


                          #       ##################          _   _
                        #         #                #        *   *
                      #   #       #     CORRECT    #          |
                       # #        #                #         \___/
                         #        ##################


LAYOUT CELL NAME:          full_adder
SOURCE CELL NAME:          full_adder

------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:               7         7

 Nets:               18        18

 Instances:          14        14         MN (4 pins)
                     14        14         MP (4 pins)
                 ------    ------
 Total Inst:         28        28


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:               7         7

 Nets:                9         9

 Instances:           4         4         MN (4 pins)
                      1         1         SPMN_2_1 (5 pins)
                      1         1         SPMP_2_1 (5 pins)
                      1         1         SPMP_3_1 (6 pins)
                      2         2         _invv (4 pins)
                      1         1         _smn2v (4 pins)
                      1         1         _smn3v (5 pins)
                      1         1         _smp2v (4 pins)
                      1         1         _smp3v (5 pins)
                 ------    ------
 Total Inst:         13        13
```



```
 ******  Measured values for the netlist  ***********************
tplh_s_cin=  2.1653e-09    targ=  6.6153n trig=  4.4500n
tplh_s_x=  5.1653e-09    targ=  6.6153n trig=  1.4500n
tplh_s_y=  4.1653e-09    targ=  6.6153n trig=  2.4500n
tplh_cout_cin=  -2.2535e-09    targ=  2.1965n trig=  4.4500n
tplh_cout_x=  7.4648e-10    targ=  2.1965n trig=  1.4500n
tplh_cout_y=  -2.5352e-10    targ=  2.1965n trig=  2.4500n
tphl_s_cin=  2.2712e-09    targ=  6.3212n trig=  4.0500n
tphl_s_x=  5.2712e-09    targ=  6.3212n trig=  1.0500n
tphl_s_y=  4.2712e-09    targ=  6.3212n trig=  2.0500n
tphl_cout_cin=  -1.5389e-09    targ=  2.5111n trig=  4.0500n
tphl_cout_x=  1.4611e-09    targ=  2.5111n trig=  1.0500n
tphl_cout_y=  4.6114e-10    targ=  2.5111n trig=  2.0500n
tpd_s_cin=  2.2183e-09     2.218e-09
tpd_s_x=  5.2183e-09     5.218e-09
tpd_s_y=  4.2183e-09     4.218e-09
tpd_cout_cin=  -1.8962e-09    -1.896e-09
tpd_cout_x=  1.1038e-09     1.104e-09
tpd_cout_y=  1.0381e-10     1.038e-10
```