ET5302701

Homework Assignment # 3

Date: November 1, 2024 **Instructor: M. B. Lin**

Due Date: November 22, 2024

Homework is due **at the class beginning.** Please note that **NO late homework** will be accepted. Working together on homework is encouraged, but copying assignments will not be allowed.

1. (A study of inverter circuits)

   (a) Design an inverter with the following circuit parameters: $L_p = L_n = L_{min}$ and $W_p = W_n = W_{min}$. Draw the schematic and the physical layout of the inverter and then perform the LVS check and extract the parameters from the physical layout.

   (b) Cascade three copies of the above inverter.

   (c) Apply an ideal square wave (that is, both rise and fall times are set to 0 ns) with the 50% duty cycle of an appropriate frequency to the input of the first stage and measure the propagation delay of the second stage.

   (d) Repeat above steps with the following circuit parameters: $W_n = W_{min}$ and $W_p = 2W_{min}$.

   (e) Compare both results and give your comments.

2. (A study of path delays)

   (a) Draw the schematic diagram of a three-stage logic circuit with a load capacitor of 0.5 pF. The output of the two-input NOR gate is connected to an inverter and the output of the inverter is in turn connected to one input of a two-input NAND gate. The output of the NAND gate drives the load capacitor. Suppose that the channel lengths and widths of all transistors are set as follows: $L_{\text{(all gates)}} = L_{\min}$, $W_{p(NOR)} = 4W_{\min}$, $W_{p(NOT)} = 2W_{\min}$, $W_{p(NAND)} = 2W_{\min}$, $W_{n(NOR)} = W_{\min}$, $W_{n(NOT)} = W_{\min}$, $W_{n(NAND)} = 2W_{\min}$. The unused inputs of the NAND and NOR gates are connected to V_{DD} and ground, respectively.

   (b) Apply an ideal square wave (that is, both rise and fall times are set to 0 ns) of an appropriate frequency to the input of the first stage, and measure both t_{pLH} and t_{pHL} of the output of the last stage.

   (c) (FO4 rule) Scale up the W of both pMOS and nMOS transistors for the second and last stages by factors of 4 and 16, respectively, and repeat the above step.

   (d) (Path-delay optimization) Use the method of path-delay optimization, scale up the W of both pMOS and nMOS transistors for each stage, and repeat the above step. Assume that $C_{in} = C_g(W_n + W_p)$.

   (e) Compare the results from (b) to (d) and give your comments.