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In this homework we have five project options. You only need to pick one of them and finish it completely using full-custom approach. Your report must at least include circuit, layout, pre-layout and post-layout simulation results, LVS result, and DRC result. Also you may add I/O pads to your circuit core and run off-line DRC.

Project 1: Design and implement an 4×4 Booth's array multiplier (Slide 12-59) studied in the class.

Project 2: Design and implement an 8-bit synchronous binary counter.

Project 3: Design and implement an 8-bit carry-lookahead adder.

Project 4: Design and implement an 8-bit carry-skip adder.

Project 5: Design and implement the non-restoring array divider (Slides 12-63 and 12-64) studied in the class.

I. Introduction

這次的做業我選擇 **Project 4: Design and implement an 8-bit carry-skip**

adder. CSA 是一種改良的加法器，通過加入 skip logic 來減少進位傳遞延遲，

以提高運算速度。相較於傳統的漣波進位加法器，CSA 能在特定條件下直接跳

過進位傳遞，從而達到更好的性能

II. Design

以下是我的步驟說明

第一步驟

先建立 2-bits carry skip adder 分為兩個部分

1.架構設計:

- 使用兩個 full adder 作為基本運算單元
- 採用 XOR 閘產生 propagate 信號
- 設計 skip 邏輯使用 AND 和 OR 閘的組合

2.Skip logic 實現

- 使用 XOR 計算每個位元的 propagate 條件($P_i = A_i \oplus B_i$)
- 將 propagate 信號和輸入進位(Cin)經過 AND 閘判斷跳躍條件
- 最後通過 OR 閘選擇是否採用跳躍路徑

再來是 8-bit CSA 設計

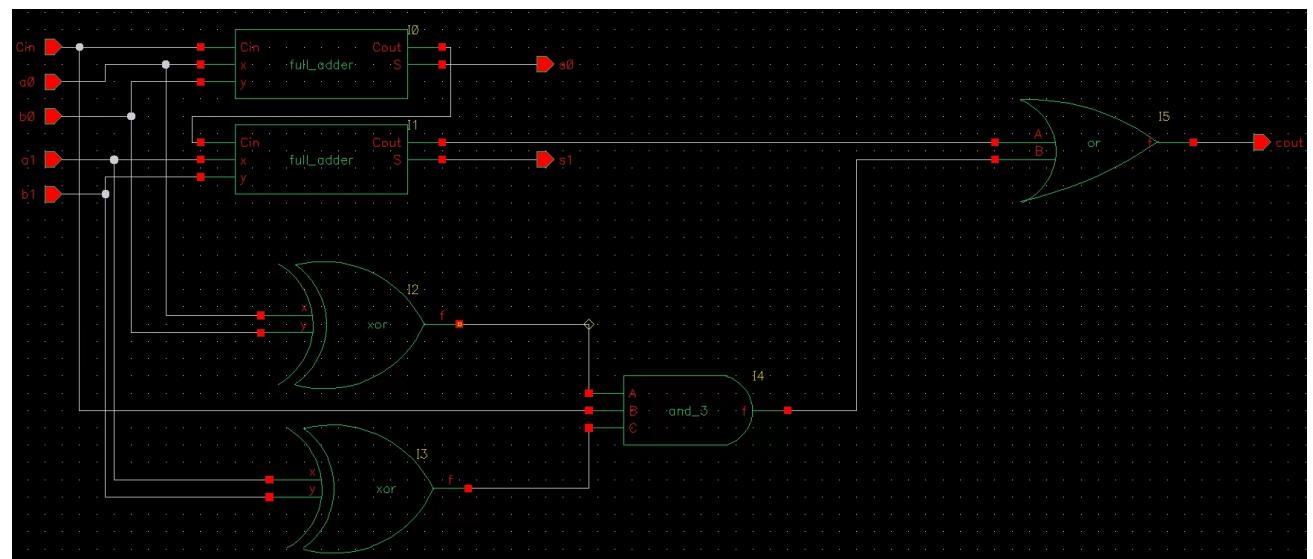
透過串接四個 2-bit CSA 模組來實現 8-bit 加法器。

這種模組化的設計方式有以下優點：

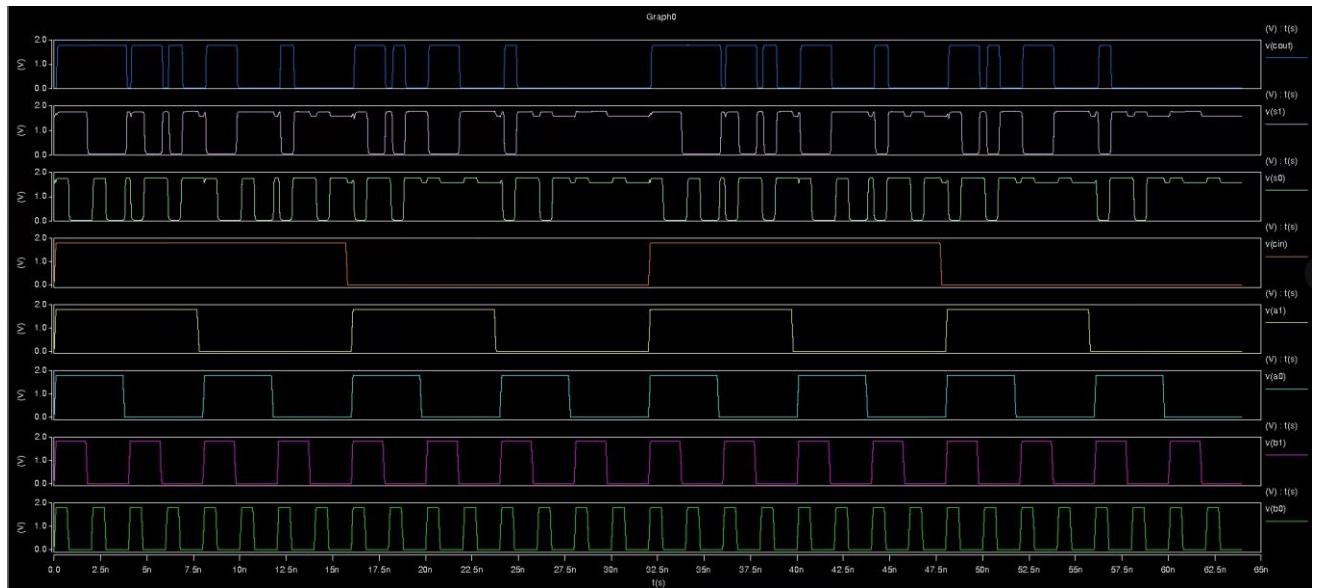
- 降低設計複雜度
- 提高電路重用性
- 便於驗證與除錯

III. Implement and Verification

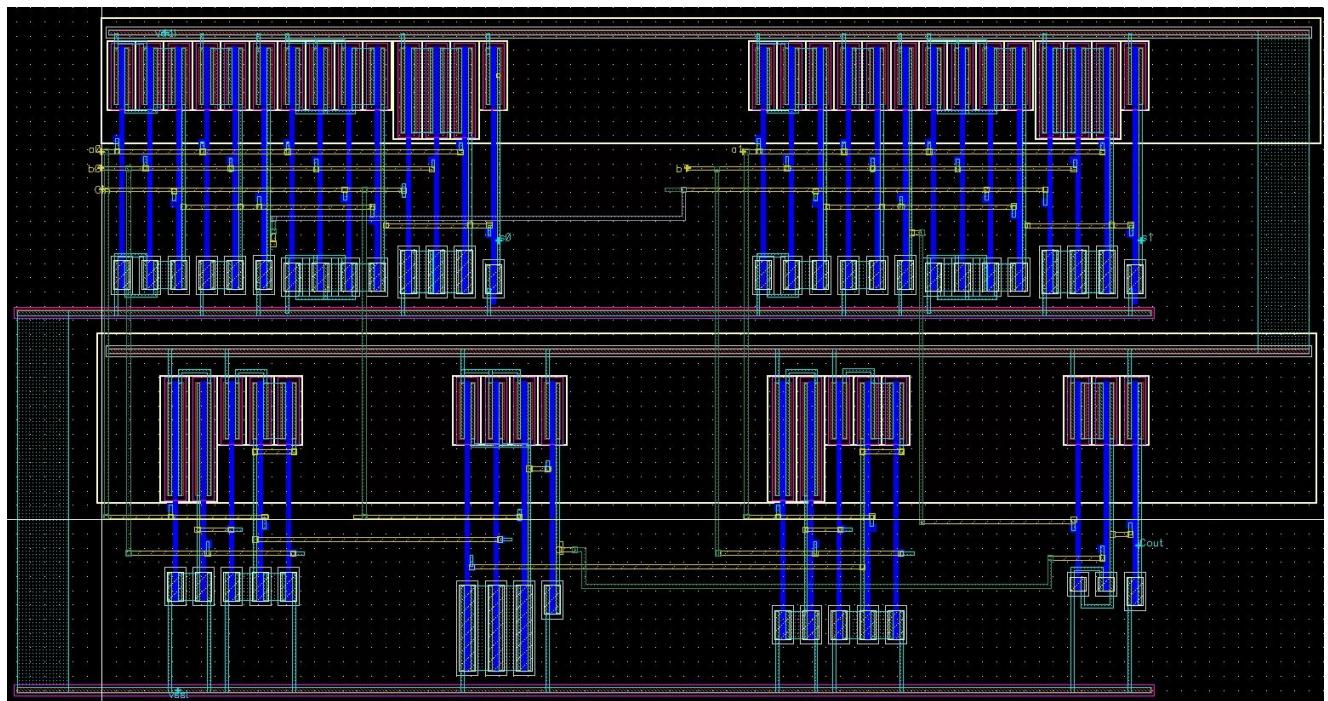
circuit:



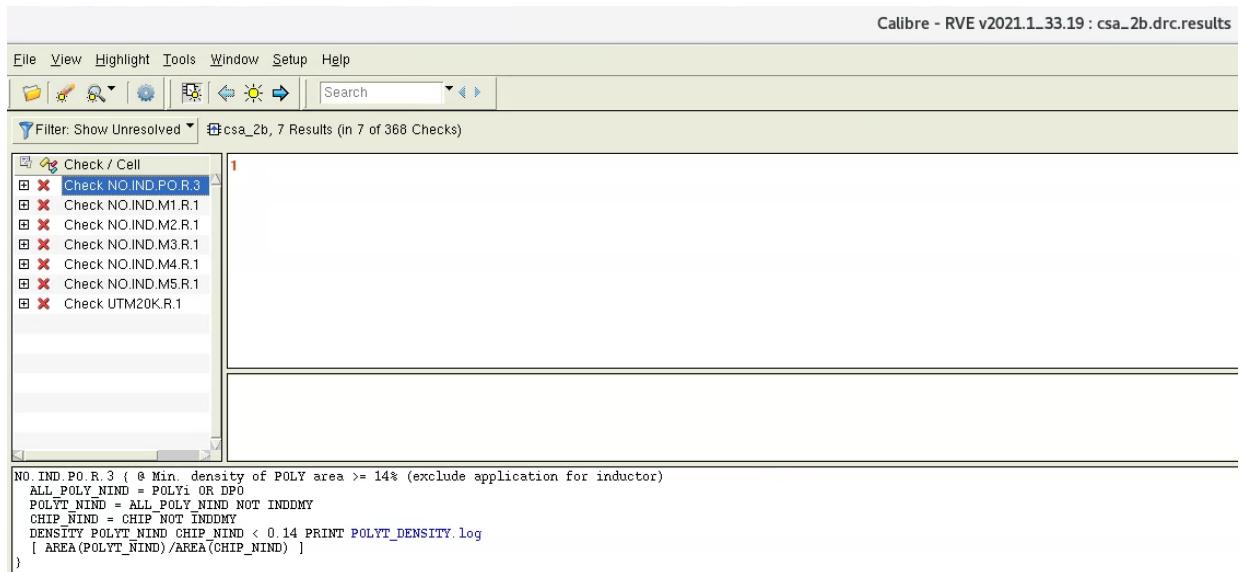
Pre-layout simulation:



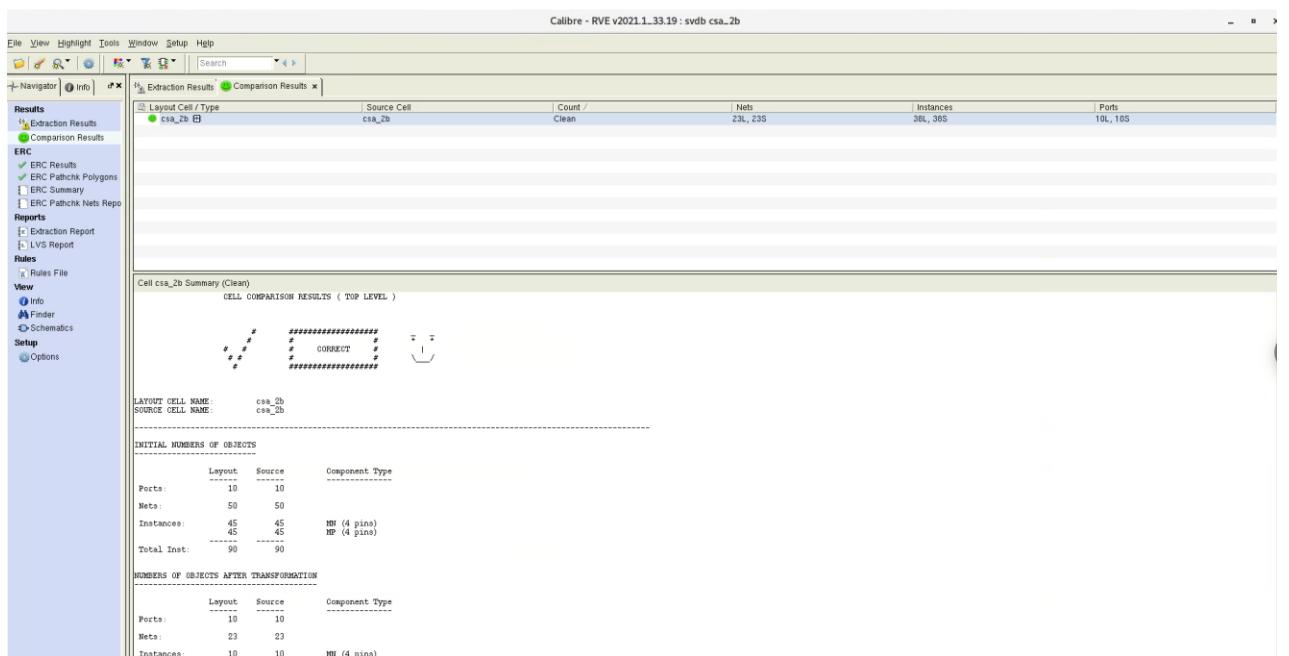
Layout:



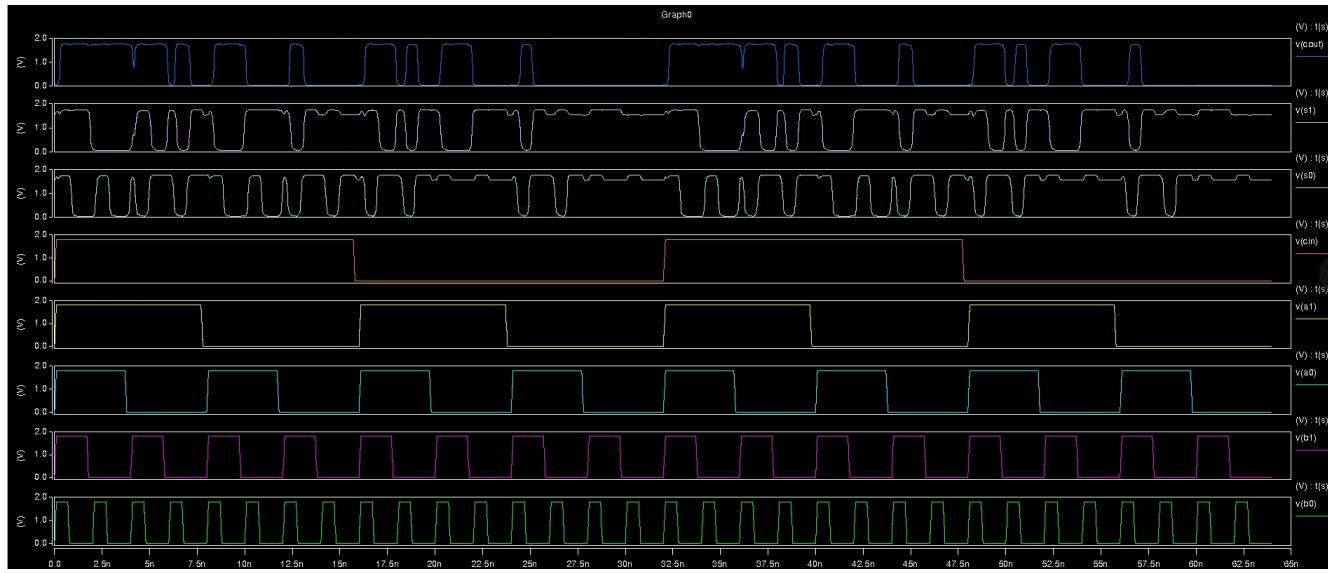
DRC:



LVS:

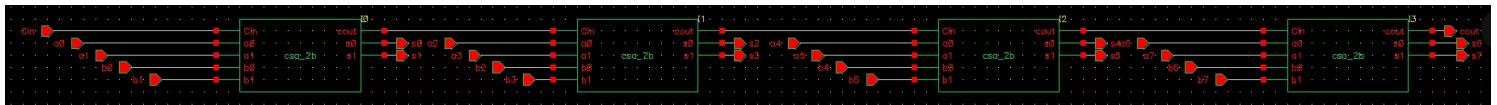


Post-layout simulation:

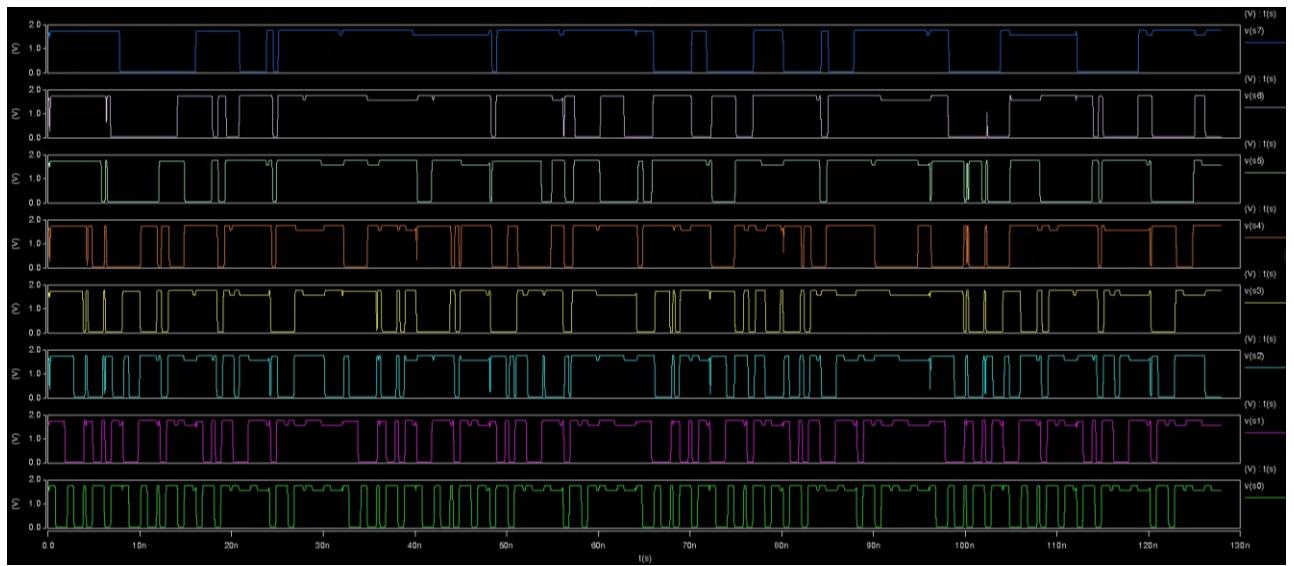


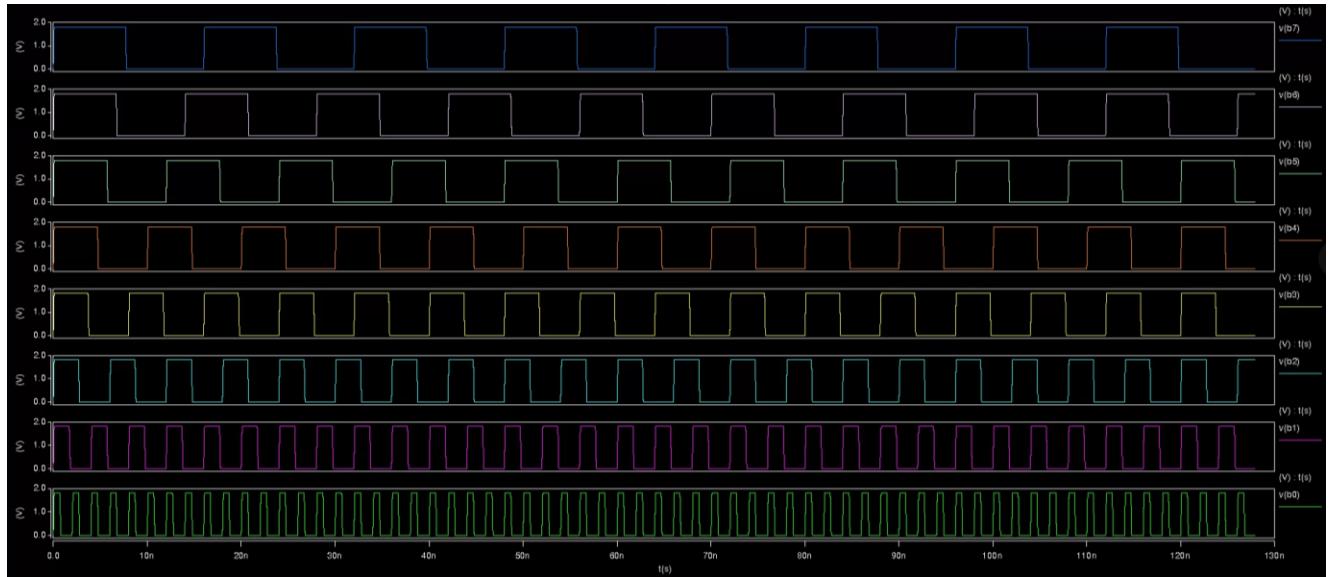
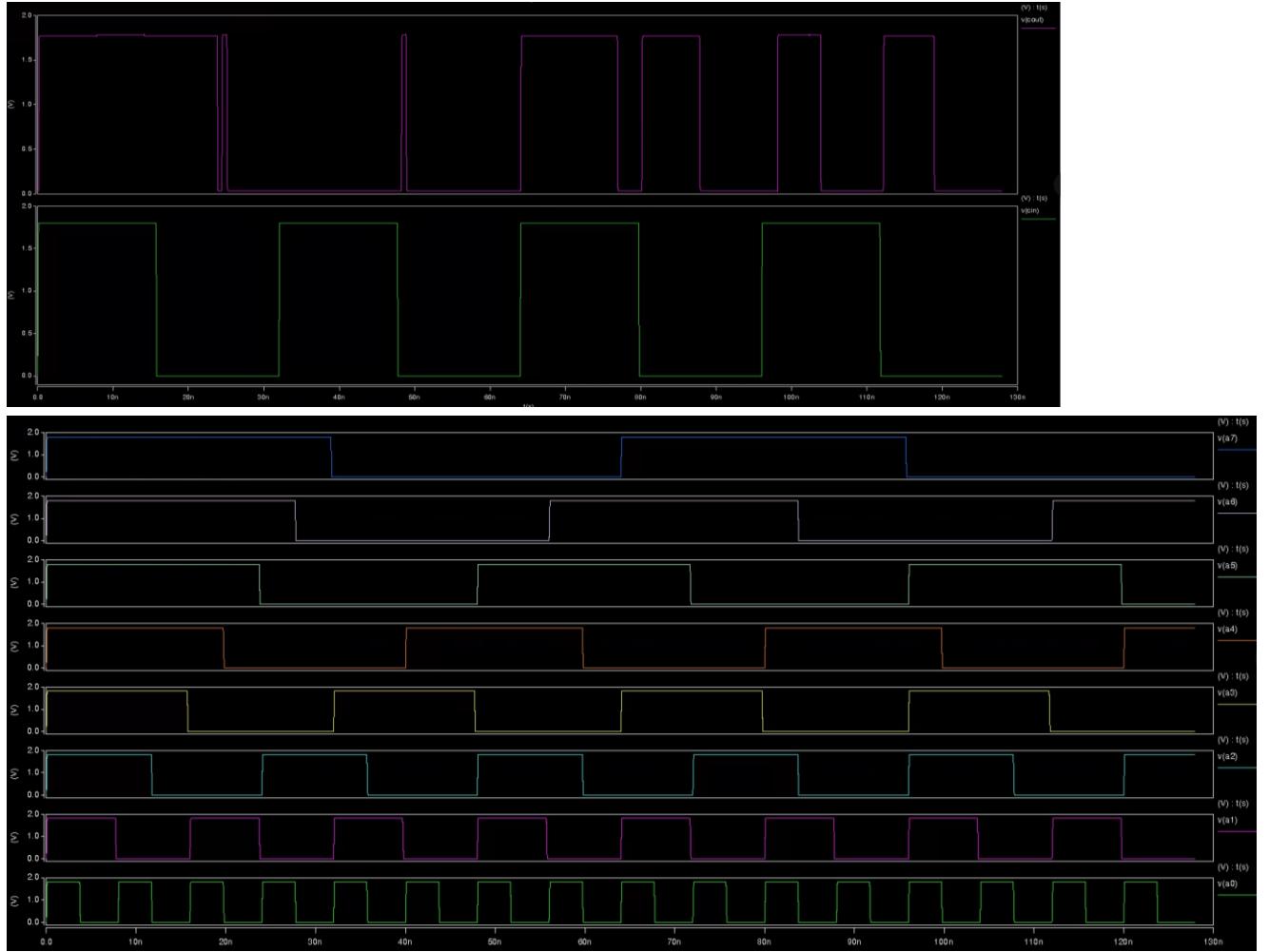
第二步驟 串聯四顆 carry skip adder 來完成 8-bits carry skip adder

circuit:



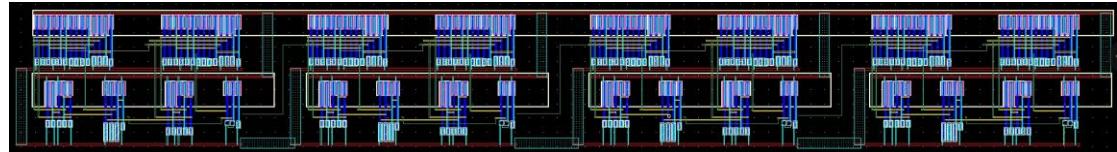
Pre-layout simulation:





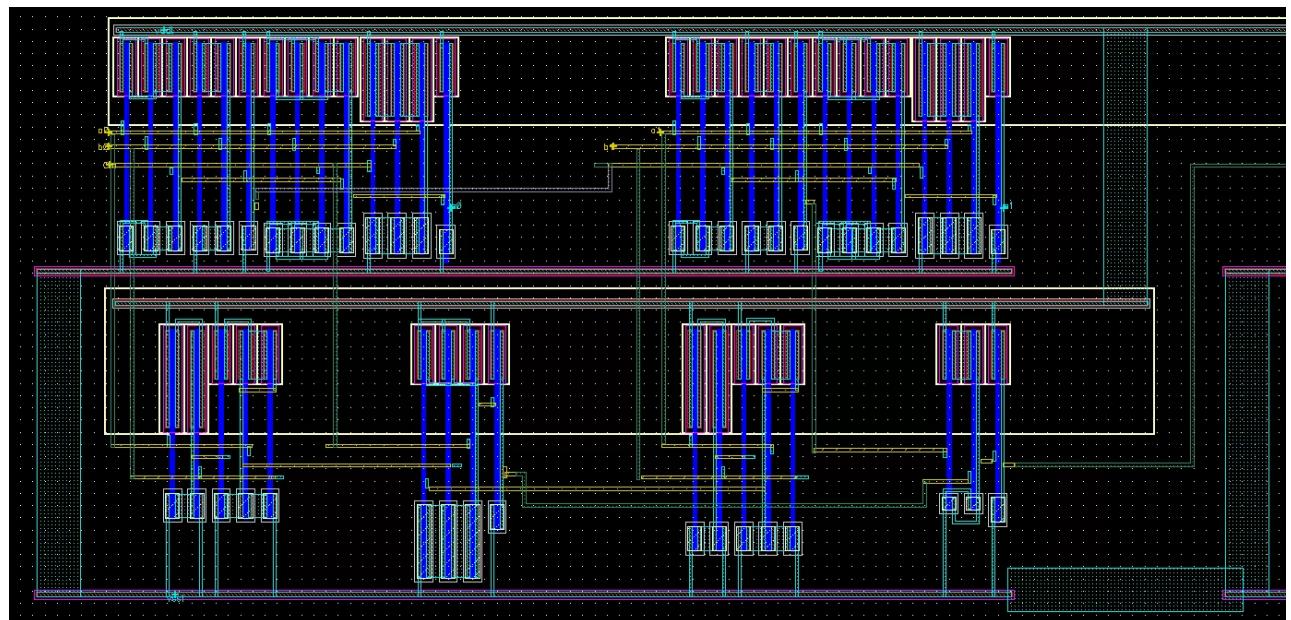
Layout:

全局圖

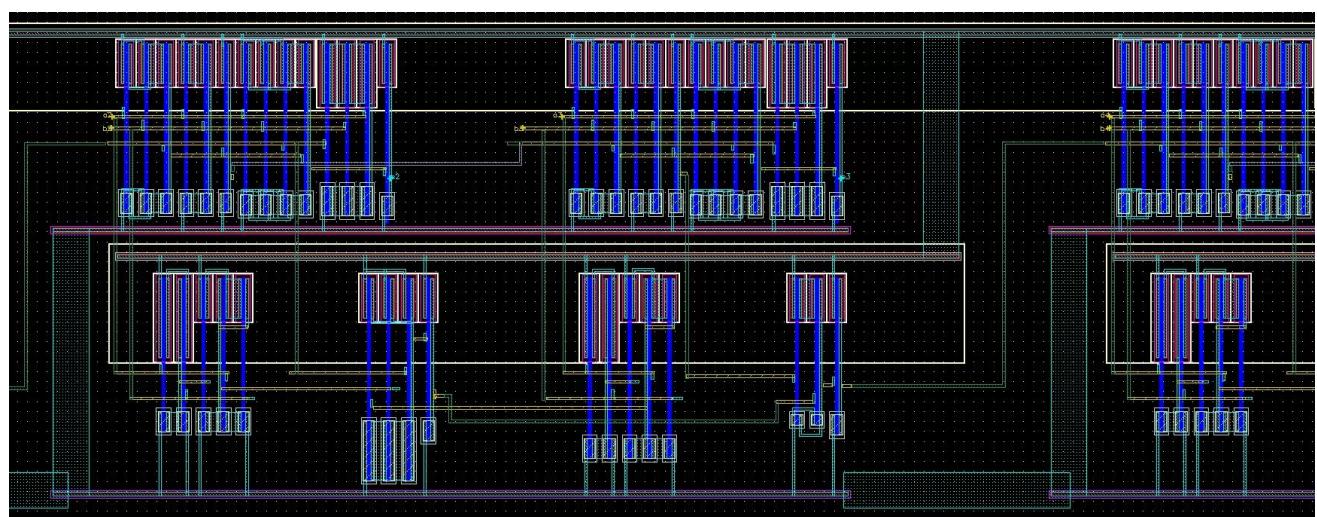


局部圖

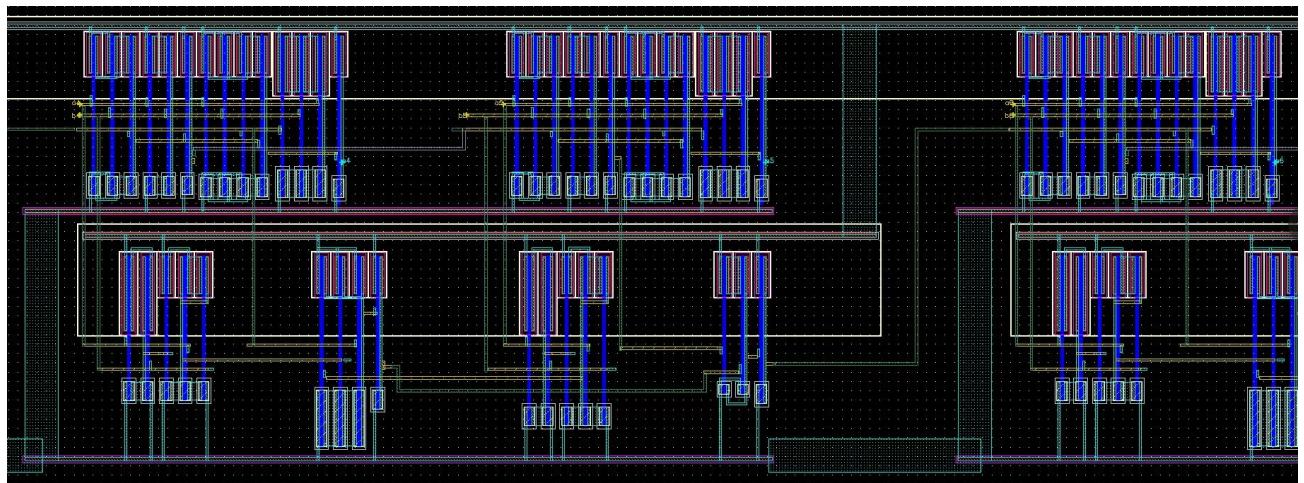
第一顆 2-bits carry skip adder



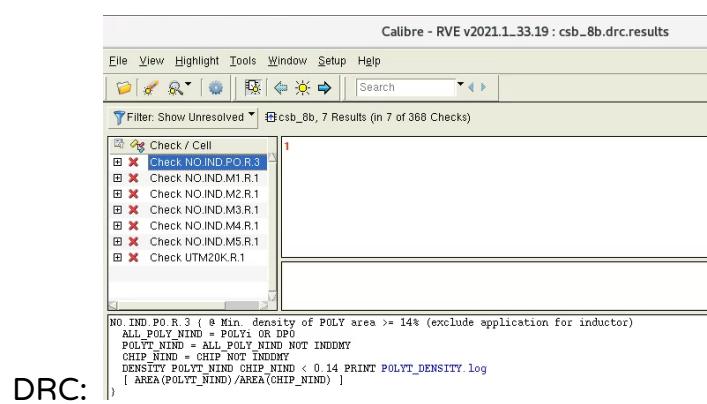
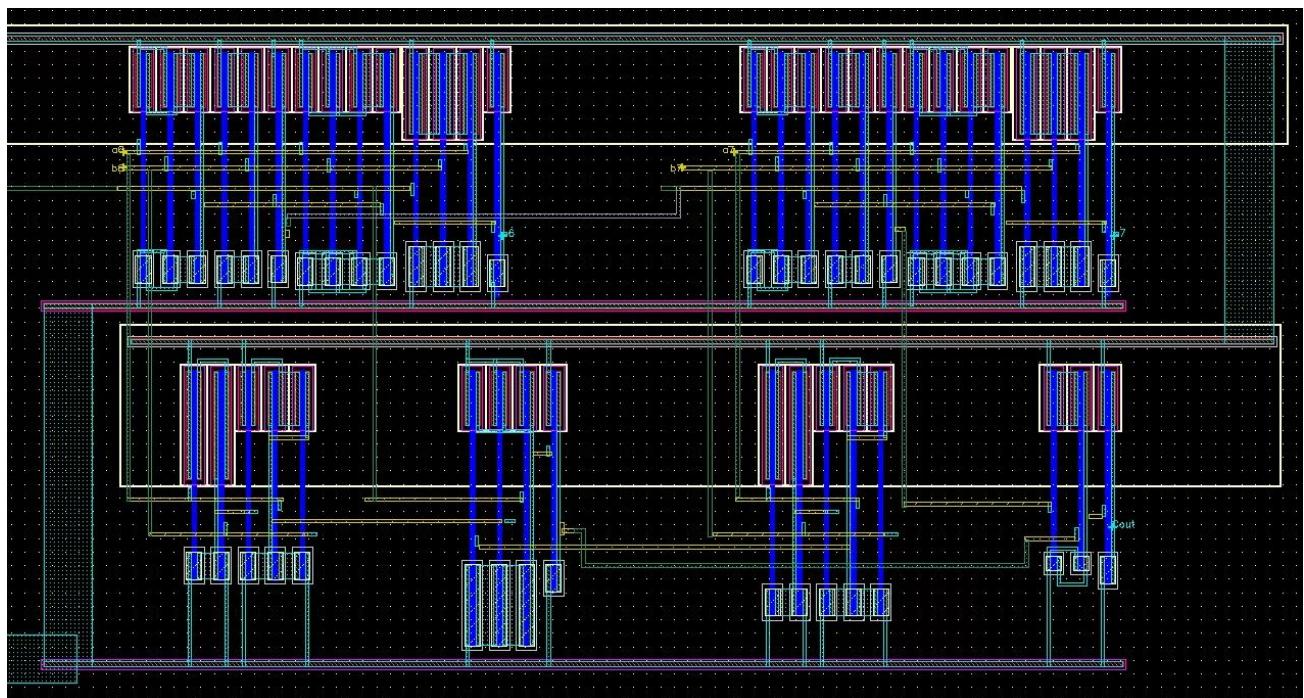
第二顆



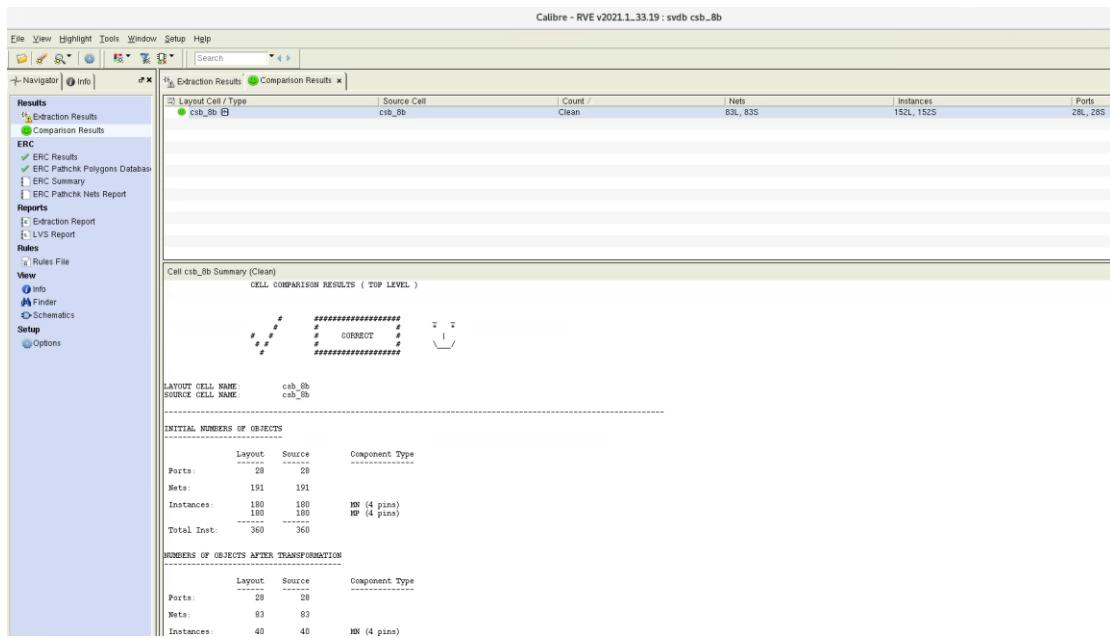
第三顆



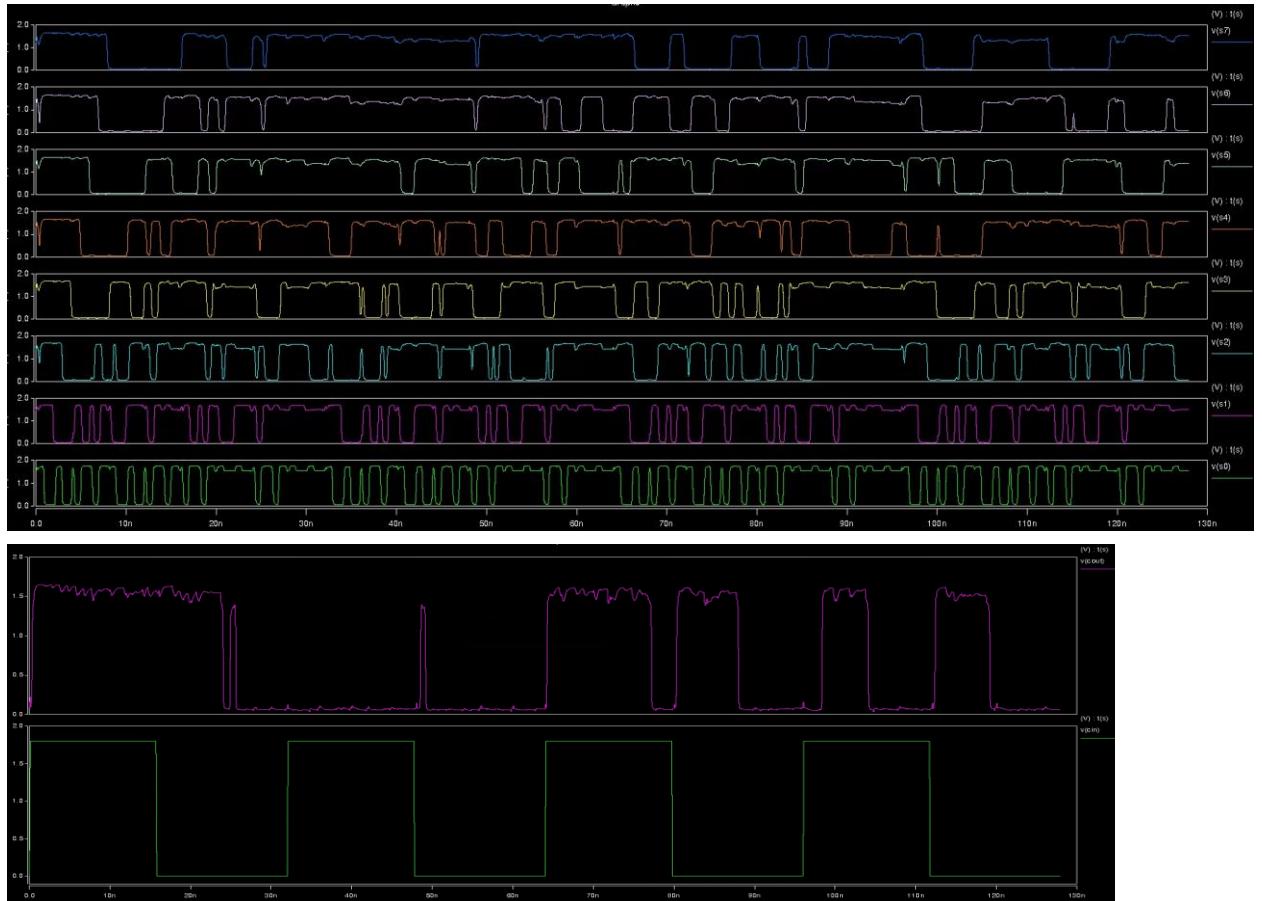
第四顆與 cout

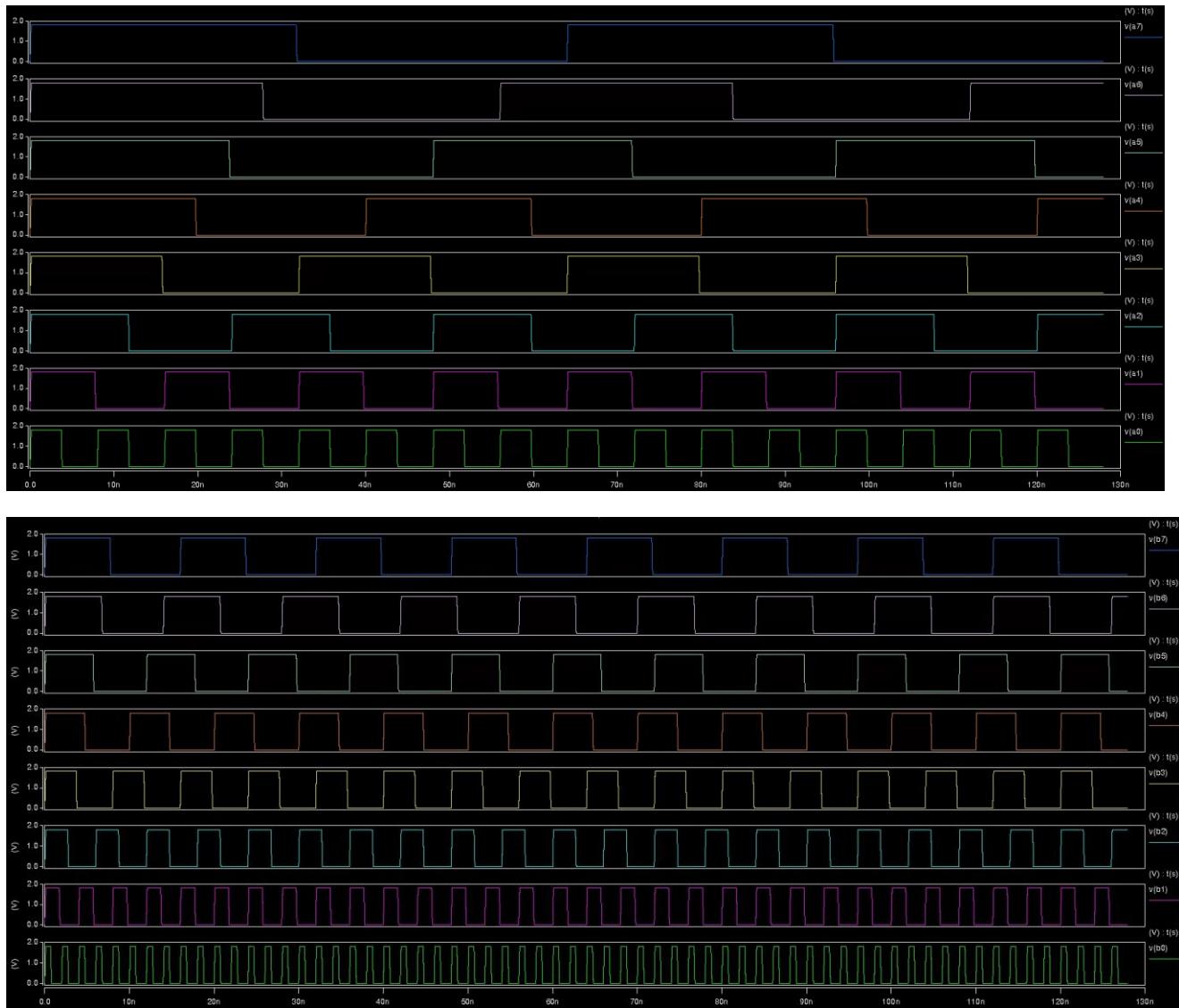


LVS:



Post-layout simulation:





IV. conclusion

成功設計與實現了 8-bit Carry skip adder，透過完整的 design flow，從電路設計, Layout, 驗證都有達到目標

實現成果：

1. 基本架構

- 成功實現 2-bit CSA 作為基本單元
- 透過模組化設計擴展至 8-bit
- 採用標準元件實現 skip logic

2.電路特點

- Skip logic 有效減少進位延遲
- 模組化設計便於維護和擴展
- Layout 繫湊，降低面積開銷
- 信號完整性良好，無明顯毛刺

3.驗證結果

- Pre-layout 與 Post-layout simulation 結果相符
- 通過 DRC 驗證，符合製程規則
- LVS 檢查無誤，確保 Layout 正確性

Future Work :

1. 探討不同 block 大小對性能的影響
2. 優化 skip logic 結構
3. 考慮功耗優化的可能性

V. References

1. Ming-Bo Lin, Digital Logic Design, 6th ed., Taipei, Taiwan: Chuan Hwa Book Ltd., 2017.
2. M. Morris Mano and Michael D. Ciletti, Digital Design: With An Introduction to the Verilog HDL, 5th Ed., Upper Saddle River, NJ: Prentice-Hall, 2013.
3. Jr. Charles H. Roth and Larry L. Kinney, Fundamentals of Logic Design, 7th Ed., Cengage Learning, 2013.
4. Ming-Bo Lin, Introduction to VLSI Systems: A Logic, Circuit, and System Perspective, CRC Press, 2012
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6. Ming-Bo Lin, VLSI Class Notes, 2024.
7. R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 2nd ed., IEEE/Wiley Interscience, 2005.
8. Michael Quirk and Julian Serda, Semiconductor Manufacturing Technology, Upper Saddle River, N. J.: Prentice-Hall, 2001.
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10. Neil H. E. Weste and David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., New-York: Pearson Education, Inc., 2010.