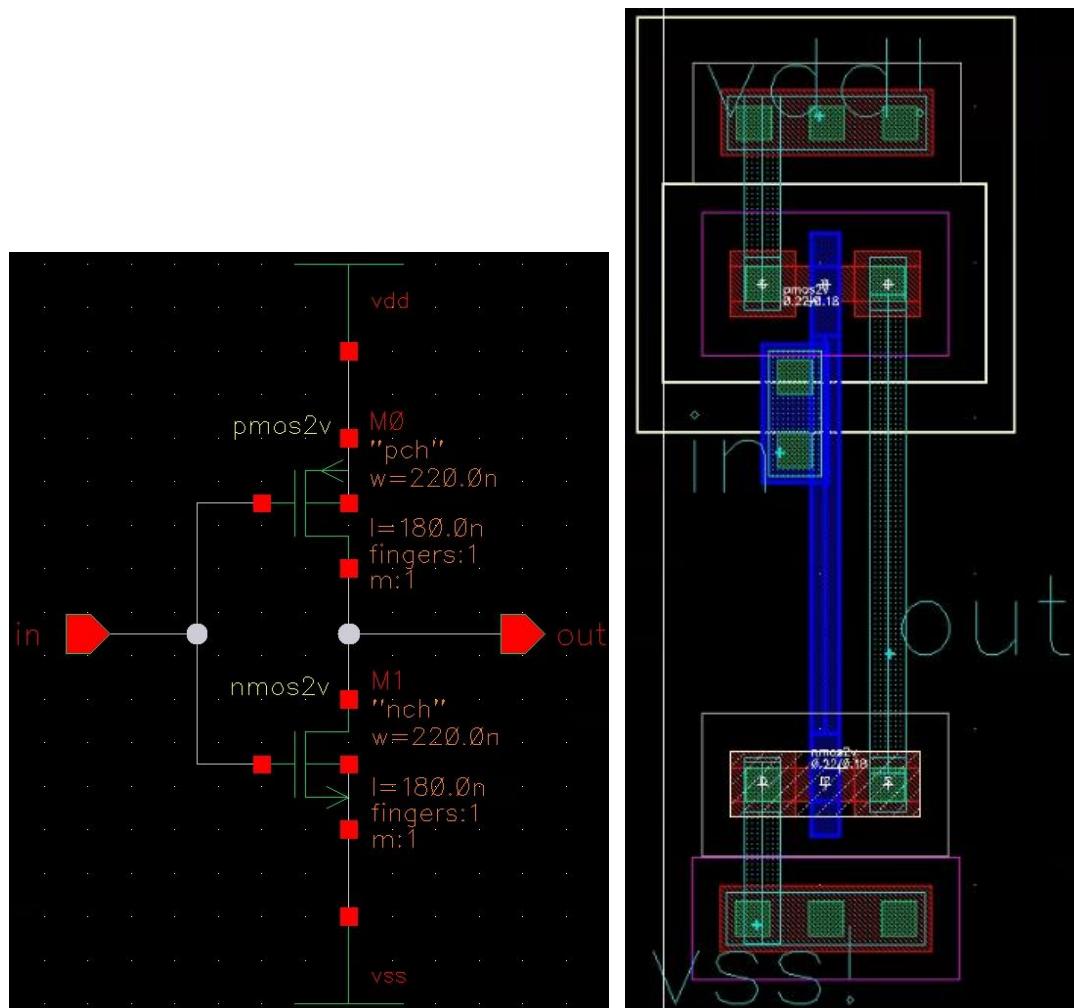


# M11215075 資工碩二 胡劭

## 1. (A study of inverter circuits)

- (a) Design an inverter with the following circuit parameters:  $L_p = L_n = L_{min}$  and  $W_p = W_n = W_{min}$ . Draw the schematic and the physical layout of the inverter and then perform the LVS check and extract the parameters from the physical layout.

Ans:



```

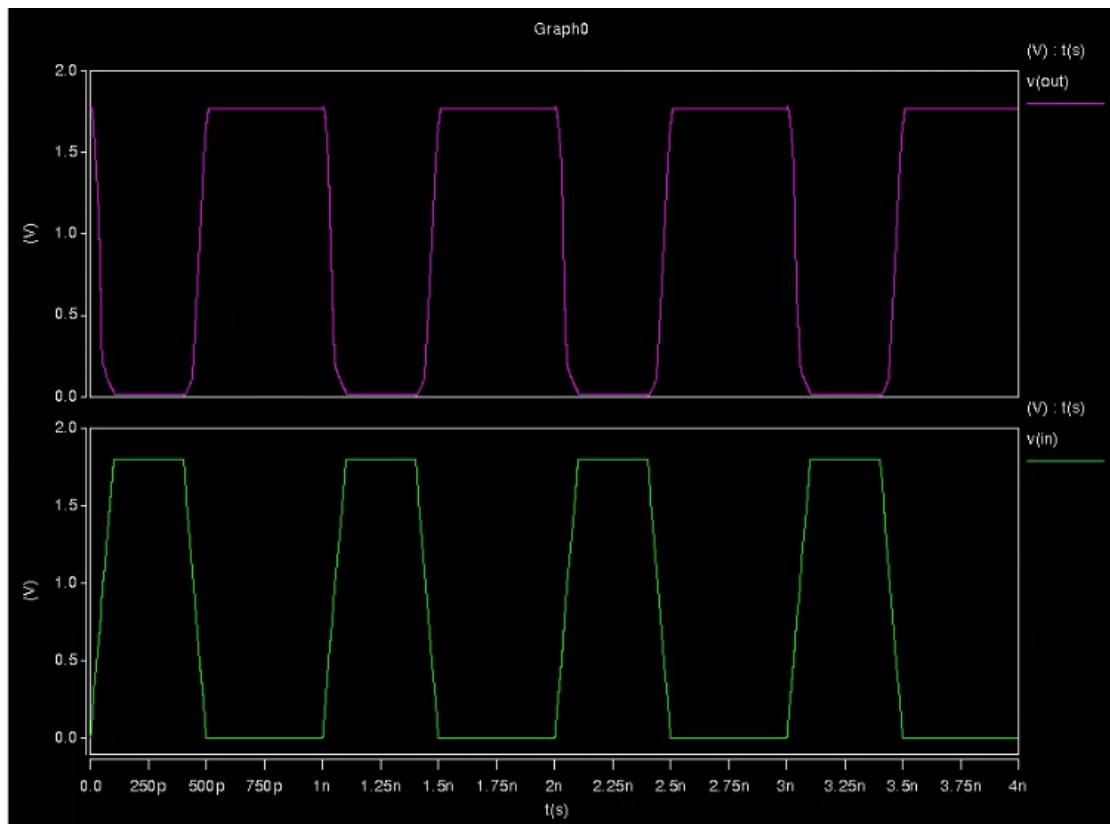
.SUBCKT inv2 in out
*.PININFO in:I out:O
MM0 out in vdd! vdd! pmos l=180.0n w=220.0n m=1
MM1 out in vss! vss! nmos l=180.0n w=220.0n m=1
.ENDS

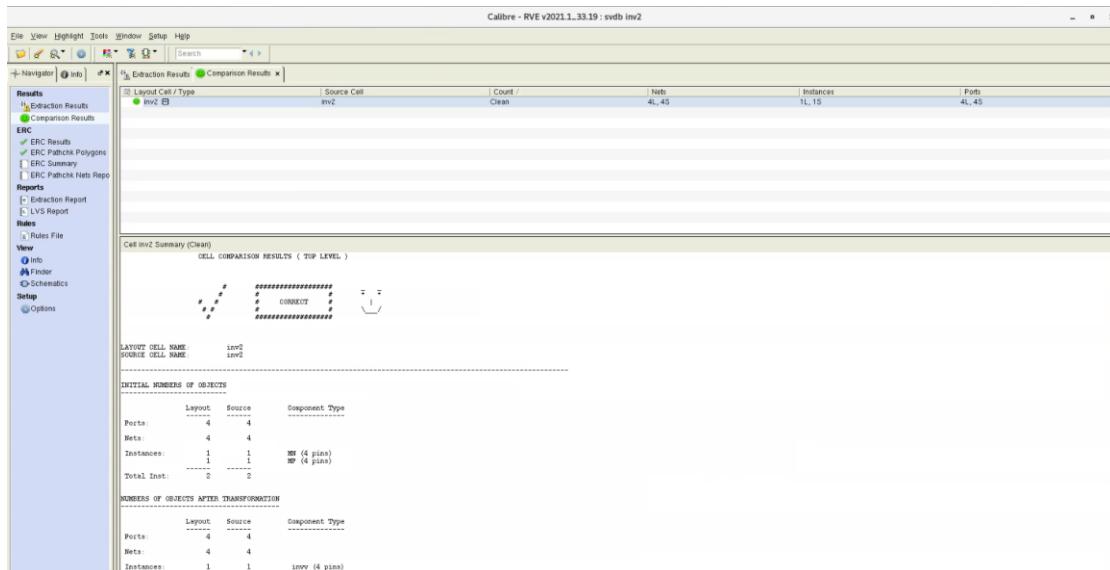
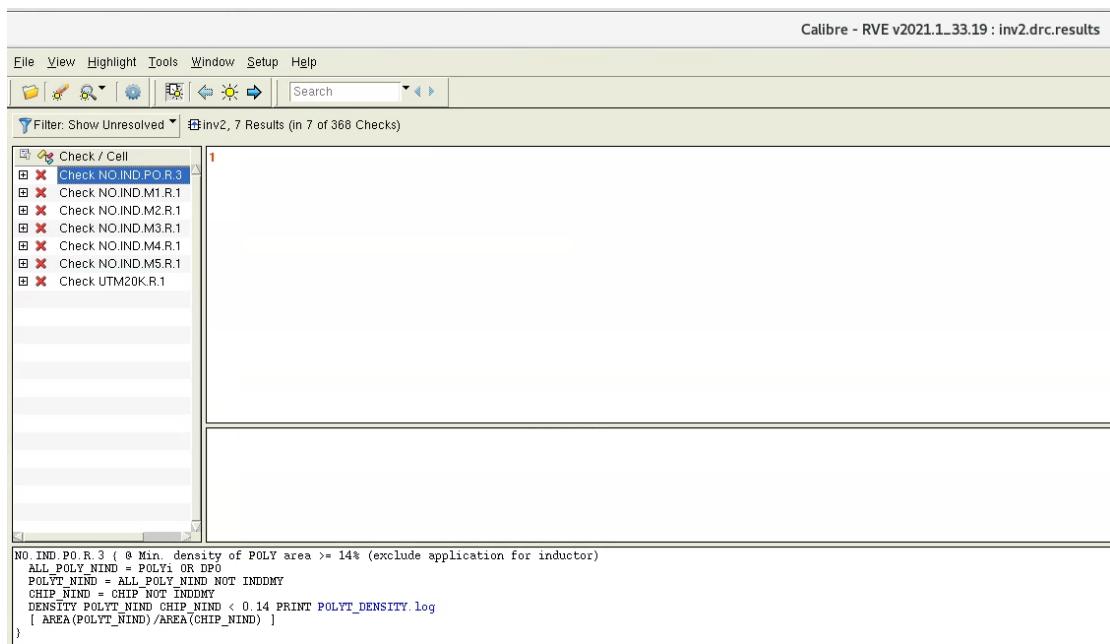
```

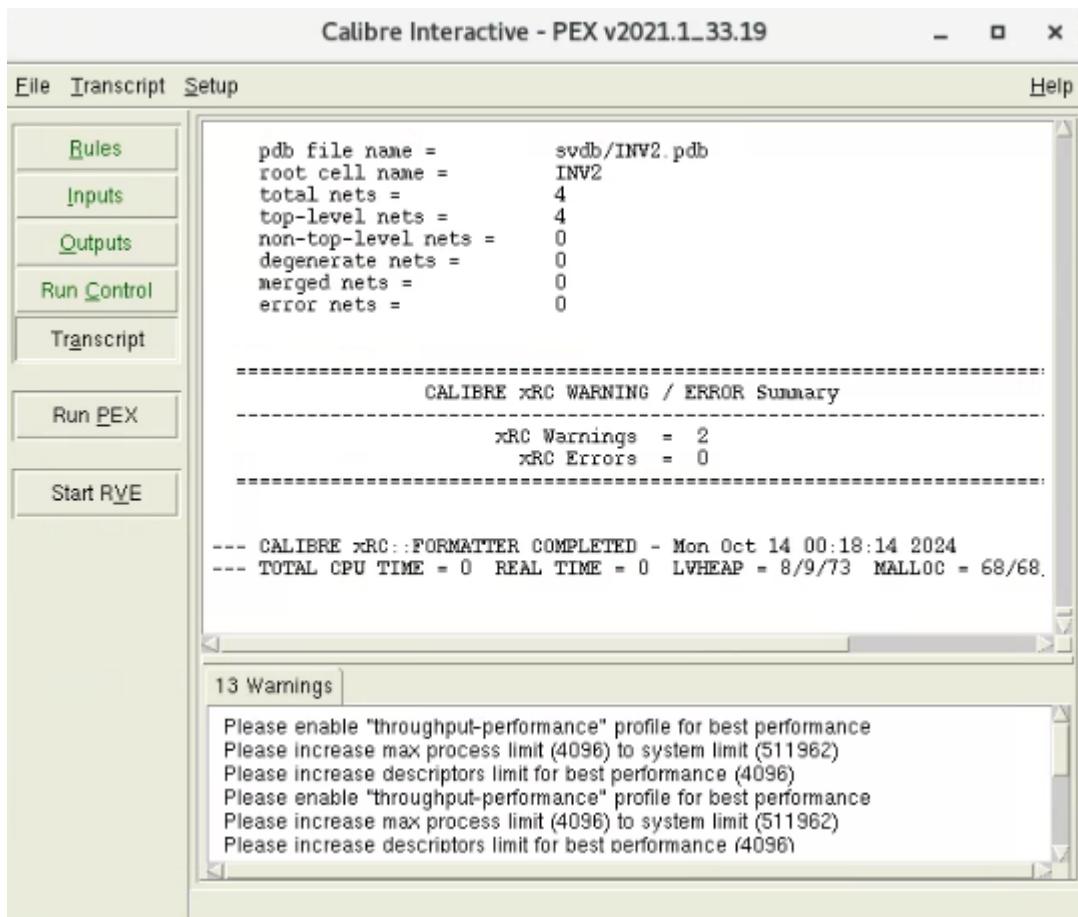
```

.lib "PTM180.l" cmos
xinv in out inv2
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0.1n 0.1n 0.3n 1n)
.trans 1ps 4ns
.measure tpLH *rising propagation delay
+ trig V(in) val=0.9 fall=2
+ targ V(out) val=0.9 rise=2
.measure tpHL *falling propagation delay
+ trig V(in) val=0.9 rise=2
+ targ V(out) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'
.probe tran V(in) V(out)
.option post=2
.end

```

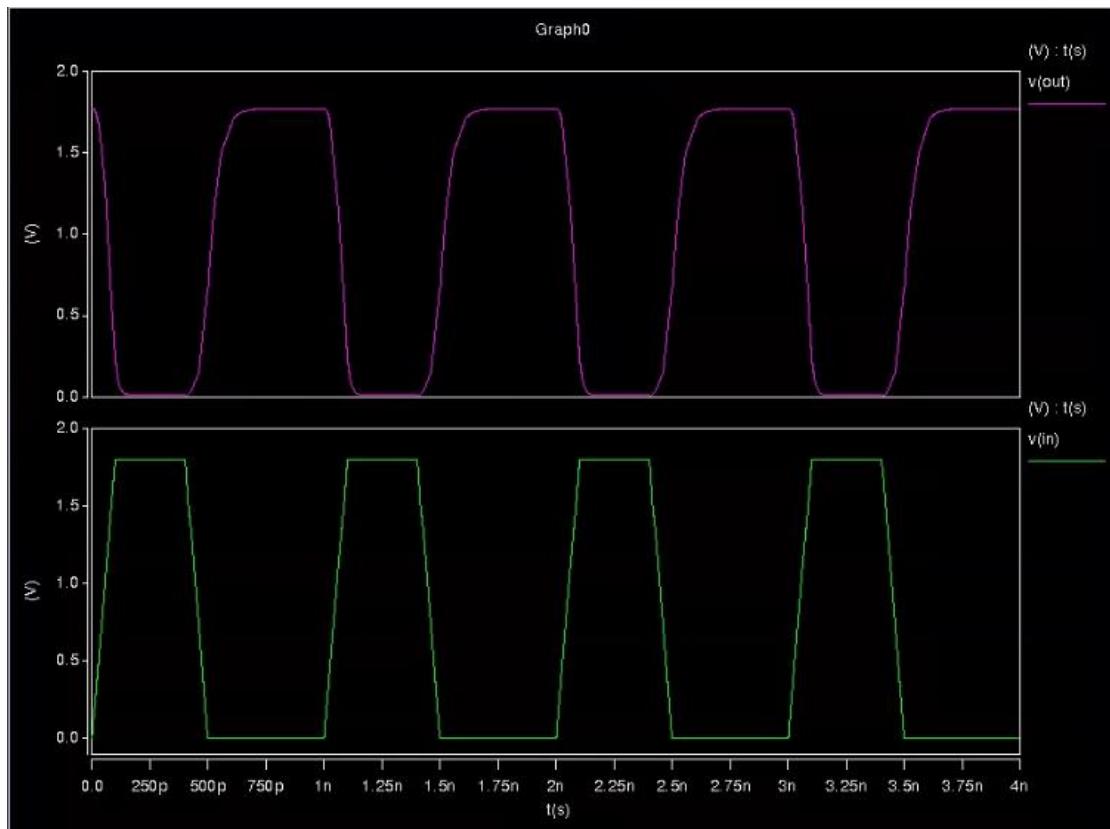






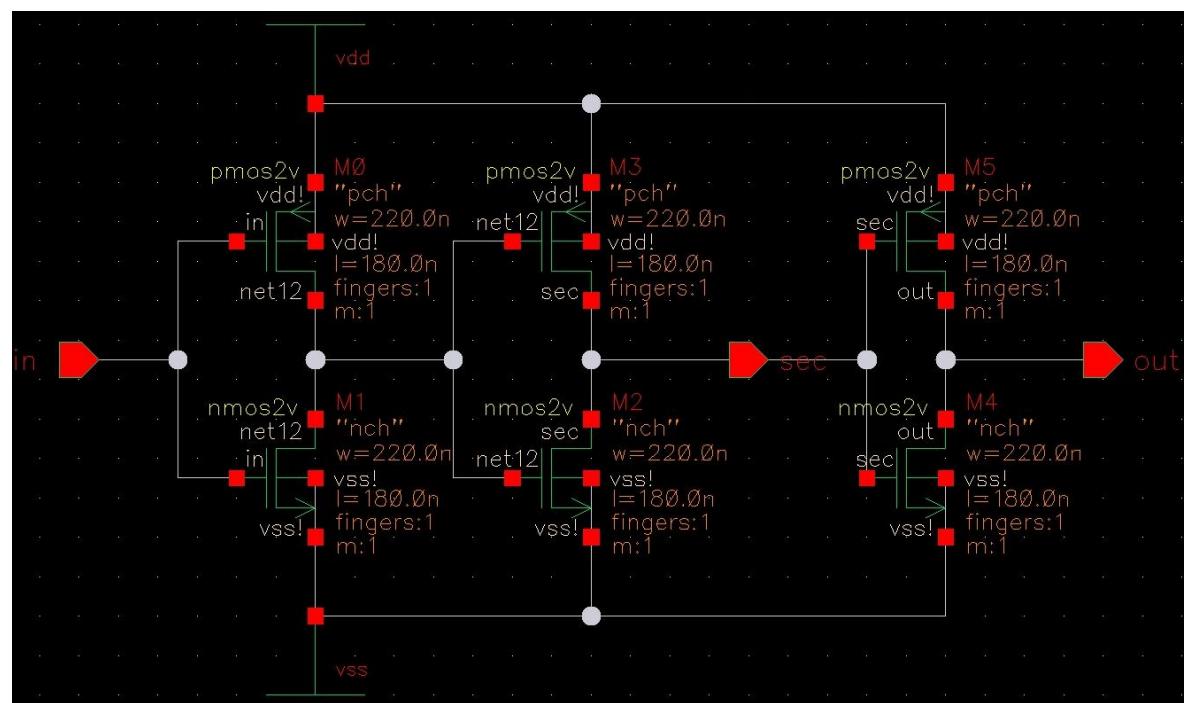
---

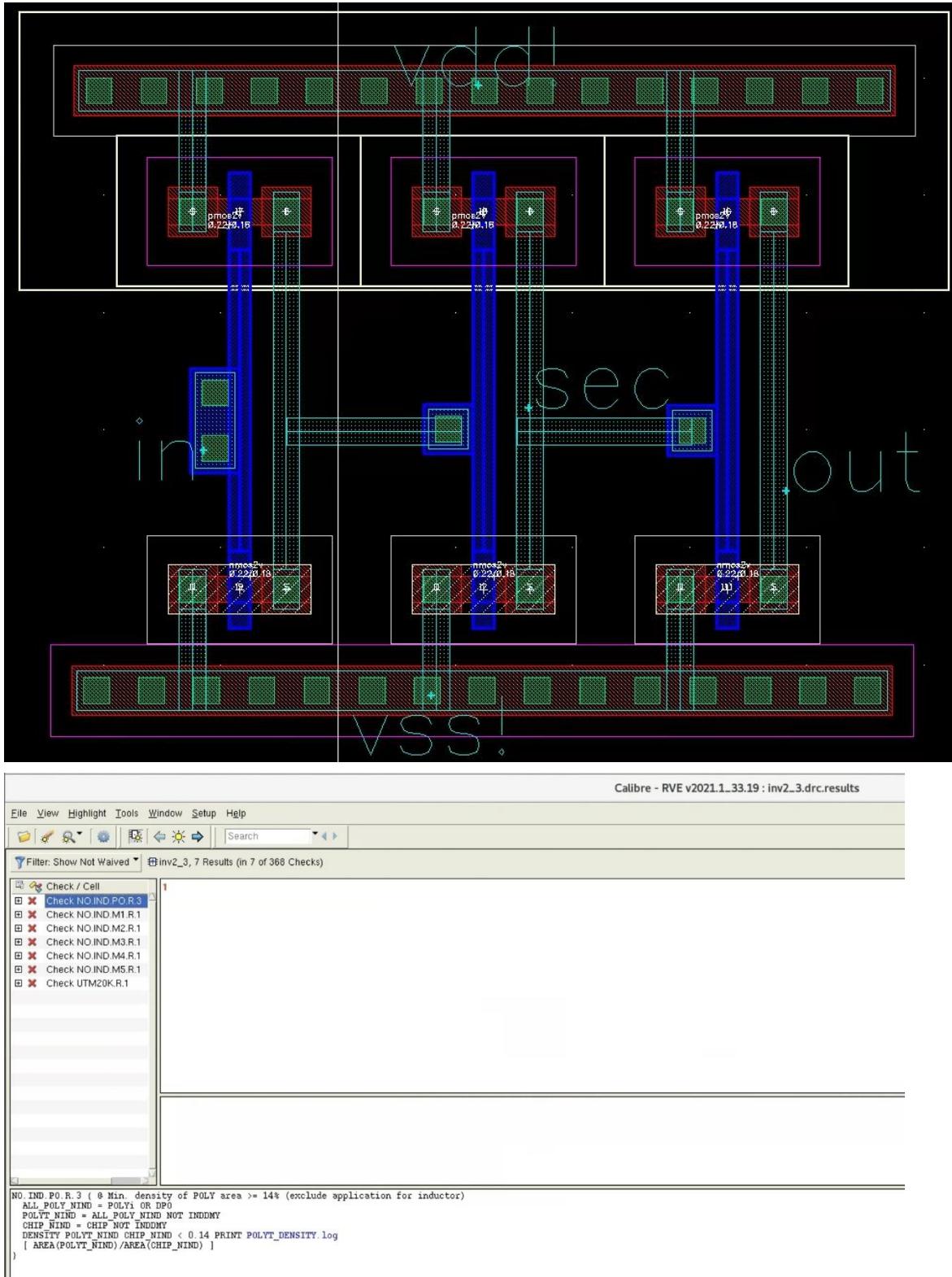
```
* File: inv2.pex.sp
* Created: Mon Oct 14 00:18:14 2024
* Program "Calibre xRC"
* Version "v2021.1_33.19"
*
.include "inv2.pex.sp.pex"
.subckt INV2 IN VSS! VDD! OUT
*
* OUT OUT
* VDD! VDD!
* VSS! VSS!
* IN IN
M0 N_OUT_M0_d N_IN_M0_g N_VSS!_M0_s N_VSS!_M0_b nmos L=1.8e-07 W=2.2e-07
+ AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917 NRS=4.09917
M1 N_OUT_M1_d N_IN_M1_g N_VDD!_M1_s N_VDD!_M1_b pmos L=1.8e-07 W=2.2e-07
+ AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917 NRS=4.09917
*
.include "inv2.pex.sp.INV2.pxi"
*
.ends
*
```



(b) Cascade three copies of the above inverter.

Ans:





Calibre - RVE v2021.1\_33.19 : svdb inv2\_3

**Extraction Results:**

Layout Cell / Type	Source Cell	Count /	Nets	Instances	Ports
inv2_3	inv2_3	Clean	5L, 5S	2L, 2S	5L, 5S

**Cell inv2\_3 Summary (Clean)**

CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: inv2\_3  
SOURCE CELL NAME: inv2\_3

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	5	5	
Nets:	6	6	
Instances:	3	3	MN (4 pins)
	3	3	MP (4 pins)
Total Inst:	6	6	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	5	5	
Nets:	5	5	
Instances:	1	1	_inv_ (4 pins)

Calibre Interactive - PEX v2021.1\_33.19

**File Transcript Setup**

**PEX Configuration:**

```

pdb file name = svdb/INV2_3.pdb
root cell name = INV2_3
total nets = 6
top-level nets = 6
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0

```

**CALIBRE xRC WARNING / ERROR Summary:**

```

=====
xRC Warnings = 2
xRC Errors = 0
=====
```

**Completion Log:**

```

--- CALIBRE xRC::FORMATTER COMPLETED - Mon Oct 14 18:16:59 2024
--- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 8/9/73 MALLOC = 69/69.
```

**13 Warnings:**

- Please enable "throughput-performance" profile for best performance
- Please increase max process limit (4096) to system limit (511962)
- Please increase descriptors limit for best performance (4096)
- Please enable "throughput-performance" profile for best performance
- Please increase max process limit (4096) to system limit (511962)
- Please increase descriptors limit for best performance (4096)

- (c) Apply an ideal square wave (that is, both rise and fall times are set to 0 ns) with the 50% duty cycle of an appropriate frequency to the input of the first stage and measure the propagation delay of the second stage.

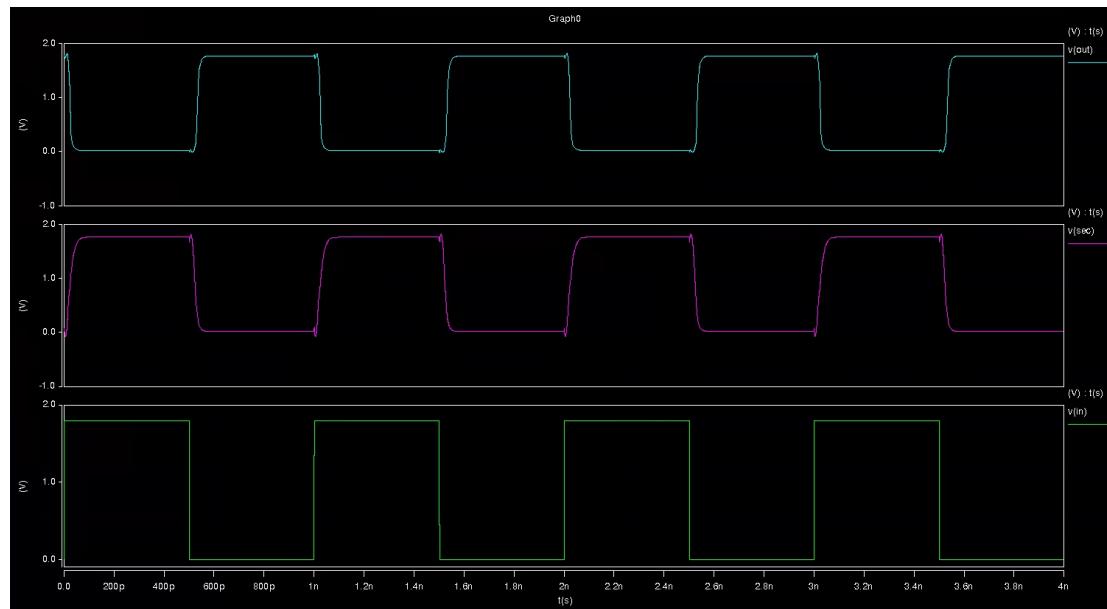
Ans:

```

.SUBCKT inv2_3 in out sec
MM4 out sec vss! vss! nmos l=180.0n w=220.0n m=1
MM2 sec net12 vss! vss! nmos l=180.0n w=220.0n m=1
MM1 net12 in vss! vss! nmos l=180.0n w=220.0n m=1
MM5 out sec vdd! vdd! pmos l=180.0n w=220.0n m=1
MM3 sec net12 vdd! vdd! pmos l=180.0n w=220.0n m=1
MM0 net12 in vdd! vdd! pmos l=180.0n w=220.0n m=1
.ENDS

.lib "PTM180.l" cmos
xinv in out sec inv2_3
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0n 0n 0.5n 1n)
.trans 1ps 4ns
.measure tpLH *rising propagation delay
+ trig V(in) val=0.9 rise=2
+ targ V(sec) val=0.9 rise=2
.measure tpHL *falling propagation delay
+ trig V(in) val=0.9 fall=2
+ targ V(sec) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'
.probe tran V(in) V(sec)
.option post
.end

```



```

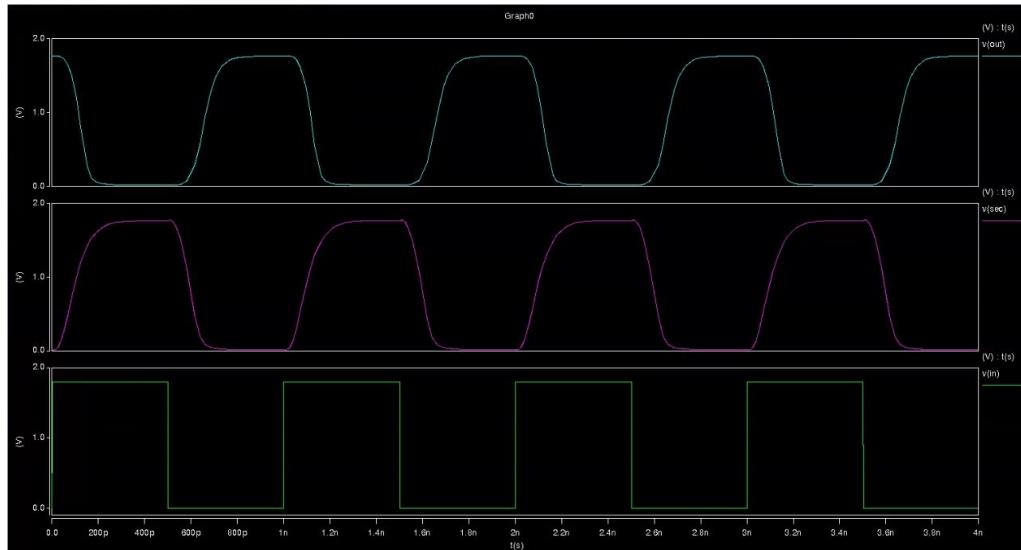
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE ****
tplh          tphl          tpd          temper
alter#
 2.4799e-11    2.2833e-11    2.3816e-11    25.00000
1

```

```

* File: inv2_3.pex.sp
* Created: Mon Oct 14 18:16:59 2024
* Program "Calibre xRC"
* Version "v2021.1_33.19"
*
.include "inv2_3.pex.sp.pex"
.subckt INV2_3 IN SEC VSS! VDD! OUT
*
* OUT    OUT
* VDD!  VDD!
* VSS!  VSS!
* SEC    SEC
* IN     IN
mX0/M0 N_2_X0/M0_d N_IN X0/M0_g N_VDD!_X0/M0_s N_VDD!_X0/M0_b pmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
mX1/M0 N_SEC_X1/M0_d N_2_X1/M0_g N_VDD!_X1/M0_s N_VDD!_X0/M0_b pmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
mX2/M0 N_OUT_X2/M0_d N_SEC_X2/M0_g N_VDD!_X2/M0_s N_VDD!_X0/M0_b pmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
mX3/M0 N_VSS!_X3/M0_d N_IN X3/M0_g N_2_X3/M0_s N_VSS!_X3/M0_b nmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
mX4/M0 N_VSS!_X4/M0_d N_2_X4/M0_g N_SEC_X4/M0_s N_VSS!_X3/M0_b nmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
mX5/M0 N_VSS!_X5/M0_d N_SEC_X5/M0_g N_OUT_X5/M0_s N_VSS!_X3/M0_b nmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
*
.include "inv2_3.pex.sp.INV2_3.pxi"
*
.ends

```



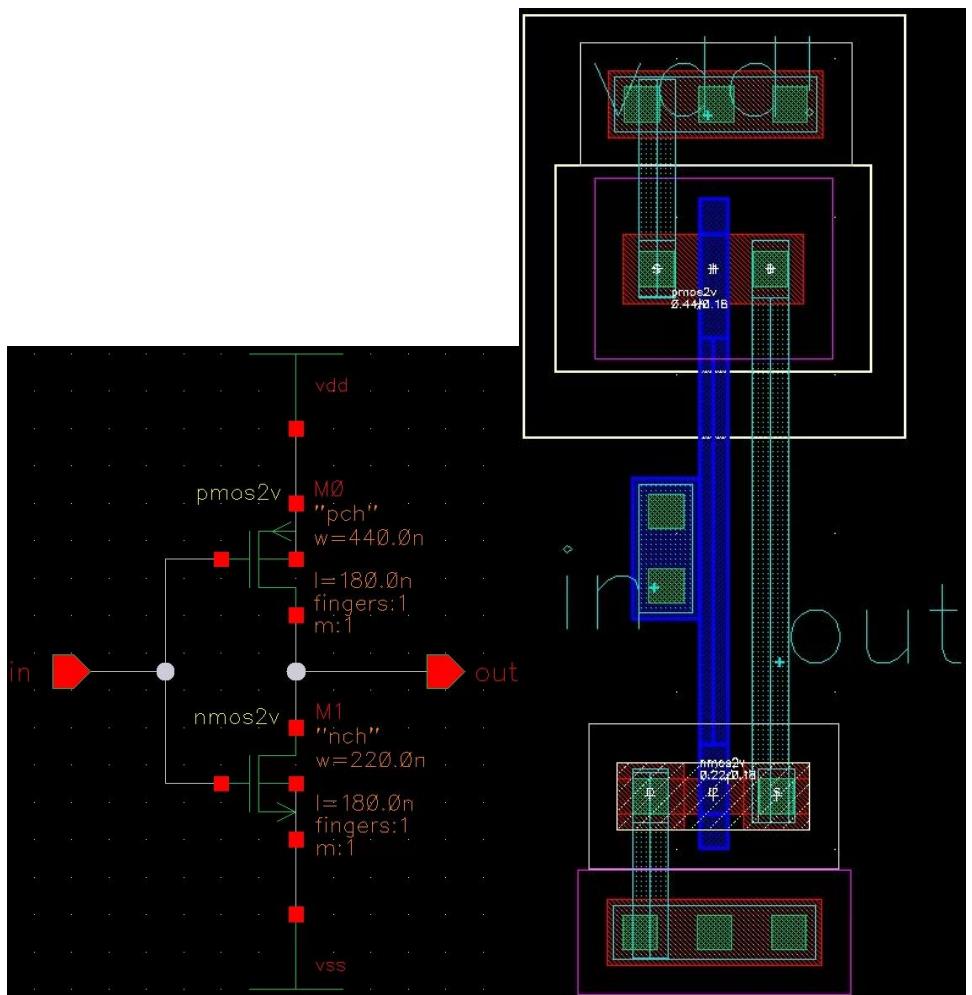
```

$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '* File: inv2_3.pex.sp'
tplh          tphl          tpd          temper
alter#
 6.4680e-11   2.0390e-11   4.2535e-11   25.00000
1

```

- (d) Repeat above steps with the following circuit parameters:  $W_n = W_{min}$  and  $W_p = 2W_{min}$ .

Ans:

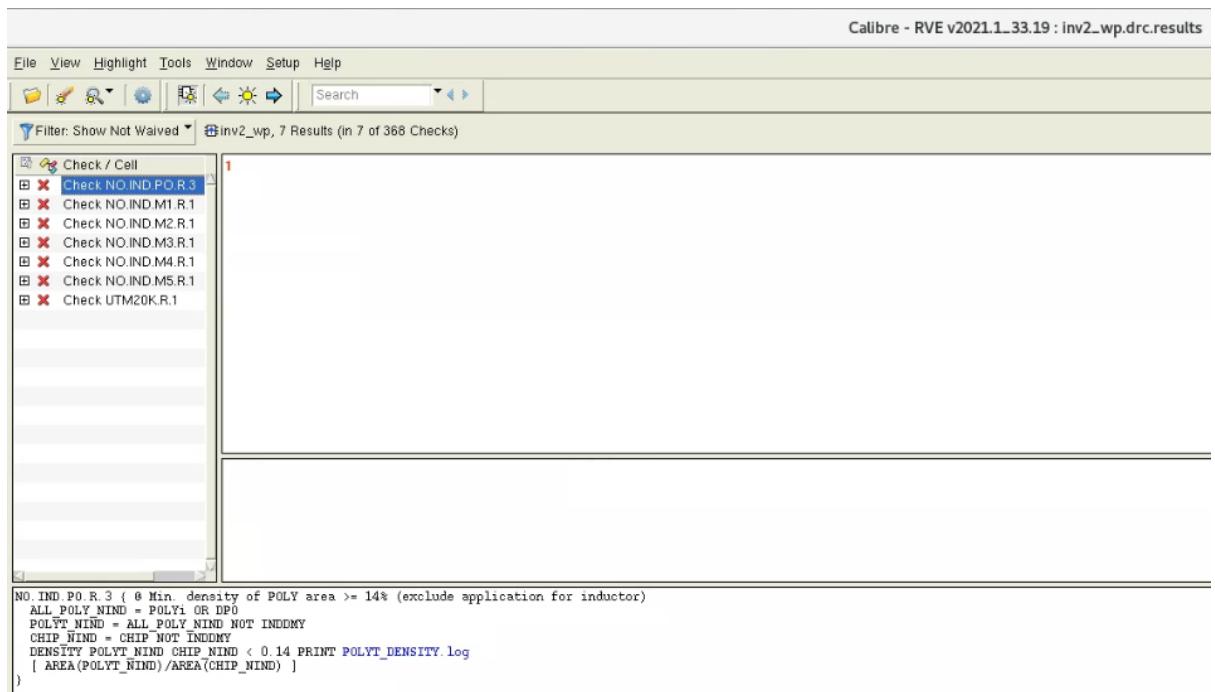
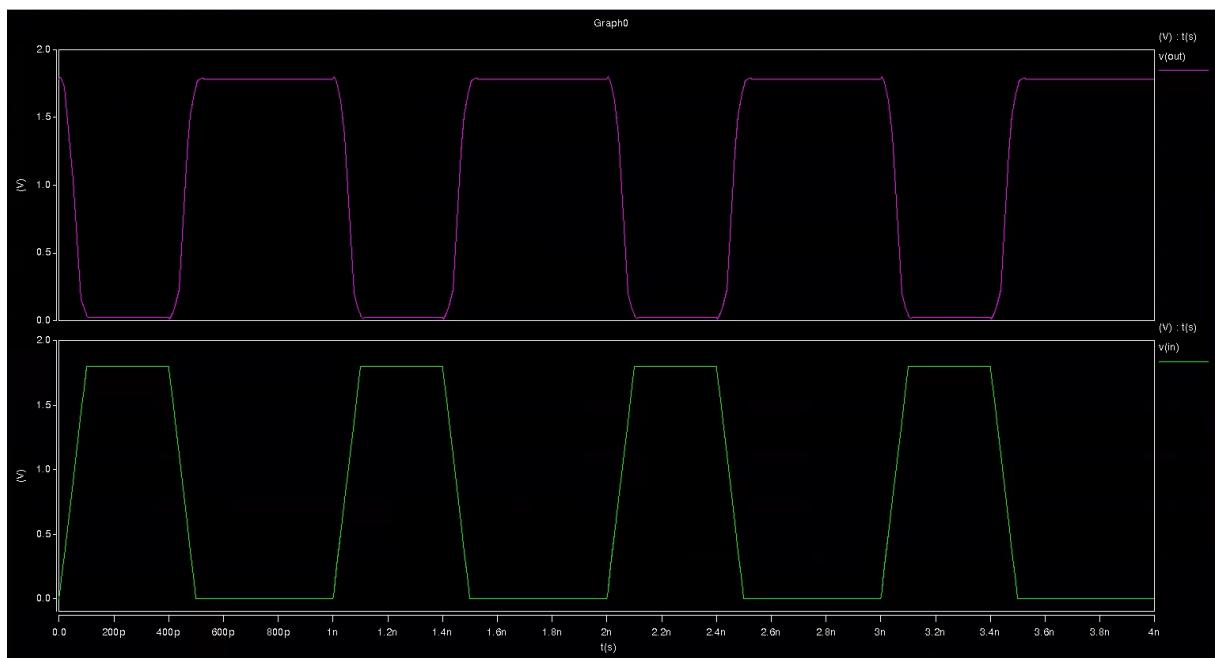


```

.SUBCKT inv2_wp in out
*.PININFO in:I out:0
MM1 out in vss! vss! nmos l=180.0n w=220.0n m=1
MM0 out in vdd! vdd! pmos l=180.0n w=440.0n m=1
.ENDS

.lib "PTM180.l" cmos
xinv in out inv2_wp
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0.1n 0.1n 0.3n 1n)
.trans 1ps 4ns
.measure tpLH *rising propagation delay
+ trig V(in) val=0.9 fall=2
+ targ V(out) val=0.9 rise=2
.measure tpHL *falling propagation delay
+ trig V(in) val=0.9 rise=2
+ targ V(out) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'
.probe tran V(in) V(out)
.option post=2
.end

```



Calibre - RVE v2021.1\_33.19 : svdb inv2\_wp

File View Highlight Tool Window Setup Help

Navigator | Info | Extraction Results | Comparison Results |

**Results**

- ERC Results
- ERC Patchk Polygons
- ERC Summary
- ERC Patchk Nets Repo

**Reports**

- Extraction Report
- LVS Report

**Rules**

- Rules File

**View**

- Info
- Finder
- Schematics

**Setup**

- Options

**Extraction Results**

Cell inv2\_wp Summary (Clean)

CELL COMPARISON RESULTS ( TOP LEVEL )

LAYOUT CELL NAME: inv2\_wp  
SOURCE CELL NAME: inv2\_wp

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	4	4	
Nets:	4	4	
Instances:	1	1	MP (4 pins)
	1	1	MP (4 pins)
Total Inst:	2	2	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	4	4	
Nets:	4	4	
Instances:	1	1	_invv (4 pins)

Calibre Interactive - PEX v2021.1\_33.19

File Transcript Setup Help

**Rules**

**Inputs**

**Outputs**

**Run Control**

**Transcript**

**Run PEX**

**Start RVE**

```

pdb file name =      svdb/INV2_WP.pdb
root cell name =    INV2_WP
total nets =         4
top-level nets =    4
non-top-level nets = 0
degenerate nets =   0
merged nets =        0
error nets =         0

=====
CALIBRE xRC WARNING / ERROR Summary
-----
xRC Warnings = 2
xRC Errors = 0
=====

--- CALIBRE xRC::FORMATTER COMPLETED - Mon Oct 14 21:49:50 2024
--- TOTAL CPU TIME = 0  REAL TIME = 0  LVHEAP = 8/9/73  MALLOC = 68/68.


```

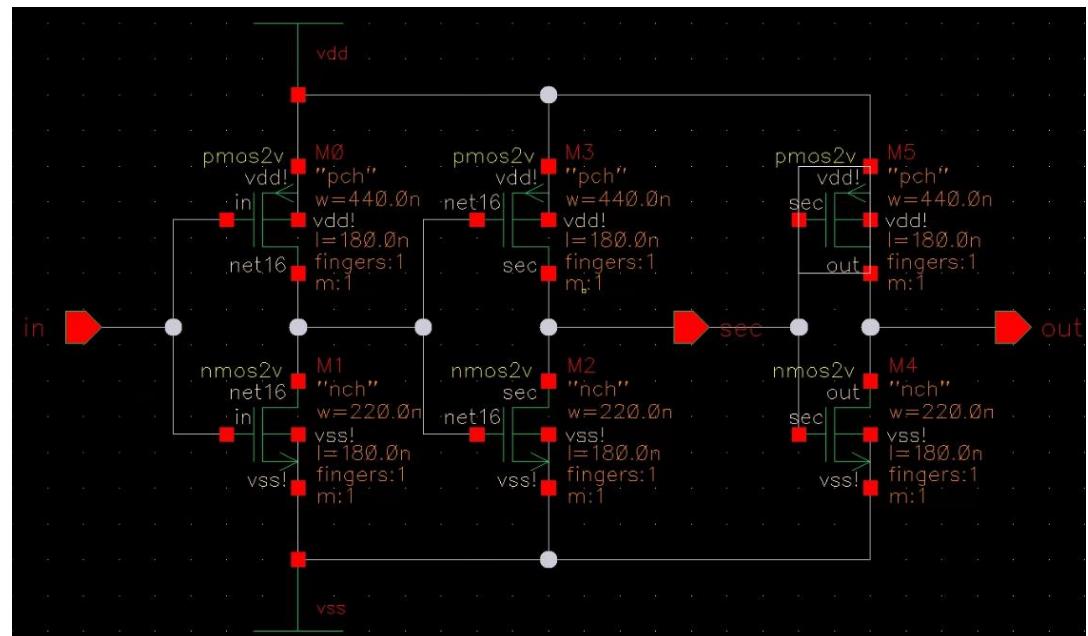
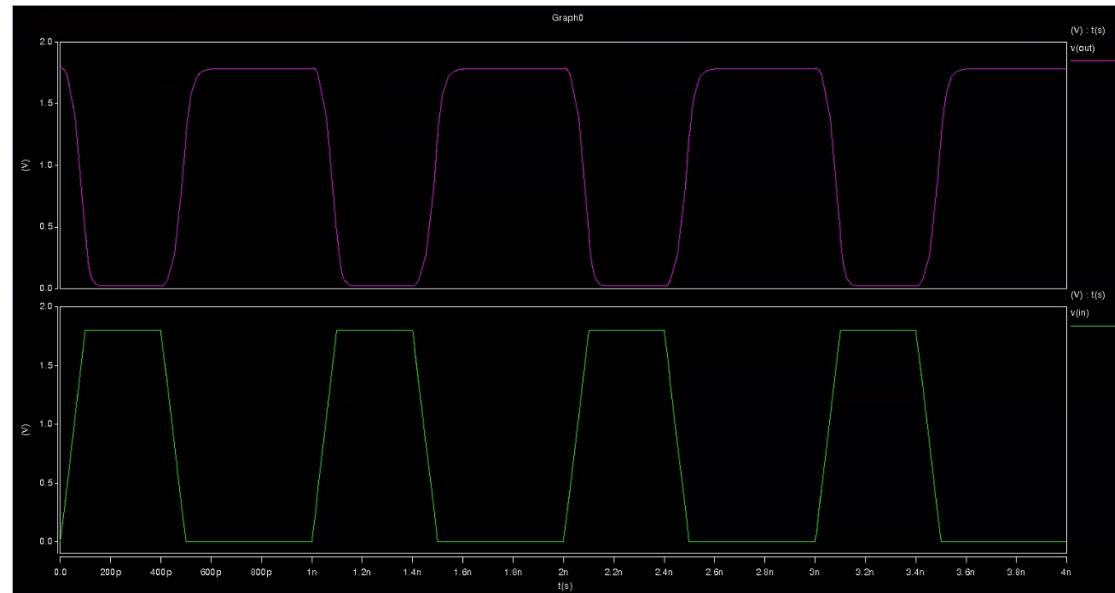
**13 Warnings**

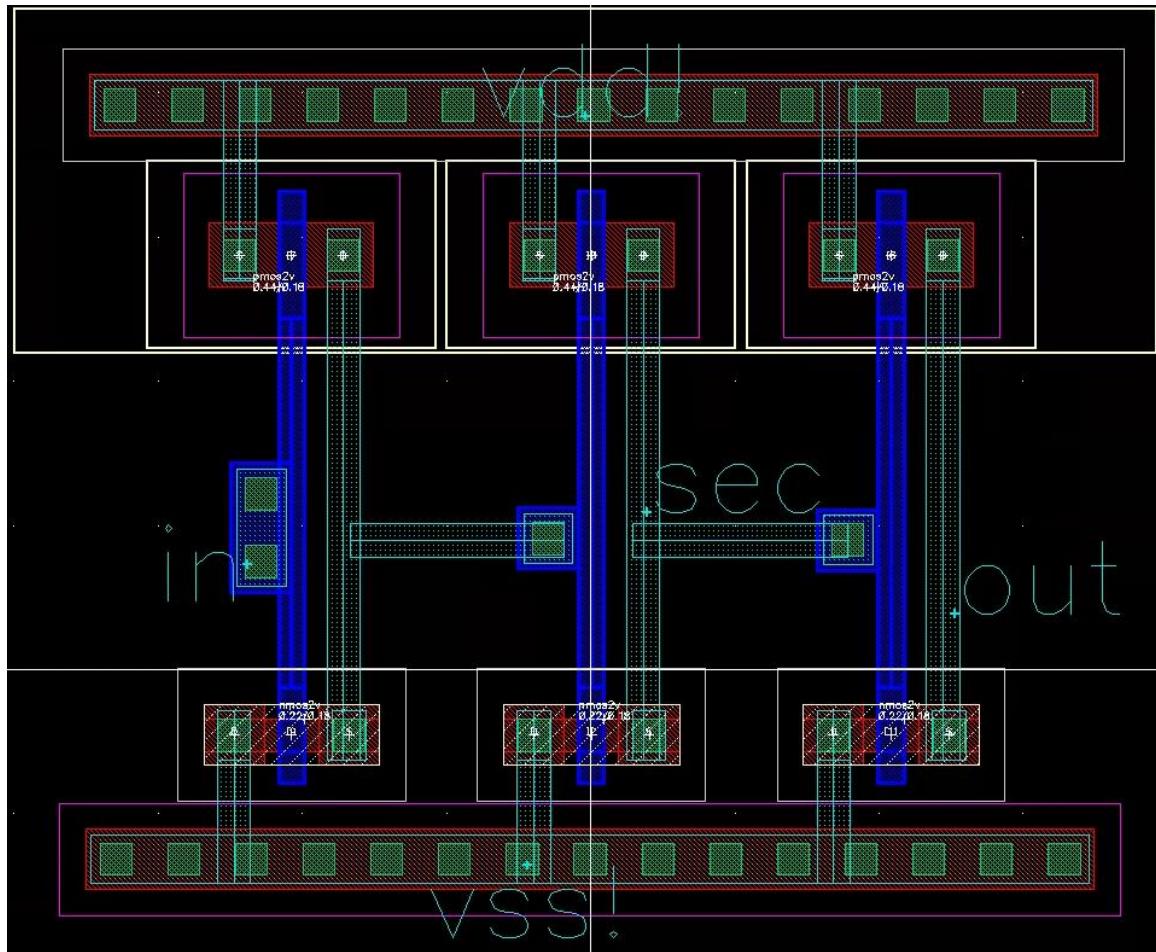
Please enable "throughput-performance" profile for best performance  
Please increase max process limit (4096) to system limit (511962)  
Please increase descriptors limit for best performance (4096)  
Please enable "throughput-performance" profile for best performance  
Please increase max process limit (4096) to system limit (511962)  
Please increase descriptors limit for best performance (4096)

```

* File: inv2_wp.pex.sp
* Created: Mon Oct 14 21:49:50 2024
* Program "Calibre xRC"
* Version "v2021.1_33.19"
*
.include "inv2_wp.pex.sp.pex"
.subckt INV2_WP IN VSS! VDD! OUT
*
* OUT OUT
* VDD! VDD!
* VSS! VSS!
* IN IN
M0 N_OUT_M0_d N_IN_M0_g N_VSS! M0_s N_VSS! M0_b nmos L=1.8e-07 W=2.2e-07
+ AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917 NRS=4.09917
M1 N_OUT_M1_d N_IN_M1_g N_VDD! M1_s N_VDD! M1_b pmos L=1.8e-07 W=4.4e-07
+ AD=2.112e-13 AS=2.112e-13 PD=1.84e-06 PS=1.84e-06 NRD=1.09091 NRS=1.09091
*
.include "inv2_wp.pex.sp.INV2_WP.pxi"
*
.ends
*

```





Calibre - RVE v2021.1\_33.19 : inv2\_3\_wp.drc.results

File View Highlight Tools Window Setup Help

Filter: Show Unresolved ▾ inv2\_3\_wp, 7 Results (in 7 of 368 Checks)

Check / Cell
<input checked="" type="checkbox"/> Check NO_IND.PO.R.3
<input checked="" type="checkbox"/> Check NO_IND.M1.R.1
<input checked="" type="checkbox"/> Check NO_IND.M2.R.1
<input checked="" type="checkbox"/> Check NO_IND.M3.R.1
<input checked="" type="checkbox"/> Check NO_IND.M4.R.1
<input checked="" type="checkbox"/> Check NO_IND.M5.R.1
<input checked="" type="checkbox"/> Check UTM20K.R.1

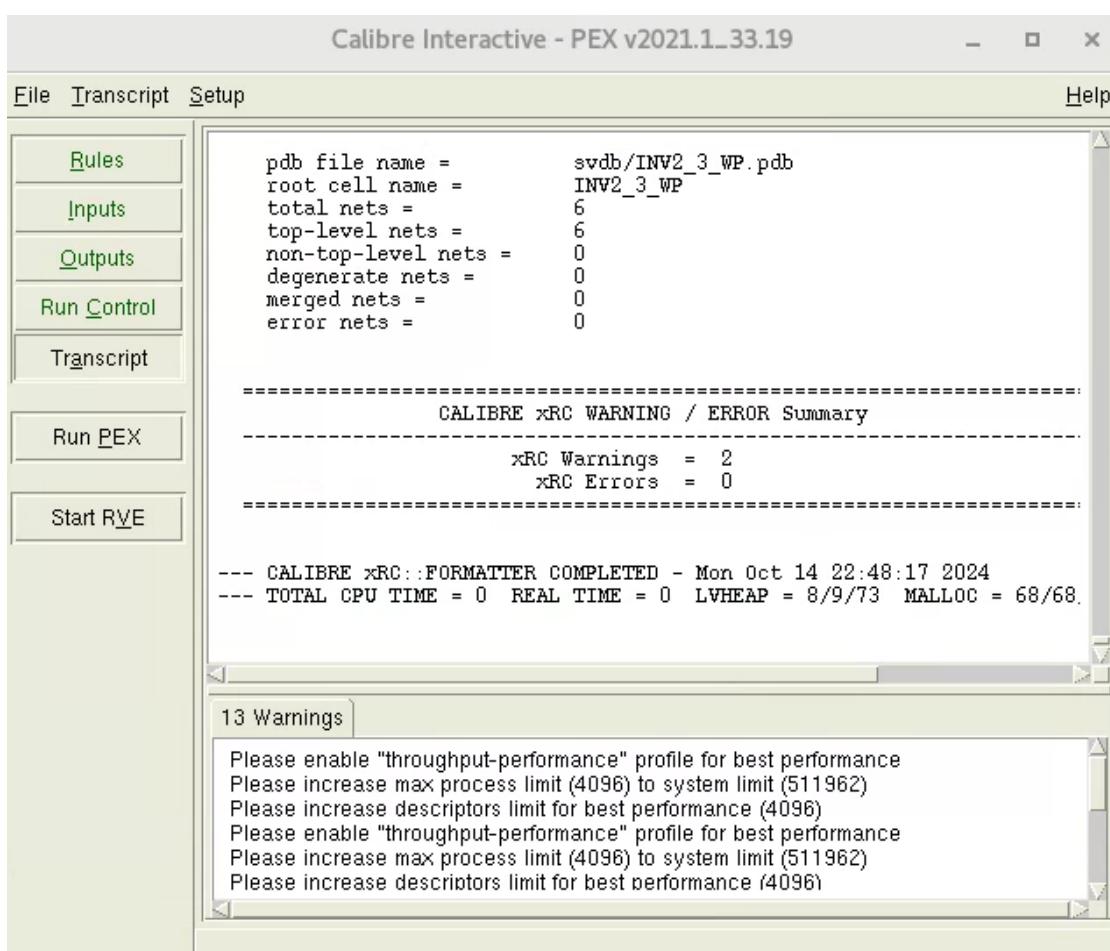
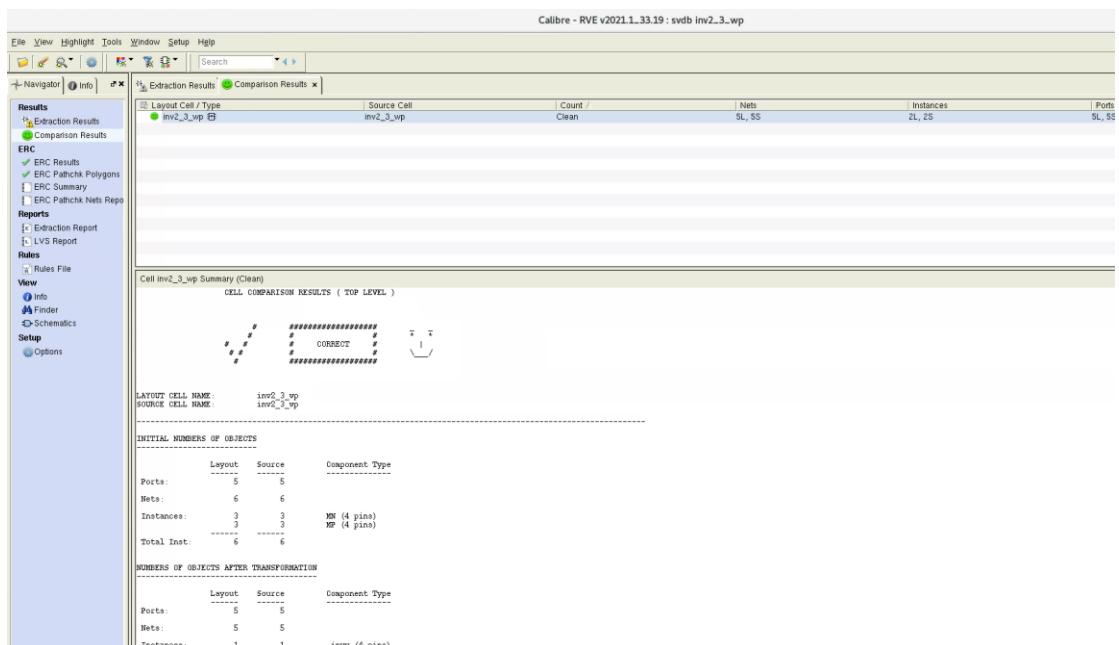
1

---

```

NO_IND.PO.R.3 { @ Min. density of POLY area >= 14% (exclude application for inductor)
    ALL_POLY_NIND = POLYi OR DPO
    POLYT_NIND = ALL_POLY_NIND NOT INDDMY
    CHIP_NIND = CHIP NOT INDDMY
    DENSITY POLYT_NIND CHIP_NIND < 0.14 PRINT POLYT_DENSITY.log
    [ AREA(POLYT_NIND)/AREA(CHIP_NIND) ]
}

```

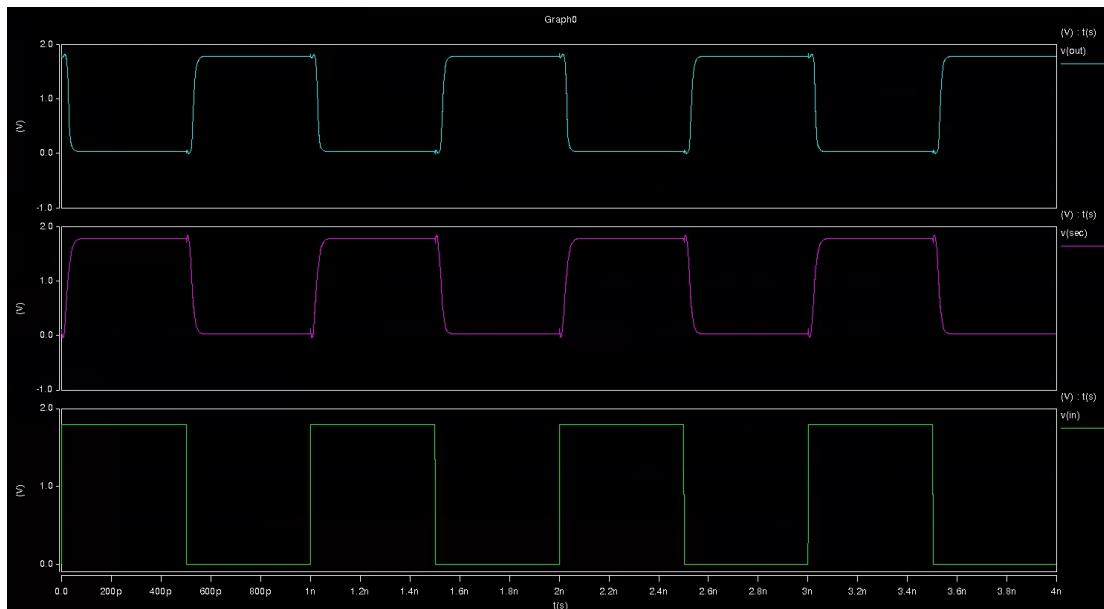


```

.SUBCKT inv2_3_wp in out sec
*.PININFO in:I out:O sec:O
MM0 net16 in vdd! vdd! pmos l=180.0n w=440.0n m=1
MM3 sec net16 vdd! vdd! pmos l=180.0n w=440.0n m=1
MM5 out sec vdd! vdd! pmos l=180.0n w=440.0n m=1
MM1 net16 in vss! vss! nmos l=180.0n w=220.0n m=1
MM2 sec net16 vss! vss! nmos l=180.0n w=220.0n m=1
MM4 out sec vss! vss! nmos l=180.0n w=220.0n m=1
.ENDS

.lib "PTM180.l" cmos
xinv in out sec inv2_3_wp
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0n 0n 0.5n 1n)
.trans lps 4ns
.measure tpLH *rising propagation delay
+ trig V(in) val=0.9 rise=2
+ targ V(sec) val=0.9 rise=2
.measure tpHL *falling propagation delay
+ trig V(in) val=0.9 fall=2
+ targ V(sec) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'
.probe tran V(in) V(sec)
.option post
.end

```



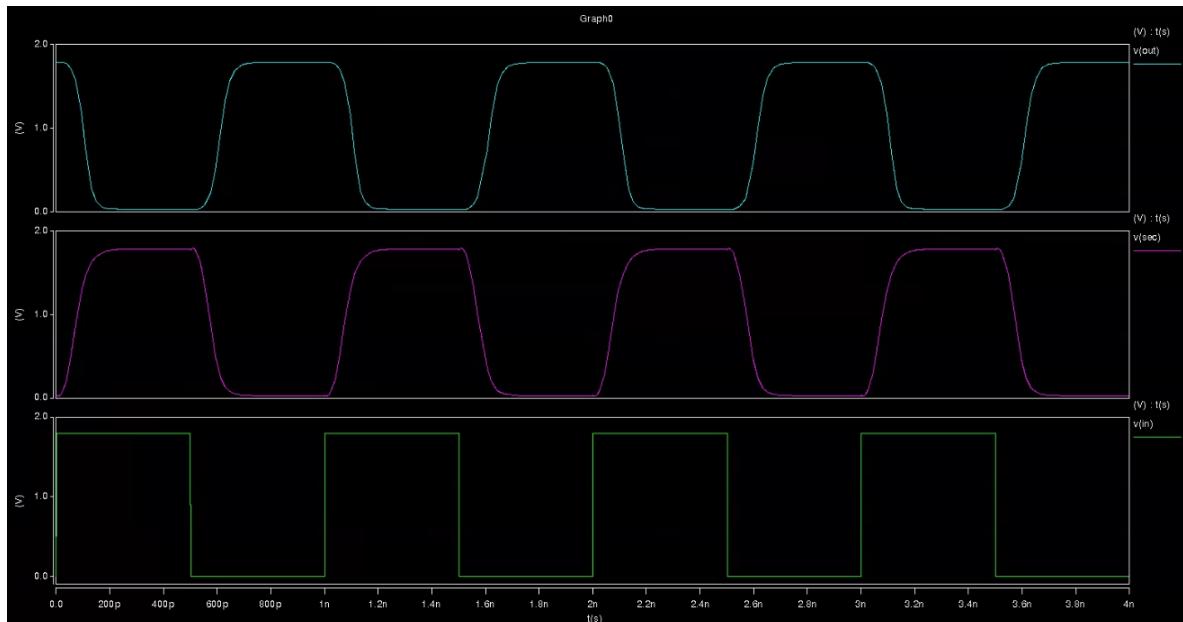
```

$DATA1 SOURCE='PrimeSim HSPICE' VERSION='5-2021.09' PARAM_COUNT=0
.TITLE ****
tphl          tphl          tpd          temper
alter#
2.4198e-11    2.4504e-11    2.4351e-11    25.00000
1

```

```

* File: inv2_3_wp.pex.sp
* Created: Mon Oct 14 22:48:17 2024
* Program "Calibre xRC"
* Version "v2021.1_33.19"
*
.include "inv2_3_wp.pex.sp.pex"
.subckt INV2_3_WP IN SEC VSS! VDD! OUT
*
* OUT OUT
* VDD! VDD!
* VSS! VSS!
* SEC SEC
* IN IN
mX0/M0 N_2_X0/M0_d N_IN_X0/M0_g N_VDD!_X0/M0_s N_VDD!_X0/M0_b pmos L=1.8e-07
+ W=4.4e-07 AD=2.112e-13 AS=2.112e-13 PD=1.84e-06 PS=1.84e-06 NRD=1.09091
+ NRS=1.09091
mX1/M0 N_SEC_X1/M0_d N_2_X1/M0_g N_VDD!_X1/M0_s N_VDD!_X0/M0_b pmos L=1.8e-07
+ W=4.4e-07 AD=2.112e-13 AS=2.112e-13 PD=1.84e-06 PS=1.84e-06 NRD=1.09091
+ NRS=1.09091
mX2/M0 N_OUT_X2/M0_d N_SEC_X2/M0_g N_VDD!_X2/M0_s N_VDD!_X0/M0_b pmos L=1.8e-07
+ W=4.4e-07 AD=2.112e-13 AS=2.112e-13 PD=1.84e-06 PS=1.84e-06 NRD=1.09091
+ NRS=1.09091
mX3/M0 N_VSS!_X3/M0_d N_IN_X3/M0_g N_2_X3/M0_s N_VSS!_X3/M0_b nmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
mX4/M0 N_VSS!_X4/M0_d N_2_X4/M0_g N_SEC_X4/M0_s N_VSS!_X3/M0_b nmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
mX5/M0 N_VSS!_X5/M0_d N_SEC_X5/M0_g N_OUT_X5/M0_s N_VSS!_X3/M0_b nmos L=1.8e-07
+ W=2.2e-07 AD=1.984e-13 AS=1.984e-13 PD=1.88e-06 PS=1.88e-06 NRD=4.09917
+ NRS=4.09917
*
.include "inv2_3_wp.pex.sp.INV2_3_WP.pxi"
*
.ends
*
```



```

$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '* File: inv2_3_wp.pex.sp'
tplh          tphl          tpd          temper
alter#
  3.5356e-11    3.0511e-11    3.2934e-11    25.00000
1

```

## (e) Compare both results and give your comments.

Ans:

pMOS:220 nm nMOS:220 nm

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE ****
      tplh          tphl          tpd          temper
      alter#
      2.4799e-11    2.2833e-11    2.3816e-11   25.00000
1
```

pMOS:440 nm nMOS:220 nm

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE ****
      tplh          tphl          tpd          temper
      alter#
      2.4198e-11    2.4504e-11    2.4351e-11   25.00000
1
```

因為  $R_n = R_{eqn} * (L/W)_n$  、  $R_p = R_{eqp} * (L/W)_p$ ，所以當  $W$  越大  $R$  則越小，

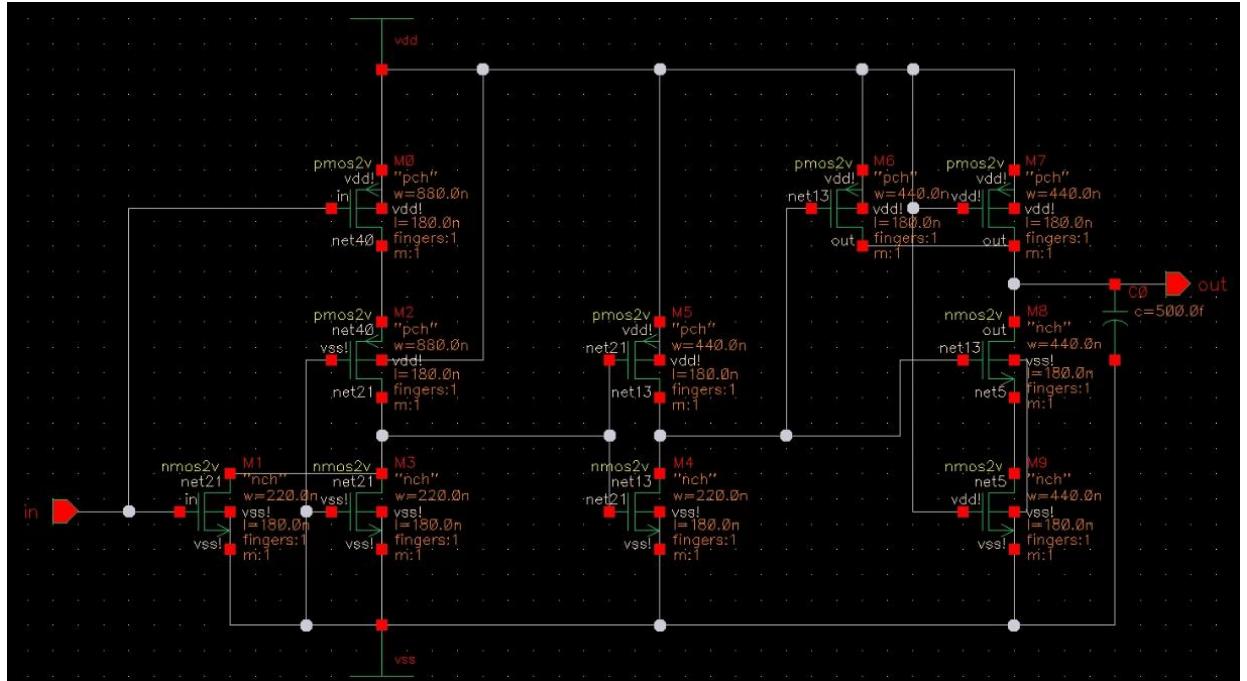
但  $C_{gs} = 1/2(C_{ox} * W * L)$ ，所以當  $W$  變大時  $C$  也會跟著變大，

所以 Delay 的變化不大。

## 2. (A study of path delays)

- (a) Draw the schematic diagram of a three-stage logic circuit with a load capacitor of 0.5 pF. The output of the two-input NOR gate is connected to an inverter and the output of the inverter is in turn connected to one input of a two-input NAND gate. The output of the NAND gate drives the load capacitor. Suppose that the channel lengths and widths of all transistors are set as follows:  $L_{\text{all gates}} = L_{\min}$ ,  $W_p(\text{NOR}) = 4W_{\min}$ ,  $W_p(\text{NOT}) = 2W_{\min}$ ,  $W_p(\text{NAND}) = 2W_{\min}$ ,  $W_n(\text{NOR}) = W_{\min}$ ,  $W_n(\text{NOT}) = W_{\min}$ ,  $W_n(\text{NAND}) = 2W_{\min}$ . The unused inputs of the NAND and NOR gates are connected to  $V_{DD}$  and ground, respectively.

Ans:

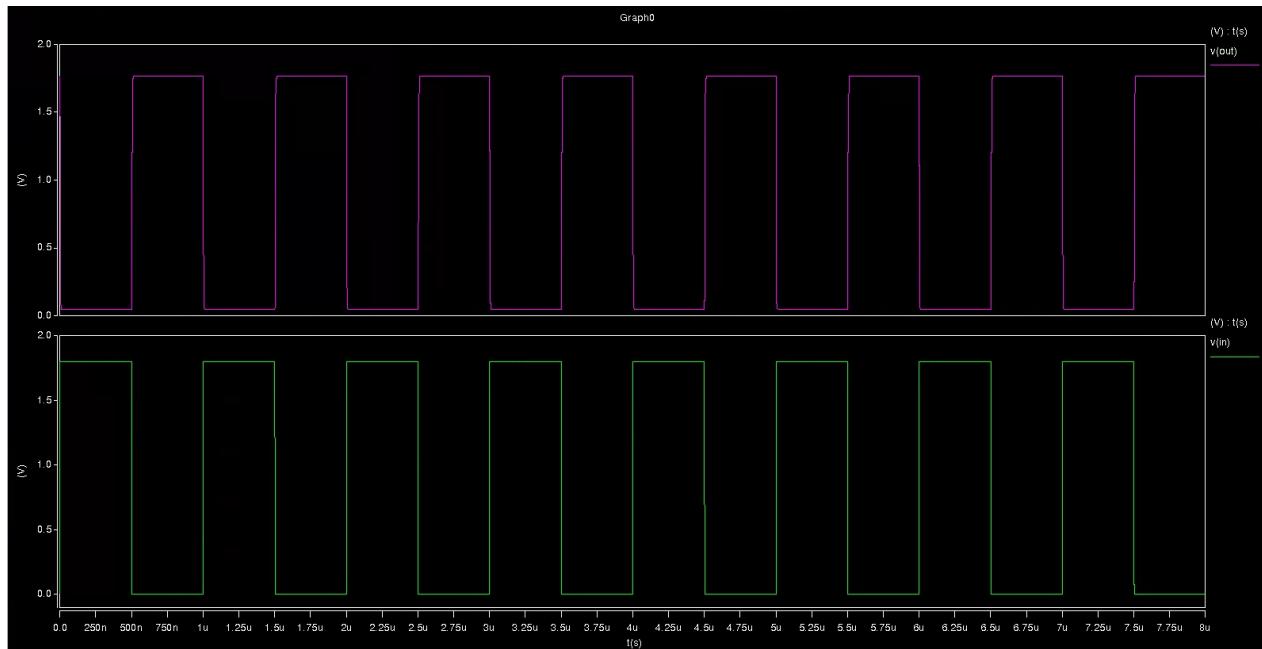


- (b) Apply an ideal square wave (that is, both rise and fall times are set to 0 ns) of an appropriate frequency to the input of the first stage, and measure both  $t_{PLH}$  and  $t_{PHL}$  of the output of the last stage.

Ans:

```
.SUBCKT tri_state in out
*.PININFO in:I out:0
CC0 out vss! 500.0f $[CP]
MM9 net5 vdd! vss! vss! nmos l=180.0n w=440.0n m=1
MM8 out net13 net5 vss! nmos l=180.0n w=440.0n m=1
MM4 net13 net21 vss! vss! nmos l=180.0n w=220.0n m=1
MM3 net21 vss! vss! vss! nmos l=180.0n w=220.0n m=1
MM1 net21 in vss! vss! nmos l=180.0n w=220.0n m=1
MM7 out vdd! vdd! vdd! pmos l=180.0n w=440.0n m=1
MM6 out net13 vdd! vdd! pmos l=180.0n w=440.0n m=1
MM5 net13 net21 vdd! vdd! pmos l=180.0n w=440.0n m=1
MM2 net21 vss! net40 vdd! pmos l=180.0n w=880.0n m=1
MM0 net40 in vdd! vdd! pmos l=180.0n w=880.0n m=1
.ENDS
```

```
*****add the following lines *****
.lib "PTM180.l" cmos
xt1 in out tri_state
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0n 0n 0.5u 1u)
.trans lns 8us
***** Output statements *****
.measure tpLH * rising propagation delay
+ trig V(in) val=0.9 fall=2
+ targ V(out) val=0.9 rise=2
.measure tpHL * falling propagation delay
+ trig V(in) val=0.9 rise=2
+ targ V(out) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'
.probe tran V(in) V(out)
.option post
.end
```

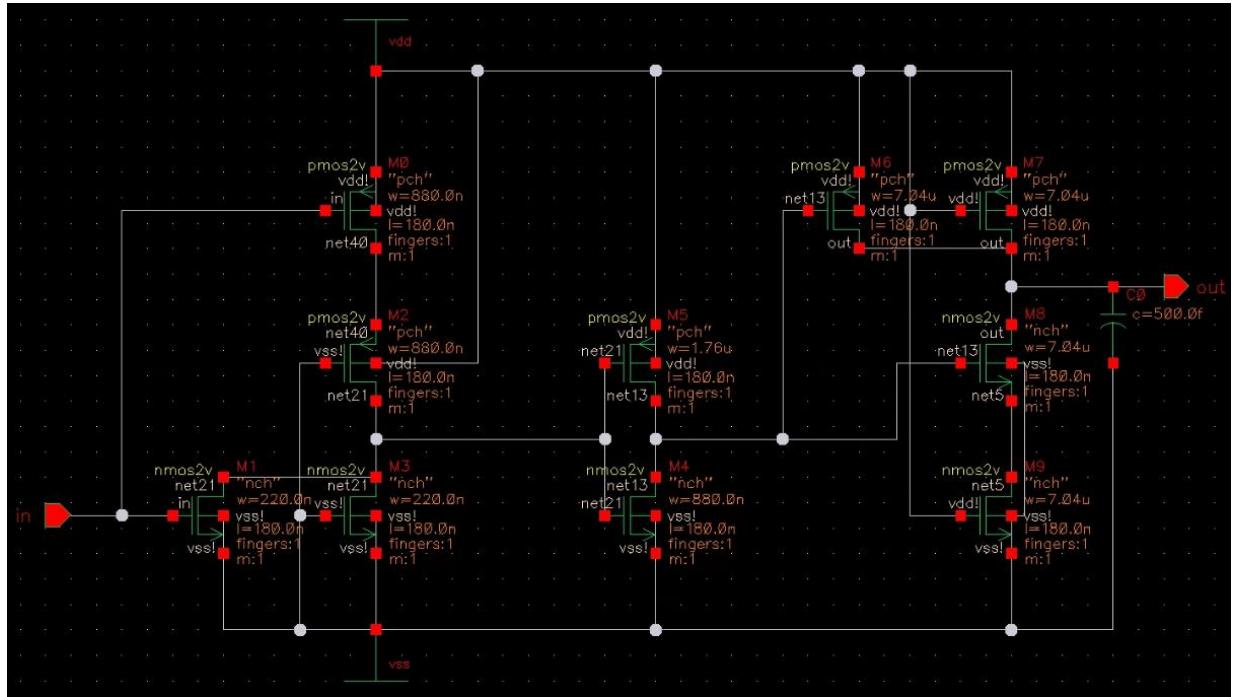



---

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE ****
.tplh          tphl          tpd          temper
alter#
2.2254e-09    1.7298e-09   1.9776e-09   25.00000
1
```

(c) (FO4 rule) Scale up the  $W$  of both pMOS and nMOS transistors for the second and last stages by factors of 4 and 16, respectively, and repeat the above step.

Ans:

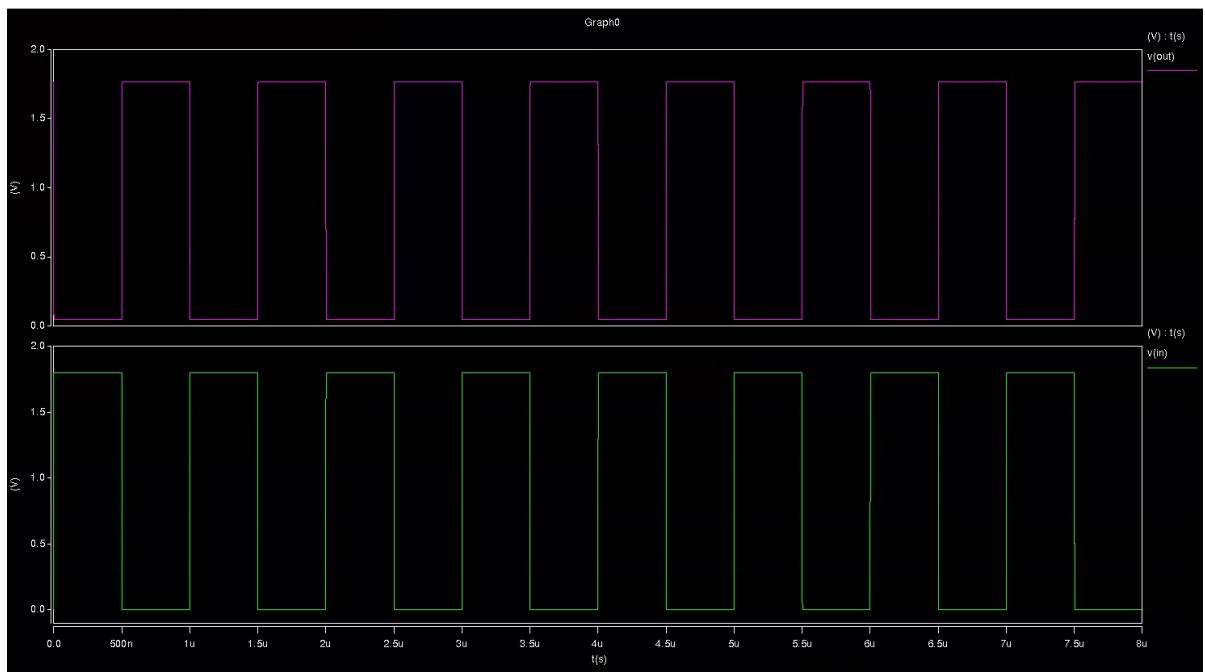


```

.SUBCKT tri_state in out
*.PININFO in:I out:O
CC0 out vss! 500.0f $[CP]
MM9 net5 vdd! vss! vss! nmos l=180.0n w=7.04u m=1
MM8 out net13 net5 vss! nmos l=180.0n w=7.04u m=1
MM4 net13 net21 vss! vss! nmos l=180.0n w=880.0n m=1
MM3 net21 vss! vss! vss! nmos l=180.0n w=220.0n m=1
MM1 net21 in vss! vss! nmos l=180.0n w=220.0n m=1
MM7 out vdd! vdd! pmos l=180.0n w=7.04u m=1
MM6 out net13 vdd! vdd! pmos l=180.0n w=7.04u m=1
MM5 net13 net21 vdd! vdd! pmos l=180.0n w=1.76u m=1
MM2 net21 vss! net40 vdd! pmos l=180.0n w=880.0n m=1
MM0 net40 in vdd! vdd! pmos l=180.0n w=880.0n m=1
.ENDS

*****add the following lines *****
.lib "PTM180.l" cmos
xtl in out tri_state
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0n 0n 0.5u 1u)
.trans ins 8us
***** Output statements *****
.measure tpLH * rising propagation delay
+ trig V(in) val=0.9 fall=2
+ targ V(out) val=0.9 rise=2
.measure tpHL * falling propagation delay
+ trig V(in) val=0.9 rise=2
+ targ V(out) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'
.probe tran V(in) V(out)
.option post
.end

```



```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE ****
.tphl          tphl          tpd          temper
alter#
 2.4574e-10    3.4927e-10    2.9750e-10    25.00000
1
```

(d) (Path-delay optimization) Use the method of path-delay optimization, scale up the  $W$  of both pMOS and nMOS transistors for each stage, and repeat the above step. Assume that  $C_{in} = C_g(W_n + W_p)$ .

Ans:

$$C_g = 3.45 \text{ fF}/\mu\text{m} [0.18 \mu\text{m}], C_{in} = C_g(W_n + W_p), C_{out} = 500 \text{ fF}/\mu\text{m}$$

$$\zeta_{NOR} = 5 R_{eqn} C_g L_n$$

$$\zeta_{NAND} = 4 R_{eqn} C_g L_n$$

$$\zeta_{NOT} = 3 R_{eqn} C_g L_n$$

$$\zeta_{NOR} = 5 C_g W_n$$

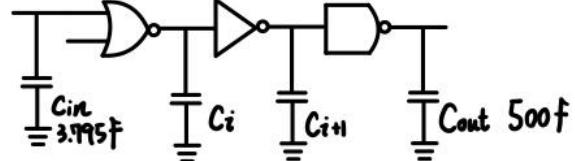
$$= 5 \times 3.45 \times 10^{-15} \times 0.22$$

$$= 3.795 \text{ fF}/\mu\text{m}$$

$$t_{stage} = \sqrt[3]{\zeta_{NOR} \times \zeta_{NOT} \times \zeta_{NAND} \times \left( \frac{C_{out}}{C_{in}} \right)}$$

$$= \sqrt[3]{5 \times 4 \times 3 \times \left( \frac{500}{3.795} \right)} R_{eqn} C_g L_n$$

$$= 19.92 R_{eqn} C_g L_n$$



$$\zeta_{NAND} \left( \frac{C_{out}}{C_{i+1}} \right) = 4 R_{eqn} C_g L_n \left( \frac{500 \text{ fF}}{C_{i+1}} \right) = 19.92 R_{eqn} C_g L_n$$

$$\Rightarrow C_{i+1} = 100.4 \text{ fF}/\mu\text{m} = 4 C_g W_n \Rightarrow W_n = W_p = 14.55 \mu\text{m}$$

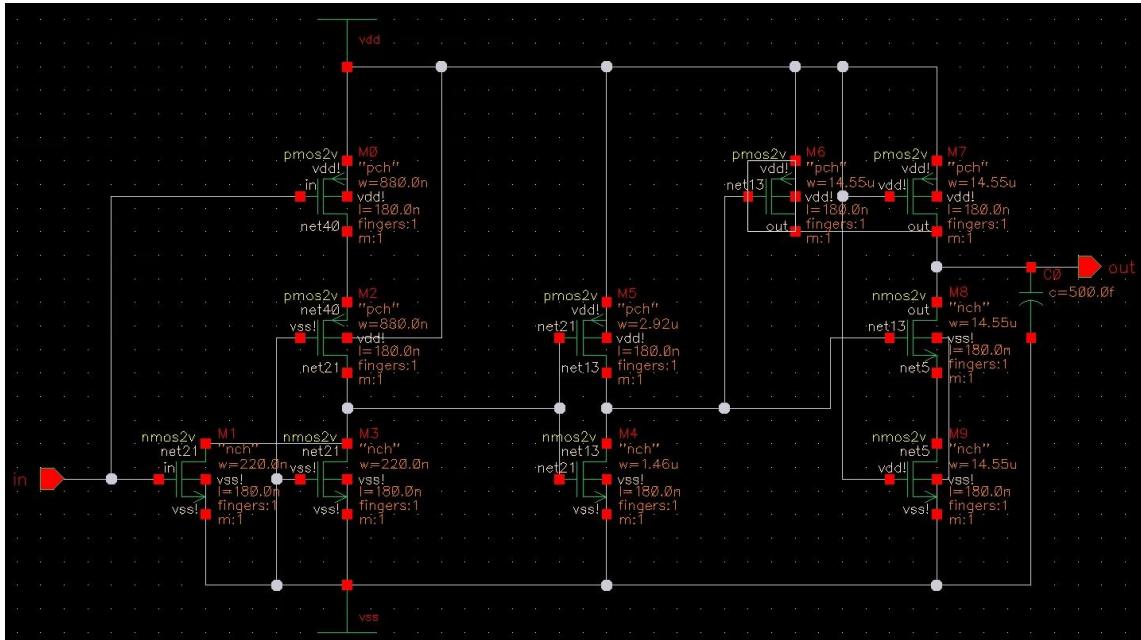
$$\zeta_{NOT} \left( \frac{C_{i+1}}{C_i} \right) = 3 R_{eqn} C_g L_n \left( \frac{100.4 \text{ fF}}{C_i} \right) = 19.92 R_{eqn} C_g L_n$$

$$\Rightarrow C_i = 15.12 \text{ fF}/\mu\text{m} = 3 C_g W_n \Rightarrow W_n = 1.461 \mu\text{m}, W_p = 2.922 \mu\text{m} \quad \# W_p = 2 W_n$$

$$\zeta_{NOR} \left( \frac{C_i}{C_{in}} \right) = 5 R_{eqn} C_g L_n \left( \frac{15.12 \text{ fF}}{C_{in}} \right) = 19.92 R_{eqn} C_g L_n$$

$$\Rightarrow C_{in} = 3.795 \text{ fF}/\mu\text{m} = 5 C_g W_n \Rightarrow W_n = 0.22 \mu\text{m}, W_p = 0.88 \mu\text{m}$$

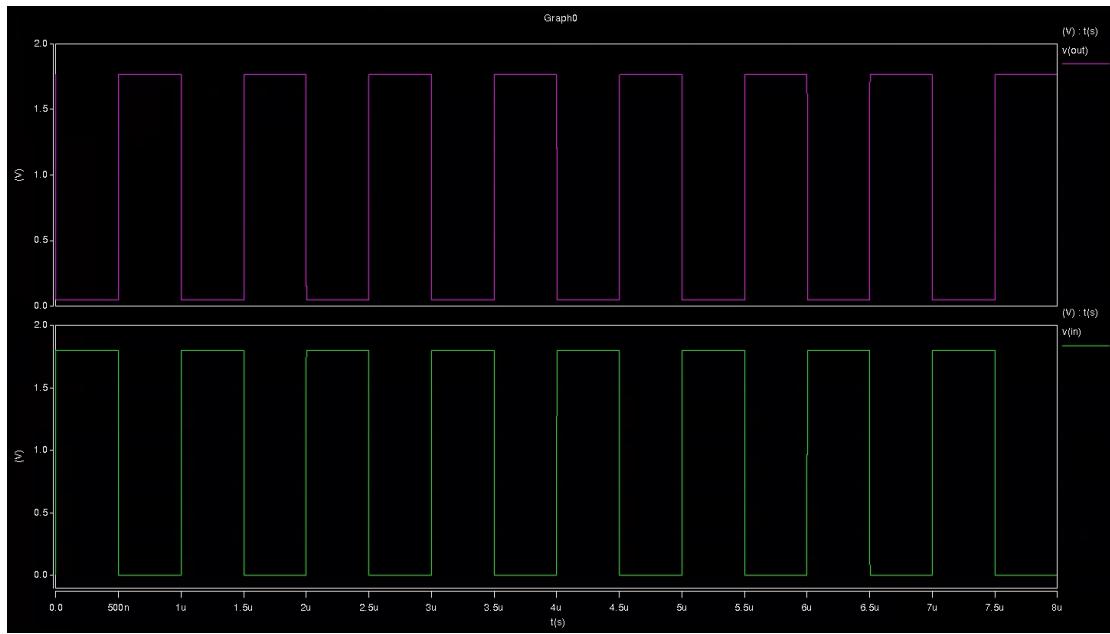
$\# NOR \quad W_p = 4 W_n$



```

* Library Name: vlsi
* Cell Name: tri_state
* View Name: schematic
*****
.SUBCKT tri_state in out
*.PININFO in:I out:0
CC0 out vss! 500.0f $[CP]
MM9 net5 vdd! vss! vss! nmos l=180.0n w=14.55u m=1
MM8 out net13 net5 vss! nmos l=180.0n w=14.55u m=1
MM4 net13 net21 vss! vss! nmos l=180.0n w=1.46u m=1
MM3 net21 vss! vss! vss! nmos l=180.0n w=220.0n m=1
MM1 net21 in vss! vss! nmos l=180.0n w=220.0n m=1
MM7 out vdd! vdd! vdd! pmos l=180.0n w=14.55u m=1
MM6 out net13 vdd! vdd! pmos l=180.0n w=14.55u m=1
MM5 net13 net21 vdd! vdd! pmos l=180.0n w=2.92u m=1
MM2 net21 vss! net40 vdd! pmos l=180.0n w=880.0n m=1
MM0 net40 in vdd! vdd! pmos l=180.0n w=880.0n m=1
.ENDS
*****add the following lines *****
.lib "PTM180.l" cmos
xt1 in out tri_state
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0n 0n 0.5u 1u)
.trans 1ns 8us
***** Output statements *****
.measure tpLH * rising propagation delay
+ trig V(in) val=0.9 fall=2
+ targ V(out) val=0.9 rise=2
.measure tpHL * falling propagation delay
+ trig V(in) val=0.9 rise=2
+ targ V(out) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'
.probe tran V(in) V(out)
.option post
.end

```



```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE ****
      tphl          tphl          tpd          temper
      alter#
      2.2781e-10    2.8862e-10    2.5821e-10    25.00000
1
```

(e) Compare the results from (b) to (d) and give your comments.

Ans: 電路中的每個級都需要用適當大小的 W 去推動後級電容,以得到最佳的延遲時間。

比較三種情況:

b 小題( $tpd \approx 1.9776\text{ns}$ ):

使用最小的 W 值，驅動能力不足，導致最大的延遲時間

c 小題 FO4 規則( $tpd \approx 0.29750\text{ns}$ ):

第二級和最後級分別放大 4 倍和 16 倍，W 值的增加大幅改善了驅動能力，比基準情況的延遲時間減少約 85%

D 小題 Path-Delay optimization( $tpd \approx 0.25821\text{ns}$ ):

使用數學最佳化計算的放大倍率，確保每級延遲時間平衡，得到最小的延遲時間，比 FO4 規則稍微快約 13%

從模擬結果可以看出，Path-delay optimization 透過精確計算的放大倍率，能夠最有效地驅動負載電容，因此得到最小的 delay time。FO4 規則雖然使用固定的放大倍率，但也達到了很好的效果，延遲時間只比 Path-delay optimization 略慢一些。而未經優化的基準情況，因為 W 值較小，無法有效驅動負載，所以 delay time 最大。這個結果顯示雖然 Path-delay optimization 理論上最佳，但在實際應用中 FO4 規則也能提供相當接近的性能。