M11215075 資工碩二 胡劭

1. Consider the switching function of XOR gate: $f(x,y) = \bar{x}y + x\bar{y}$.

   (a) Prove that $f(x,y) = \overline{\overline{x+y} + xy}$.

Ans:

$$F(x,y) = \overline{\overline{x+y}+xy} = \overline{\bar{x}\cdot\bar{y}+xy} = \overline{\bar{x}\cdot\bar{y}}\cdot\overline{x\cdot y} = (x+y)(\bar{x}+\bar{y}) = x\bar{x}+x\bar{y}+\bar{x}y+y\bar{y}$$

$$= 0 + x\bar{y}+\bar{x}y + 0 = x\bar{y}+\bar{x}y$$

x	y	$\bar{x}$	$\bar{y}$	$\overline{x+y}$	xy	$\overline{x+y}+xy$	$\overline{\overline{x+y}+xy}$	$x\bar{y}+\bar{x}y = x\oplus y$
0	0	1	1	1	0	1	0	0
0	1	1	0	0	0	0	1	1
1	0	0	1	0	0	0	1	1
1	1	0	0	0	1	1	0	0

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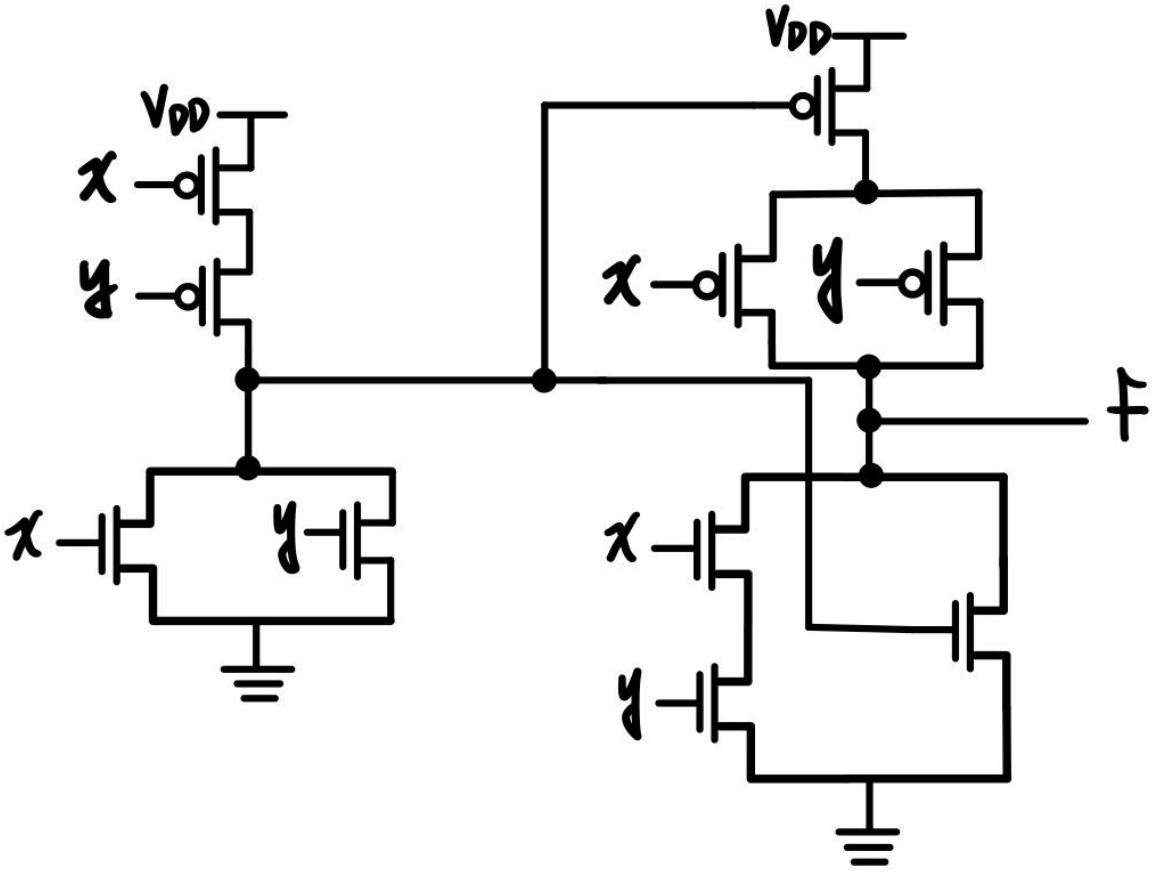
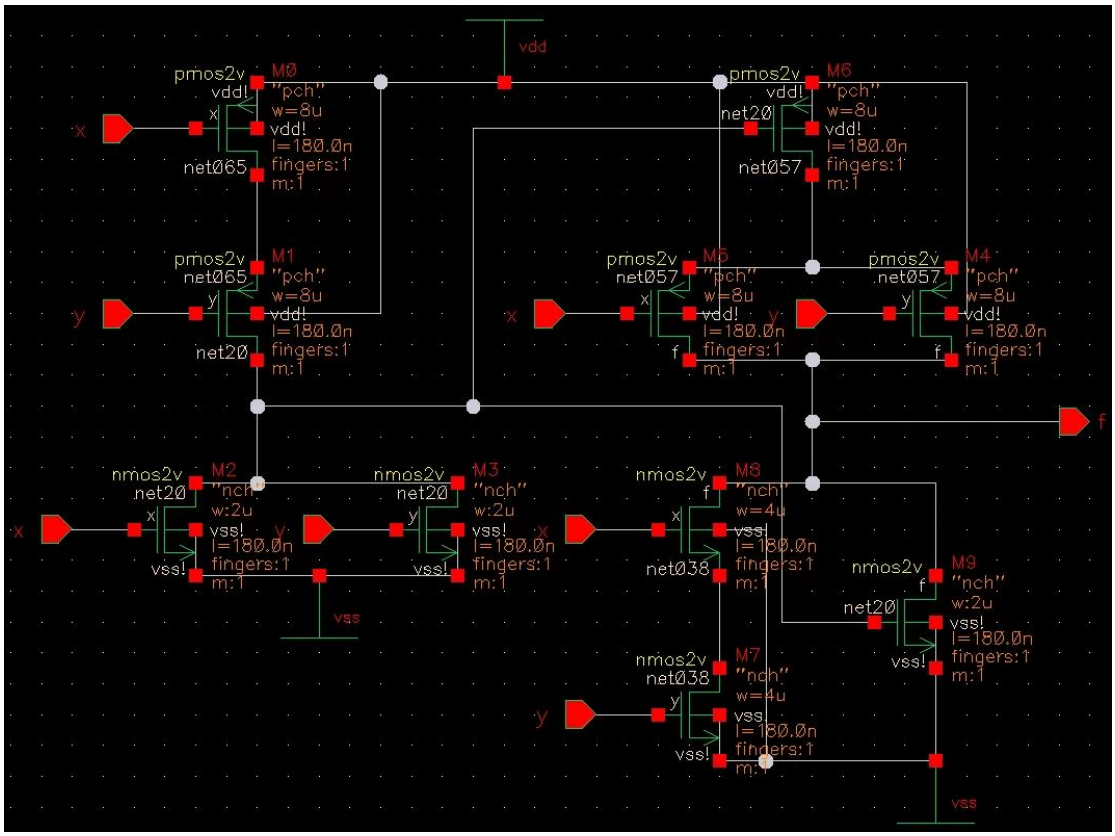
(b) Realize it using a CMOS logic circuit. Your design must be limited to use 10 transistors at most.

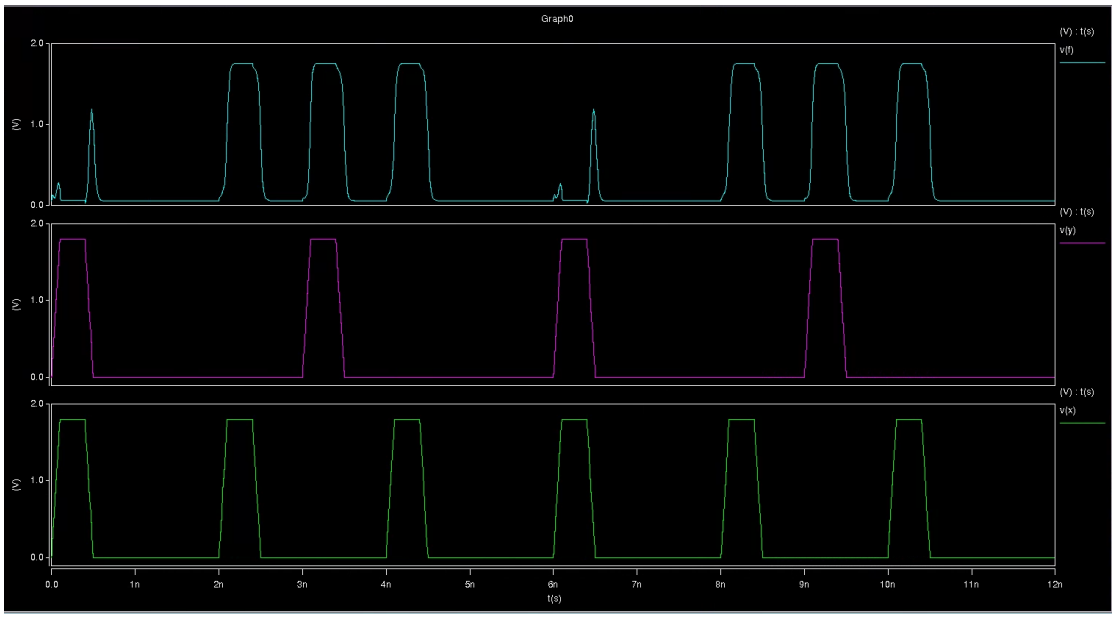
Ans:





(c) Use HSPICE to verify the functionality of the resulting circuit. What is the maximum propagation delay of the resulting circuit?

Ans:

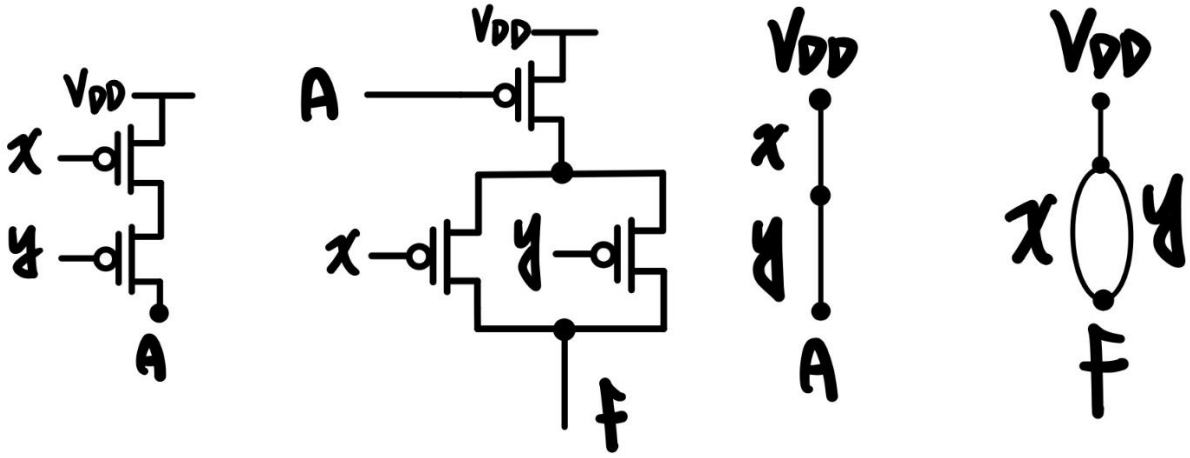



```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '*********************************************************
 tplh_x          tphl_x          tplh_y          tphl_y
 tpd_x           tpd_y           temper          alter#
  8.3605e-12      4.5429e-10      8.3605e-12      4.5429e-10
  2.3133e-10      2.3133e-10       25.00000       1
```

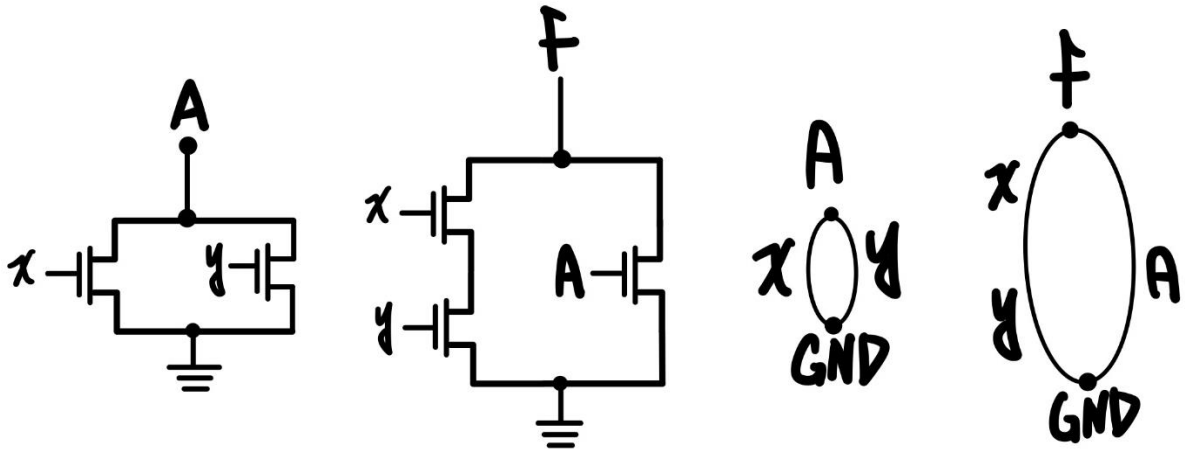
(d) Draw the pMOS and nMOS logic graphs and find the Euler paths.

Ans:

pMOS

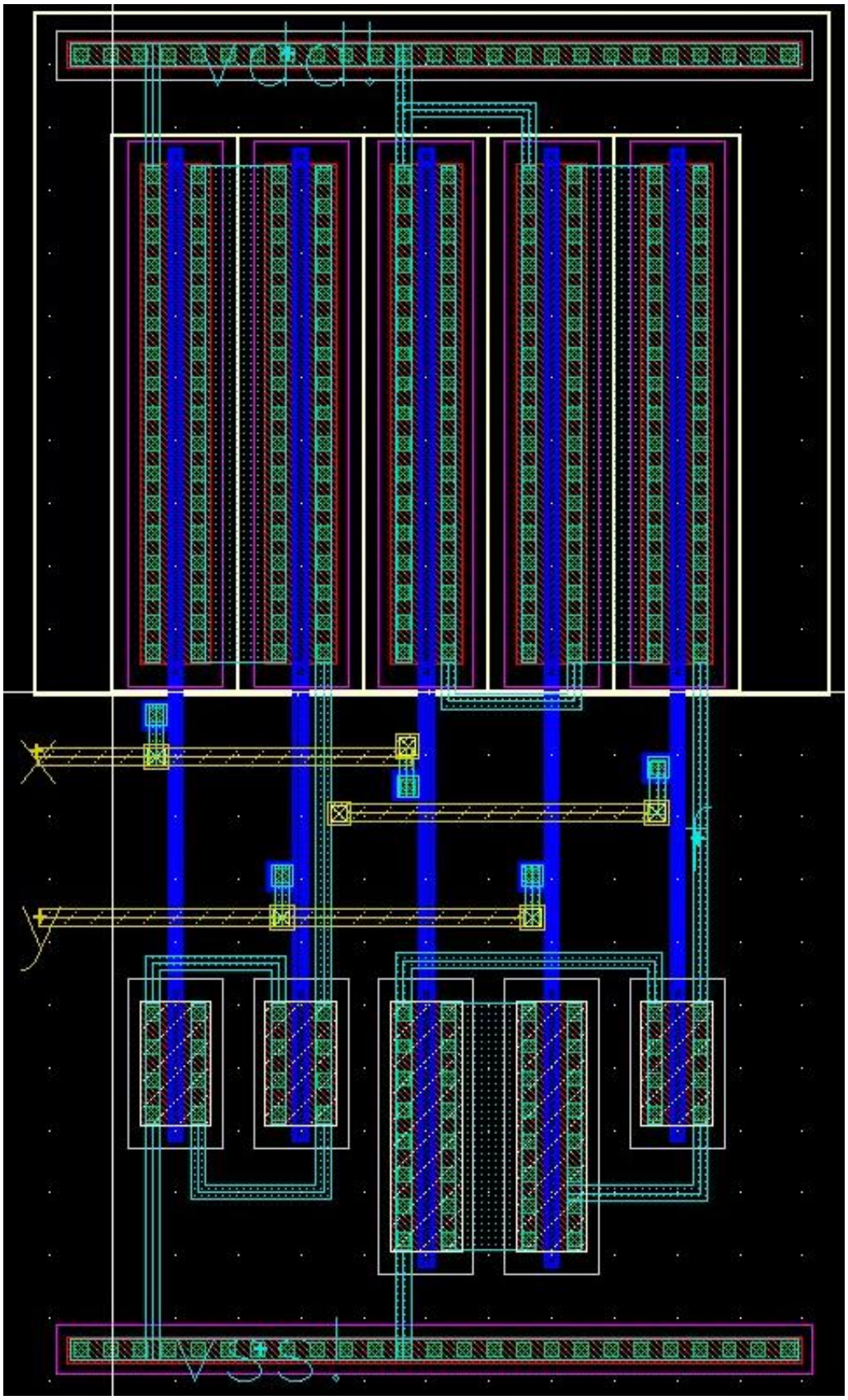


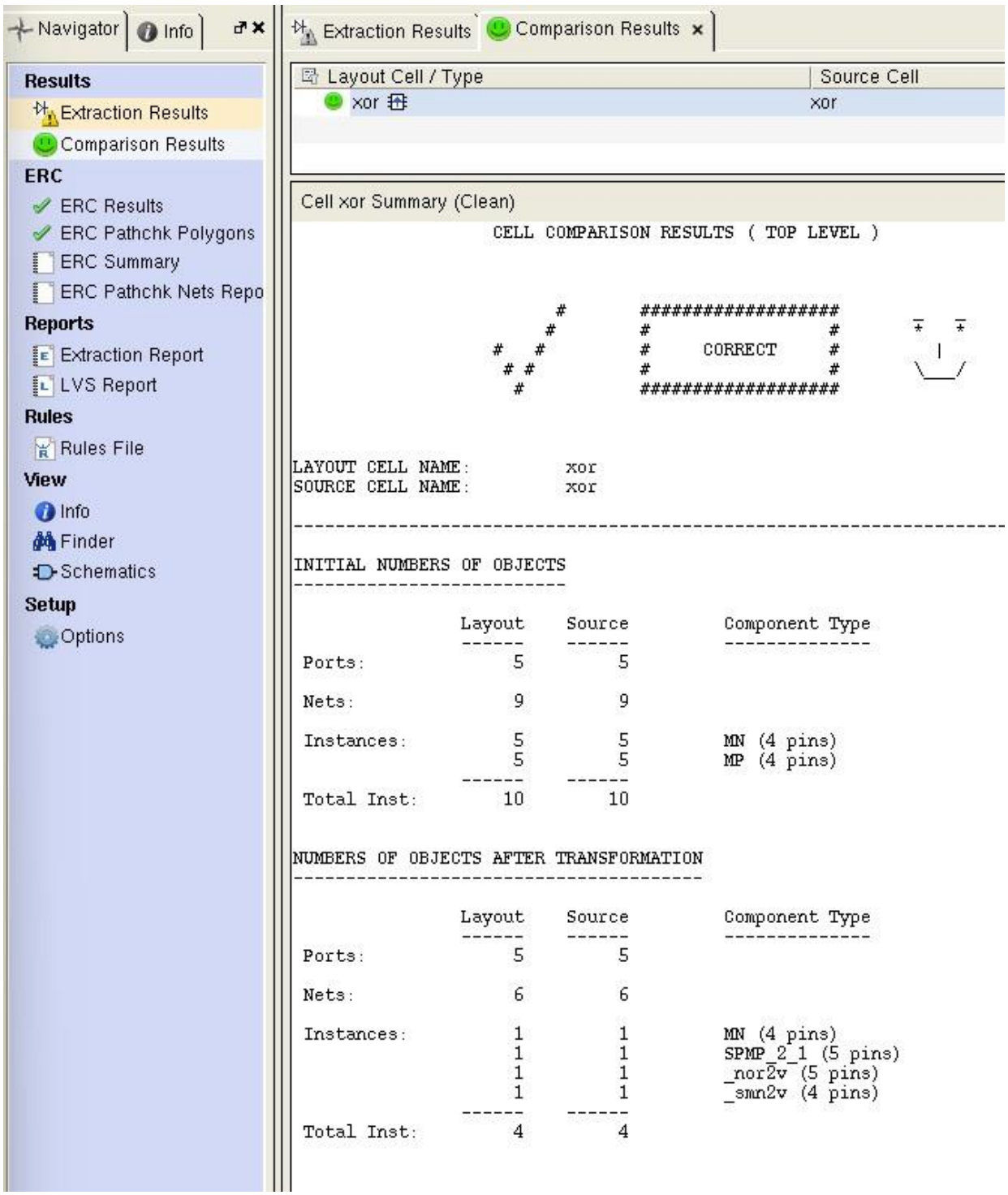
nMOS



(e) Design and carry out a physical layout.

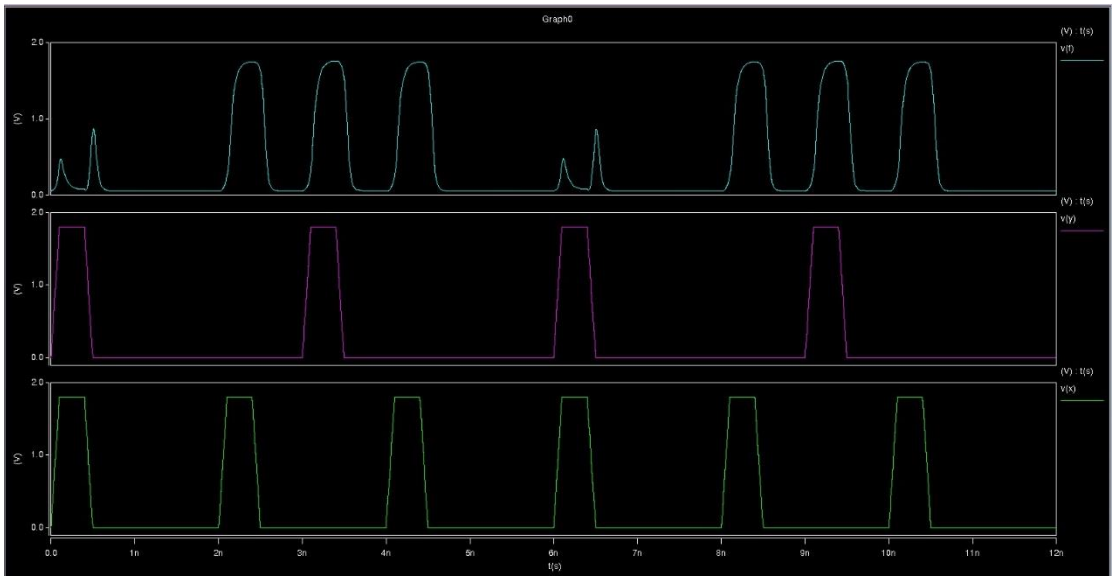
Ans:




Navigator
Info
Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Pathchk Polygons
ERC Summary
ERC Pathchk Nets Repo
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Extraction Results
Comparison Results
Layout Cell / Type
Source Cell
xor
xor
Cell xor Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: xor
SOURCE CELL NAME: xor
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 5 5
Nets: 9 9
Instances: 5 5 MN (4 pins)
5 5 MP (4 pins)
Total Inst: 10 10
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 5 5
Nets: 6 6
Instances: 1 1 MN (4 pins)
1 1 SPMP_2_1 (5 pins)
1 1 _nor2v (5 pins)
1 1 _smn2v (4 pins)
Total Inst: 4 4

(f) Use HSPICE to verify the functionality and estimate the maximum propagation delay of the resulting physical layout.

Ans:




```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '* File: xor.pex.sp'
 tplh_x           tphl_x           tplh_y           tphl_y
 tpd_x            tpd_y            temper           alter#
  1.6990e-09       2.5014e-09       1.6990e-09       2.5014e-09
  2.1002e-09       2.1002e-09         25.00000       1
```

2. Consider the switching function of the XNOR gate: $f(x,y) = xy + \bar{x}\bar{y}$.

   (a) Prove that $f(x,y) = \overline{\overline{xy} \cdot (x+y)}$.

Ans:

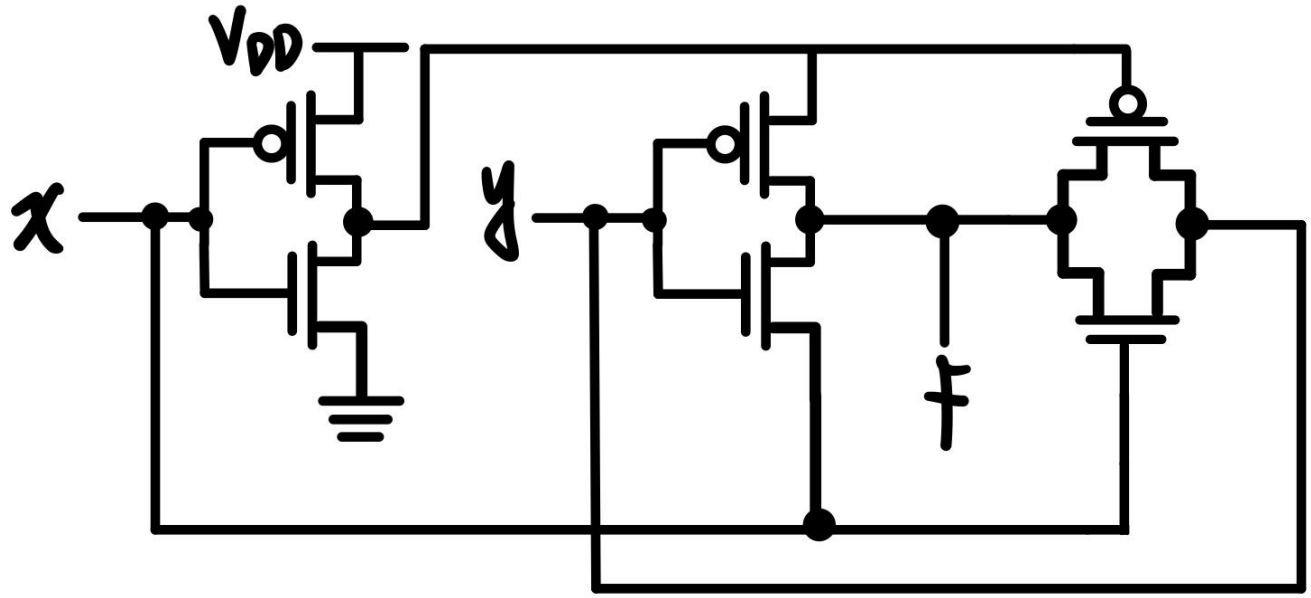
$$F(x,y) = \overline{\overline{xy}\cdot(x+y)} = (\overline{\bar{x}+\bar{y}})\cdot(x+y) = (\bar{x}+\bar{y}) + \overline{(x+y)} = (xy) + \bar{x}\bar{y}$$

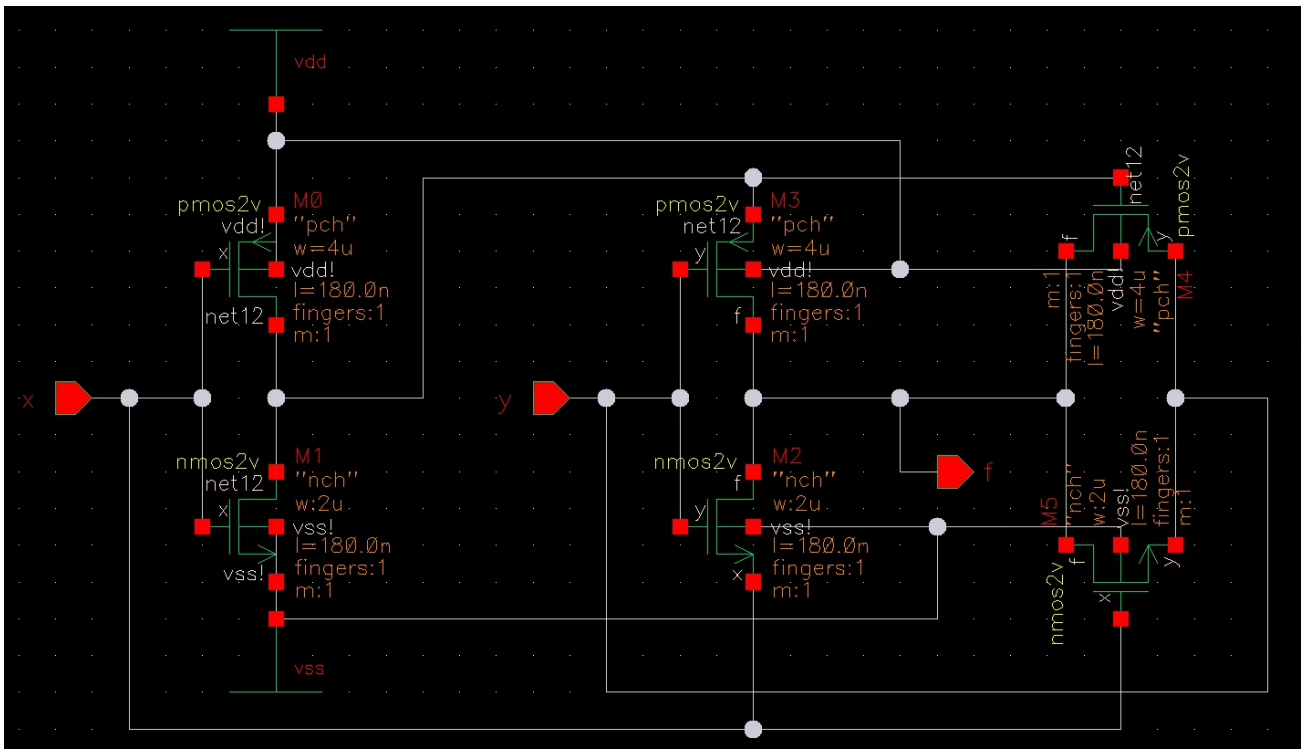
x	y	$\bar{x}$	$\bar{y}$	$x+y$	$\overline{xy}$	$(x+y)\cdot\overline{xy}$	$\overline{(x+y)\cdot\overline{xy}}$	$xy+\bar{x}\bar{y} = \overline{x \oplus y}$
0	0	1	1	0	1	0	1	1
0	1	1	0	1	1	1	0	0
1	0	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1	1

#

(b) Realize it using a CMOS logic circuit. Your design must be limited to use 10 transistors at most.

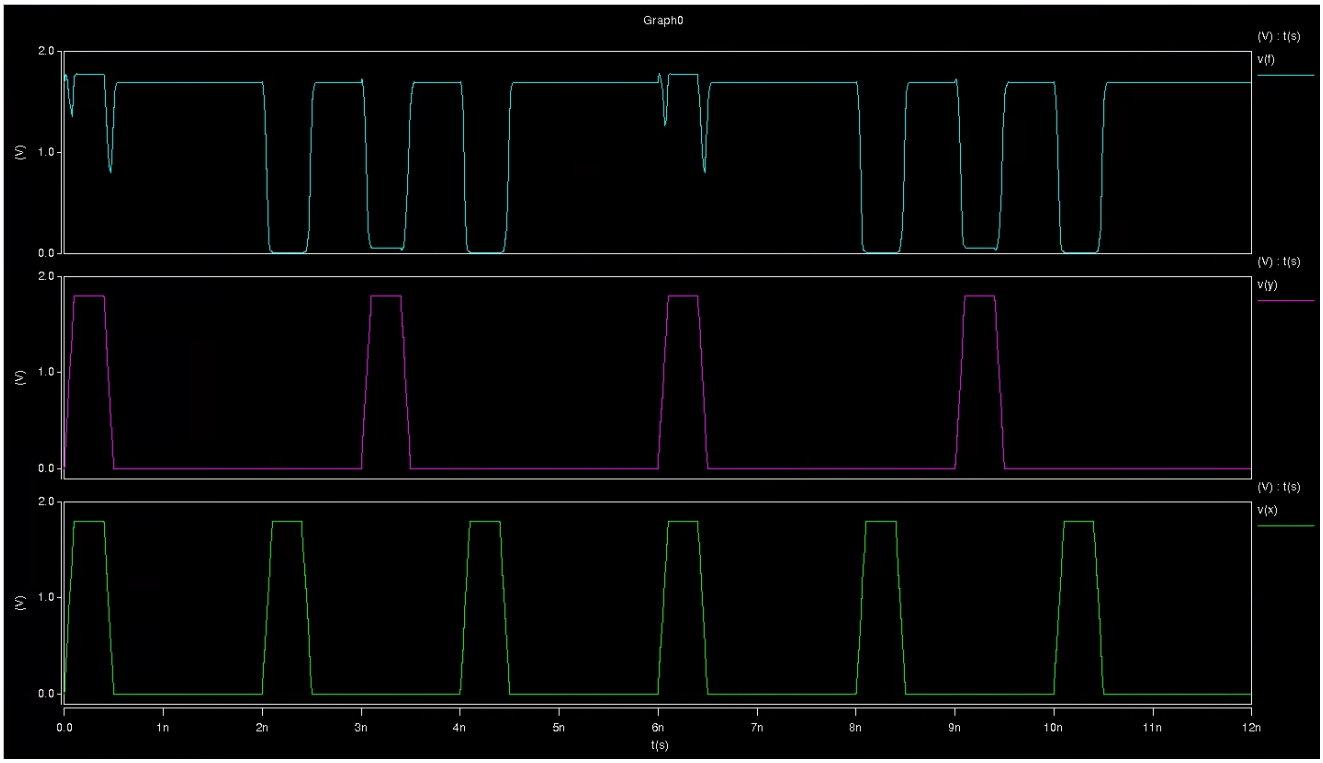
Ans:





(c) Use HSPICE to verify the functionality of the resulting circuit. What is the maximum propagation delay of the resulting circuit?

Ans:

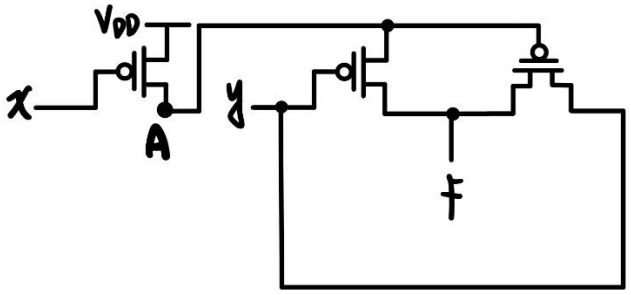


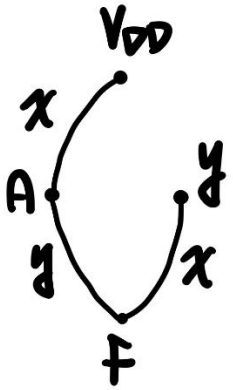

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '*************************************************************
 tplh_x           tphl_x           tplh_y           tphl_y
 tpd_x            tpd_y            temper           alter#
  2.7080e-11       4.0179e-10       2.7080e-11       4.0179e-10
  2.1443e-10       2.1443e-10        25.00000        1
```

(d) Draw the pMOS and nMOS logic graphs and find the Euler paths.

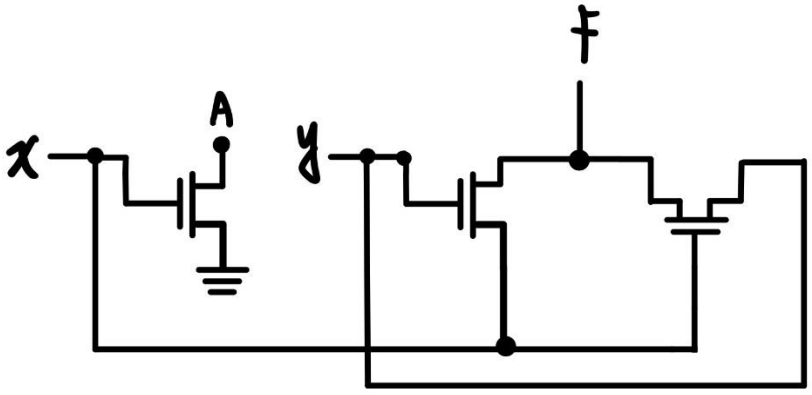
Ans:

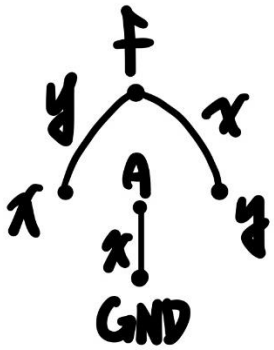
pMOS





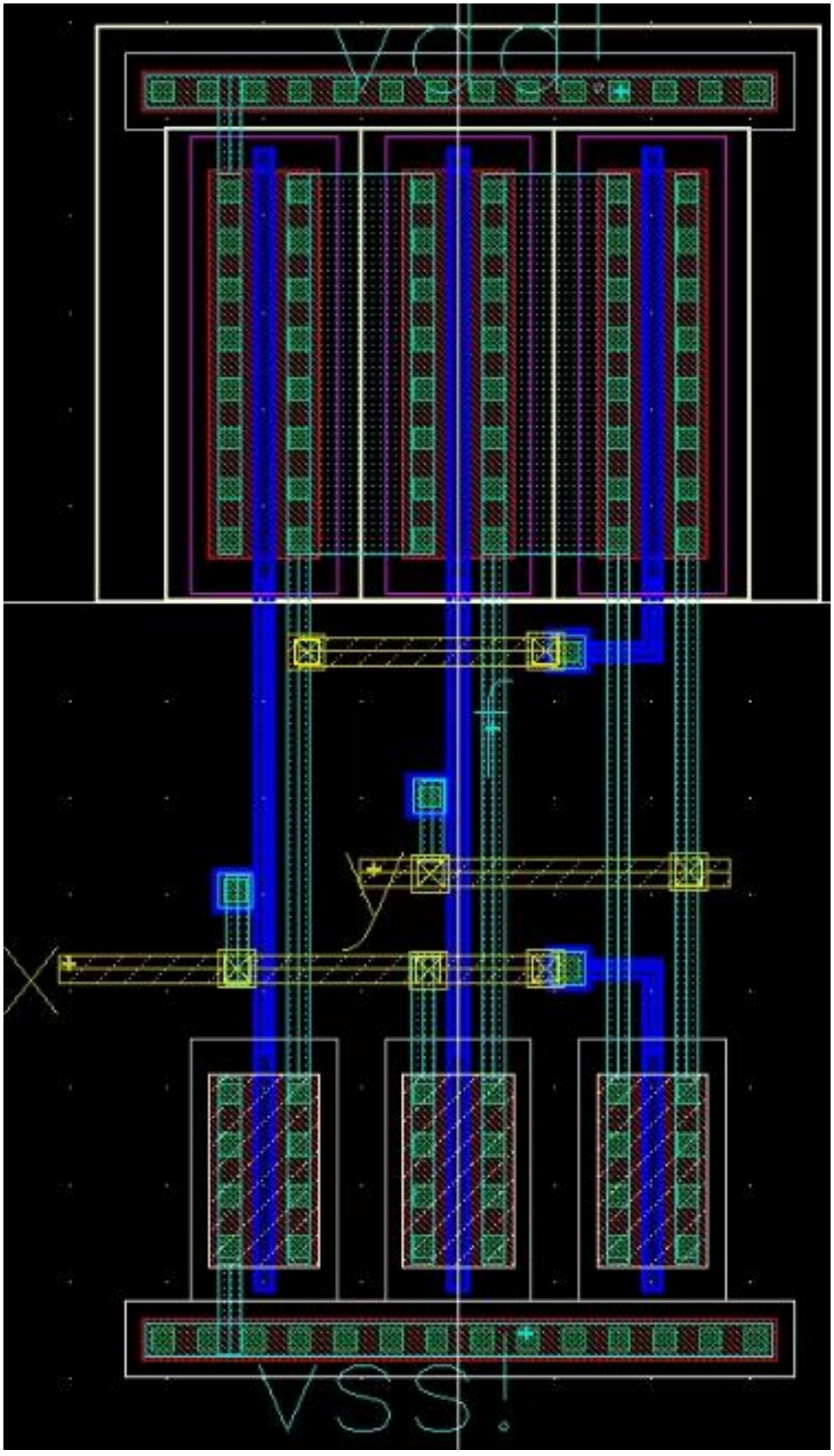
nMOS

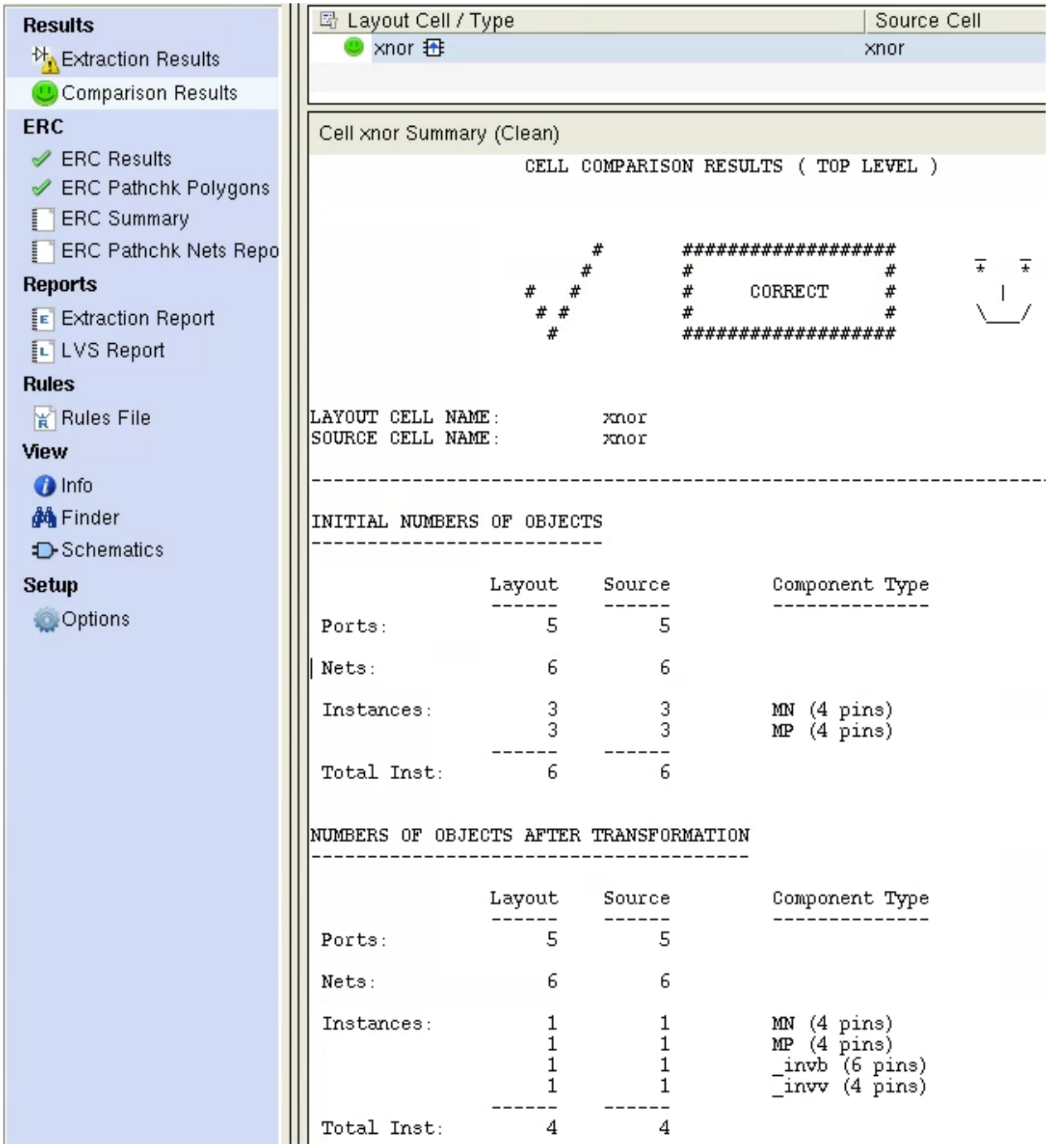




(e) Design and construct a physical layout.

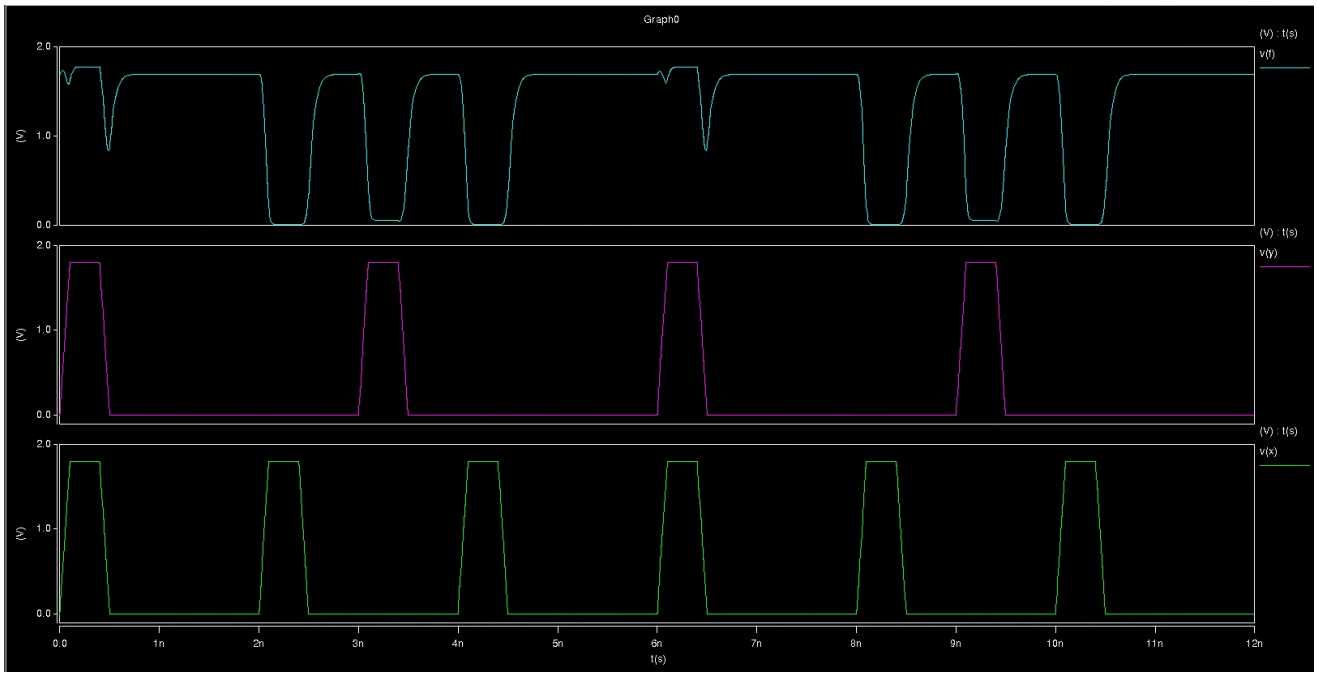
Ans:




Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Pathchk Polygons
ERC Summary
ERC Pathchk Nets Repo
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
xnor
xnor
Cell xnor Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: xnor
SOURCE CELL NAME: xnor
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 5 5
Nets: 6 6
Instances: 3 3 NN (4 pins)
3 3 MP (4 pins)
Total Inst: 6 6
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 5 5
Nets: 6 6
Instances: 1 1 NN (4 pins)
1 1 MP (4 pins)
1 1 _invb (6 pins)
1 1 _invv (4 pins)
Total Inst: 4 4

(f) Use HSPICE to verify the functionality and estimate the maximum propagation delay of the resulting physical layout.

Ans:




```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '* File: xnor.pex.sp'
 tplh_x           tphl_x           tplh_y           tphl_y
 tpd_x            tpd_y            temper           alter#
  5.1570e-11       4.2272e-10       5.1570e-11       4.2272e-10
  2.3714e-10       2.3714e-10        25.00000        1
```