Hspice 補充

```
Open
*inv.sp
inv.mt0
*.EQUATION
*.SCALE METER
*.MEGA
.PARAM

.GLOBAL vdd!
+        vss!

*.PIN vdd!
*+    vss!

********************************************************************************
* Library Name: vlsi
* Cell Name:    inv
* View Name:    schematic
********************************************************************************

.SUBCKT inv in out
*.PININFO in:I out:O
MM0 out in vss! vss! nmos l=180.0n w=2u m=1
MM2 out in vdd! vdd! pmos l=180.0n w=4u m=1
.ENDS

.lib "PTM180.l" cmos
xinv in out inv
vdd vdd! 0 1.8
vss vss! 0 0
vin in 0 pulse (0 1.8 0 0.1n 0.1n 0.3n 1n)
********** Output statements **************
.measure tpLH * rising propagation delay
+ trig V(in)  val=0.9 fall=1
+ targ V(out) val=0.9 rise=1

.measure tpHL * falling propagation delay
+ trig V(in)  val=0.9 rise=2
+ targ V(out) val=0.9 fall=2
.measure tpd param='(tpLH+tpHL)/2'

.probe tran V(in) V(out)
.trans 1ps 4ns
.option post=2
.end
```

打好sp檔後
執行hspice inv.sp

看波形圖

(產生輸入波形)

量測 tpLH 與 tpHL

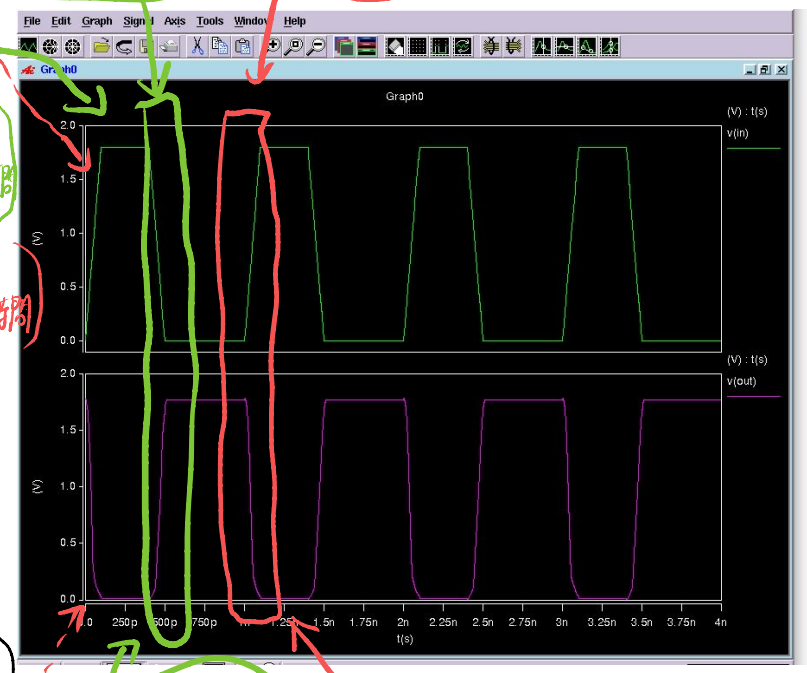
(tpLH為 用in觸發 目標out 從 low→high 變化的時間)

(tpHL為 用in觸發 目標out 從 high→low 變化的時間)

in第一次rise

in 第一次fall

in 第二次rise



到 mt0 檔查看 tpLH, tpHL, tpd

out第一次rise

out 第一次 fall

out第二次fall

Open
inv.mt0
~/Desktop/cic018/spfile
inv.sp
inv.mt0

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '********************************************************************************'
 tplh             tphl             tpd              temper
 alter#
  7.3428e-12       6.0684e-12       6.7056e-12       25.00000
1
```

tpLH, tpHL, tpd 皆為正值)

(每次sp檔有變動, hspice inv.sp 就要重新執行.)

1. 如果遇到 tpLH, tpHL 有負值，可以先檢查是否量測的 rise, fall 點沒有對好。

2. 或是如下（MOS 寬度數值 or 其他參數要改動）

Layout 跟 schematic 裡 MOS 寬度也要記著改。

改好後 schematic 要重跑 hspice，看波形圖，tpd 是否正確。

Layout 要重跑後面 DRC, LVS, PEX verify.

inv.sp | inv.mt0

```
$DATA1 SOURCE='PrimeSim HSPICE' VERSION='S-2021.09' PARAM_COUNT=0
.TITLE '*************************************************************
 tplh             tphl             tpd              temper
 alter#
  2.0747e-11      -1.2700e-11       4.0234e-12       25.00000
```

負值

```
Warning: For measurement TPHL, target time is smaller than trigger time.
 tran: time= 1.2038e-09 tot_iter=     129 conv_iter=      57 cpu clock= 1.52e+00
 tran: time= 1.6331e-09 tot_iter=     166 conv_iter=      75 cpu clock= 1.52e+00
 tran: time= 2.0010e-09 tot_iter=     171 conv_iter=      79 cpu clock= 1.52e+00
 tran: time= 2.4010e-09 tot_iter=     219 conv_iter=      98 cpu clock= 1.52e+00
 tran: time= 2.9252e-09 tot_iter=     253 conv_iter=     115 cpu clock= 1.52e+00
 tran: time= 3.2043e-09 tot_iter=     299 conv_iter=     133 cpu clock= 1.52e+00
 tran: time= 3.6332e-09 tot_iter=     336 conv_iter=     151 cpu clock= 1.52e+00
```

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inv.sp

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```

tpHL為負

這樣就是 pMOS寬度不足導致不平衡，使輸出信號傳播延遲異常。

改為 w=4u 就沒有負值。

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參考資料:

1. https://hackmd.io/@azoo/hspice_tutorial