

OpenROAD: The Journey So Far, and the Roadmap

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<https://theopenroadproject.org>

<https://github.com/The-OpenROAD-Project>



QUALCOMM arm



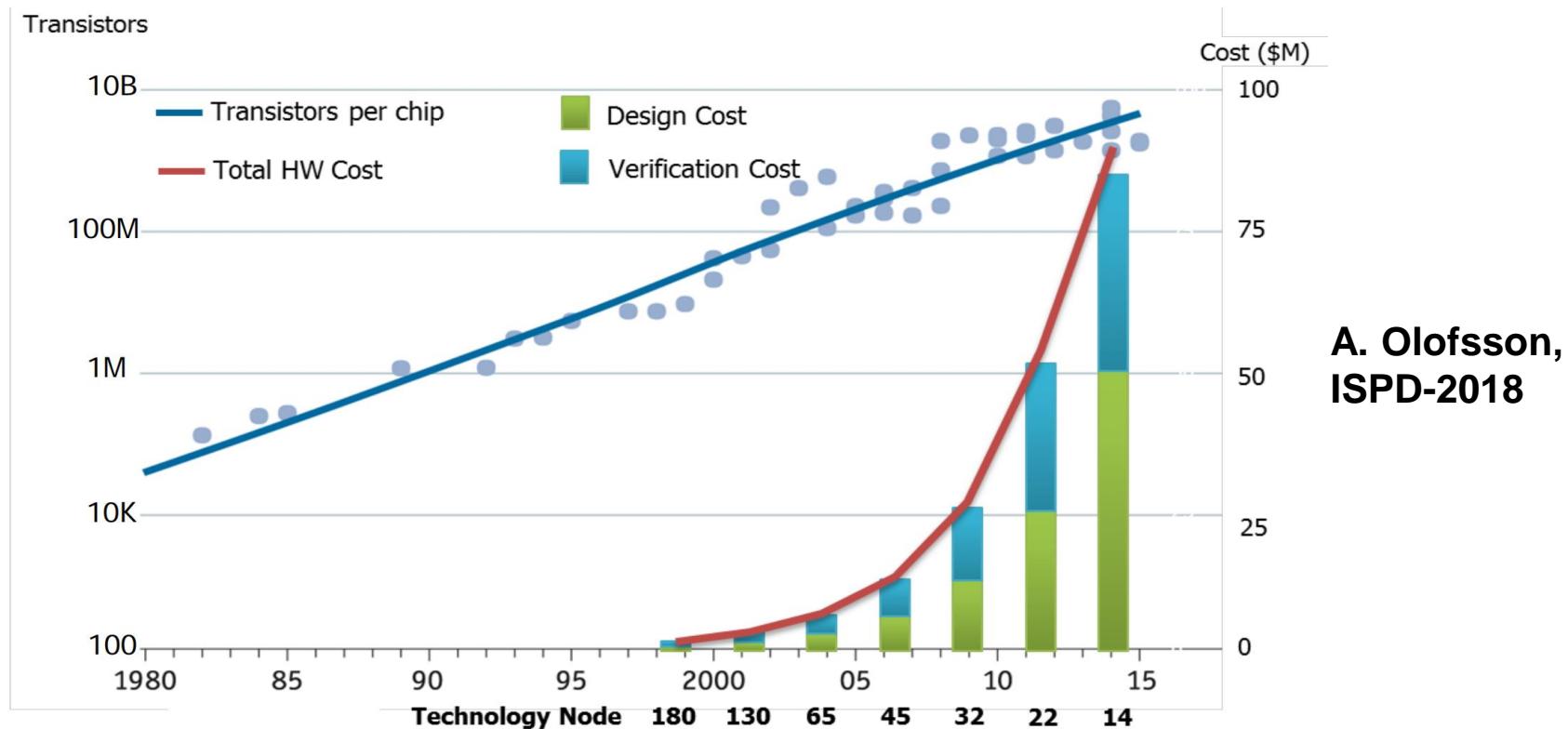
precision
Innovating chip design

Agenda

- **What is OpenROAD ?**
- **How did we get here ? (The Journey)**
- **Where are we going ? (The Roadmap)**

The Crisis of Hardware Design

- ASIC design in advanced nodes: barriers of Cost, Expertise, Risk



- Innovators can't evaluate PPAC metrics of their design ideas

Design with Proprietary EDA: Need \$\$\$, Experts

- **Very sophisticated tools with 1000's of commands**
- **Vendor focus: performance, power, area for bleeding-edge customers**
 - 20+ years of “hyperoptimization” in two main platforms (silos)
- **Need large teams of expert users, many manual steps**
- **Long project schedules: tool latencies, limited licenses, ...**
- **Significant project risks**

OpenROAD: June 2018 – December 2023

- “Foundations and Realization of Open, Accessible Design”
- Funded by U.S. DARPA as part of the Electronics Resurgence Initiative (ERI). (UCSD = prime contractor)
- Mission: Democratize IC Design, Boost HW & EDA Innovation
 - Revitalize EDA
 - Contract: Deliver an Open-Source, RTL-to-GDS EDA system
 - 24-hour, no-human-in-loop, tapeout-clean layout in FinFET nodes



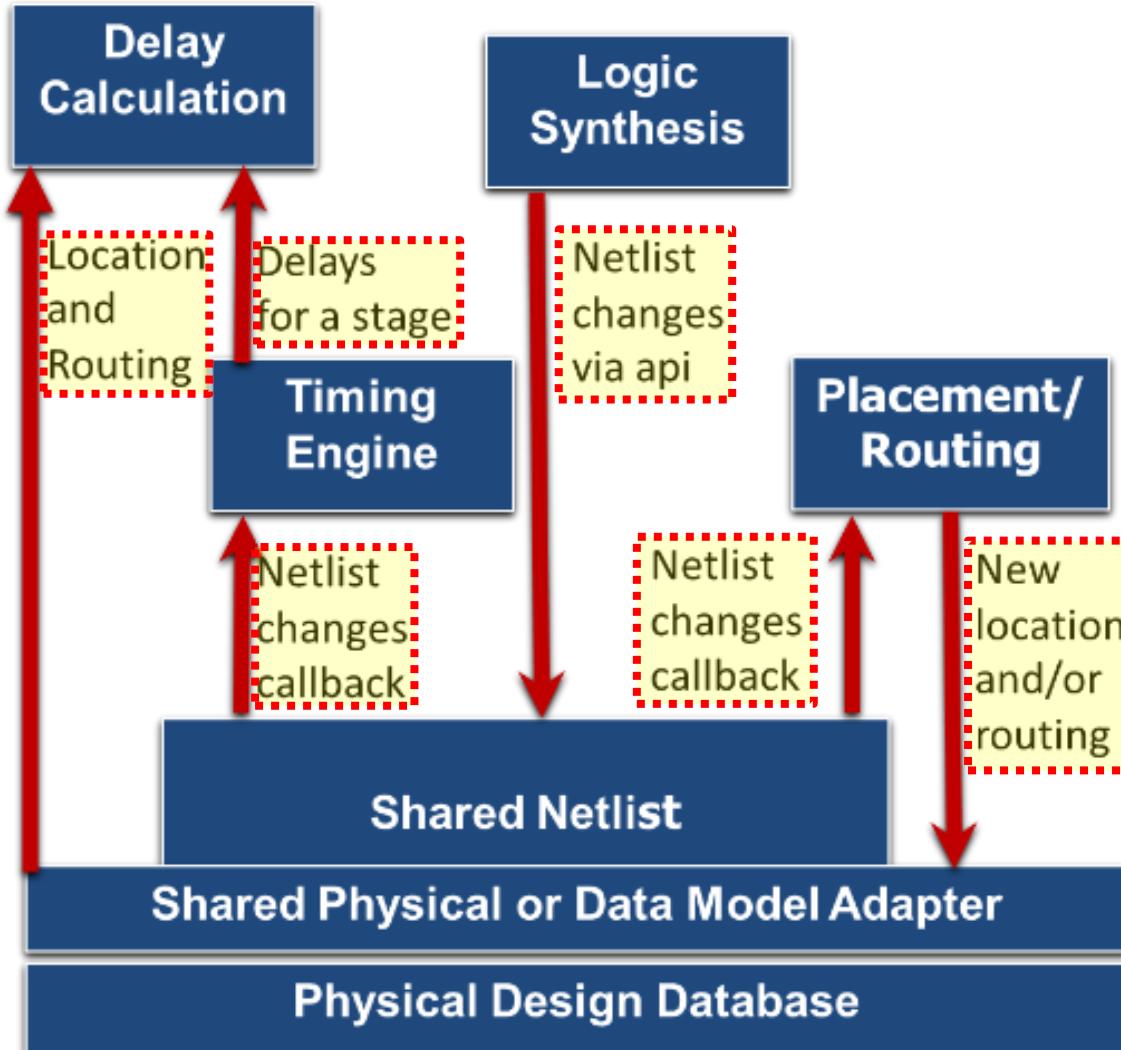
- Since 2020, Precision Innovations, Inc has been the key industrial developer: R&D, support, outreach
- Major support from Google (+ commercial engagements)

OpenROAD: RTL-to-GDS, No Humans, 24 Hours

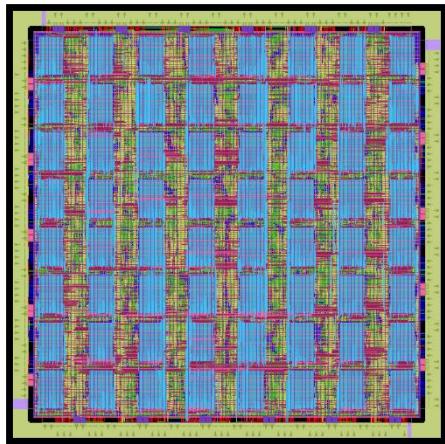
- **FOCUS: Ease of use and runtime**
- **Directly attack the crises of design and innovation**
 - **Schedule barrier:** **RTL-to-GDS** in 24 hours
 - **Expertise barrier:** No-human-in-loop, tapeout GDS
 - **Cost barrier:** Open source (and, runs in 24 hours)
- **Unleash system innovation and design innovation**
- **Enable tool customization to system, application needs**

Industrial Strength Incremental Architecture: Built to Last

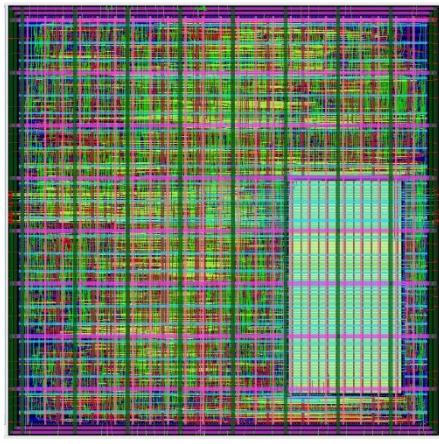
Further notes: [link](#) [link](#) [link](#)



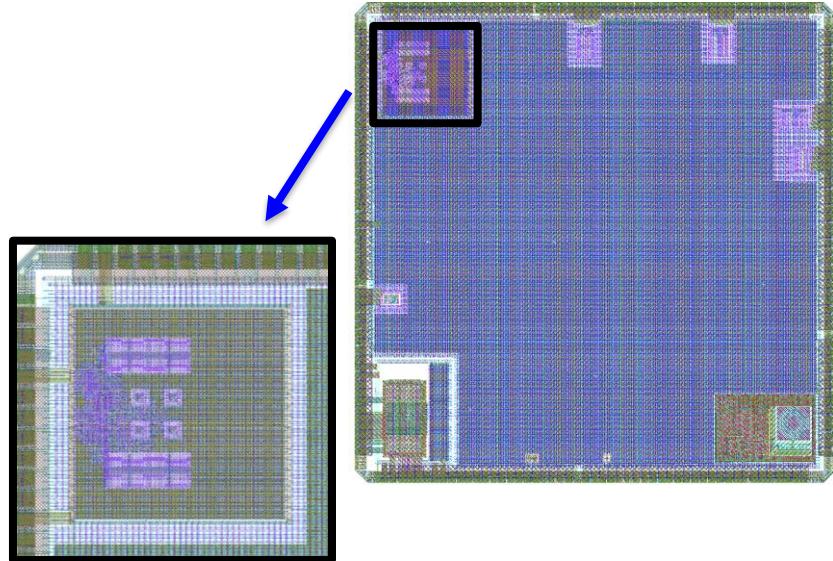
Usage in Advanced Nodes



GF55 AI platform



GF12LP AI tile



OpenTitan SoC

Army Research Labs
GF55, GF12LP

U. Michigan / FASoC
GF12LP

Current Status



Data Prep

Synthesis (Yosys+ABC)

Floorplan

Placement

Clock Tree Synthesis

Routing

Static Timing Analysis

BEOL Fill

GDSII

DRC + LVS (KLayout)

Supported Nodes

GF180nm

SKY130nm

SKY90nm

TSMC 65nm

GF55nm

Intel 22/16nm

GF12LP

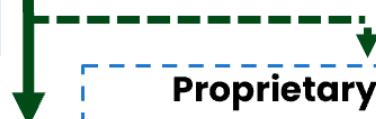
- **Functionality:** 600+ tapeouts at 180-12nm

- **Community:** OpenROAD app has >18K commits from 84 contributors

- **Education and Workforce:** from high school to graduate level, extension

- **Researchers**

- **Small R&D teams, startups**

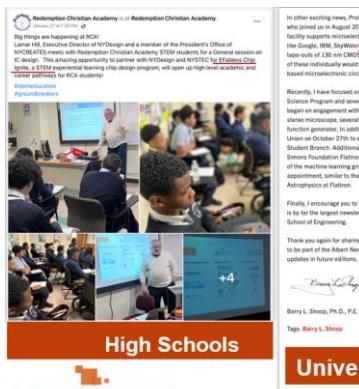


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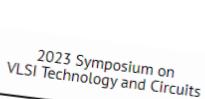
Momentum, “Virality”



High Schools

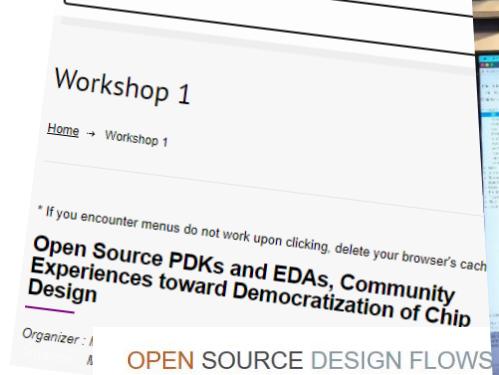
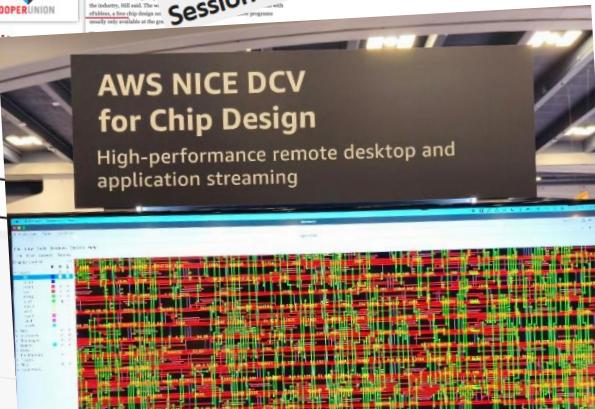
NYDESIGN

Made possible with Efabless' chipIgnite

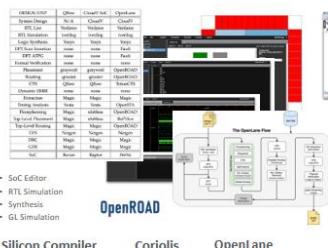


2023 VLSI
SYMPOSIUM

ABOUT



OPEN SOURCE DESIGN FLOWS

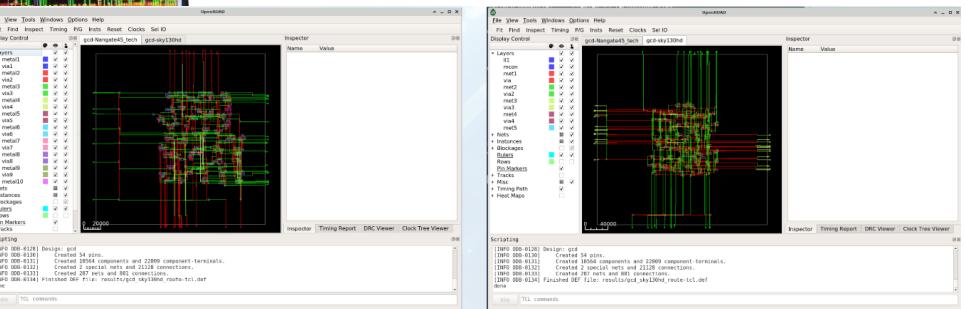


L-R: NY Design HS, CC, University programs w/Efabless ChipIgnite; VLSI Symposium workshop in June; multiple OS EDA flows; OpenROAD demo in AWS booth at Semicon West; 4th DAC birds-of-a-feather meeting on OS EDA; OpenROAD DB and GUI extensions showing heterogeneous multi-tier post-route layout.

efabless

- **Functionality:** 600+ tapeouts at 180-12nm
- **Community:** OpenROAD app has >18K commits from 81 contributors
- **Education and Workforce:** from high school to graduate level, extension

- **Researchers**
- **Small R&D teams, startups**



OpenROAD Availability

- The Project on GitHub
 - <https://github.com/The-OpenROAD-Project>
- The Flow
 - Automated full flow, built using tool components that are created for automation
 - <https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts>
- The Top-level Application
 - An integrated EDA tool focused on full automation
 - <https://github.com/The-OpenROAD-Project/OpenROAD>
- More!
 - Documentation:
<https://openroad.readthedocs.io/en/latest/main/README.html>
 - Slack: <https://skywater-pdk.slack.com/archives/C0161A4A59V>
 - OpenTapeout video:
<https://www.youtube.com/watch?v=wvPZREaP7E0&t=2652s>

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- Where are we going ? (The Roadmap)

MARCO [GSRC](#) Calibrating Achievable Design

VLSI CAD Bookshelf 2

 Andrew B. Kahng, and Igor Markov

The bookshelf is a new electronic medium centered around high-quality implementations of optimization algorithms for VLSI CAD and information relevant to creating and evaluating such implementations. The project started with emphasis on Physical Design for VLSI and is now rapidly expanding to related areas.

If you would like to contribute : see [instructions](#)

• [Overview](#)

• [Bookshelf as a New Electronic Medium](#)

• Our talk at Berkeley on Sept 2, 1999 ([ppt](#)) ([ps](#))

• Stanford, Sept 24, 1999 (GSRC Workshop) ([ppt](#))

• San Jose, Dec 9, 1999 (GSRC Annual review) ([ppt](#))

• Los Angeles, Jun 4, 2000 (GSRC workshop) ([ppt](#))

• Los Angeles, Jun 8, 2000 (Design Automation Conference) ([ppt](#)), ([ps](#)), ([pdf](#)), • [Source Code Standards](#) (to be greatly expanded)

• Las Vegas, Jun 18 2001 (GSRC Workshop) ([ppt](#))

• Santa Clara, Sep 6 2001 (GSRC Workshop) ([ppt](#))

• [Submission \(release\) Standards](#)

• [New Data Formats](#) 

• [Copyright issues and support issues](#)

<https://vlsicad.eecs.umich.edu/BK>

“Seeding an Ecosystem”

- ERI Summit 2018: Critical mass and critical quality
- ICCAD 2019: Open Source is a mirror
- VLSI-SoC 2020: If we build it, who will come?

SWINGING FOR THE FENCES

- Must achieve critical mass and critical quality



11 of 13 IDEA TA-1 subtasks
+ Base Technologies, Design

Common Infrastructure	Databases / Processing
✓ Cloud Infrastructure	
✓ Timing Analysis	
✓ Parasitic Extraction	
✓ Readers + Writers	
✓ Power and SI Analysis	
Layout Generators	Logic Synthesis
✓ Floorplanning	
✓ Placement	
✓ Clock Tree Synthesis	
✓ Detailed Routing	
✓ Layout Finishing	
Design	SoC Design Advisors

Looking Into the Mirror of Open Source

(Invited Paper)

Andrew B. Kahng

CSE and ECE Departments, UC San Diego, La Jolla, CA 92093
abk@ucsd.edu

Open-Source EDA: If We Build It, Who Will Come?

Andrew B. Kahng

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All talks are at <https://vlsicad.ucsd.edu>

If We Build It, Who Will Come? **Who is “We”?**

Lesson: Open-source EDA goes beyond academic research abilities

- **Original proposal:** OpenROAD would be developed by Ph.D. students and post-docs at **five** universities
- Separately, students and post-docs at a sixth university would be the “internal design advisors”
 - Vision: span product engineering, expert user testing, corporate AE-like functions
- **Key point:** clear separation between “internal design advisors” and “tool developers” is built into OpenROAD
- Deliverables such as PPA assessment and calibration must come from design advisors

If We Build It, Who Will Come? **Who is “We”?**

- *What actually happened ...*
- By 9 months in, need for experienced EDA architect was clear → belt-tightening and non-DARPA gift funds allowed EDA veterans to be brought into the project



JAMES
CHERRY



DIMITRIS
FOTAKIS



MOHAMED
SHALAN



TOM
SPYROU



MATT
LIBERTY



DON
MACMILLEN

- Technical leadership and know-how: tool delivery, project management, infrastructure (DB, GUI, build/CI), key engines (STA, RCX)

*Lesson: “We” must include professional
EDA software developers and architects.*



Skills and Mindset

- Strongest contributors have software skills **and** the right mindset
 - E.g., undergraduate and graduate students from CS backgrounds, in other countries (!)
 - Coached by EDA veterans
 - Obtain thesis topics, publications along the way

ICCAD-2020

Contributions to OpenROAD from Abroad: Experiences and Learnings

Invited Paper

Mateus Fogaça^{1,3}, Eder Monteiro³, Marcelo Danigno⁵, Isadora Oliveira^{1,3}, Paulo F. Butzen^{1,4} and
Ricardo Reis^{1,2,3}

¹PGMicro/²PPGC, ³Inst. de Informática, ⁴Dep. de Elétrica, Universidade Federal do Rio Grande do Sul

⁵Centro de Ciências Computacionais, Universidade Federal do Rio Grande - FURG

{mpfogaca,emrmonteiro,isoliveira,reis}@inf.ufrgs.br,marcelo@furg.br,paulo.butzen@ufrgs.br

Abstract

The OpenROAD project is an ambitious initiative seeking to develop an automated, open-source RTL-to-GDSII flow. To build its complex toolset, OpenROAD brings together a

1 Introduction

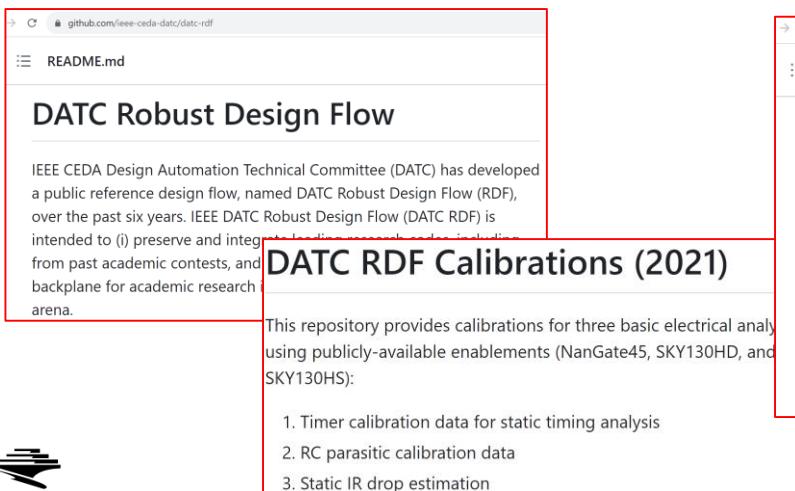
Modern technologies introduce an ever-increasing set of design rules and ever-more demanding power, performance, and area targets. The cost of IC design continues to increase,

“We” Must Also Include the Right **Users**

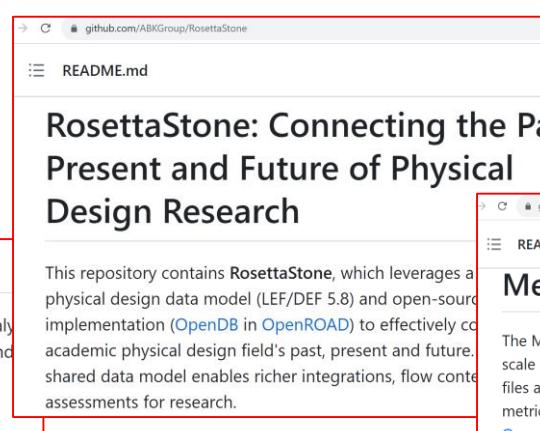
- Open-source EDA is still EDA
- There has never been a successful EDA tool that hasn't had an amazing AE and power user behind it
 - “*we're still in taxicab mode with our key beta customer*”
- Mainstream tool user attitude: file bug, wait for fix
 - **Passive, problem-reporting**
- Power user / AE attitude: find fixes and workarounds, and package these up for R&D (developers)
 - **Active, problem-solving**
 - OpenROAD team has a design services / tapeout consultant

If We Build It, Who Will Come? Who is “Who”?

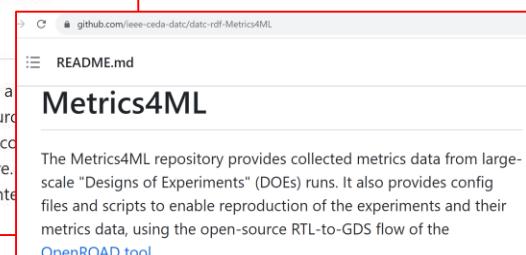
- Who will use open-source EDA in the future?
- Original vision: Users will make enhancements, pull requests ...
 - What we found: This is a very rare type of user !
 - (Greatly outnumbered by the “want poor-man’s Innovus” crowd)
- On the other hand
 - Good news #1: the Open Hardware community is very engaged and supportive
 - Good news #2: Academic EDA researchers increasingly see the value of open-source foundations, transparent baselines



The screenshot shows a GitHub repository page for `github.com/ieee-ceda-datc/datc-rdf`. The main content is the `README.md` file, which describes the DATC Robust Design Flow. A red box highlights a section titled "DATC RDF Calibrations (2021)". Below this section, it says: "This repository provides calibrations for three basic electrical analysis using publicly-available enablements (NanGate45, SKY130HD, and SKY130HS):". Underneath, there is a numbered list: "1. Timer calibration data for static timing analysis", "2. RC parasitic calibration data", and "3. Static IR drop estimation".



The screenshot shows a GitHub repository page for `github.com/ABKGroup/RosettaStone`. The main content is the `README.md` file, which discusses RosettaStone: Connecting the Past, Present and Future of Physical Design Research. A red box highlights this title. Below it, it says: "This repository contains RosettaStone, which leverages a physical design data model (LEF/DEF 5.8) and open-source implementation ([OpenDB](#) in [OpenROAD](#)) to effectively connect academic physical design field's past, present and future. shared data model enables richer integrations, flow consistency and assessments for research."



The screenshot shows a GitHub repository page for `github.com/ieee-ceda-datc/datc-rdf-Metrics4ML`. The main content is the `README.md` file, which describes the Metrics4ML repository. A red box highlights the title "Metrics4ML". Below it, it says: "The Metrics4ML repository provides collected metrics data from large-scale "Designs of Experiments" (DOEs) runs. It also provides config files and scripts to enable reproduction of the experiments and their metrics data, using the open-source RTL-to-GDS flow of the [OpenROAD](#) tool."

“Not Research As Usual”

- An **academic** research project, delivering **tapeout-clean** layout generation for **commercial** FinFET nodes in **permissive open source**, per **contract** with the U.S. Government
- → expectations, names, “signoff”, ...
- “**Not Research As Usual**”

SWINGING FOR THE FENCES

- Must achieve critical mass and critical quality

UCSD Qualcomm arm
BROWN MICHIGAN UNIVERSITY OF MINNESOTA
ILLINOIS UIUC

11 of 13 IDEA TA-1 subtasks + Base Technologies, Design

Common Infrastructure	Databases / Processing
✓ Timing Analysis	✓ Cloud Infrastructure
✓ Parasitic Extraction	✓
✓ Readers + Writers	✓
✓ Power and SI Analysis	✓
✓ Logic Synthesis	✓
✓ Floorplanning	✓
✓ Placement	✓
✓ Clock Tree Synthesis	✓
✓ Detailed Routing	✓
✓ Layout Finishing	✓
Design	SoC Design Advisors

First ERI Summit, July 2018

New: OpenROAD RTL-to-GDS v1.0 Expectations

30 Nov 2019

NEW: OpenROAD “Safe Names” Conventions, v1.0

10 Dec 2019

A post-route timing evaluation flow with OpenRCX is available !

14 Dec 2020

AND MORE ...

- Open-sourcing of commercial timing engine
- Donated commercial tool source code base
- Industry advisors and technical contributors
 - Dr. Chi-Ping Hsu, Avatar
 - Dr. Noel Menezes, Intel
 - Dr. Richard Ho, Google
 - ...
- Worldwide outreach, engagement, support ...

Parallax software



National
Taiwan
University



KAIST



UNIVERSIDADE FEDERAL
DO RIO GRANDE DO SUL



CUHK
香港中文大學



SEOUL
NATIONAL
UNIVERSITY



intel



AVATAR
Integrated Systems



And More Dimensions: The Next Generation

• Help with curriculum development, sharing, mentoring !

Semiconductor Engineering certificate program objectives

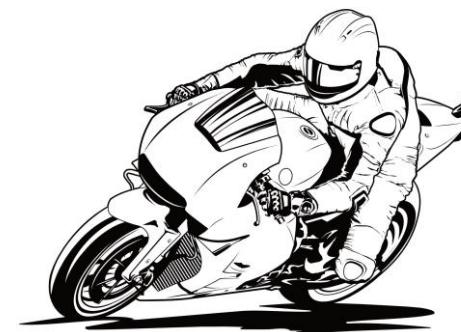
- Implement Verilog modeling of digital logic
- Write assertions for formal verification using SystemVerilog
- Build an advanced UVM verification environment
- Understand and implement DFT concepts in an ASIC design
- Complete practical designs with Xilinx FPGAs
- Implement a design from RTL to GDS

Access to premier tools

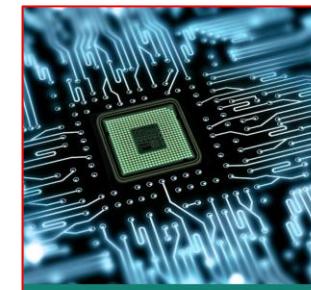
Using premier industry tools from Cadence, OpenROAD, Siemens, and Synopsys, you'll learn front-end and back-end ASIC design and leave the classroom ready to apply new skills at your job.



before



In March 2020 I started getting interested in Open Source ASIC tooling.



Why teach Chip Engineering?

The design and creation of semiconductor products is an exciting field that requires a high-demand skill set in the industry. As a first of its kind, high school students will learn how to design microchips, learn and apply software methodologies to create hardware designs including logic representation in binary systems, basic building blocks and structure of digital, analog and mixed-signal components. You will learn the use of Verilog - a popular hardware description language, open-source software such as OpenROAD and the main stages of building a chip, from specification, testing and to manufacturing.

These are very important skills that lead to fulfilling and long term opportunities -- jobs in industries -- from building toys, cellphones, cars, thermostats and military systems. Entry level pay can start at \$48K + per year depending on location, position and background. So sign up fast!

$A \cdot B$ or $A \uparrow B$		INPUT	OUTPUT
A	B	Q	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

Foundational Path



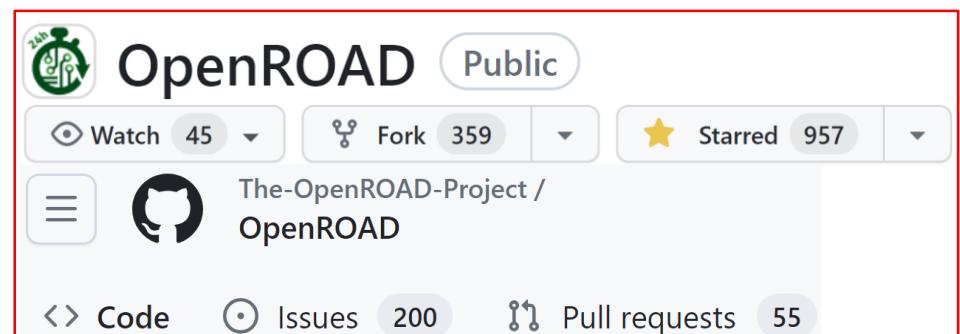
Partial Path



Full Path

And More Dimensions: Community

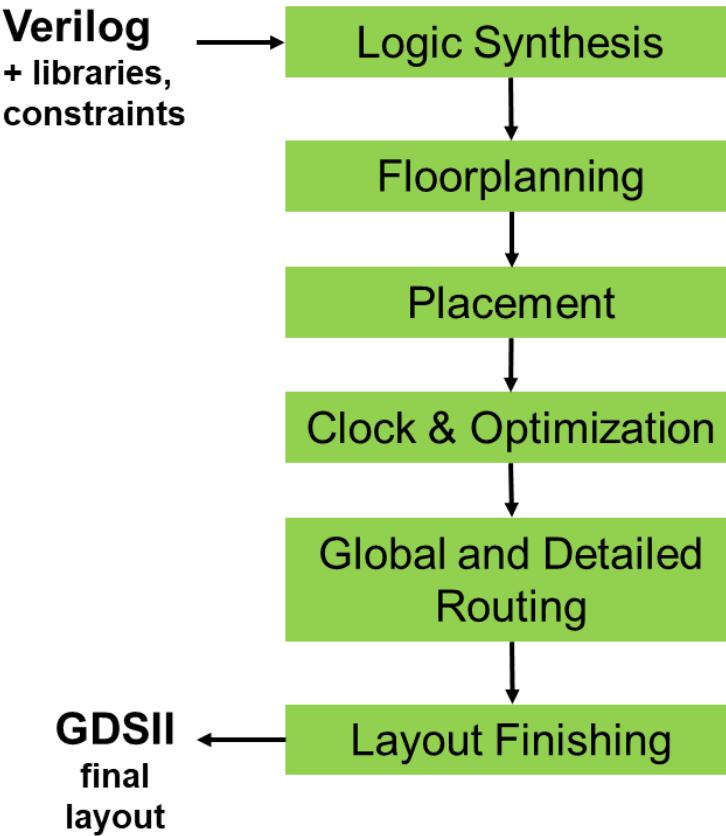
- Join the community !
 - Novice to Expert
 - Applications: Trust, 3DIC, AI/ML, ...



Agenda

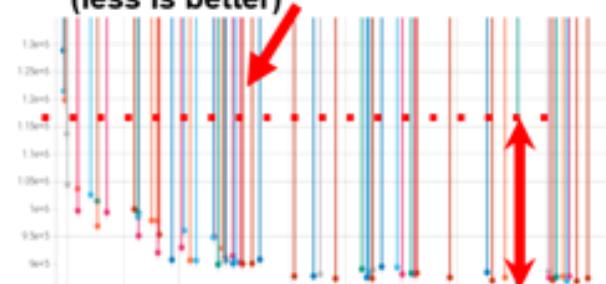
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High-Level Direction: Cloud, ML



- What if tool licenses are unlimited?
“COPILOT” = Cloud Optimized Physical Implementation using OpenROAD Technology
- ML challenge: predict failure and intervene
- + low-hanging fruits such as AutoTuner

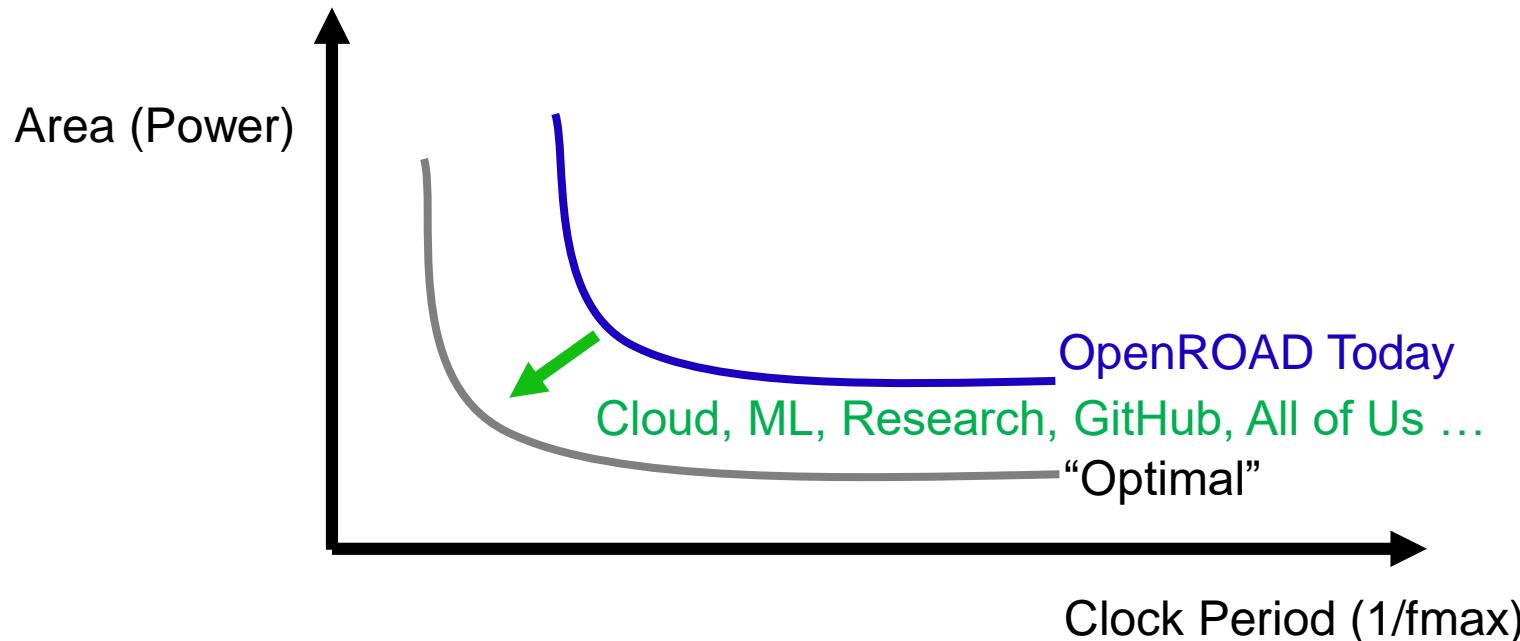
Default flow score = 1,174,346
Our Best Score = 855,373
(370 trials in total 500 #trials)
(less is better)



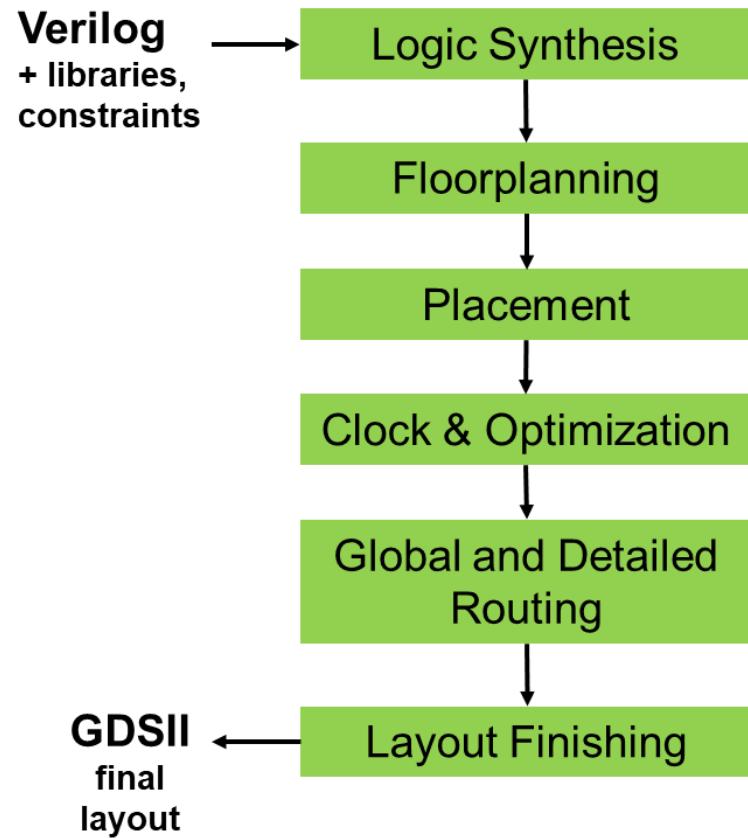
Improvement
WL 1003801um → 843258um (**-16%**)
Effective CP 20.935ns → 16.185 ns (**-23%**)
Total power 0.024 W → 0.0133 W (**-45%**)

IC Design and EDA = Optimization

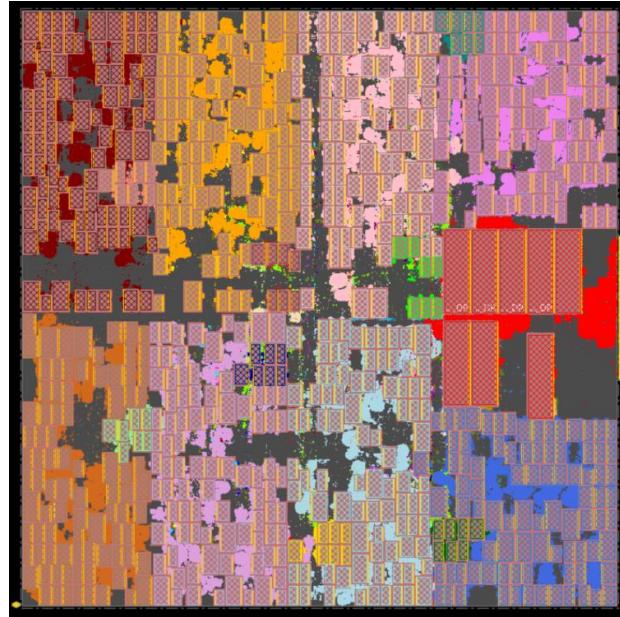
- Optimization of Power, Performance, Area, Cost...
... within design resources !
... boosted by AI / ML !



High-Level Direction: Early DSE (Arch, RTL)

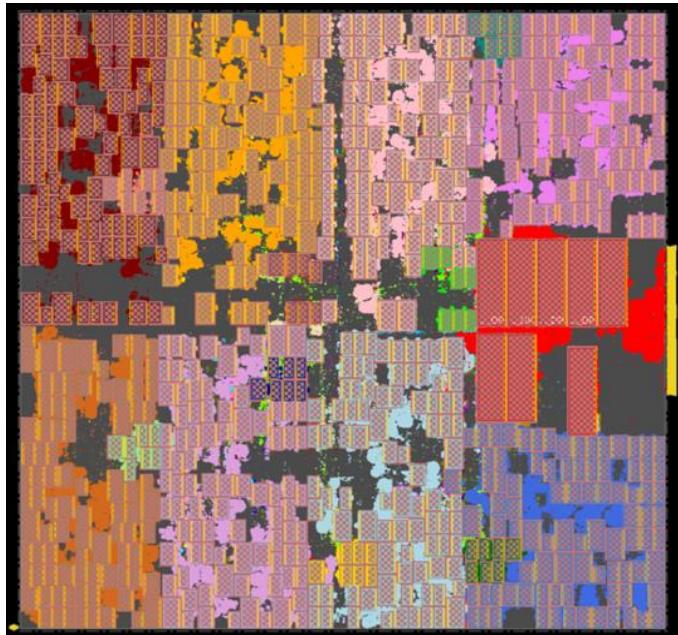


- Can we better explore architecture and SoC floorplan design spaces?
- Hier-RTLMP: /src/mpl2
 - RTL and dataflow-driven, human expert-like

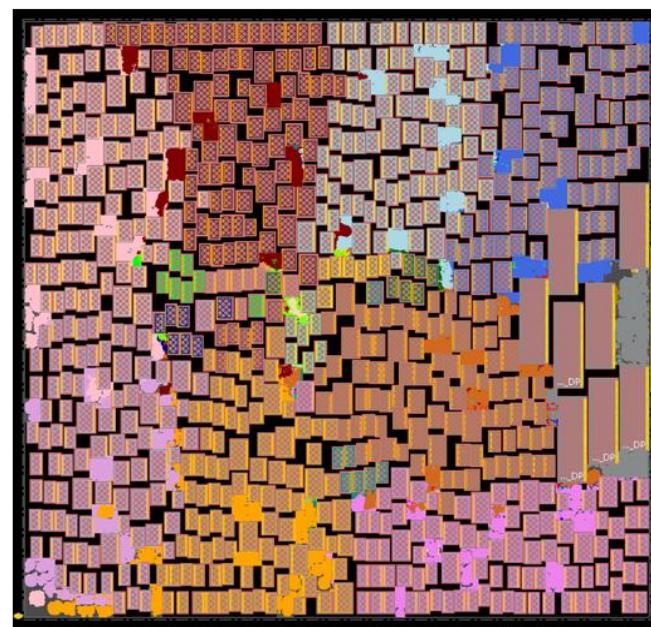


Hier-RTLMP vs. Commercial Macro Placer

- TABLA01 (GF12) **760 macros**



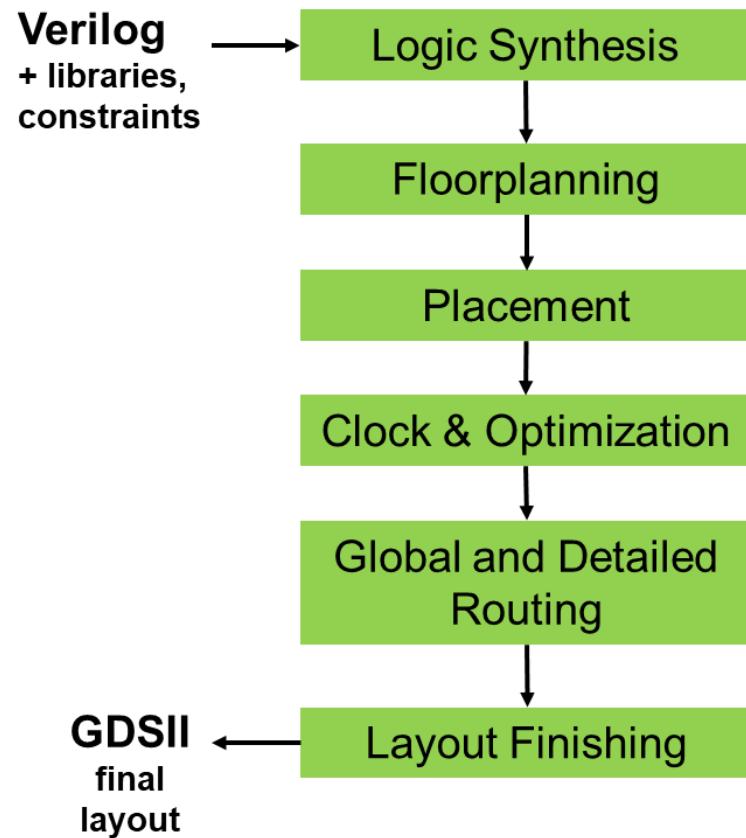
Hier-RTLMP (postRoute)



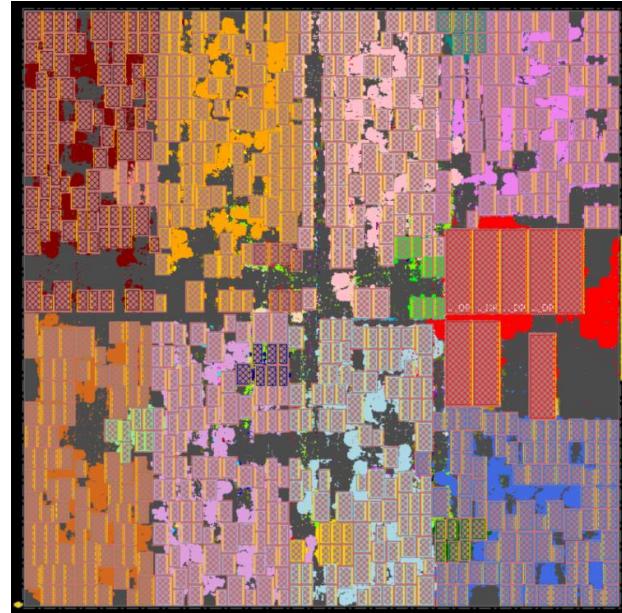
Commercial Macro Placer (postRoute)

Macro Placer	Std Cell Area (mm ²)	Power (mW)	WNS (ns)	TNS (ns)
Hier-RTLMP	0.160	640	-0.085	-0.417
Comm	0.165	689	-0.370	-92.246

Direction: Early Design Space Exploration



- Can we better explore architecture and SoC floorplan design spaces?
- Hier-RTLMP: /src/mpI2
 - RTL and dataflow-driven, human expert-like



- TritonPart: /src/par
 - Timing- and constraint-driven partitioner
 - Displaces hMETIS, KaHyPar

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- What is OpenROAD ?
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- Where are we going ? (The Roadmap)
 - Tool Development

OpenROAD Development

- How do we determine our priorities?
 - Align to recurring issues/requests
 - Strive for biggest impact to the most users
 - Ensure project sponsors, funders are getting what they want
 - Allow enough time, effort for each project to build code to last
- How do partners determine our priorities?
 - Drive tool development
 - Example: multi-height cell support
 - Support tool development
 - Gifts, contracts (for specific enhancements, user support)
- Many targets are awaiting resources
 - Improved timing awareness in GRT
 - Post-GRT repair ERC and timing
 - DFT (scan chains and reordering)
 - CCS
 - ...

Synthesis is a Priority

- **QOR from Yosys + ABC needs to be improved**
 - This has been very consistent feedback
 - Project focus has been on Netlist to GDS
- **Looking for some dedicated people to work on this**
- **Current thinking on prioritization**
 - System Verilog support
 - Reduction of gate count
 - Timing-driven operator implementation selection
 - Timing-driven resource sharing
 - Remapping after placement to improve timing

Other Current Priorities

- **CTS usability and QOR**
 - Dedicated developer time now going into CTS
 - Reduce need for manual parameter tuning
 - Hierarchical CTS (latency inside large macros)
 - There are still usability and quality issues with CTS
- **Preliminary UPF support**
 - Support of multiple power domains = long-standing request
 - UPF is a rich standard with many features
 - Starting with support of simple on-off domains
- **Exploiting more PPA optimization levers**
 - Multi-height cells, multi-bit FFs
 - Timing and power recovery: Gate cloning, VT swap

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 - Governance and Transition

OpenROAD DARPA Contract Ends 12/31/2023

- Sustaining the project and the development team has been top of mind
 - *How would things change if the OpenROAD project ended?*
- Substantial funding today is from industry gifts, and software development + support contracts
 - *E.g., hardware startups*
- Some structure is known:
 - Precision Innovations will continue to develop and support OpenROAD
 - A new OpenROAD Initiative foundation (non-profit) provides a path for philanthropic support

Precision Innovations, Inc. Overview

Company/Team Overview

- Principal industrial developer and integrator of the OpenROAD RTL to GDS ASIC/SoC Development solution
- Founded 2019
- Electronic Design Automation (EDA) veterans – 10 employees / contractors
- HQ – San Diego, CA.

History

- DARPA award for OpenROAD
- Key customers – Google and Intel
- Partners - Siemens and GlobalFoundries

Technology Overview

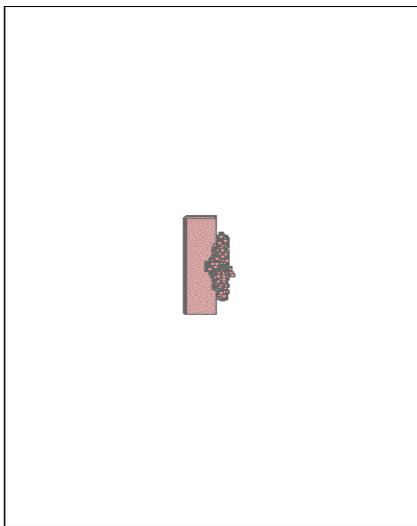
- OpenROAD is an EDA solution for hardware implementation of ASIC and SoC chips
- Proven (600+ tapeouts), open source, physical design solution.
- Used on designs down to 12nm
- Core competency: RTL to GDS EDA flows leveraging AI/ML for design space exploration and automated design implementation
- AI based Autotuner to maximize results
- Fast estimation / new design feasibility analysis
- Professional Support Solutions available.

The OpenROAD Initiative 501(c)(3) Nonprofit

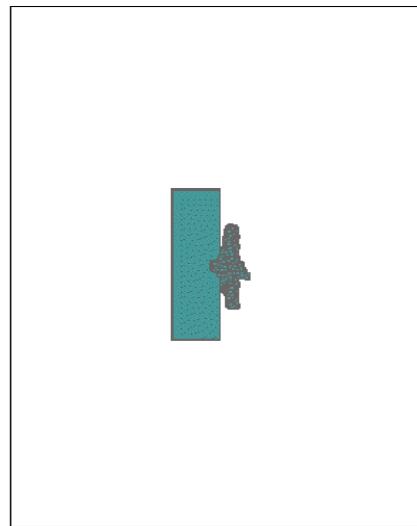
- **What is The OpenROAD Initiative** www.openroadinitiative.org
 - A 501(c)(3) public charity for the benefit of open source EDA and related technology
- **Founded in February 2023 by Tom Spyrou**
- **Vision: Foster open-source chip design, EDA projects, and programs that lower costs, democratize access to tools, provide training and accelerate innovation for the semiconductor industry**
- **Goals**
 - Continued development of OpenROAD and all open-source EDA
 - Development of open source PDKs both manufacturable and Proxy
 - Creation of education material teaching chip design
 - Training of new EDA developers via a high quality software system
- **Who would contribute**
 - Any person or organization interested in the continued development of the open design ecosystem

Agile Development on OpenROAD: Example

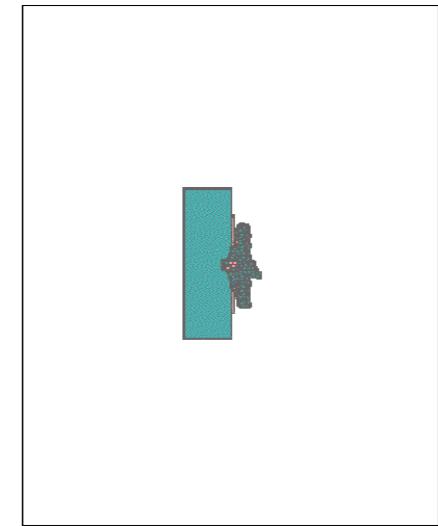
Top Die



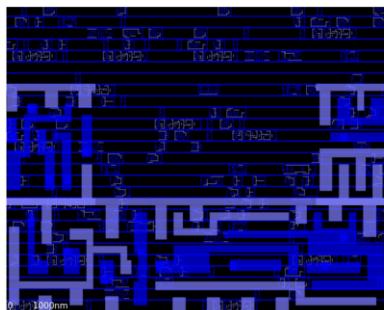
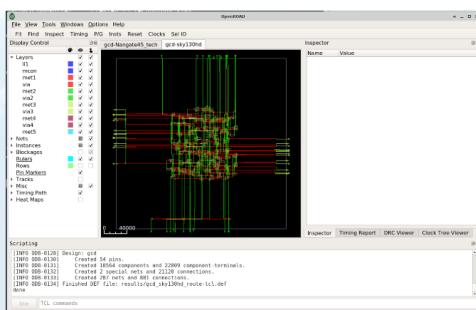
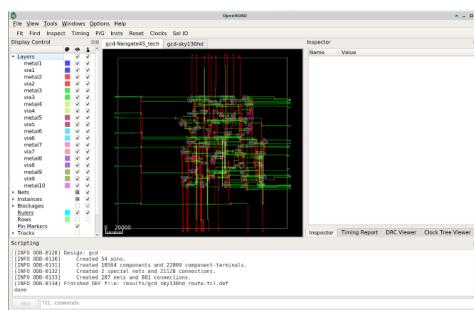
Bottom Die



Both



ICCAD-2023 Contest
testcase, 32 macros
and 740K stdcells

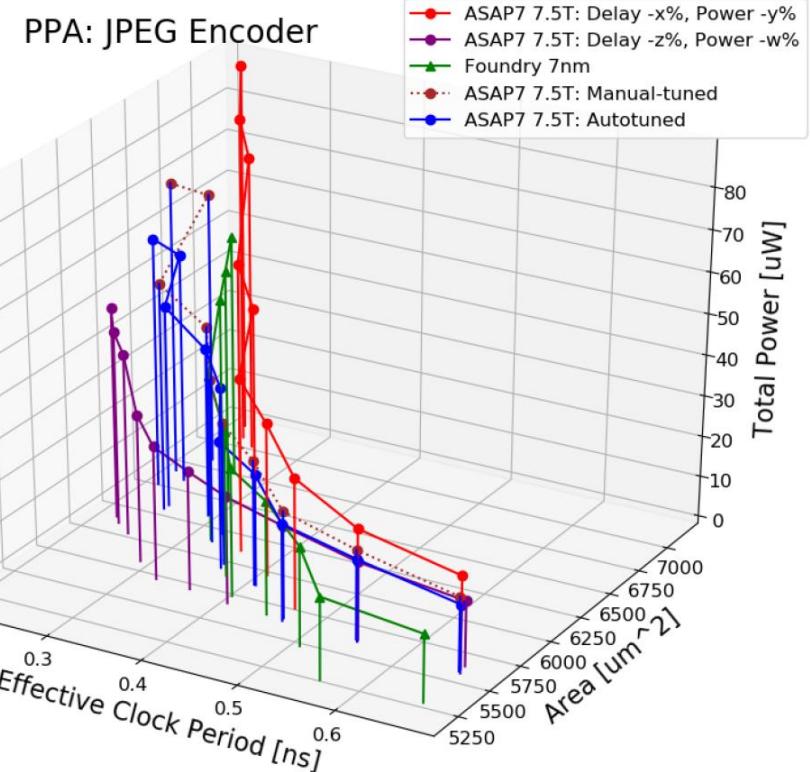
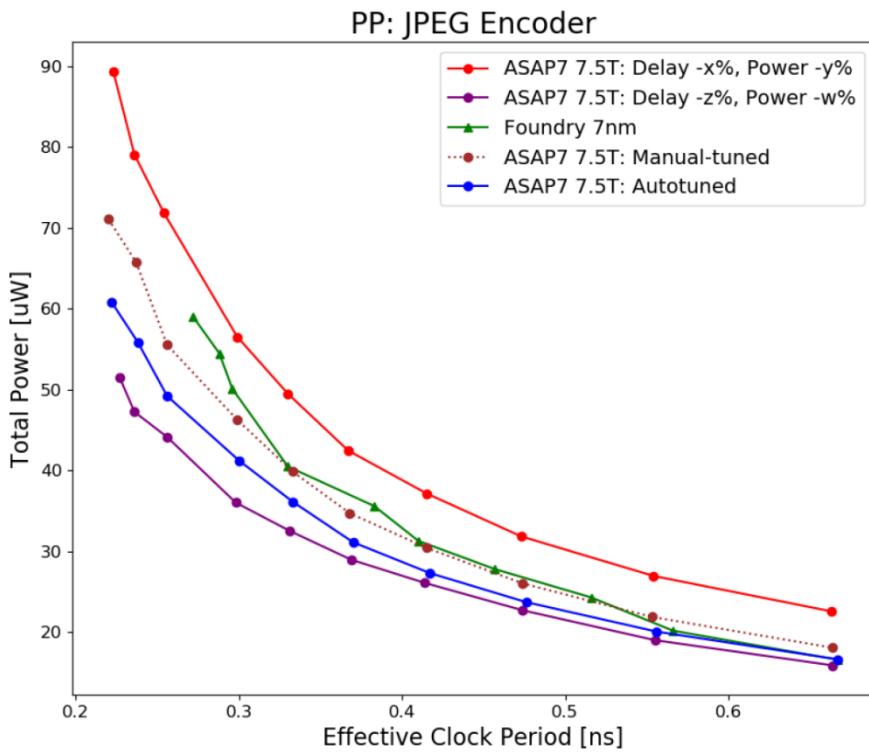


Placement of SKY130 design on one die and ASAP7 design on second die



DB/GUI enhancements: 2-tier P&R views

Building Out Proxies: Example



- **Scaled ASAP7 PDK** and enablement can be used to bound power and performance of foundry 7nm
- Area scaling can match foundry 7nm outcomes
- Autotuning of scaling factors has been implemented

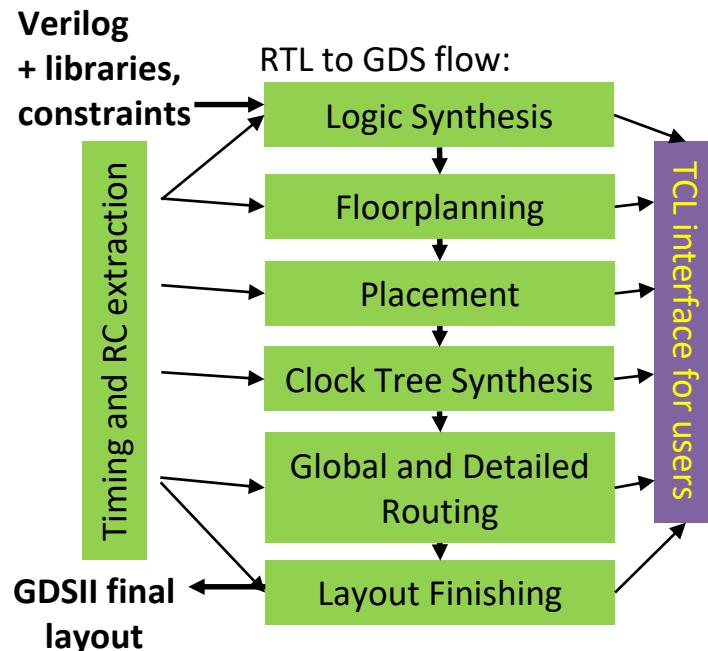
Agenda

- What is OpenROAD ?
- How did we get here ? (The Journey)
- Where are we going ? (The Roadmap)
 - Tool Development
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 - ML Enablement for OpenROAD

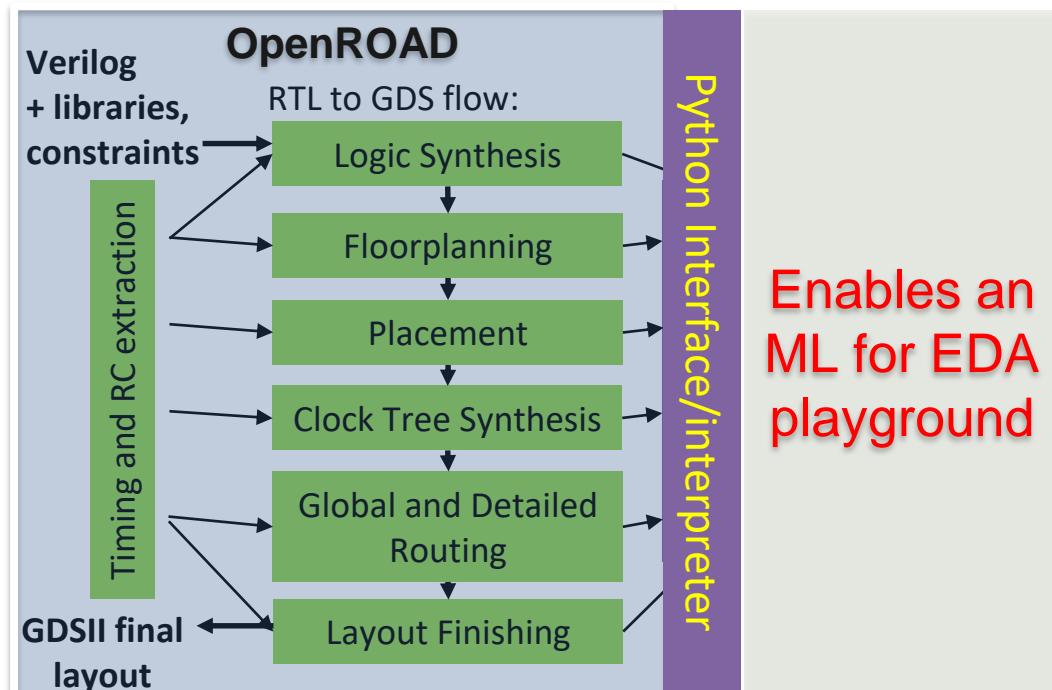
What Exists Today in OpenROAD?

- OpenROAD: Open-source EDA enabling AI for EDA

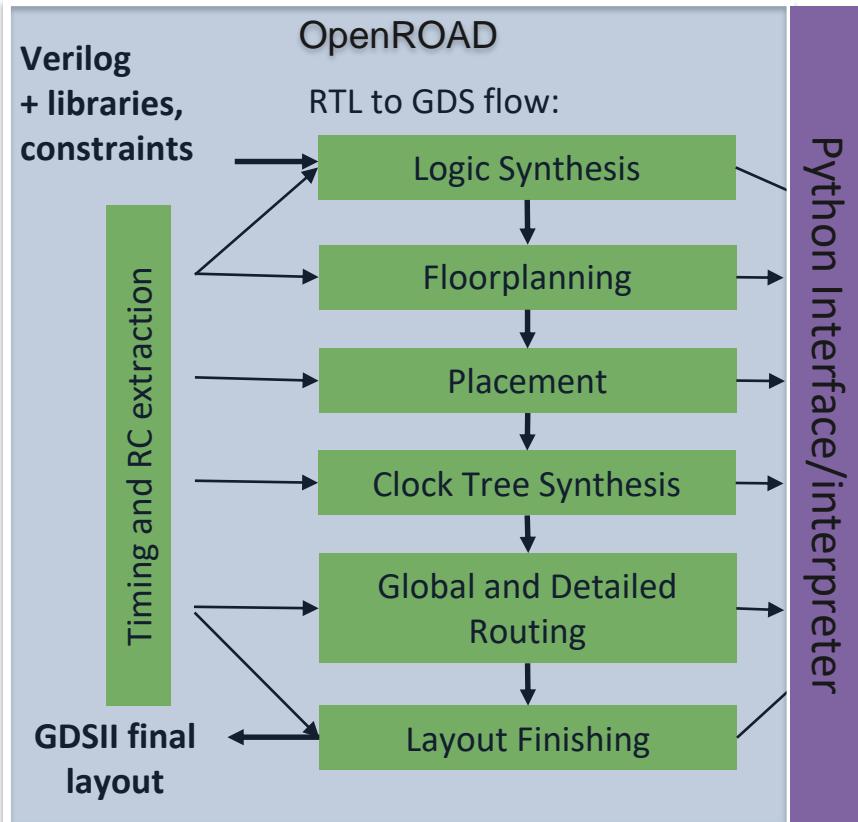
What do designers/users work with?



What can they also work with?



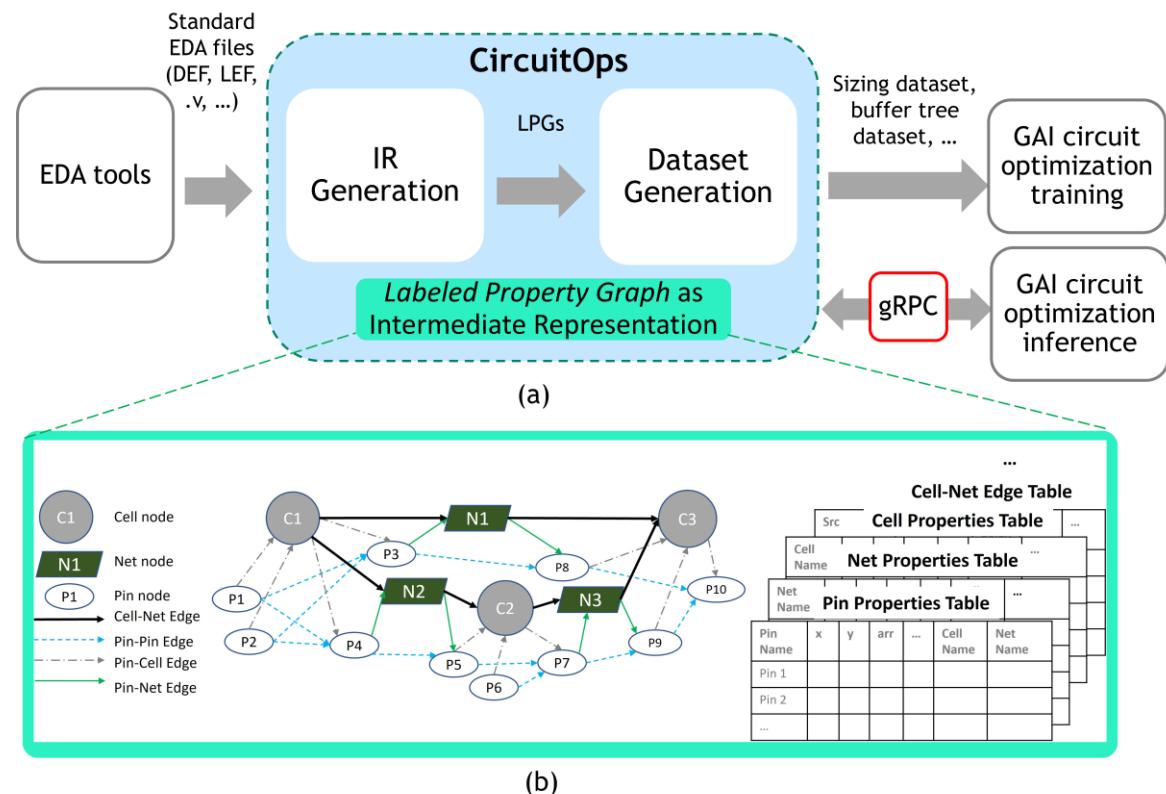
Vision: OpenROAD as an ML for EDA Playground



Enables an ML for EDA playground

- **User friendly data formats**
 - Standard ML-friendly data representation formats
- **Python APIs on existing EDA tools**
 - Enable data generation in ML-friendly format
- **Callbacks and EDA database writebacks from the ML environment**
 - Node and edge transformation to automatic EDA tool python API translation for novice EDA tool users

ML for EDA Playground: CircuitOps Data Format



- ML-friendly data representation format

- Intermediate representation of EDA data as labeled property graphs (LPG) represented as deep graph library (DGL) object or graph tool which integrates easily with PyTorch
- Each node has associated relational tables that store node features, e.g., pin slack, transition, etc.

ML for EDA Playground: ML-centric APIs

1) `all_slacks = ord.get_property(list_pins, "rise_slack")`

where `all_slacks` is a numpy array.

2) `graph_design = ord.get_netlist(list_insts, properties)`

where `graph_design` is a DGL graph object where all nodes are instances in `list_insts` annotated with `properties` as node/edge features.

3) `cong_map = ord.get_map(map=congestion, resolution=1um)`

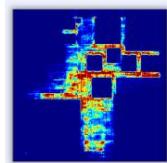
where `cong_map` is a 2D numpy array representing a heat map.

Examples of
image-based ML
data extraction

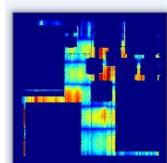
Congestion



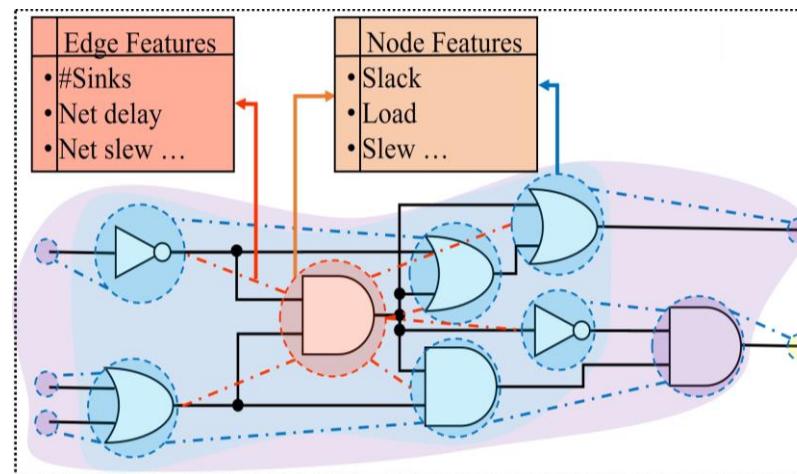
DRC violations



IR drop



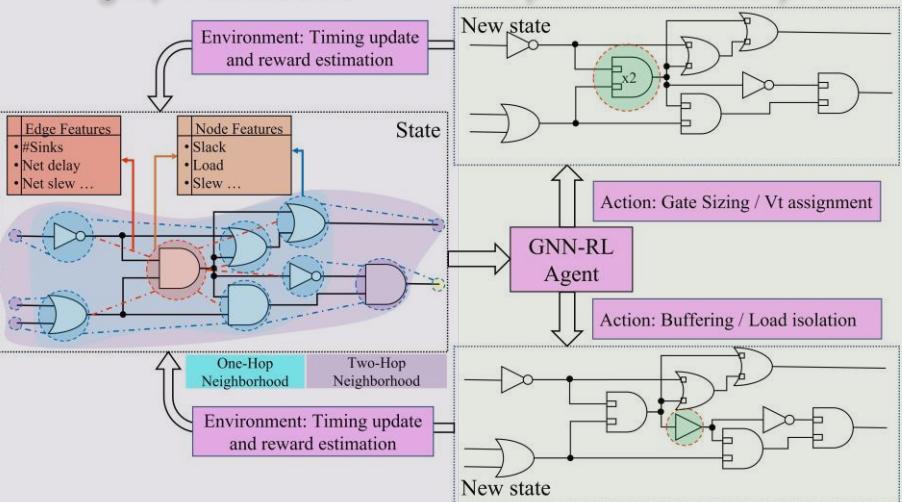
Examples of graph-based data extraction:
node, edge features



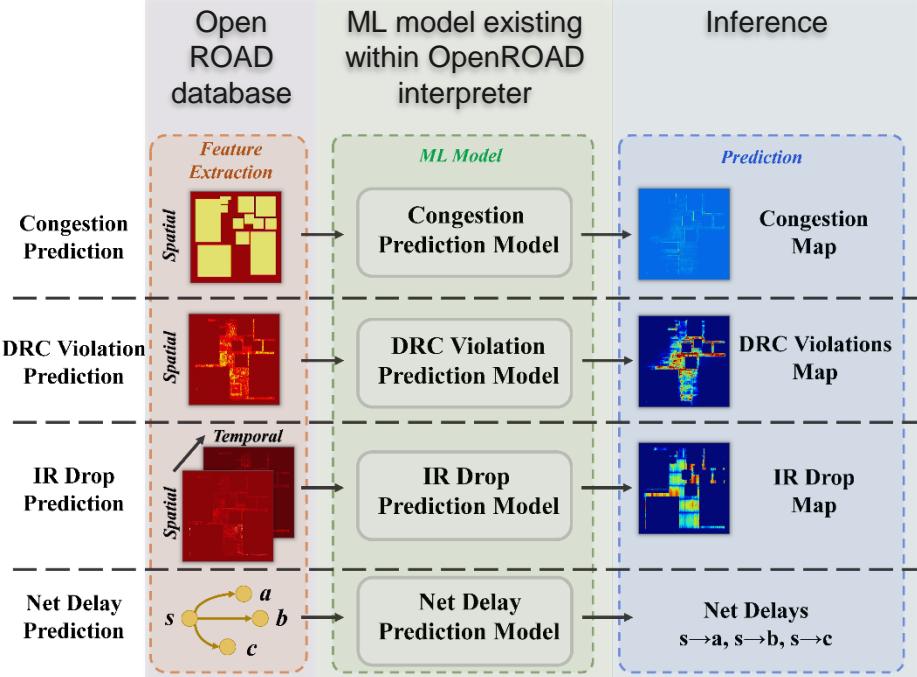
ML for EDA Playground: Example Optimization and Analysis

ML-based optimization by training **RL agents *within* OpenROAD**

OpenROAD CircuitOps graph database



ML-based analysis for OpenROAD algorithm optimization

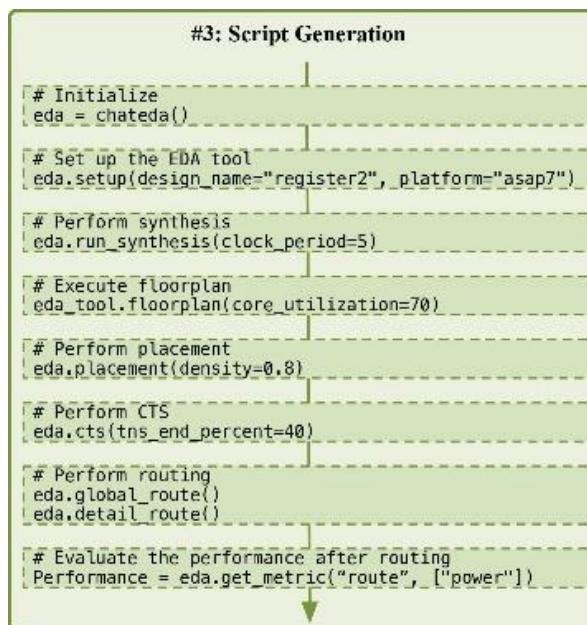
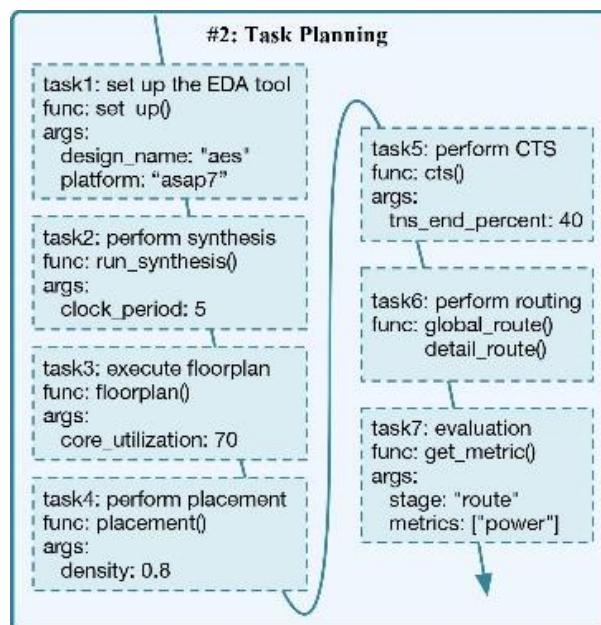


ChatEDA: Autonomous EDA Agent Empowered by LLM

Conversational interface for human-toolflow interaction
→ improved productivity

#1. User Requirement

For the design named “aes” on the platform “asap7”, please perform synthesis with a clock period of 5, followed by floorplan with a core utilization of 70%. Then, execute placement with a density of 0.8. Next, proceed with CTS to fix 40% of violating paths. Finally, evaluate the performance after routing using “power” metric.

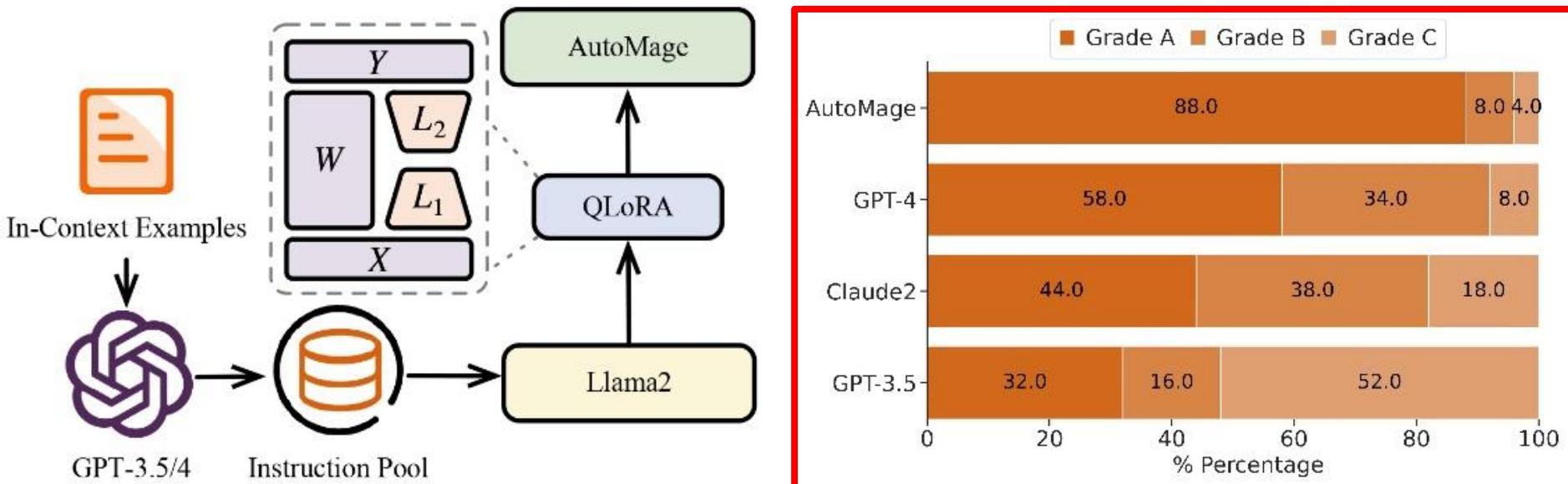


Workflow

1. (user) natural language input
2. (ChatEDA) task planning
3. (ChatEDA) script generation
4. (OpenROAD) task execution

LLM with EDA Domain Knowledge

ChatEDA is based on an LLM + fine-tuning with EDA domain knowledge
→ outperforms GPT-4 in various domain-specific tasks



For more details, please refer to the MLCAD'23 paper (arXiv: 2308.10204) or contact byu@cse.cuhk.edu.hk

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 - Background Thoughts

Background Thought #1: Bars Matter

- **Is it good enough?**

- Relevance (functionality, data, quality of results)
 - Foundry N5 vs. [ASAP7](#) / [ASAP5](#)
 - Commercial SP&R (PPAC) vs. academic/open-source SP&R
 - Commercial product designs vs. open hardware designs
- Quality, continuous improvement
- Support

- **Can I rely on it?**

- Ph.D. students vs. design/EDA professionals
- Documented, maintained, supported
- User community
- Availability, terms and conditions

“more wood behind fewer arrows” ?

Background Thought #2: Infrax = Commodity

- **Claim: Infrastructure is not differentiating**
 - This means *Pick one, move on*
- **For (digital) IC EDA and design:**
 - Data model, DB, incremental STA, readers/writers, standards support, PDK support, logging, scripting, parallelization, GUI ... **should be like plumbing and utilities**
 - “Don’t need to think about these” is also a Bar !
- **See:**
 - OpenDB
 - METRICS2.1
 - OpenROAD
 - ...

“more wood behind fewer arrows” !

Background Thought #3: Don't Ignore Proxies!

- What else blocks adoption of open-source EDA?
 - Validations (of relevance)
 - Root-cause blocker: “not sharable”
- Ex: foundry N5 PDKs, enablements **are not sharable**
 - grow ASAP7 / ASAP5 PDKs, enablements into **research proxies**
- Ex: commercial EDA SP&R tools/IP **are not sharable**
 - can grow OpenROAD, etc. into **research proxies**
- Ex: commercial IPs **are not sharable**
 - can grow NVDLA, OpenPiton, Chipyard, etc. into **research proxies**
- **Improve proxies to unblock ourselves !**

“A journey of a thousand miles begins with a single step”

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- Summary

Summary

- **OpenROAD is now in its 6th year**
 - “Going viral” in many dimensions: community, education and workforce development, commercial use
- **December 31, 2023: formal end of the DARPA project**
 - Precision Innovations, Inc is the core R&D organization
 - OpenROAD Initiative 501(c)(3) foundation for philanthropic support
- **Thank You:** On behalf of the entire project, heartfelt thanks to so many of you in the audience for support, feedback, and trust in OpenROAD and its mission

Let's continue the journey !

Some Links

(talks are always posted at vlsicad.ucsd.edu)

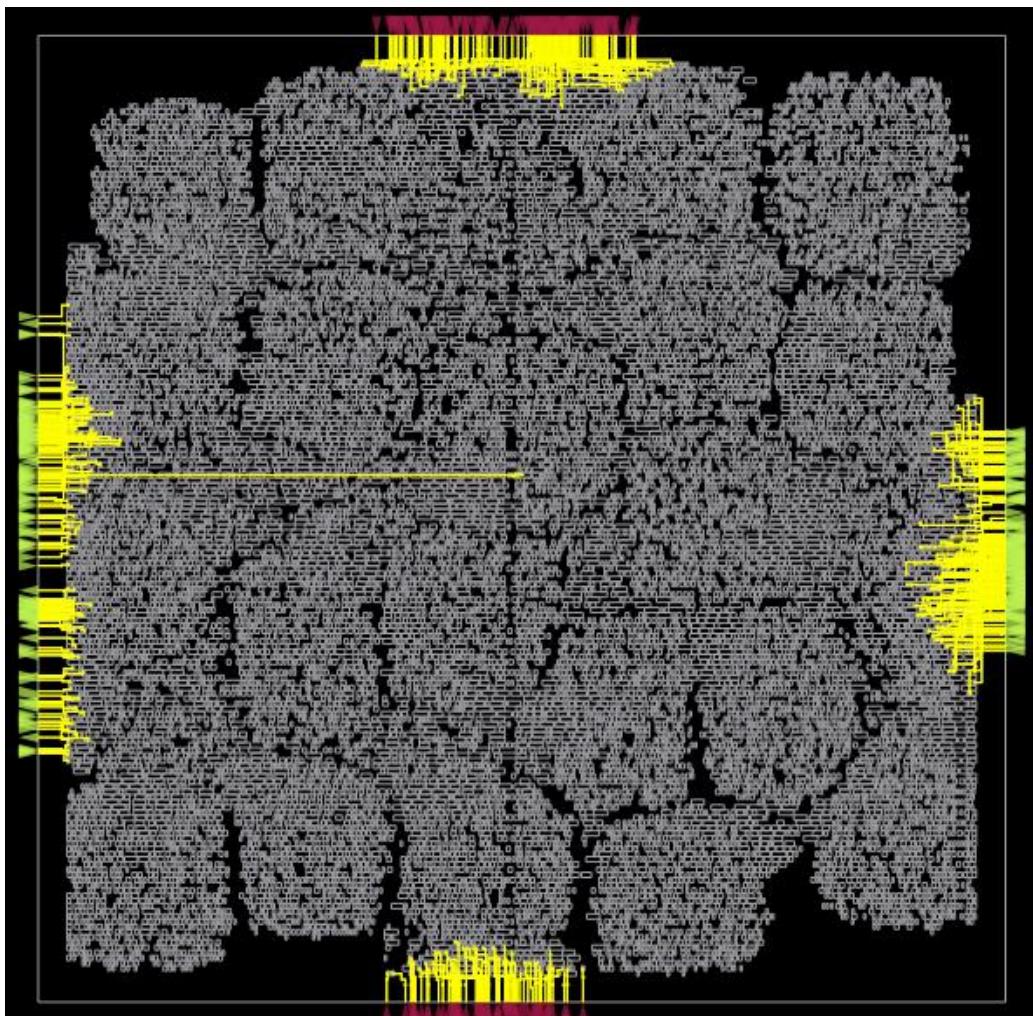
- “Leveling Up: A Trajectory of OpenROAD, TILOS and Beyond”, *Proc. ISPD*, March 2022. [.pdf](#) [.pptx](#)
- “Our Real Scaling Challenge: People”, ACCESS-CEDA seminar, Sept. 2022. [.pptx](#)
- “Bars and Barriers to Overcome for Shared ML EDA Infrastructure”, NSF Workshop on Shared Infrastructure for Machine Learning EDA, March 2023. [.pptx](#)
- Thoughts on open source in EDA
 - 2002: “Toward CAD-IP Reuse: The MARCO GSRC Bookshelf of Fundamental CAD Algorithms” [[.pdf](#)] (also: [\[.pdf\]](#))
 - 2019: “Looking Into the Mirror of Open Source” [[.pdf](#)]
 - 2020: “Open-Source EDA: If We Build It, Who Will Come?” [[.pdf](#)]
 - 2021: “The OpenROAD Project: Unleashing Hardware Innovation” [[.pdf](#)]
 - 2022: “The OpenROAD Project: A Foundation for Research and Education in EDA and IC Design” [[.pptx](#)]
 - 2022: “A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping”, [[.pdf](#)] [[.pptx](#)]
 - 2023: Talk on OpenROAD at the 3rd Open-Source Design Automation Workshop (OSDA-2023) [[.pptx](#)]
- <https://theopenroadproject.org> and <https://github.com/The-OpenROAD-Project>

THANK YOU !



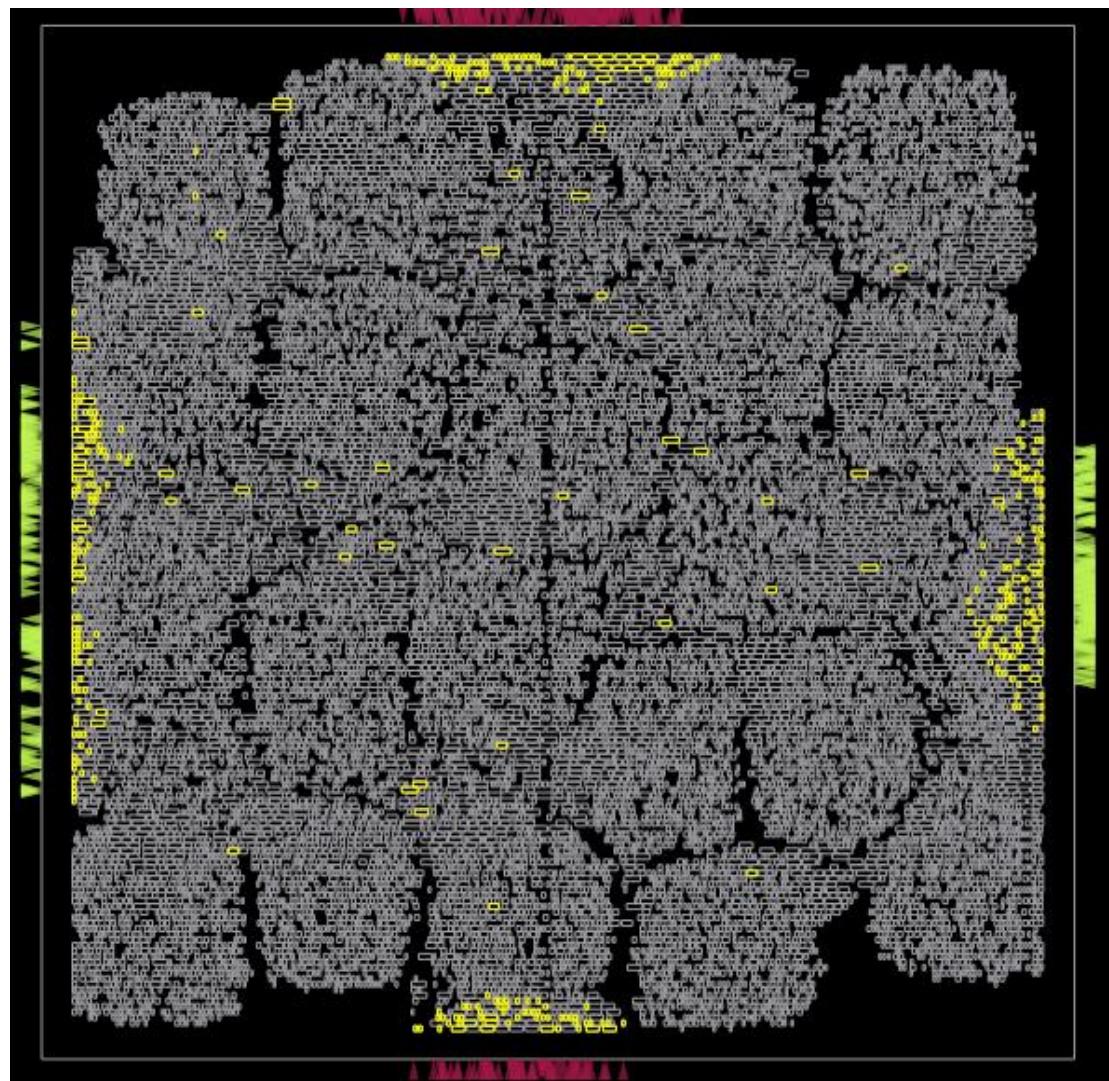
BACKUP: GUI

GUI: Select command usage to find all IO nets



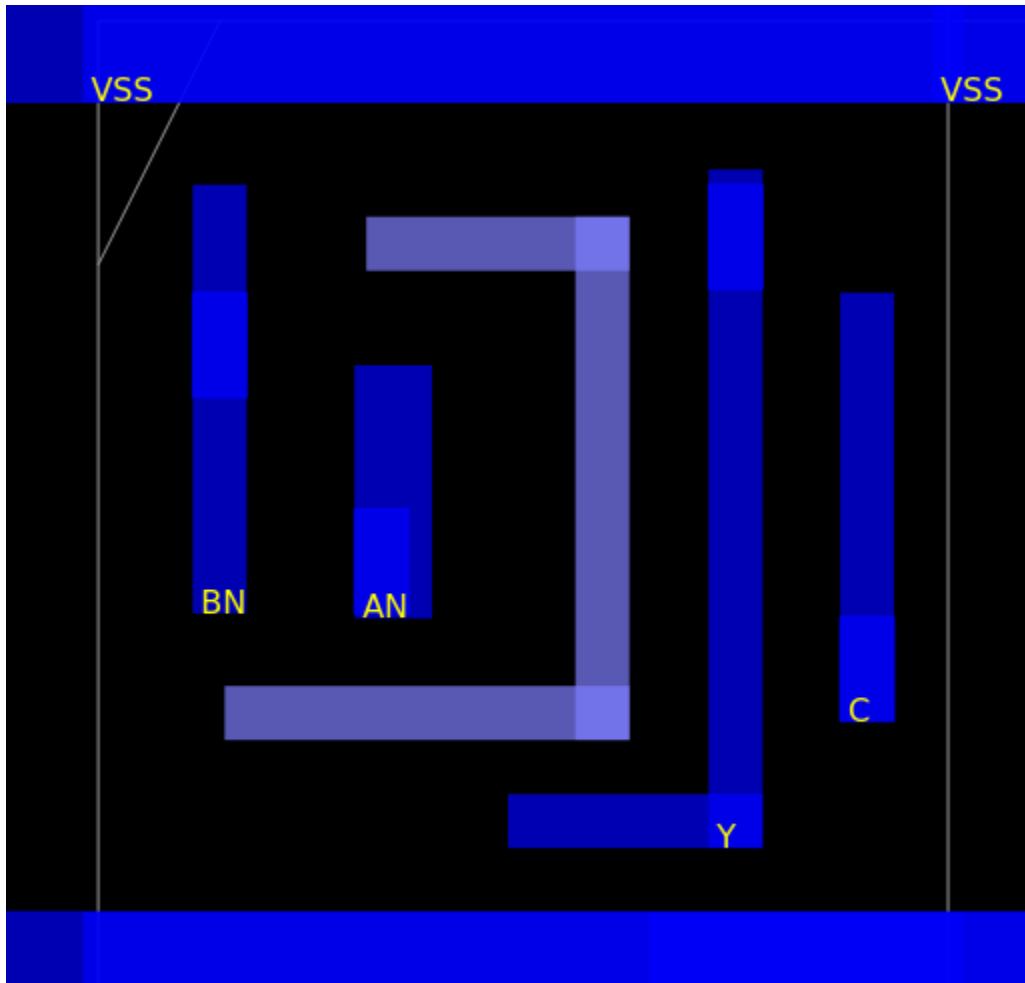
```
select -type Net -filter  
BTerms=CONNECTED
```

Find instances related to timing optimization

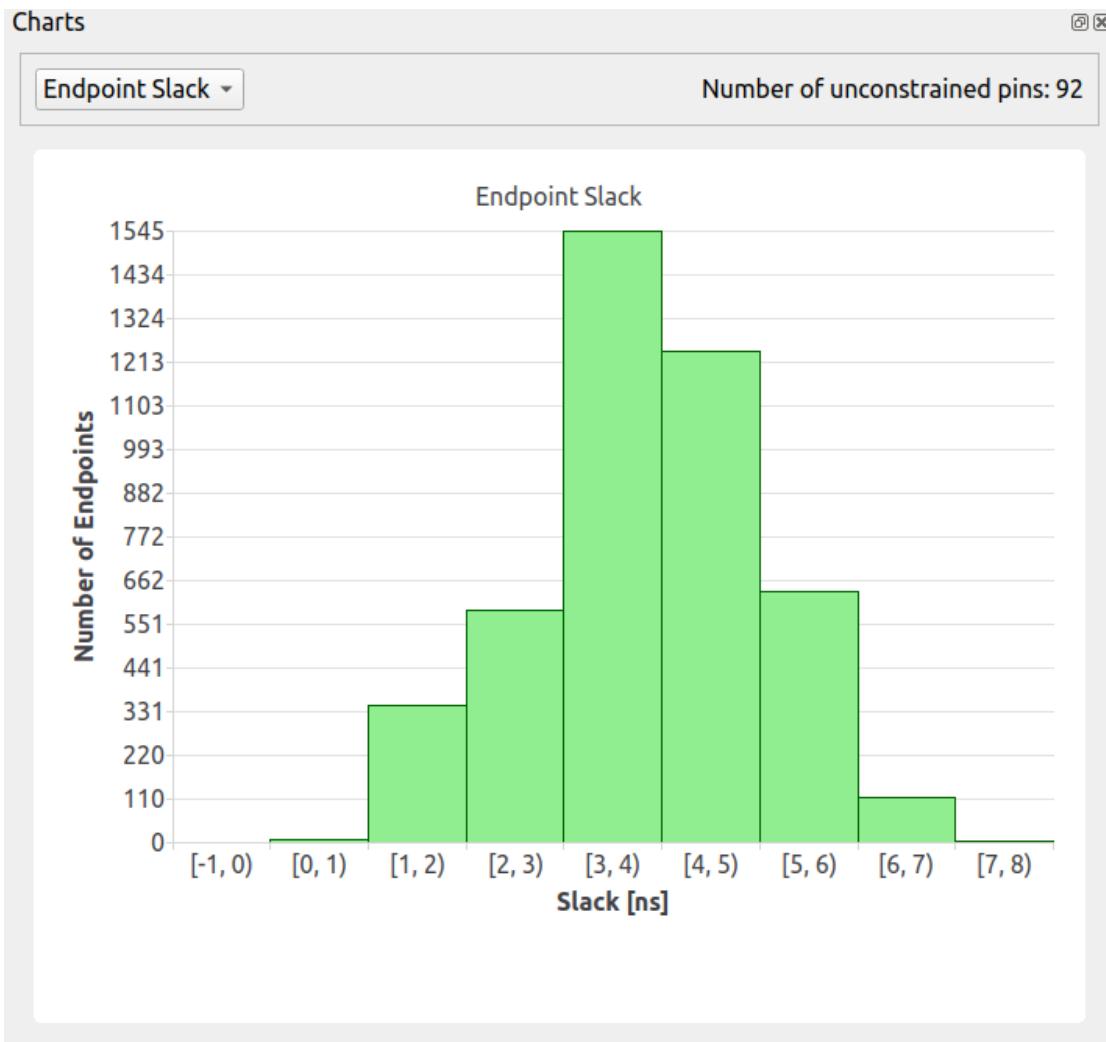


select -type Inst -filter "Source type=TIMING"

Pin Labels



Slack Histogram



This Past Tuesday

Axel Kloth • 2nd
Founder & CEO at Abacus Semiconductor Corporation & V...
3h •

We at [Abacus Semiconductor Corporation](#) use this open source EDA toolset because it enables our **#innovation** in **#processors** for **#hpc** and **#AI** and **#machinelearning** creating and engineering our post-von-Neumann and post-Harvard architecture processors. Thanks to [Tom Spyrou](#) and [Matt Liberty](#) of the OpenROAD Project for making this available and supporting it.

VLSI Professional Group
Kumar Priyadarshi • 2nd
5h •

Join

Building your own chip used to be a very expensive and complex process. However, thanks to the OpenROAD Project and other open source initiatives, it is now possible to build your own chip for free. In this post, we will walk you through the steps involved in building your own chip using free tools.



7 steps to Design and Fabricate Your Chip Using Free Tools - [techovedas](#)
[techovedas.com](#) • 4 min read