PG – 664

I Semester M.C.A. (Two Years Course) Examination, May/June 2025
(CBCS) (2020 – 21 and Onwards)
COMPUTER SCIENCE
1MCA3 : Computer Organisation and Architecture

Time : 3 Hours Max. Marks : 70

Instructions : *1) Answer **any 5** questions from Part – **A**.*
*2) Answer **any 4** questions from Part – **B**.*

PART – A

I. Answer **any five** questions. **(5×6=30)**

1) Convert the following :
   i) $ACF_{(16)}$ = _____ (10)
   ii) $304.25_{(10)}$ = _____ (2)
   iii) $101101.11_{(2)}$ = _____ (10)
2) Write the differences between Half Adder and Full Adder.
3) Explain the working of master slave flip-flop.
4) Explain different instruction formats with an example for each.
5) Describe data transfer methods using DMA.
6) Briefly explain memory hierarchy.
7) What is memory mapped I/O and program controlled I/O ?
8) Explain different types of ROM.

PART – B

II. Answer **any 4 full** questions. **(4×10=40)**

9) a) Minimize the following expression
   $F(A, B, C, D) = \sum(5, 6, 9, 13, 15) + d(1, 7, 14)$. **5**
   b) Explain error detection using hamming code. **5**
10) a) Implement the following boolean function using 8 : 1 multiplexer
   $F(A, B, C, D) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$. **5**
   b) Explain instruction level parallelism in detail. **5**

P.T.O.

11) a) Differentiate between RISC and CISC. 5

b) Content of a 4-Bit register is initially 1101. Register is shifted six times to the right with serial input 101101. What is the content of the register after each shift ? 5

12) a) What is cache coherence problem ? Discuss different cache coherence approaches. 5

b) Explain the basic organization of microprogrammed control unit. 5

13) Explain distributed memory MIMD architecture with a neat diagram. 10

14) Briefly explain inter process communication and process synchronization. 10
