



Final Year Report - FYP (A3311-232)

**Survey of Intelligent Reflecting Surfaces and
Localization for Wireless Systems**

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Abstract

The project is driven by the motivation to investigation tradeoffs in location information. Localization techniques can be used to triangulate a user's position, through methods like identifying patterns in the time-varying data. A suitable localization technique in Wi-Fi bands can be found in the form of Intelligent Reflecting Surfaces (IRS). IRSs are array-like structures that draw upon the operating principles of patch antennas and traditional reflectarrays. They are effectively beamformers that use phase/amplitude shifts to reflect the received signal, but do not typically emit any wireless power of their own.

This project explores the optimization of a single fully-passive IRS that performs localization functionality. The IRS rapidly performs phase-shift functionality in real-time. In the IRS array, the unit cells communicate data in a shift-register motion, ensuring that it can be easily scaled to a reasonable amount of unit cells. The implementation of the control circuit and relay signals is demonstrated at the printed circuit board (PCB) level, along with the unit cell design.

Several important elements of the core control circuit are realized as discrete components on the PCB. After undergoing electrical rule checks, the prototype serves as a proof-of-concept of a fully asynchronous control system for the IRS. Differences between the integrated circuit (IC) and PCB implementations are surveyed, including cost, dimensions etc.

A setback was that the PCB footprint exceeded the 2x2 metallic plate size, which is one unit cell, and the metallic element size had the limitations of being influenced by the frequency of operation (5.8 Ghz). Nevertheless, the literature surveyed in this paper assists in future evaluation of the IRS use case in localization.

Acknowledgment

Firstly, I would like to express my heartfelt thanks to Assoc. Prof Soong Boon Hee, who supported me with the ideation, and helped me with some of my queries and concerns.

I thank the authors of numerous literature listed within this project report, since it builds upon their contributions. Additionally, credit is due to some key researchers, namely Emil Björnson, Rui Zhang amongst others, for sharing their insights & positioning complex antenna/IRS domain knowledge such that it is accessible as a research topic. I am grateful for the numerous online resources/tooling associated with circuit simulation, antenna design, without which this project would not have been possible, and which are primarily curated by engineers from around the world.

My original motivation for this project is credited to Prof Lee Yee Hui and Prof Lu Yilong for conducting the intriguing course on Wireless Systems Design (EE4109) which covered antenna systems and parameters in-depth, inspiring me to take on wireless systems for this final-year project.

Finally, I sincerely express my gratitude to my mother for her enduring support during the challenging times, and my friends / faculty mates from EEE NTU.

Jan 2025

Acronyms

5G	5 th Generation (of cellular network technology)
AP	Access Point
BS	Base Station
CRB	Cramér-Rao bound
CSI	Channel state information
DOA	Direction-of-arrival
FPGA	Field-programmable gate array
IRS	Intelligent Reflecting Surface
LAN	Local Area Networks
LOS	Line-of-Sight
MIMO	Multiple-Input Multiple-Output
nLOS	Non-Line-of-Sight
SNR	Signal-to-noise ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
PEB	Position Error Bound
PCB	Printed circuit board
tDoA	Time-Difference of Arrival
WAN	Wide Area Networks

Symbols

B	channel bandwidth in Hz
C	channel capacity / maximum rate of data in bits per second
S	received signal power
t_{total}	total timeframe for power analysis
t_{pilots}	total time to transmit and receive pilot signals at the BS
$t_{processing}$	total channel noise power across bandwidth B
N	

Chapter 1: Introduction

1.1 Background

Modern communication networks, such as that of Wi-Fi 802.11ac, necessitate a highly interconnected infrastructure, consisting of base stations (BS), access points (AP), and the connected users, User Equipment (UE). They allow multiple clients on the same network to communicate with each other, often in a full-duplex fashion. Recent years have observed huge surges in traffic from streaming services, internet browsing etc.

The drive for better information transfer can be quantified by the Shannon Capacity Theorem, which “defines the maximum amount of information, or data capacity, which can be sent over any channel or medium”, including wireless. This can be expressed by the relation $C = B \times \log_2(1 + S/N)$, where C is the data capacity in bits/s [1]. This is the hard upper limit for data transmission rates that wireless technologies are seeking to maximize, mostly by improving received beams and ensuring good signal-to-noise ratio.

It is beneficial to examine large-scale wireless systems which encompass large frequencies, namely wireless MIMO. This encompasses Massive MIMO systems, which feature massive antenna arrays that increase throughput. In the local Singapore context, the telco company Singtel rolled out a deployment of massive MIMO to serve its 2.6 GHz (LTE) spectrum in 2017 [2]. Subsequently, the telco invested in better radio provisions in the form of AIR 3268, being significantly less bulky and consuming 18% less energy than earlier generations, to build up its 5G network [3]. These investments demonstrate the keenness of the industry to invest and reflects the added demands on current infrastructure.



Fig. 1. Massive MIMO system. Adapted from [4]

However, the issue of high upfront cost and energy consumption remains, and for reliable service, the issues of backhaul, interference management must be solved with added infrastructure [5]. Moving into the indoor domain, short-range Wireless Local Area Networks (LAN) operate on similar principles, where clients can connect to a Wireless Access Point to gain access to the network, or internet.

Improving wireless networks in the 5GHz operating frequency are of particular interest, because they offer greater speeds (typically ~800 Mbps) and offer less co-channel interference. However, 5GHz waves are notably worse at penetrating solid objects, and scaling up the antenna array size (like in MIMO) is not as feasible in short-range settings due to the footprint and power consumption.

Numerous research has emerged on Intelligent Reflecting Surfaces, or IRS for short. IRS is akin to an array of reflectors for electromagnetic waves, operating via electronic phase shifters. It acts as a supplement to both outdoor long-range networks, and indoor Wi-Fi networks. The benefits are promising where the direct line-of-sight (LOS) signals from the BS may be heavily attenuated, e.g. in a typical commercial-size building which has dense environments, and where the network nodes are often isolated behind concrete walls.

1.2 Motivation

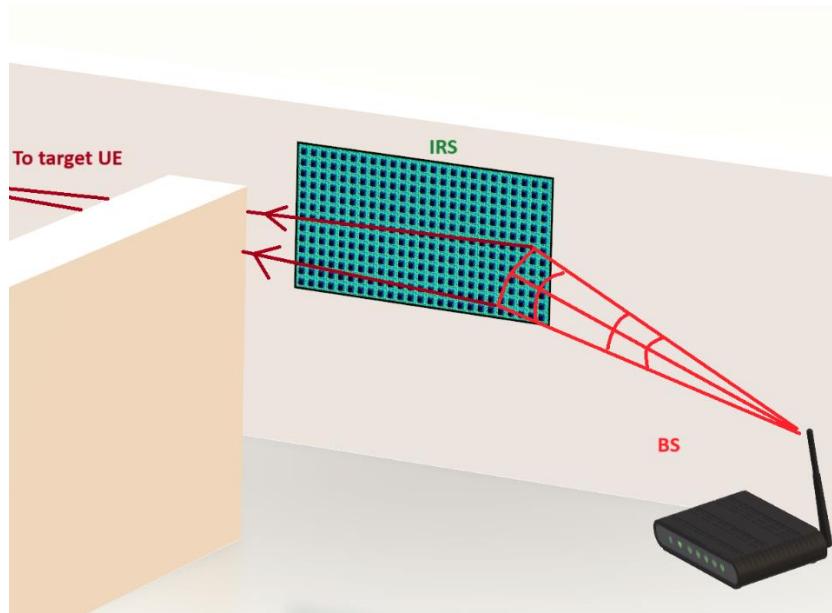


Fig. 2. IRS affixed on a wall

An integrated system with a single BS, IRS and user equipment (UE), will outperform a system without IRS in scenarios where it is optimized, due to less complicated interference management. IRS has the potential to reduce the complexity of current heterogeneous wireless networks, allowing the system to serve more UEs, especially in indoors environments. Another key reason to undertake IRS infrastructure is due to the massive reduction in power consumption, since less active BS relays are needed for backhaul.

It remains a research challenge to generalize an optimal over-arching solution for IRS in most situations. A direction was obtained for this project when I identified that proposed channel estimation schemes which are imperative for wireless communication, involved the BS and UE sending out pilot signals, before the IRS-related channels could be estimated by cancelling out the BS-UE direct channels. Then, the differing wireless channels necessitate the IRS physically changing its transmission characteristics; in this case, by using phase shifts.

This process of channel estimation is very environment dependent. There is a particular use-case for the IRS benefitting from such environmental optimization – localization, which is identifying the rough location of the receiving node from IRS. Various methods have been proposed, and an especially promising method uses Direction of Arrival (DoA) to triangulates the position of the UE. Notably, before localization is performed, channel estimation must occur to create the desired IRS reflection, and thus the project must take that into account.

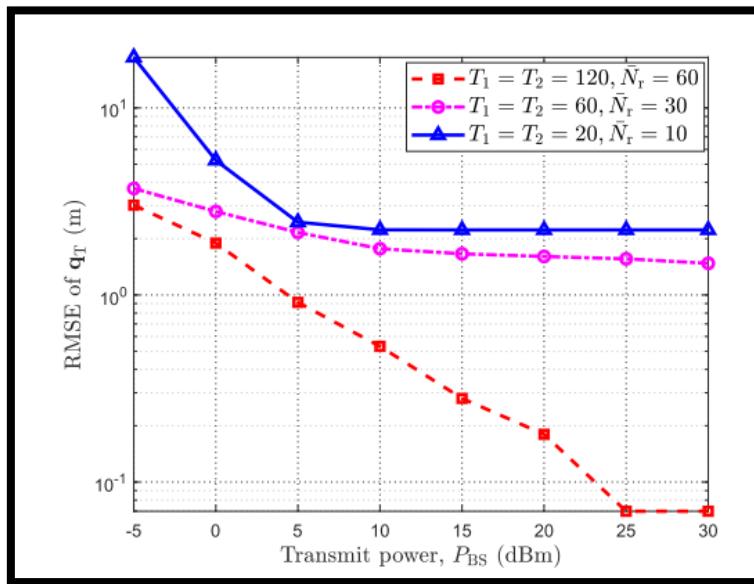


Fig. 2. Sub-meter accuracy for $N_r = 60$ elements, red dotted line. Adapted from [3, p. 10]

Competing localization techniques employ other EM frequencies like satellite GPS, Bluetooth, Zigbee etc. However, these come at the cost of either requiring specific hardware, or lower accuracy indoors. [2] IRS-enabled localization for the 802.11ax standard matches or surpasses the positioning accuracy of its closest competitor, Bluetooth LE. When optimized, it can demonstrate sub-meter accuracy as shown above. [3, p. 10], while having far greater data transmission rates, and makes use of existing Wi-Fi infrastructure. This justifies the use of IRS operation in such situations. Additionally, the spatial resolution of having numerous IRS elements points to better accuracy, closer to the Position Error Bound (PEB).

A key characteristic to be examined is power consumption which is already a key draw for service operators. The power and electrical transients of the IRS are difficult to analyze, due to the requirement of the separate microcontroller that controls the phase shifts. Therefore, it is useful to idealize and create the control circuit of the IRS.

1.3 Objectives and Scope

The initial goal of this project was to examine the power consumption behavior of an IRS performing a localization operation and analyses the optimal parameters (number of unit cells, array size, input power etc.) for the most efficient performance of the entire system. However, due to limitations of the control circuit, which will be detailed in later chapters, there was the final realization that it was not possible to fabricate the Intelligent Reflecting Surface or test it. Therefore, the project goal has diverted towards creating a proof-of-concept for the control circuit element.

The scope of the project is as follows:

- Establish a circuit model which controls the surface impedance and S-parameters of the IRS unit cell. The metallic patches form an RC-circuit equivalent, looking into the port. In turn, the effective resistance and capacitance of the RC circuit is tuned by the DAC circuit and supporting components.
- Conducted timing analysis of the custom Muller-C elements necessary for the control circuit

in SPICE software, and build them using discrete components.

- Proceeded with component selection and PCB layout of the control circuit using software, performed electrical rule checks
- Basic review of possible IRS simulation environment, in 3D-Cartesian coordinate system.

In addition, some literature review is conducted that paves the way for future research. The initial planned deliverables were to:

- Perform realization of the IRS through antenna models. To do this, I establish a unit cell configuration which comprises the individual element of the IRS. This unit cell then extends to a patch antenna array with $N_X^{IRS} \times N_Y^{IRS}$ elements, forming the simplified model for the entire IRS. The unit cell consists of 4 metallic patches that are each likened to a probe-fed patch antenna.
- Perform simulation of IRS with the transmitting BS and receiving UE, defined in 3D Cartesian coordinate system. Transmitting frequency is 5.8 GHz (802.11ax-compatible). The simulated system includes a blockage or wall between BS and UE, asserting a direct-LOS path that is present but weak.
- Consider the phase-shifting and localization algorithms used, computed by the IRS microcontroller, and determine if they are performance or bandwidth-limited. Uses the roofline model to analyze arithmetic intensity.
- Estimate overall system power consumption. This is achieved by examining input power of circuit models for the IRS/BS beamforming systems, added together with IRS microcontroller power consumption. Thereafter, draw a suitable conclusion and include comments on the optimal system for localization uses.

Optimal factors for the IRS system have been determined by previous literature, including but not limited to: - a fully-passive IRS, efficient phase-shifts, a certain number of unit cells. The performance of the localization system is heavily reliant on IRS signal characteristics, and

therefore it is intuitive to allocate some time to design/adapt IRS circuitry. There is the reliance on existing works to adopt the IRS conceptual design, and this helps to steer the project away from being antenna maximization focused.

1.4 Timeline

Many of the works mentioned in this timeline will be discussed in the Chapter 2: Literature Review and Chapter 3: Current Work.

2024

Feb — April

- Researched into various localization techniques using various technologies: Bluetooth, Zigbee, GPS
- Chose to focus on close-range Wi-Fi technologies in WAN systems

May

- Met with supervisor A/P Soong Boon Hee on 16 May and discovered IRS technologies after some review.
- Attempted MATLAB examples on IRS channel estimation, electromagnetic analysis

June — August

- Simulated sub-wavelength sized unit cell in Ansys HFSS using Floquet Port analysis

- Selecting localization methods from existing literature

Sep — Nov

- Thorough analysis of suitable circuit models for IRS
- Analysis of localization algorithm and complexity

Dec

- Finished mockup of printed circuit board (PCB) containing IRS, supported by digital-to-analog-converter and LDO integrated circuits.
- Attempt to perform co-simulation of the circuit and antenna model with Ansys Circuit and HFSS, realizing limited IRS functionality.

Chapter 2: Literature Review

This chapter will discuss typical communication networks and contrast it with IRS-based ones. Terminologies that pertain to IRS, channel estimation, and DOA-based localization techniques are explored briefly. A significant amount of time was spent on reviewing IRS-based terminology, which I viewed as a particularly challenging aspect.

2.1 General wireless networks

2.1.1 Overview

Wireless networks span the various frequencies in the electromagnetic spectrum and are regulated by authorities that control the frequency bands. These different categories can be categorized into Personal Area Networks, Local Area Networks (LAN), Wide Area Networks (WAN) and Non-terrestrial (i.e. satellites). IRS deployments can be found in terrestrial networks e.g. LAN and WAN. In general, to achieve widespread coverage, it is frequent practice to add more BSs, access points (APs) or UEs, but this comes at a massive cost in terms of power consumption and maintenance cost. [4, pp. 1]. Backhaul management also needs to be performed. Backhaul involves connecting heavy traffic cells to the core network, with the infrastructure itself being expensive and power-hungry.

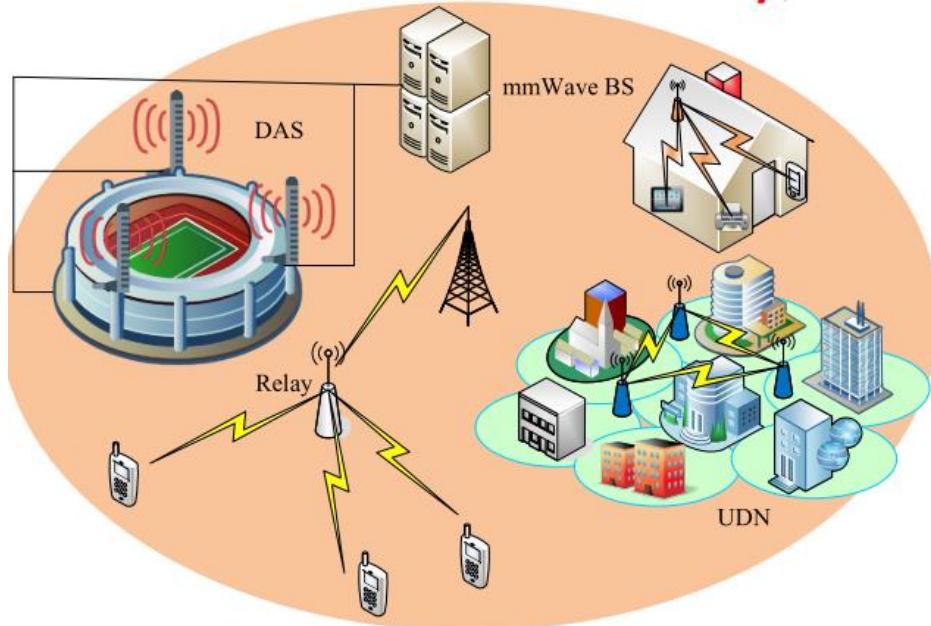


Fig. 3. Typical mmWave system. Adapted from [5, p. 15]

Generally, for both LAN and WAN, good wireless coverage and wireless capacity must be achieved. Wireless coverage can be defined as the total area of signal reach and received signal power. Wireless capacity often refers to the amount of bandwidth/data rate available in the network and may be defined by Shannon's Capacity theorem as mentioned earlier. The implementation of even bigger antennas (MIMOs) and moving to higher frequency bands is inevitably expensive, even though MIMOs are considered the best-in-class currently brought to market.

There is a need to explore supplementary systems to aid in strengthening the direct LOS path, to reduce the path loss at the typical mmWave frequencies (generally 30-300GHz). Research that proposes IRS deployments in tandem with mmWave BS is thus very common, and many optimization problems exist including placement, resource allocation, access methods e.g. Non-Orthogonal Multiple Access (NOMA) and so on. Central to many of these optimization problems are the effects of surrounding geometry, which can be also applied to the near field scenarios, moving into the discussion of LAN networks.

2.1.2 LAN topology and characteristics

A Local Area Network (LAN) is different from WANs in that they are typically smaller in size and do not require leased telecommunication circuits or underground data lines. The network size is limited to a single geographical entity, and a router usually comprises the AP, that can

optionally contain multiple network switches. The router facilitates packet delivery from end to end, which is Level 3 of the Open Systems Interconnect Model (OSI). Often, in indoor networks, multiple switches can be connected to a single router, where the switch creates instant networks for two devices to talk to each other (Level 2 of the OSI). [6]

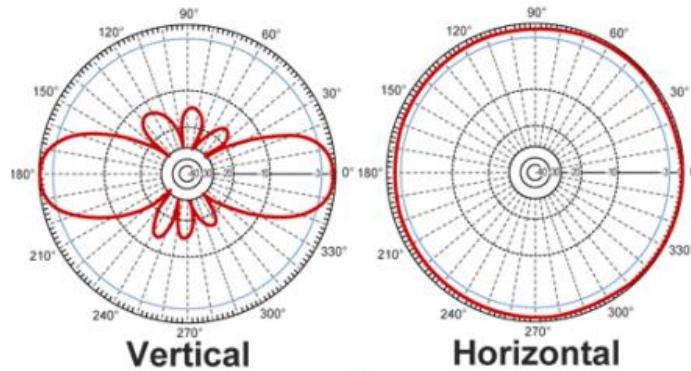


Fig. 4. Typical omnidirectional radiation pattern in vertical (elevation) and horizontal (azimuth).

Adapted from [7, pp. 2].

Routers are often a key component of a wireless LAN network and follow the IEE 802.11 standards. The operational frequencies are either 2.4 GHz under 802.11b/g or 5GHz, under variations of 802.11a. Most commercial routers feature built-in antennas that transmits beams that are omnidirectional in nature, with a mostly uniform 360° coverage in the horizontal (azimuth) plane. This is due to the need to provide ample coverage to the end user's UE which is usually situated some distance in the horizontal plane.

Practical antenna loss can be calculated from the Friis path loss equation [8, pp. 3].

$$P_{RX} = P_{TX} G_{RX} G_{TX} \frac{\lambda^2}{(4\pi R)^2 L} \quad (2)$$

P_{RX} = Total power received P_{TX} = Total power transmitted G_{RX} = receiving antenna gain G_{TX} = transmitting antenna gain R = LOS distance separating transmitting and receiving antennas λ = wavelength (in same units as R) L = system loss factor ≥ 1
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and the ratio of wave power can be quantified by $\frac{P_{RX} (\text{watts})}{P_{TX} (\text{watts})}$. In practice, mmWave signals are quantified by high loss due to their high frequency, since $\lambda = \frac{v}{f}$. The wave power of lower frequency waves e.g., at 5GHz also suffers, but due to different factors. This includes

frequent attenuation by the surrounding surfaces in a typical indoor environment, ‘shadowing’ by objects, and to compound the issue, WLAN antennas typically are not as high-powered as massive WAN MIMOS.

To combat this issue, the industry is constantly testing and deploying new standards, such as Wi-Fi 802.11ax. It is part of the “Wi-Fi 6” generation introduced in 2021. Under this specification, the total network throughput (of all users) increases to 300%, and latency is reduced by 75% [9]. It also enabled orthogonal frequency-division multiple access, where the subsets of subcarriers are assigned to each user, allowing for more effective bandwidth. This is similar to some existing research challenges on IRS. By discussing the framework through which wireless systems exist, I thus provide context for the challenges faced by IRS as a supplementary system.

2.2 Intelligent Reflecting Surfaces

2.2.1 Operating principles

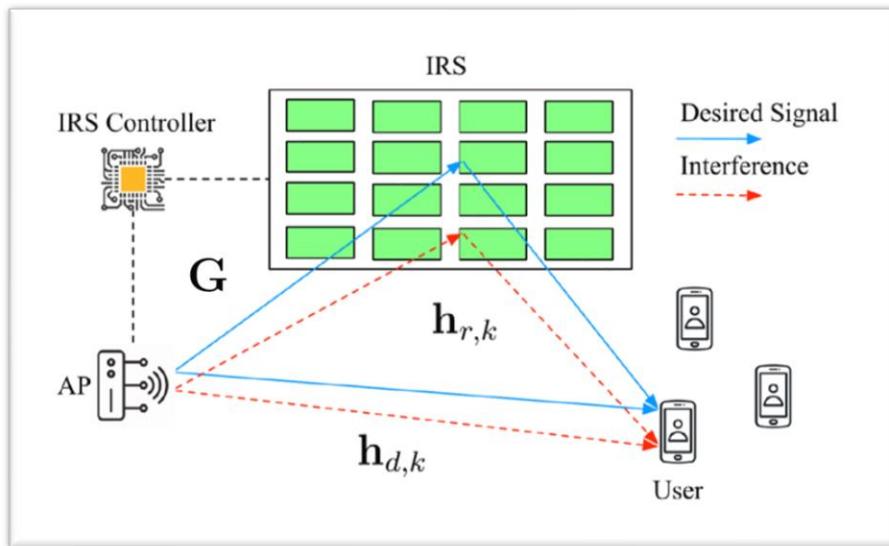


Fig. 5. Typical passive, singular IRS configuration

Intelligent Reflecting Surfaces (IRS), also known as Reconfigurable Intelligent Surfaces in some publications, are a new paradigm in wireless technology that are promising to supplement emerging needs for high-speed data transmission, compatible with IEEE 802.11 modern standards. IRSs functionally consist of a rectangular array of reflecting elements that introduce a phase shift/amplitude change into the incoming signal and use beamforming to increase the

Non-Line-of-Sight (nLOS) signal by several degrees of magnitude [4, pp. 5].

In literature, IRS are idealized to metasurfaces, where each element is actually a meta-atom. Metasurfaces are in turn, composed of “artificially periodic or quasi-periodic structures with sub-wavelength scales” [13]. The appeal of metasurfaces is that they are relatively two-dimensional, or thin, by merit of their fabrication that uses widely available materials like metal and FR4 substrate. Metasurfaces can be controlled to fulfill various functions such as polarization conversion, which is changing the direction of an incoming wave, reflection, absorption and refraction. Also, there is the choice between amplitude and phase shifting. I consider that phase shifts are easier to achieve with low-complexity input. Semi-passive IRSs have sensors that communicate with the controller but are more difficult to implement.

Therefore, a fully passive, idealized IRS without sensing elements will be considered in this project. All received signals contributing to the algorithms will be from the perspective of the BS, which communicates with the IRS’s microcontroller.

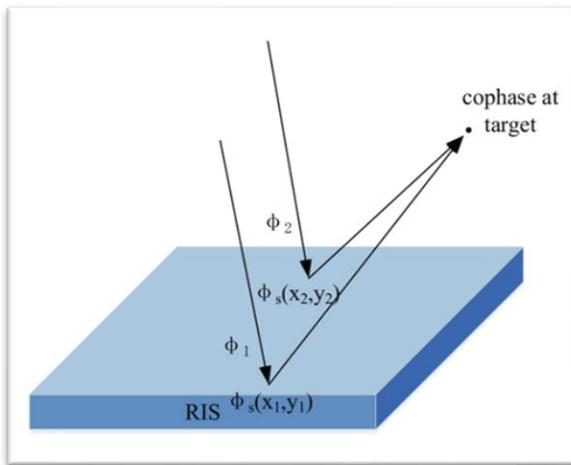


Fig. 6. IRS acts as focuser, not reflector.

Adapted from [14].

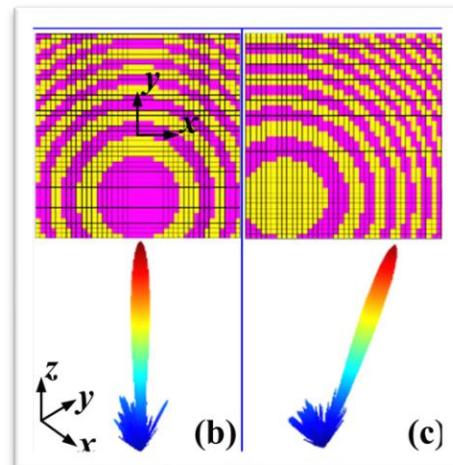


Fig. 7. Beam steering, adapted from [13].

For the purposes of normal data transmission, IRS will be configured primarily as a good reflector averaged over the whole surface. In this project, the incident EM radiation will be viewed as single ‘rays’ compatible with vector calculations, which have a direction, an amplitude, and a phase [14]. Doing this however discards the wave-optics perspective that takes

into account power flow on the surface of the IRS, but I choose to ignore the surface currents to simplify the scope. Also, this ray-optic view is compatible with the Huygens principle that states that a new wavefront is formed tangential to multiple spherical wavefronts [15]. Thus the incident rays will be in phase, as can be shown in Fig. 6, Φ_1 is in phase with Φ_2 .

The functionality of a reflective IRS can be based upon the individual elements constructively adding up at a target location, as can be visualized in Fig. 7. above. The maximization of this constructive signal is called channel estimation, typical for most wireless systems.

The phase shifts can be contained in a single column vector $\omega_\theta = [e^{-j\theta_1}, e^{-j\theta_2}, \dots, e^{-j\theta_N}]$ for N number of IRS elements. In an IRS array with x rows and y columns, $N = x \times y$. In turn, the individual element phase $\{\theta_n \in [0, 2\pi) \text{ for } n = 1, \dots, N\}$. The hardware necessary to induce phase shifts, usually include the microcontroller, and control circuitry which is usually fabricated on the IRS board with the unit cells.

2.2.2 Unit cell design

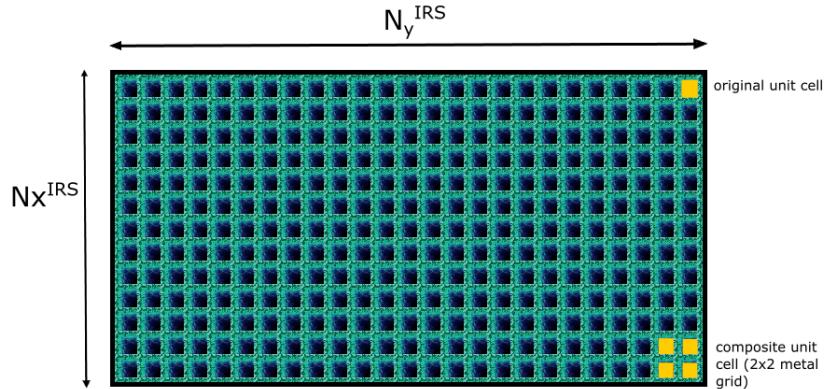


Fig. 8. Different unit cells

The optimal unit cell is most commonly configured as a square metal patch. Previously, experiments were made on pin-bed surfaces which are one-quarter of the wavelength thick, which led to even thinner surfaces that exhibited an extraordinary characteristic; the surface waves are zero due to high impedance. [30] Thus, compatible with the Huygens ray principle. This behaviour includes both magnetic and electrical fields, but the gist of the research was that the “leaky” TE waves resulting from these surfaces could be steered, which, when combined with reflectarrays, formed the basis for steerable surfaces using configuration of the

elements.

Most research emphasizes that varying the resonance frequency relies on some combination of changing the impedance, capacitance and inductance of the forward port. At a macro level, once certain requirements can be met, the entire surface is characterized more by its sheet characteristics, or being “periodic” as previously mentioned. One such parameter that has gathered large consensus is that the square unit cell length D is such that $D \ll \lambda$.

[DYNAMIC MODEL OF ARTIFICIAL REACTIVE IMPEDANCE SURFACES,

The methods of varying surface impedance has already been detailed, but this variation described in Fig. 9., [17] mentions the discrete components used in the design: varactor diodes. They are either turned ON or OFF by biasing the gate voltage, implying $2^2 = 4$ possible states for one unit cell. When the diodes are turned on, the surface impedance changes as seen by the incident wave. This enables the phase shift of $\theta_n \in [0, 2\pi)$ within the unit cell.

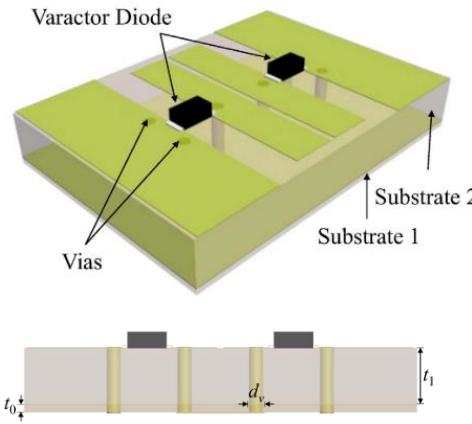


Fig. 9. Varactor-diode fed unit cell, adapted from [17]

As aforementioned, the unit cell follows the distinct rule of having its period, the length of the cell be much shorter than the wavelength (14.3mm as compared to 5.17cm for 5.8GHz). This approach immediately shows a few drawbacks; namely, that the resolution of phase shifts is relatively low, contrary to the numerous levels that control signals can be quantized into. Also, the 1-1 approach to controlling the varactor diodes indicates that a relatively large parallel configuration has to be envisioned for increasing elements N , which commonly comes in the form of field-programmable gate arrays (FPGAs).

Although FPGAs can be a viable solution due to their massive pin counts and configurability, they have a longer development cycle and higher power consumption than dedicated ICs or discrete elements, therefore it is worth exploring alternative control schemes. Particularly, it is worth considering a scheme that can be “hot-plugged”. For instance, given some newly fabricated IRS unit cells and the corresponding control circuit IC/PCB, the operator can immediately expand the IRS array size without reconfiguring the FPGA programming.

Looking away from the established approach, certain aspects of the fabrication process have to be accounted for, when designing such a device. In particular, the paper in [18] specifies that the vias (drilled holes through the substrate and metal) require certain clearance between the edge of the metal and the via itself. Also, the ICs that control the varactors, in practice, need to be located on the bottom edge of the PCB, unlike the design realized in Fig. 9. This is done to minimize electromagnetic interference (EMI/EMC) issues.

This improved unit cell shown in Fig. 10. accounts for these aspects by consisting of 4 copper patches that are probe-fed at their corners, and are sub-wavelength sized.

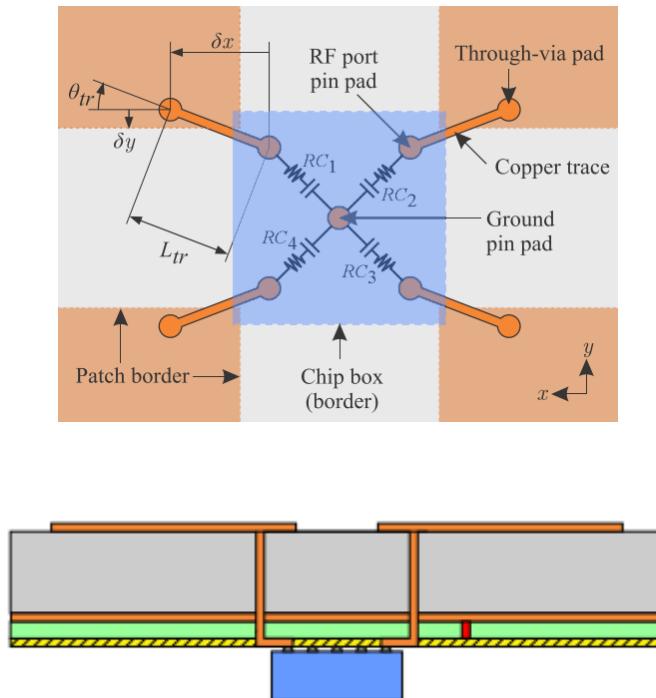


Fig. 10. Cross section of improved unit cell. Orange is the metallic patches and vias, grey is the dielectric substrate and green is the ground plane. Adapted from [18].

The research specifies that the individual control of patches is crucial for more “demanding functionalities because the change of each control element strongly affects the collective

response”, and that tuning the metasurface at the sheet level may not be sufficient, for functionality such as good-performing reflection [18]. There is an emphasis on extremely small unit cells, and it concludes that the unit cell length $D < 5\lambda$ for optimal performance.

Its control is facilitated by increased resolution of the phase shifts; with an 8 bit DAC attached to control the voltage levels of the varactors diodes, $2^8 = 256$ states of voltage shifts (and thus phase shifts) are realizable. This may appear to increase complexity of the phase-control. However, this is negated with more efficient phase-control algorithms, that are linear in complexity, such as that proposed in Section 2.4.1 [12]. The control scheme and IC functionality will be discussed in the following chapters.

In summary, I have chosen the 2x2 unit as an adequate unit cell and will be surveying its control scheme for the IRS.

2.2.3 Transmitter and receiver models

Since modelling the transmission characteristics of the IRS is of interest, it is beneficial to condense the BS and receiving UE models, in the BS-IRS-UE chain, down to their simplified versions.

Most base stations (BS) that emit wireless signals typically behave in an omnidirectional fashion. This implies that the transmitted power is equal in all direction is an ideal case. However, it should not be simplified to a point source, as typical wireless routers are composed of at least a few transmitting elements. It would be optimal to ensure that the Effective Isotropic Radiated Power (EIRP) by the BS is sufficiently large, thus the BS may be sufficiently modelled by a horn antenna.

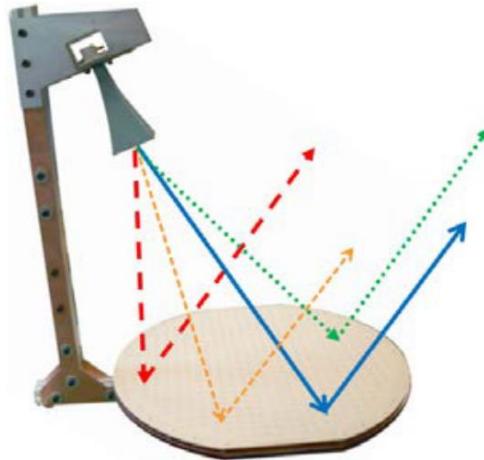


Fig. 11. Reflectarray with horn antenna. [19]

Horn antennas were ideal sources for several experiments in the 1960s and 70s, particularly reflectarrays, which were the predecessor to IRSs in the aspects of acting as waveguides. The presence of a horn antenna helps to match the impedance of the waveguide to the impedance of free space Z_0 , ensuring maximum power transmission through impedance matching, a key concept in transmission lines [10]. $Z_0 \approx 377 \Omega$, which is derived from the Maxwell's equations using the relation:

$$Z_0 = \frac{|\mathbf{E}|}{|\mathbf{H}|} = \mu_0 c = \frac{1}{\epsilon_0} \quad (3)$$

$|\mathbf{E}|$ = electric field strength
 $|\mathbf{H}|$ = magnetic field strength
 $\mu_0 \approx 12.566 \times 10^{-7}$ H/m
 $\epsilon_0 \approx 8.854 \times 10^{-12}$ F/m
 $c \approx 3 \times 10^8$ m/s

The gain of an ideal pyramidal horn antenna roughly equals its directivity, defined as:

$$Gain = \frac{4\pi}{\lambda} \epsilon_{ap} A_p \quad (4)$$

λ = wavelength
 ϵ_{ap} = aperture efficiency
 A_p = physical area of the aperture

Typically, for an optimal horn antenna, $\epsilon_{ap} = 0.5$, and the gain is typically 10-20 dBi [10]. The BS antenna can be treated as projecting a spherical wavefront directed toward the IRS. The nature of aperture gain means that an IRS with a larger area will collect and radiate more energy.

Indeed, it is in the designer's interest to increase the number of IRS elements as it results in more reradiated energy, higher gain. In one paper studying the phase shifting algorithm, signal-to-noise ratio (SNR) encountered a 15 dB boost with $N=100$ against $N=20$ elements [12]. This is also true for systems with two or more separate IRS working in tandem [5, pp. 38].

Therefore, modern UEs / routers can be modelled by a horn source, but the element by which the receiver can be modelled is much more complex. Typical receiving nodes in a WLAN wireless system include mobile phones, laptops, security cameras and IoT Devices, all of which have many different specifications. Even if the prominence of "older" devices is excluded, which do not adhere to the latest communication standards, the receiving antenna hardware exhibits too much variance between users. A comprehensive overview of mobile antenna design and philosophies is found in [20].

Smartphone users tend to benefit more by incremental improvements to quality of network and location information due to apps' typical requirements. There is also the reality that smartphones simply have one of the highest market penetration rates, greater than even computers. Initial research proves difficult to obtain reliable models for the average smartphone receiver; some smartphones may have dedicated broadband chips and transceivers, while others have antenna arrays embedded into the aluminum frame, limited by available space in the phone. Interestingly, it is discovered the entire cavity of a phone may behave in a resonant manner when excited by an EM wave, causing co-interference. It may also be harnessed in a beneficial way. [21]

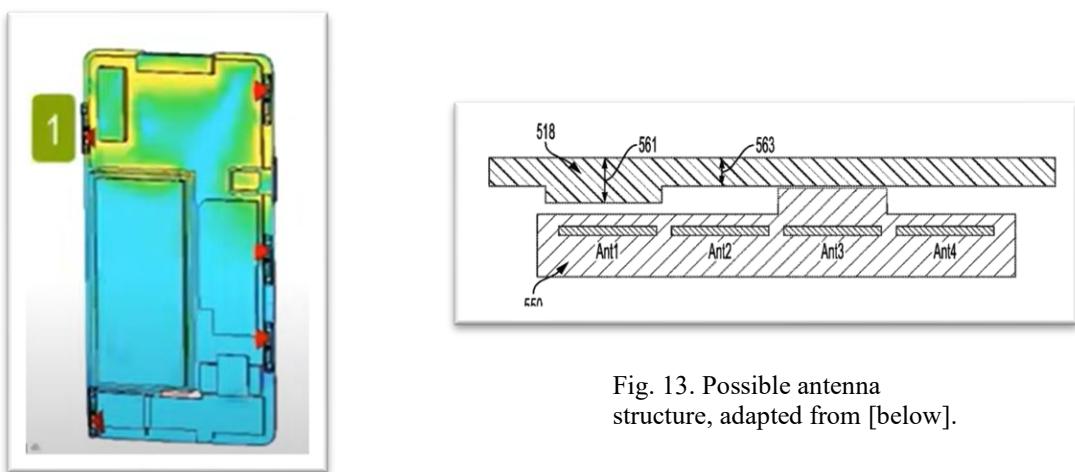


Fig. 13. Possible antenna structure, adapted from [below].

Fig. 12. Current distribution visualization in a phone shell, where yellow indicates

higher surface currents.

Adapted from [21].

A patent for mobile phone antennas is detailed in Fig. 10., which was filed in 2022 by Qualcomm Inc. [22] Terms were found within the patent which suggest possible commercial use. The design features two antenna strips with “L”-shaped elements perpendicular to each other. This serves as a simple yet excellent model since the 2 antenna strips are perpendicular to each other. Additionally, there is evidence of this antenna setup being used in popular phones. This ensures more reliable quality of signal, higher SNR, given the prior knowledge on elevation and azimuth plane differences, and the fact that phones are almost always in yaw (tilt) with respect to the BS.

Therefore, the BS can be modelled by a horn antenna, and the UE can be sufficiently modelled by two antenna strips perpendicular to each other. With one strip facing the vertical direction and one facing horizontal. This is especially useful when calculating wireless parameters using software.

2.2.4 Complex propagation environment

It can be inferred that in a typical WLAN environment without the IRS, performance will be impacted greatly as distance from BS increases. In Fig. 5 above, a signal propagating from the IRS to the k th user is characterized by two vectors. Firstly, a direct path vector $\mathbf{h}_{d,k}$ which is the LOS path. There is also the non-direct path vector $\mathbf{h}_{r,k}$, which first impinges on the IRS surface but is constructively combined at the k th user (UE).

Upon inspection of all signals received at the BS, the BS receives the composite of these signals from the environment: ① BS→target→BS, ② BS→IRS→target→IRS→BS, ③ BS→IRS→target→BS ④ BS→target→IRS→BS, and this is in the presence of a direct link, even if it is relatively weak. A research paper on localization concerned with these links found that this causes difficulty with Time-of-Arrival (TOA) based algorithms, because the IRS is close to the target. In this project scope, it would be within 20-50m. The paper then goes

on to propose and test a localization algorithm based on a monostatic radar system, which is considered in this project [3].

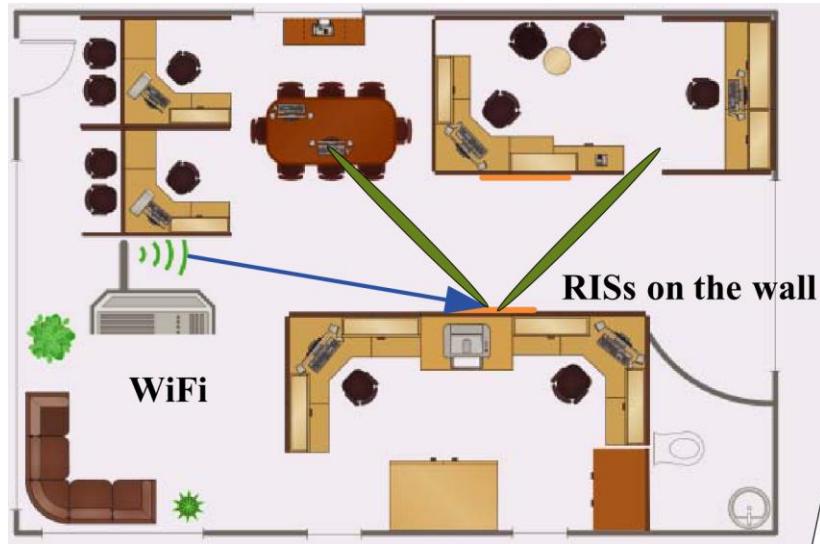


Fig. 14. Typical indoor environment with IRS, adapted from [14].

An indoor environment is also characterized by objects and furniture placed in variable positions, which makes the wireless characteristics ever-changing. Additionally, building materials such as solid walls attenuate wireless signals heavily. E.g. concrete walls of just 10.2 cm were shown to attenuate signals by 10-15 dB [16]. Combined with the complexity of signals received at the BS, research shows it is beneficial to run simulations in an environment with some non-idealities.

The challenge is increased when the target(s) for communication are moving, characteristic of the Doppler Effect, which distorts the phase and timing of digital communications, interrupting the typical burst-like nature of TDM and OFDMA mode signals. The effects on channel coherence time, which is the period where the impulse response is not varying, can be quantified when the target is moving. For instance, coherence time is lowered by a factor of 10 at a slow walking pace. [23] Due to the indoor environment, multipath components of a

wireless signal change rapidly and cause fast fading as well.

It can therefore be concluded that in order to sufficiently account for multipath components while keeping error to a minimum, there is some reasonable parameters for the environmental setup. The environment should have a steady target with some blockage in between the BS and UE. The blockage/wall could attenuate the magnitude of direct path $\mathbf{h}_{d,k}$ by a set specified amount.

2.3 IRS Control Scheme

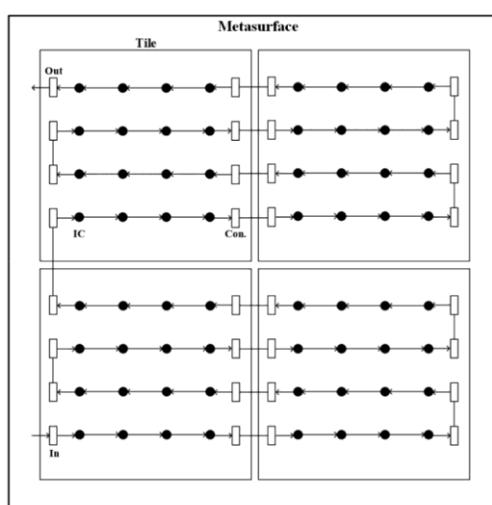


Fig. 15. Communication grid of the proposed ICs [19].

For a high-level overview, the IRS is displayed like a grid in Fig. 15. The ICs, 1 to each 4 metal

elements, selectively push the bits in a shift-register motion, the input port being at the bottom left. Typically, in synchronous circuits which are the most common, the “In” signal chain shifts right on an edge of the given clock signal. Here, there is an “Out” as well, which is fed back to the microcontroller, which may be useful for checking for bit errors or estimating delays.

For this instance, this grid shows an example with 64 logic elements, thus having 256 metal patches in all. Each element being $8\text{ bits} = 1\text{ byte}$ means that a single update being $\sim 64\text{ bytes}$ large will update all the patch coefficients to suitable values from a completely empty position. This chapter discusses the inner workings of the proposed IC from [19].

2.3.1 Asynchronous circuits

Digital circuits that are truly asynchronous are rare, because of the existence of both SPI and I2C formats for serial data transmission; most systems with dedicated chips will follow the system’s CLK signal. Asynchronous circuits, on the other hand rely purely on handshake signals between the ingoing and outgoing ports, which eliminates the need for a global clock signal to be sent with minimal skew. [24, pp., 1]

These async circuits greatly suit the IRS shift-register mechanism; it guarantees that clock issues are a non-issue, which may get compounded through numerous cascading stages. Universally, the sender and the receiver have at minimum a dual-channel, 2-phase protocol where “Request” and “Ack” for acknowledge signals are sent.

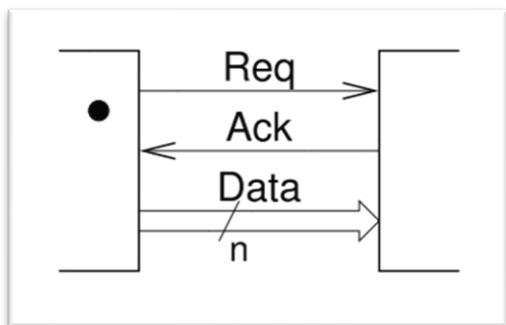


Fig. 16. Bundled-data channel [24]

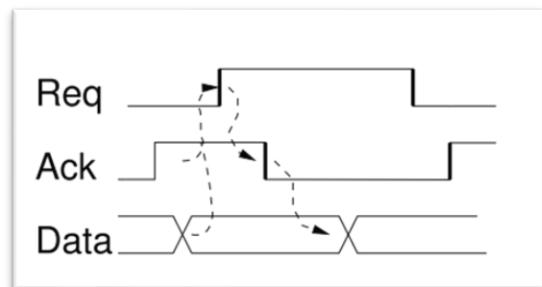


Fig. 17. Dual phase protocol [24]

Regardless of a L → H transition or vice versa, a signal transition will be triggered, and the data signal will change. However, to improve this signal's sensitivity to delays, dual-rail protocols are introduced, which involve having 2 dedicated data wires for each bit of information. Therefore, between subsequent stages, there will be a true and false signal, where '1,0' or '0,1' are accepted but not '1,1'. This forms the foundation of the IRS control circuit as shown in Fig. 18.,

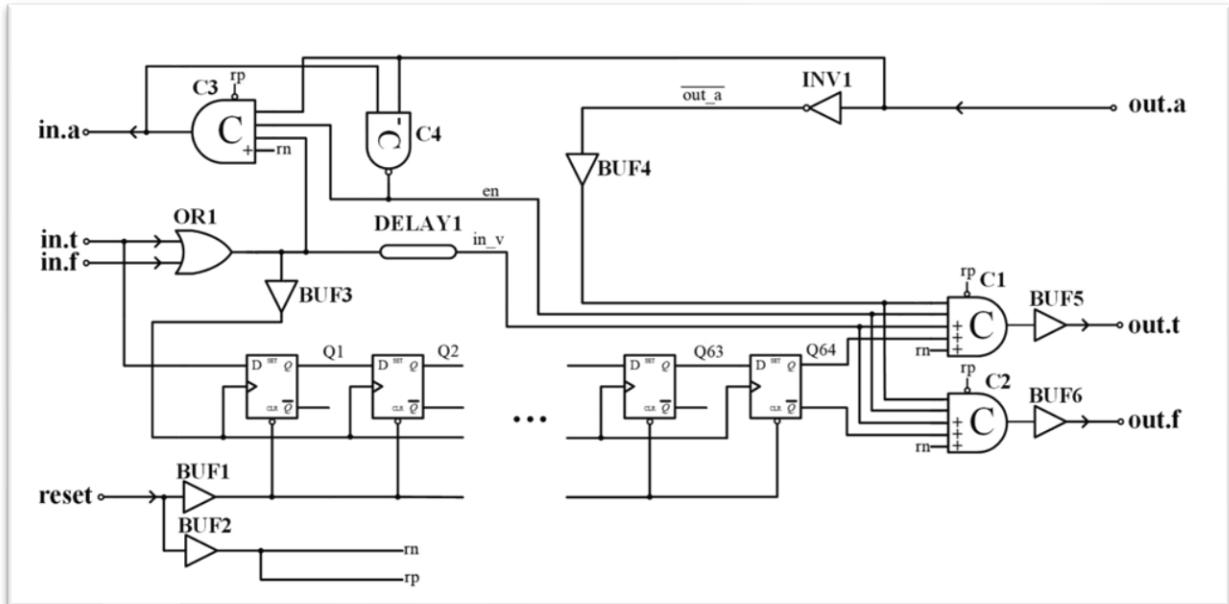


Fig. 18. IRS control circuit [25]

Seen above are several muller-C elements denoted by C1-C4, which only output a 1 when all their inputs agree, and retain their state otherwise. The truth table is given by:

TABLE I
Muller-C Truth Table

<i>a</i>	<i>b</i>	<i>y</i>
0	0	0
1	1	1
0	1	<i>y_{n-1}</i>
1	0	<i>y_{n-1}</i>

Symmetric C-elements behave as if all inputs have equal importance, for both L → H and vice versa transitions. On the other hand, asymmetric C-elements do not consider the values of

certain inputs when going from H → L transition. In addition to the Muller-C elements, there are also buffers, logic gates and other elements present, but these are mainly digital based instead of directly realizable components. The MOSFET equivalent of the 3 different Muller-C elements will be fully realized in Chapter 3.

The aforementioned dual-rail buffer system is used in this circuit, except that the acknowledge signals are only on a single wire. [25] Therefore, the output and input ports shown in Fig. 18. form the contacts on the 0.18 μm IC that was fabricated. For partly practical and educational purposes, it is of interest to form a circuit model with commercial components, instead of going through the IC design process. However, any PCB equivalent runs the risk of not being physically compatible with the size-sensitive IRS unit cells, because the patches of the cells need to be sub-wavelength sized.

2.3.2 D-flip flop and functionality

The inputs *in.t* and *in.f* as shown in Fig. 18. are guaranteed complimentary. For instance, the controller outputs “1,0”, “0,1” at the first stage. The activity in the shift register is as follows: *in.t* becomes high, then get clocked in into Q1 after buffer *BUF3* outputs high as well. The inputs reset to “0,0” in between, then “0,1” causes *in.f* to become high and clocks a “0” into Q1, pushing the “1” into the input of Q2.

The D-flip flops numbered from Q1…Q64 can be represented by 8 shift registers, each being 8-bit. Logically converting the D-flip flops is done to save on component cost and save space on the PCB layout. In Fig. 19. below, as per a manufacturer guide, a common strategy for the clock signal is to introduce the CLK signal in the reverse order of the shift registers, so that the correct value is loaded from the intermediary wire. Before this stage shown, “A, Wire, H” was represented by “L,L,L”. meaning that the “H” has been correctly updated into H of Device 1. Therefore, any design involving shift registers will have to introduce a clock signal with buffers propagating backwards.

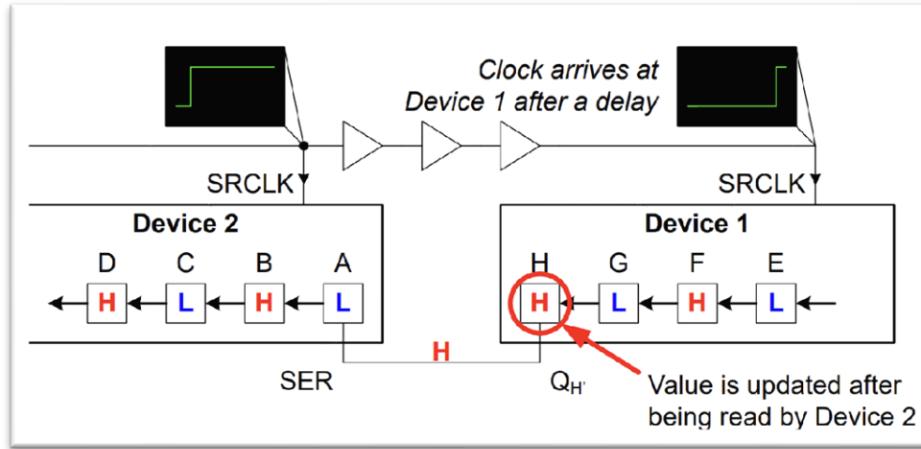


Fig. 19. Shift registers, adapted from [26, pp. 11].

A serial-in, serial-out shift register is required to ensure that the bits flow in a cascaded manner. Thereafter, the 8-bit outputs at each stage are introduced into the digital-to-analog converters (DACs). In particular, the output stages need to be exposed so that the DACs can tap into them in parallel. Therefore, octal D-type flip flops can be used, such as the Texas Instruments SNx4HC273. As shown in Fig. 20., the output of the first stage “1Q” is an open pin that is ideally connected to the second stage “2D”.

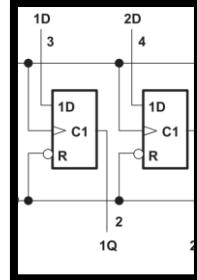


Fig. 20. D-type flip flops, [27]

2.3.3 Digital-to-analog converters

The DACs implemented in the literature is a 8-stage resistor string, which should be implemented using diffused or epi-pinch transistor in the IC to accommodate the 2.2mm footprint. A parallel-in, serial-out DAC is desired. The 8-bit outputs from the shift-registers are fed into the DAC. With a V_{ref} of 1.8V, the analog output voltage is given by equation (5):

$$V_0 = \text{analog output voltage}$$

$$V_{ref} = \text{fixed input voltage}$$

$$D = \text{digital input in decimal}$$

$$V_0 = V_{ref} \left(\frac{D}{256} \right) \quad (5)$$

Thus, for an input of $(1000\ 1011)_2$, the voltage $V_0 = 1.8 \times 139/256 = 0.977V$. For the configuration of the complex impedance IC in [19], it was previously mentioned that the copper elements are probe-fed at their corners. Crucially, the connection to each of the four corners of the pad as seen in Fig. 10, involve an equivalent RC circuit in parallel; the effective resistance and capacitance are tuned through varistors and varactors.

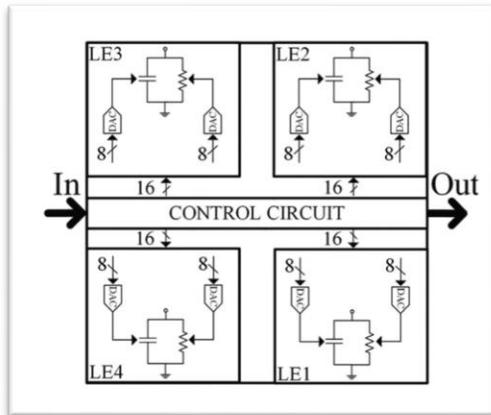


Fig. 21. Control circuit shown with 8 DACs at the corners, [19]

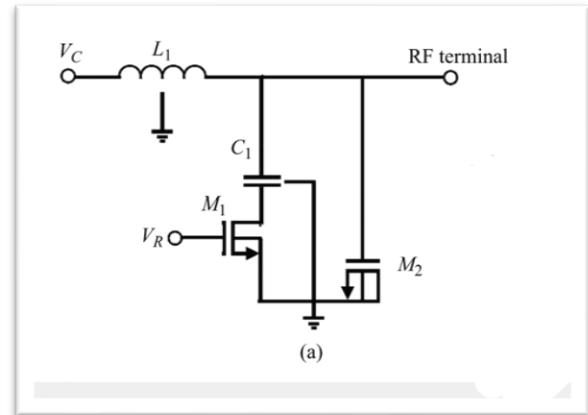


Fig. 22. V_R and V_C biasing [19]

Primarily, V_R and V_C are the net names of the two biasing voltages that affect the input resistance and capacitance as seen from the RF port. The effective range of both V_R and V_C range from 0-1.8V, and for a 180nm process node, it provides the best balance between capacitance and resistance tuning.

2.4 Algorithms

Various research has been conducted for the main use cases considered in the IRS: Channel estimation, which can only occur as a result of efficient phase control, and localization. Channel estimation works to maximise the received SNR at the receiving UE, or achieve best-case SNR for multiple users.

When executing the code on the microprocessor, several factors need to be considered. Intuitively, the complexity in Big "O" notation is an initial factor. Secondly, arithmetic intensity and roofline models can be used to determine whether these algorithms are more

computationally or memory intensive [28]. This in turn facilitates the choosing of a cheap but “good enough” microprocessor. Once the microcontroller is identified, a power consumption model can be formed. However, there are various limitations to most traditional simulators for microcontrollers that exist, such as *Wokwi*. In fact, these simulators may not be suited for projects of larger complexity than a few single line drawings.

In order to be aligned with the original aim of creating a power consumption model, an important fact to be reconciled is that the microcontroller has been physically tested in order for any accurate analysis. The microcontroller and supporting systems have to have its power draw physically measured, or even its serial data ports and voltage sources linked to the connected IRS. This is especially true due to unknown factors such as heavy CPU usage, and the various background processes in the microcontroller which cannot be feasibly controlled.

Therefore, the proposed algorithms mentioned here may only be tested when the entire IRS construction, inclusive of the unit cells are at least demonstrably working, but this is incompatible with the current project stage. The algorithms mentioned are therefore only explored at a surface level, but they are already being widely used in literature elsewhere and are very promising.

2.4.1 Phase control algorithm

A potential phase control algorithm that possesses linear complexity is described in [12]. Being research that was recently published in 2023, it supersedes the previous established knowledge that phase shift algorithms have to be exponential complexity (from a summary paper in 2021 [4, pp. 3330]).

2.4.2 Localization of user

Localization can be performed, given the limitations of the IRS system I am working towards [29]. This algorithm uses known values that can be obtained through simulation in software solvers such as the bandwidth of received signal, Noise Figure of the receiving end etc. Interestingly, the IRS is treated as a lens in this scenario which generates a stream of observations.

This is suitable and much less complex than the multi-stage solution proposed in [3] where the IRS has to be turned off, then on again.

Chapter 3: Current Work

Comprehensive review of IRS terminologies & applications has been conducted. Circuit models have been established for the control circuit. The project explores many areas of circuit design and analysis. Realizing the digital, asynchronous functionality of the control circuit is the main challenge of this project. Of particular interest are the following:-

- Muller-C elements, asymmetric and primarily consisting of N-channel and P-channel MOSFETs
- D-flip flops
- Associated DACs
- Output varactor diodes

In particular, timing analysis and some design has been conducted for the Muller-C elements, because it involves custom logic, with three different asymmetric elements.

The software used so far include LTSpice for SPICE simulation, Altium Designer which helps with comprehensive component selection, schematic design and PCB design. Lastly, Ansys HFSS which is useful for simulating high-frequency electromagnetic wave interactions.

The full schematics and layout on the PCB have been realized, being compiled in a hierarchical manner with a single parent schematic and 6 child schematics. These can be viewed in the Appendix sections.

3.1 Varactor parameters

Initially, I had made an attempt to determine the RC equivalent circuit as seen at the RF port. Therefore, the equivalent of Fig. 22. was setup as a *SPICE* simulation initially. *SPICE* (Simulation Program with Integrated Circuit Emphasis) software are usually used to check circuit behaviour, and for analysis purposes. In order to calculate the parallel impedance of the RC circuit, it was useful to obtain $\max(R_p) = 440\Omega$ and $\max(C_p) = 3.8pF$, from the 180nm process graph in [18, pp. 1445]. Then, the total effective impedance for parallel RC at 5.8GHz impinging on the metal is given by:

$$\frac{1}{Z_{total}} = \frac{1}{440} + \frac{1}{(2\pi \times 5.8 \times 10^9 \times 3.8 \times 10^{-12})}$$

$$Z_{total} = 0.138\Omega$$

The inductor L₁ in Fig. 22 needs to act as a RF choke, so it is specified such that it operates at its self-resonant frequency (SRF), and thus this becomes a small exercise to obtain value of L₁. From [32], the equation of SRF is as follows:

$$SRF = \frac{1}{2\pi\sqrt{LC}} \quad (6)$$

However, the intrinsic capacitance of the inductor is unknown. Instead, a common rule of thumb can be used where the inductive reactance of inductor, needs to be about 100 times the impedance as seen from the RF port. Inductive reactance is specified by $X_{inductor}$ and therefore min(L₁) can be found.

$$X_{inductor} = 100 \times Z_{total} = 13.8\Omega$$

$$L_{min} = \frac{X_{inductor}}{2\pi \times 5.8 \times 10^9}$$

$$L_{min} = 0.37nH$$

Now, to consider the DC blocking capacitor C₁. Generally, the capacitive reactance X_c describes the varying current flowing through itself, which is affected by the frequency.

$$X_c = \frac{1}{2\pi \times 5.8 \times 10^9 \times C}$$

The reactance needs to be relatively low compared to the 50 Ω line impedance, say 2 Ω. Thus min(C₁) = 27pF, which is reasonable.

Fig. 23 below shows the LTspice schematic, set up for simulation with C₁ and L₁ values. LTspice offers transient analysis, AC/DC sweep amongst other options, and is a useful tool for modelling discrete components. Also useful is the fact that voltage sources can be modelled as a pulse, piecewise, or A.C. aside from being standard DC sources.

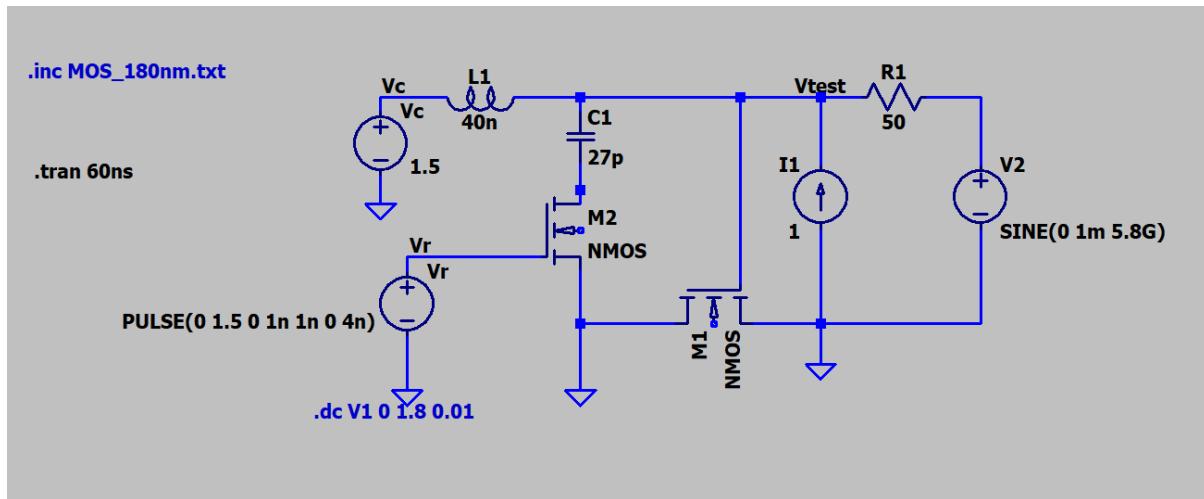


Fig. 23. Varactor model from [18].

```

1. *
2. * Predictive Technology Model Beta Version
3. * 180nm NMOS SPICE Parametersv (normal one)
4. *
5.
6. .model NMOS NMOS
7. +Level = 49
8.
9. +Lint = 4.e-08 Tox = 4.e-09
10. +Vth0 = 0.3999 Rdsw = 250
11.
12. +lmin=1.8e-7 lmax=1.8e-7 wmin=1.8e-7 wmax=1.0e-4
13. +Xj= 6.000000E-08 Nch= 5.950000E+17
14. +-----+ 1.000000E+00 1.000000E+00

```

Fig. 24. Predictive model text file

The original goal of placing this system in LTSpice was to measure the impedance and capacitance as seen from the RF port; voltage source V_2 was modelled as a low-amplitude RF source, similar to a wireless EM wave. Predictive model file was included from [33], which helped to accurately simulated 180nm gate length MOSFETs, labelled as M_1/M_2 . The model file is stored in Appendix.

I used the traditional method to measure resistance across the port by placing a 1A current source in series, but the transient analysis did not show much variance in the waveform in any of the input ports. This might be due to an oversight in measurement methods, but it serves as a good starting point for LTspice simulation nonetheless and shows that the varactor

circuit can be somewhat accurately modelled.

3.2 Muller-C elements

3.2.1 Muller-C(a)

The first Muller-C element shown in the paper can be described by the logic function:

$$Y_n = A \cdot B \cdot (C + D + Y_{n-1}) \quad (6)$$

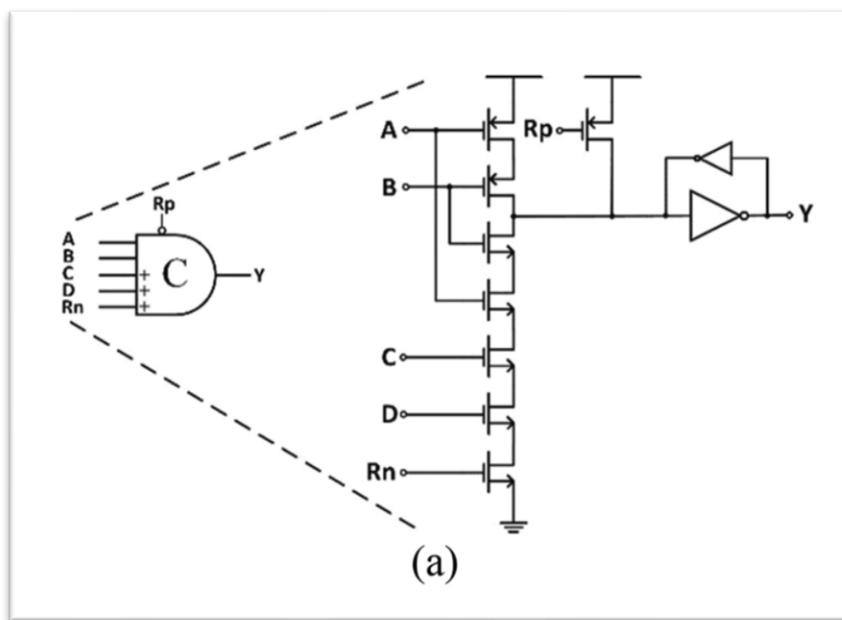


Fig. 25. Muller C(a) element, adapted from [19]

The truth table of the base Muller-C element was earlier explored in Section 2.3.1, however beginning with the schematic, there are some differences. The 3 Muller-C elements are all asymmetric, meaning that the output is only *always* asserted on some of its inputs; namely those without the ‘+’ or ‘-‘ signs, which are seen as “weak” inputs. [34]

This Muller-C(a) element changes to ‘1’ for $0 \rightarrow 1$ transition for all elements, but only changes to ‘0’ if $A \cdot B = 0$. Therefore some pseudo-code can be used to gauge the expected output, aside from the logic function:

```

1. If 4. Y = A.B.C.D = 1
5. else
6. Y = A.B OR reset = 0
7. else
8. Y_n+1= Yn

```

This element is implemented using FDC638P p-channel transistors, and FDC637AN n-channel transistors, both of which were chosen for their low $R_{on} \approx 0.03 \Omega$ and $V_{to} = 1.1V$; being from the same manufacturer. LTspice shows very minimal time-averaged power dissipation – on the order of picowatts for the whole Muller-C system.

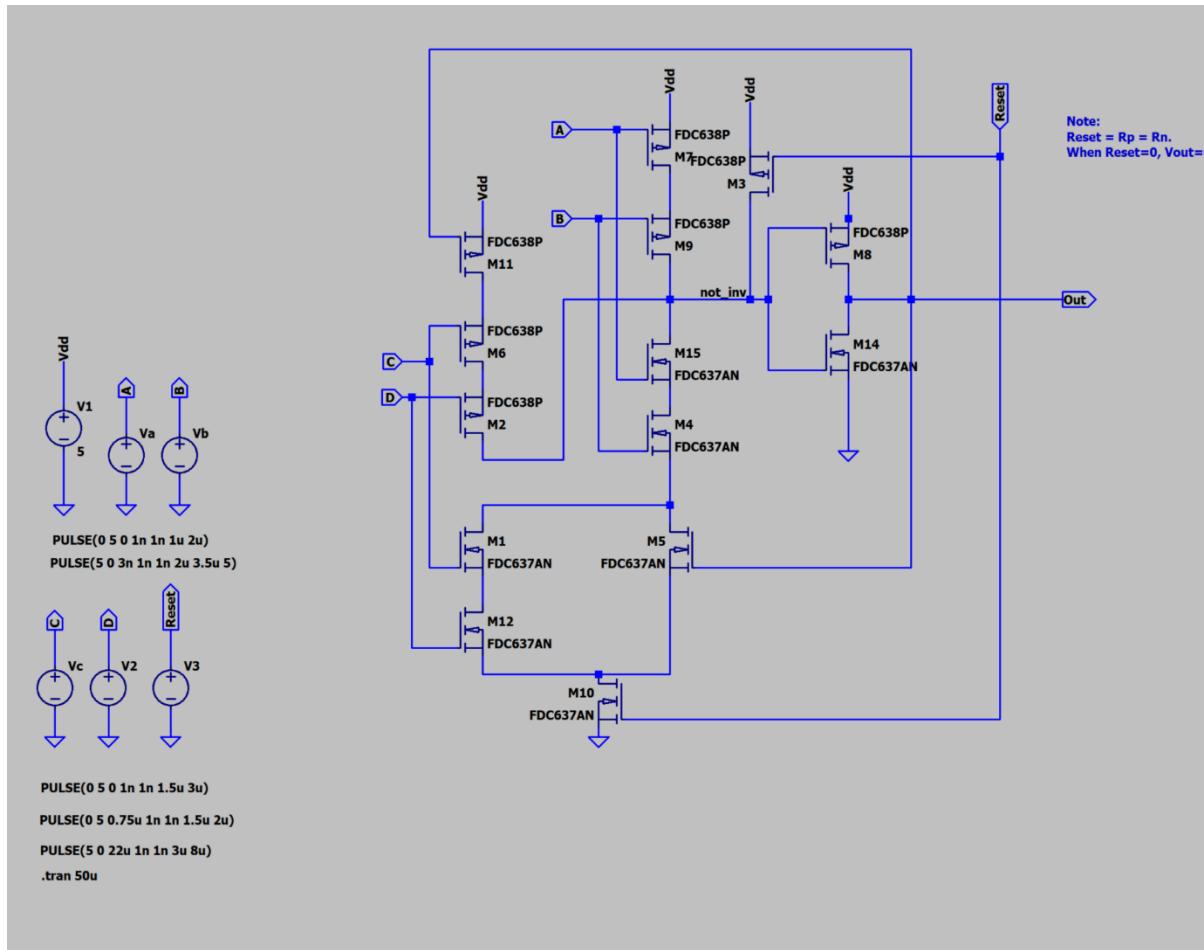


Fig. 26. Muller C(a) element in LTspice

Layout of several gates were changed slightly, and some complimentary pairs were added, e.g. for C and D even thought the original design as depicted in Fig. 25. did not do so. Additionally, the cross-coupled inverter as depicted earlier depended on a weaker upper inverter, which caused problems when it was fed directly back in series to the first inverter. Therefore, the inverting feedback loop actually travels to the first stage instead.

To verify the logic function, I set several pulse-behaviour sources with differing delays and the same amplitude of 5V, to guarantee the switching behaviour of the MOSFETs. It is confirmed that the signal V_{out} behaves as expected, and with minimal voltage drop from

presumed $V_{\text{logic}} = 5V$. In Fig. 27 below, the green arrows correspond to a rising V_{out} when $A.B.C.D = 1$, and the red arrow points to an instance where Reset pin pulls output low.

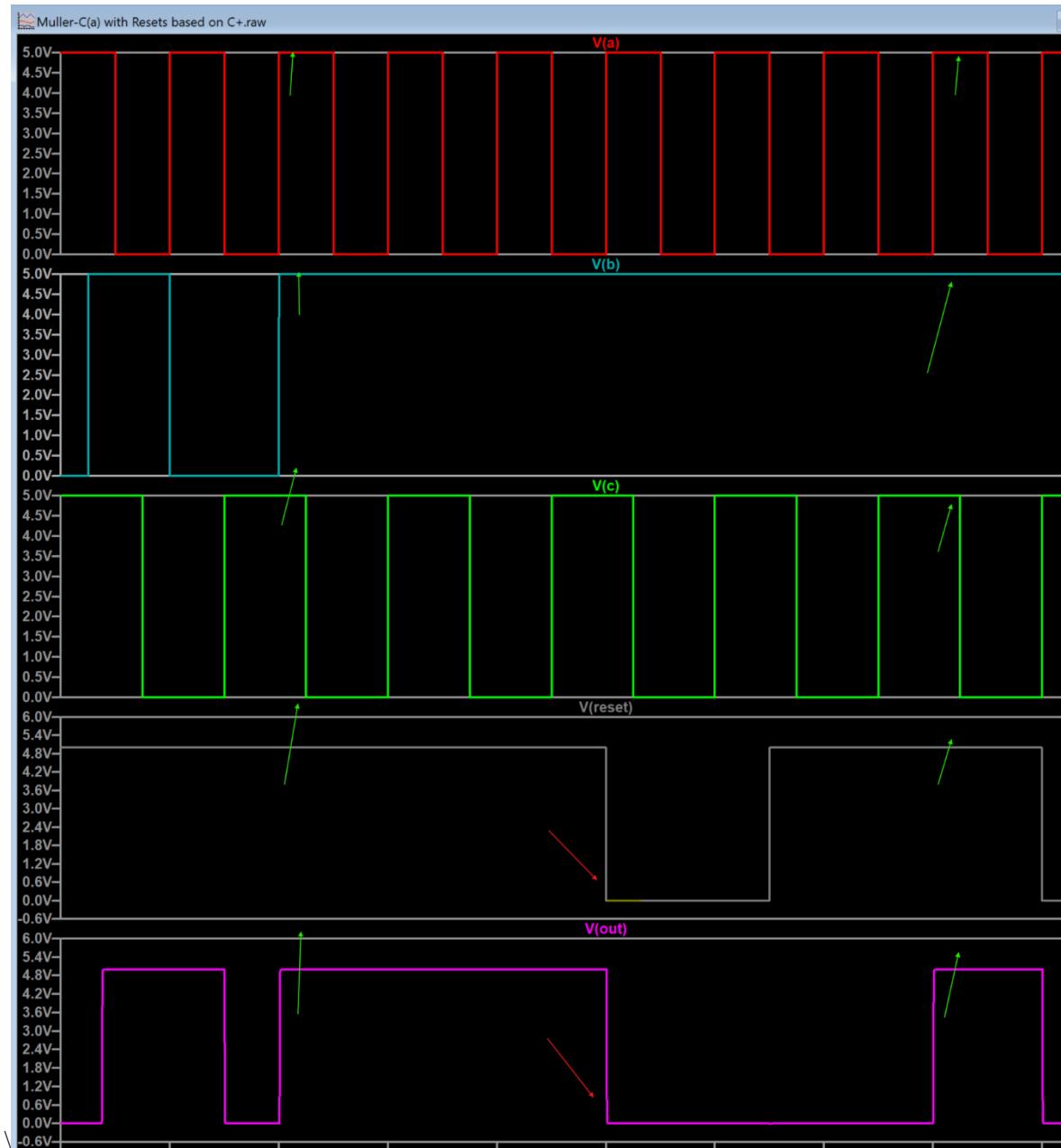


Fig. 27. Transient analysis of Muller-C(a).

3.2.2 Muller-C(b)

Similarly, for Muller C(b) element, which is the simplest asymmetric element with a negative pin pointing to A, indicating that A is ignored for $1 \rightarrow 0$ transition:

$$Y_n = B + A \cdot Y_{n-1} \quad (7)$$

```

Y = B = 1
else
Y= A.B = 0` 
else
Y_n+1 = Y_n

```

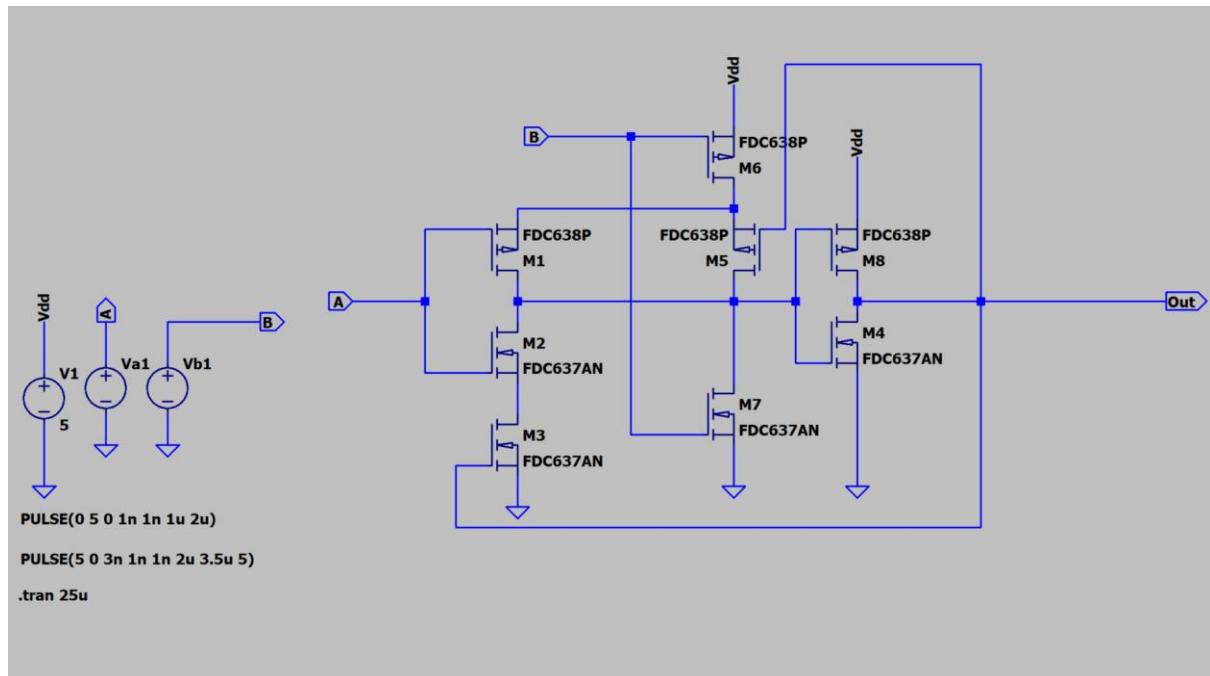


Fig. 28. Muller C(b) element in LTspice

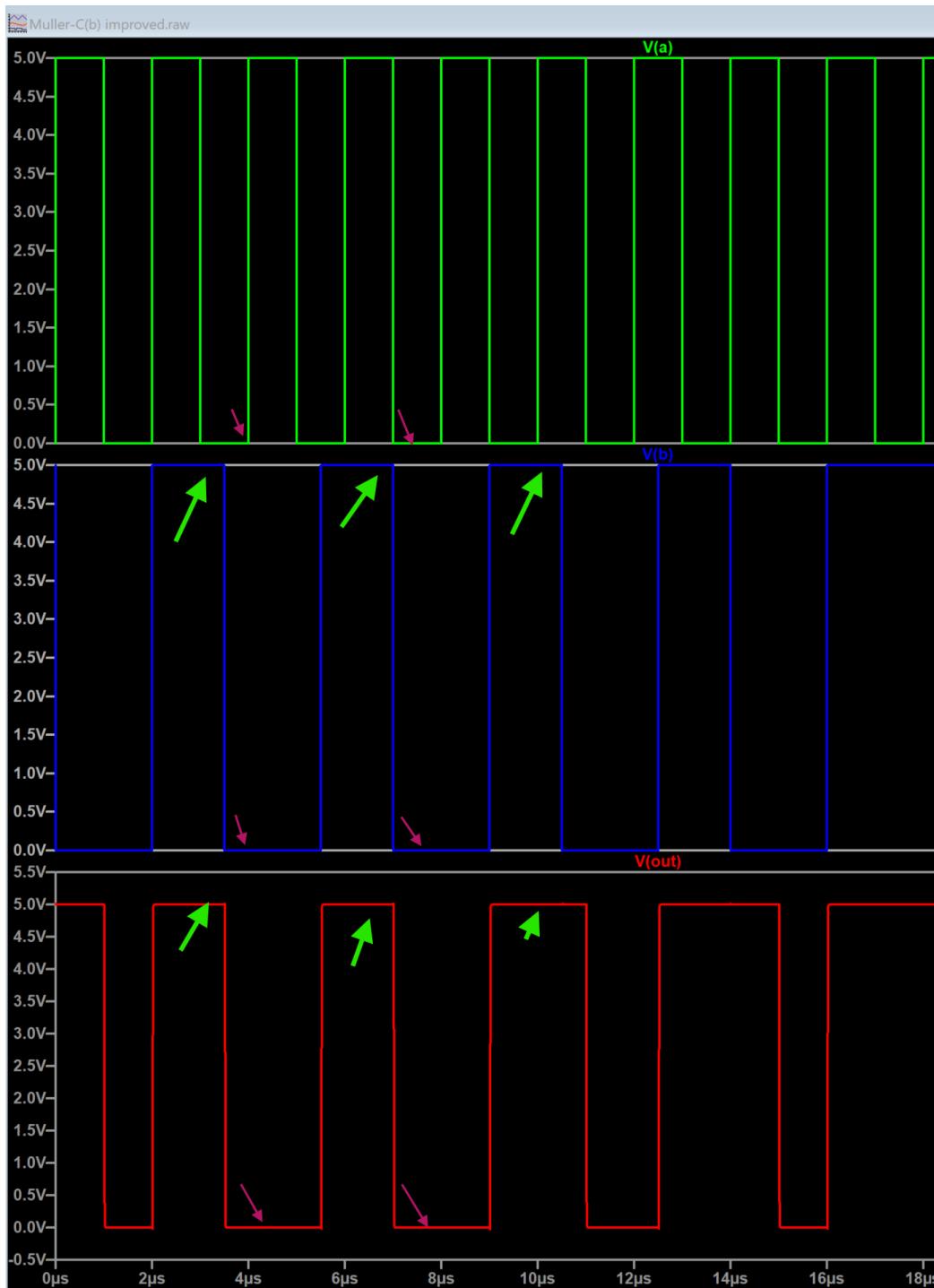


Fig. 28. Transient analysis of Muller C(b).

3.2.3 Muller-C(c)

Lastly, Muller C(c) element is symmetric for $1 \rightarrow 0$ transition and $0 \rightarrow 1$ inputs, except when $\text{reset} = 0$ is active.

$$Y_n = A \cdot B \cdot C + Y_{n-1} \quad (7)$$

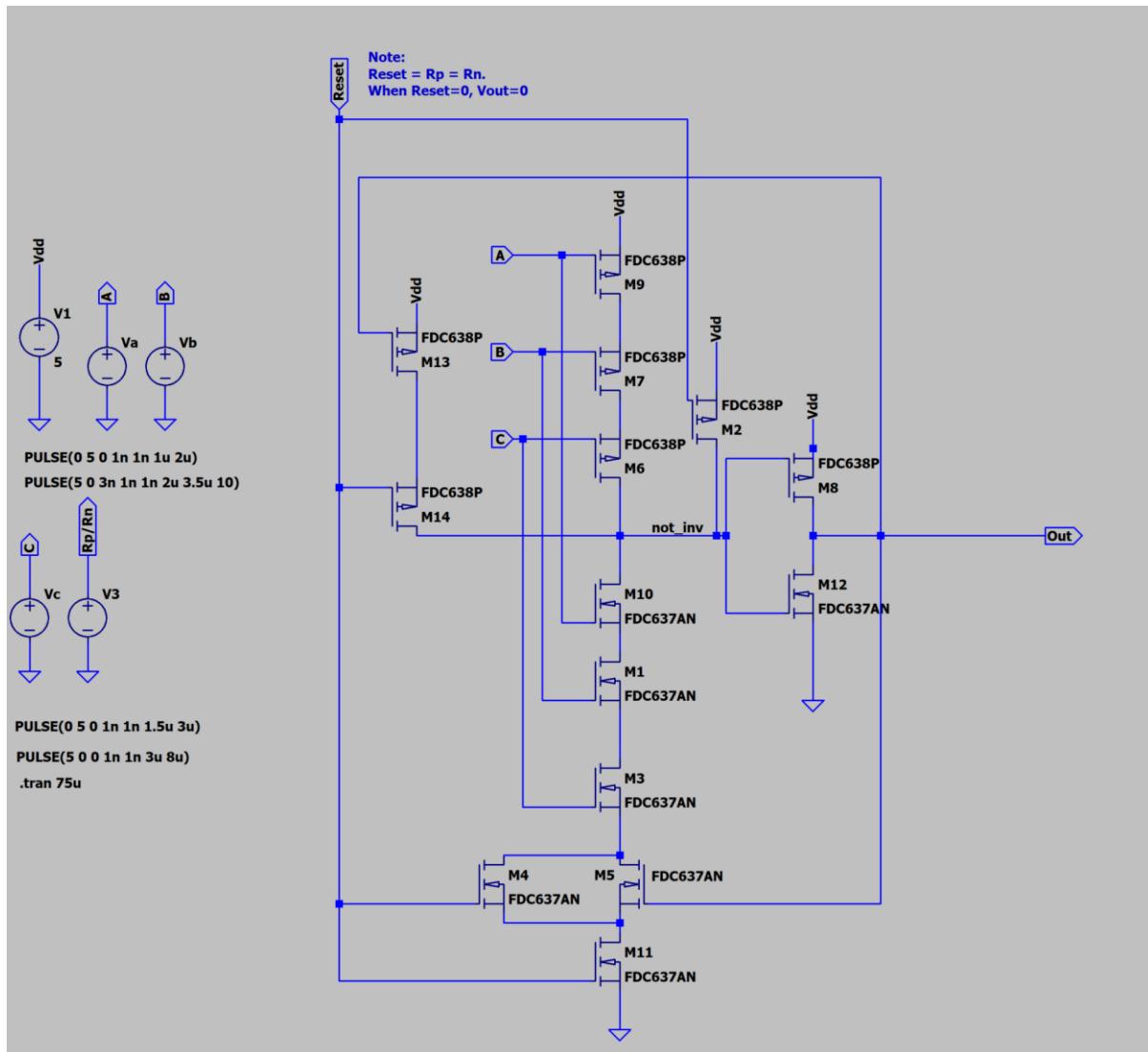


Fig. 29. Muller C(c) element in LTspice

All three muller elements are thus demonstrably accurate with their logic functions, which assures that the digital gates may be realizable using discrete components. The next logical step would be to construct the rest of the control circuit. The logical design is brought over to the electrical CAD software, Altium Designer, where a similar schematic is constructed, this time under more strict rules such as grid, electrical rule checks and so on. Placing the logic gates in the CAD software means that there is the benefit of linking 3D models, creating revisions and managing the workflow for designing circuits.

Also, the elements can be quickly fabricated on a low cost PCB for prototyping purposes, and electronic parts/PCB fabrication are readily available through suppliers.

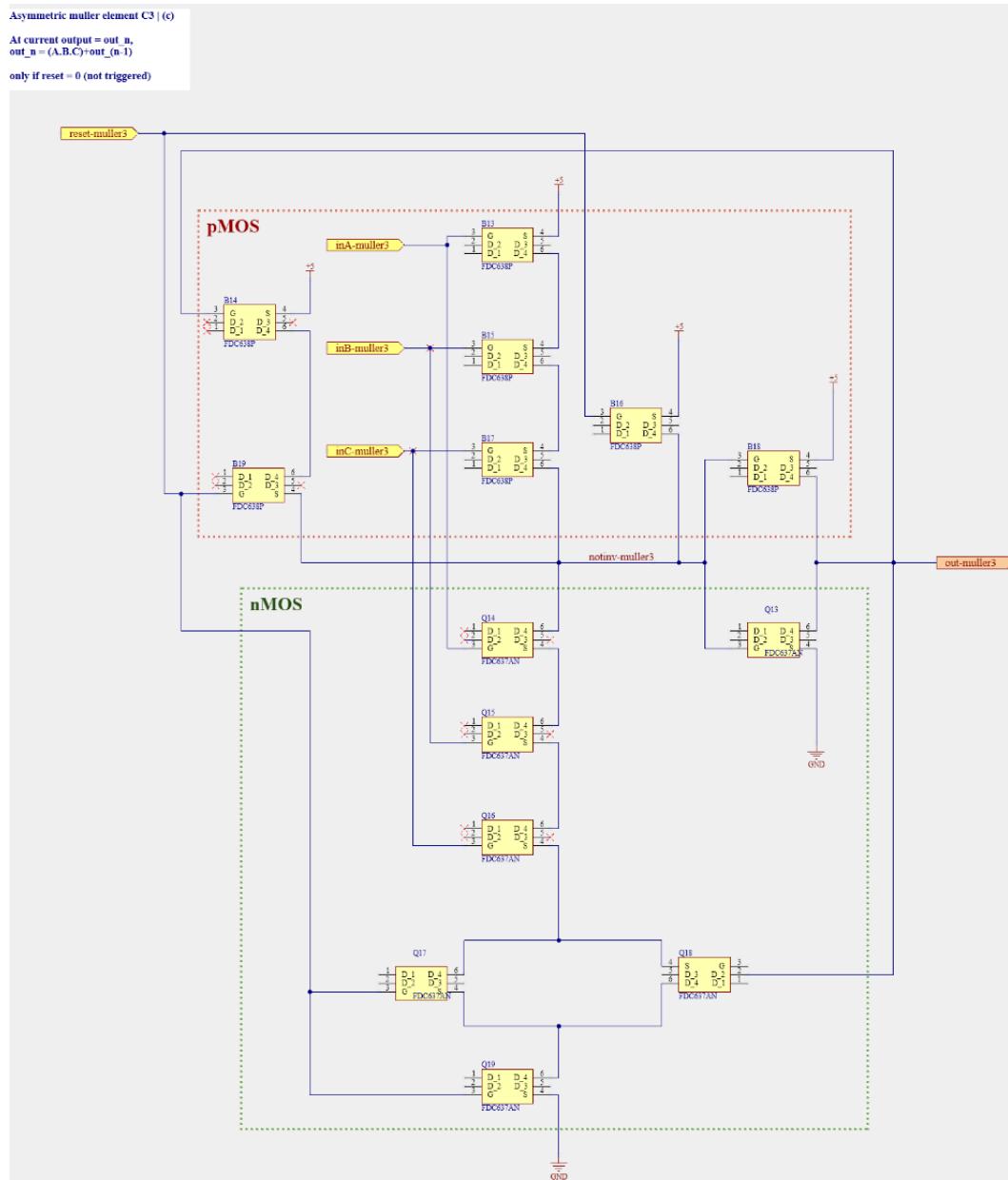


Fig. 30. Muller-C(c) element in the schematic.

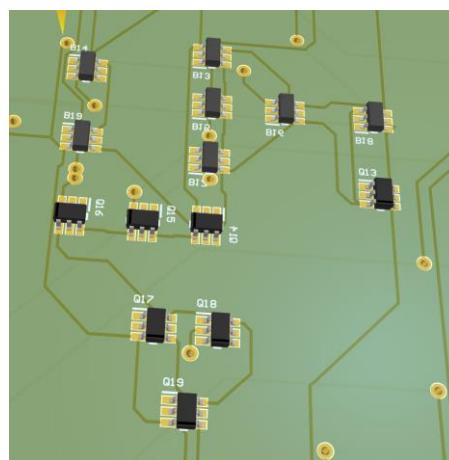


Fig. 31. MOSFETS consisting of muller-C(c) on the PCB

3.3 Control circuit implementation

The entire control circuit is implemented from a top-down level, where there is a main schematic ensuring electrical connectivity and logic flow. The primitive objects in the CAD software consist of power ports, components, wires, buses and so on, each of which serve different purposes, but mainly ensure coherency between different parts of the schematics.

As seen below in Fig. 32, the direction of the wire flow is reminiscent of the original logic diagram of the IC, but while that consisted of pure logic gates with little active components, modern day electronic design demands the use of active components. The green sheets displayed here are the child sheets under this hierarchy. Much time was spent on familiarizing myself with the CAD software and the workflow.

Several different discrete components are sourced, through an in-house manufacturer part engine, to check for availability, and then placed on the schematic. In addition, the sheet symbols in yellow here should have a corresponding 3D model / footprint.

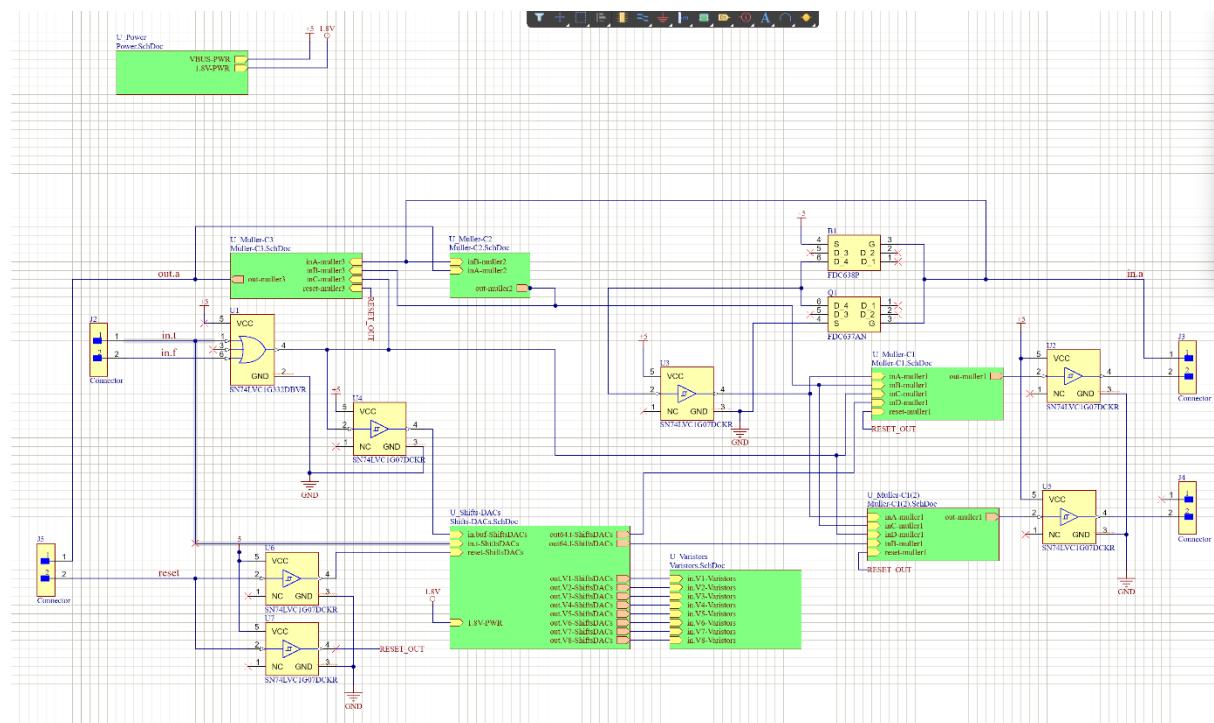


Fig. 32. Main parent schematic

4 of the child sheets are Muller elements which have already been explored. The inputs are actually connected to a physical connector that is factory soldered onto the board using SMD technology. The most detailed child sheet is the DAC control circuit. One stage of it is shown in Fig. 33:

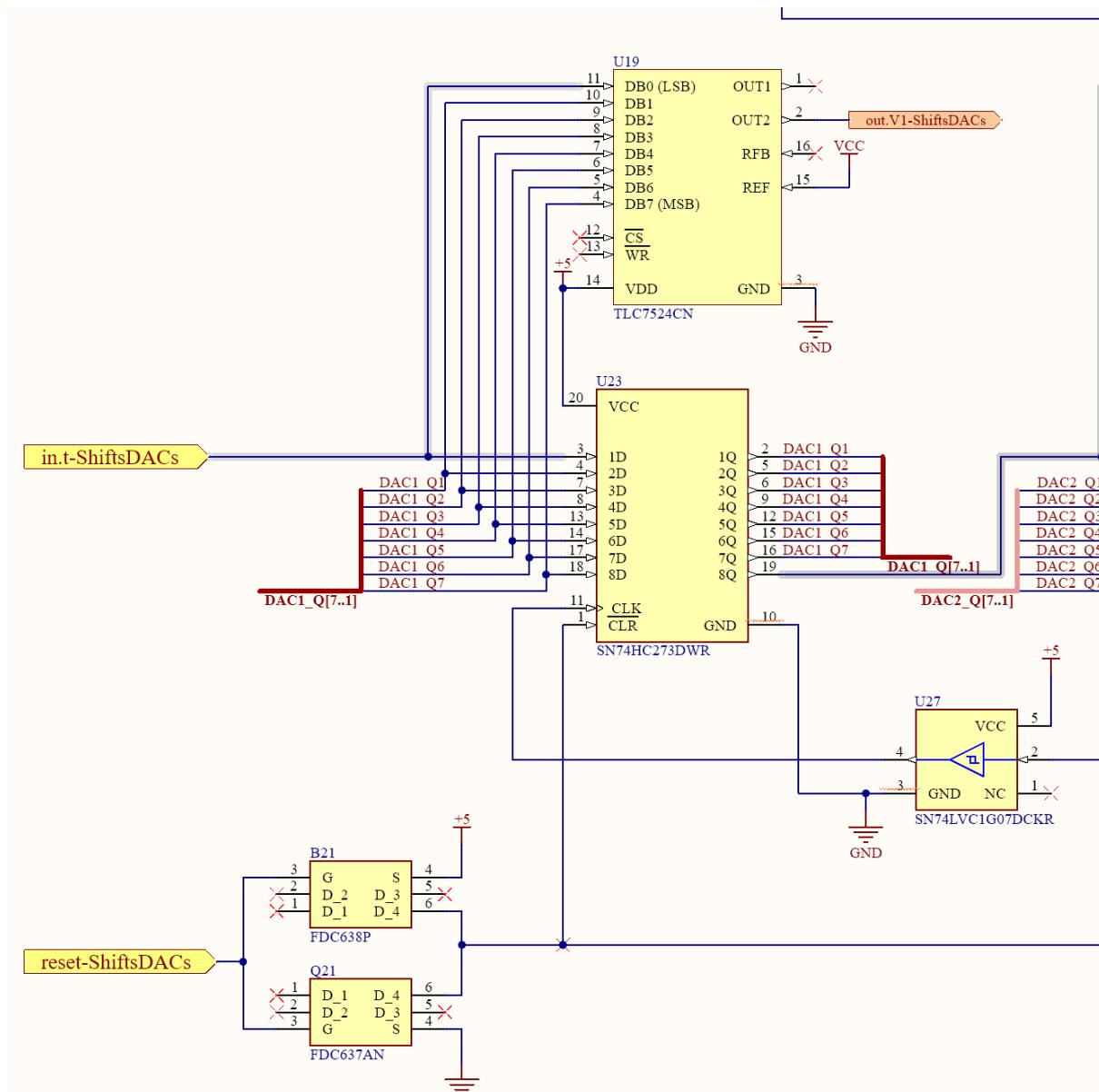


Fig. 33. Input stage of “ShiftsDACS” schematic

It can be observed that the input stage leads into the very first D-flip flop (U23), which is also connected in parallel to a corresponding DAC (U19). Thus, the DAC refreshes its output whenever the leading clock edge arrives at the input. The CLK is led in starting from the last shift register, and ending with this one, while U27, which is the buffer, acts as a time delay

between subsequent stages.

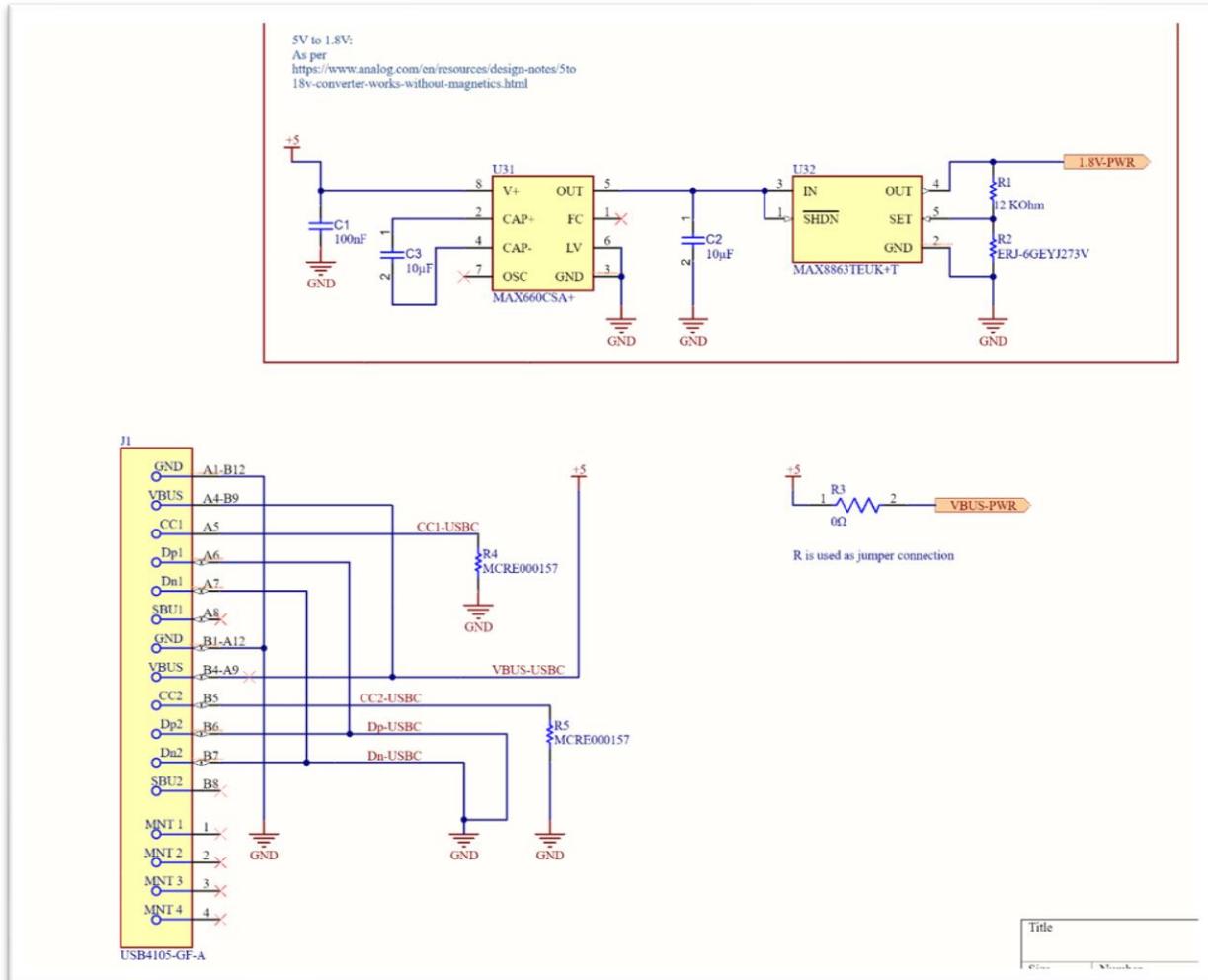


Fig. 34. Schematic for input power, and Buck converter

Fig. 34 displays the power delivery components for the entire PCB, measuring about 19x17cm. J1 is actually a USB-C connector, where ports CC1 and CC2 are pulled down to ensure free power delivery of about 15W from the USB-C.

Circled in red is the buck converter, to step the 5v voltage down to 1.8V while still providing sufficient current of ~500mA. All the schematics for the project can be found in Appendix at the end of this paper.

3.4 Layout on PCB

After carrying out simple design rule checks, the components were ready to be transferred onto the PCB.

The PCB layer consists of a thin solder mask, prepeg, substrate, and signal layers. All the components in one schematic could be grouped into “Rooms” which enabled the placement of similar component close together. Visible are the copper traces connecting different components; initially there was the plan to route the traces by hand, but for demonstration purposes, the built-in automatic router sufficed.

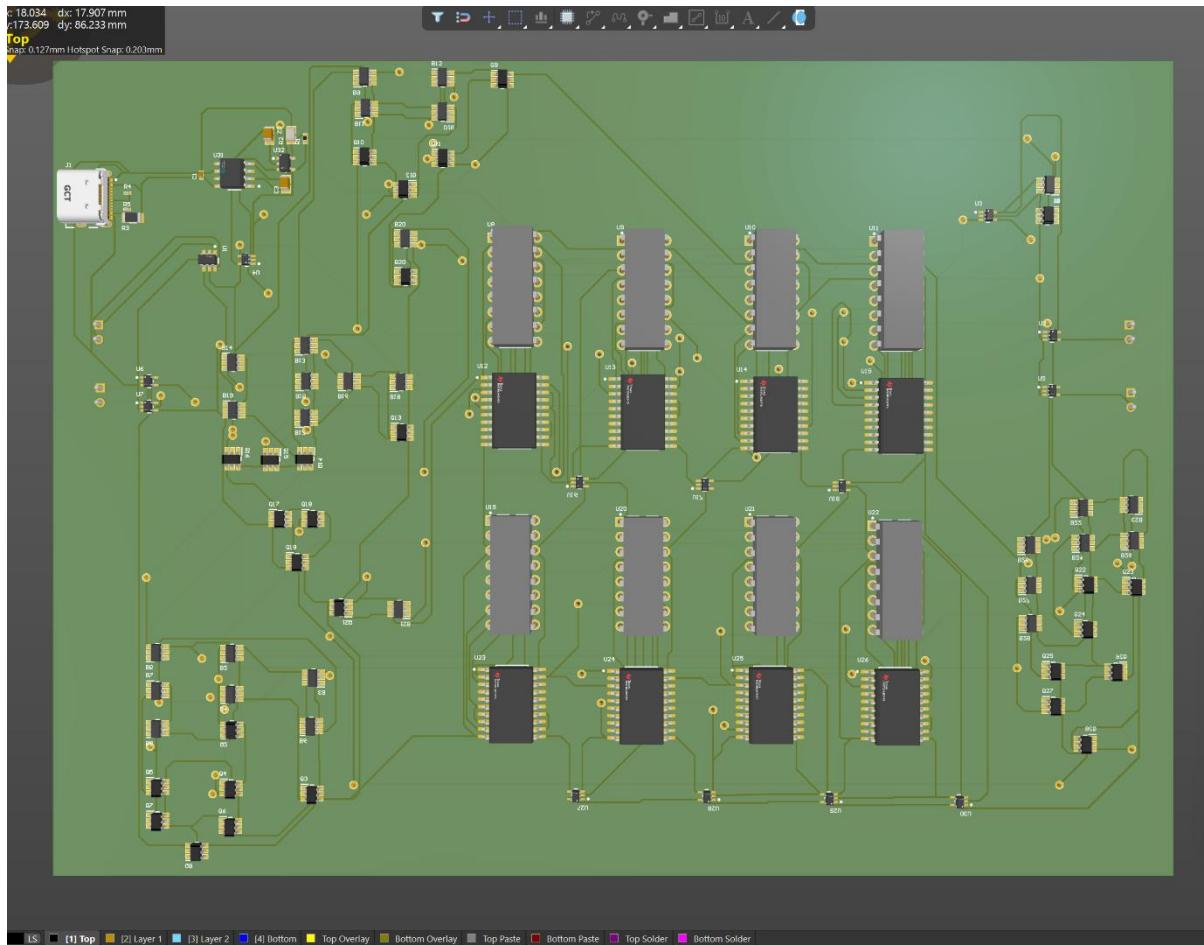


Fig. 35. PCB with solder mask, top view

There was definitely room for improvement; the underutilized space on the board meant that there was additional room for components to move together. However, concerns arise about electromagnetic interference, a very common problem in PCB design as copper traces run parallel and close to one another. However, I felt that as a proof of concept, the overall layout and design of the board would suffice, and with a lead time of 1-3 day, the design could have been markedly improved.

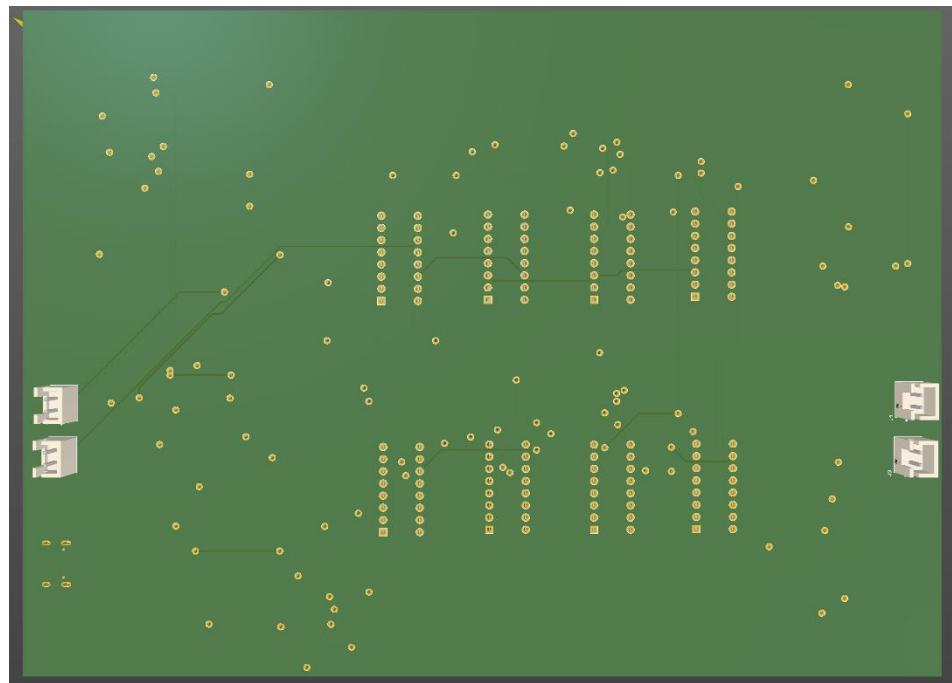
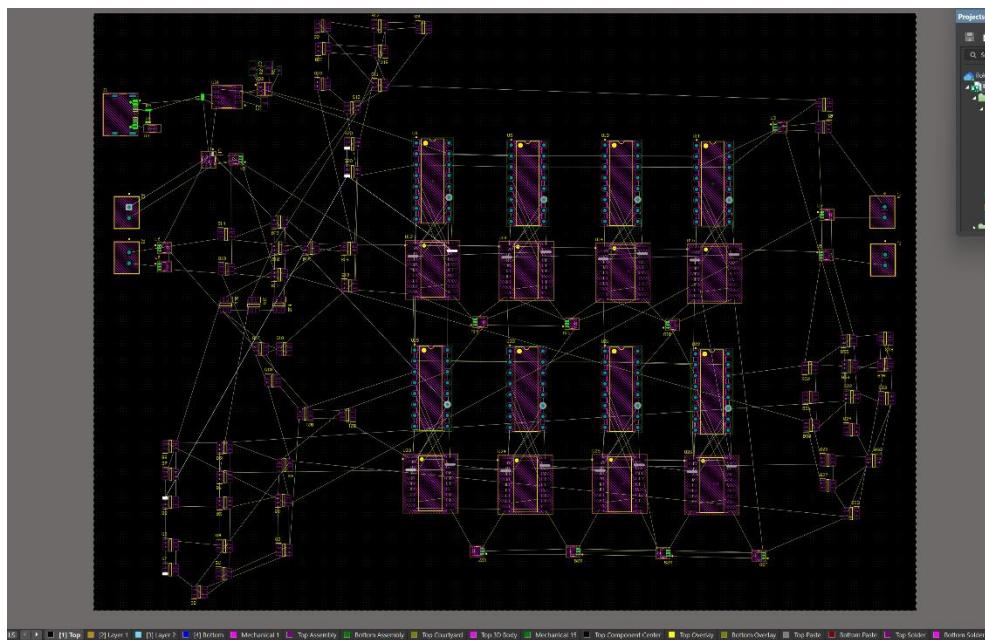


Fig. 36. Back of PCB. 2 pin connectors are included



Chapter 4: Remarks

The previous chapter embarks heavily on the circuit design aspect of the control circuit and all the way up to fabrication. To elaborate on the possible expansion for this project, the control circuit does give us some information as to compatible hardware. For instance, the minimum rise time of the DACs is about 28ns. Additionally, the mounting of the pads on the back as shown in Fig. 36. opens up the possibility of connection to the different unit cells. Further areas for exploration include the realization of varactor diodes, and solving

the issue of having a control board too large for the IRS unit cells, especially in this 2x2 configuration as shown.

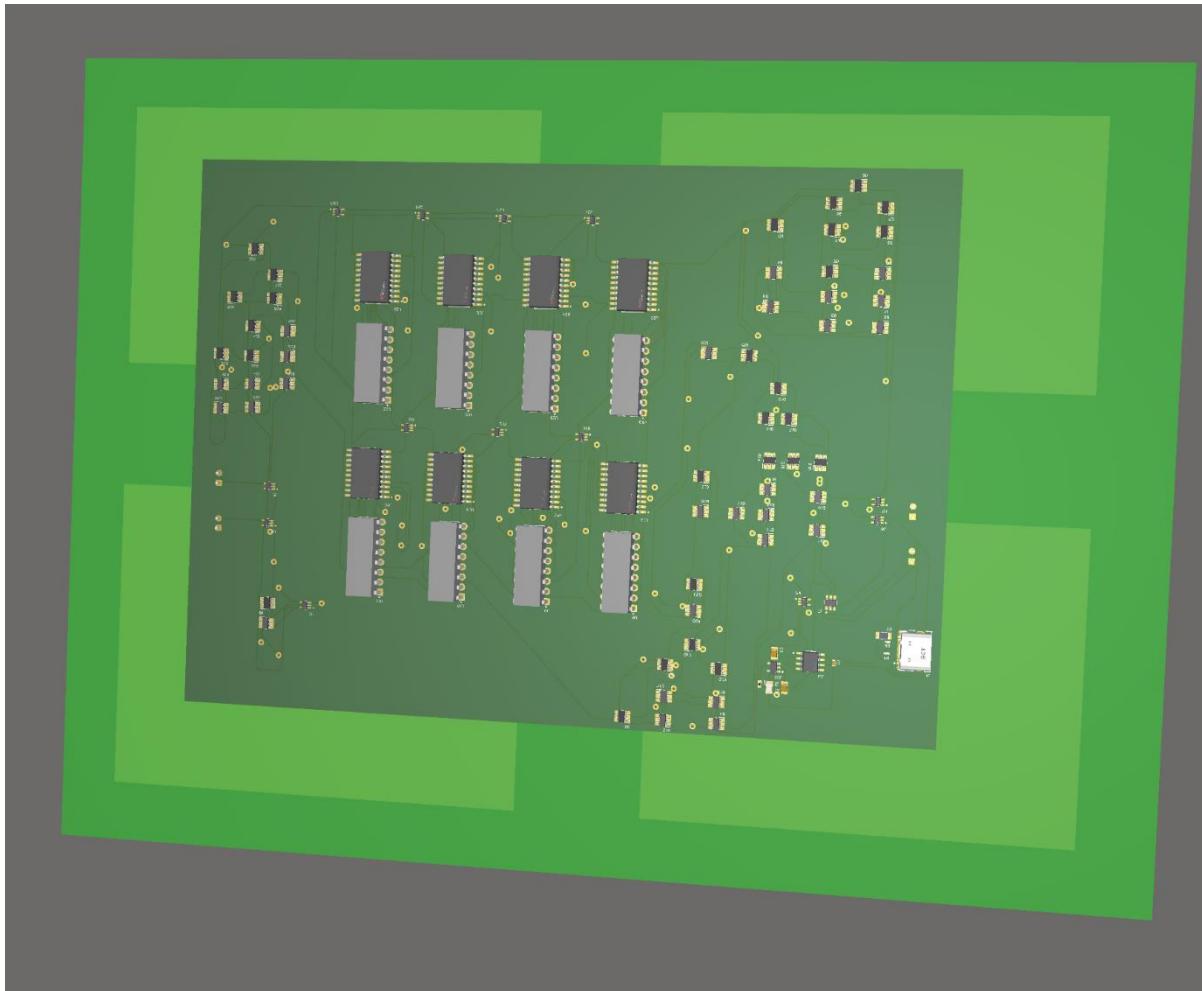


Fig. 38. Proof-of-concept. (the unit cells are not connected)

Chapter 5: Conclusion

This report has primarily focused on reviewing the existing literature on Intelligent Reflecting Surfaces (IRS) to establish key system requirements for a more comprehensive evaluation. A suitable unit cell and circuit model for the IRS system has been identified; however, this project suffered from over-generalization, which made it challenging, especially for such a research topic that is on the frontier of wireless communications.

Several challenges were encountered throughout this phase. One of the primary difficulties was understanding and applying the literature. The numerous nuances behind the performance characteristics of the IRS was difficult to understand, compounded by the fact that these are fundamentally RF systems, one of the most challenging areas in EE to understand.

However, as an individual I did have many learning takeaways in learning to use various software to aid me in circuit simulation, synthesis, as well as the process of drawing up proper schematics and creating a PCB for the control circuit, which is the typical workflow of engineers. I also learnt to use discretion when thinking about the flow of control in circuits. For the bigger picture, fabricating the PCB was an area I focused on which was difficult to do given my initial interest in the localization and functional aspects of the IRS.

Further constraints included limited time availability due to the complexity of researching the BS-IRS-UE system. However, there should be adequate literature review completed at this point to provide the basic for a Cartesian coordinate-based model, given many of the optimal aspect of IRS like being semi-passive, large number of elements most aspects of the design have been refined to ensure a precise and structured analysis. In the future, if the control circuit as demonstrated here is refined and fabricated, a more suitable unit cell will need to be chosen. The proof-of-concept PCB created here may serve as a suitable stepping stone, if complex IC fabrication capabilities are not available.

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[https://entuedu.sharepoint.com/sites/Student/dept/ctlp/SitePages/Exploring-the-Impact-of-Generative-Artificial-Intelligence-\(GAI\)-Tools-on-Education.aspx](https://entuedu.sharepoint.com/sites/Student/dept/ctlp/SitePages/Exploring-the-Impact-of-Generative-Artificial-Intelligence-(GAI)-Tools-on-Education.aspx)

1. Complete the following declaration if applicable.
2. Create a Paper Trail to document the input prompt, output obtained, and how you have used it.

I Loke Yee Wai, Ivan (student name), ILOKE002 @e.ntu.edu.sg (NTU email) honestly and sincerely make the following declaration in relation to the following course submission.

1. Name of course:
2. Course Code: A3311-232
3. Instructor: A/P Soong Boon Hee
4. Title of Assignment/Project Submission: Survey of Intelligent Reflecting Surfaces and Localization for Wireless Systems

In relation to the foregoing I hereby declare that, fully and properly in accordance with the Assignment/Project Instructions I have (check where appropriate):

- | | |
|--|-------------------------------------|
| i. Used GAI as permitted to assist in generating key ideas only | <input checked="" type="checkbox"/> |
| ii. Used GAI as permitted to assist in generating a first text only. | <input checked="" type="checkbox"/> |
| And/or | |
| iii. Used GAI to refine syntax and grammar for correct language submission only. | <input checked="" type="checkbox"/> |
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| iv. As it is not permitted: Not used GAI assistance in any way in the development or generation of this assignment or project. | <input checked="" type="checkbox"/> |

I also declare that I have:

- a. Fully and honestly submitted the digital paper trail required under the assignment/project instructions; and that
- b. Wherever GAI assistance has been employed in the submission in word or paraphrase or inclusion of a significant idea or fact suggested by the GAI assistant, I have acknowledged this by a footnote; and that,
- c. Apart from the foregoing notices, the submission is wholly my own work.

Loke Yee Wai, Ivan 
Student Name & Signature

1 Feb 2025
Date

References

- [1] M. Parker, “Error Correction Coding,” in *Digital Signal Processing 101*, Newnes, 2010, pp. 125–142. doi: <https://doi.org/10.1016/B978-1-85617-921-8.00016-X>.
- [2] H. Obeidat, W. Shuaieb, O. Obeidat, and R. Abd-Alhameed, “A Review of Indoor Localization Techniques and Wireless Technologies,” *Wireless Personal Communications*, vol. 119, pp. 295–296, Feb. 2021, doi: <https://doi.org/10.1007/s11277-021-08209-5>.
- [3] M. Hua, G. Chen, K. Meng, S. Ma, C. Yuen, and H. C. So, “3D Multi-Target Localization Via Intelligent Reflecting Surface: Protocol and Analysis,” *arXiv.org*, 2023. <https://arxiv.org/abs/2310.15574> (accessed Oct. 12, 2024).
- [4] Q. Wu, S. Zhang, B. Zheng, C. You, and R. Zhang, “Intelligent Reflecting Surface-Aided Wireless Communications: A Tutorial,” *IEEE Transactions on Communications*, vol. 69, no. 5, pp. 3313–3351, May 2021, doi: <https://doi.org/10.1109/tcomm.2021.3051897>.
- [5] R. Zhang, Q. Wu. (2020). "Towards Smart and Reconfigurable Environment: Intelligent Reflecting Surface Aided Wireless Network", IEEE Global Communications Conference (Globecom). Available: https://www.ece.nus.edu.sg/stfpage/elezhang/Publications_new/IRS_GC%202020.pdf
- [6] D. Reynders and E. Wright, *Practical TCP/IP and Ethernet Networking for Industry*. Elsevier, 2003, p. 75. Available: <https://github.com/akib1162100/mac/blob/master/Practical%20TCP-IP%20and%20Ethernet%20Networking%20for%20Industry.pdf>
- [7] L-com, “Choosing the Right WiFi Antenna for your Application,” 2019. Available: <https://www.l-com.com/images/downloadables/white-papers>Selecting-the-Right-Wifi-Antenna-for-your-application.pdf>
- [8] K.-C. Huang, Z. Wang, *Millimeter Wave Communication Systems*. John Wiley & Sons, 2011. Available: <https://books.google.com/books?id=kCmyPdxme1AC&pg=PP17>
- [9] R. Goodwins, “Next-generation 802.11ax wi-fi: Dense, fast, delayed,” ZDNET, Oct. 03, 2018. <https://www.zdnet.com/home-and-office/networking/next-generation-802-11ax-wi-fi-dense-fast-delayed/> (accessed Jul. 04, 2024).
- [10] Electronics-Notes.com, “Horn Antenna | Microwave Horn | Electronics Notes,” *Electronics-notes.com*, 2019. Available: <https://www.electronics-notes.com/articles/antennas-propagation/horn-antenna/basics-primer.php>
- [11] D. W. Ball, “Maxwell’s Equations,” *Spie.org*, 2024. https://spie.org/publications/spe-publication-resources/optipedia-free-optics-information/fg08_p07-08_maxwells_equation
- [12] G. H. Kim and D. K. Kim, “Computationally efficient phase control algorithm for

intelligent reflecting surface-aided multiuser systems," *ICT Express*, vol. 9, no. 6, pp. 1137, Apr. 2023, doi: <https://doi.org/10.1016/j.icte.2023.04.002>.

[13] H. Yang *et al.*, "A programmable metasurface with dynamic polarization, scattering and focusing control," *Scientific Reports*, vol. 6, no. 1, Oct. 2016, doi: <https://doi.org/10.1038/srep35692>.

[14] Y. Liu *et al.*, "Reconfigurable Intelligent Surfaces: Principles and Opportunities," *IEEE Communications Surveys & Tutorials*, vol. 23, no. 3, p. 1551, 2021, doi: <https://doi.org/10.1109/comst.2021.3077737>.

[15] BYJU'S, "Huygens Principle - Principle of Wavefront, Diffraction, FAQs," *BYJUS*. <https://byjus.com/physics/the-huygens-principle-and-the-principle-of-a-wave-front/>

[16] National Institute of Standards and Technology, "NISTIR 6055 NIST Construction Automation Program Report No. 3 Electromagnetic Signal Attenuation in Construction Materials," Oct. 1997. Available: <https://nvlpubs.nist.gov/nistpubs/Legacy/IR/nistir6055.pdf>

[17] X. Pei *et al.*, "RIS-Aided Wireless Communications: Prototyping, Adaptive Beamforming, and Indoor/Outdoor Field Trials," *IEEE TRANSACTIONS ON COMMUNICATIONS*, vol. 69, no. 12, pp. 8627–8640, Dec. 2021, doi: <https://doi.org/10.1109/tcomm.2021.3116151>.

[18] Alexandros Pitilakis *et al.*, "A Multi-Functional Reconfigurable Metasurface: Electromagnetic Design Accounting for Fabrication Aspects," *IEEE Transactions on Antennas and Propagation*, vol. 69, no. 3, pp. 1440–1454, Mar. 2021, doi: <https://doi.org/10.1109/tap.2020.3016479>.

[19] L. Petrou, K. M. Kossifos, M. A. Antoniades, and J. Georgiou, "A Programmable Complex Impedance IC for Scalable and Reconfigurable Meta-Atoms," *IEEE Transactions on Nanotechnology*, vol. 21, pp. 692–702, Jan. 2022, doi: <https://doi.org/10.1109/tnano.2022.3221309>.

[20] Y. Wang, L. Sun, Z. Du, and Z. Zhang, "Review antenna design for Modern Mobile Phones: A Review," *Electromagnetic Science*, vol. 2, no. 2, pp. 1–36, Jun. 2024. doi:10.23919/emsci.2023.0052

[21] M. Rütschlin, "5G Antenna Design for Mobile Phones," *SIMULIA EM eSeminar Series 2018*, Nov. 29, 2018, Available: <https://www.youtube.com/watch?v=aldh5e4XH6w>.

[22] J. J. Kim *et al.*, "ANTENNA AND DEVICE CONFIGURATIONS," Oct. 8, 2024, Available: [US020220278452A120220901](https://www.uspto.gov/patent-application-number-US020220278452A120220901).

[23] Y. Lu, M. Koivisto, J. Talvitie, M. Valkama and E. S. Lohan, "Positioning-Aided 3D Beamforming for Enhanced Communications in mmWave Mobile Networks," in *IEEE Access*, vol. 8, pp. 55513–55525, 2020, doi: 10.1109/ACCESS.2020.2981815.

[24] Srivastava, P. (2022). Introduction to Asynchronous Circuit Design," *Completion Detection in Asynchronous Circuits*. Springer, Cham. pp. 1, <https://doi.org/10.1007/978-3->

031-18397-3_1.

- [25] L. Petrou, K. M. Kossifos, M. A. Antoniades, and J. Georgiou, “A Programmable Complex Impedance IC for Scalable and Reconfigurable Meta-Atoms,” *IEEE Transactions on Nanotechnology*, vol. 21, pp. 692–702, Jan. 2022, doi: <https://doi.org/10.1109/tnano.2022.3221309>.
- [26] E. Maier, “Application Note: Designing with Shift Registers,” , pp. 11, Jul. 2022, Available: https://www.ti.com/lit/an/scea117/scea117.pdf?ts=1739274271767&ref_url=https%252F%252Fwww.google.com%252F.
- [27] Texas Instruments, SNx4HC273 Octal D-Type Flip-Flops With Clear,” SCLS136F datasheet, Dec. 1982 [Apr. 2022]. Available: <https://www.ti.com/lit/gpn/sn74hc273>
- [28] Georg Ofenbeck, R. Steinmann, V. Caparros, D. G. Spampinato, and M. Püschel, “Applying the roofline model,” *2014 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Mar. 2014, doi: <https://doi.org/10.1109/ispass.2014.6844463>.
- [29] henkwymeersch, “GitHub - henkwymeersch/RISLensLocalization: 3D Localization with RIS lens and a single antenna,” GitHub, 2020. <https://github.com/henkwymeersch/RISLensLocalization> (accessed Dec. 01, 2024).
- [30] D. F. Sievenpiper, J. H. Schaffner, H. J. Song, R. Y. Loo, and G. Tangonan, “Two-dimensional beam steering using an electrically tunable impedance surface,” *IEEE Transactions on Antennas and Propagation*, vol. 51, no. 10, pp. 2713–2722, Oct. 2003, doi: <https://doi.org/10.1109/tap.2003.817558>.
- [31] Sergei Tretyakov and Constantin Simovski, “DYNAMIC MODEL OF ARTIFICIAL REACTIVE IMPEDANCE SURFACES,” *Journal of Electromagnetic Waves and Applications*, vol. 17, no. 1, pp. 131–145, Jan. 2003, doi: <https://doi.org/10.1163/156939303766975407>.
- [32] “Measuring Self Resonant Frequency.” Available: https://www.coilcraft.com/getmedia/8ef1bd18-d092-40e8-a3c8-929bec6adfc9/doc363_measuringsrf.pdf
- [33] PTM, “Microelectronics Co-design Research Group,” *Umn.edu*, 2024. <https://mec.umn.edu/ptm>
- [34] “C-element | Semantic Scholar,” *Semanticscholar.org*, 2025. <https://www.semanticscholar.org/topic/C-element/878060> (accessed Feb. 03, 2025).

Appendix

180nm SPICE predictive transistor model, from [PTM](#)

```

1. *
2. * Predictive Technology Model Beta Version
3. * 180nm NMOS SPICE Parametersv (normal one)
4. *
5.
6. .model NMOS NMOS
7. +Level = 49
8.
9. +LInt = 4.e-08 Tox = 4.e-09
10. +Vth0 = 0.3999 Rdsw = 250
11.
12. +lmin=1.8e-7 lmax=1.8e-7 wmin=1.8e-7 wmax=1.0e-4 Tref=27.0 version =3.1
13. +Xj= 6.000000E-08 Nch= 5.950000E+17
14. +lln= 1.000000 lwn= 1.000000 wln= 0.00
15. +wwn= 0.00 ll= 0.00
16. +lw= 0.00 lwl= 0.00 wint= 0.00
17. +wl= 0.00 ww= 0.00 wwl= 0.00
18. +Mobmod= 1 binunit= 2 xl= 0
19. +xw= 0 binflag= 0
20. +Dwg= 0.00 Dwb= 0.00
21.
22. +K1= 0.5613000 K2= 1.000000E-02
23. +K3= 0.00 Dvt0= 8.000000 Dvt1= 0.7500000
24. +Dvt2= 8.000000E-03 Dvt0w= 0.00 Dvt1w= 0.00
25. +Dvt2w= 0.00 Nlx= 1.650000E-07 W0= 0.00
26. +K3b= 0.00 Ngate= 5.000000E+20
27.
28. +Vsat= 1.3800000E+05 Ua= -7.000000E-10 Ub= 3.500000E-18
29. +Uc= -5.250000E-11 Prwb= 0.00
30. +Prwg= 0.00 Wr= 1.000000 U0= 3.500000E-02
31. +A0= 1.100000 Keta= 4.000000E-02 A1= 0.00
32. +A2= 1.000000 Ags= -1.000000E-02 B0= 0.00
33. +B1= 0.00
34.
35. +Voff= -0.12350000 NFactor= 0.9000000 Cit= 0.00
36. +Cdsc= 0.00 Cdscb= 0.00 Cdscd= 0.00
37. +Eta0= 0.2200000 Etab= 0.00 Dsub= 0.8000000
38.
39. +Pclm= 5.000000E-02 Pdiblc1= 1.200000E-02 Pdiblc2= 7.500000E-03
40. +Pdiblc= -1.350000E-02 Drout= 1.7999999E-02 Pscbe1= 8.6600000E+08
41. +Pscbe2= 1.000000E-20 Pvag= -0.2800000 Delta= 1.000000E-02
42. +Alpha0= 0.00 Beta0= 30.000000
43.
44. +kt1= -0.3700000 kt2= -4.000000E-02 At= 5.500000E+04
45. +Ute= -1.4800000 Ua1= 9.5829000E-10 Ub1= -3.3473000E-19
46. +Uc1= 0.00 Kt1l= 4.000000E-09 Prt= 0.00
47.
48. +Cj= 0.00365 Mj= 0.54 Pb= 0.982
49. +Cjsw= 7.9E-10 Mjsw= 0.31 Php= 0.841
50. +Cta= 0 Ctp= 0 Pta= 0
51. +Ptp= 0 JS=1.50E-08 JSW=2.50E-13
52. +N=1.0 Xti=3.0 Cgdo=2.786E-10
53. +Cgso=2.786E-10 Cgbo=0.0E+00 Capmod= 2
54. +NQSMOD= 0 Elm= 5 Xpart= 1
55. +Cgsl= 1.6E-10 Cgd1= 1.6E-10 Ckappa= 2.886
56. +Cf= 1.069e-10 Clc= 0.0000001 Cle= 0.6
57. +Dlc= 4E-08 Dwc= 0 Vfbcv= -1
58.

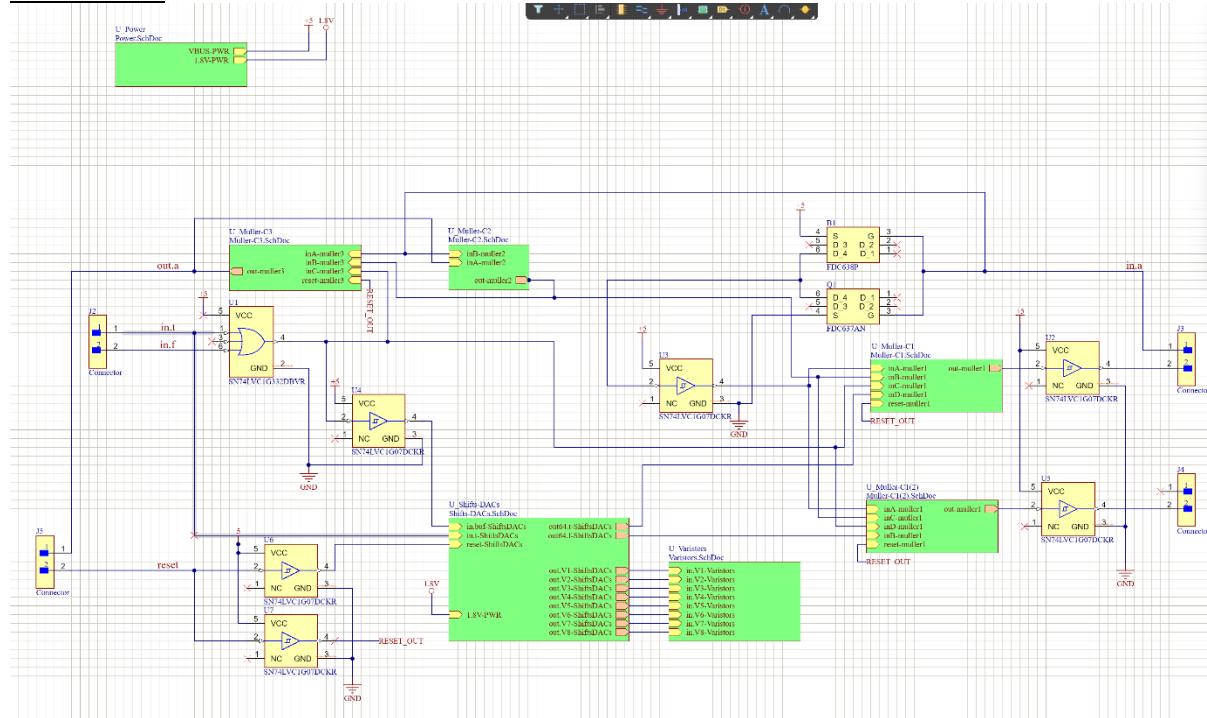
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Appendix - Schematics

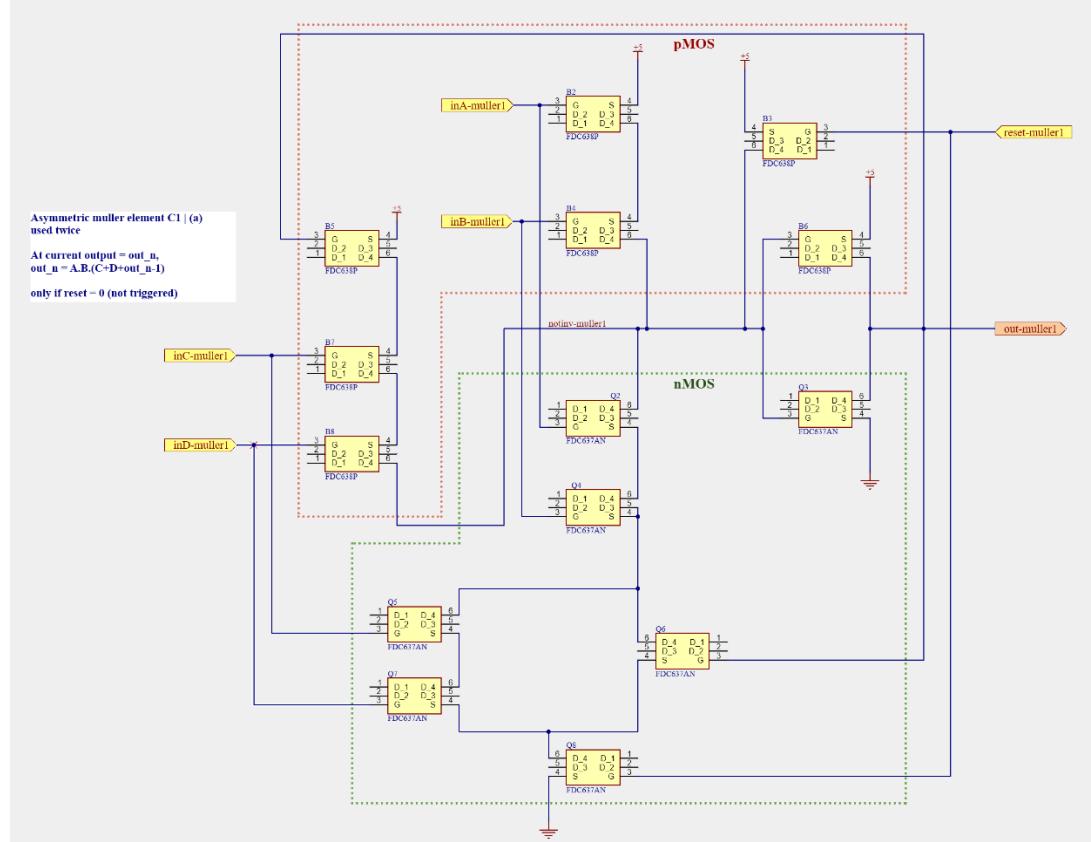
Screenshots are high-resolution

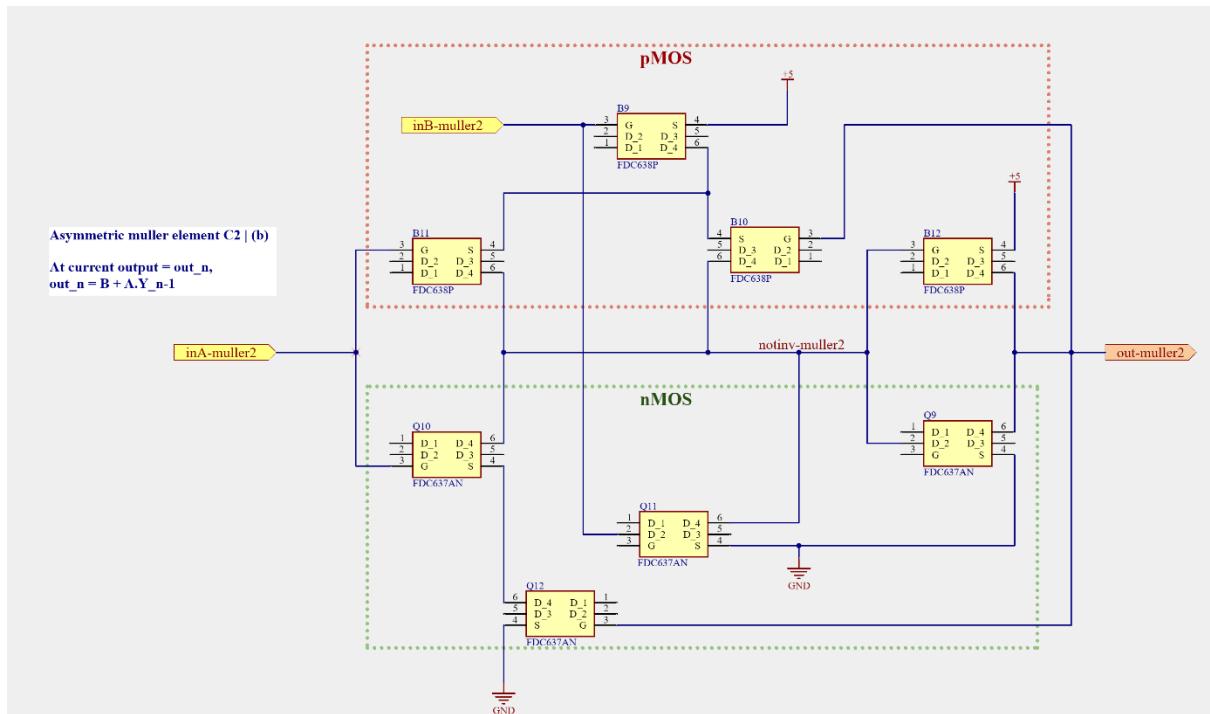
Schematics are also available at https://github.com/ivloke/FYP_IRS for reference

Main.SchDoc



Muller-C1.SchDoc

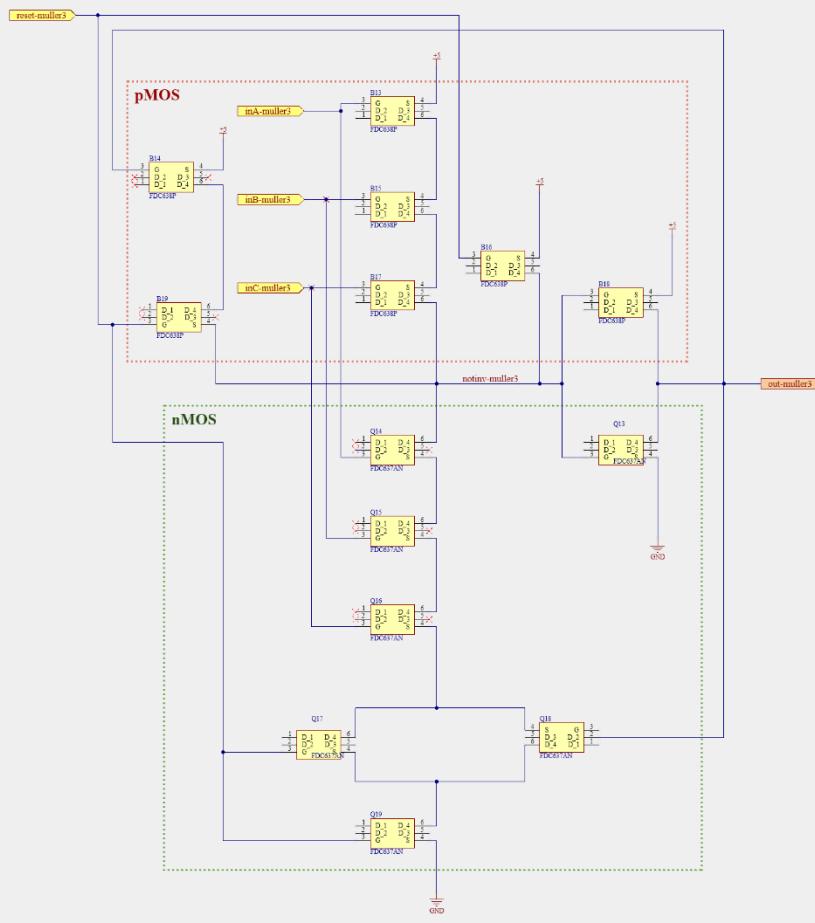


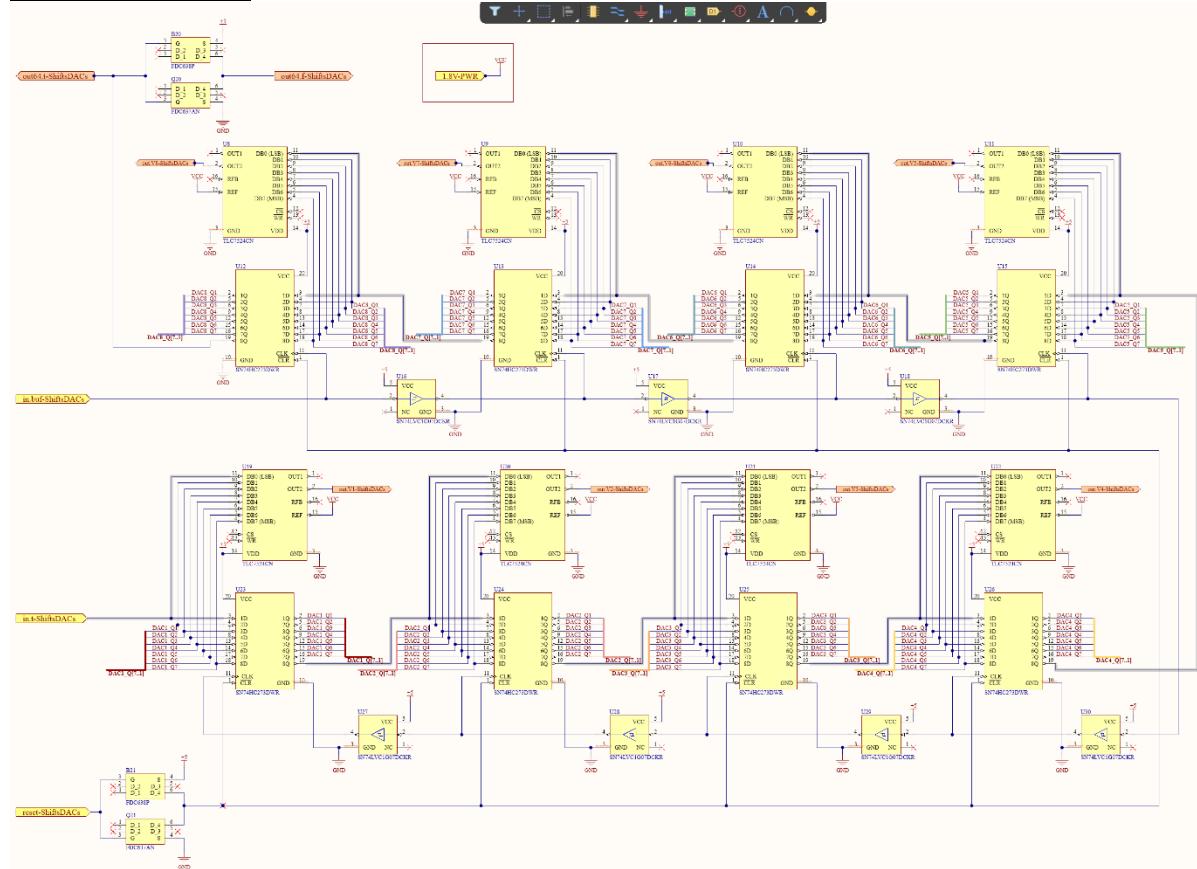
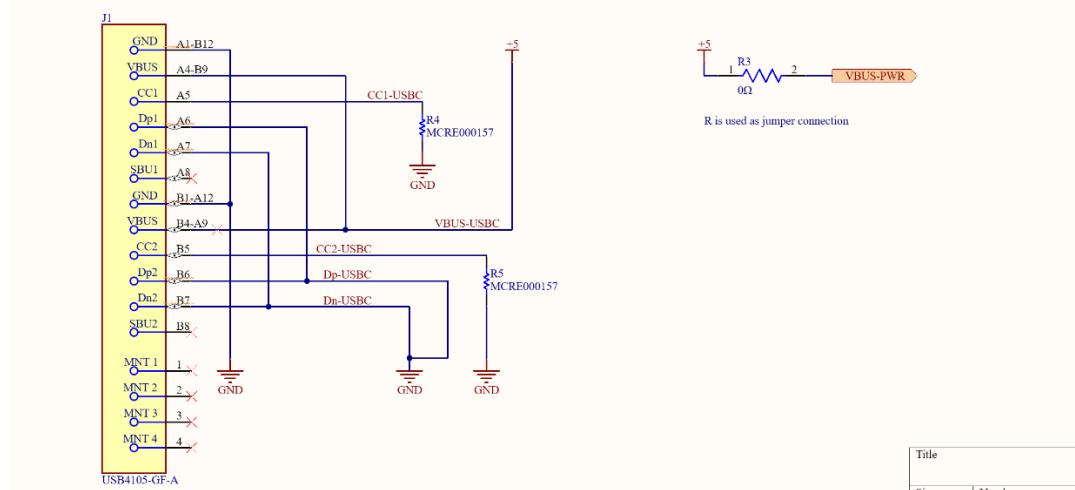
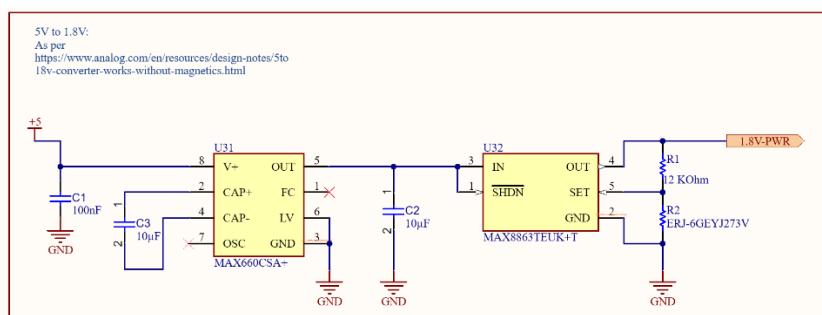


Muller-C3.SchDoc

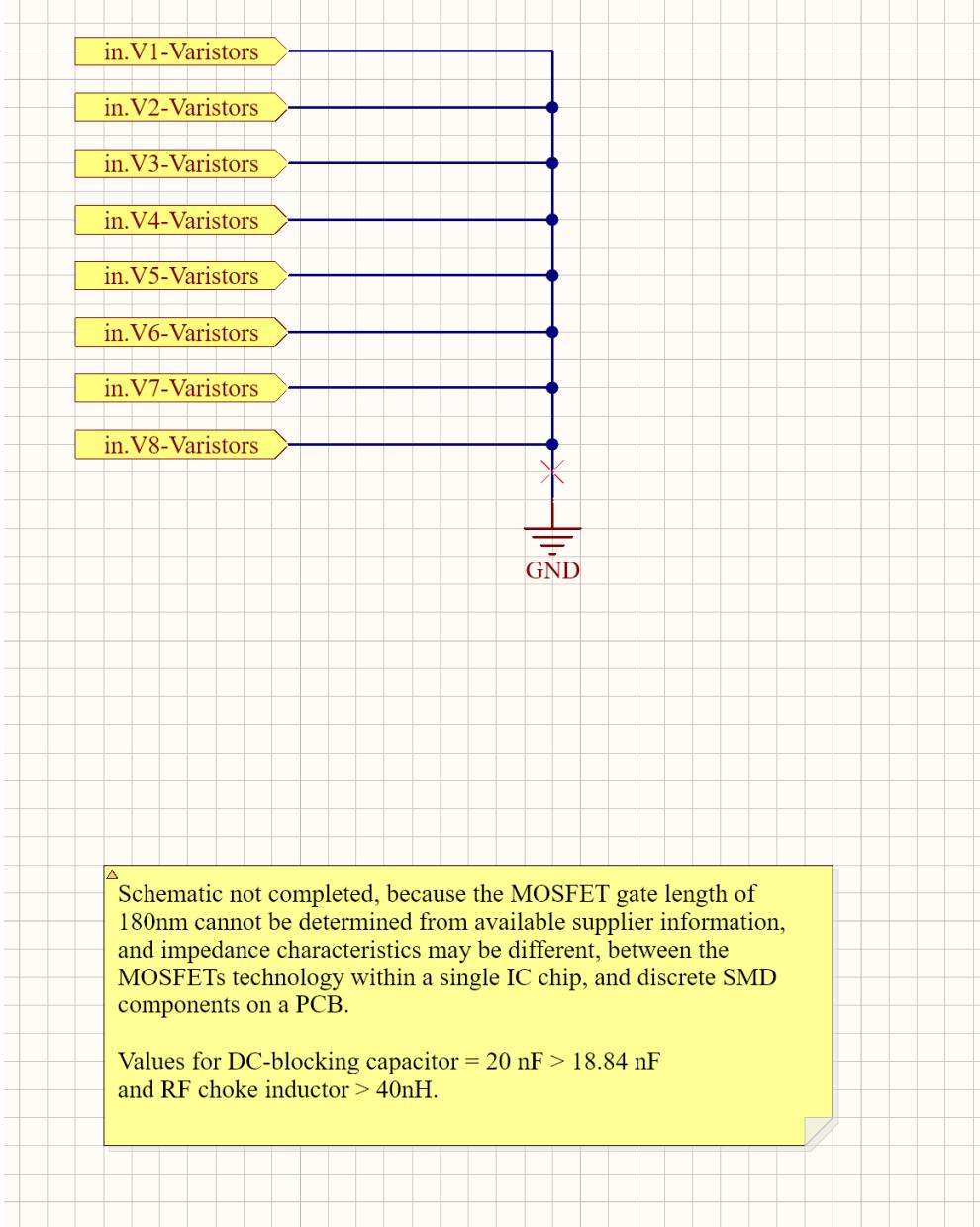
Asymmetric muller element C3 | (c)At current output = out_n ,
 $\text{out_n} = (\text{A.B.C}) \oplus \text{out_n-1}$

only if reset = 0 (not triggered)



Shifts-DACs.SchDocPower.SchDoc

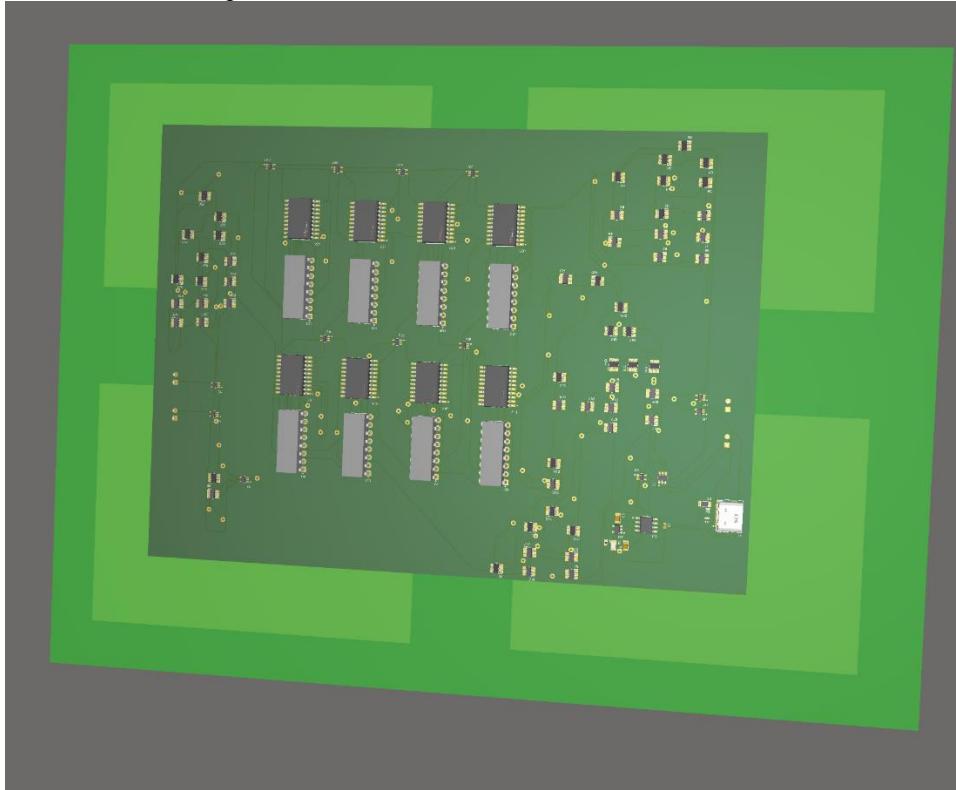
Title	Size	Number
-------	------	--------

Varistors.SchDocBill of Materials

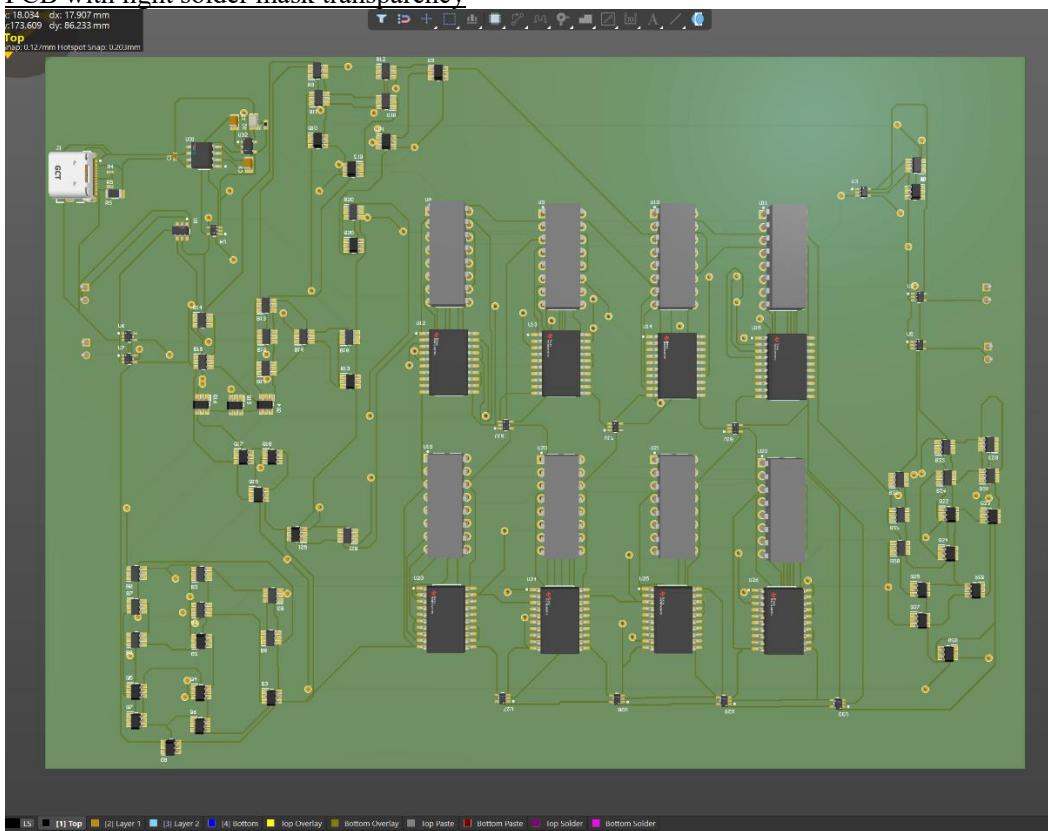
Item Details							Document options		
Line #	Name	Description	Designator	Revision ID	Revision State	Revision Status			
1	FDC638P	Low gate charge (10...	B1, B2, B3, B4, B5, B...	CMP-007...	Draft	Up to date			
2	Capacitor 0.1 uF +/-...	Chip Capacitor, 0.1...	C1	CMP-001...	Draft	Up to date			
3	Capacitor 10 uF +/-...	Chip Capacitor, 10 u...	C2, C3	CMP-001...	Draft	Up to date			
4	USB4105-GF-A	CONN RCPT USB2.0...	J1	CMP-2451...	New From Design	Up to date			
5	B2B-XH-A(LF)(SN)	CONN HEADER VER...	J2, J3, J4, J5	CMP-2000...	Released	Up to date			
6	FDC637AN	Low gate charge (10...	Q1, Q2, Q3, Q4, Q5,...	CMP-005...	Draft	Up to date			
7	ERJ-2RKF1202X	Chip Resistor, 12 KO...	R1	CMP-2002...	Released	Up to date			
8	ERJ-GGEV1273V		R2	CMP-0201...	Released	Up to date			
9	CRCW12060000Z0E...	RES 0 OHM JUMPER...	R3	CMP-0240...	New From Design	Up to date			
10	MCRE000157		R4, R5	CMP-2004...	Released	Up to date			
11	SN74LVC1G332DBVR	IC GATE OR 1CH 3-I...	U1	CMP-0859...	New From Design	Up to date			
12	SN74LVC1G07DCKR	Buffer, LVC/LCX/Z S...	U2, U3, U4, U5, U6,...	CMP-0002...	Draft	Up to date			
13	TLC7524CN	8-Bit, 0.1 us MDAC...	U8, U9, U10, U11, U...	CMP-0004...	Released	Up to date			
14	SN74HC273DWR	D Flip-Flop, HC/UH...	U12, U13, U14, U15,...	CMP-0002...	Draft	Out of date			
15	MAX660CSA+	IC REG CHARGE PU...	U31	CMP-0572...	New From Design	Up to date			
16	MAX8863TEUK+T	IC REG LIN POS ADJ...	U32	CMP-0572...	New From Design	Up to date			

Appendix – PCB screenshots

IRS Proof of Concept

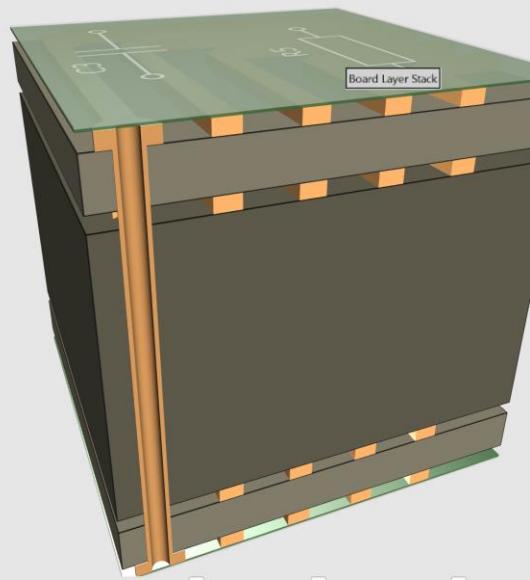
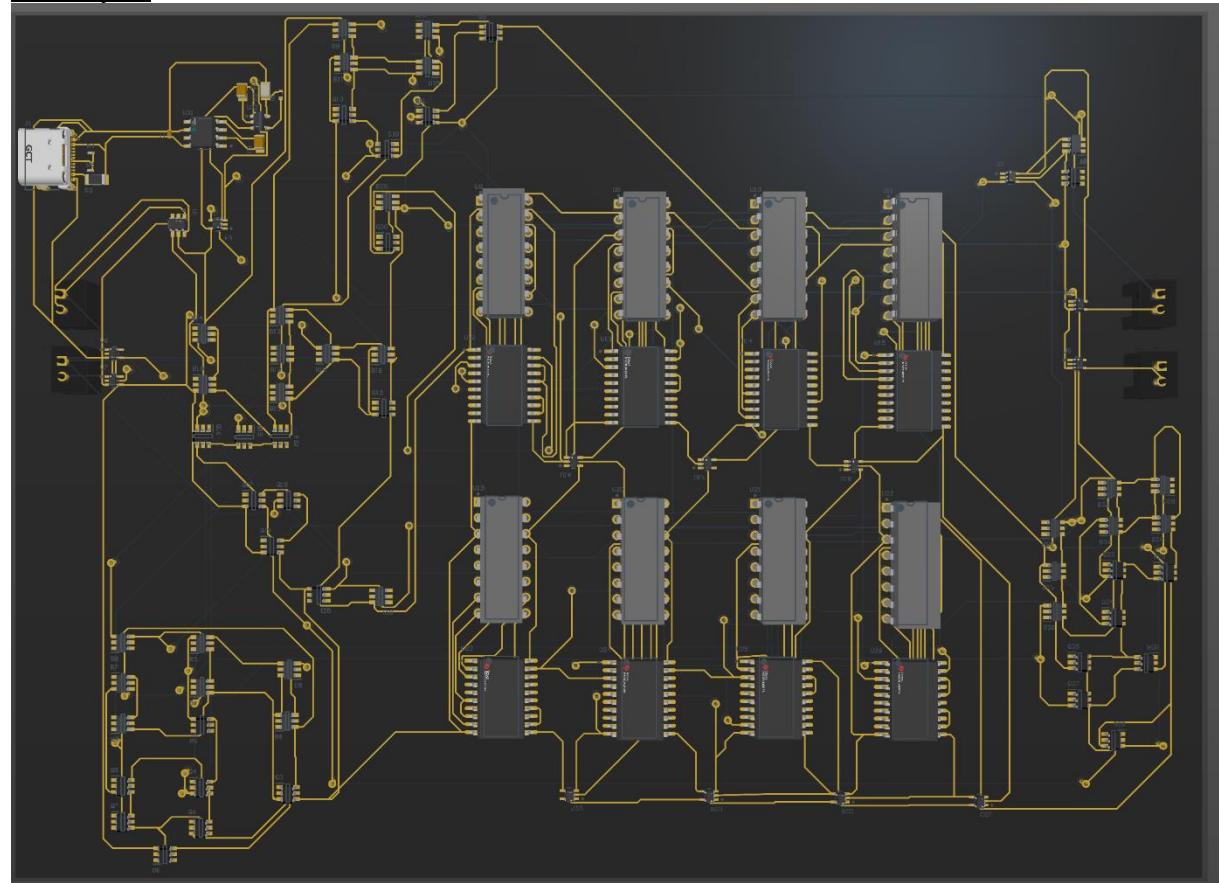


PCB with light solder mask transparency

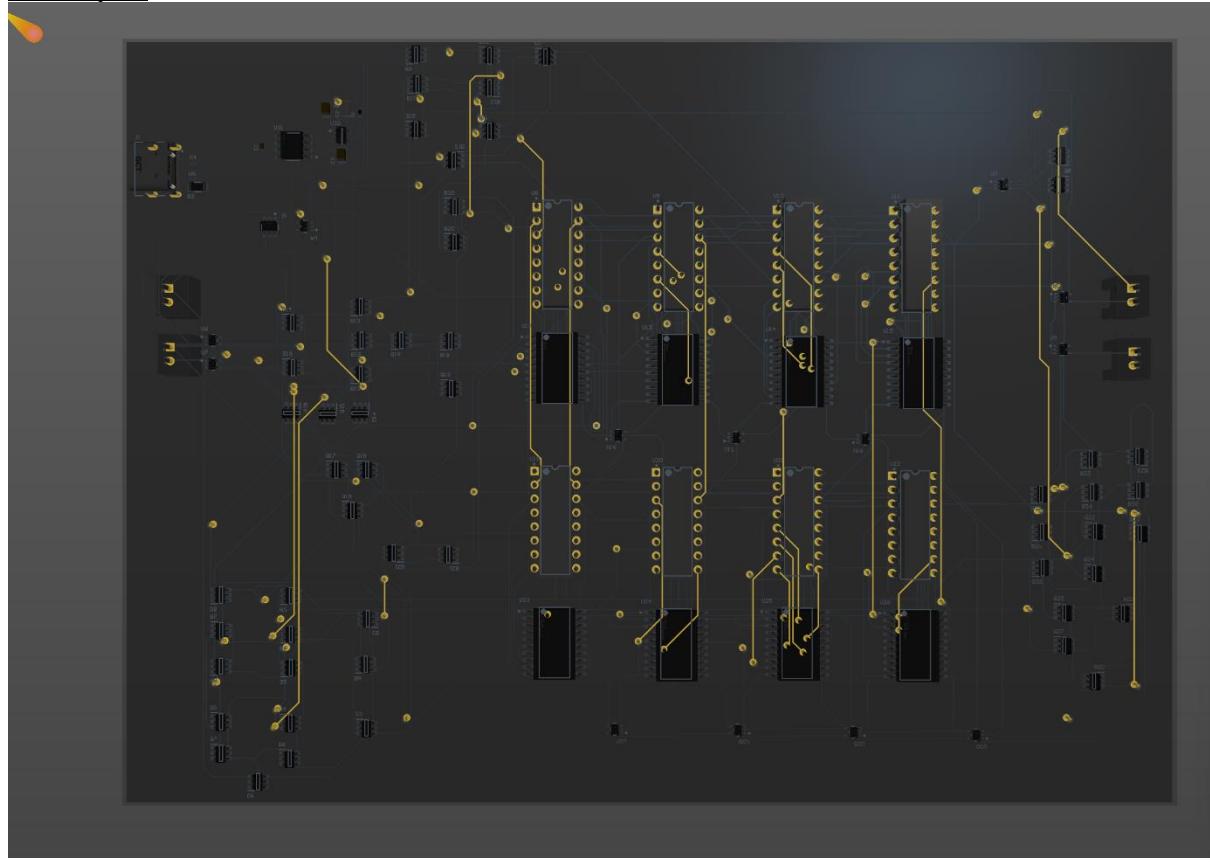


PCB stackup and visualizer

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
1	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
1	Top	PP-006	Signal	1oz	0.06mm		
2	Layer 1	CF-004	Prepreg		0.2mm	4.1	0.02
2	Core1	Core-009	Core		1.2mm	4.5	
3	Layer 2	CF-004	Signal	1oz	0.06mm		
3	PP2	PP-006	Prepreg		0.2mm	4.1	0.02
4	Bottom	CF-004	Signal	1oz	0.06mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5	
	Bottom Overlay		Overlay				

PCB Layer1

PCB Layer2



PCB_NetsOnly

