

# Ivor Benderavage

SOFTWARE DEVELOPER | PROJECT MANAGER

✉ ivor.benderavage@gmail.com | 🏠 ivorysoap.github.io | 📺 ivorysoap | 🌐 ibenderavage | 📍 Ottawa

## Skills

|                    |   |
|--------------------|---|
| <b>Tools</b>       | Linux, Git, SVN, SQL, ElasticSearch, REST API, Flask, Jekyll, Docker, TravisCI, FPGA, ESP8266, embedded systems |
| <b>Programming</b> | Python, C, C++, Java, VHDL, assembly (various), HTML, CSS, Matlab, LaTeX  |
| <b>Languages</b>   | English, French   |

## Experience

### Faculty of Engineering, University of Ottawa

Ottawa, Ont.

TEACHING ASSISTANT · PROJECT MANAGER

09/2018 - 04/2020

- Managed design projects undertaken by students enrolled in undergraduate engineering design courses.
- Delivered engineering design lab content to students, including labs on Arduino, Matlab, PCB design, soldering, 3D printing, and laser cutting.
- Oversaw students' meetings with clients and graded their progress throughout the term.

### Solace

Kanata, Ont.

SOFTWARE DEVELOPER (INTERN)

05/2019 - 08/2019

- Performed Python and C++ maintenance work on a production-level RESTful API as a component of event broker software.
- Investigated bug reports and tested bug patches on software and hardware event brokers.
- Ensured documentation was properly generated and accurately reflected code structure.
- Ensured continuity of QA tests between releases.

### Solace

Kanata, Ont.

SUPPORT ENGINEER (INTERN)

05/2018 - 08/2018

- Addressed support and enhancement requests from clients.
- Developed bash scripts to streamline the process of handling support requests.
- Assisted clients with technical queries pertaining to the Python, C++, Java, .NET, and NodeJS event broker API offerings.
- Configured and debugged PubSub+ hardware and software event brokers.

## Projects

### Data from Home

Built an IoT mesh network for sensing environmental data in C++ using ESP8266/ESP32 microcontrollers, Raspberry Pi, and various sensors; data stored in SQLite database and served in a Flask web app.

### MIPS in VHDL

Designed a 32-bit MIPS microcontroller in VHDL; design featured a five-stage instruction pipeline, hazard detection, and hazard avoidance, and could run MIPS assembly programs using an FPGA.

## Education

### University of Ottawa

Ottawa, Ont.

B.A.Sc. IN COMPUTER ENGINEERING (BILINGUAL)

09/2015 - 07/2020 (anticipated)

- IEEE Canadian Foundation scholarship (2019)

## Extracurricular Activity

### IEEE uOttawa student branch

Ottawa, Ont.

VP COMMUNICATIONS · DIRECTOR OF McNAUGHTON RESOURCE CENTRE

09/2017 - 04/2019

- Organized and hosted a series of coding interview workshops for software engineering students seeking internships.
- Procured lab equipment (soldering stations, oscilloscopes, computers) for our lab and instructed students on how to use them.

### uOttHack

Ottawa, Ont.

MARKETING COORDINATOR · ADVISOR

04/2017 - 02/2020

- Helped to launch and run uOttHack, the University of Ottawa's first hackathon.
- Liaised with local media outlets, communicated with participants through social media, and assisted with development of the website.