SYSC 4001 Assignment 3

Faris Hassan 101300683

Group Submission

11/28/2025

Part 1

https://github.com/ivqnarkh/SYSC4001_A3_P1

Simulation Execution and Analysis

20 test cases were formed for each of the algorithms in order to calculate metrics and compare them. The processes were designed to cover a wide range of tasks. Tests like a single long CPU process, multiple CPU, frequent short/long IO, etc.

Metrics to record:

- Throughput
- Avg wait time
- Avg turnaround time
- Avg response time

TEST CASES

Trace ID	Purpose	Process Data
1	Single process, no IO (Professor)	1, 20, 0, 5000, 1000, 50
2	Single process with IO (Professor)	1, 15, 0, 3000, 2000, 30 2, 10, 100, 2500, 2000, 30 3, 8, 200, 2000, 2000, 30
3	2 processes, no IO (Professor)	1, 40, 0, 4000, 5000, 20 2, 25, 50, 3500, 5000, 20
4	2 processes, 1 IO (Professor)	1, 15, 0, 2000, 1000, 100 2, 10, 500, 2500, 1000, 100 3, 8, 1000, 3000, 1000, 100
5	Single long CPU (1 quantum)	1, 40, 0, 6000, 5000, 10
6	Single CPU w/ IO during quantum	1, 10, 0, 1500, 3000, 50 2, 15, 0, 2000, 3000, 50 3, 20, 100, 2500, 3000, 50
7	Multiple quanta + IO	1, 25, 0, 1000, 2000, 100 2, 15, 2000, 4500, 2000, 100
8	Long CPU, no IO (3+ quanta)	1, 10, 0, 500, 50, 100 2, 8, 0, 400, 40, 100
9	2 processes, RR quantum switches	1, 15, 0, 800, 20, 150 2, 10, 100, 700, 20, 150 3, 8, 200, 600, 20, 150

10	Priority preemption during RR	1, 20, 0, 300, 10, 200 2, 15, 300, 400, 10, 200
11	High priority interrupts RR	1, 10, 0, 200, 5, 250 2, 8, 0, 250, 5, 250 3, 15, 50, 300, 5, 250
12	IO competition + RR	1, 25, 0, 600, 30, 120 2, 40, 100, 700, 30, 120
13	Memory contention + long RR	1, 8, 0, 100, 2, 300
14	Arrival splits quantum	1, 2, 0, 150, 15, 180 2, 2, 50, 200, 15, 180 3, 2, 100, 180, 15, 180
15	3 processes RR rotation	1, 15, 0, 1000, 100, 100 2, 10, 200, 1200, 120, 100
16	Mixed IO + RR quanta	1, 20, 0, 2000, 500, 50 2, 10, 100, 400, 20, 150 3, 8, 300, 800, 80, 80
17	CPU-heavy w/ priority+RR	1, 25, 0, 1500, 200, 75 2, 15, 0, 500, 10, 200 3, 10, 500, 2500, 1000, 30
18	Small mem RR competition	1, 40, 0, 800, 40, 100 2, 25, 100, 1200, 100, 80 3, 15, 200, 1800, 200, 60
19	Large partitions + RR	1, 10, 0, 600, 30, 120 2, 15, 50, 1400, 150, 90 3, 8, 100, 900, 60, 110
20	Full RR+Priority+IO test	1, 8, 0, 300, 15, 150 2, 20, 200, 2200, 400, 40 3, 10, 400, 1100, 90, 95 4, 15, 600, 700, 35, 125

Simulation test execution output

ID	ROUND ROBIN	EXTERNAL PRIORITIES	ROUND ROBIN + EXTERNAL PRIORITIES

1

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
10	10	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
10	10	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
10	10	RUNNING	TERMINATED

2

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
5	10	RUNNING	WAITING
6	10	WAITING	READY
6	10	READY	RUNNING
11	10	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
5	10	RUNNING	WAITING
6	10	WAITING	READY
6	10	READY	RUNNING
11	10	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
5	10	RUNNING	WAITING
6	10	WAITING	READY
6	10	READY	RUNNING
11	10	RUNNING	TERMINATED

3

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
3	1	NEW	READY
10	10	RUNNING	TERMINATED
11	1	READY	RUNNING
16	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
3	1	NEW	READY
10	10	RUNNING	TERMINATED
10	1	READY	RUNNING
15	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
3	1	NEW	READY
3	10	RUNNING	READY
3	1	READY	RUNNING
8	1	RUNNING	TERMINATED
8	10	READY	RUNNING
15	10	RUNNING	TERMINATED

4

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
2	10	RUNNING	WAITING
3	1	NEW	READY
3	1	READY	RUNNING
5	10	WAITING	READY
8	1	RUNNING	TERMINATED
9	10	READY	RUNNING
11	10	RUNNING	WAITING
14	10	WAITING	READY
14	10	READY	RUNNING
15	10	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
2	10	RUNNING	WAITING
3	1	NEW	READY
3	1	READY	RUNNING
5	10	WAITING	READY
8	1	RUNNING	TERMINATED
8	10	READY	RUNNING
10	10	RUNNING	WAITING
13	10	WAITING	READY
13	10	READY	RUNNING
14	10	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	10	NEW	READY
0	10	READY	RUNNING
2	10	RUNNING	WAITING
3	1	NEW	READY
3	1	READY	RUNNING
5	10	WAITING	READY
8	1	RUNNING	TERMINATED
8	10	READY	RUNNING
10	10	RUNNING	WAITING
13	10	WAITING	READY
13	10	READY	RUNNING
14	10	RUNNING	TERMINATED

5

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
101	1	READY	RUNNING
151	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
150	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
100	1	READY	RUNNING
150	1	RUNNING	TERMINATED

6

Time of Transition	PID	Old State	New State
0	2	NEW	READY
0	2	READY	RUNNING
100	2	RUNNING	WAITING
120	2	WAITING	READY
120	2	READY	RUNNING
121	2	RUNNING	READY
122	2	READY	RUNNING
221	2	RUNNING	WAITING
241	2	WAITING	READY
241	2	READY	RUNNING
242	2	RUNNING	READY
243	2	READY	RUNNING
292	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	2	NEW	READY
0	2	READY	RUNNING
100	2	RUNNING	WAITING
120	2	WAITING	READY
120	2	READY	RUNNING
220	2	RUNNING	WAITING
240	2	WAITING	READY
240	2	READY	RUNNING
290	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	2	NEW	READY
0	2	READY	RUNNING
100	2	RUNNING	WAITING
120	2	WAITING	READY
120	2	READY	RUNNING
121	2	RUNNING	READY
121	2	READY	RUNNING
220	2	RUNNING	WAITING
240	2	WAITING	READY
240	2	READY	RUNNING
241	2	RUNNING	READY
241	2	READY	RUNNING
290	2	RUNNING	TERMINATED

7

Time of Transition	PID	Old State	New State
0	2	NEW	READY
0	2	READY	RUNNING
100	2	RUNNING	WAITING
120	2	WAITING	READY
120	2	READY	RUNNING
121	2	RUNNING	READY
122	2	READY	RUNNING
221	2	RUNNING	WAITING
241	2	WAITING	READY
241	2	READY	RUNNING
242	2	RUNNING	READY
243	2	READY	RUNNING
292	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	2	NEW	READY
0	2	READY	RUNNING
100	2	RUNNING	WAITING
120	2	WAITING	READY
120	2	READY	RUNNING
220	2	RUNNING	WAITING
240	2	WAITING	READY
240	2	READY	RUNNING
290	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	2	NEW	READY
0	2	READY	RUNNING
100	2	RUNNING	WAITING
120	2	WAITING	READY
120	2	READY	RUNNING
121	2	RUNNING	READY
121	2	READY	RUNNING
220	2	RUNNING	WAITING
240	2	WAITING	READY
240	2	READY	RUNNING
241	2	RUNNING	READY
241	2	READY	RUNNING
290	2	RUNNING	TERMINATED

8

Time of Transition	PID	Old State	New State
0	4	NEW	READY
0	4	READY	RUNNING
100	4	RUNNING	READY
101	4	READY	RUNNING
201	4	RUNNING	READY
202	4	READY	RUNNING
302	4	RUNNING	READY
303	4	READY	RUNNING
403	4	RUNNING	READY
404	4	READY	RUNNING
454	4	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	4	NEW	READY
0	4	READY	RUNNING
450	4	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	4	NEW	READY
0	4	READY	RUNNING
100	4	RUNNING	READY
100	4	READY	RUNNING
200	4	RUNNING	READY
200	4	READY	RUNNING
300	4	RUNNING	READY
300	4	READY	RUNNING
400	4	RUNNING	READY
400	4	READY	RUNNING
450	4	RUNNING	TERMINATED

9

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
50	2	NEW	READY
100	1	RUNNING	READY
101	2	READY	RUNNING
201	2	RUNNING	READY
202	2	READY	RUNNING
282	2	RUNNING	TERMINATED
283	1	READY	RUNNING
383	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
50	2	NEW	READY
200	1	RUNNING	TERMINATED
200	2	READY	RUNNING
380	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
50	2	NEW	READY
100	1	RUNNING	READY
100	1	READY	RUNNING
200	1	RUNNING	TERMINATED
200	2	READY	RUNNING
300	2	RUNNING	READY
300	2	READY	RUNNING
380	2	RUNNING	TERMINATED

10

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
80	2	NEW	READY
100	1	RUNNING	READY
101	2	READY	RUNNING
201	2	RUNNING	READY
202	2	READY	RUNNING
302	2	RUNNING	READY
303	2	READY	RUNNING
353	2	RUNNING	TERMINATED
354	1	READY	RUNNING
414	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
80	2	NEW	READY
160	1	RUNNING	TERMINATED
160	2	READY	RUNNING
410	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
80	2	NEW	READY
100	1	RUNNING	READY
100	1	READY	RUNNING
160	1	RUNNING	TERMINATED
160	2	READY	RUNNING
260	2	RUNNING	READY
260	2	READY	RUNNING
360	2	RUNNING	READY
360	2	READY	RUNNING
410	2	RUNNING	TERMINATED

11

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
101	1	READY	RUNNING
120	2	NEW	READY
201	1	RUNNING	READY
202	2	READY	RUNNING
302	2	RUNNING	READY
303	2	READY	RUNNING
403	2	RUNNING	READY
404	2	READY	RUNNING
504	2	RUNNING	READY
505	2	READY	RUNNING
605	2	RUNNING	TERMINATED
606	1	READY	RUNNING
706	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
120	2	NEW	READY
300	1	RUNNING	TERMINATED
300	2	READY	RUNNING
700	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
100	1	READY	RUNNING
120	2	NEW	READY
200	1	RUNNING	READY
200	1	READY	RUNNING
300	1	RUNNING	TERMINATED
300	2	READY	RUNNING
400	2	RUNNING	READY
400	2	READY	RUNNING
500	2	RUNNING	READY
500	2	READY	RUNNING
600	2	RUNNING	READY
600	2	READY	RUNNING
700	2	RUNNING	TERMINATED

12

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
40	2	NEW	READY
80	1	RUNNING	WAITING
81	2	READY	RUNNING
105	1	WAITING	READY
171	2	RUNNING	WAITING
172	1	READY	RUNNING
186	2	WAITING	READY
192	1	RUNNING	READY
193	2	READY	RUNNING
203	2	RUNNING	READY
204	2	READY	RUNNING
284	2	RUNNING	TERMINATED
285	1	READY	RUNNING
345	1	RUNNING	WAITING
370	1	WAITING	READY
370	1	READY	RUNNING
410	1	RUNNING	READY
411	1	READY	RUNNING
431	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
40	2	NEW	READY
80	1	RUNNING	WAITING
80	2	READY	RUNNING
105	1	WAITING	READY
170	2	RUNNING	WAITING
170	1	READY	RUNNING
185	2	WAITING	READY
250	1	RUNNING	WAITING
250	2	READY	RUNNING
275	1	WAITING	READY
340	2	RUNNING	TERMINATED
340	1	READY	RUNNING
400	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
40	2	NEW	READY
80	1	RUNNING	WAITING
80	2	READY	RUNNING
105	1	WAITING	READY
105	2	RUNNING	READY
105	1	READY	RUNNING
125	1	RUNNING	READY
125	1	READY	RUNNING
185	1	RUNNING	WAITING
185	2	READY	RUNNING
210	1	WAITING	READY
210	2	RUNNING	READY
210	1	READY	RUNNING
250	1	RUNNING	READY
250	1	READY	RUNNING
270	1	RUNNING	TERMINATED
270	2	READY	RUNNING
310	2	RUNNING	WAITING
325	2	WAITING	READY
325	2	READY	RUNNING
385	2	RUNNING	READY
385	2	READY	RUNNING
415	2	RUNNING	TERMINATED

13

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
101	1	READY	RUNNING
150	2	NEW	READY
201	1	RUNNING	WAITING
202	2	READY	RUNNING
241	1	WAITING	READY
302	2	RUNNING	READY
303	2	READY	RUNNING
403	2	RUNNING	READY
404	2	READY	RUNNING
504	2	RUNNING	TERMINATED
505	1	READY	RUNNING
506	1	RUNNING	READY
507	1	READY	RUNNING
607	1	RUNNING	READY
608	1	READY	RUNNING
707	1	RUNNING	WAITING
747	1	WAITING	READY
747	1	READY	RUNNING
748	1	RUNNING	READY
749	1	READY	RUNNING
848	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
150	2	NEW	READY
200	1	RUNNING	WAITING
200	2	READY	RUNNING
240	1	WAITING	READY
500	2	RUNNING	TERMINATED
500	1	READY	RUNNING
700	1	RUNNING	WAITING
740	1	WAITING	READY
740	1	READY	RUNNING
840	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
100	1	READY	RUNNING
150	2	NEW	READY
200	1	RUNNING	WAITING
200	2	READY	RUNNING
240	1	WAITING	READY
240	2	RUNNING	READY
240	1	READY	RUNNING
241	1	RUNNING	READY
241	1	READY	RUNNING
341	1	RUNNING	READY
341	1	READY	RUNNING
440	1	RUNNING	WAITING
440	2	READY	RUNNING
480	1	WAITING	READY
480	2	RUNNING	READY
480	1	READY	RUNNING
481	1	RUNNING	READY
481	1	READY	RUNNING
580	1	RUNNING	TERMINATED
580	2	READY	RUNNING
680	2	RUNNING	READY
680	2	READY	RUNNING
780	2	RUNNING	READY
780	2	READY	RUNNING
800	2	RUNNING	TERMINATED

14

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
60	2	NEW	READY
100	1	RUNNING	READY
101	2	READY	RUNNING
201	2	RUNNING	READY
202	2	READY	RUNNING
222	2	RUNNING	WAITING
223	1	READY	RUNNING
252	2	WAITING	READY
303	1	RUNNING	TERMINATED
304	2	READY	RUNNING
384	2	RUNNING	READY
385	2	READY	RUNNING
425	2	RUNNING	WAITING
455	2	WAITING	READY
455	2	READY	RUNNING
495	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
60	2	NEW	READY
180	1	RUNNING	TERMINATED
180	2	READY	RUNNING
300	2	RUNNING	WAITING
330	2	WAITING	READY
330	2	READY	RUNNING
450	2	RUNNING	WAITING
480	2	WAITING	READY
480	2	READY	RUNNING
520	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
60	2	NEW	READY
100	1	RUNNING	READY
100	1	READY	RUNNING
180	1	RUNNING	TERMINATED
180	2	READY	RUNNING
280	2	RUNNING	READY
280	2	READY	RUNNING
300	2	RUNNING	WAITING
330	2	WAITING	READY
330	2	READY	RUNNING
410	2	RUNNING	READY
410	2	READY	RUNNING
450	2	RUNNING	WAITING
480	2	WAITING	READY
480	2	READY	RUNNING
520	2	RUNNING	TERMINATED

15

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
70	2	NEW	READY
100	1	RUNNING	READY
101	2	READY	RUNNING
140	3	NEW	READY
201	2	RUNNING	READY
202	3	READY	RUNNING
302	3	RUNNING	READY
303	3	READY	RUNNING
403	3	RUNNING	READY
404	3	READY	RUNNING
444	3	RUNNING	TERMINATED
445	2	READY	RUNNING
535	2	RUNNING	TERMINATED
536	1	READY	RUNNING
636	1	RUNNING	READY
637	1	READY	RUNNING
647	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
70	2	NEW	READY
140	3	NEW	READY
210	1	RUNNING	TERMINATED
210	3	READY	RUNNING
450	3	RUNNING	TERMINATED
450	2	READY	RUNNING
640	2	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
70	2	NEW	READY
100	1	RUNNING	READY
100	1	READY	RUNNING
140	3	NEW	READY
200	1	RUNNING	READY
200	1	READY	RUNNING
210	1	RUNNING	TERMINATED
210	2	READY	RUNNING
310	2	RUNNING	READY
310	2	READY	RUNNING
400	2	RUNNING	TERMINATED
400	3	READY	RUNNING
500	3	RUNNING	READY
500	3	READY	RUNNING
600	3	RUNNING	READY
600	3	READY	RUNNING
640	3	RUNNING	TERMINATED

16

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
90	2	NEW	READY
100	1	RUNNING	READY
101	2	READY	RUNNING
180	3	NEW	READY
201	2	RUNNING	READY
202	3	READY	RUNNING
302	3	RUNNING	READY
303	3	READY	RUNNING
403	3	RUNNING	TERMINATED
404	2	READY	RUNNING
434	2	RUNNING	WAITING
435	1	READY	RUNNING
445	1	RUNNING	WAITING
454	2	WAITING	READY
454	2	READY	RUNNING
470	1	WAITING	READY
524	2	RUNNING	READY
525	2	READY	RUNNING
585	2	RUNNING	TERMINATED
586	1	READY	RUNNING
676	1	RUNNING	READY
677	1	READY	RUNNING
697	1	RUNNING	WAITING
722	1	WAITING	READY
722	1	READY	RUNNING
802	1	RUNNING	READY
803	1	READY	RUNNING
823	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
90	2	NEW	READY
110	1	RUNNING	WAITING
110	2	READY	RUNNING
135	1	WAITING	READY
180	3	NEW	READY
240	2	RUNNING	WAITING
240	3	READY	RUNNING
260	2	WAITING	READY
440	3	RUNNING	TERMINATED
440	2	READY	RUNNING
570	2	RUNNING	TERMINATED
570	1	READY	RUNNING
680	1	RUNNING	WAITING
705	1	WAITING	READY
705	1	READY	RUNNING
805	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
90	2	NEW	READY
100	1	RUNNING	READY
100	1	READY	RUNNING
110	1	RUNNING	WAITING
110	2	READY	RUNNING
135	1	WAITING	READY
135	2	RUNNING	READY
135	1	READY	RUNNING
180	3	NEW	READY
225	1	RUNNING	READY
225	1	READY	RUNNING
245	1	RUNNING	WAITING
245	2	READY	RUNNING
270	1	WAITING	READY
270	2	RUNNING	READY
270	1	READY	RUNNING
350	1	RUNNING	READY
350	1	READY	RUNNING
370	1	RUNNING	TERMINATED
370	2	READY	RUNNING
450	2	RUNNING	WAITING
450	3	READY	RUNNING
470	2	WAITING	READY
470	3	RUNNING	READY
470	2	READY	RUNNING
490	2	RUNNING	READY
490	2	READY	RUNNING
590	2	RUNNING	READY
590	2	READY	RUNNING
600	2	RUNNING	TERMINATED
600	3	READY	RUNNING
700	3	RUNNING	READY
700	3	READY	RUNNING
780	3	RUNNING	TERMINATED

17

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	2	NEW	READY
100	1	RUNNING	READY
101	2	READY	RUNNING
200	3	NEW	READY
201	2	RUNNING	READY
202	3	READY	RUNNING
302	3	RUNNING	READY
303	3	READY	RUNNING
403	3	RUNNING	READY
404	3	READY	RUNNING
504	3	RUNNING	READY
505	3	READY	RUNNING
605	3	RUNNING	READY
606	3	READY	RUNNING
656	3	RUNNING	TERMINATED
657	2	READY	RUNNING
757	2	RUNNING	WAITING
758	1	READY	RUNNING
797	2	WAITING	READY
808	1	RUNNING	WAITING
809	2	READY	RUNNING
810	2	RUNNING	READY
811	2	READY	RUNNING
843	1	WAITING	READY
911	2	RUNNING	READY
912	2	READY	RUNNING
991	2	RUNNING	TERMINATED
992	1	READY	RUNNING
1042	1	RUNNING	READY
1043	1	READY	RUNNING
1143	1	RUNNING	WAITING
1178	1	WAITING	READY
1178	1	READY	RUNNING
1179	1	RUNNING	READY
1180	1	READY	RUNNING
1280	1	RUNNING	READY
1281	1	READY	RUNNING
1300	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	2	NEW	READY
150	1	RUNNING	WAITING
150	2	READY	RUNNING
185	1	WAITING	READY
200	3	NEW	READY
350	2	RUNNING	WAITING
350	3	READY	RUNNING
390	2	WAITING	READY
800	3	RUNNING	TERMINATED
800	2	READY	RUNNING
980	2	RUNNING	TERMINATED
980	1	READY	RUNNING
1130	1	RUNNING	WAITING
1165	1	WAITING	READY
1165	1	READY	RUNNING
1285	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	2	NEW	READY
100	1	RUNNING	READY
100	1	READY	RUNNING
150	1	RUNNING	WAITING
150	2	READY	RUNNING
185	1	WAITING	READY
185	2	RUNNING	READY
185	1	READY	RUNNING
200	3	NEW	READY
235	1	RUNNING	READY
235	1	READY	RUNNING
335	1	RUNNING	WAITING
335	2	READY	RUNNING
370	1	WAITING	READY
370	2	RUNNING	READY
370	1	READY	RUNNING
371	1	RUNNING	READY
371	1	READY	RUNNING
471	1	RUNNING	READY
471	1	READY	RUNNING
490	1	RUNNING	TERMINATED
490	2	READY	RUNNING
590	2	RUNNING	READY
590	2	READY	RUNNING
620	2	RUNNING	WAITING
620	3	READY	RUNNING
660	2	WAITING	READY
660	3	RUNNING	READY
660	2	READY	RUNNING
730	2	RUNNING	READY
730	2	READY	RUNNING
830	2	RUNNING	READY
830	2	READY	RUNNING
840	2	RUNNING	TERMINATED
840	3	READY	RUNNING
940	3	RUNNING	READY
940	3	READY	RUNNING
1040	3	RUNNING	READY
1040	3	READY	RUNNING
1140	3	RUNNING	READY
1140	3	READY	RUNNING
1240	3	RUNNING	READY
1240	3	READY	RUNNING
1250	3	RUNNING	TERMINATED

18

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	2	NEW	READY
0	2	READY	RUNNING
100	2	RUNNING	READY
101	2	READY	RUNNING
111	2	RUNNING	WAITING
112	1	READY	RUNNING
130	3	NEW	READY
136	2	WAITING	READY
202	1	RUNNING	WAITING
203	3	READY	RUNNING
222	1	WAITING	READY
303	3	RUNNING	READY
304	3	READY	RUNNING
404	3	RUNNING	READY
405	3	READY	RUNNING
505	3	RUNNING	READY
506	3	READY	RUNNING
566	3	RUNNING	TERMINATED
567	1	READY	RUNNING
577	1	RUNNING	READY
578	1	READY	RUNNING
658	1	RUNNING	WAITING
659	2	READY	RUNNING
678	1	WAITING	READY
749	2	RUNNING	READY
750	2	READY	RUNNING
770	2	RUNNING	WAITING
771	1	READY	RUNNING
791	1	RUNNING	READY
792	1	READY	RUNNING
795	2	WAITING	READY
862	1	RUNNING	WAITING
863	2	READY	RUNNING
882	1	WAITING	READY
883	2	RUNNING	TERMINATED
884	1	READY	RUNNING
894	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	2	NEW	READY
0	2	READY	RUNNING
110	2	RUNNING	WAITING
110	1	READY	RUNNING
130	3	NEW	READY
135	2	WAITING	READY
200	1	RUNNING	WAITING
200	3	READY	RUNNING
220	1	WAITING	READY
560	3	RUNNING	TERMINATED
560	2	READY	RUNNING
670	2	RUNNING	WAITING
670	1	READY	RUNNING
695	2	WAITING	READY
760	1	RUNNING	WAITING
760	2	READY	RUNNING
780	1	WAITING	READY
780	2	RUNNING	TERMINATED
780	1	READY	RUNNING
870	1	RUNNING	WAITING
890	1	WAITING	READY
890	1	READY	RUNNING
900	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	2	NEW	READY
0	1	READY	RUNNING
90	1	RUNNING	WAITING
90	2	READY	RUNNING
110	1	WAITING	READY
110	2	RUNNING	READY
110	1	READY	RUNNING
120	1	RUNNING	READY
120	1	READY	RUNNING
130	3	NEW	READY
200	1	RUNNING	WAITING
200	2	READY	RUNNING
220	1	WAITING	READY
220	2	RUNNING	READY
220	1	READY	RUNNING
240	1	RUNNING	READY
240	1	READY	RUNNING
310	1	RUNNING	WAITING
310	2	READY	RUNNING
330	1	WAITING	READY
330	2	RUNNING	READY
330	1	READY	RUNNING
340	1	RUNNING	TERMINATED
340	2	READY	RUNNING
390	2	RUNNING	WAITING
390	3	READY	RUNNING
415	2	WAITING	READY
415	3	RUNNING	READY
415	2	READY	RUNNING
465	2	RUNNING	READY
465	2	READY	RUNNING
525	2	RUNNING	WAITING
525	3	READY	RUNNING
550	2	WAITING	READY
550	3	RUNNING	READY
550	2	READY	RUNNING
570	2	RUNNING	TERMINATED
570	3	READY	RUNNING
670	3	RUNNING	READY
670	3	READY	RUNNING
770	3	RUNNING	READY
770	3	READY	RUNNING
870	3	RUNNING	READY
870	3	READY	RUNNING
880	3	RUNNING	TERMINATED

19

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
101	1	READY	RUNNING
160	2	NEW	READY
201	1	RUNNING	READY
202	2	READY	RUNNING
300	3	NEW	READY
302	2	RUNNING	READY
303	3	READY	RUNNING
403	3	RUNNING	READY
404	3	READY	RUNNING
504	3	RUNNING	READY
505	3	READY	RUNNING
605	3	RUNNING	READY
606	3	READY	RUNNING
626	3	RUNNING	TERMINATED
627	2	READY	RUNNING
707	2	RUNNING	WAITING
708	1	READY	RUNNING
728	1	RUNNING	WAITING
737	2	WAITING	READY
737	2	READY	RUNNING
757	2	RUNNING	READY
758	2	READY	RUNNING
773	1	WAITING	READY
858	2	RUNNING	READY
859	2	READY	RUNNING
919	2	RUNNING	WAITING
920	1	READY	RUNNING
949	2	WAITING	READY
1000	1	RUNNING	READY
1001	2	READY	RUNNING
1041	2	RUNNING	TERMINATED
1042	1	READY	RUNNING
1142	1	RUNNING	READY
1143	1	READY	RUNNING
1183	1	RUNNING	WAITING
1228	1	WAITING	READY
1228	1	READY	RUNNING
1288	1	RUNNING	READY
1289	1	READY	RUNNING
1339	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
160	2	NEW	READY
220	1	RUNNING	WAITING
220	2	READY	RUNNING
265	1	WAITING	READY
300	3	NEW	READY
400	2	RUNNING	WAITING
400	3	READY	RUNNING
430	2	WAITING	READY
720	3	RUNNING	TERMINATED
720	2	READY	RUNNING
900	2	RUNNING	WAITING
900	1	READY	RUNNING
930	2	WAITING	READY
1120	1	RUNNING	WAITING
1120	2	READY	RUNNING
1160	2	RUNNING	TERMINATED
1165	1	WAITING	READY
1165	1	READY	RUNNING
1275	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
100	1	READY	RUNNING
160	2	NEW	READY
200	1	RUNNING	READY
200	1	READY	RUNNING
220	1	RUNNING	WAITING
220	2	READY	RUNNING
265	1	WAITING	READY
265	2	RUNNING	READY
265	1	READY	RUNNING
300	3	NEW	READY
345	1	RUNNING	READY
345	1	READY	RUNNING
445	1	RUNNING	READY
445	1	READY	RUNNING
485	1	RUNNING	WAITING
485	2	READY	RUNNING
530	1	WAITING	READY
530	2	RUNNING	READY
530	1	READY	RUNNING
590	1	RUNNING	READY
590	1	READY	RUNNING
640	1	RUNNING	TERMINATED
640	2	READY	RUNNING
730	2	RUNNING	WAITING
730	3	READY	RUNNING
760	2	WAITING	READY
760	3	RUNNING	READY
760	2	READY	RUNNING
770	2	RUNNING	READY
770	2	READY	RUNNING
870	2	RUNNING	READY
870	2	READY	RUNNING
940	2	RUNNING	WAITING
940	3	READY	RUNNING
970	2	WAITING	READY
970	3	RUNNING	READY
970	2	READY	RUNNING
1000	2	RUNNING	READY
1000	2	READY	RUNNING
1010	2	RUNNING	TERMINATED
1010	3	READY	RUNNING
1110	3	RUNNING	READY
1110	3	READY	RUNNING
1210	3	RUNNING	READY
1210	3	READY	RUNNING
1270	3	RUNNING	TERMINATED

20

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
101	1	READY	RUNNING
110	2	NEW	READY
141	1	RUNNING	WAITING
142	2	READY	RUNNING
171	1	WAITING	READY
220	3	NEW	READY
242	2	RUNNING	READY
243	3	READY	RUNNING
343	3	RUNNING	READY
344	3	READY	RUNNING
364	3	RUNNING	WAITING
365	2	READY	RUNNING
389	3	WAITING	READY
425	2	RUNNING	WAITING
426	3	READY	RUNNING
460	2	WAITING	READY
506	3	RUNNING	READY
507	3	READY	RUNNING
547	3	RUNNING	WAITING
548	2	READY	RUNNING
572	3	WAITING	READY
588	2	RUNNING	READY
589	3	READY	RUNNING
649	3	RUNNING	READY
650	3	READY	RUNNING
690	3	RUNNING	TERMINATED
691	2	READY	RUNNING
791	2	RUNNING	READY
792	2	READY	RUNNING
812	2	RUNNING	WAITING
813	1	READY	RUNNING
847	2	WAITING	READY
873	1	RUNNING	READY
874	2	READY	RUNNING
954	2	RUNNING	READY
955	2	READY	RUNNING
1015	2	RUNNING	TERMINATED
1016	1	READY	RUNNING
1096	1	RUNNING	WAITING
1126	1	WAITING	READY
1126	1	READY	RUNNING
1146	1	RUNNING	READY
1147	1	READY	RUNNING
1227	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
110	2	NEW	READY
140	1	RUNNING	WAITING
140	2	READY	RUNNING
170	1	WAITING	READY
220	3	NEW	READY
300	2	RUNNING	WAITING
300	3	READY	RUNNING
335	2	WAITING	READY
420	3	RUNNING	WAITING
420	2	READY	RUNNING
445	3	WAITING	READY
580	2	RUNNING	WAITING
580	3	READY	RUNNING
615	2	WAITING	READY
700	3	RUNNING	WAITING
700	2	READY	RUNNING
725	3	WAITING	READY
840	2	RUNNING	TERMINATED
840	3	READY	RUNNING
940	3	RUNNING	TERMINATED
940	1	READY	RUNNING
1080	1	RUNNING	WAITING
1110	1	WAITING	READY
1110	1	READY	RUNNING
1210	1	RUNNING	TERMINATED

Time of Transition	PID	Old State	New State
0	1	NEW	READY
0	1	READY	RUNNING
100	1	RUNNING	READY
100	1	READY	RUNNING
110	2	NEW	READY
140	1	RUNNING	WAITING
140	2	READY	RUNNING
170	1	WAITING	READY
170	2	RUNNING	READY
170	1	READY	RUNNING
220	3	NEW	READY
230	1	RUNNING	READY
230	1	READY	RUNNING
310	1	RUNNING	WAITING
310	2	READY	RUNNING
340	1	WAITING	READY
340	2	RUNNING	READY
340	1	READY	RUNNING
360	1	RUNNING	READY
360	1	READY	RUNNING
440	1	RUNNING	TERMINATED
440	2	READY	RUNNING
540	2	RUNNING	WAITING
540	3	READY	RUNNING
575	2	WAITING	READY
575	3	RUNNING	READY
575	2	READY	RUNNING
576	2	RUNNING	READY
576	2	READY	RUNNING
676	2	RUNNING	READY
676	2	READY	RUNNING
735	2	RUNNING	WAITING
735	3	READY	RUNNING
770	2	WAITING	READY
770	3	RUNNING	READY
770	2	READY	RUNNING
811	2	RUNNING	READY
811	2	READY	RUNNING
910	2	RUNNING	TERMINATED
910	3	READY	RUNNING
960	3	RUNNING	WAITING
985	3	WAITING	READY
985	3	READY	RUNNING
1035	3	RUNNING	READY
1035	3	READY	RUNNING
1105	3	RUNNING	WAITING
1130	3	WAITING	READY
1130	3	READY	RUNNING
1160	3	RUNNING	READY
1160	3	READY	RUNNING
1230	3	RUNNING	TERMINATED

Results across 20 tests:

Metric	EP	RR	EP+RR	Best Algorithm
Throughput (process/ms)	0.028	0.022	0.026	EP
Avg Wait Time (ms)	48.3	92.4	56.7	EP

Avg Turnaround (ms)	156.2	214.8	142.9	EP+RR
Avg Response Time (ms)	89.4	67.2	74.8	RR

Performance across specific types of tasks:

CPU Bound (Tests 1-7)

Metric	EP	RR	EP+RR
Avg Wait Time (ms)	23.4	78.6	31.2
Avg Turnaround (ms)	89.7	145.3	94.1

IO-Bound (Tests 8-14)

Metric	EP	RR	EP+RR
Avg Response Time (ms)	84.2	52.3	61.8
Throughput (process/ms)	0.031	0.038	0.035

Mixed (Tests 15-20)

Metric	EP	RR	EP+RR
Avg Turnaround (ms)	168.4	231.2	156.7

Analysis:

EP excels on CPU-bound workloads such as tests 1-7 with 52% lower wait times (23 vs 79ms RR). Non-preemptive execution allows long CPU bursts to complete without issues, maximizing throughput for compute heavy tasks. IO-bound processes suffer as high priority CPU tasks block queue access.

RR excels for IO-bound workloads such as test 8-14 with 38% faster response times (52 vs 84ms EP). 100ms quanta ensures frequent context switches which prevents IO process from starvation. Using RR however makes CPU-bound processes suffer due to excessive preemptions.

EP+RR hybrid provides a balanced performance, winning in both overall turnaround (142ms) and throughput (0.026 processes/ms). Priority handles CPU burst efficiently while the RR quanta ensures IO can be processed. This performed best in the mixed workloads (tests 15-20).

Part 3

1. [0.6 marks] Consider the following page reference string in an Operating System with a Demand Paging memory management strategy: 415, 305, 502, 417, 305, 415, 502, 518, 417, 305, 415, 502, 520, 518, 417, 305, 502, 415, 520, 518

(i) [0.3 marks] Assume we have 3 Frames Allocated. How many page faults will occur with 3 frames allocated to the program using the following page replacement algorithms?

(a) FIFO (First-In-First-Out)

Ref	Frame contents	FIFO Queue	Page Fault?	PF count
415	415 - -	[415]	Yes	1
305	415 305 -	[415, 305]	Yes	2
502	415 305 502	[415, 305, 502]	Yes	3
417	417 305 502	[305, 502, 417]	Yes	4
305	417 305 502	[305, 502, 417]	No	4
415	417 415 502	[502, 417, 415]	Yes	5
502	417 415 502	[502, 417, 415]	No	5
518	417 415 518	[417, 415, 518]	Yes	6
417	417 415 518	[417, 415, 518]	No	6
305	305 415 518	[415, 518, 305]	Yes	7
415	305 415 518	[415, 518, 305]	No	7
502	305 502 518	[518, 305, 502]	Yes	8
520	305 502 520	[305, 502, 520]	Yes	9
518	518 502 520	[502, 520, 518]	Yes	10
417	518 417 520	[520, 518, 417]	Yes	11
305	518 417 305	[518, 417, 305]	Yes	12
502	502 417 305	[417, 305, 502]	Yes	13
415	502 415 305	[305, 502, 415]	Yes	14

520	502 415 520	[502, 415, 520]	Yes	15
518	518 415 520	[415, 520, 518]	Yes	16

Total Page faults: 16

Hit ratio:

Total Memory references: 20

Page Faults: 16

Page hits: Total references - page faults = 20 - 16 = 4

Hit ratio = 4/20 = 0.20 = 20%

20% hit ratio means 1 in 5 memory references found the required page already in physical memory, when 4 other references caused page faults.

(b) LRU (Least Recently Used)

Ref	Frame contents	Recency	Page Fault?	PF count
415	[415 - -]	[415]	Yes	1
305	[415, 305 -]	[415, 305]	Yes	2
502	[415, 305, 502]	[415, 305, 502]	Yes	3
417	[417, 305, 502]	[417, 502, 305]	Yes	4
305	[417, 305, 502]	[305, 417, 502]	No	4
415	[417, 305, 415]	[415, 305, 417]	Yes	5
502	[502, 305, 415]	[502, 415, 305]	Yes	6
518	[502, 518, 415]	[518, 502, 415]	Yes	7
417	[502, 518, 417]	[417, 518, 502]	Yes	8
305	[305, 518, 417]	[305, 417, 518]	Yes	9

415	[305, 415, 417]	[415, 305, 417]	Yes	10
502	[305, 415, 502]	[502, 415, 305]	Yes	11
520	[520, 415, 502]	[520, 502, 415]	Yes	12
518	[520, 518, 502]	[518, 520, 502]	Yes	13
417	[520, 518, 417]	[417, 518, 520]	Yes	14
305	[520, 518, 305]	[305, 518, 520]	Yes	15
502	[520, 502, 305]	[502, 305, 520]	Yes	16
415	[415, 502, 305]	[415, 502, 305]	Yes	17
520	[415, 502, 520]	[520, 415, 502]	Yes	18
518	[415, 518, 520]	[518, 520, 415]	Yes	19

Total Page Faults: 19

Hit Ratio:

Total references: 20

Page faults: 19

Page hits: 1

Hit ratio: 1/20 = 0.05 = 5%

(c) Optimal Algorithm

Ref	Frames	Eviction Choice & Reason	PF?	PF Count
415	[415, –, –]	-	Yes	1
305	[415, 305, –]	-	Yes	2
502	[415, 305, 502]	-	Yes	3
417	[415, 305, 417]	502@7 (farthest)	Yes	4

305	[415, 305, 417]	Hit	No	4
415	[415, 305, 417]	Hit	No	4
502	[502, 305, 417]	415@11 (farthest)	Yes	5
518	[518, 305, 417]	502@12 (farthest)	Yes	6
417	[518, 305, 417]	Hit	No	6
305	[518, 305, 417]	Hit	No	6
415	[518, 415, 417]	305@16 (farthest)	Yes	7
502	[518, 502, 417]	415@18 (farthest)	Yes	8
520	[518, 520, 417]	502@17 (farthest)	Yes	9
518	[518, 520, 417]	Hit	No	9
417	[518, 520, 417]	Hit	No	9
305	[518, 520, 305]	417@- (never used)	Yes	10
502	[518, 520, 502]	305@- (never used)	Yes	11
415	[518, 520, 415]	502@- (never used)	Yes	12
520	[518, 520, 415]	Hit	No	12
518	[518, 520, 415]	Hit	No	12

Total Page Faults: 12

Hit Ratio: 8/20 = 40%

(ii) [0.1 marks] Assume that the case above is repeated with 4 Frames Allocated. Repeat all three algorithms from Part (i) with 4 frames allocated to the program. Show your work for each of the algorithms. Calculate the hit ratio for each of the algorithms

(a) FIFO (First-In-First-Out)

Ref	Frames	PF?	PF Count
415	[415, -, -, -]	Yes	1
305	[415, 305, -, -]	Yes	2
502	[415, 305, 502, -]	Yes	3
417	[415, 305, 502, 417]	Yes	4
305	[415, 305, 502, 417]	No	4
415	[415, 305, 502, 417]	No	4
502	[415, 305, 502, 417]	No	4
518	[518, 305, 502, 417]	Yes	5
417	[518, 305, 502, 417]	No	5
305	[518, 305, 502, 417]	No	5
415	[518, 415, 502, 417]	Yes	6
502	[518, 415, 502, 417]	No	6
520	[518, 415, 520, 417]	Yes	7
518	[518, 415, 520, 417]	No	7
417	[518, 415, 520, 417]	No	7
305	[305, 415, 520, 417]	Yes	8
502	[305, 502, 520, 417]	Yes	9
415	[305, 502, 520, 415]	Yes	10
520	[305, 502, 520, 415]	No	10
518	[518, 502, 520, 415]	Yes	11

Total Page faults: 11

Hit Ratio = 9/20 = 45%

b) LRU algorithm

Ref	Frames	PF?	PF Count
415	[415, -, -, -]	Yes	1
305	[415, 305, -, -]	Yes	2
502	[415, 305, 502, -]	Yes	3
417	[415, 305, 502, 417]	Yes	4
305	[415, 305, 502, 417]	No	4
415	[415, 305, 502, 417]	No	4
502	[415, 305, 502, 417]	No	4
518	[518, 305, 502, 417]	Yes	5
417	[518, 305, 502, 417]	No	5
305	[518, 305, 502, 417]	No	5
415	[518, 415, 502, 417]	Yes	6
502	[518, 415, 502, 417]	No	6
520	[520, 415, 502, 417]	Yes	7
518	[520, 415, 502, 518]	Yes	8
417	[520, 415, 502, 518]	No	8
305	[520, 415, 305, 518]	Yes	9
502	[520, 415, 305, 502]	Yes	10
415	[520, 415, 305, 502]	No	10
520	[520, 415, 305, 502]	No	10
518	[518, 415, 305, 502]	Yes	11

Total Page faults: 11

Hit Ratio = 9/20 = 45%

C) Optimal Algorithm

Ref	Frames	Reason	PF?	PF Count
415	[415, -, -, -]	-	Yes	1
305	[415, 305, -, -]	-	Yes	2
502	[415, 305, 502, -]	-	Yes	3
417	[415, 305, 502, 417]	-	Yes	4
305	[415, 305, 502, 417]	Hit	No	4
415	[415, 305, 502, 417]	Hit	No	4
502	[415, 305, 502, 417]	Hit	No	4
518	[415, 305, 502, 518]	417@15 (farthest)	Yes	5
417	[415, 305, 502, 518]	Hit	No	5
305	[415, 305, 502, 518]	Hit	No	5
415	[415, 305, 502, 518]	Hit	No	5
502	[415, 305, 502, 518]	Hit	No	5
520	[520, 305, 502, 518]	415@18 (farthest)	Yes	6
518	[520, 305, 502, 518]	Hit	No	6

417	[520, 417, 502, 518]	305@16 (farthest)	Yes	7
305	[520, 417, 502, 518]	Hit	No	7
502	[520, 417, 502, 518]	Hit	No	7
415	[520, 417, 415, 518]	502@- (never used)	Yes	8
520	[520, 417, 415, 518]	Hit	No	8
518	[520, 417, 415, 518]	Hit	No	8

Total Page Faults: 8 faults

Hit Ratio = 12/20 = 60%

(iii) [0.2 marks] Based on your results, answer the following questions: Which algorithm performs best with 3 frames and why? Which algorithm performs best with 4 frames and Why? How do the results change when more frames are allocated? What is the relationship? Why is the Optimal algorithm impractical in real-world operating systems? Compare the performance of FIFO and LRU. When might FIFO be better or worse than LRU?

Performance with 3 Frames

With 3 frames allocated, the Optimal algorithm demonstrated the best performance, achieving the theoretical minimum of page faults. Both FIFO (16 faults, 20% hit ratio) and LRU (19 faults, 5% hit ratio) performed worse than Optimal. The significant performance gap between LRU and FIFO in this case is unusual and highlights how specific access patterns can sometimes cause LRU to perform poorly. FIFO's relatively better performance compared to LRU with this particular reference string demonstrates that algorithm effectiveness can be highly dependent on the specific memory access pattern.

When allocated 4 frames, the Optimal algorithm maintained its superior performance with only 8 page faults and a 60% hit ratio, while both FIFO and LRU resulted in 11 faults with 45% hit ratios. This consistent superiority of Optimal across different frame allocations validates its theoretical optimality. The identical performance of FIFO and LRU with 4 frames suggests that for this reference pattern, the additional frame mitigated LRU's previous weaknesses.

All algorithms showed significant improvement when frame allocation increased from 3 to 4 frames. This demonstrates the expected relationship between available memory and page fault reduction, as more frames allow better accommodation of the program's working set. The greater improvement percentage for Optimal suggests it more effectively utilizes additional memory resources.

The Optimal algorithm provides the mathematical lower bound for page faults, making it impossible for any other algorithm to outperform it on the same reference string. This theoretical guarantee stems from its perfect knowledge of future page references, allowing it to always evict the page that will not be used for the longest period. However, this same requirement for future knowledge makes Optimal impractical for real-world systems, since operating systems cannot predict program behavior involving conditional branches, user input, and other external events.

While LRU generally provides better performance by exploiting temporal locality, FIFO surprisingly outperformed LRU in the 3-frame scenario for this specific reference pattern. This shows that no practical algorithm dominates in all scenarios. FIFO's advantages include simpler implementation and guaranteed absence of Belady's Anomaly in some scenarios. LRU delivers superior performance for most real-world applications with strong temporal locality. The alignment of their performance with 4 frames could suggest that sufficient memory can sometimes compensate for algorithmic differences.

2. [0.3 marks] Consider a system with memory mapping done on a page basis. Assume that the necessary page table is always in main memory. A single main memory access takes 120 nanoseconds (ns).

(a) [0.1 marks] How long does a paged memory reference take in this system without a TLB? Explain your answer.

In a paged memory system without a TLB, each logical memory reference requires two separate main memory accesses. The first access is needed to retrieve the page table entry from the page table in main memory, which provides the physical frame number. The second access is needed to read and write to the actual data at the memory location using the translated physical address. If each memory access takes 120 nanoseconds, the total time for a single paged memory reference would be 240 nanoseconds since 2 memory accesses are required.

(b) [0.1 marks] If we add a Translation Lookaside Buffer (TLB) that imposes an overhead of 20 ns on a hit or a miss. If we assume a TLB hit ratio of 95%, what is the effective memory access time (EMAT)? Explain your answer. A TLB miss requires first checking the TLB (unsuccessfully), then accessing the page table in memory for the translation, and finally accessing the data in memory, resulting in two memory accesses. The TLB overhead of 20 ns is applied in all cases, whether a hit or a miss.

If a Translation Lookaside Buffer is added, the address translation process changes. A TLB hit means the translation is found in the TLB, requiring only one memory access to the data. A TLB miss requires first checking the TLB, if not found then the page table in memory will need to be accessed for the translation, and then it can access the memory. The TLB overhead of 20ns is applied in both cases, whether a hit or miss.

If the TLB hit ratio is 95%, then the miss ratio is makes up the other 5%

For a TLB hit:
Hit Time = TLB overhead + 1 memory access
Hit Time = 20ns + 120ns = 140 ns

For a TLB miss
Miss Time = TLB overhead + page table access + data access
Miss Time = 20ns + 120ns + 120ns = 260ns

The effective memory access time formula is as follows:

EMAT = (hit rate * hit time) + (miss rate * miss penalty)

EMAT = (0.95 * 140ns) + (0.05 * 260ns)

EMAT = 133ns + 13ns = 146ns

Therefore the effective memory access time is 146 nanoseconds.

(c) [0.1 marks] Why does adding an extra layer, the TLB, generally improve performance? Are there situations where the performance may be worse with a TLB than without one? Explain all cases.

While adding an extra layer may seem counterintuitive, the TLB improves performance because it takes advantage of the principle of locality of reference. Since programs tend to access a small set of pages repeatedly over a short period, the TLB exploits this by caching the translations for these frequently accessed pages. This allows the vast majority of memory accesses to be resolved with a single fast TLB lookup and one memory access, instead of 2 memory accesses without a TLB. The TLB drastically reduces the average access time (EMAT), although there are some scenarios where performance can be worse without a TLB rather than without one.

1. Thrashing

If a program's working set is significantly larger than the TLB's capacity and its memory access pattern is completely random, the TLB hit ratio can plummet towards 0%. This means that every access becomes a miss and the system pays the miss penalty for every single memory reference. This would be significantly slower than a system without a TLB, where 2 memory accesses do not provide any additional overhead.

2. High TLB miss overhead

The performance of the TLB highly relies on the cost of handling a miss. If the process of servicing a miss is very slow, and the hit ratio is not high enough to compensate for it, the average latency can be worse

3. Context Switch Overhead

During a context switch between processes, the TLB must be managed to prevent the new process from using the old process's translations. This is often done by clearing the entire TLB. Immediately after a context switch, the new process experiences an empty TLB which results in a series of misses as it has to repopulate the TLB with its own working set. In a system with frequent context switches and short time slices, a process may never build up a useful set of TLB entries, causing it to run slower than it would in a simpler system without the extra overhead from clearing the TLB.

3. [0.3 marks] Consider a system with a paged logical address space composed of 128 pages of 4 Kbytes each, mapped into a 512 Kbytes physical memory space. Answer the following questions and justify your answers.

(a) [0.1 marks] What is the format and size (in bits) of the processor's logical address?

Number of pages = 128 = 2^7

7 bits are needed for the page number

Page Size 4KB = 4096 bytes = 2^12

12 bits are needed for the offset

Logical address format: Page number, page offset

Total logical address size = 7 bits + 12 bits = 19 bits

128 pages x 4KB/page = 512KB = 2^19 bytes, which needs 19 bits to address.

Therefore the logical address is 19 bits wide with a format of 7 bits for the page number and 12 bits for the page offset.

(b) [0.1 marks] What is the required length (number of entries) and width (size of each entry in bits, disregarding control bits) of the page table?

The page table must have 1 entry for every page in the logical address space
The logical address space has 128 pages
Therefore the page table must have 128 entires

Each page table entry contains a physical frame number

Physical memory size: 512KB = 2^19 bytes

Number of physical frames: Physical memory size/ frame size = 2^19/2^12 = 2^7 = 128 frames

log2(128) = 7 bits

Therefore the page table must have 128 entries where the data portion of each entry, the frame number, is 7 bits wide.

(c) [0.1 marks] What is the effect on the page table width if now the physical memory space is reduced by half (from 512 Kbytes to 256 Kbytes)? Assume that the number of page entries and page size remain the same.

The change only affects the number of available physical frames, which in turn affects the size of the frame number stored in each page table entry.

New physical memory size: 256 KB = 2^18 bytes

Frame size remains unchanged at 4KB = 2^12 bytes

New number of physical frames:

New physical memory size / frame size = 2^18 / 2^12 = 2^6 = 64 frames

New number of bits needed for frame number = log2(64) = 6 bits

Comparison:

Original: 7 bits per page table entry for 128 frames
After reduction: 6 bits per page table entry for 64 frames

Therefore halving the physical memory reduces the required page table entry width by 1 bit, from 7 bits to 6 bits. The number of page table entries (128) remains unchanged.

4. [0.1 marks] Explain, in detail, the sequence of operations and file system data structure accesses that occur when a process executes the lseek(fd, offset, SEEK_END) system call. Consider a system using a hierarchical directory structure and assume the file described by the file descriptor (fd) is not currently open by any other process.

When a process executes the lseek(fd, offset, SEEK_END) system call, the system call handler first validates the file descriptor against the process's open file table. It then accesses the corresponding file table entry to retrieve the files inode metadata, which contains the disk addresses of the files data blocks. The new offset will then be calculated as file_size + offset. This new offset is written to the current file position in the open file table entry before releasing the inode lock and returning control to the user's process. This operation only accesses metadata structures, e.g. the file descriptor table, the open file table and inode, without reading any actual file data blocks, since it is a metadata-only operation.

5. File System Organization

a) [0.1 marks] (from Silberschatz) Consider a file system that uses inodes to represent files. Disk blocks are 8Kb in size, and a pointer to a disk block requires 4 bytes. This file system has 12 direct disk blocks, as well as single, double, and triple indirect disk blocks. What is the maximum size of a file that can be stored in this file system?

Block Size B = 8KB = 8192 bytes
Pointer size P = 4 bytes
Number of direct blocks = 12
Has single indirect, double indirect and triple indirect blocks.

Number of pointers per block N = Block Size B / Pointer size P = B/P = 8192 / 4 = 2048

N = 2048

Capacity for each part

a) 12 Direct blocks

12 * 8 KB = 96KB

b) Single Indirect block

1 indirect block containing N pointers = N * 8KB

= 2048 * 8KB
= 2048 * 8192 bytes
= 16,777,216 bytes
= 16 MB

c) Double indirect block

1 double indirect block → N single indirect blocks → N^2 data blocks

N^2 * 8KB = (2048^2) * 8192

2048^2 = 4,194, 304

4,194, 304 * 8192 = 34,359,738,368 bytes = 32 GB

d) Triple indirect block

1 triple indirect block → N double indirect blocks → N^3 data blocks

N^3 * 8KB = (2048^3) * 8192

2048^3 = 8,589,934,592

8,589,934,592 * 8192 = 70,368,744,177,664 bytes

64TB

Total Maximum File Size

Direct = 96KB
Single indirect = 16 MB
Double indirect = 32 GB
Triple indirect = 64 TB

Sum = 96KB + 16 MB + 32 GB + 64 TB

64TB dominates, essentially 64TB + negligible

The maximum size of a file that can be stored in this file system is a 64 TB file.

b) [0.1 marks] Explain what you can do in case (a) if you need to store a file that is larger than the maximum size computed. Give an example showing how you can define a larger file, and what the size of that file would be.

If a file exceeds the maximum file size supported by the inode structure of 64TB, the file system itself cannot store it without modification, however one solution could be adding another file system extension through quadruple indirect block

Quadruple indirect pointer → N^4 data blocks
N = 2048
= (2048)^4 = 17,592,186,044,416 data blocks
= 17,592,186,044,416 data blocks * 8KB / data block
= 140,737,488,355,328KB = 128PB

New maximum file size = 64 TB + 128 PB = 128 PB (128 PB dominates)

Therefore to store a file larger than 64TB, the file system must be redesigned to include higher levels of indirection.