DATA SHEET
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14-Stage Binary Ripple Counter With Oscillator

High−Performance Silicon−Gate CMOS

MC74HC4060A

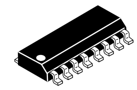
The MC74HC4060A is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master−slave flip−flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip−flop feeds the next and the frequency at each output is half of that of the preceding one. The state of the counter advances on the negative−going edge of the Osc In. The active−high Reset is asynchronous and disables the oscillator to allow very low power consumption during stand−by operation.

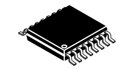
State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with Osc Out 2 of the HC4060A.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

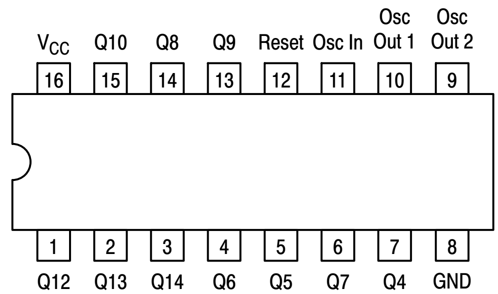


SOIC−16
D SUFFIX
CASE 751B



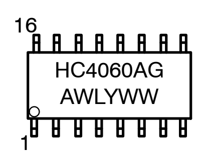
TSSOP−16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT



16−Lead Package (Top View)

MARKING DIAGRAMS



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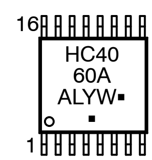


TSSOP−16

A	=	Assembly Location
L, WL	=	Wafer Lot
Y, YY	=	Year
W, WW	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

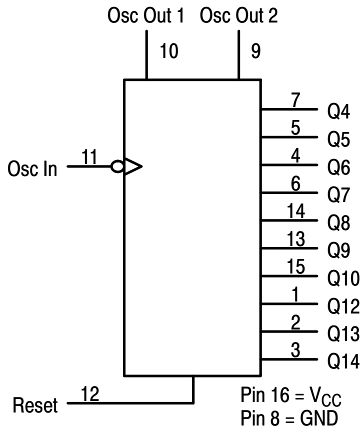
Clock	Reset	Output State
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5

LOGIC DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: –6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.5*	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types		–55	+125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition		V_{CC} V	Guaranteed Limit			Unit
					–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1V or V_{CC} –0.1V $\lvert I_{out}\rvert$ ≤ 20μA		2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1V or V_{CC} – 0.1V $\lvert I_{out}\rvert$ ≤ 20μA		2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High−Level Output Voltage (Q4−Q10, Q12−Q14)	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 20μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL}	$\lvert I_{out}\rvert$ ≤ 2.4mA $\lvert I_{out}\rvert$ ≤ 4.0mA $\lvert I_{out}\rvert$ ≤ 5.2mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage (Q4−Q10, Q12−Q14)	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 20μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL}	$\lvert I_{out}\rvert$ ≤ 2.4mA $\lvert I_{out}\rvert$ ≤ 4.0mA $\lvert I_{out}\rvert$ ≤ 5.2mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	

DC CHARACTERISTICS (Voltages Referenced to GND) (continued)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
V_{OH}	Minimum High−Level Output Voltage (Osc Out 1, Osc Out 2)	$V_{in} = V_{CC}$ or GND $\lvert I_{out} \rvert \le 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{CC}$ or GND $\lvert I_{out} \rvert \le 0.7mA$ $\lvert I_{out} \rvert \le 1.0mA$ $\lvert I_{out} \rvert \le 1.3mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage (Osc Out 1, Osc Out 2)	$V_{in} = V_{CC}$ or GND $\lvert I_{out} \rvert \le 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{CC}$ or GND $\lvert I_{out} \rvert \le 0.7mA$ $\lvert I_{out} \rvert \le 1.0mA$ $\lvert I_{out} \rvert \le 1.3mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	6.0	4	40	160	μA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 10 30 50	9.0 14 28 45	8.0 12 25 40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4)	2.0 3.0 4.5 6.0	300 180 60 51	375 200 75 64	450 250 90 75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4)	2.0 3.0 4.5 6.0	500 350 250 200	750 450 275 220	1000 600 300 250	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0 3.0 4.5 6.0	195 75 39 33	245 100 49 42	300 125 61 53	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Qn to Qn+1 (Figures 3 and 4)	2.0 3.0 4.5 6.0	75 60 15 13	95 75 19 16	125 95 24 20	ns

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns) **− continued**

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤85°C	≤125°C	Unit
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF

* For T_A = 25°C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

V_{CC} = 2.0 V: t_P = [93.7 + 59.3 (n−1)] ns V_{CC} = 4.5 V: t_P = [30.25 + 14.6 (n−1)] ns
V_{CC} = 3.0 V: t_P = [61.5+ 34.4 (n−1)] ns V_{CC} = 6.0 V: t_P = [24.4 + 12 (n−1)] ns

Symbol	Parameter	Typical @ 25°C, V_{CC} = 5.0 V	Unit
C_{PD}	Power Dissipation Capacitance (Per Package)*	35	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	100 75 20 17	125 100 25 21	150 120 30 25	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 23 19	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 23 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4060ADR2G	SOIC−16 (Pb−Free)	2500 Units / Reel
MC74HC4060ADTR2G	TSSOP−16 (Pb−Free)	2500 Units / Reel

DISCONTINUED (Note 1)

Device	Package	Shipping†
MC74HC4060ADG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV74HC4060ADR2G*	SOIC−16 (Pb−Free)	2500 Units / Reel
MC74HC4060ADTG	TSSOP−16 (Pb−Free)	96 Units / Rail
NLVHC4060ADTR2G*	TSSOP−16 (Pb−Free)	2500 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PIN DESCRIPTIONS

INPUTS

Osc In (Pin 11)

Negative−edge triggering clock input. A high−to−low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

Reset (Pin 12)

Active−high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4—Q10, Q12−Q14 (Pins 7, 5, 4, 6, 13, 15, 1, 2, 3)

Active−high outputs. Each Qn output divides the Clock input frequency by 2^N. The user should note the Q1, Q2, Q3 and Q11 are not available as outputs.

Osc Out 1, Osc Out 2 (Pins 9, 10)

Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

SWITCHING WAVEFORMS

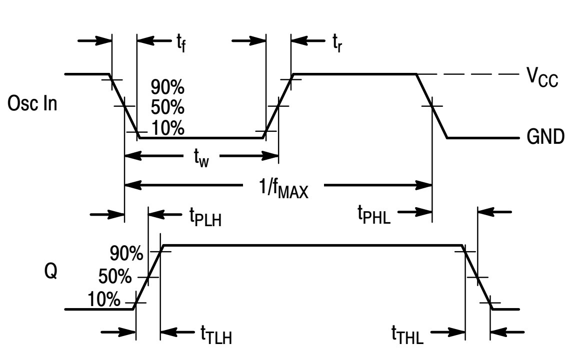


Figure 1.

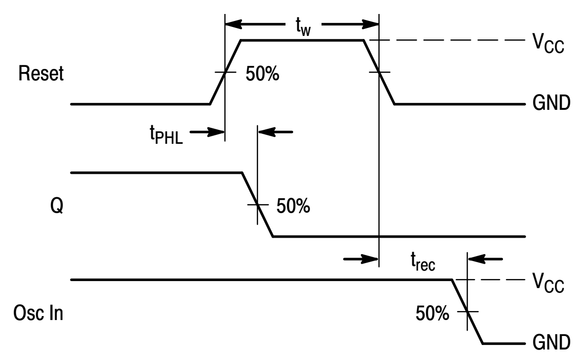


Figure 2.

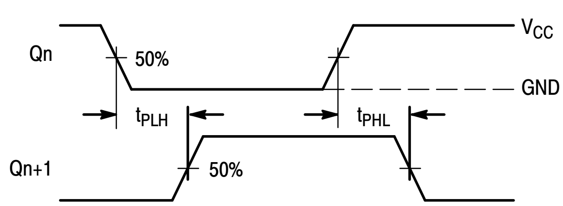
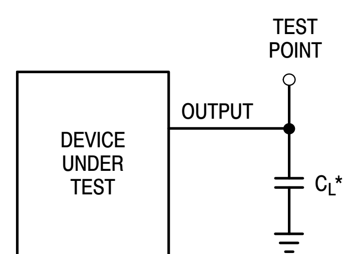


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

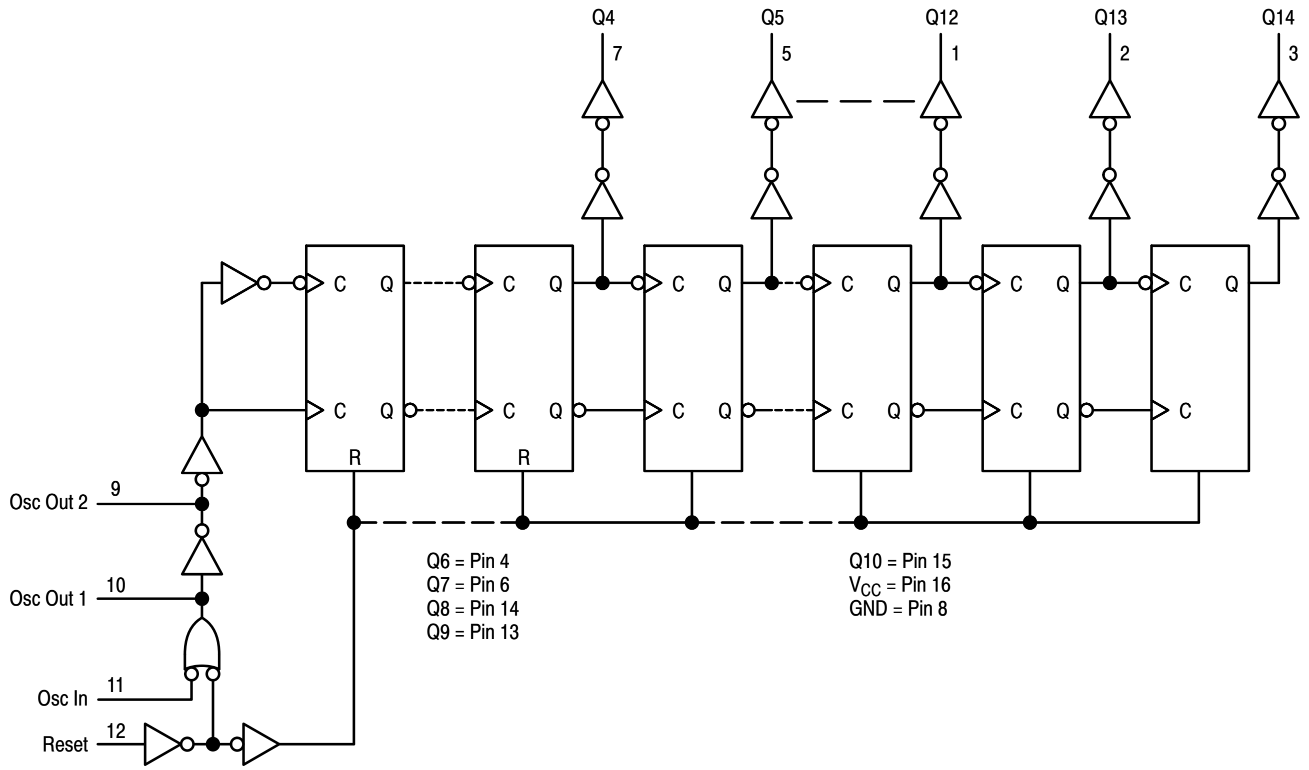
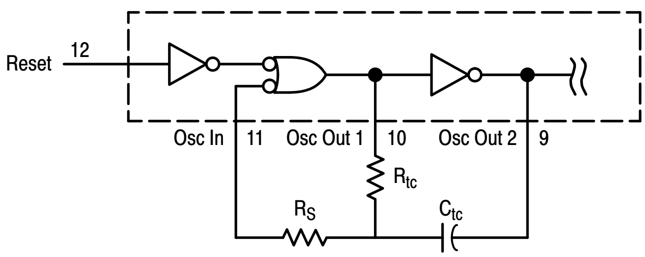


Figure 5. Expanded Logic Diagram



For $2.0V \leq V_{CC} \leq 6.0V$
$10R_{tc} > R_S > 2R_{tc}$
$400Hz \leq f \leq 400Khz$:

$f \approx \frac{1}{2.2\,R_{tc}C_{tc}}$ (f in Hz, R_{tc} in ohms, C_{tc} in farads)

The formula may vary for other frequencies.

Figure 6. Oscillator Circuit Using RC Configuration

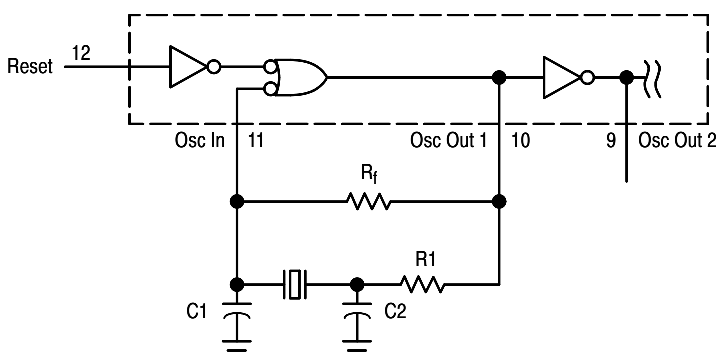
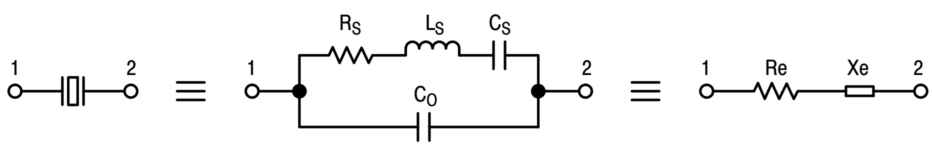


Figure 7. Pierce Crystal Oscillator Circuit

TABLE 1. CRYSTAL OSCILLATOR AMPLIFIER SPECIFICATIONS (T_A = 25°C; Input = Pin 11, Output = Pin 10)

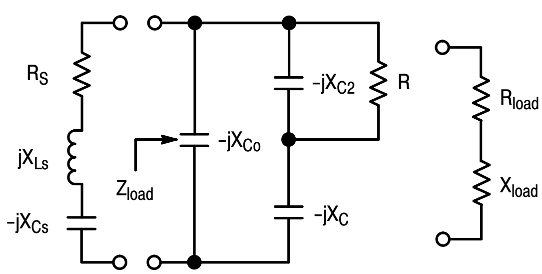
Type		Positive Reactance (Pierce)
Input Resistance, R_{in}		60MΩ Minimum
Output Impedance, Z_{out} (4.5V Supply)		200Ω (See Text)
Input Capacitance, C_{in}		5pF Typical
Output Capacitance, C_{out}		7pF Typical
Series Capacitance, C_a		5pF Typical
Open Loop Voltage Gain with Output at Full Swing, α	3Vdc Supply 4Vdc Supply 5Vdc Supply 6Vdc Supply	5.0 Expected Minimum 4.0 Expected Minimum 3.3 Expected Minimum 3.1 Expected Minimum

PIERCE CRYSTAL OSCILLATOR DESIGN



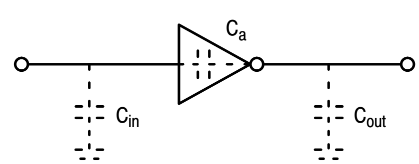
Value are supplied by crystal manufacturer (parallel resonant crystal).

Figure 8. Equivalent Crystal Networks



NOTE: C = C1 + C_{in} and R = R1 + R_{out}. C_o is considered as part of the load. C_a and R_f typically have minimal effect below 2MHz.

Figure 9. Series Equivalent Crystal Load



Values are listed in Table 1.

Figure 10. Parasitic Capacitances of the Amplifier

DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2MHz where Z is a resistor R1. Above 2MHz, additional impedance elements should be considered: C_{out} and C_a of the amp, feedback resistor R_f, and amplifier phase shift error from 180°C.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_O}(R_S + jX_{L_S} - jX_{C_S})}{-jX_{C_O} + R_S + jX_{L_S} - jX_{C_S}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_s for the crystal should be used in the equation.

Step 2: Determine β, the attenuation, of the feedback network. For a closed-loop gain of $2, A_v\beta = 2, \beta = 2/A_v$ where A_v is the gain of the HC4060A amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: A manufacturer may specify an external load capacitance of 32pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load}, For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then $R_{load} = (2\pi f_o L_S/Q) - R_s$ where L_s and R_s are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2}(X_e - X_C)} \quad \text{(with feedback phase shift = 180°)} \qquad \text{(Eq 1}$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{Cload} \quad \text{(where the loading capacitor is an external load, not including } C_o\text{)} \qquad \text{(Eq 2}$$

$$R_{load} = \frac{R X_{C_o} X_{C2}\left[(X_C + X_{C2})(X_C + X_{C_o}) - X_C(X_C + X_{C_o} + X_{C2})\right]}{X^2_{C2}(X_C + X_{C_o})^2 + R^2(X_C + X_{C_o} + X_{C2})^2} \qquad \text{(Eq 3}$$

Here $R = R_{out} + R1$. R_{out} is amp output resistance, R1 is Z. The C corresponding to X_C is given by $C = C1 + C_{in}$.

Alternately, pick a value for R1 (i.e, let $R1 = R_S$). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that $Q = 2\pi f_o L_s/(R_s + R_{load})$ to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

SELECTING R_f

The feedback resistor, R_f, typically ranges up to 20MΩ. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, "Designing Crystal Oscillators", Machine Design, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", Machine Design, April 25, 1985.

ALSO RECOMMENDED FOR READING:

E. Hafner, "The Piezoelectric Crystal Unit-Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", Electro-Technology, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

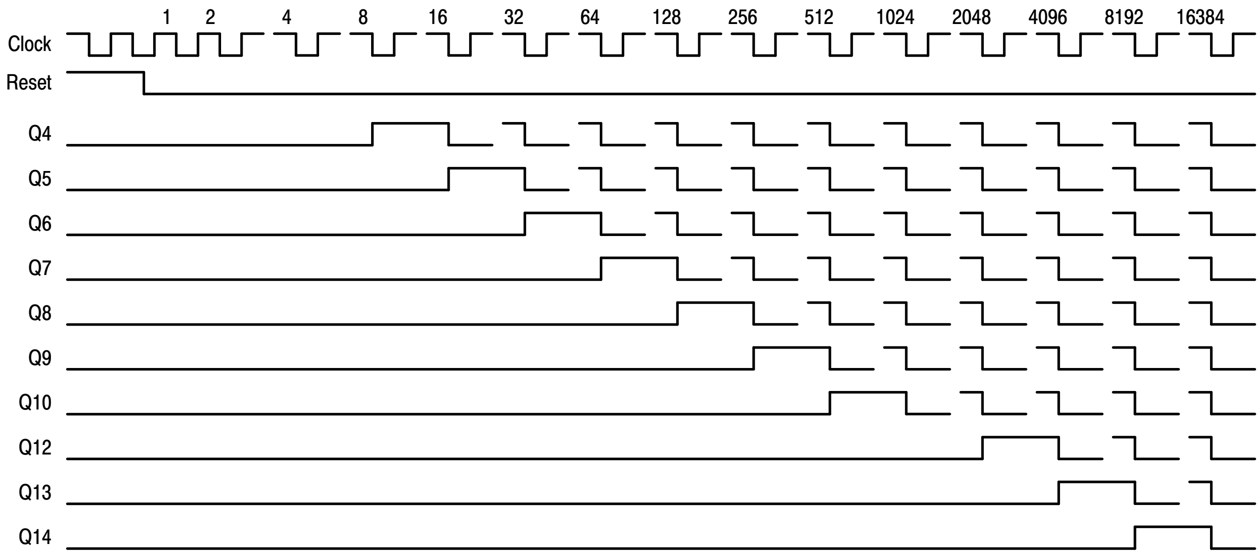
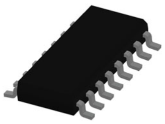


Figure 11. Timing Diagram

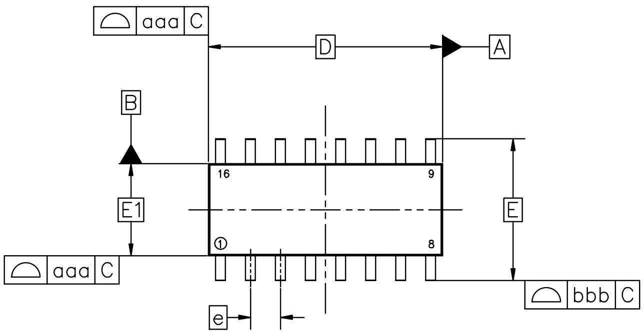


SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

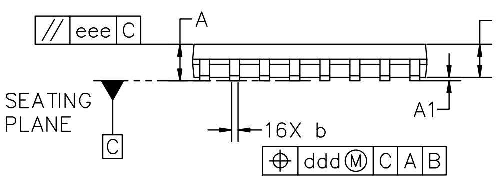
DATE 18 OCT 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

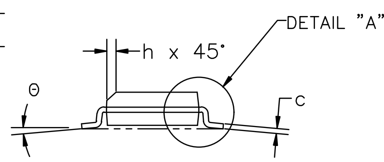
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



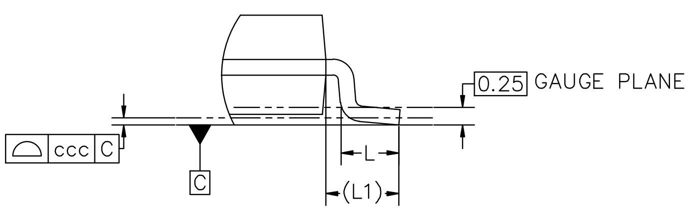
TOP VIEW



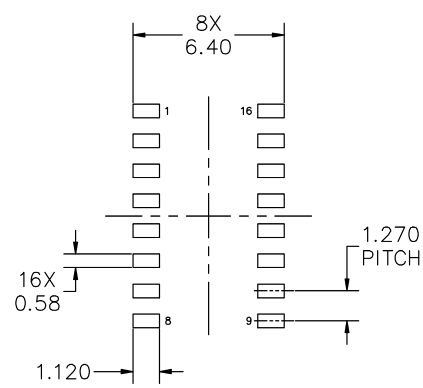
SIDE VIEW



END VIEW



DETAIL "A"
Scale 3:1

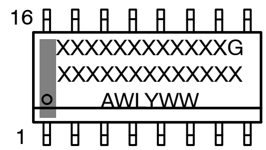


RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**	**PAGE 1 OF 2**

GENERIC MARKING DIAGRAM*

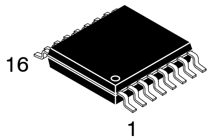


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

PIN	STYLE 1	STYLE 2	STYLE 3	STYLE 4
PIN 1.	COLLECTOR	CATHODE	COLLECTOR, DYE #1	COLLECTOR, DYE #1
2.	BASE	ANODE	BASE, #1	COLLECTOR, #1
3.	EMITTER	NO CONNECTION	EMITTER, #1	COLLECTOR, #2
4.	NO CONNECTION	CATHODE	COLLECTOR, #1	COLLECTOR, #2
5.	EMITTER	CATHODE	COLLECTOR, #2	COLLECTOR, #3
6.	BASE	NO CONNECTION	BASE, #2	COLLECTOR, #3
7.	COLLECTOR	ANODE	EMITTER, #2	COLLECTOR, #4
8.	COLLECTOR	CATHODE	COLLECTOR, #2	COLLECTOR, #4
9.	BASE	CATHODE	COLLECTOR, #3	BASE, #4
10.	EMITTER	ANODE	BASE, #3	EMITTER, #4
11.	NO CONNECTION	NO CONNECTION	EMITTER, #3	BASE, #3
12.	EMITTER	CATHODE	COLLECTOR, #3	EMITTER, #3
13.	BASE	CATHODE	COLLECTOR, #4	BASE, #2
14.	COLLECTOR	NO CONNECTION	BASE, #4	EMITTER, #2
15.	EMITTER	ANODE	EMITTER, #4	BASE, #1
16.	COLLECTOR	CATHODE	COLLECTOR, #4	EMITTER, #1

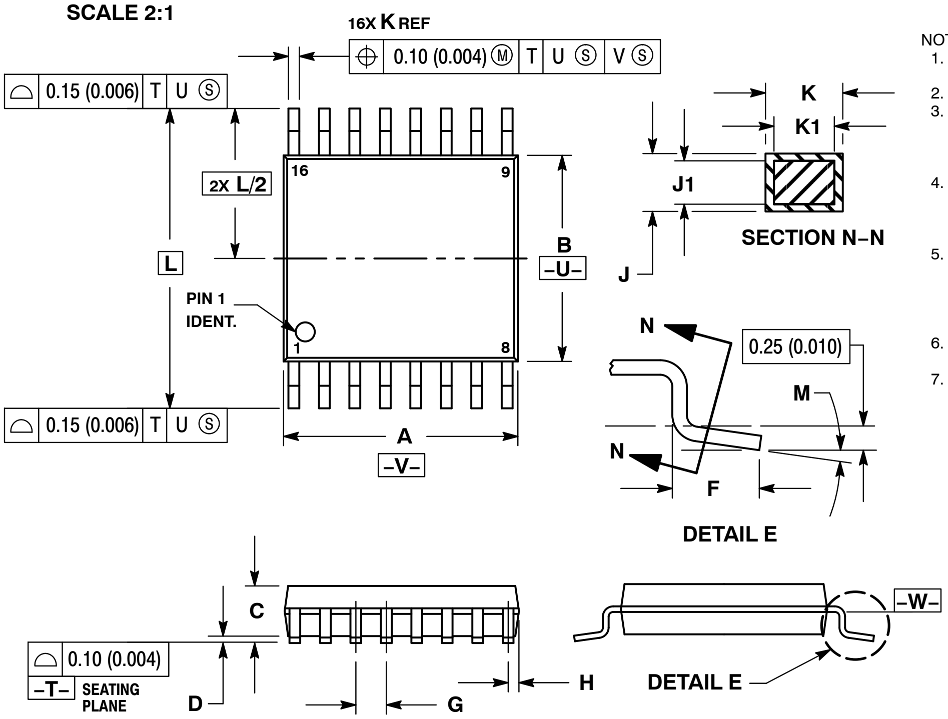
PIN	STYLE 5	STYLE 6	STYLE 7
PIN 1.	DRAIN, DYE #1	CATHODE	SOURCE N-CH
2.	DRAIN, #1	CATHODE	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	CATHODE	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	CATHODE	GATE P-CH
5.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	CATHODE	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	CATHODE	SOURCE P-CH
9.	GATE, #4	ANODE	SOURCE P-CH
10.	SOURCE, #4	ANODE	COMMON DRAIN (OUTPUT)
11.	GATE, #3	ANODE	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	ANODE	COMMON DRAIN (OUTPUT)
13.	GATE, #2	ANODE	GATE N-CH
14.	SOURCE, #2	ANODE	COMMON DRAIN (OUTPUT)
15.	GATE, #1	ANODE	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	ANODE	SOURCE N-CH



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

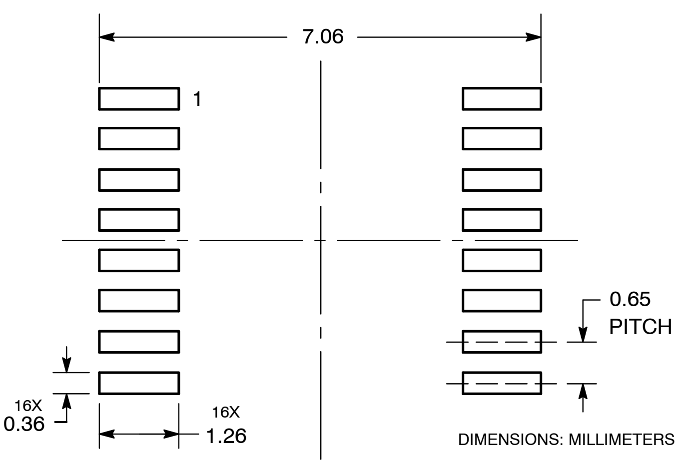
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

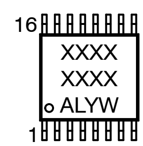
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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