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Two Multichannel Integrated Circuits for Neural Recording and Signal Processing

Iyad Obeid*, James C. Morizio, Karen A. Moxon, Miguel A. L. Nicolelis, and Patrick D. Wolf

***Abstract*—We have developed, manufactured, and tested two analog CMOS integrated circuit "neurochips" for recording from arrays of densely packed neural electrodes. Device A is a 16-channel buffer consisting of parallel noninverting amplifiers with a gain of 2 V/V. Device B is a 16-channel two-stage analog signal processor with differential amplification and high-pass filtering. It features selectable gains of 250 and 500 V/V as well as reference channel selection. The resulting amplifiers on Device A had a mean gain of 1.99 V/V with an equivalent input noise of 10 μV_{rms}. Those on Device B had mean gains of 53.4 and 47.4 dB with a high-pass filter pole at 211 Hz and an equivalent input noise of 4.4 μV_{rms}. Both devices were tested *in vivo* with electrode arrays implanted in the somatosensory cortex.**

***Index Terms*—Integrated headstage, neural amplifier, neural recording, neurochip.**

I. Introduction

The rapidly expanding field of neuroprosthetics aims to interface artificial devices with the brain. Advancements in this field will require an increase in the number and density of simultaneously monitored electrodes implanted in multiple cortical and subcortical regions [1], [2]. A clear solution to this problem is to use custom designed analog integrated circuits (ICs) to acquire and process the electrical signals transduced from implanted extracellular cortical electrodes.

Manuscript received March 4, 2002; revised October 1, 2002. This work was supported by grants from Defense Advanced Research Projects Agency (DARPA), the Office of Naval Research (ONR), and the National Institutes of Health (NSF). *Asterisk indicates corresponding author.*

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Digital Object Identifier 10.1109/TBME.2002.807643

Single-unit action potentials require signal processing to enhance the resolution of their arrival times and the differentiability of their waveform morphologies. Such signals must be buffered to reduce high source impedances and then amplified before being digitized. Bandpass filtering attenuates out-of-band biological and electrical noise, while high-pass filtering may attenuate low-frequency baseline drifts [3]. Published neural signal bandwidths range from 100–400 Hz to 3 k–10 kHz [2], [4], [5].

To explore the development of a single-chip hardware platform for neural data acquisition, two ICs were designed, fabricated, and tested. Device A was designed as a prototype headstage to investigate simple buffering and gain strategies, while Device B was used to investigate the integration of more advanced analog signal processing strategies customized for single units.

II. Methods

A. Device A

Device A is a 16-channel analog CMOS IC that amplifies and buffers signals taken directly from implanted neural electrodes. Each channel features a follower with a gain of 2 V/V formed from an opamp with two 20-kΩ feedback resistors [6]. Electrodes interface directly to the noninverting opamp inputs on each channel. Since these inputs are CMOS gates with picoamp leakage currents, the electrodes are not loaded. The voltage gain improves the signal-to-noise ratio (SNR) by reducing the relevance of electrical noise incurred in later stages. The gain of 2 V/V was selected for its potential for accurate implementation in silicon (to reduce gain variability across channels) and to limit the risk of saturation due to low-frequency electrode offsets. The opamp is a two stage amplifier with a P-type input differential pair operating from $\pm$2.5-V supplies. P-type devices were used for the differential pair (instead of N-type) for superior noise performance.

B. Device B

Device B is a 16-channel high-pass filter with a variable passband gain of either 250 or 500 V/V. The block diagram is shown in Fig. 1. The IC is divided into two sets of eight channels. Each channel consists of a variable gain high-pass filter cascaded into a single differential amplifier. The eight output signals from the variable gain filters of each eight-channel set are also wired to a 9 : 1 multiplexer. The ninth input on each of the multiplexers is the ground reference voltage, typically tied to a screw in the subject's skull [7]. The outputs of the two multiplexers are wired to the reference inputs of the eight differential amplifiers of the corresponding set of channels. The multiplexer allows the user to select between unipolar (ground reference) and bipolar (signal reference) recordings.

The architecture of the variable gain high-pass filters is seen in Fig. 2. Switch S may be closed to short R_{2b} and decrease the gain, while capacitor C gives the amplifier a high-pass filter characteristic with a dc gain of unity. The circuit was designed for a gain of 25 V/V or 50 V/V, with a high-pass filter pole at 217 Hz; the gain setting for all channels is determined by a single digital signal. Due to the prohibitive size of capacitors in silicon ($950 \cdot 10^{-18}$ F/μm^2 for our process) all 16 capacitors are placed off-chip. Designs using this circuit topology with smaller, integratable capacitors were rejected for noise concerns, as they would require resistors as large as tens of gigaohms to realize comparable gain and filter cutoffs. Our filter architecture combines a high input impedance with both gain and high-pass filtering, and requires only one additional input-output (I/O) per channel. The second section of Device B is a basic single-opamp differential amplifier with

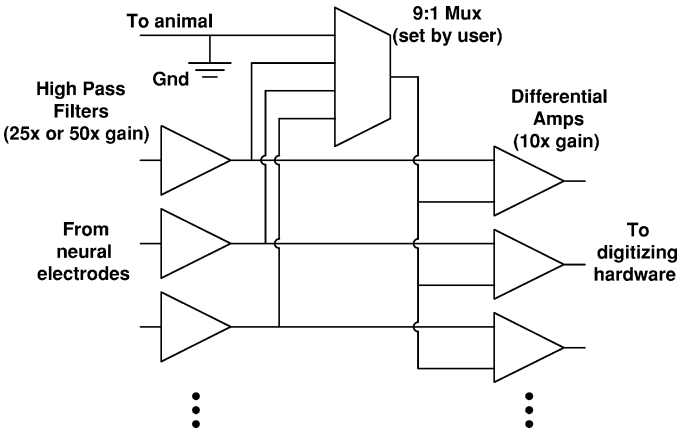

Fig. 1. Device B block diagram. Functionality is broken down into two sections. The first is a bank of two sets of eight variable gain high-pass filters. The second section is a bank of two sets of differential amplifiers. First section outputs from each group of eight are wired to one of two user controlled 9 : 1 multiplexers. The ninth input on both multiplexers is the ground reference voltage. This architecture allows the user to select between a unipolar (ground reference) or bipolar (user selected channel reference) recording.

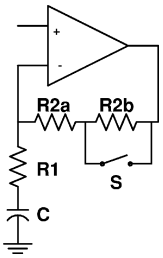

Fig. 2. Device B's variable gain filter architecture combines high input impedance, variable gain, and a high-pass filter characteristic into a single-opamp design requiring only one capacitor I/O per channel. At dc, capacitor C is an open circuit and gain is one, regardless of switch status.

a gain of ten set using resistor feedback [6]. The active component used in all Device B amplifiers is a three-stage CMOS opamp with an N-type input differential pair operating from ± 2.5 V supplies.

C. Fabrication and Packaging

The circuit die sizes were 1.4×3.4 mm for Device A and 3×3.25 mm for Device B. Device A was manufactured using the HP 0.8-μm double-metal double-poly process, while Device B was made using the AMI 0.5-μm triple-metal double-poly process. Both devices were mounted on custom-designed printed circuit boards for evaluation. The raw die for Device A was epoxied and gold wire bonded to a headstage board measuring 9.5×19 mm [8], along with input and output connectors, a bias setting resistor, and two bypass capacitors. The raw die was used instead of a packaged device to reduce the headstage size.

III. Results

Both devices were characterized and used to make *in vivo* neural recordings.

A. Circuit Evaluation

The evaluation of Device A showed that the gain varied little across channels ($\mu = 1.99$, $\sigma = 0.035$). The input referred noise was found to be 10 $\mu V_{\rm rms}$ using a high-precision test unit (Audio Precision AP2) that set the bandwidth at 400–22 kHz. The 20-kΩ feedback resistors, therefore, represent only 1.8% of the total noise. Device A consumed 1.4 mW per channel, had an average output impedance of 113.5 Ω, and showed an output dc offset of 1.35 V, possibly due to device mismatch in the opamp output stage.

Device B was found to have mean low and high gains of 47.4 and 53.4 dB, respectively ($\approx$0.6 dB below predicted values), with a high-pass filter pole at 211 Hz. The spread of the pole locations ($\sigma = 4.89$ Hz) corresponds to a capacitor mismatch of less than 5%. Device B consumed 950 μW per channel and had an output impedance of 62.3 Ω and an input referred noise of 4.4 $\mu V_{\rm rms}$. The output dc offset was 37 mV. The common mode rejection ratio (CMRR) was measured to be -42.6 dB at 4 kHz, compared with the predicted value of -58 dB. Although extracted parasitic parameters were included in the simulations, resistor and finite-element transfer size mismatch due to process variations were not modeled. We, therefore, expect that approximately 15 dB of CMRR is lost in the passband due to device mismatch. The dc common mode range was increased tenfold (from -50–70 mV to -500–700 mV) when the ground referencing was changed from unipolar to bipolar. This is as expected, since bipolar referencing makes use of the differential amplifier CMRR to attenuate low-frequency common mode signals whereas unipolar referencing does not.

B. In Vivo Testing

The practical functionality of both devices was evaluated by testing them *in vivo*. Subjects were rats and macaques with preexisting microwire electrodes implanted in the somatosensory cortex. The implanted electrodes were grouped into sets of eight and terminated in nine-pin sockets epoxied to the animal's skull. The ninth pin of each socket was wired to a grounding screw in the subject's skull. Fig. 3 shows examples of action potentials recorded using each of the devices.

Device A was shown to produce equivalent signals to a commercially available headstage (HST/8o25, Plexon Inc., Dallas, TX). This device is an eight channel unity gain buffer measuring 16×19 mm. A "Y" adapter was used to facilitate signal recordings using both devices simultaneously. Fig. 4 demonstrates that single-unit waveforms acquired with the two devices are nearly indistinguishable. The variance of the differences between the Device A and Plexon waveforms (92.4 μV^2) closely matches the predicted value based on the measured noise of the two devices (111.9 μV^2). The difference between these values may be attributable to common mode noise. These measurements verify that the Device A and Plexon headstages produced identical signals and that any differences between the respective waveforms are attributable to circuit noise.

IV. Discussion

As a first step toward developing fully integrated silicon neural interfaces, we have designed, manufactured, and tested two ICs for acquiring neural signals. Device A has demonstrated our ability to generate headstages with gain, while Device B has explored the integration of high input impedance, dc rejection, high-pass filtering, gain, and reference channel selection in the neural interface.

A challenging problem when designing neural interfaces is the need to measure microvolt level neural signals superimposed on large low-frequency electrode offset voltages. One solution for rejecting these offsets has been to combine the capacitance of the electrode with a low input impedance at the headstage to produce a high-pass filter [3]. However, this technique requires the headstage amplifiers to be matched to a particular type of electrode and may require trimmable devices to control input impedance [9]. Lowering the input impedance may also decrease the accuracy of the high-pass filter poles, thus reducing the CMRR of any differential amplification that follows [10]. In contrast, the high-pass filter design of Device B does not require any matching between electrode and circuit. Other techniques that exist

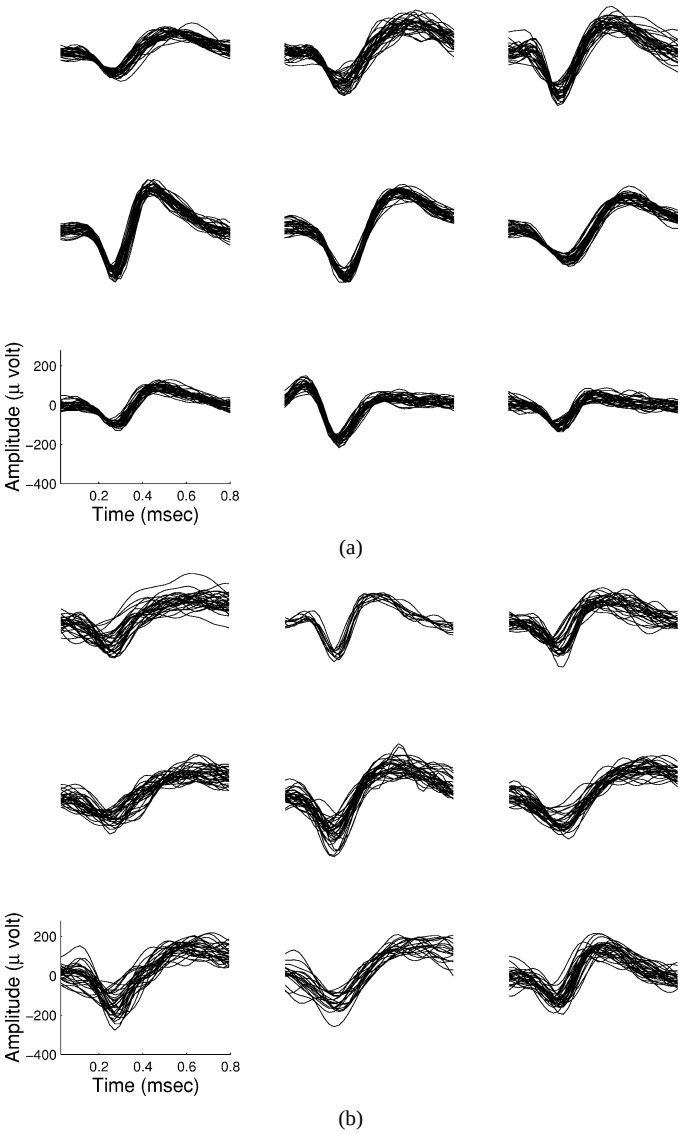

Fig. 3. Single units acquired using (a) Device A and (b) Device B. Signal amplitudes are referred back to the input. Device A units were acquired using the Device A headstage feeding into a Multichannel Acquisition Processor (Plexon). Device B units were acquired without a headstage; signals were amplified using the high gain setting (500 V/V), recorded onto digital tape ($\boldsymbol{F_s = 44.1}$ kHz), and then bandpass filtered (200 Hz–7.5 kHz Butterworth) in Matlab. All signals were spike sorted using Plexon spike sorting software.

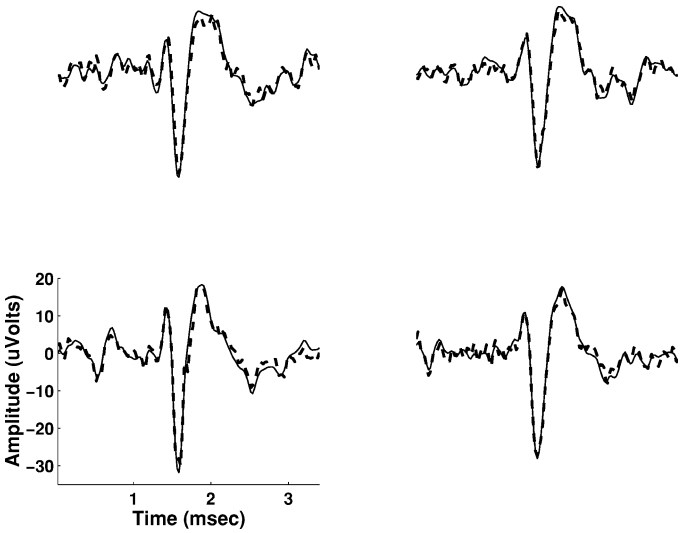

Fig. 4. A single unit captured simultaneously using both Device A (dashed traces) and a commercially available headstage (solid traces). Background biological noise is visible as local irregularities common to both sets of traces. Differences between the signals are due to differences in the devices' noise characteristics.

for high-pass filtering may not be applicable for filtering unamplified neural signals; switched capacitor and chopper modulated filters add switching noise to the microvolt range neural signals. Device B passes dc signals with unity gain while applying a passband gain of 250 or 500 V/V at the cost of a single off-chip capacitor per channel. More elaborate filters may be applied in later stages, after the signals are amplified and switching noise is less significant. Advanced headstages using our filter design for the first stage would, therefore, still require only one capacitor I/O per channel.

Device B featured variable gain and reference channel selection. The variable gain was included because our eventual goal is to wirelessly transmit digitized neural signals. Variable gain increases dynamic range while maintaining analog-to-digital converter resolution and, thus, minimizes the transmitted bit-rate. We saw no evidence however that the variable gain improved the SNR. The capability to switch between unipolar and bipolar recordings facilitated *in vivo* recordings; unipolar *in vivo* recordings were often saturated because the electrode offset voltages exceeded the unipolar mode's common mode range. The ability to select the bipolar reference channel improves the rejection of common mode biological signals [11].

The measured noise metrics indicate that both devices are adequate for visualizing neural signals. The input referred noise measurements for Devices A and B were 10 and 4.4 $\mu\mathrm{V_{rms}}$, respectively, compared with 3.5 $\mu\mathrm{V_{rms}}$ for the Plexon headstage. The difference between Devices A and B may be attributed to the difference in silicon processes. Our noise levels approximately match the expected noise in implantable microwire electrodes [7]. Although these noise levels are smaller than the typical levels of background biological noise, their contributions are noticeable in the signal traces (see Figs. 3 and 4). Since the circuit noise is in-band with the neural signals, it cannot be effectively attenuated without degrading neural signal quality. Based on our observations, future designs should have less than 5 $\mu\mathrm{V_{rms}}$ of in-band circuit noise.

V. Conclusion

This paper has presented two analog CMOS ICs for acquiring and processing cortically derived neural signals. The ability to obtain such signals in a compact and scalable form factor is a necessary first step in developing a robust neuroprosthesis.

Acknowledgment

The authors gratefully acknowledge the contributions of time and expertise from D. Krupa, D. Katz, R. Crist, D. Won, and H. Wiggins.

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Real-Time Signal Processing for Fetal Heart Rate Monitoring

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***Abstract*—An algorithm based on digital filtering, adaptive thresholding, statistical properties in the time domain, and differencing of local maxima and minima has been developed for the simultaneous measurement of the fetal and maternal heart rates from the maternal abdominal electrocardiogram during pregnancy and labor for ambulatory monitoring. A microcontroller-based system has been used to implement the algorithm in real-time. A Doppler ultrasound fetal monitor was used for statistical comparison on five volunteers with low risk pregnancies, between 35 and 40 weeks of gestation. Results showed an average percent root mean square difference of 5.32% and linear correlation coefficient from 0.84 to 0.93. The fetal heart rate curves remained inside a ±5-beats-per-minute limit relative to the reference ultrasound method for 84.1% of the time.**

***Index Terms*—Abdominal electrocardiogram, digital filtering, Doppler ultrasound, fetal heart rate.**

I. Introduction

FETAL heart rate (FHR) variations observed over 20 min during pregnancy and labor have commonly been used as indirect indications of the fetal condition [1]. The ability to perform long-term (e.g., 24 h) monitoring of the FHR would, thus, provide more information on the fetal condition [2].

Attempts to produce a portable system suited for long-term monitoring using Doppler ultrasound have not been successful because of its sensitivity to movements. Although there is no significant evidence from clinical data that short-term exposure to low-power ultrasound (used for imaging) is harmful to the fetus, complete safety of long-term exposure has yet to be established. To avoid these hazards, some researchers have even investigated phonocardiography applied to FHR detection [3].

Methods utilizing the abdominal electrocardiogram (AECG) have a better prospect for long-term monitoring using signal processing techniques [4]. The main difficulties encountered in determining the FHR from the AECG signal are the interference due to the maternal electrocardiogram (MECG), electromyogram (EMG), and motion artifact. To overcome the above problems, some multiple-lead algorithms use the thoracic MECG to cancel the abdominal MECG [5], but this is inconvenient for the patient during long-term monitoring.

In the present study, we have developed a system utilizing the AECG to determine the fetal heart rate. The objectives of our study are:

1) to utilize a single abdominal lead signal to extract the FHR;
2) to implement the algorithm in real-time using a small sized microprocessor-based system, making it suitable for ambulatory long-term monitoring;
3) to assess the accuracy of the developed system compared with data derived from Doppler ultrasound.

II. Methods

A. Algorithm

The algorithm was developed through a combination and modification of earlier techniques [6]–[8]. It is based on digital filtering, adaptive thresholding, statistical properties in the time domain and differencing of local maxima and minima. As shown in Fig. 1, two almost similar sets of operations are used to enhance and detect the maternal and fetal QRS complexes respectively. The AECG is first passed through a finite impulse response bandpass filter (cut-off frequencies of 10 and 40 Hz) using a Hamming window. The digital filter's coefficients have been chosen to effectively pass the highest power density of the maternal and fetal R waves. The filtered signal was then cross-correlated with an 80-ms averaged maternal QRS template, based on the normal width of the maternal QRS complex. An initial template resembling the QRS complex was first used, then continuously updated based on a running average of detected QRS complexes.

The next routine (local maxima search) records the three largest local maxima within an R wave search interval. One of the maxima is accepted as the R wave peak by the use of a thresholding technique [7] and comparison to the QRS template. These steps, performed within the validation routine, allow to discriminate between the R peak and noise. The length of the search interval is initially 1 s and it is then continuously updated after the first RR interval measurement. The threshold is updated to varying R peak and noise levels [7].

Upon detection of the maternal QRS, the corresponding MECG complex is ensemble averaged over three samples to reduce the maternal contribution from the abdominal signal. The signal is then passed through another bandpass filter (cut-off frequencies of 30 and 40 Hz) to enhance the fetal QRS complexes. The filter parameters have been selected for the steepest possible cutoffs with the requirement of real-time implementation. The differencing of local maxima and

Manuscript received November 21, 2001; revised October 12, 2002. This work was supported by the Ministry of Science, Technology, and the Environment of Malaysia through the Intensification of Research on Priority Areas scheme under Grant 03-02-02-0033. *Asterisk indicates corresponding author.*

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Digital Object Identifier 10.1109/TBME.2002.807642