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Successive Approximation Register (SAR) ADC

The Successive Approximation Register (SAR) ADC is a widely used Analog-to-Digital Converter (ADC) that operates by approximating the input signal in a step-by-step manner.

Working Principle of SAR ADC:

The SAR ADC works on the principle of binary search and successive approximation. It includes the following components:

1. Sample and Hold Circuit (S/H): Captures the input analog voltage.
2. Comparator: Compares the input voltage with the DAC output.
3. Successive Approximation Register (SAR): Controls the DAC output.
4. Digital-to-Analog Converter (DAC): Converts the digital code from the SAR to an analog voltage.
5. Control Logic: Manages the conversion process.

Step-by-Step Operation:

1. Sampling: The input analog signal is sampled and held constant.
2. Initialization: The SAR sets the MSB (Most Significant Bit) to 1.
3. Comparison: The DAC output is compared with the input voltage using the comparator.
4. Decision: If DAC output < input voltage, the bit remains 1; else, it is cleared to 0.
5. Iteration: Repeat for the next MSB until all bits are evaluated.
6. Output: The final digital code is the closest binary approximation of the input signal.

Characteristics and Applications:

Characteristics:

- Resolution: Typically 8 to 16 bits.
- Conversion Time: Moderate, depends on clock frequency and resolution.
- Accuracy: Moderate to high.

- Speed: Faster than integrating ADCs but slower than flash ADCs.

Applications:

- Data acquisition systems
- Digital oscilloscopes
- Microcontroller-based measurement systems