How to select a proper alternative source

Notes: Keep the secrets of my company, I can not reveal some specific information. My apology.

First we need look through the features of target material, here is a list about a plenty of eminent function and characteristics:

1. Control inputs (DIR and OE) V_{IH} and V_{IL} levels are referenced to V_{CCA} voltage direction-control (DIR)
2. Bus hold on data inputs eliminates the need for external pullup or pulldown resistors it does not have any external resistors indeed.
3. V_{CC} isolation feature The VCC isolation feature allows the outputs to be in the high-impedance state when either VCCA or VCCB is at GND. The bus-hold circuitry on the powered-up side always stays active.
4. Fully configurable dual-rail design VccA and VccB
5. I/Os are 4.6-V tolerant
6. I_{off} supports partial-power-down mode operation What a prominent design in our schematic. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device.
7. Maximum data rates:
   320 Mbps ($V_{CCA} \geq 1.8$ V and $V_{CCB} \geq 1.8$ V) Mbps:Million bits per second
   170 Mps ($V_{CCA} \leq 1.8$ V or $V_{CCB} \leq 1.8$ V)
8. Latch-up performance exceeds 100 mA per JESD 78, class II I-test:The positive direction of I-test is outweigh or equal positive 100 mA.
   ESD protection exceeds JESD 22: electrostatic **discharge**
9. Joint Electron Device Engineering Council
   8000-V Human-Body Model (A114-A)
   200-V Machine Model (A115-A)
   1000-V Charged-Device Model (C101)

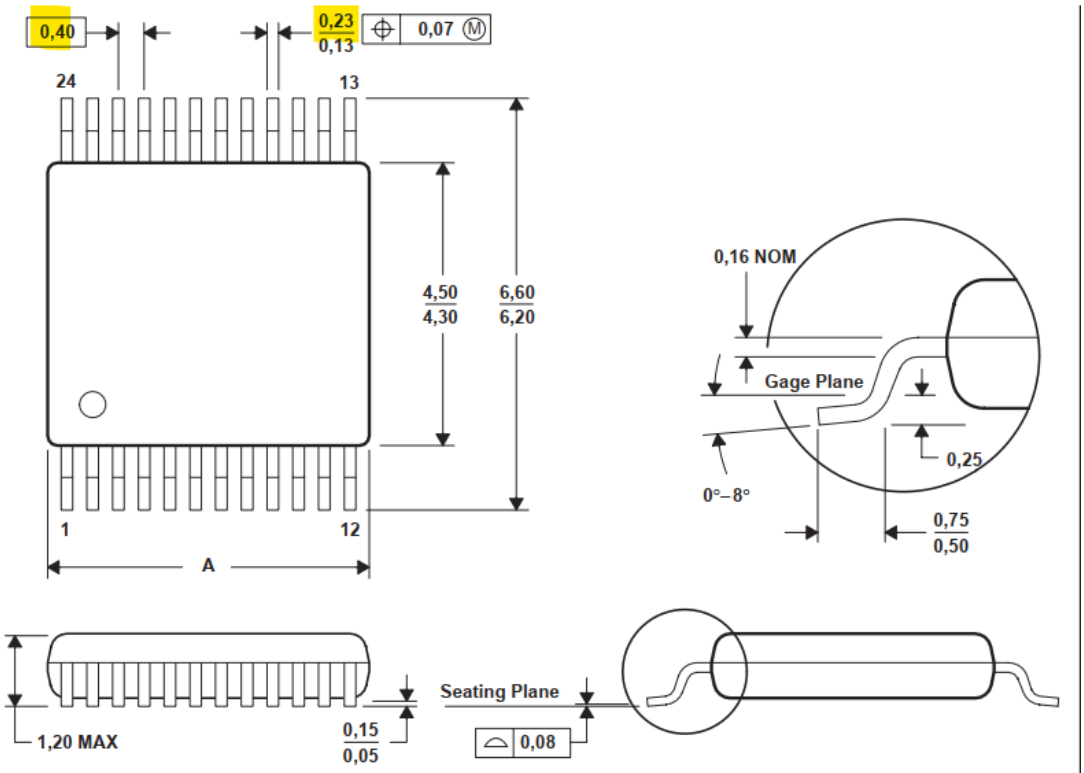
Overall I can scan important items from feature, and followed data is also vital for professional engineers. Because we should put the ICs into the PCB layout. The package, electrical parameters, Logic timing and etc. are also eminent.

Talking the package, well it is the first thing we care about. It would not put the target place properly supposing that the outline and pad size of ICs have big difference with original item, definitely we can ignore some bias/deviation. The key step is the difference within our range of tolerance in order to keep producting.Nowadays suppliers prefer to product thinner and less power loss ICs due to save energy and obey ESR(**Environmental**、**Social**、**Governance**). Check the below information please.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
[redacted]	DGV (TVSOP, 24)	5 mm × 6.4 mm
	PW (TSSOP, 24)	7.8 mm × 6.4 mm
	RHL (VQFN, 24)	5.5 mm × 3.5 mm

i.e DGV package Drawing (TVSOP packge type ,24 pins) 5mm length * 6.4mm width



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

Well, please pay more attention while you are a product engineer in the data of length, width and pitch. Also the distance of pin to pin should we care about. Check the data number by number, and you would better use a certain software like free CAD to check 3D dimensions, which is more accurate and intuitive that only PDF.It is convenient that we all check out the suppliers' website.