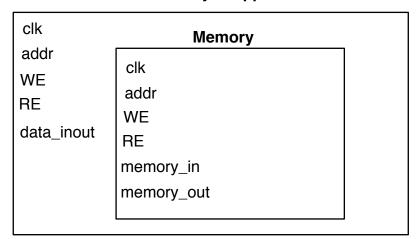
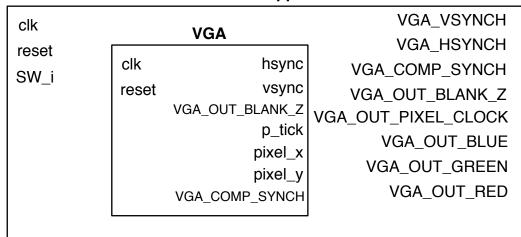
Memory wrapper



VGA wrapper



CPU

clk_enable	address
clk	data
reset	
program	
	WE
	RE

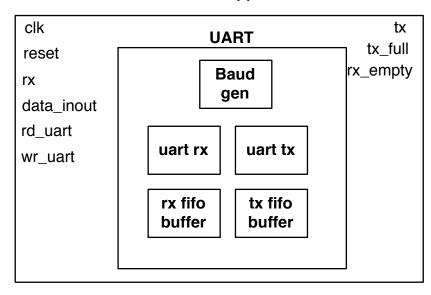
7sea hex mux

/seg nex mux			
	clk	an	
	reset	sseg	
	hex3		
	hex2		
	hex1		
	hex0		
	dp_in		

ClockDivider



UART wrapper



Steering Wheel A/D Conv.

clk	sclk
rst	ncs
sdata1	data1
start	done

Complete System

Complete System			
tx			
led			
ledg			
seg			
an			
mb_led_o			
vsync_out			
hsync_out			
comp_synch			
blank_out			
pixelclk_out			
b_out			
g_out			
r_out			
nCS			
SCLK			