CS2100 Computer Organisation
Lab #8: Multiplexer

Please prepare your report before attending the lab!

[This document is available on LumiNUS and module website http://www.comp.nus.edu.sg/~cs2100]

Name: _____ Matric. No: _____

Lab Group: _____

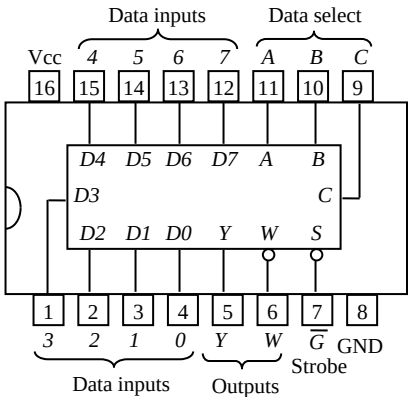
Objectives:

In this experiment, you will use a multiplexer to implement a logic function.

IC chips:

1. One **74LS151** chip (8-input Data Selector/Multiplexer).
2. One **74LS04** chip (inverters).

The 74LS151 chip contains an 8:1 multiplexer. The pin configuration and function table are shown below.



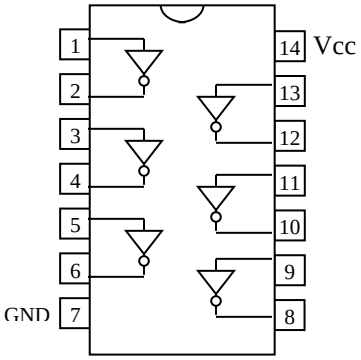
74LS151

INPUTS				OUTPUTS	
Select			Strobe		
C	*B*	*A*	$\overline{G}$	*Y*	*W*
x	x	x	H	L	H
L	L	L	L	*DO*	$\overline{DO}$
L	L	H	L	*D1*	$\overline{D1}$
L	H	L	L	*D2*	$\overline{D2}$
L	H	H	L	*D3*	$\overline{D3}$
H	L	L	L	*D4*	$\overline{D4}$
H	L	H	L	*D5*	$\overline{D5}$
H	H	L	L	*D6*	$\overline{D6}$
H	H	H	L	*D7*	$\overline{D7}$

x = don't care

Function table of 74LS151

The 74LS04 chip contains six inverters. The pin configuration is shown below.



74LS04

Procedure:

You are to design a **four-variable Boolean function *F(P,Q,R,S)*** that outputs 1 if the input *PQRS* is a palindrome (that it, if you read it in reverse it is the same as the original), or outputs 0 otherwise. Two outputs are already filled for you in the truth table below.

1. Complete the truth table for *F* below.

P	*Q*	*R*	*S*	*F*
0	0	0	0	
0	0	0	1	
0	0	1	0	**0**
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	**1**
0	1	1	1	

P	*Q*	*R*	*S*	*F*
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

3. Using an 8:1 multiplexer, provide four alternative solutions and fill in the multiplexer inputs in the respective diagrams below. If an input is complemented, for example, *P'*, you may write *P'* instead of drawing an inverter to obtain *P'* from *P*.

   (a) Implement function *F* using *QRS* as the selector lines. Fill in figure A below.

   (b) Implement function *F* using *PRS* as the selector lines. Fill in figure B below.

   (c) Implement function *F* using *PQS* as the selector lines. Fill in figure C below.

   (d) Implement function *F* using *PQR* as the selector lines. Fill in figure D below.

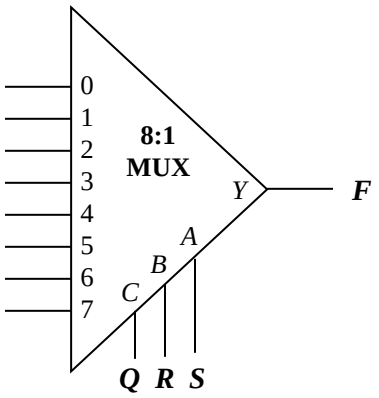


Figure A

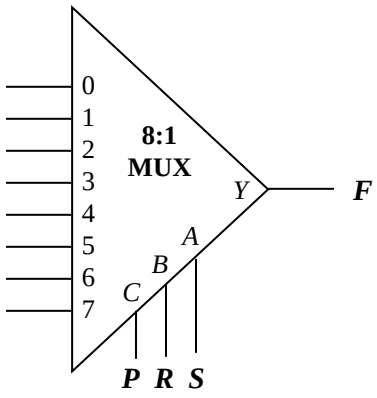


Figure B

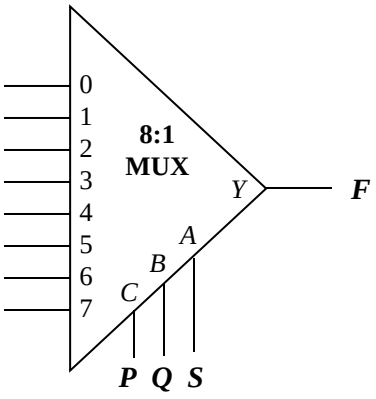


Figure C

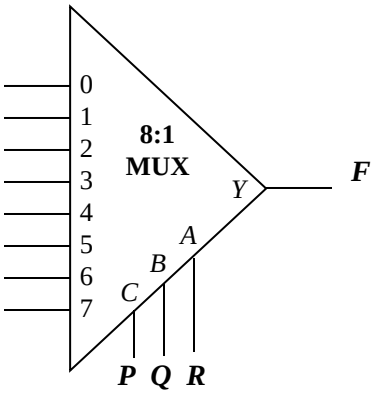


Figure D

4. You only need to implement Figure A. Connect the inputs *P*, *Q*, *R* and *S* to switches SW7, SW6, SW5 and SW4 respectively on the logic trainer for easy checking.

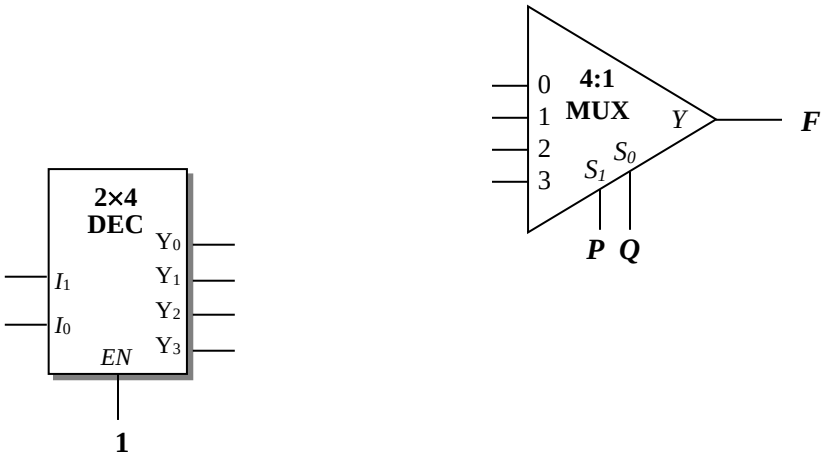
   You need to use an inverter in the 74LS04 chip to provide the necessary complemented input.

5. Show your implementation to your lab TA.

6. Using one 4:1 multiplexer and one 2×4 decoder with 1-enable as shown below, show how you might implement function *F* without using any additional logic gate. Complete the diagram below.

   Note that the selector lines for the 4:1 multiplexer are fixed to *PQ*, and you are not allowed to change them.

   You do not need to implement this circuit since you are not given any decoder in this lab.



Marking Scheme: Report (15 marks), Circuit (5 marks); Total: 20 marks.
Your graded report will be returned to you at the next lab.