Peripheral clock enable LSI LPTimer clock Peripheral LSE clock enable HSI USART clocks SYSCLK Peripheral PCI Kx clock enable I2C clocks LSI RC 32 kHz **IWDGCLK** RTCSEL[1:0] RTC To Independent watchdog Watchdo<u>g</u> enable RTCCLK OSC32 IN [► To RTC LSE OSC 32.768 kHz OSC32_OUT ► SDMMC2 clock Peripheral SYSCLK Periprieran clock enable мсо2 Г /1 to 5 ◀ PLLI2S HSE RTC PLL48CLK SDMMC1 clock LSE /2 to 31 ► HDMI-CEC clock Peripheral MCO1 ____/1 to 5 ◀ ► Ethernet PTP clock clock enable /488 Clock enable to AHB bus, memory HSI 200 MHz max 16 MHz and DMA HSI RC /8 SW ▶ to Cortex System timer HSI FCLK free-running clock HSE 200 MHz max. Not in sleep PRESC /1,2,..512 Cotex core Peripheral 200 MHz APBx PRESC /1,2,4,8,16 clock enable ► APBx peripheral clocks OSC_OUT [HSE 4-26 MHz HSE OSC max Peripheral OSC_IN clock enable if (APBx presc = 1x1 else x2 APBx timer clocks PCLK2 ►DFSDM kernel clock Peripheral clock enable ►DFSDM APB interface Periphera PLLDSICLK DSIHOST byte lane clock enable clock Periphera DSI PLL DSI PHY DSIHOST rxclkesc clock vco HSE/ or HSI PLLQ χN PLLDSICLK ►DFSDM audio clock /R PLL48CLK Peripheral clock enable USB & RNG Clock /P SPDIF-Rx Clock vco Peripheral clock enable
Peripheral /Q 12SSRC χN PLLI2SR ► I2S Clock PLLI2S /R lock enable Ext. clock I2S_CKIN Peripheral PLLI2SQ DIV ➤ SAI1 clock clock enable • Peripheral PLLSAIP clock enable ➤ SAI2 clock **PLLSAIQ** DIV /Q xΝ Peripheral LCD-TFT clock PLLLSAIR LTDC Clock /R DIV clock enable PLLSAI Peripheral ETH_MII_TX_CLK_MII clock enable MACTXCLK PHY Ethernet 25 to 50 MHz MII_RMII_SEL in SYSCFG_PMC to Ethernet MAC /2,20 Peripheral MACRXCLK clock enable ETH_MII_RX_CLK_MI Peripheral clock enable ► MACRMIICLK Peripheral USBHS USB2.0 PHY clock enable OTG HS SCL ► ULPI clock 24 to 60 MHz MSv39616V1

Figure 12. Clock tree