CS 2110 Quiz 3

Izaan Kamal

TOTAL POINTS

64 / 100

QUESTION 1

1 State Machines 20 / 20

✓ + 0 pts Graded

✓ + 2 pts $$S_0$$ output: $$ABC$$

✓ + 2 pts $$S_1$$ output: $$A$$

✓ + 2 pts $$S_2$$ output: $$C$$

✓ + 2 pts $$S_3$$ output: $$AB$$

✓ + 3 pts Transitions out of $$S_0$$: $$X \rightarrow S_2$$, $$\overline{X} \rightarrow S_2$$

✓ + 3 pts Transitions of out $$S_1$$: $$X \rightarrow S_0$$, $$\overline{X} \rightarrow S_3$$

✓ + 3 pts Transitions of out $$S_2$$: $$X \rightarrow S_2$$, $$\overline{X} \rightarrow S_1$$

✓ + 3 pts Transitions of out $$S_3$$: $$X \rightarrow S_2$$, $$\overline{X} \rightarrow S_1$$

- 5 pts More than eight possible transitions indicated, more than three transitions to different states, or similar major diagram improprieties/mistakes

QUESTION 2

Karnaugh Maps 16 pts

2.1 1111 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$1$$

2.2 1110 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.3 1100 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.4 1101 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$1$$

2.5 1011 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.6 1010 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.7 1000 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.8 1001 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.9 0011 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$1$$

2.10 0010 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.11 0000 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.12 0001 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$1$$

2.13 0111 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$1$$

2.14 0110 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$1$$

2.15 0100 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$0$$

2.16 0101 1 / 1

✓ + 0 pts Graded

✓ + 1 pts Correct: $$1$$

QUESTION 3

Sequential Logic: Edge-Triggered Components 10 pts

3.1 Box A 0 / 5

✓ + 0 pts Graded

+ 5 pts Correct: $$\text{NOT}$$

3.2 Box B 0 / 5

✓ + 0 pts Graded

+ 5 pts Correct: $$\text{NOT}$$

QUESTION 4

Short Answer 10 pts

4.1 Greatest positive imm5 value 0 / 5

✓ + 0 pts Graded

+ 5 pts Correct: $$15_{10}$$

4.2 Address space 0 / 2.5

✓ + 0 pts Graded

+ 2.5 pts Correct: $$\text{0x0800}$$ or $$2^{11}$$ or $$2048$$ addresses (i.e. distinct locations)

4.3 Addressability 0 / 2.5

✓ + 0 pts Graded

+ 2.5 pts Correct: $$8$$

+ 1 pts Partial: Off-by-one ($$7$$ or $$9$$)

QUESTION 5

LC-3 Datapath 20 pts

5.1 ST Cycle 1: ADDR1MUX = PC 2 / 2

✓ + 0 pts Graded

✓ + 2 pts Correct: $$\text{PC}$$

5.2 ST Cycle 1: ADDR2MUX = PCoffset9 0 / 2

✓ + 0 pts Graded

+ 2 pts Correct: $$\text{PCoffset9}$$

5.3 ST Cycle 2: ALUK = PassA 0 / 2

✓ + 0 pts Graded

+ 2 pts Correct: $$\text{PassA}$$

5.4 ST Cycle 2: GateALU 0 / 2

✓ + 0 pts Incorrect

+ 2 pts Correct: $$\text{GateALU}$$

5.5 ST Cycle 3: MEM.WE 2 / 2

✓ + 0 pts Graded

✓ + 2 pts Correct: $$\text{MEM.WE}$$

5.6 LEA Cycle 1: ADDR1MUX = PC 2 / 2

✓ + 0 pts Graded

✓ + 2 pts Correct: $$\text{PC}$$

5.7 LEA Cycle 1: ADDR2MUX = PCoffset9 0 / 2

✓ + 0 pts Graded

+ 2 pts Correct: $$\text{PCoffset9}$$

5.8 LEA Cycle 1: GateMARMUX 0 / 2

✓ + 0 pts Graded

+ 2 pts Correct: $$\text{GateMARMUX}$$

5.9 LEA Cycle 1: MARMUX = ADDER 2 / 2

✓ + 0 pts Graded

✓ + 2 pts Correct: $$\text{ADDER}$$

5.10 LEA Cycle 1: LD.CC 0 / 2

✓ **+ 0 pts** **Graded**

+ 2 pts Correct: $$\text{LD.CC}$$

QUESTION 6

LC-3 Instruction Disassembly 24 pts

6.1 Address x3003: x94BF 4 / 4

✓ **+ 0 pts** **Graded**

✓ **+ 4 pts** **Correct: $$\text{x94BF}$$**

6.2 Address x3004: ADD R2, R2, #1 4 / 4

✓ **+ 0 pts** **Graded**

✓ **+ 4 pts** **Correct: $$\text{ADD R2, R2, \#1}$$**

+ 2 pts Partial: $$\text{ADD DR, SR1, imm5}$$

Incorrect $$\text{DR}$$, $$\text{SR1}$$, or $$\text{imm5}$$ but correct opcode and proper syntax

- 1 pts Small syntax error: e.g. extra or missing commas

6.3 Address x3005: LDR R3, R1, #0 4 / 4

✓ **+ 0 pts** **Graded**

✓ **+ 4 pts** **Correct: $$\text{LDR R3, R1, \#0}$$**

+ 2 pts Partial: $$\text{LDR DR, BaseR, offset6}$$

Incorrect $$\text{DR}$$, $$\text{BaseR}$$, or $$\text{offset6}$$ but correct opcode and proper syntax

- 1 pts Small syntax error: e.g. extra or missing commas

6.4 Address x3006: x0405 0 / 4

✓ **+ 0 pts** **Graded**

+ 4 pts Correct: $$\text{x0405}$$

6.5 Address x3008: BRNP SKIP 4 / 4

✓ **+ 0 pts** **Graded**

✓ **+ 4 pts** **Correct: $$\text{BRNP SKIP}$$**

+ 2 pts Partial: $$\text{BRNP LABEL}$$

Correctly identified $$\text{BRNP}$$, and will assemble, but used incorrect label or an offset instead of a label

+ 1 pts Partial: $$\text{BRxxx LABEL}$$

Correctly identified $$\text{BR}$$ instruction, and will assemble, but used incorrect condition codes

Select this criteria even if the $$\text{LABEL}$$ is correct

6.6 Address x300C: STI R0, ADDR_CNT 4 / 4

✓ **+ 0 pts** **Graded**

✓ **+ 4 pts** **Correct: $$\text{STI R0, ADDR\_CNT}$$**

+ 2 pts Partial: $$\text{STI SR, LABEL}$$

Incorrect $$\text{SR}$$ or $$\text{LABEL}$$ but correct opcode and proper syntax OR, contrary to directions, wrote the offset instead of $$\text{LABEL}$$

- 1 pts Small syntax error: e.g. extra or missing commas

CS 2110 — Quiz 3 (35 minutes)
October 3rd, 2018

Full name: Izaan Kamal

GT username: ikamal3

This quiz is worth a total of **100 points**.

In accordance with the Georgia Institute of Technology Honor Code, I have neither given nor received aid on this quiz.

Signature: Izaan Kamal

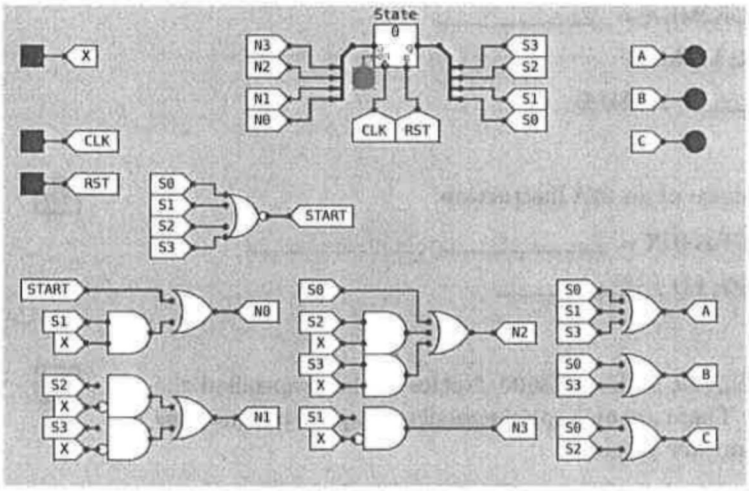
Please make sure all of your answers are contained within the answer boxes or the fill-in lines.

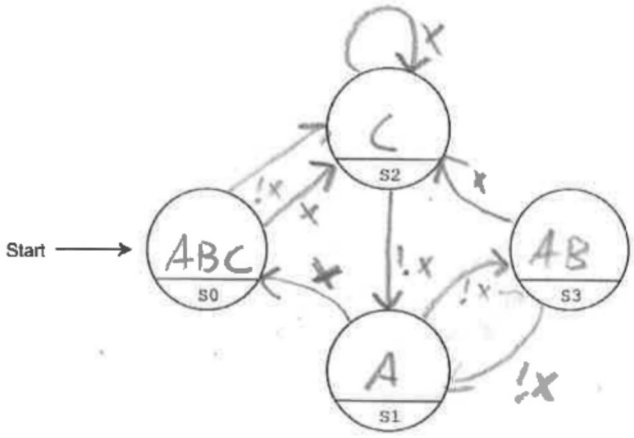
You have been provided with scratch paper for your work. You will **NOT** be given credit for showing work. Having anything except the answer inside the boxes or above the fill-in lines might cause incorrect results.

Write your name and answers legibly. You will not receive credit for illegible answers.

State Machines

1. Consider the following one-hot state machine circuit. The current state of the machine is represented by four bits, $S_3S_2S_1S_0$. The next state of the machine is represented by four bits, $N_3N_2N_1N_0$. There is one input $\{X\}$ and three outputs $\{A, B, C\}$. Annotate the diagram (on the right) with appropriate arrows for transitions and letters for outputs. **You must explicitly draw every possible transition.** [20]





Karnaugh Maps

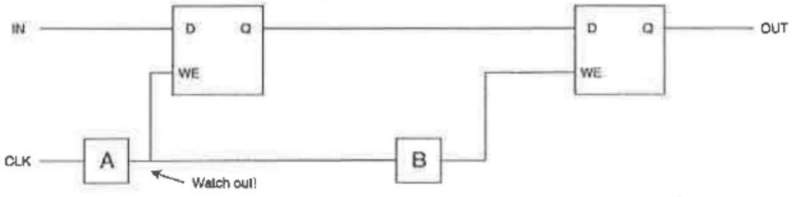
2. Consider the following simplified boolean expression and fill-in cells of the corresponding Karnaugh map with either 0s or 1s. [16]

Expression: $BD + \overline{A}D + \overline{A}\overline{B}C$

AB \ CD	11	10	00	01
11	1	0	0	1
10	0	0	0	0
00	1	0	0	1
01	1	1	0	1

Sequential Logic: Edge-Triggered Components

3. Consider the following edge-triggered component composed of two *positive level-triggered* D latches. OUT should only change when CLK is moving from low to high, i.e. *positive edge-triggered.* [10]



Which component for box A?:

● Wire ○ NOT

Which component for box B?:

● Wire ● NOT

Short Answer

4. For the following questions please answer in the space provided.

   (a) What is the largest positive number (in **decimal**) we can represent literally (i.e. as an immediate value) within an LC-3 AND instruction? [5]

   2^4

   (b) Consider a machine with memory addresses 0x0000 to 0x07FF where the largest decimal integer that can be read or written is 127 and the smallest is -128. Integers are stored with **two's complement**. [5]

   What is the address space? 255

   What is the addressability? 254

LC-3 Datapath

5. The Fetch and Decode instruction phases have been completed. Consider the Execute phase for the following instructions. *Note:* Please use the signal name terminology indicated on your reference sheet.

   (a) Fill-in the appropriate signals for the Execute phase of an ST instruction: [10]

   Cycle 1: ADDR1MUX = PC; ADDR2MUX = Base R;
   MARMUX = ADDER; gateMARMUX; LD.MAR

   Cycle 2: ALUK = AND; Gate MDR; LD.MDR

   Cycle 3: MEM.EN; MEM.WE

   (b) Fill-in the appropriate signals for the Execute phase of an LEA instruction: [10]

   Cycle 1: ADDR1MUX = PC; ADDR2MUX = Base R; LD.CC;
   MARMUX = ADDER; LD.REG; LD. PC

LC-3 Instruction Dissassembly

6. Consider the following LC-3 assembly program, starting at address x3000. Notice we have specified the addresses in memory and contents at those addresses. There are also comments detailing the instructions at each address, where appropriate, as well as a column for labels. [24]

   Please appropriately fill in each empty entry (notice there are **six** lines) in the "Contents" and "Instruction" columns. **Indicate the appropriate label, not the offset.**

Label	Address	Contents	Instruction
	x3000	x5020	;; AND R0, R0, #0
	x3001	x220D	;; LD R1, ADDR_STR
	x3002	xA40B	;; LDI R2, ADDR_CHR
	x3003	x94BF	;; NOT R2, R2
	x3004	x14A1	;; ADD R2, R2, #1
LOOP	x3005	x6640	;; LDR R3, R1, #0
	x3006	x0404	;; BRZ DONE
	x3007	x16C2	;; ADD R3, R3, R2
	x3008	x0A01	;; BRNP SKIP
	x3009	x1021	;; ADD R0, R0, #1
SKIP	x300A	x1261	;; ADD R1, R1, #1
	x300A	x0FF9	;; BR LOOP
DONE	x300A	xB003	;; STI R0, ADDR_CNT
	x300A	xF025	;; TRAP x25
ADDR_CHR	x300A	x4050	;;
ADDR_STR	x300A	x4800	;;
ADDR_CNT	x300A	x5000	;;