



电子科技大学

University of Electronic Science and Technology of China



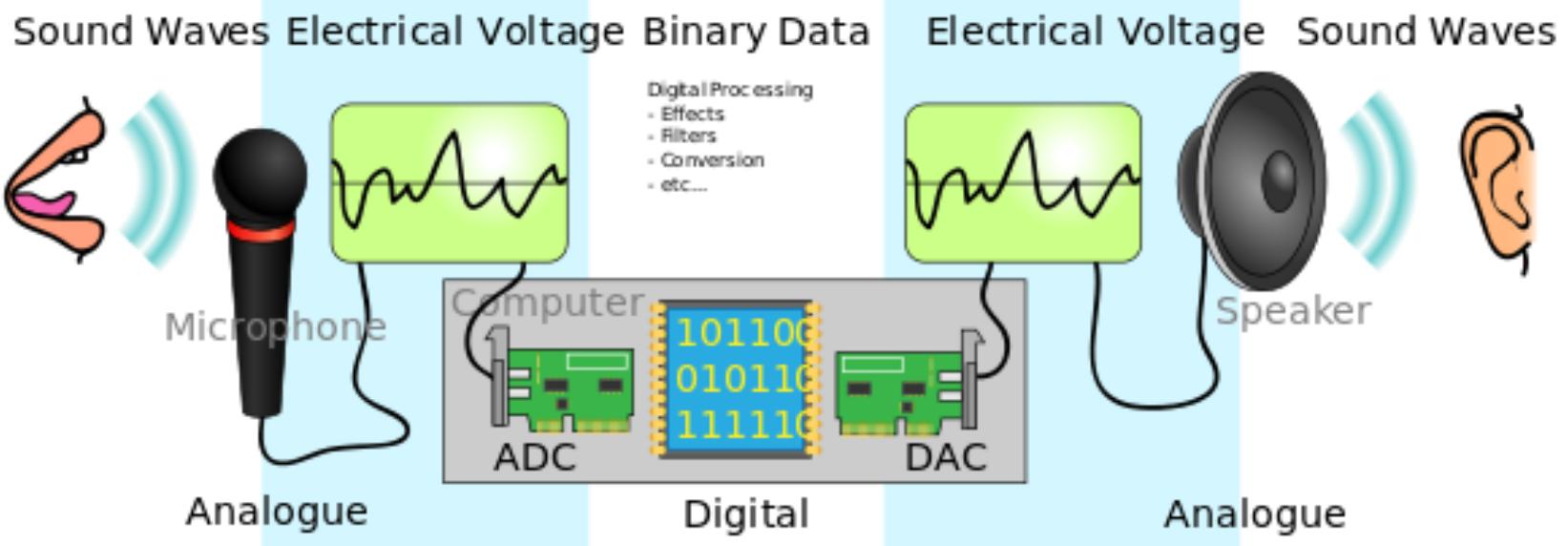
University
of Glasgow

UESTC1008: Microelectronic Systems

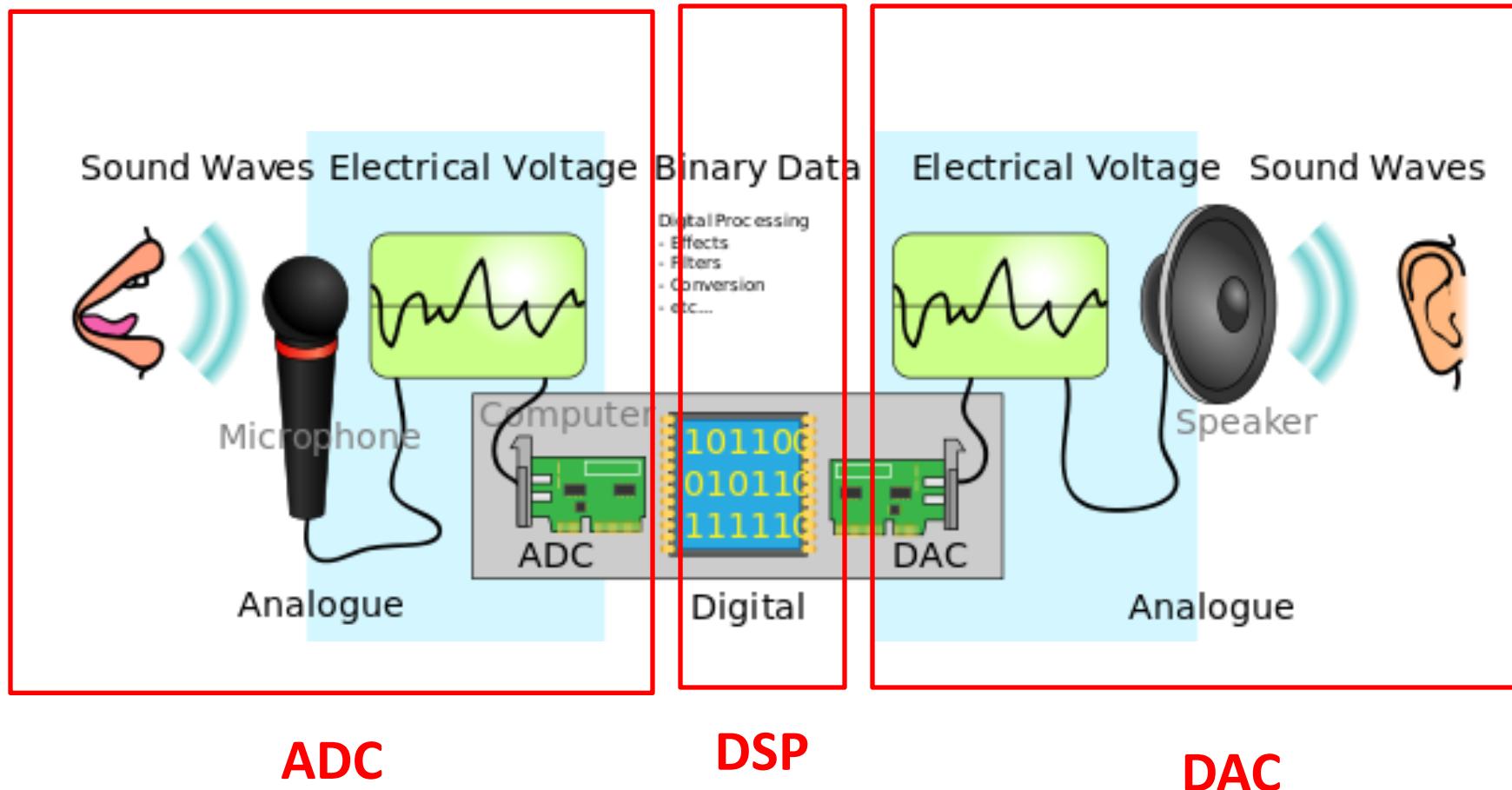
Analogue to Digital Conversion (ADC) Lecture 7

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ADC and DAC Conversions



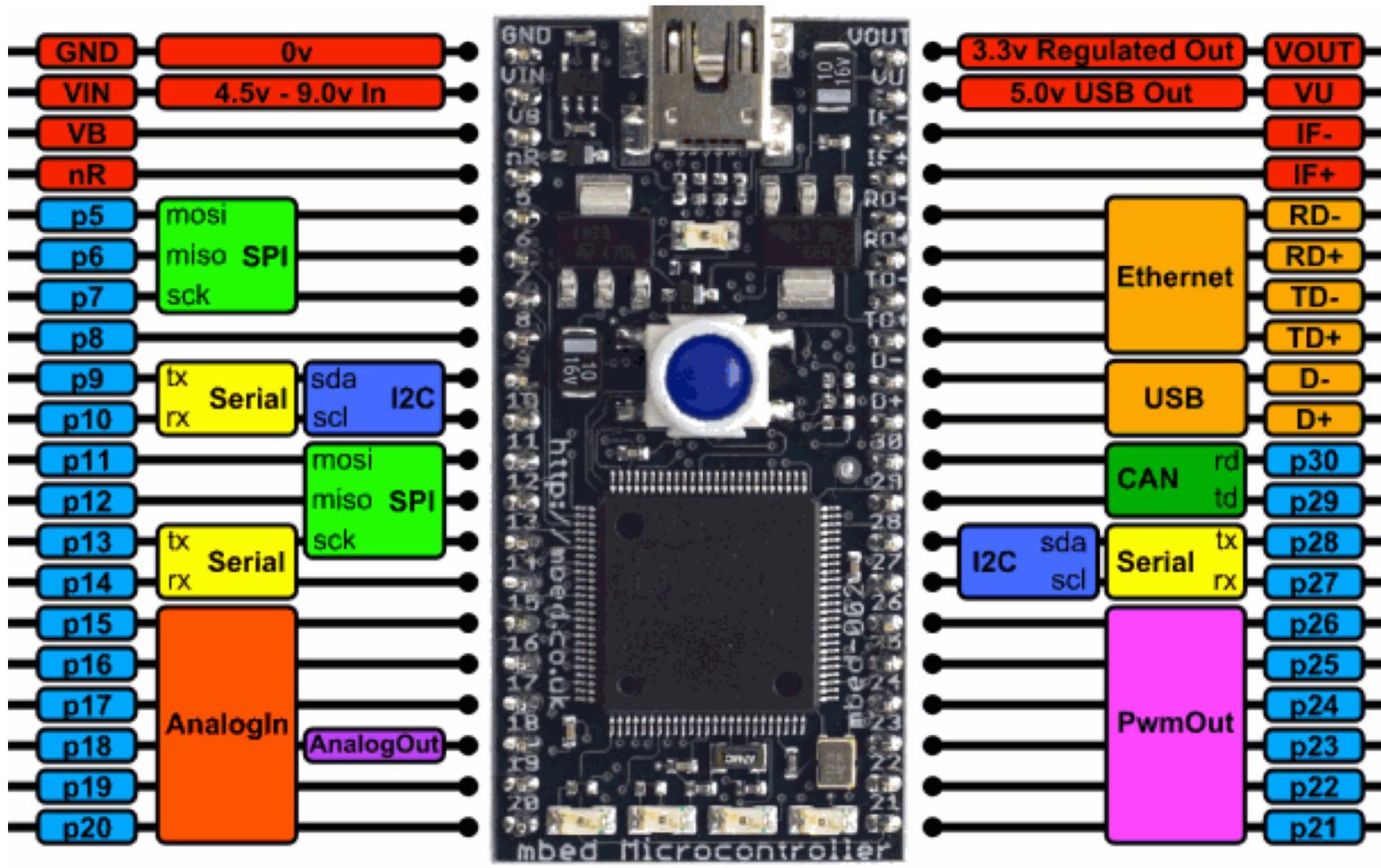
ADC and DAC Conversions



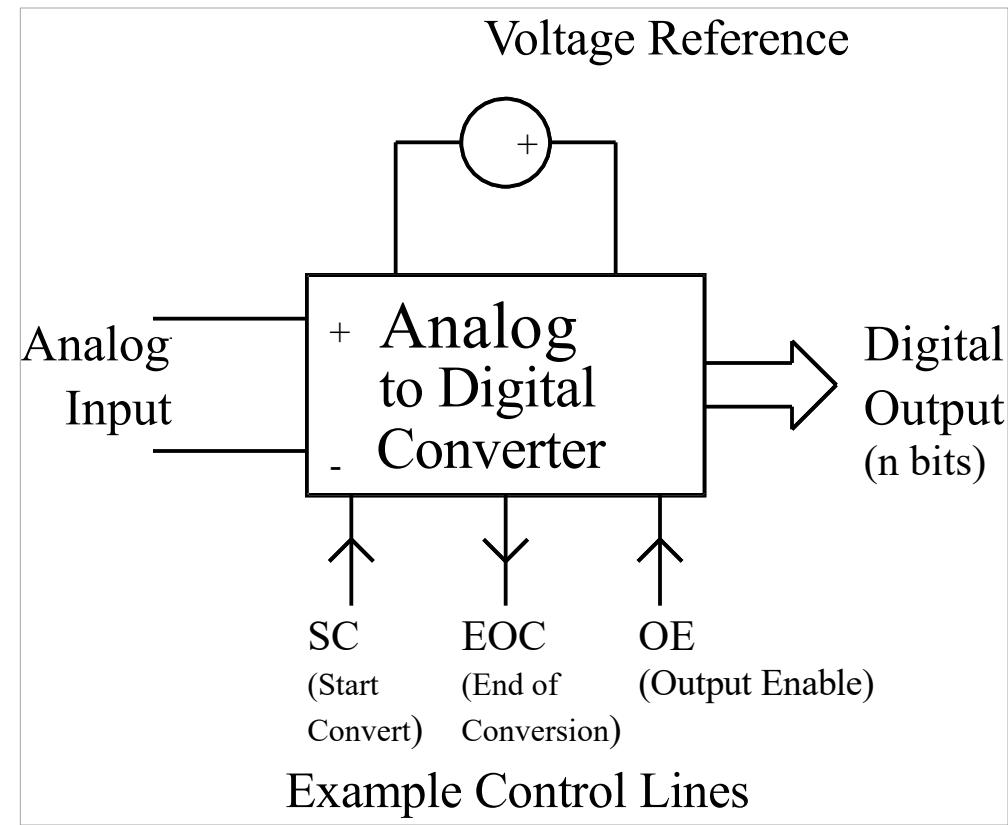
ADC

- As mentioned before, most sensors of temperature, sound, and acceleration have analog outputs. However, these analog outputs have to be converted into digital signals before they can be stored or used in calculations by the microcontroller.
- Analog signals are converted into digital representations with a **resolution** and a **rate** determined by the Analog to Digital Converter (ADC)
- An ADC is a circuit whose digital output is proportional to the analog input
- Effectively, an ADC measures the input analog voltage, and gives a binary output proportional to the size of the input signal
- The input range of the ADC is usually determined by the value of a voltage reference

mbed – ADC and DAC pins

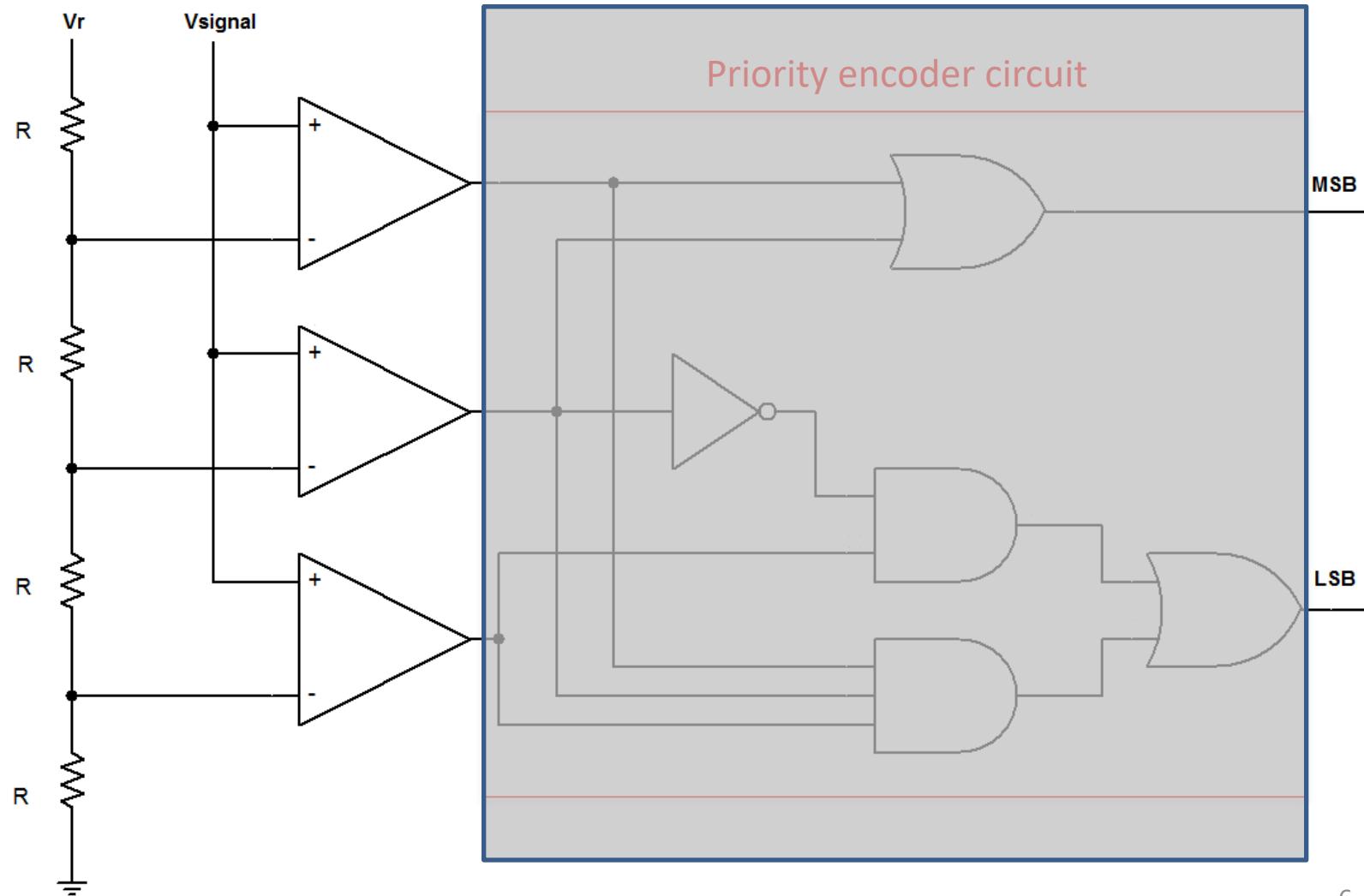


ADC Block Diagram



- The conversion process is started by a digital input called **SC**, start convert
- It takes a finite time to perform the conversion, depending on the clock frequency
- The ADC signals that the conversion is completed via the **EOC**, end of conversion line
- The resulting data can then be written onto the output data bus, when the output enable, **OE** control line, is high

2 bit Flash ADC



ADC

- Many ADCs follow the relation where:

$$D = \left\lfloor \text{floor} \left(\frac{V_i}{V_r} \times 2^n \right) \right\rfloor_{\text{Base2}}$$

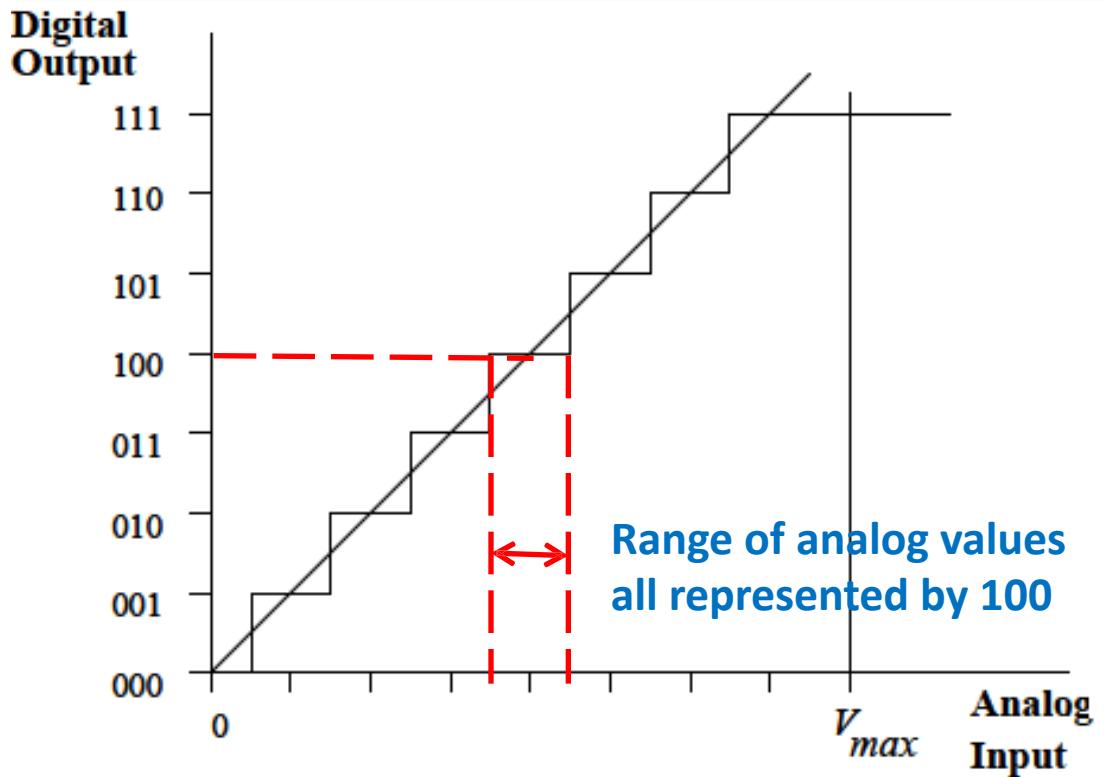
- D is the digital output value
 - Note that D will never be equal to $\text{base}_2(2^n)$ as the range of the ADC is limited to $2^n - 1$
- V_i is the analog input voltage
- V_r is the reference voltage
- n is the number of bits in the converter output
- How many voltage comparators are needed for a 12-bit ADC?

$$N_{\text{comparators}} = 2^n - 1$$

ADC

- The output binary number is an integer, and for an n-bit number can take any value from 0 to $(2^n - 1)$
- The ADC process **rounds** (truncates) the calculation to produce an integer output
- An ADC will have maximum and minimum input values that it converts. The difference is the **range**
 - Often the minimum value is 0 V, so the range is then just the maximum possible input value. Analog input values that exceed the maximum or minimum will likely be digitized as the maximum or minimum values (a limiting or clipping action occurs)

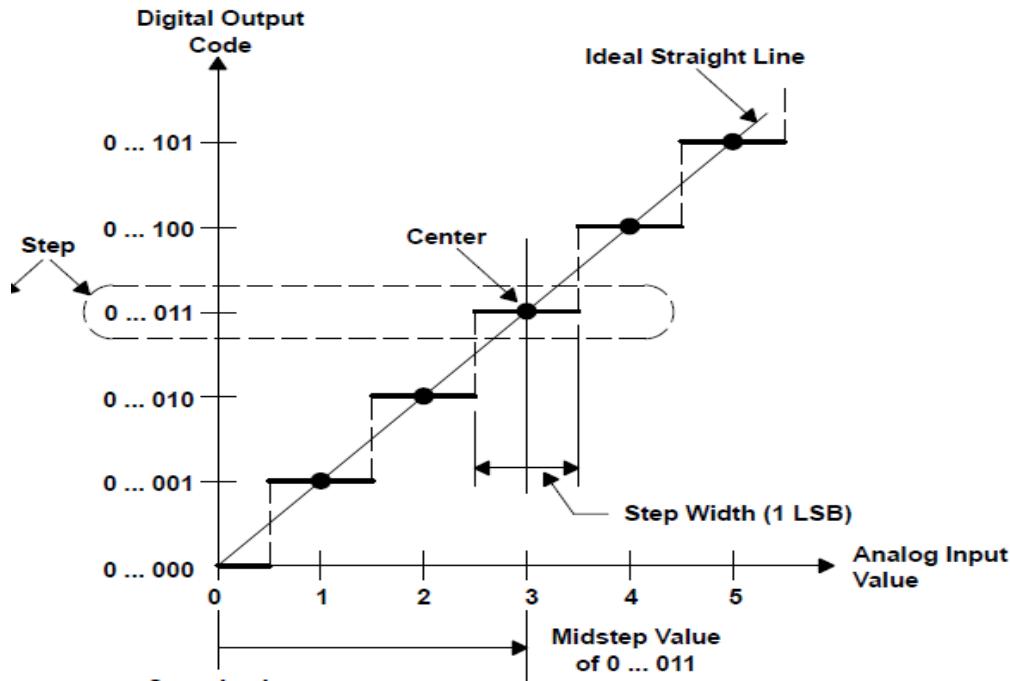
3 bit ADC



As input voltage goes from 0 V to V_{max} , the digital output will step from 000 to 111 or ($2^3 - 1$)

- This shows that in making the conversion, an approximation is involved as any one digital output value has to represent a range of analog input signals
 - For example, if the output value of 100 is precisely correct in the middle of the step, the greatest errors will occur at either end

Error Made by ADC



$$V_{step} = \frac{V_{ref}}{2^n}$$

$$\text{Quantisation Error} = \frac{V_{step}}{2}$$

From Understanding Data Converters, Texas Instruments Application Note

Quantisation Error

- The greatest quantisation error is **one half of the step width**, or half of one least significant bit (LSB) equivalent on the voltage scale.
- To reduce the quantisation error, the “step width” should be narrowed. This can be achieved by increasing the number of bits in the ADC process
 - This increases complexity and cost, and often the time taken to undertake the conversion
- What is the step width and worst case quantisation error?
 - The mbed ADC for STM32L432kc is 12 bit
 - The reference voltage is taken from the regulated 3.6 V supply

Summary Formulas

- The digital output

$$D = \left[\text{floor} \left(\frac{V_i}{V_r} \times 2^n \right) \right]_{\text{Base2}}$$

- Number of voltage comparators

$$N_{\text{comparators}} = 2^n - 1$$

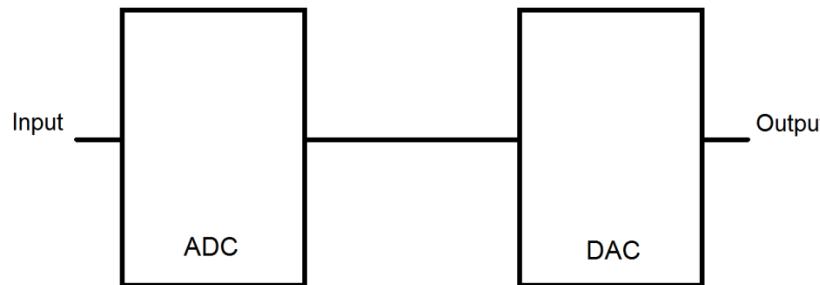
- Step width

$$V_{\text{step}} = \frac{V_{\text{ref}}}{2^n}$$

- Worst quantization error

$$\text{Quantisation Error} = \frac{V_{\text{step}}}{2}$$

Example: An engineer designed a 3-bit ADC where the input signal can be between 0 V to 12 V. The engineer also designed a 3-bit DAC where the output signal is between 0 V to 5 V. The reference voltage (V_r) for the ADC is 12 V and the reference voltage for the DAC is 5 V. The engineer connects the output of the ADC to the input of the DAC, as shown in Figure.

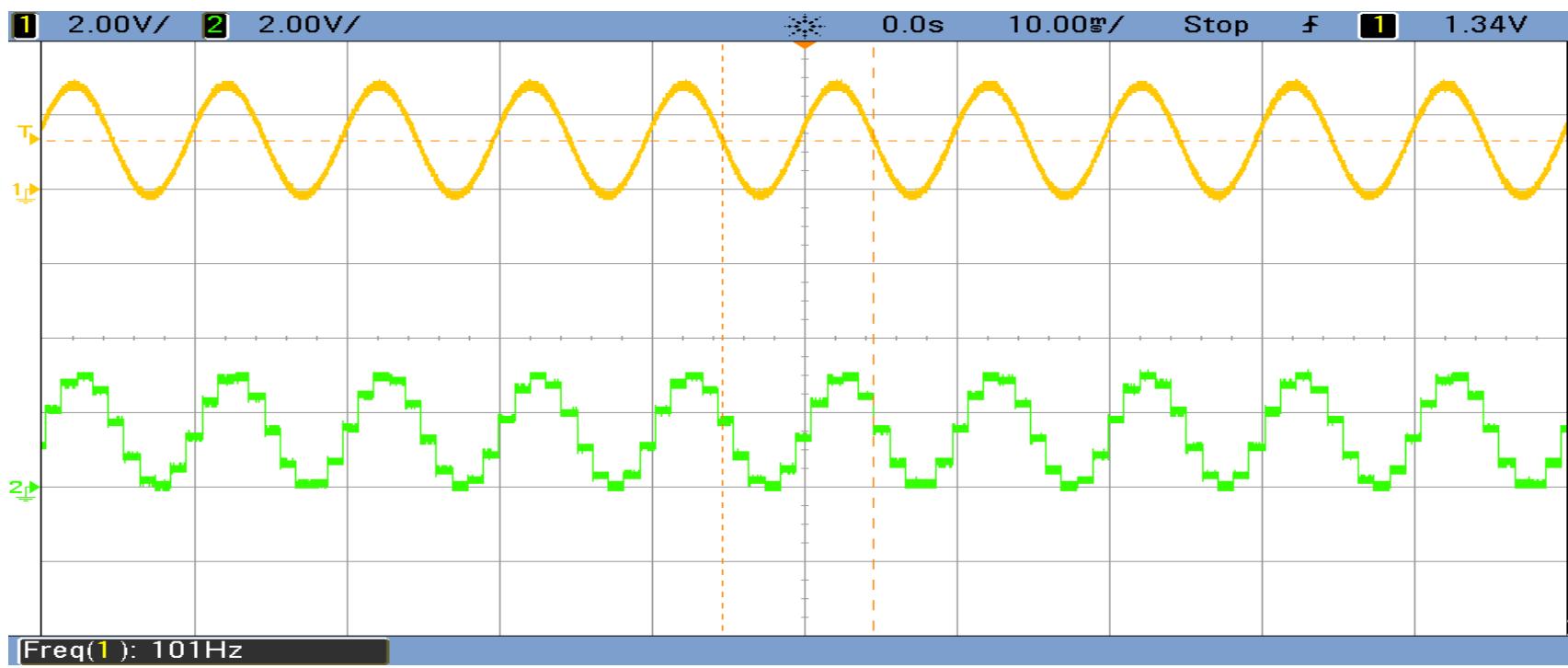
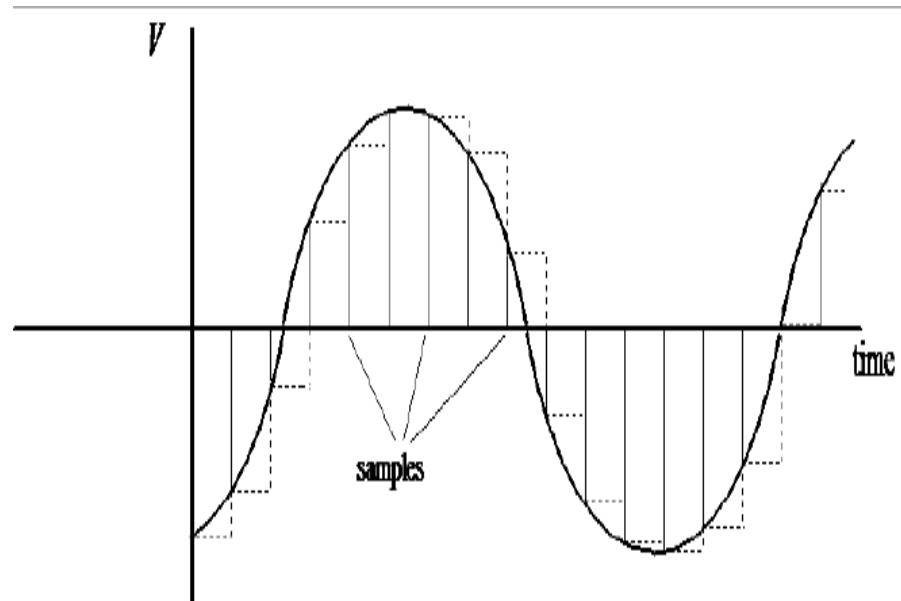


The input voltage to the ADC is 9.3 V.

- a) What is the digital signal that is outputted by the ADC?
- b) How many voltage comparators are used in the design of the ADC?
- c) How large is the quantization error of the ADC?
- d) What is the output voltage of the DAC?
- e) How many bits should the DAC have to obtain a resolution of about 10 mV from the DAC?

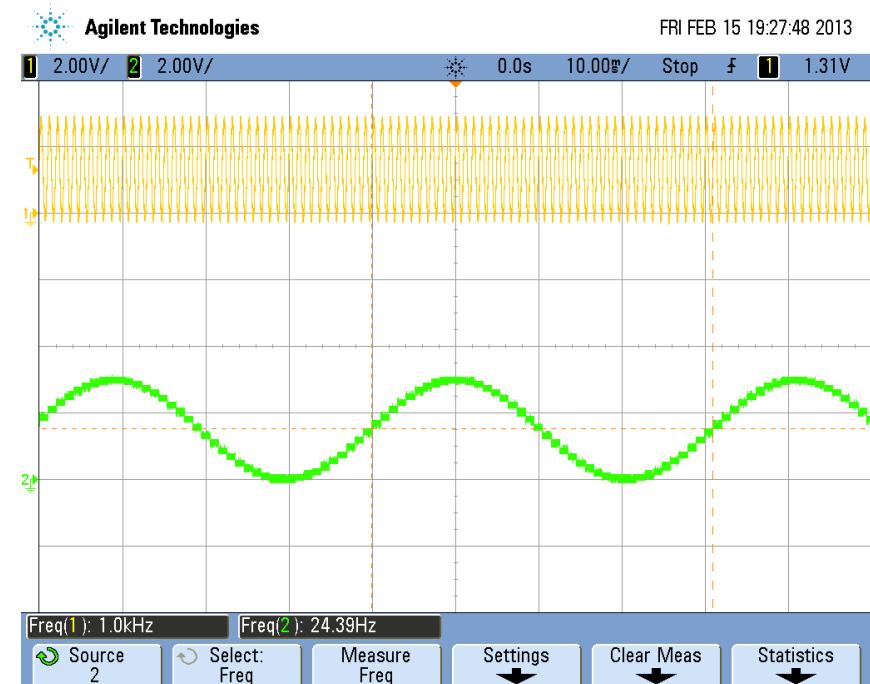
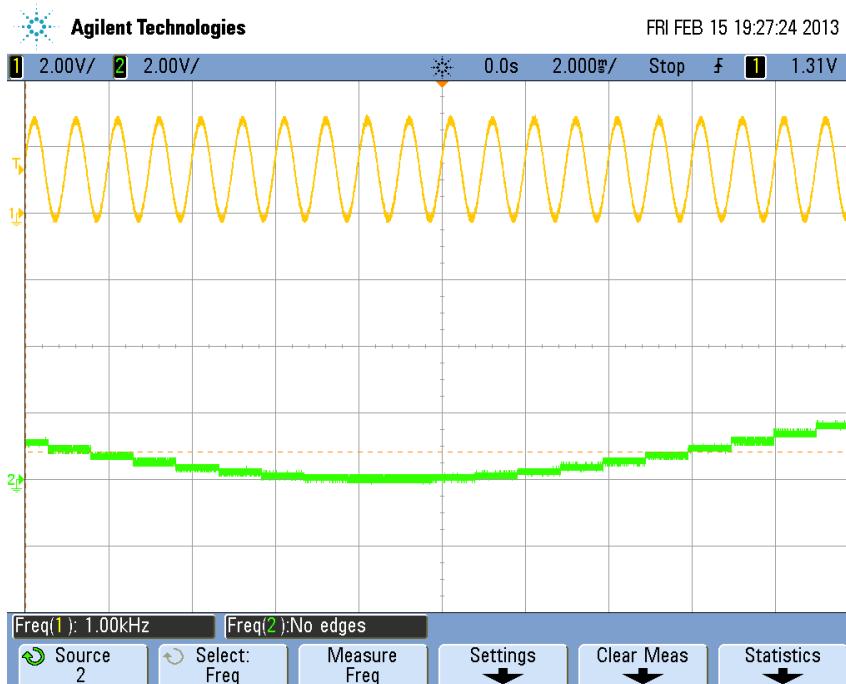
Sample and Hold

- When performing an analog to digital conversion, a “sample” is taken of analog signal and quantized to the accuracy defined by the resolution of the ADC
 - The signal is held, which means that it is stored temporally while the signal is compared to the reference voltage and the digital signal is generated
- Sometimes, the digital signal is generated by averaging the results of several analog samples. The more samples taken, the more accurate the digital data will be as long as the analog signal is not changing
- **Sampling is generally done at a fixed frequency, called the sampling frequency**



Sampling Frequency

The **ideal sampling frequency** depends on the maximum frequency of the signal being digitised. If the sampling frequency is too low, then rapid changes in the analog signal may not be represented in the resulting digital data.



Waveforms showing that undersampling results in the digitised output (lower traces) not representing the input waveforms (upper traces)

Nyquist-Shannon Sampling Theorem

- The Nyquist-Shannon sampling criterion states that the sampling frequency must be at least double that of the highest frequency of interest.
 - However, it is generally agreed that the sampling frequency should be 5+ times the highest frequency found in the analog signal.
 - If the highest frequency that is created when a human speaks is 3.5 kHz, what is the minimum sampling frequency that should be used?
 - The name of the criterion is usually shortened one or the other names – Nyquist criterion or Shannon Criterion.

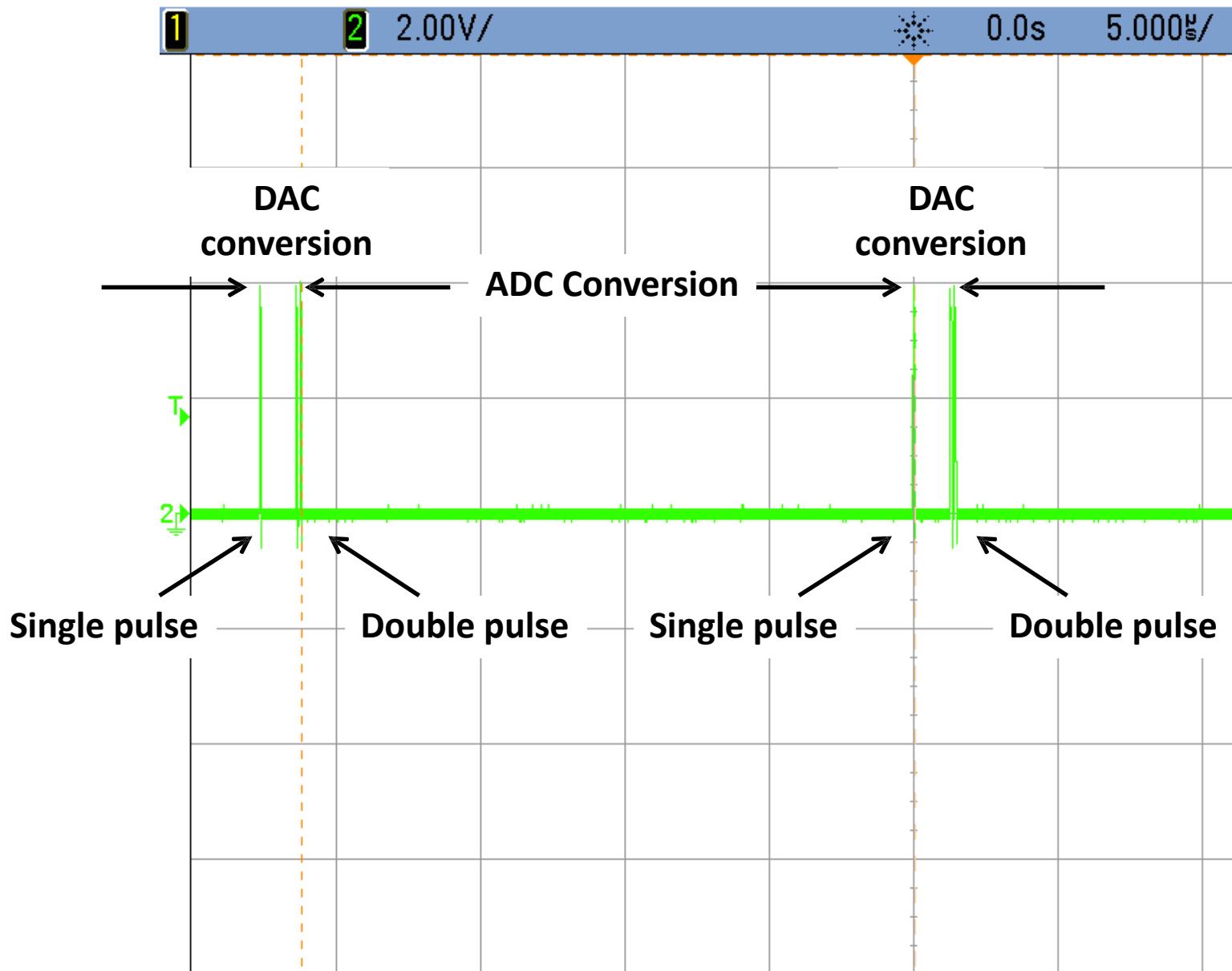
ADC/DAC Program

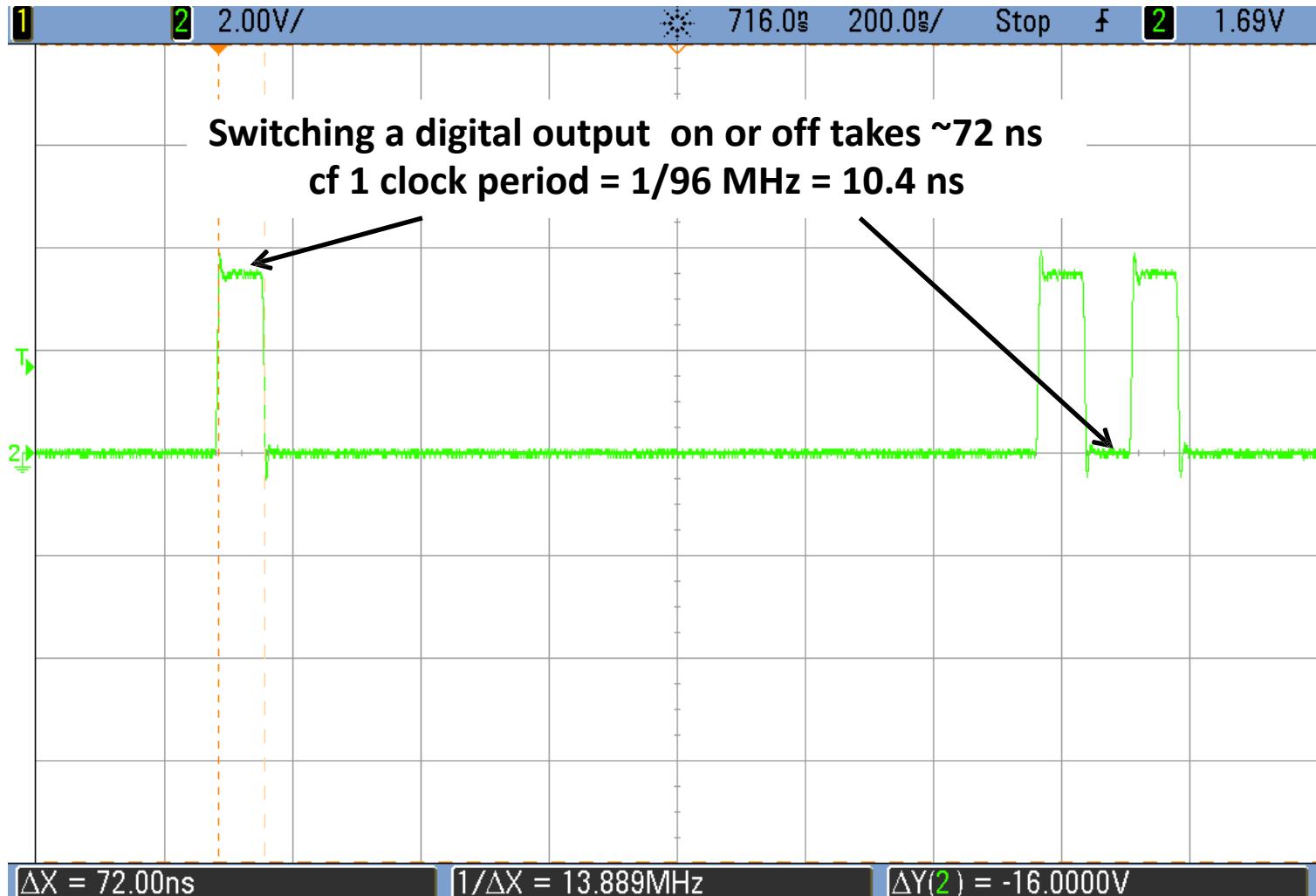
```
/*Program to explore some of the time-related aspects of the mbed DAC and ADC/
#include "mbed.h"

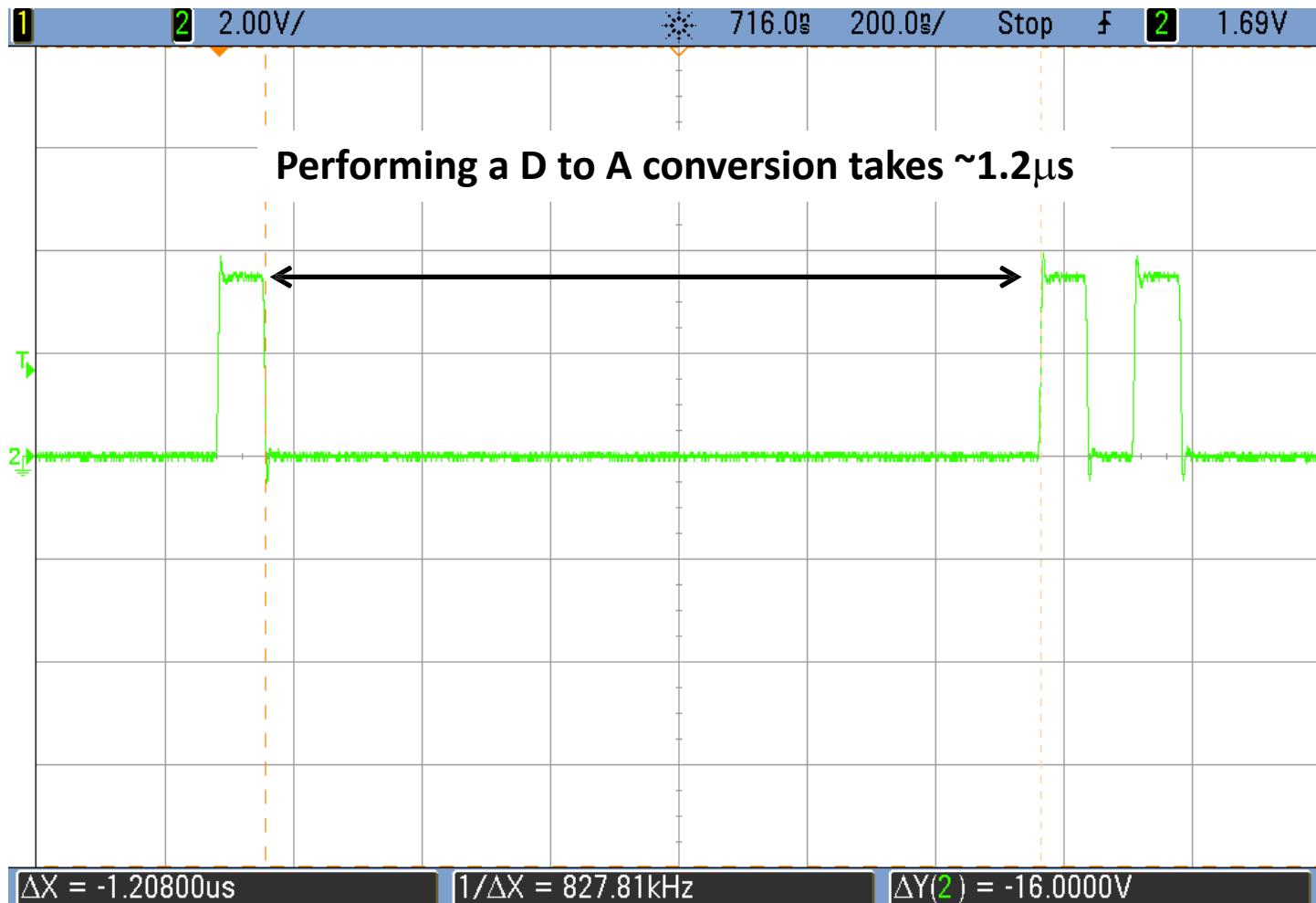
AnalogOut Aout(A4);
AnalogIn Ain (A6);
DigitalOut test(D3);
float ADCdata;

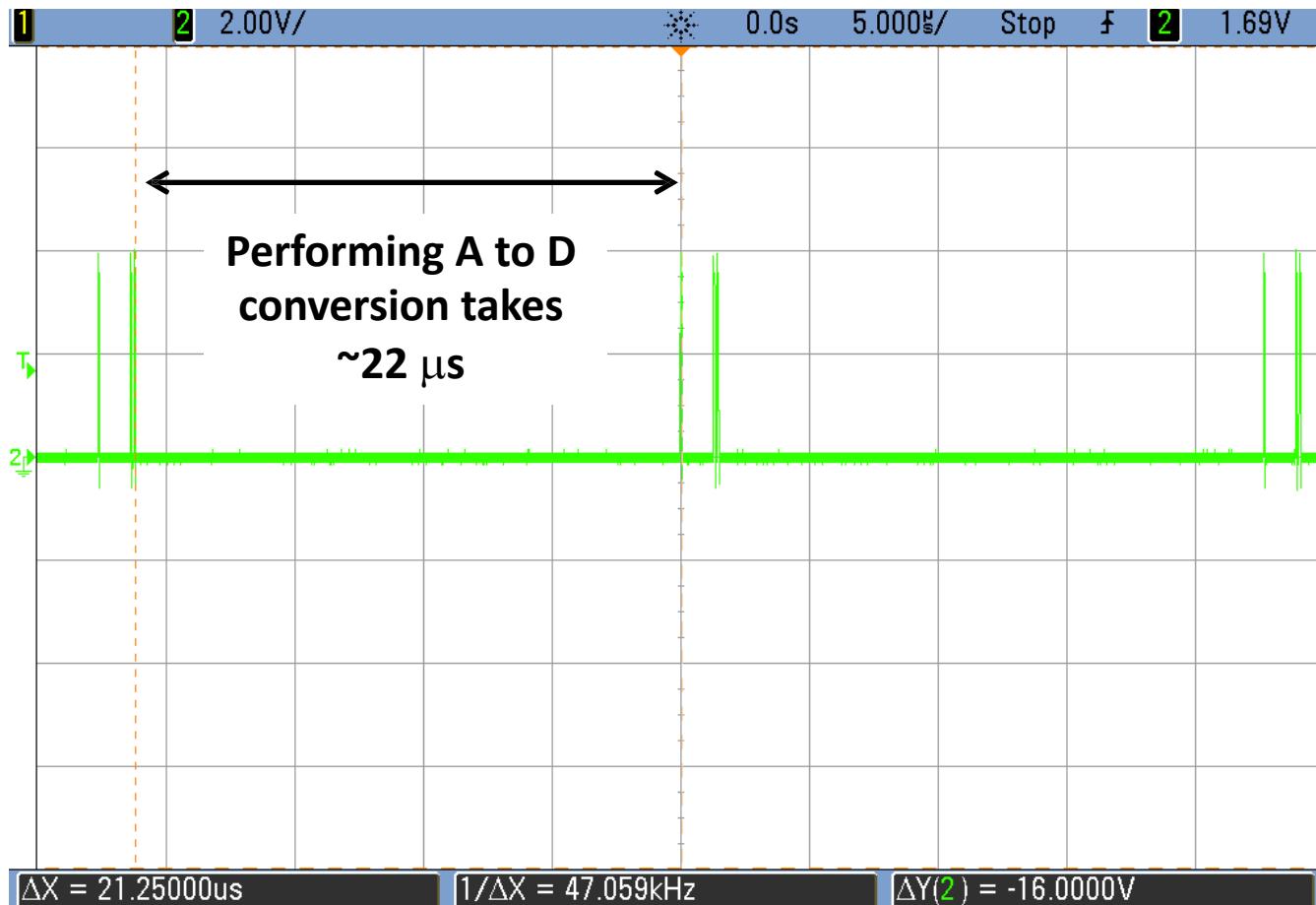
int main(){
    while(1){
        ADCdata=Ain; //Perform an ADC conversion
        test=1;
        test=0;      //1 pulse on D3 shows end of the ADC conversion
        Aout=ADCdata; //Perform a DAC conversion
        test=1;
        test=0;
        test=1;      //2 pulses on D3 show end of the DAC conversion
        test=0;
    }
}
```

Timing issues and consequences







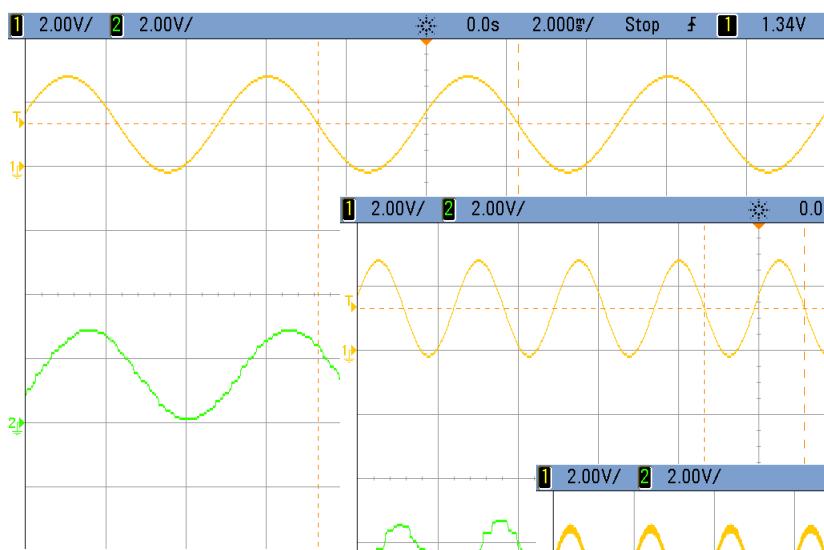


Sampling rate

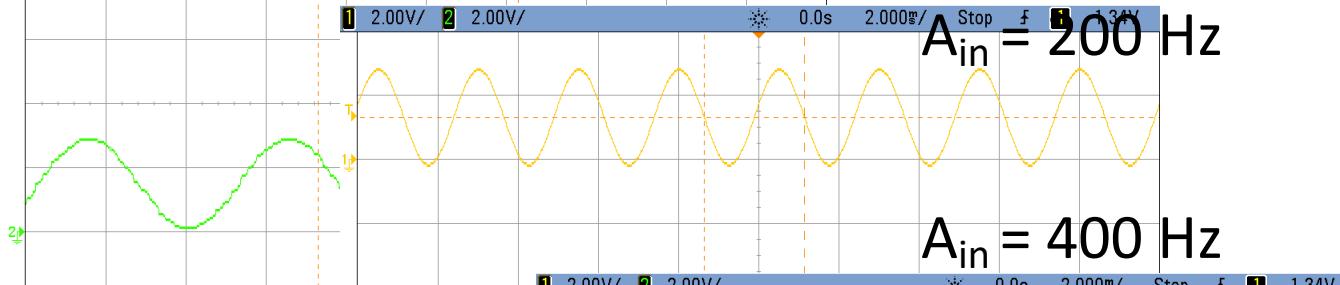
```
/*Program to explore some of the time-related aspects of the mbed DAC and ADC/
#include "mbed.h"

AnalogOut Aout(A4);
AnalogIn Ain (A6);
DigitalOut test(D3);
float ADCdata;

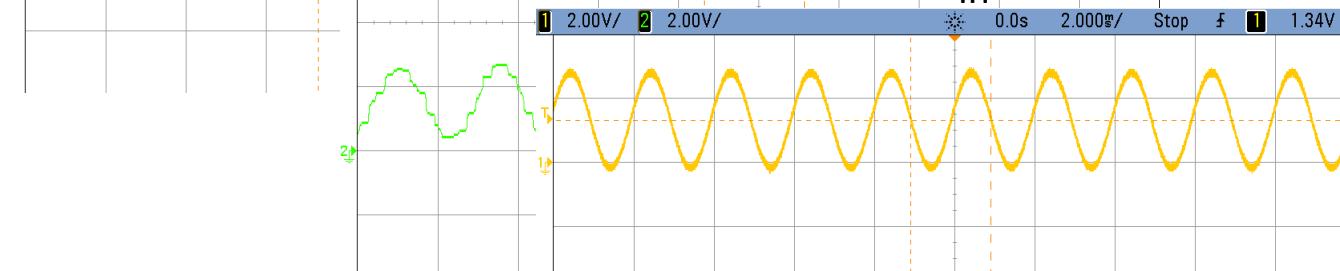
int main(){
    while(1){
        ADCdata=Ain; //Perform an ADC conversion
        test=1;
        test=0; //1 pulse on p5 shows end of the ADC conversion
        Aout=ADCdata; //Perform a DAC conversion
        test=1;
        test=0;
        test=1; //2 pulses on p5 show end of the DAC conversion
        test=0;
        wait (0.001) // shows sampling rate
    }
}
```



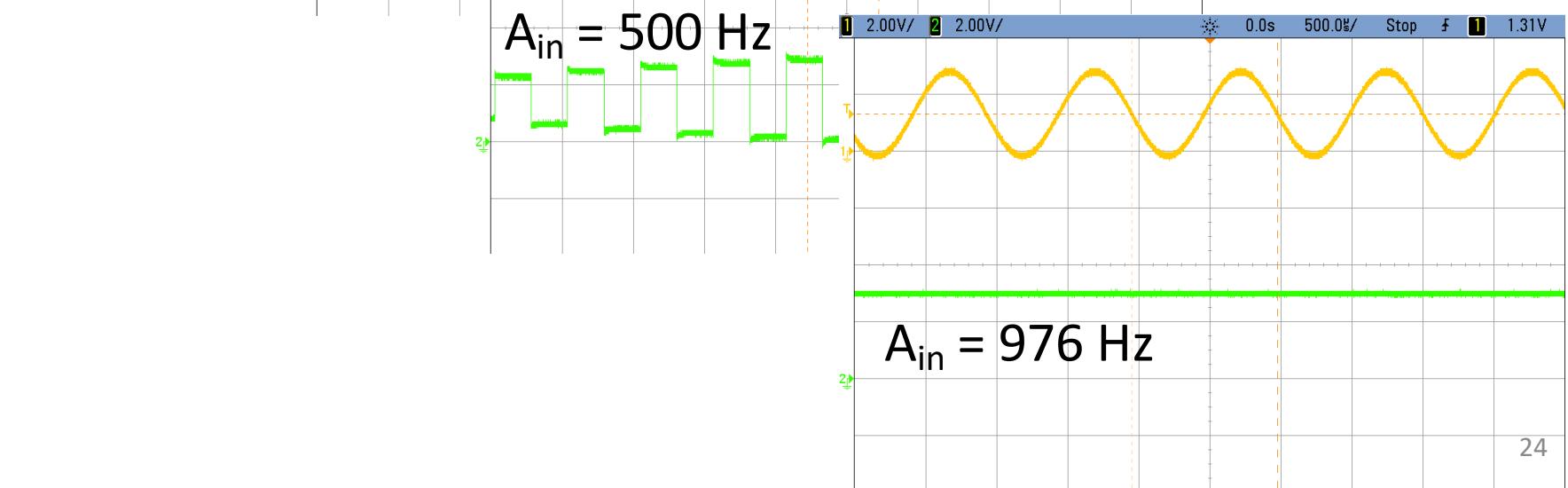
wait = 1ms
Maximum frequency < 500 Hz



$A_{in} = 400 \text{ Hz}$



$A_{in} = 500 \text{ Hz}$



$A_{in} = 976 \text{ Hz}$

`wait = 0 ms.` What is Nyquist frequency ?

Looks ~ 44 kHz.

Standard audio CDs are sampled at played back at 44.1 kHz, to adhere to Nyquist sampling criteria as it relates to human auditory system which extends to ~ 20 kHz. Coincidence?