UESTC 3003: Electronic System Design

Static Errors
Lecture 2.2: OpAmp Imperfections

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ESD3

- Imperfections in opamp modelled as Perfect Opamp + sources
- Performance of system is measured against a specification

• ESD3 is concerned with the methods used to connect the two to produce a design which can be proven to meet specification

CHEAPLY.

System Engineering : Signal Conditioning

- In **Electronic System Design** we will consider how to provide the best possible input signals to the system. This means signals that are:-
  - **Accurate**: providing the most accurate signal to the system
  - **Clean**: providing the system with the cleanest, lowest noise signal
  - **Immune:** (from disturbance): signals remain accurate and clean when there is interference
- Our course will explore how to deal with low level signals and condition them for the system to use (probably in a digital process)

"Pray, Mr. Babbage, if you put into the machine wrong figures, will the right answers come out?" ... I am not able rightly to apprehend the kind of confusion of ideas that could provoke such a question.
— *Charles Babbage, Passages from the Life of a Philosopher* Source Wikipedia

Imperfect Opamps

- Perfect Opamp: ⇨ $V_{OUT} = \infty\left(V_{IN}(+) - V_{IN}(-)\right)$
- Imperfect Opamp [1]
  - Current flows in inputs
    - **Bias**
    - **Offset**
  - Slow
    - **Bandwidth**
    - **Slew Rate**
    - **Phase margin**
  - O/P has finite impedance (but reduced by feedback)
  - Input voltage error
    - **Offset**
    - **Common-Mode rejection**
    - **Power Supply rejection**
    - **Drift (Time / Temperature)**

For a more detailed analysis read:

"Opamps for Everyone" Chapter 11

[1] "*Users Guide to Applying and Measuring Operational Amplifier Specifications*" Ray Stata Analog Devices Application Note AN-356

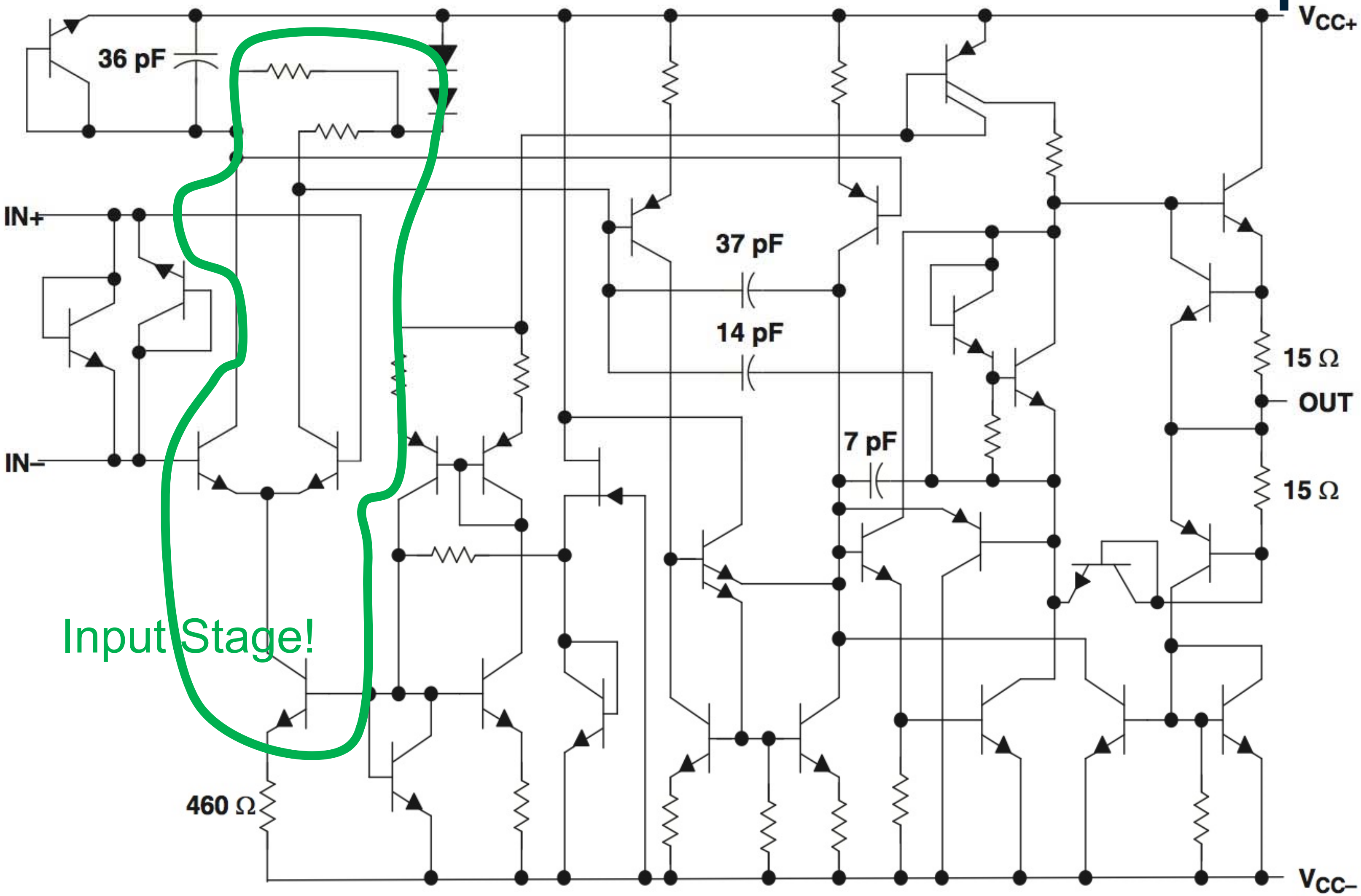
How to design with imperfect components…

- Specify (sub)system
  - Function (e.g. Gain of +10)
  - External connections (e.g. source voltage range, impedance…)
  - Performance (e.g. scale and offset error, bandwidth, power dissipation..)

1. **Naïve design for basic function**
   - Full design including choice of opamp, component values…
   - Hint: Start with cheap components then work upwards
2. **Analyse circuit for sources of error**
   - Identify dominant errors
   - Remove/reduce the dominant errors
3. **Optimise your design…**
   - Best performance….
   - Minimum cost

- **Specification** and **Analysis** are the keys to good design.

NE5532: Where is the input stage ?



Component values shown are nominal.

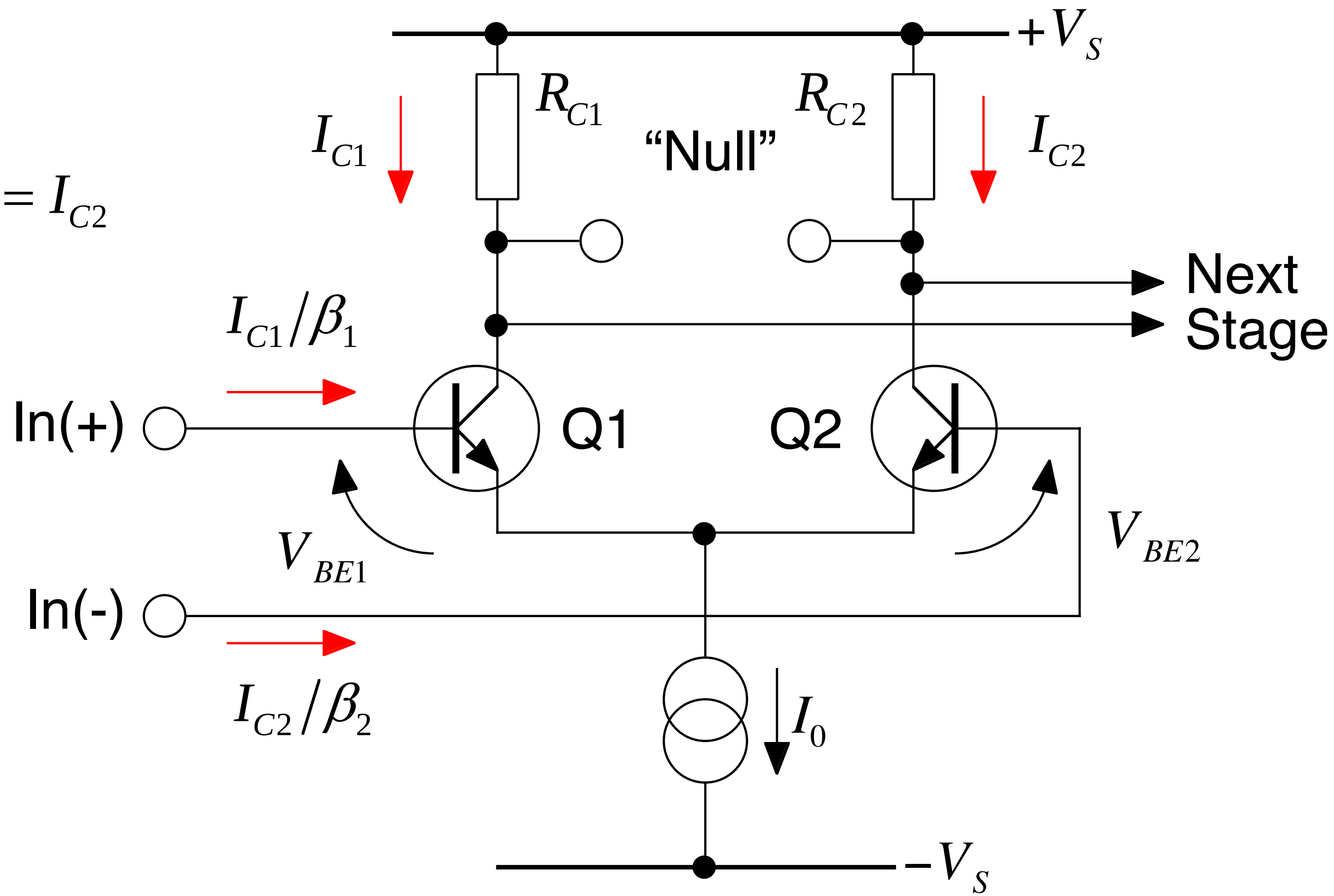
Input Stage

Q1 ≡ Q2

$V_{BE1} = V_{BE2} \therefore I_{C1} = I_{C2}$

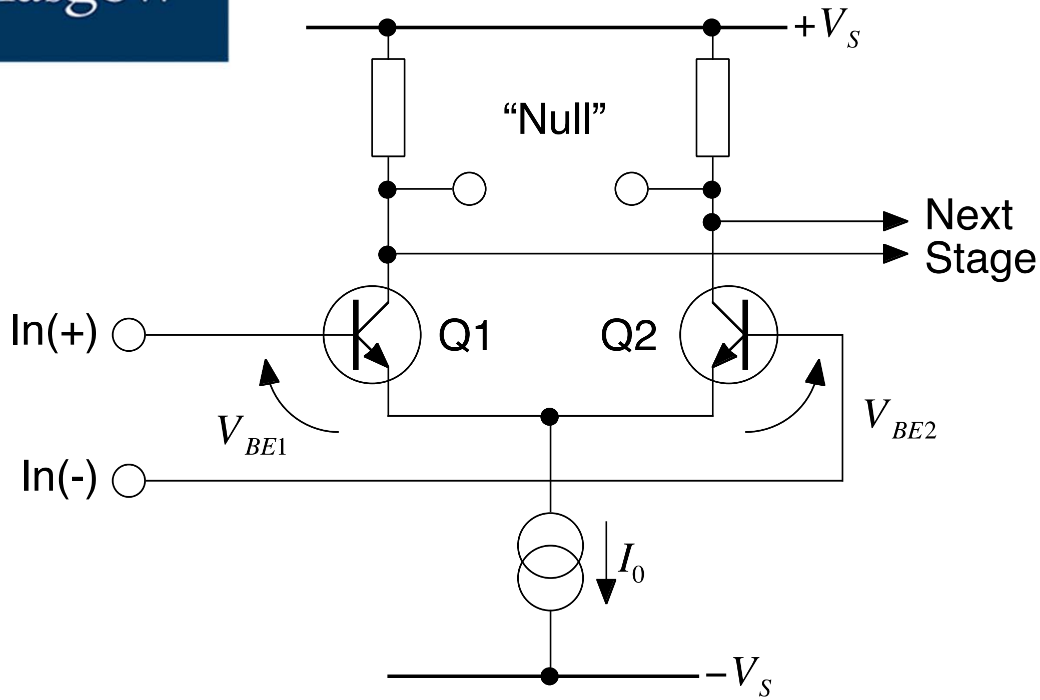
$I_{C1}/\beta_1 = I_{C2}/\beta_2$

In(+)=In(-)
(virtual earth)



See, for example
"The Monolithic Operational Amplifier: A Tutorial Study"
National Semiconductor Application Note AN-A

Input Stage



Because of constant current "tail" total collector current is constant

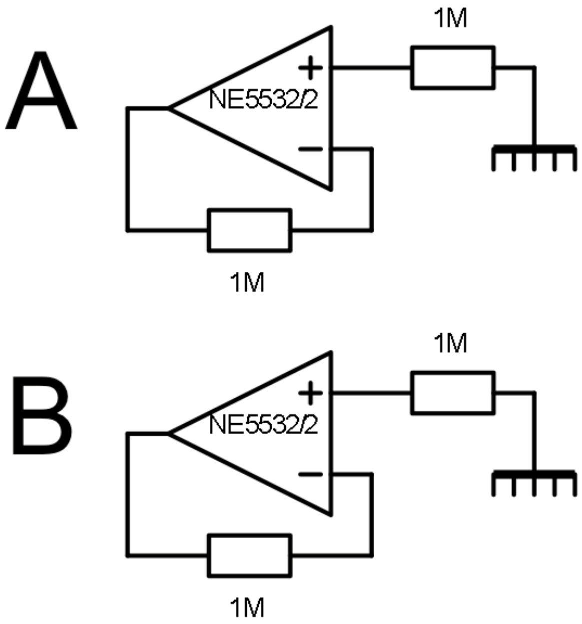
Because of matched components and virtual earth principle both input currents are equal

Input currents are equal and independent of input voltage if negative feedback present; Constant input current

$$Z_{IN} \approx \infty; \quad i_{IN} \neq 0$$

Intellectual Experiment…

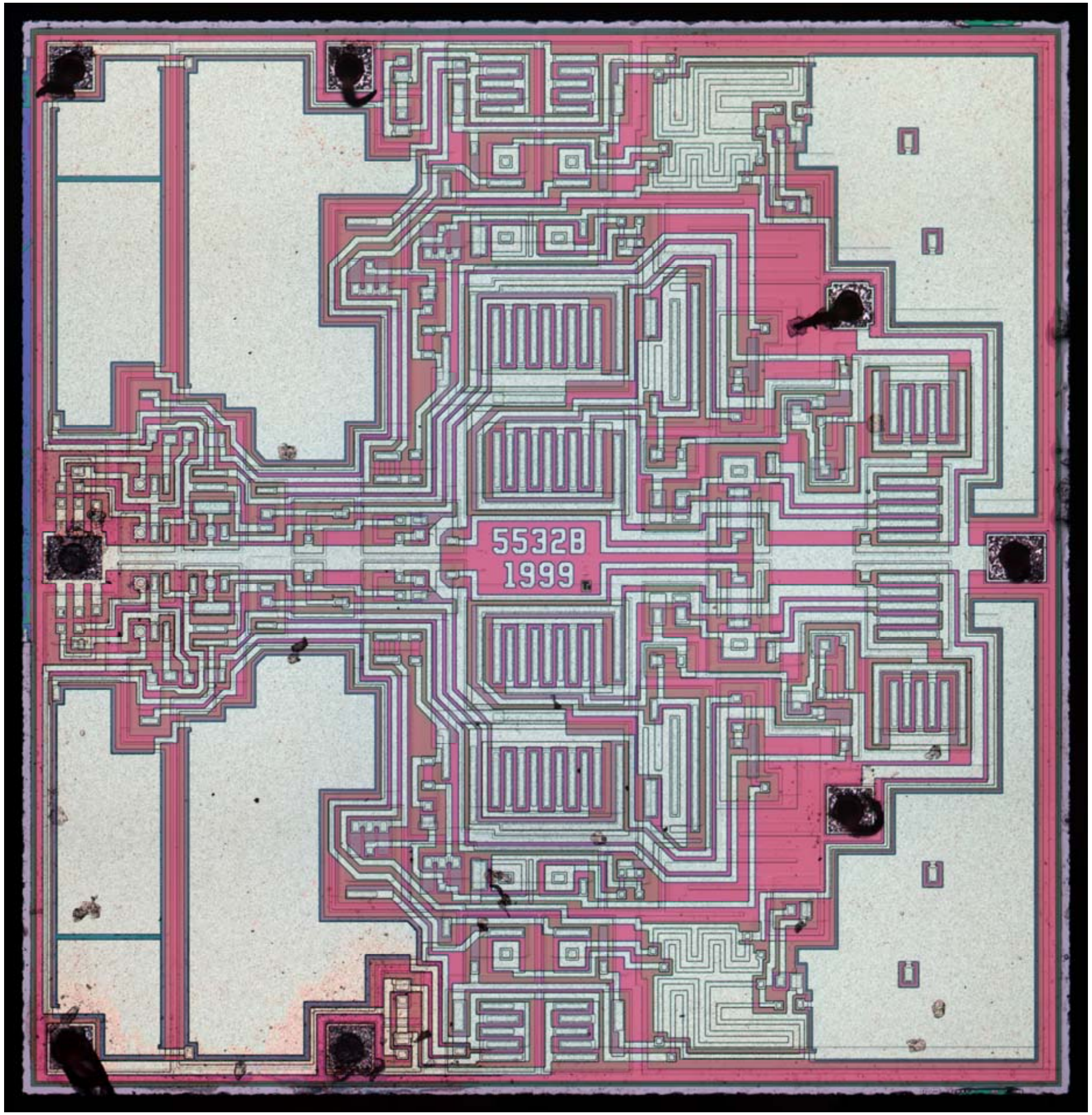
NE5532 has two opamps in one package
Put 1MΩ in series with inputs to measure current…



Input current (nA)	Noninverting	Inverting
Chip 1 Amplifier A		
Chip 1 Amplifier B		
Chip 2 Amplifier A		
Chip 2 Amplifier B		

Wait !!

For a perfect opamp input current = 0 so no voltage across 1MΩ resistors



What is inside the NE 5532?

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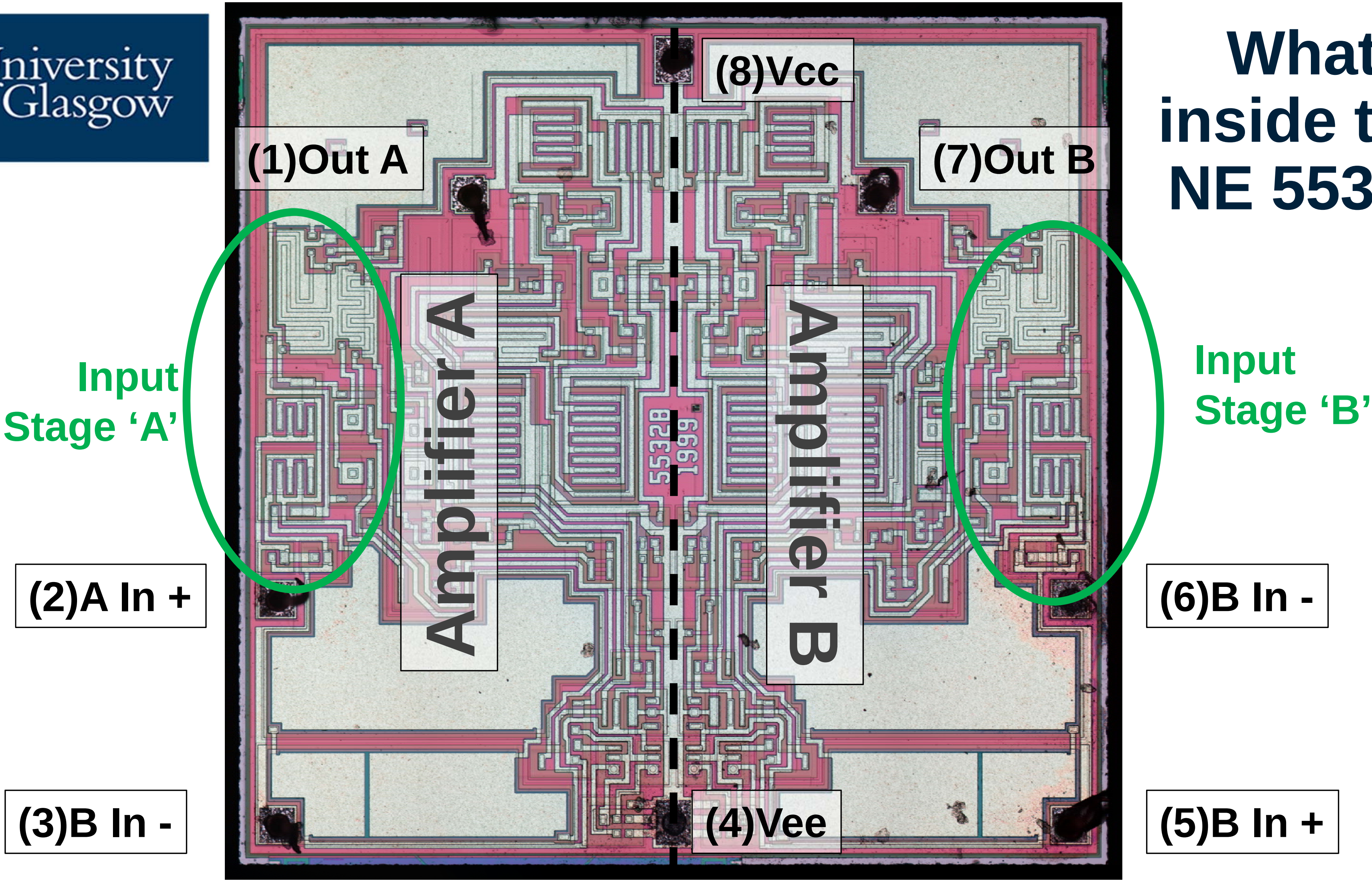
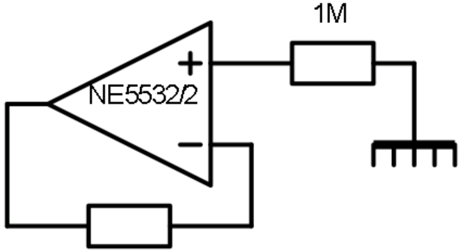


Back to our Experiment…

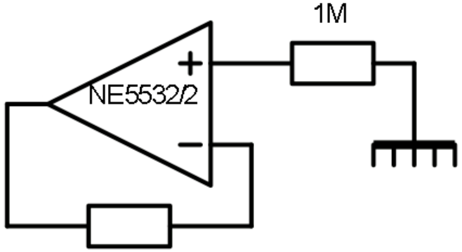
NE5532 has two opamps in one package

Put 1MΩ in series with inputs to measure current…

A



B



For a perfect opamp input current = 0 so no voltage across 1MΩ resistors

Input current (nA)	**Noninverting**	**Inverting**
Chip 1 Amplifier A	180nA	190nA
Chip 1 Amplifier B	230nA	210nA
Chip 2 Amplifier A	350nA	370nA
Chip 2 Amplifier B	420nA	430nA

- **Matching is good** between inputs
- **Matching is good** between amplifiers on the same chip
- **Matching is bad** between chips

Input Errors (1)

- <u>If</u> transistors are identical
  - Differential current depends on difference in inputs

    <Virtual Earth>
  - Input currents (1,2) are equal **= Input Bias Current, I_B**

- Collector resistors are equal
  - Differential O/P Voltage = 0 for Differential I/P Voltage = 0

    (Use multiple stages of differential gain then subtract currents)

$$I_{C1} + I_{C2} \approx I_0 \text{ for all In}(\pm)$$

- Emitter is connected to a constant current source

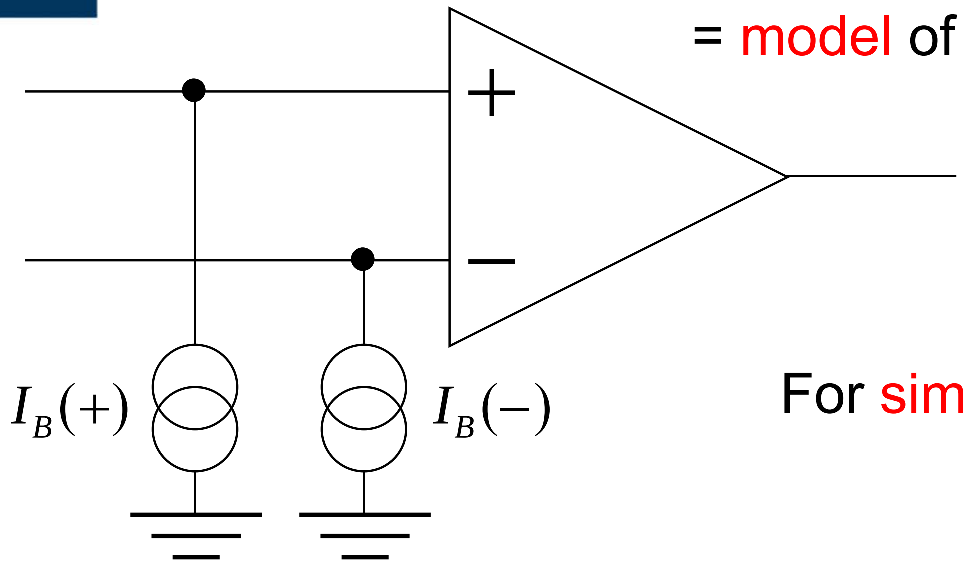
$$\Rightarrow \frac{\partial I_B}{\partial V_{IN}} = 0; \quad R_{IN} = \infty$$

I_B is constant with input voltage

Even ants look different if you look closely!

Imperfect Opamp model (so far)

Perfect Opamp + Current sources
= model of a real opamp



$$I_B(+) \approx I_B(-)$$

For simple opamp. (Not always)

$$I_B \equiv \frac{I_B(+) + I_B(-)}{2} \quad \text{(i.e. the average current)}$$

Min 10fA	Typical	Max ~10μA
1pA (MOSFET)	100pA (JFET)	10nA(Bipolar)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Thank you
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