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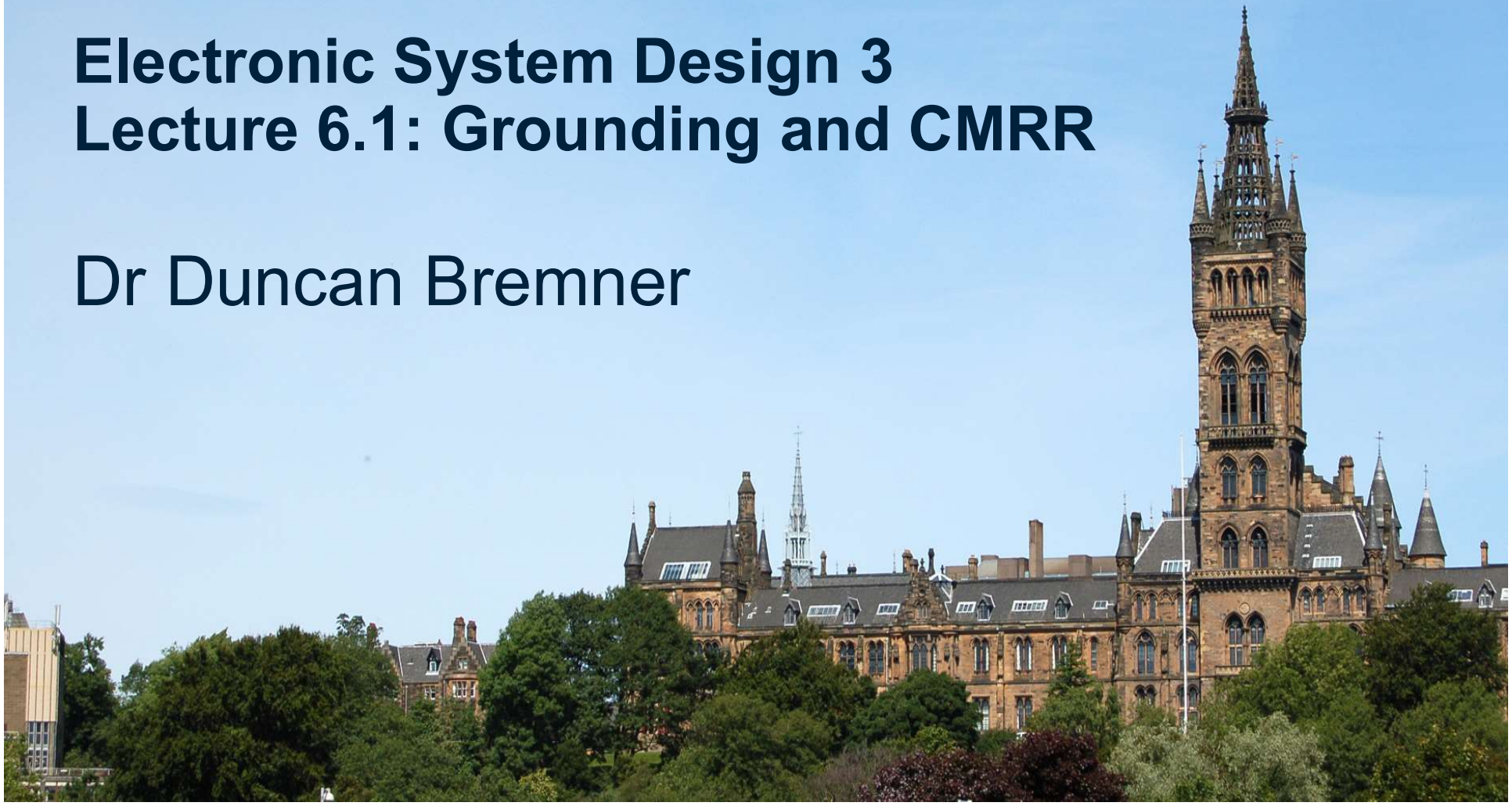
Electronic System Design 3
Lecture 6.1: Grounding and CMRR

Dr Duncan Bremner



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There is no ground.

Electricity leaves the battery, does something useful and then returns to the battery.

It doesn't flow away into a "ground puddle"….

Signals flow on **two** wires

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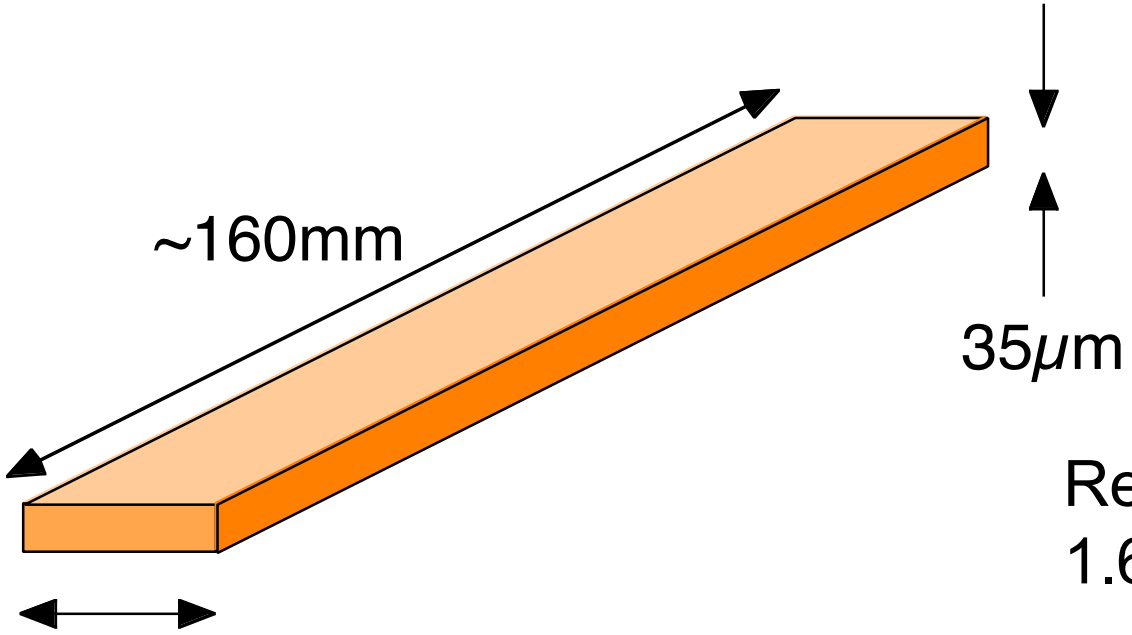
Grounding and Common-Mode Rejection

Have assumed *connections* between components are ideal

Untrue: Wires have significant impedance:
Calculate resistance of PCB track:-



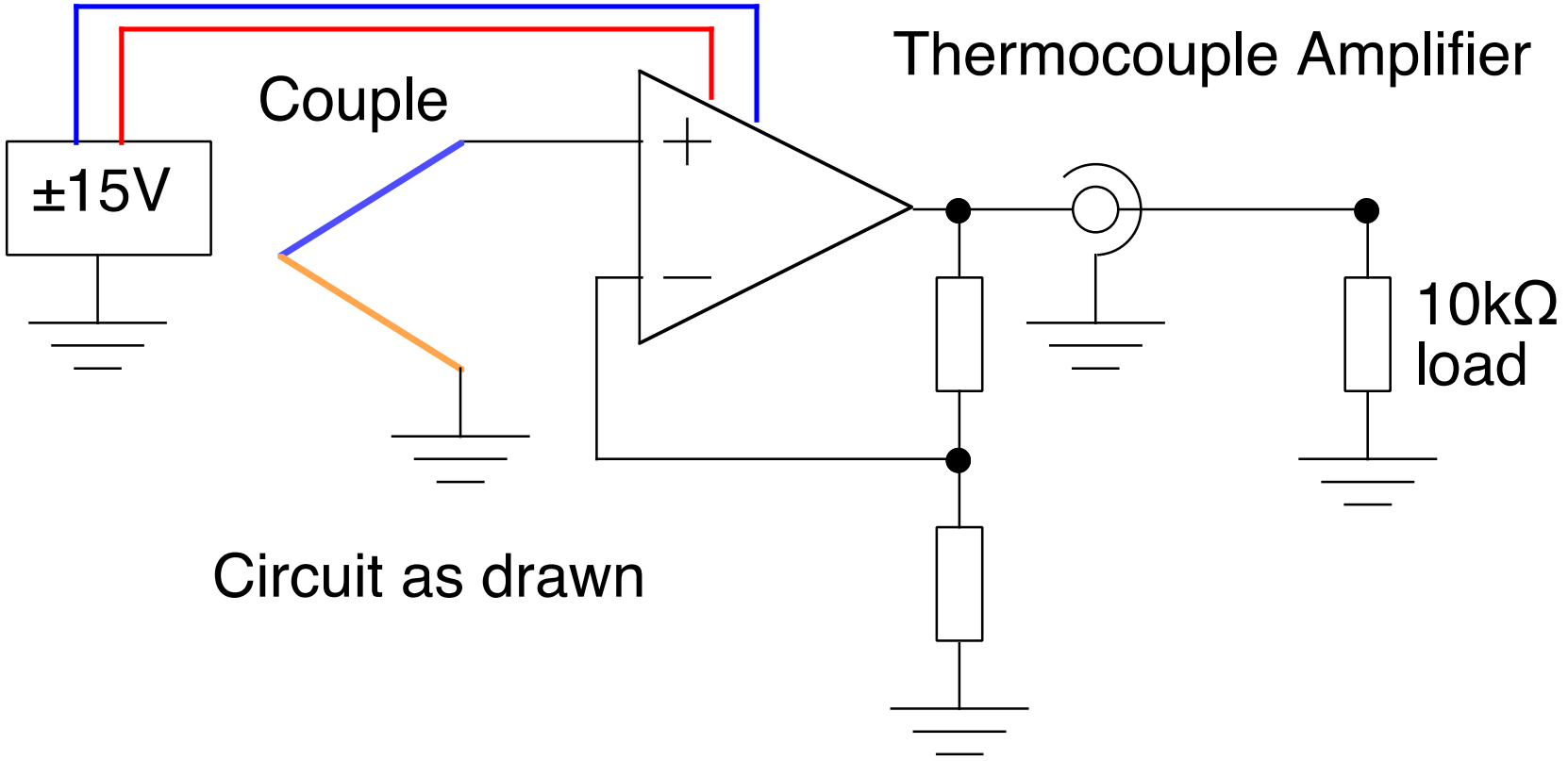
Resistivity of copper
1.69μΩ-cm (20° C)

$$R = \frac{\rho l}{A} \sim \frac{1.69 \cdot 10^{-8}\,\Omega m \cdot 0.16 m}{6.3 \cdot 10^{-4}\, m \cdot 3.5 \cdot 10^{-5}\, m} = 0.123\Omega$$

Common-Mode Signals

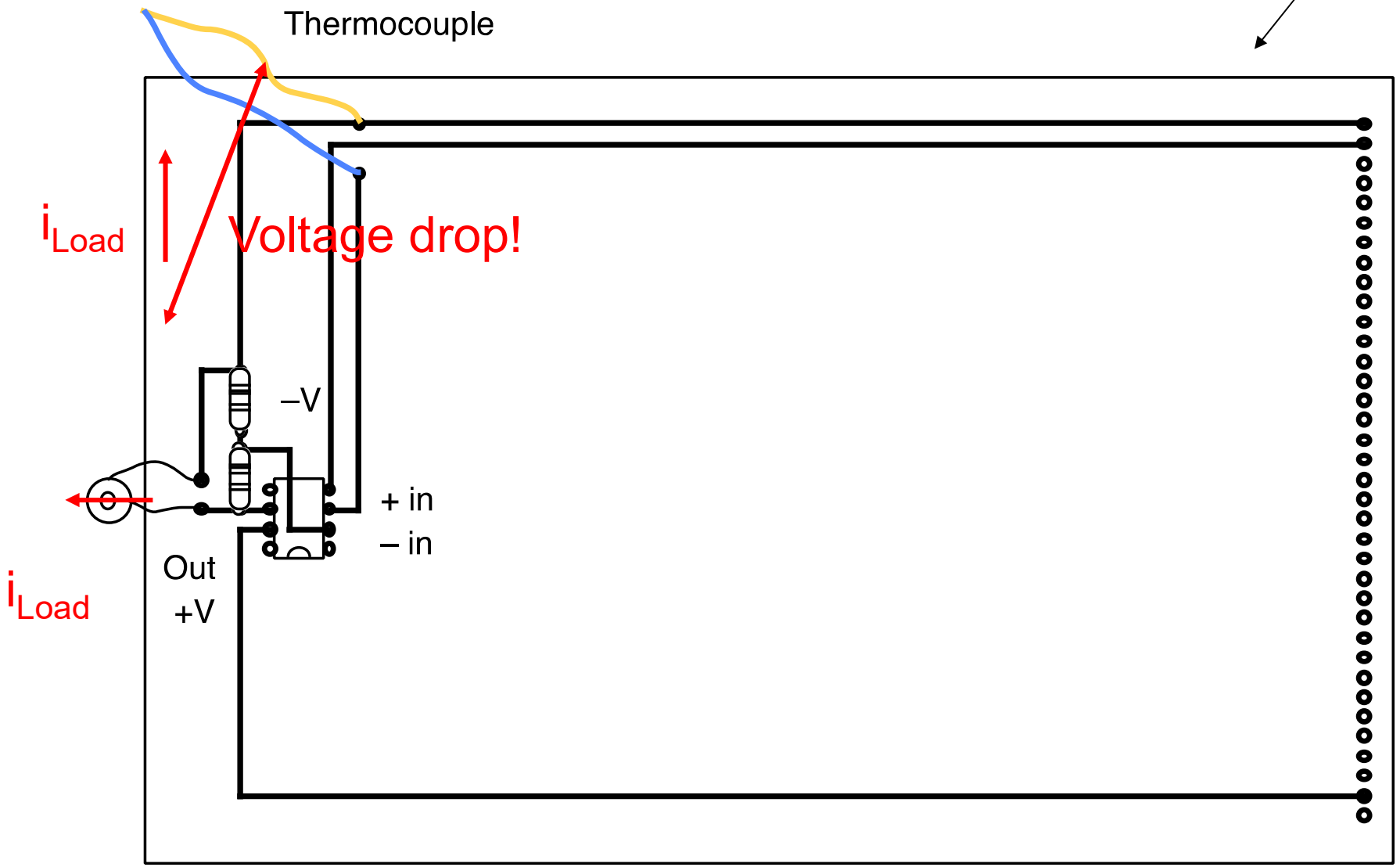
Typical signal wires have resistances ~0.1Ω
Typical signal currents ~ 10V / 10kΩ =1mA -> 100μV!

BAD!!



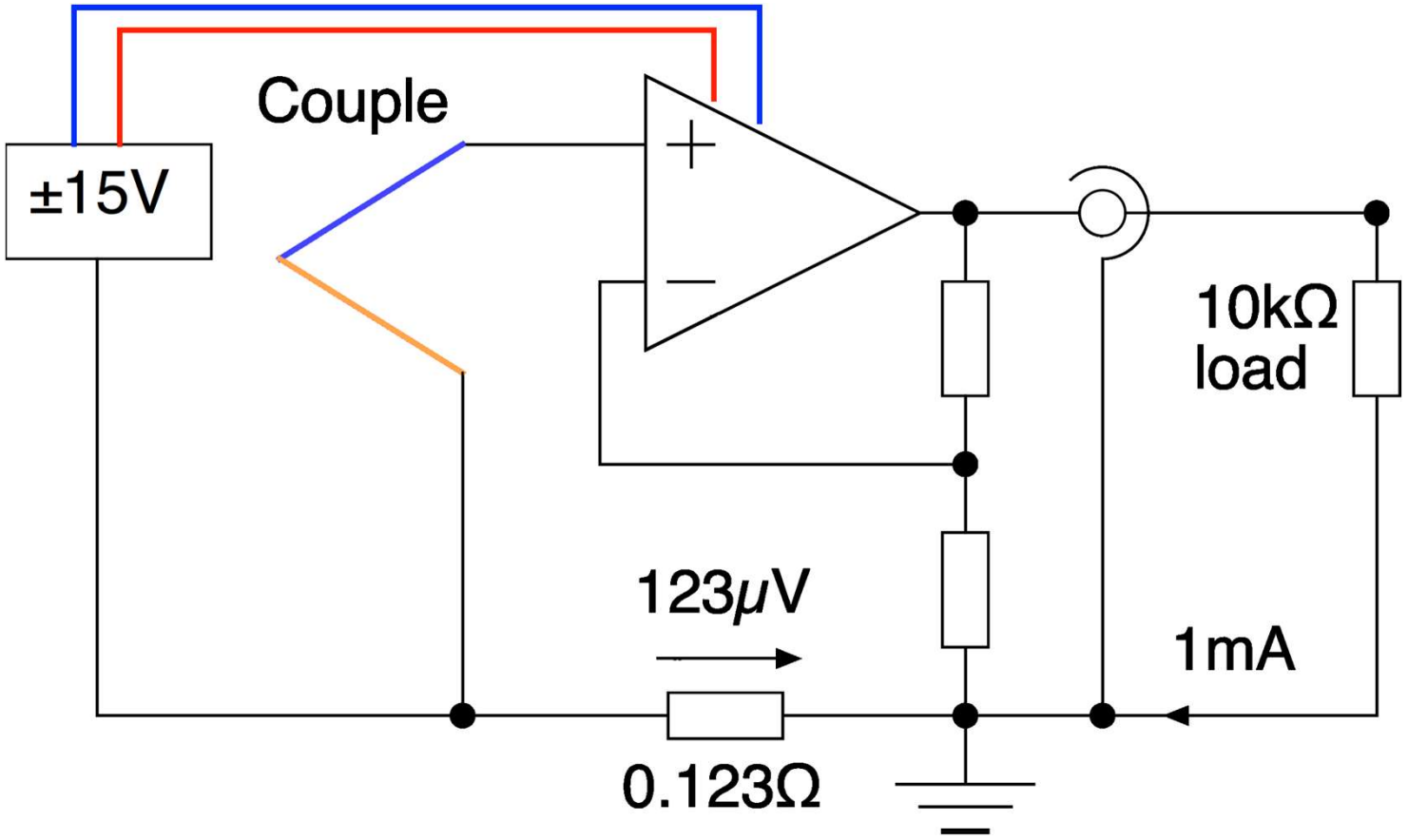
Circuit as drawn

PCB Layout



Common-Mode Signals (2)

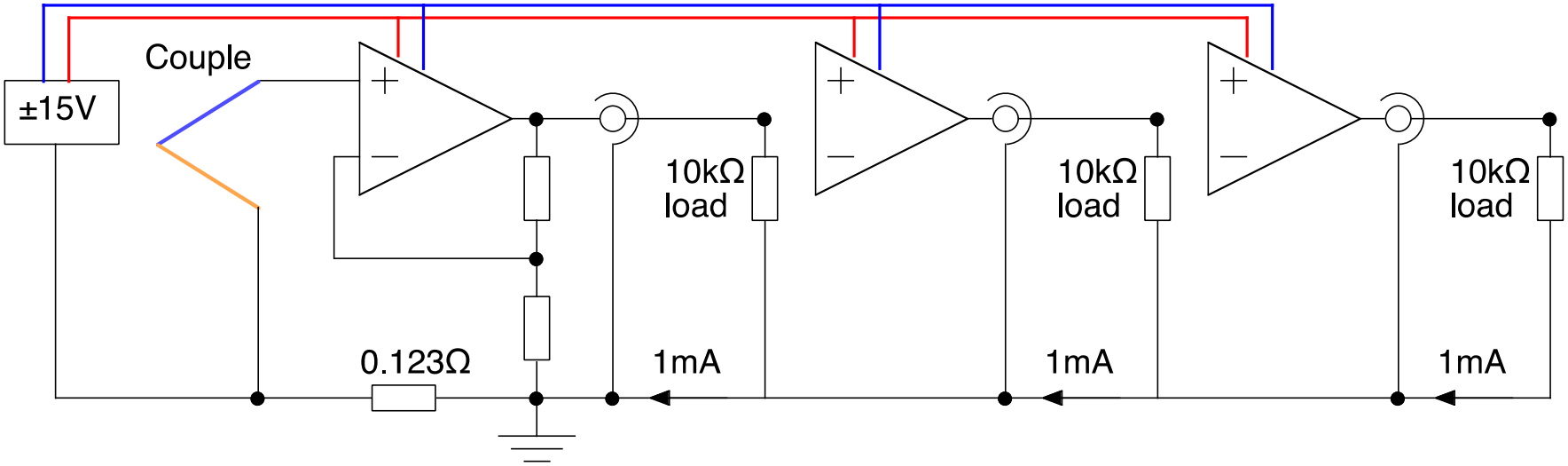
What you really built



Gain changes with load. 123μV (~2° C error for type K)
Error proportional to load current.

Common-Mode Signals (3)

Worse in any normal system (>1 opamp)



Large currents flow.

Induced voltages depend on

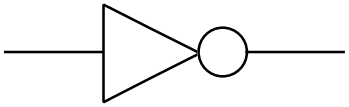
- Loads on other amplifiers
- Signals on other amplifiers
- Details of PCB design
- Quality of soldering

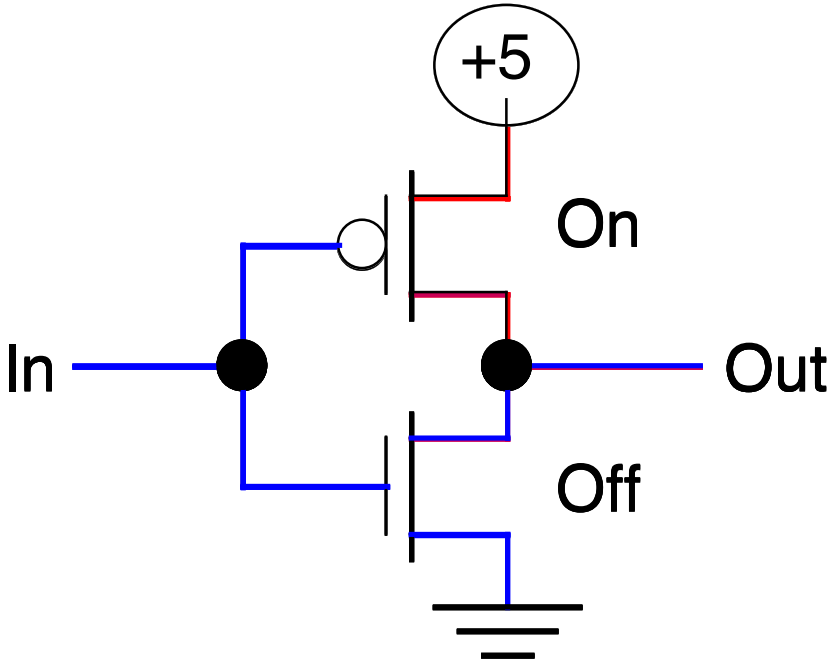
=> Can't design!

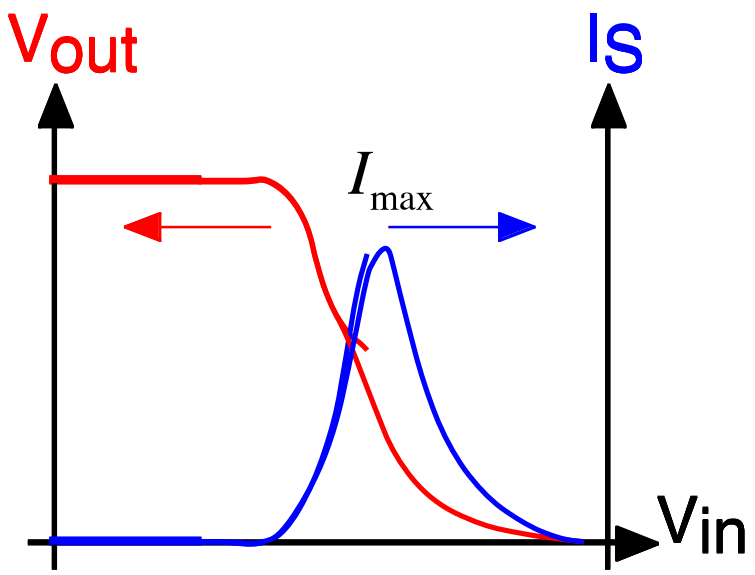
Dynamic current for logic

Fast logic is massively worse:

CMOS “NOT” gate







Typical values of "Ground Bounce"

For CMOS logic current only flows for switching time.

$$\Rightarrow \text{Charge} = Q_{switch} \approx \tau_{switch} \cdot I_{\max} = \tau_{switch} \cdot \frac{V_{CC}}{R_{switch}}$$

Define a *"Power Dissipation Capacitance"* $C_{PD} = \frac{Q_{switch}}{V_{CC}} = \frac{\tau_{switch}}{R_{switch}}$

For 74AHC00 $C_{PD} = 9pF, \tau_{switch} = 3.5ns \Rightarrow I_{\max} \sim 13mA$

A single gate will produce a spike of 0.12Ω x 13mA = 1.6mV.

Worse: Inductance ~ 0.18μH ~ 32Ω @ 1/2π x 3.5ns

-> 0.42 VOLTS

A big system can produce ~1V of junk.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Thank you
谢谢
INSPIRING PEOPLE