Tutorial-2: Real-Time Computer Systems and Architecture

Q 1. What general categories of functions are specified by computer instructions?

Q 2. List and briefly define the possible states that define an instruction execution.

Q 3. List and briefly define the QPI protocol layers.

Q 4. List and briefly define the PCIe protocol layers.

Mem.

Q 5. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a) What is the maximum directly addressable memory capacity (in bytes)?
b) Discuss the impact on the system speed if the microprocessor bus has:
   1) 32-bit local address bus and a 16-bit local data bus, or
   2) 16-bit local address bus and a 16-bit local data bus.
c) How many bits are needed for the program counter and the instruction register?

Q 6. Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/sec? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make, and explain.
Hint: Determine the number of bytes that can be transferred per bus cycle.

Q 7. Consider a computer system that contains an I/O module controlling a simple keyboard/printer teletype. The following registers are contained in the processor and connected directly to the system bus:

INPR: Input Register, 8 bits
OUTR: Output Register, 8 bits
FGI: Input Flag, 1 bit
FGO: Output Flag, 1 bit
IEN: Interrupt Enable, 1 bit

Keystroke input from the teletype and printer output to the teletype are controlled by the I/O module. The teletype is able to encode an alphanumeric symbol to an 8-bit word and decode an 8-bit word into an alphanumeric symbol.

a) Describe how the processor, using the first four registers listed in this problem, can achieve I/O with the teletype.
b) Describe how the function can be performed more efficiently by also employing IEN.

Q 8. Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.

a) Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?
b) Repeat assuming that half of the operands and instructions are one byte long.

Q 9. What are the differences among sequential access, direct access, and random access?

Q 10. What are the differences among direct mapping, associative mapping, and set-associative mapping?

Q 11. For a direct-mapped cache, a main memory address is viewed as consisting of three fields. List and define the three fields.

Q 12. For an associative cache, a main memory address is viewed as consisting of two fields. List and define the two fields.

Q 13. For a set-associative cache, a main memory address is viewed as consisting of three fields. List and define the three fields.

Q 14. A two-way set-associative cache has lines of 16 bytes and a total size of 8 kB. The 64-MB main memory is byte addressable. Show the format of main memory addresses.

Q 15. Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a) How is a 16-bit memory address divided into tag, line number, and byte number?
b) Into what line would bytes with each of the following addresses be stored?
0001 0001 0001 1011
1100 0011 0011 0100
1101 0000 0001 1101
1010 1010 1010 1010
c) Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?
d) How many total bytes of memory can be stored in the cache?
e) Why is the tag also stored in the cache?

I/O

Q 16. List three broad classifications of external, or peripheral, devices.

Q 17. List and briefly define three techniques for performing I/O.

Q 18. 7.5 What is the difference between memory-mapped I/O and isolated I/O?

Q 19. When a device interrupt occurs, how does the processor determine which device issued the interrupt?

Q 20. On a typical microprocessor, a distinct I/O address is used to refer to the I/O data registers and a distinct address for the control and status registers in an I/O controller for a given device. Such registers are referred to as ports. In the Intel 8088, two I/O instruction formats are used. In one format, the 8-bit opcode specifies an I/O operation; this is followed by an 8-bit port address. Other I/O opcodes imply that the port address is in the 16-bit DX register. How many ports can the 8088 address in each I/O addressing mode?

Q 21. A similar instruction format is used in the Zilog Z8000 microprocessor family. In this case, there is a direct port addressing capability, in which a 16-bit port address is part of the instruction, and an indirect port addressing capability, in which the instruction references one of the 16-bit general purpose registers, which contains the port address. How many ports can the Z8000 address in each I/O addressing mode?

Q 22. Consider a microprocessor that has a block I/O transfer instruction such as that found on the Z8000. Following its first execution, such an instruction takes five clock cycles to re- execute. However, if we employ a nonblocking I/O instruction, it takes a total of 20 clock cycles for fetching and execution. Calculate the increase in speed with the block I/O instruction when transferring blocks of 128 bytes.

Q 23. A system is based on an 8-bit microprocessor and has two I/O devices. The I/O controllers for this system use separate control and status registers. Both devices handle data on a 1-byte-at-a-time basis. The first device has two status lines and three control lines. The second device has three status lines and four control lines.

a) How many 8-bit I/O control module registers do we need for status reading and control of each device?
b) What is the total number of needed control module registers given that the first device is an output-only device?
c) How many distinct addresses are needed to control the two devices?

Q 24. What is an operating system?

Q 25. List and briefly define the key services provided by an OS?

Q 26. What is the difference between a process and a program?

Q 27. An I/O-bound program is one that, if run alone, would spend more time waiting for I/O than using the processor. A processor-bound program is the opposite. Suppose a short-term scheduling algorithm favors those programs that have used little processor time in the recent past. Explain why this algorithm favors I/O-bound programs and yet does not permanently deny processor time to processor-bound programs.