



电子科技大学

University of Electronic Science and Technology of China



University
of Glasgow

UESTC1008: Microelectronic Systems

Logic Gates and Propagation Delays

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Overview

- The following topics are covered in this lecture:
 - Logic gates
 - Adders (half and full bit)
 - Digital circuit current and voltages
 - Propagation Delay Time

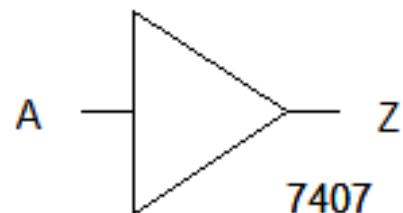
Assumptions

- Truth Tables. https://en.wikipedia.org/wiki/Truth_table
 - True = logical “1”
 - False = logical “0”
- Function Tables
 - Ideal gate
 - Output is 0V, which is equivalent to a logical “0”
 - Output is 5V, which is equivalent to a logical “1” for TTL

TTL: https://en.wikipedia.org/wiki/Transistor%20transistor_logic

Single Input Gates - Buffer

Symbol



https://en.wikipedia.org/wiki/Digital_buffer

- Truth Table
- Function Table

A	Z
0	0
1	1

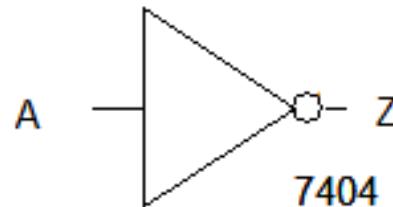
V _A	V _o
0V	0V
5V	5V

Applications

- Reshape signal to increase voltage of a logical ‘1’/lower the voltage of a logical ‘0’.
 - Digital signals degrade as the signal passes through components (e.g., resistive losses in wires), addition of noise from electromagnetic interference (EMI), etc.
- Source or sink current beyond the specifications of the other gates.
 - Acts as a voltage follower (an op amp circuit).

Single Input Gates- Inverter

Symbol



7404

[https://en.wikipedia.org/wiki/Inverter_\(logic_gate\)](https://en.wikipedia.org/wiki/Inverter_(logic_gate))

- Truth Table

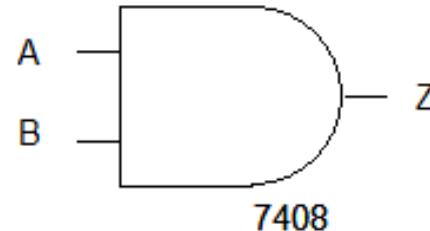
A	Z
0	1
1	0

- Function Table

V _A	V _o
0V	5V
5V	0V

Two Input Gates - AND

Symbol



https://en.wikipedia.org/wiki/AND_gate

- Truth Table

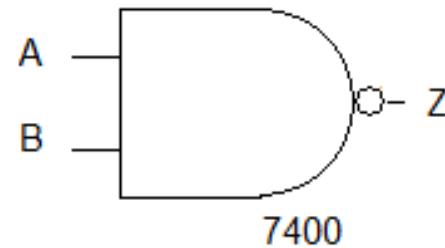
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

- Function Table

V _A	V _B	V _o
0V	0V	0V
0V	5V	0V
5V	0V	0V
5V	5V	5V

Two Input Gates – NAND(Not-AND)

Symbol



https://en.wikipedia.org/wiki/7400-series_integrated_circuits

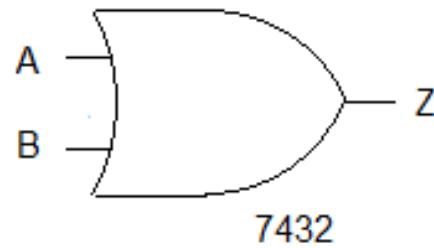
- Truth Table
- Function Table

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

V _A	V _B	V _o
0V	0V	5V
0V	5V	5V
5V	0V	5V
5V	5V	0V

Two Input Gates - OR

Symbol



https://en.wikipedia.org/wiki/OR_gate

- Truth Table

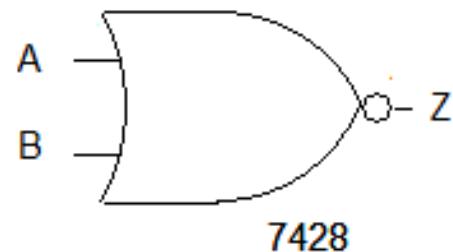
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

- Function Table

V _A	V _B	V _o
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V

Two Input Gates - NOR

Symbol



https://en.wikipedia.org/wiki/NOR_gate

- Truth Table
- Function Table

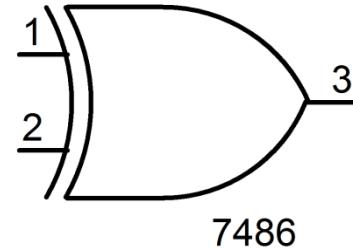
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

V _A	V _B	V _o
0V	0V	5V
0V	5V	0V
5V	0V	0V
5V	5V	0V

Two Input Gate - XOR

pronounced as **Exclusive OR**

- **Symbol**



7486

https://en.wikipedia.org/wiki/XOR_gate

- Truth Table

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

- Function Table

V _A	V _B	V _o
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	0V

Quick Test

Gate	A	B	Z
XOR-?	0	1	
NAND-?	1	1	
NOR-?	0	0	
AND-?	1	0	

Quick Test

Gate	A	B	Z
XOR-?	0	1	1
NAND-?	1	1	0
NOR-?	0	0	1
AND-?	1	0	0

Boolean Expression and its Implementation

Boolean Expression	Gate Implementation
$A \cdot B$	A AND B
$A + B$	A OR B
\bar{A}	Inverter -NOT A
\overline{AB}	NOT(A AND B)=NAND
$\overline{A + B}$	Not(A OR B)=NOR
$\overline{A \oplus B}$	NOT (A XOR B)

Example: Boolean Expression

$$\overline{A \cdot (B + C)}$$

Implementation: NOT (A AND (B OR C))

Example

Example: Boolean Expression

$$\overline{A \cdot (B + C)}$$

Implementation: NOT (A AND (B OR C))



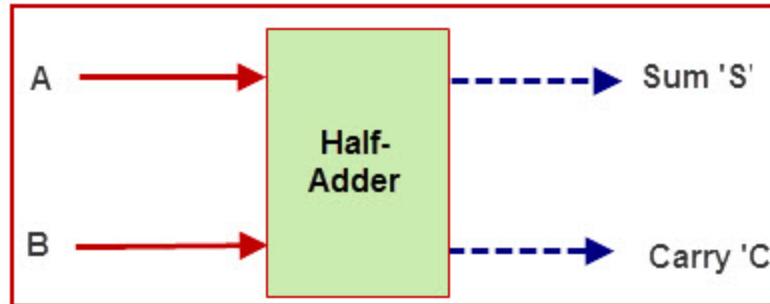
- Please find more examples on
 - Boolean expression to logic diagram
 - logic diagram to Boolean expression

Boolean Algebra Simplification Rules

1. $A + \bar{A} = 1$	2. $A + A = A$
3. $A \cdot A = A$	4. $A \cdot \bar{A} = 0$
5. $A \cdot (B + C) = A \cdot B + A \cdot C$	6. $A + 0 = A$
7. $A + 1 = 1$	8. $A \cdot 1 = A$
9. $A \cdot 0 = 0$	10. $A \cdot B = B \cdot A$
11. $A + B = B + A$	12. $B \cdot (A + \bar{A}) = B$
13. $A + A \cdot B = A$	14. $A \cdot (A + B) = A$
15. $A + \bar{A} \cdot B = A + B$	16. $A \cdot (\bar{A} + B) = A \cdot B$
17. $\overline{A + B} = \overline{A} \cdot \overline{B}$	18. $\overline{A \cdot B} = \overline{A} + \overline{B}$

- Please find some examples of Boolean expression simplification

Half adder – 2 bit adder



INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder

$$0 + 0 = 00$$

$$0 + 1 = 01$$

$$1 + 0 = 01$$

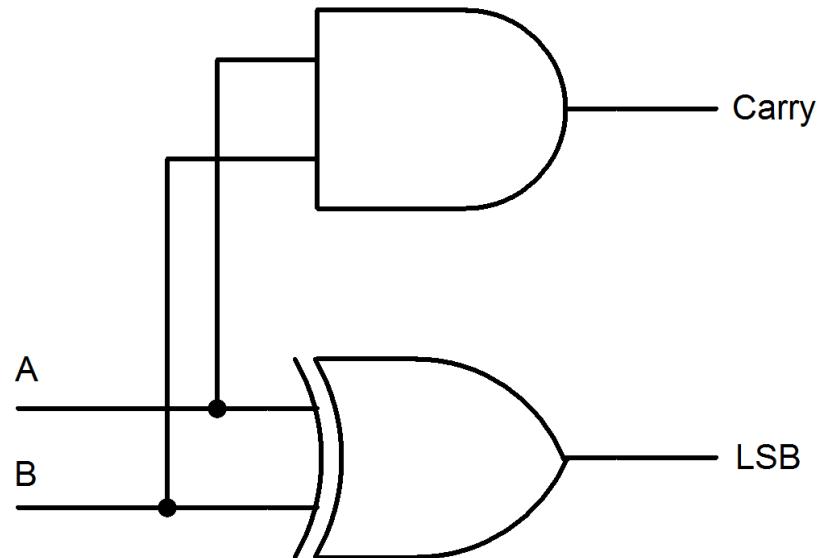
$$1 + 1 = 10$$

A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1

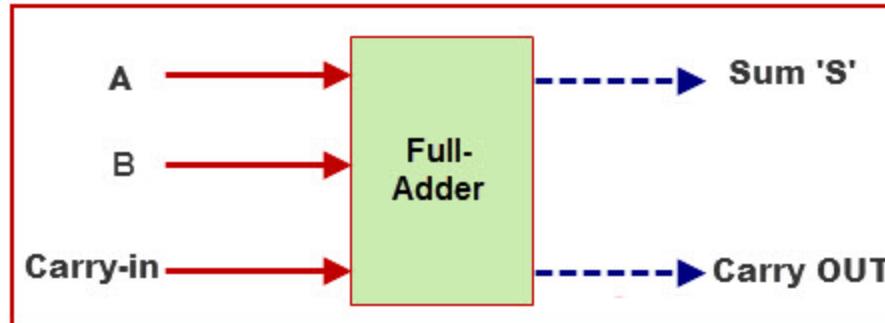
A	B	LSB
0	0	0
0	1	1
1	0	1
1	1	0

Half Adders

- A half adder is an Exclusive OR gate.
 - The output of the XOR gate is the least significant bit (LSB) of the addition of 2 1-bit numbers.
- A adder with carry is an XOR gate and an AND gate.
 - The output of the XOR gate is the LSB.
 - The output of the AND gate is the Carry.

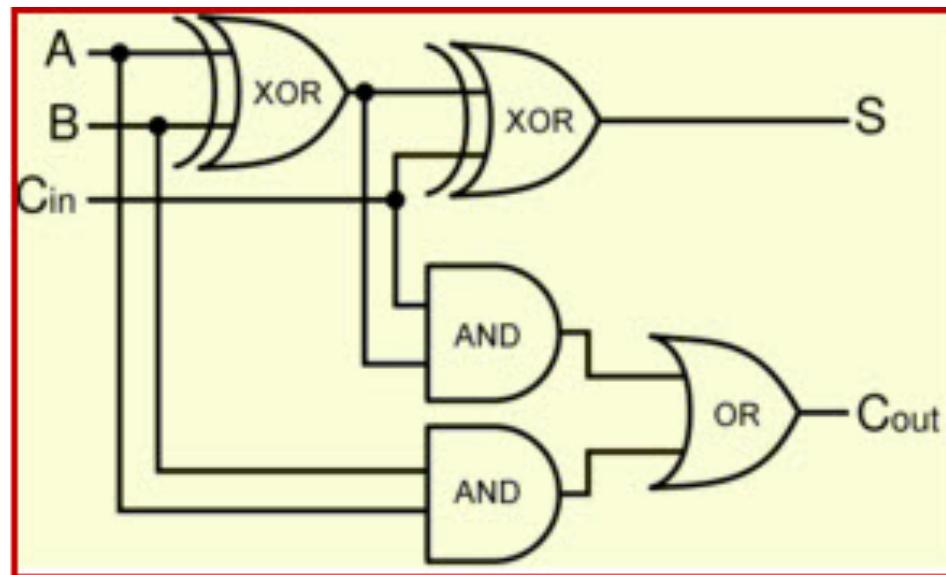
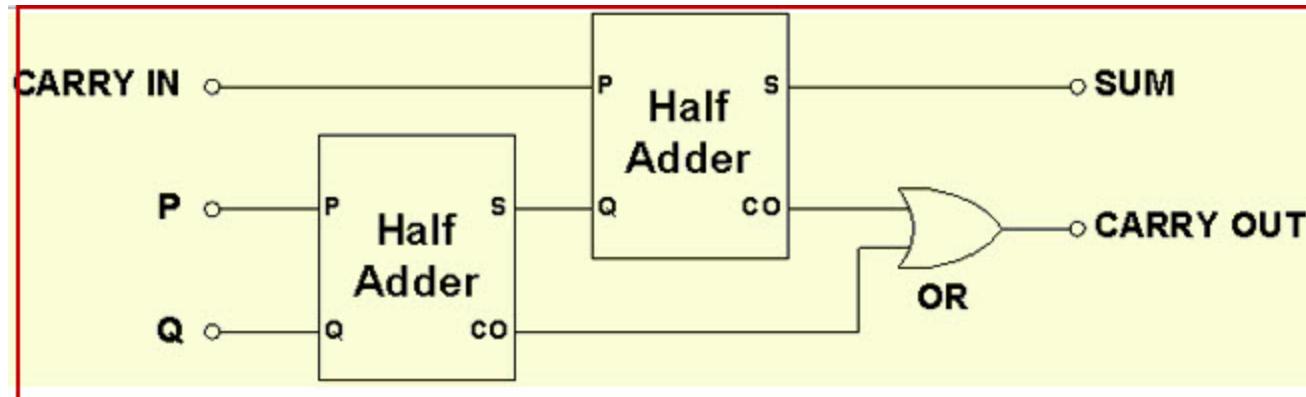


Full Adders – 3 bit adders



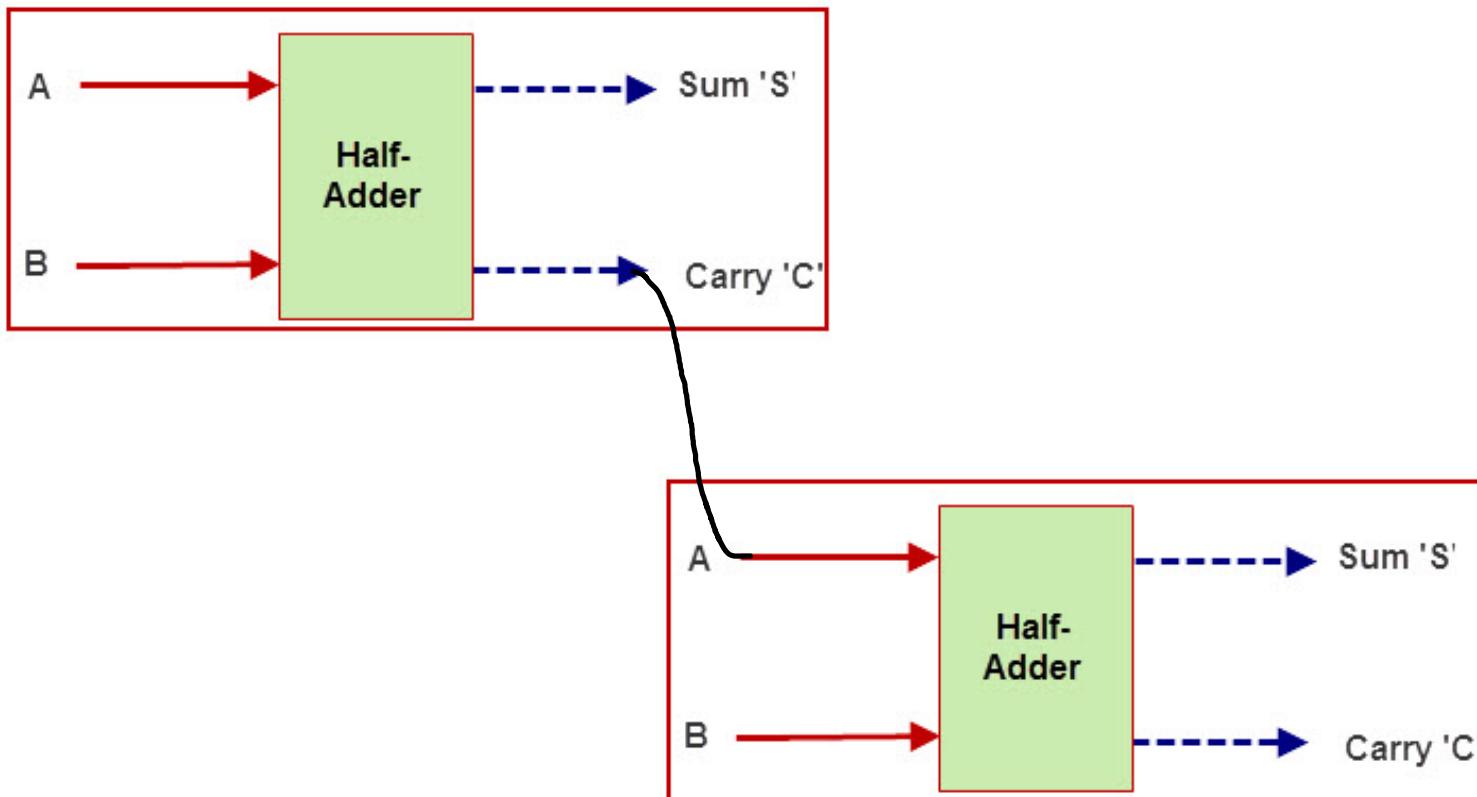
INPUTS			OUTPUT	
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full Adders – 3 bit adders



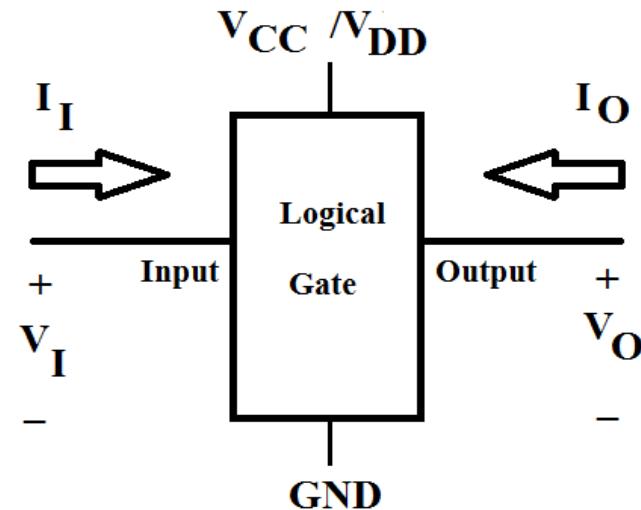
Question

- What happens if we connect two half-adders as follows



Currents and Voltages

- **All currents** are defined as positive when they flow into the terminal of a logical gate. This includes the output terminals.
- **All voltages** are measured with respect to ground, unless otherwise specified.
- The **first subscript** on a voltage or current indicates the terminal where the parameter was measured. I_I is the current entering the input terminal. V_O is the voltage at the output terminal.



Output Voltages

- $V_{OH}(\min)$ is the smallest voltage that can occur on a gate output when the output is in the HIGH (logic 1) voltage range output
- $V_{OL}(\max)$ is the largest voltage that can occur on the output of a gate when the output is in the LOW (logic 0) voltage range

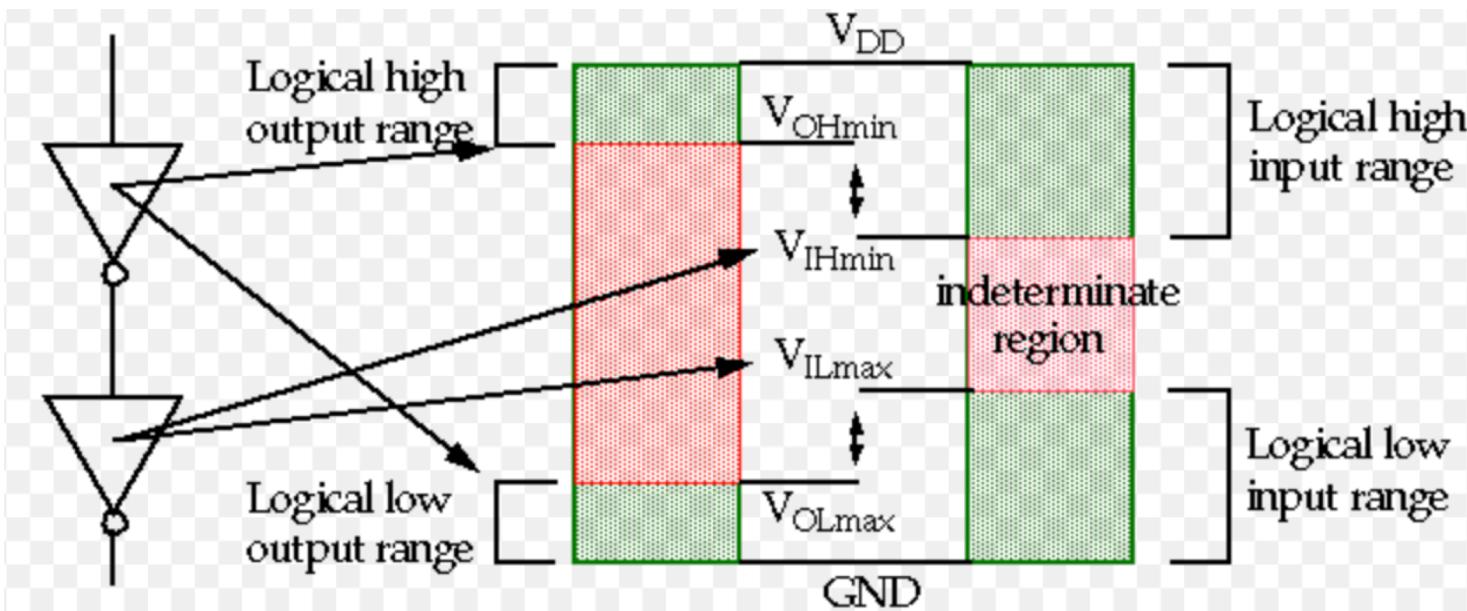
Input Voltages

- $V_{IH}(\min)$ is the smallest input voltage that will be interpreted as a HIGH input
- $V_{IL}(\max)$ is the greatest input voltage that will be interpreted as a LOW input

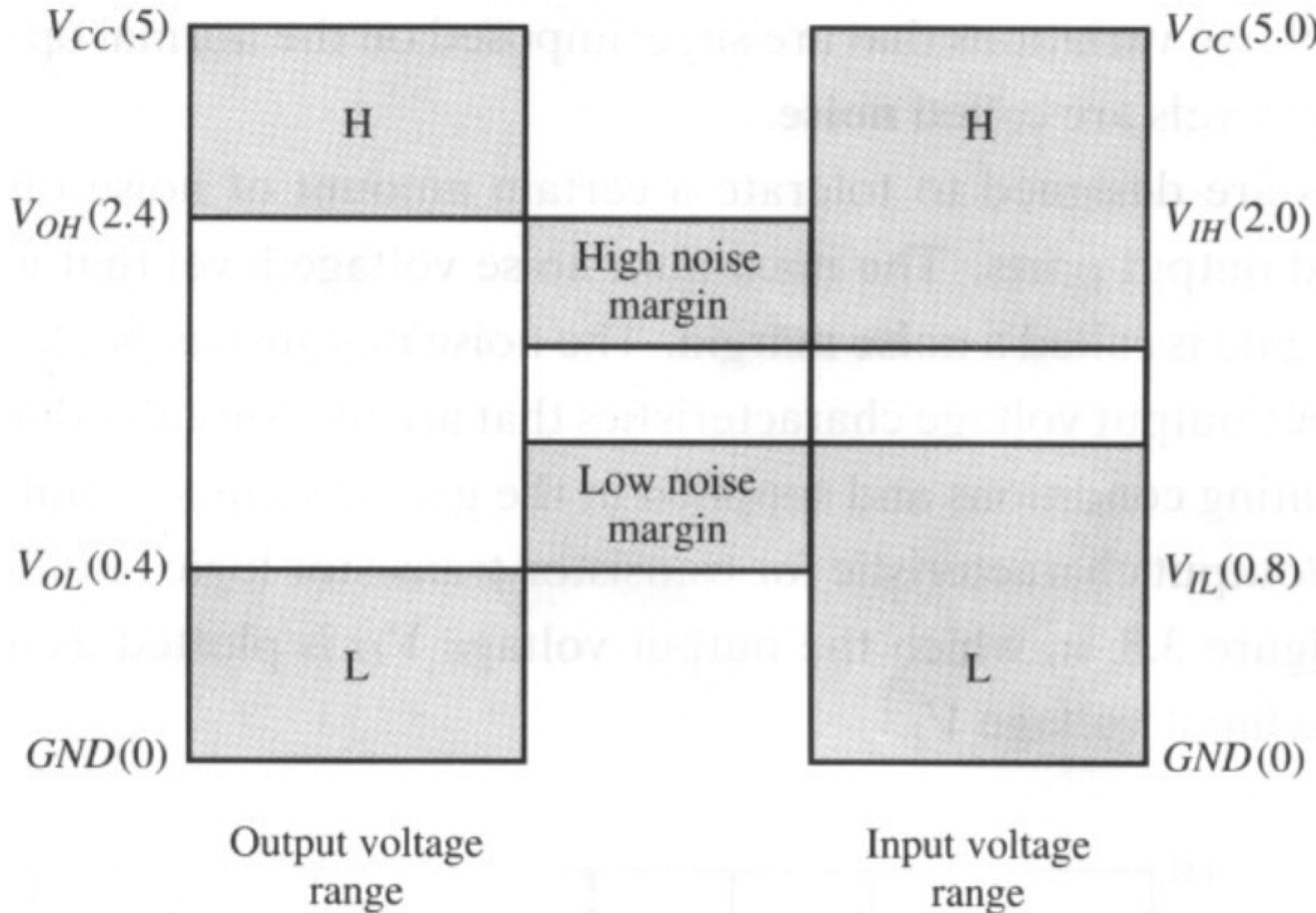
Noise Margin for TTL

- NML: $V_{NL} = V_{IL}(max) - V_{OL}(max)$
 - Noise margin low. The maximum amount of noise allowed at the output terminal of a logic gate that, added to V_{OLmax} , will always be recognized as a low at the input of a cascaded gate.
- NMH: $V_{NH} = V_{OH}(min) - V_{IH}(min)$
 - Noise margin high. The maximum amount of noise allowed at the output terminal of a gate that, subtracted from V_{OHmin} , will always be recognized as a high at the input of a cascaded gate

Noise Margin for TTL



Noise Margin for TTL



Undefined

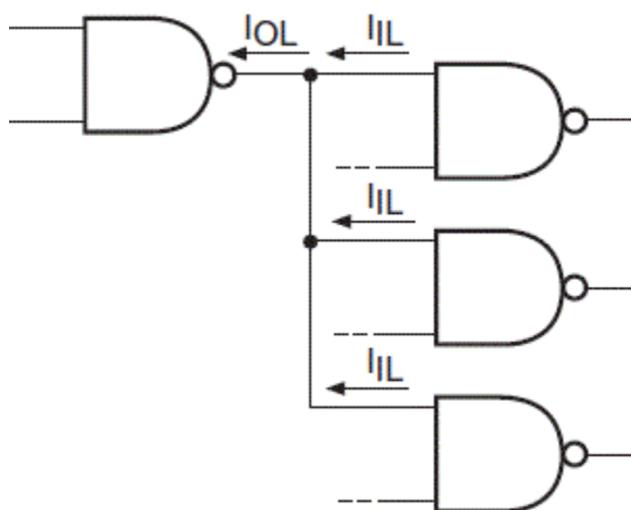
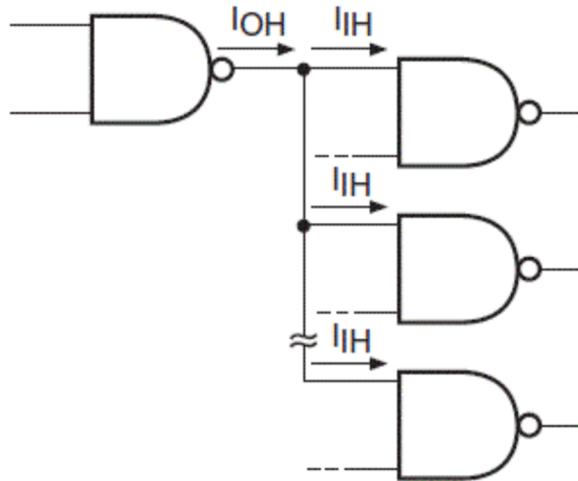
- X – an undefined logic level that is associated with a voltage between $V_{IL}(\max)$ and $V_{IH}(\min)$.

Currents

- $I_{OH}(\max)$
 - the maximum current that flow into the output terminal when the output of the logical circuit is a “1”.
- $I_{OL}(\max)$
 - the maximum current that flow into the output terminal when the output of the logical circuit is a “0”.
- $I_{IH}(\max)$
 - the maximum current that flow into the input terminal when the input of the logical circuit is a “1”.
- $I_{IL}(\max)$
 - the maximum current that flow into the input terminal when the input of the logical circuit is a “0”.

Fanout

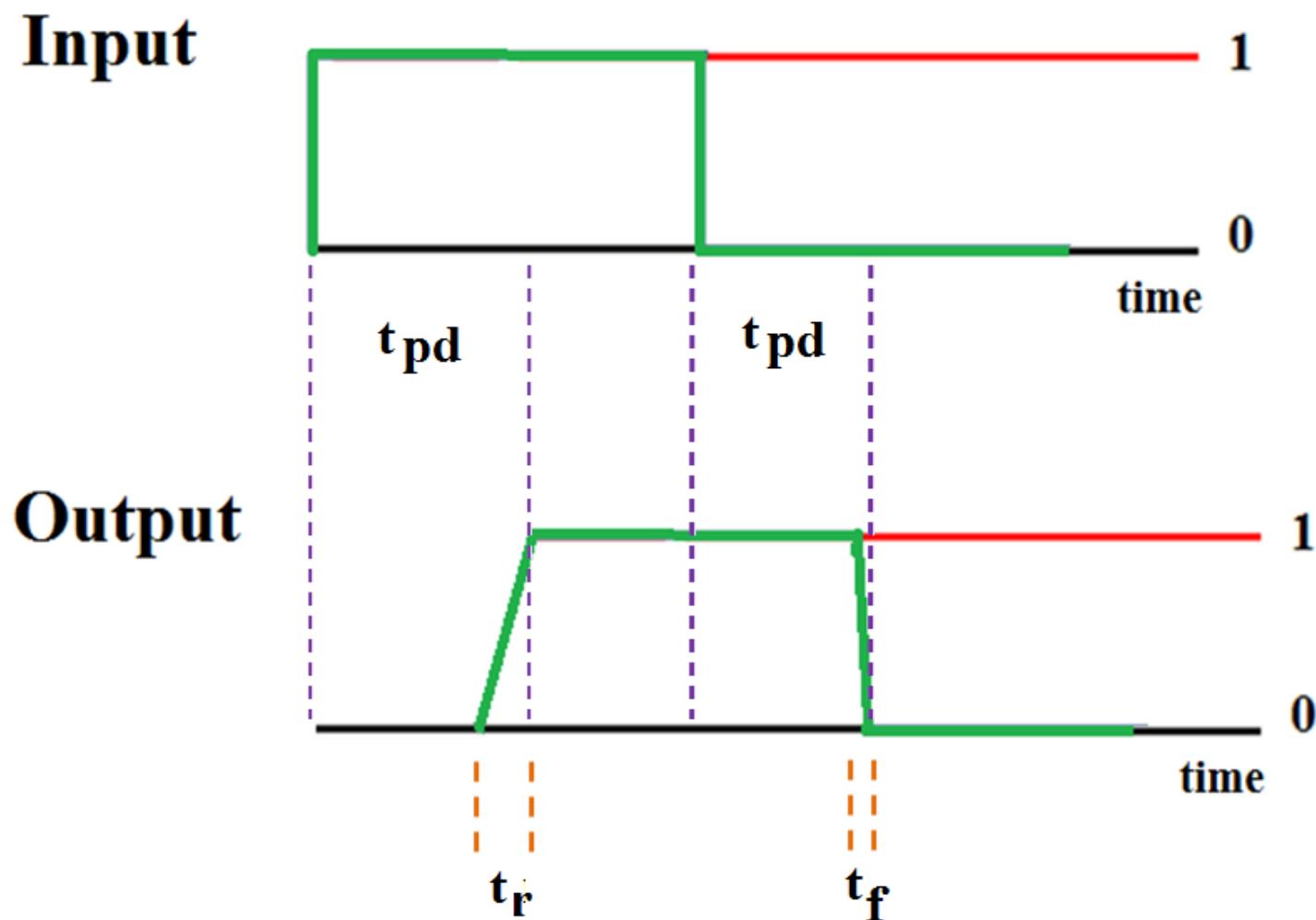
- N – Fanout
 - Fanout is the maximum number of logic gates (exactly the same at the first one) that can be attached in parallel to the output of the logic gate.



Propagation Delay Time

- t_{pd} is the time required for a change of voltage at the input terminals of a logic gate to cause a change in the voltage at the output of the gate.
 - Note that the **rise time**, t_r , and the **fall time**, t_f , do not have to be the same.
 - Also, the propagation delay time may not be the same length of time when the transition is from $0 \rightarrow 1$ as it is from $1 \rightarrow 0$.
 - something like charging and discharging

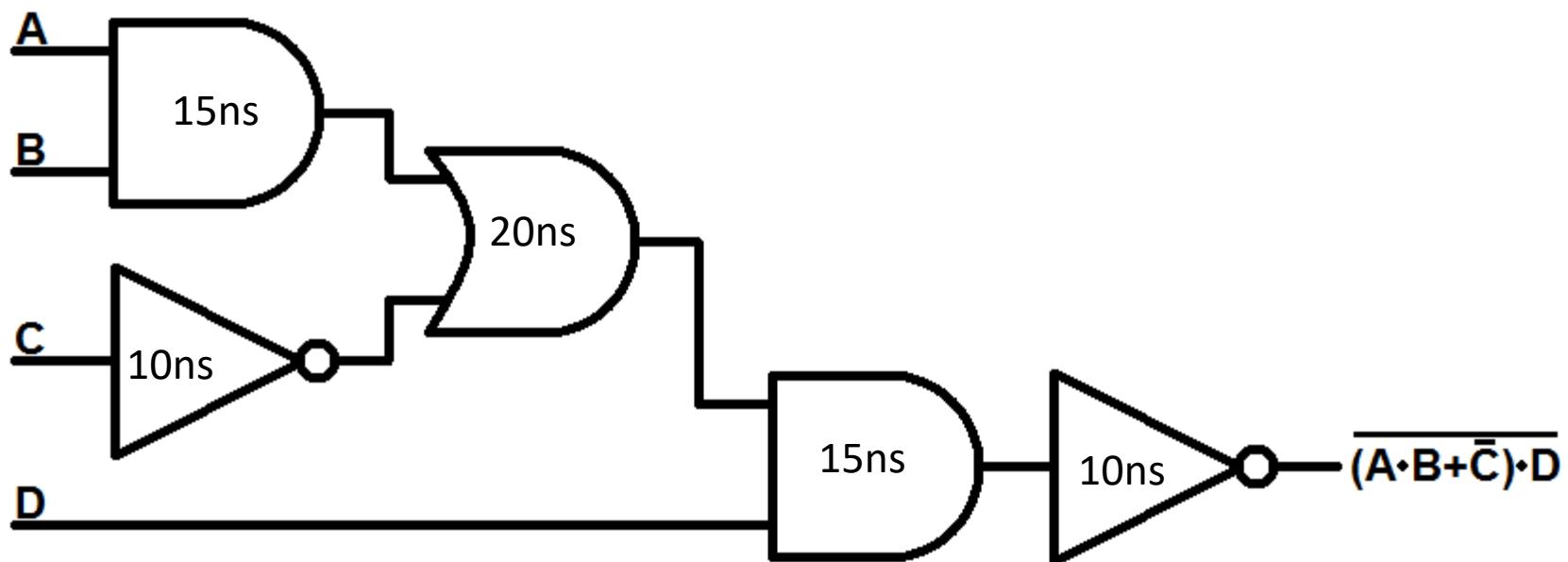
Propagation Delay Time



Example - Propagation Delay

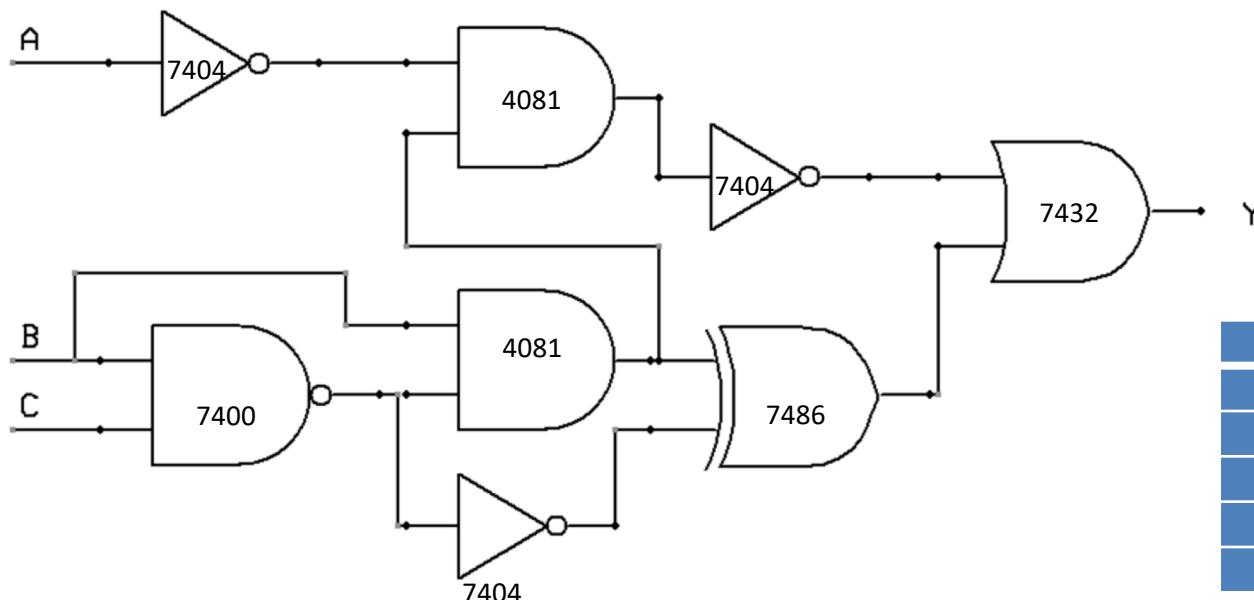
Propagation delay is the maximum delay faced by any input to reach the output.

Using the given timing specifications for each component, what is the propagation delay, t_{PD} , for the circuit shown below?



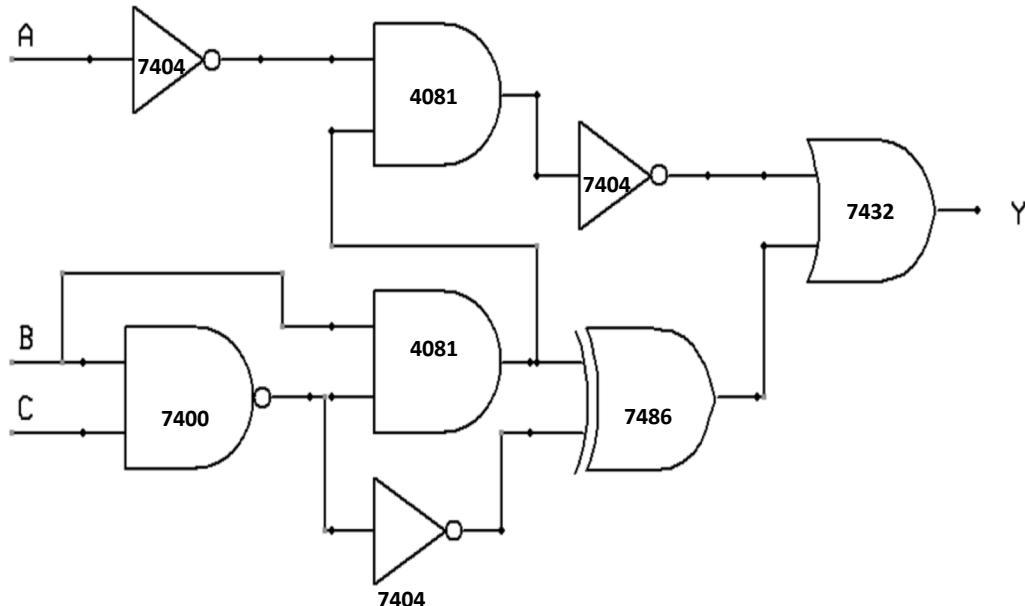
Example - Propagation Delay

- Using the following table of timing specifications for each component, what is the propagation delay, t_{PD} , for the circuit shown below?



Gate	t_{PD}
4081	15 ns
7400	20 ns
7404	10 ns
7432	15 ns
7486	25 ns

Example - Propagation Delay



Gate	t_{PD}
4081	15 ns
7400	20 ns
7404	10 ns
7432	15 ns
7486	25 ns

- Some of the possible path flows are given below:
- For A: $7404 + 4081 + 7404 + 7432 = 10 + 15 + 10 + 15 = 50\text{ns}$
- For B: $4081 + 4081 + 7404 + 7432 = 15 + 15 + 10 + 15 = 55\text{ns}$
 $4081 + 7486 + 7432 = 15 + 25 + 15 = 55\text{ns}$
 $7400 + 4081 + 7486 + 7432 = 20 + 15 + 25 + 15 = 75\text{ns}$
 $7400 + 7404 + 7486 + 7432 = 20 + 10 + 25 + 15 = 70\text{ns}$
- For C: $7400 + 4081 + 7486 + 7432 = 20 + 15 + 25 + 15 = 75\text{ns}$
 $7400 + 7404 + 7486 + 7432 = 20 + 10 + 25 + 15 = 70\text{ns}$
 $7400 + 4081 + 4081 + 7404 + 7432 = 20 + 15 + 15 + 10 + 15 = 75\text{ns}$

We need to calculate propagation delay time for all the possible path flows and then take the maximum value out of them.

- The propagation delay, t_{PD} , for the circuit is 75ns