



电子科技大学
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UESTC4019: Real-Time Computer Systems and Architecture

Lecture 7

Computer Function and Interconnection (Part-3)

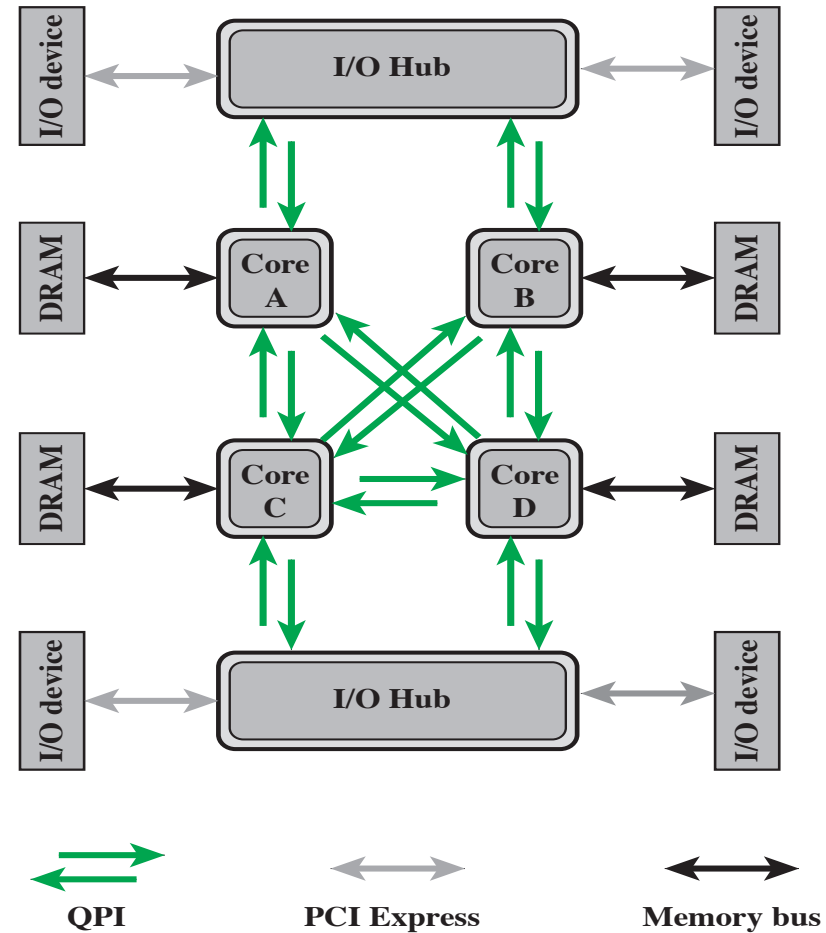
Point-to-Point Interconnect

- The shared bus architecture was the standard approach to interconnection between the processor and other components (memory, I/O, and so on) for decades. But contemporary systems increasingly rely on point-to-point interconnection rather than shared buses.
- Principal reason for change was the electrical constraints encountered with increasing the frequency of wide synchronous buses
- At higher and higher data rates it becomes increasingly difficult to perform the synchronization and arbitration functions in a timely fashion
- A conventional shared bus on the same chip magnified the difficulties of increasing bus data rate and reducing bus latency to keep up with the processors
- Has lower latency, higher data rate, and better scalability

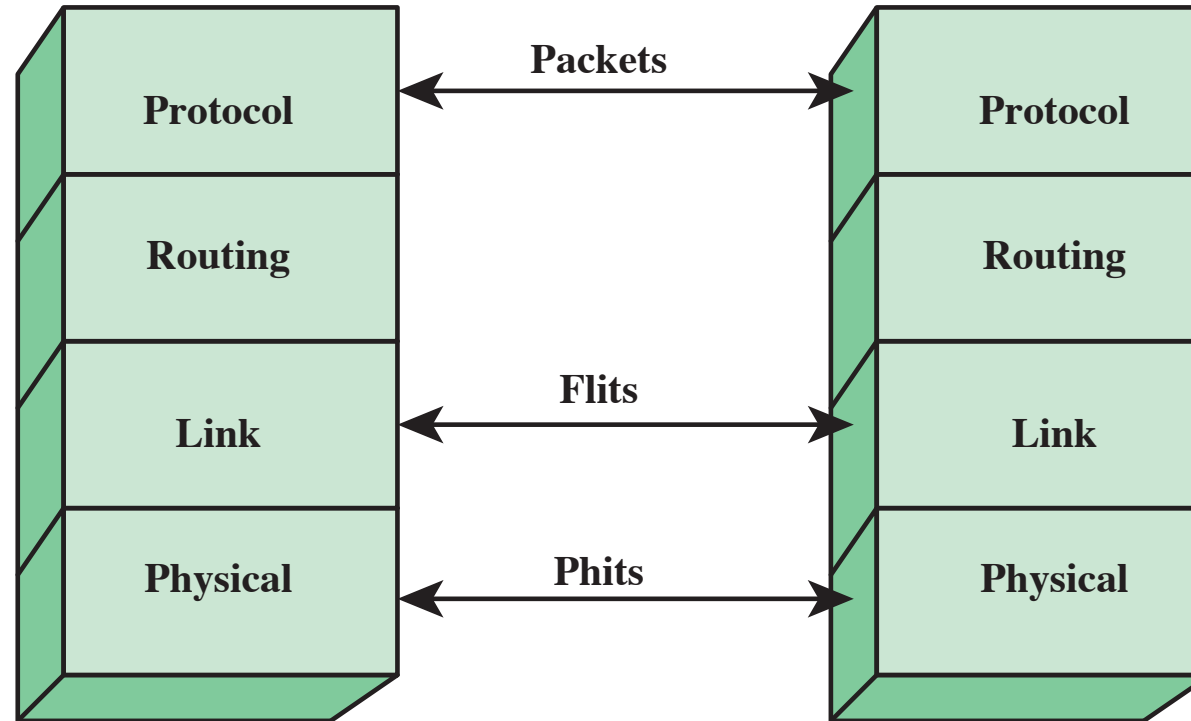
Quick Path Interconnect (QPI)

- Introduced in 2008
- Multiple direct connections
 - Direct pairwise connections to other components eliminating the need for arbitration found in shared transmission systems
- Layered protocol architecture
 - These processor level interconnects use a layered protocol architecture rather than the simple use of control signals found in shared bus arrangements
- Packetized data transfer
 - Data are sent as a sequence of packets each of which includes control headers and error control codes

Multicore Configuration Using QPI

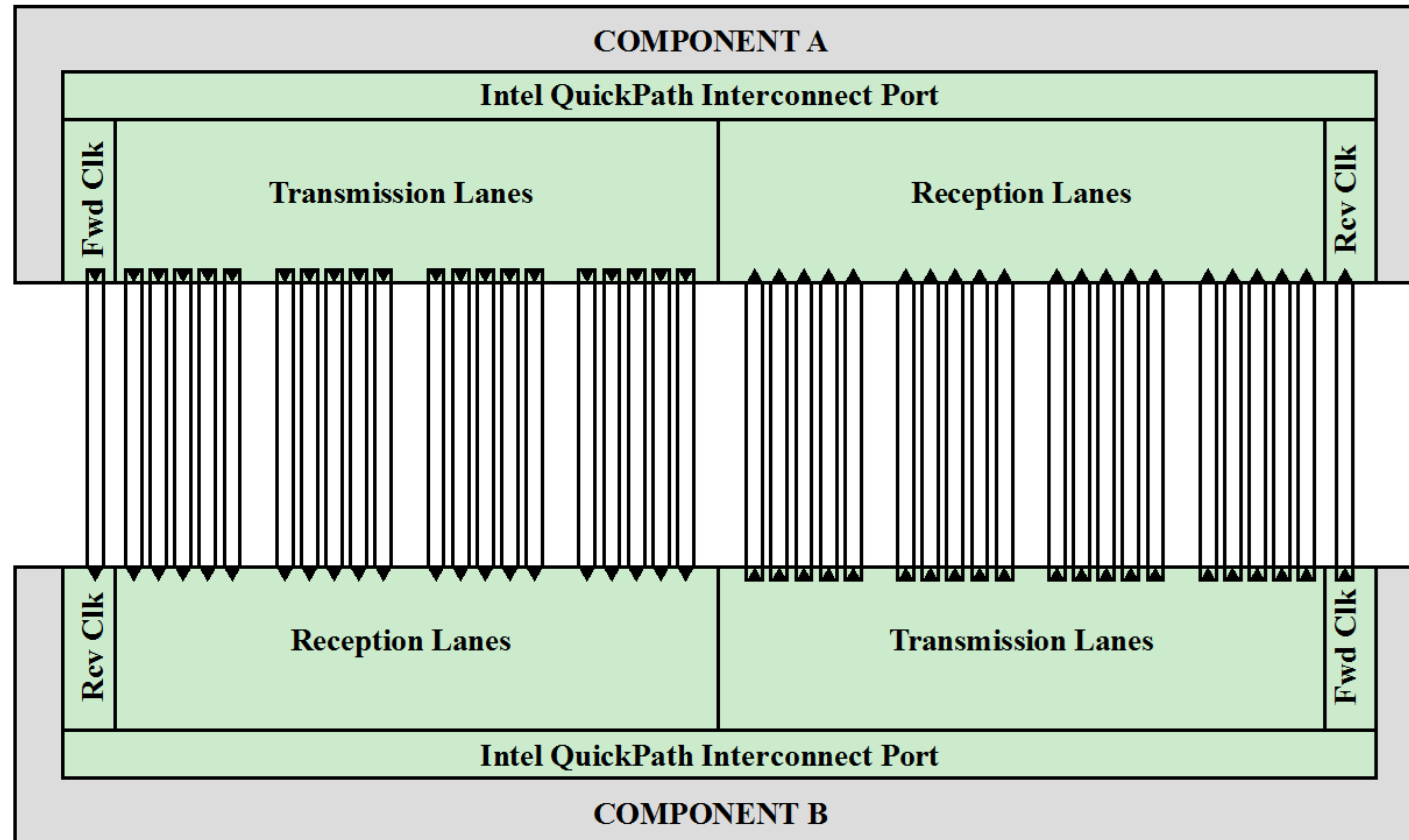


QPI Layers

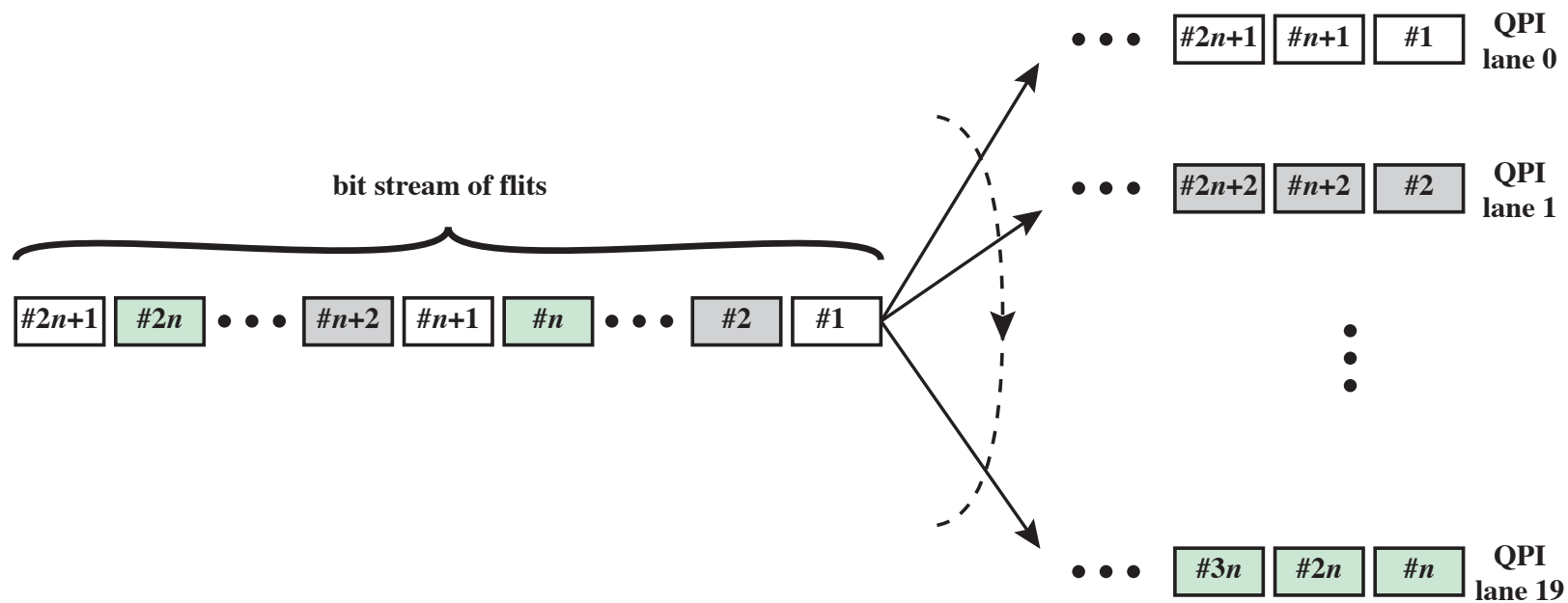


- **Physical:** Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s and 0s. The unit of transfer at the Physical layer is 20 bits, which is called a **Phit** (physical unit).
- **Link:** Responsible for reliable transmission and flow control. The Link layer's unit of transfer is an 80-bit **Flit** (flow control unit).
- **Routing:** Provides the framework for directing packets through the fabric.
- **Protocol:** The high-level set of rules for exchanging **packets** of data between devices. A packet is comprised of an integral number of Flits.

Physical Interface of the Intel QPI Interconnect



QPI Multilane Distribution



QPI Link Layer

- Performs two key functions: **flow control** and **error control**
 - Operate on the level of the flit (flow control unit)
 - Each flit consists of a **72-bit message** payload and **an 8-bit error control code** called a **cyclic redundancy check (CRC)**
- Flow control function
 - Needed to ensure that a sending QPI entity **does not overwhelm a receiving QPI** entity by sending data faster than the receiver can process the data and clear buffers for more incoming data
- Error control function
 - **Detects and recovers from bit errors**, and so isolates higher layers from experiencing bit errors

QPI Routing and Protocol Layers

- Routing Layer
 - Used to determine the course that a packet will traverse across the available system interconnects
 - Defined by firmware and describe the possible paths that a packet can follow
- Protocol Layer
 - Packet is defined as the unit of transfer
 - One key function performed at this level is a cache coherency protocol which deals with making sure that main memory values held in multiple caches are consistent
 - A typical data packet payload is a block of data being sent to or from a cache

Peripheral Component Interconnect (PCI)

(1 of 2)

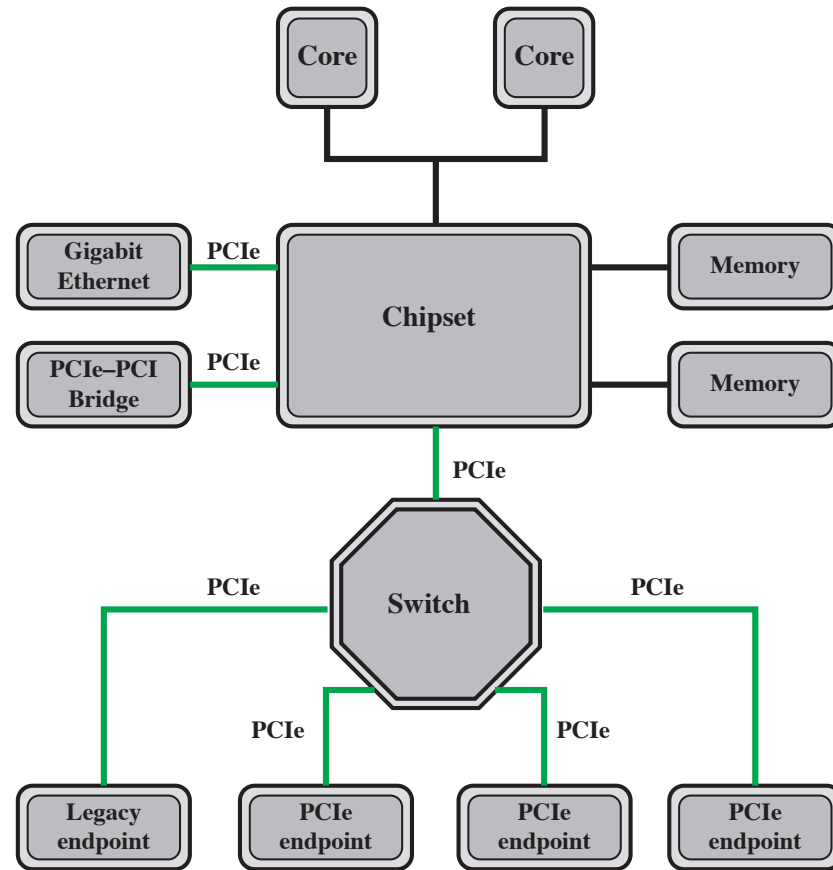
- A popular **high bandwidth, processor independent** bus that can function as a mezzanine or peripheral bus
- Delivers **better system performance** for high speed I/O subsystems
- PCI **Special Interest Group (SIG)**
 - Created to develop further and maintain the compatibility of the PCI specifications

Peripheral Component Interconnect (PCI)

(2 of 2)

- **PCI Express (PCIe)**
 - **Point-to-point interconnect scheme** intended to replace bus-based schemes such as PCI
 - Key requirement is **high capacity** to support the needs of **higher data rate** I/O devices, such as Gigabit Ethernet
 - Another requirement deals with the need to support time dependent data streams

Typical Configuration Using PCIe



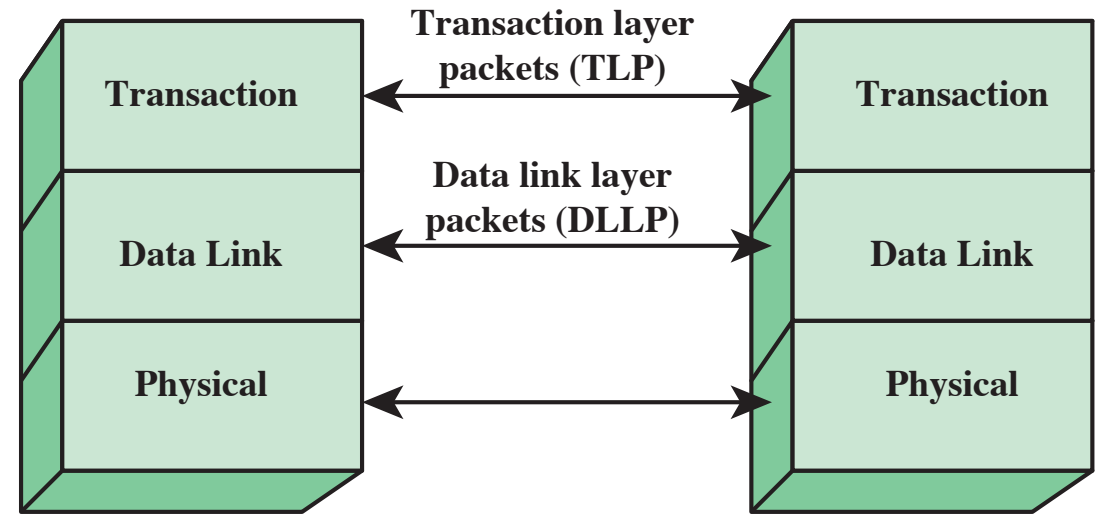
PCIe Protocol Layers

The PCIe protocol architecture encompasses the following layers:

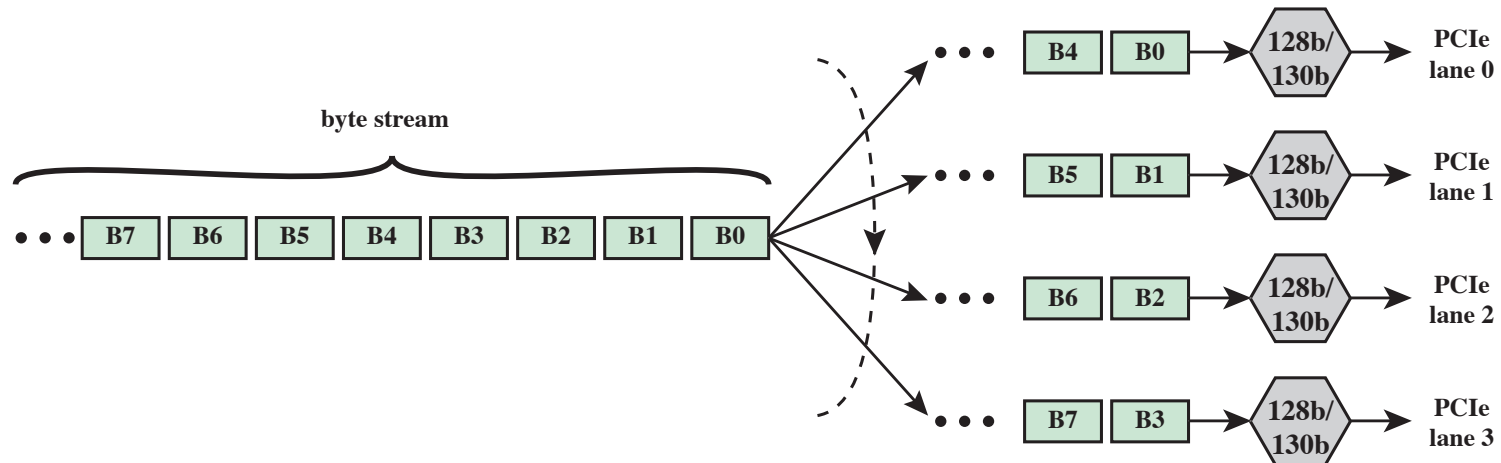
Physical: Consists of the **actual wires carrying the signals, as well as circuitry and logic to support** ancillary features required in the transmission and receipt of the 1s and 0s.

Data link: Is responsible for reliable transmission and flow control. Data packets generated and consumed by the DLL are called **Data Link Layer Packets (DLLPs)**.

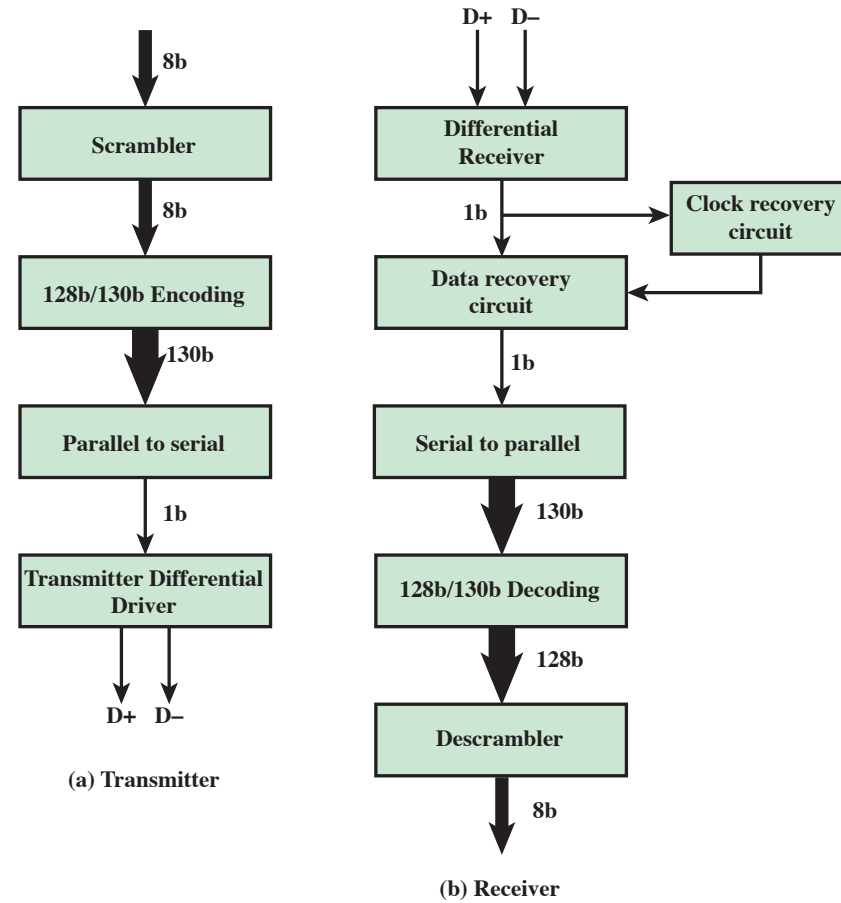
Transaction: **Generates and consumes data packets** used to implement **load/store data transfer mechanisms** and also manages the flow control of those packets between the two components on a link. Data packets generated and consumed by the TL are called Transaction Layer Packets (TLPs).



PCIe Multilane Distribution



PCIe Transmit and Receive Block Diagrams



PCIe Transaction Layer (TL) (1 of 2)

- Receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer
- Most transactions use a **split transaction** technique
 - A request packet is sent out by a source PCIe device which then waits for a response called a **completion** packet

PCIe Transaction Layer (TL) (2 of 2)

- TL messages and some write transactions are posted transactions (meaning that no response is expected)
- TL packet format supports 32-bit memory addressing and extended 64-bit memory addressing

The TL supports four address spaces (1 of 2)

- Memory
 - The memory space includes system main memory and PCIe I/O devices
 - Certain ranges of memory addresses map into I/O devices
- Configuration
 - This address space enables the TL to read/write configuration registers associated with I/O devices

The TL supports four address spaces (2 of 2)

- I/O
 - This address space is used for legacy PCI devices, with reserved address ranges used to address legacy I/O devices
- Message
 - This address space is for control signals related to interrupts, error handling, and power management

Table 3-2 PCIe TLP Transaction Types

(1 of 2)

Address Space	TLP Type	Purpose
Memory	Memory Read Request	Transfer data to or from a location in the system memory map.
	Memory Read Lock Request	
	Memory Write Request	
I/O	I/O Read Request	Transfer data to or from a location in the system memory map for legacy devices.
	I/O Write Request	
Configuration	Config Type 0 Read Request	Transfer data to or from a location in the configuration space of a PCIe device.
	Config Type 0 Write Request	
	Config Type 1 Read Request	
	Config Type 1 Write Request	

Table 3-2 PCIe TLP Transaction Types

(2 of 2)

Address Space	TLP Type	Purpose
Message	Message Request	Provides in-band messaging and event reporting.
	Message Request with Data	
Memory, I/O, Configuration	Completion	Returned for certain requests.
	Completion with Data	
	Completion Locked	
	Completion Locked with Data	

PCIe Protocol Data Unit Format

