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UESTC4019: Real-Time Computer Systems and Architecture

Lecture 6

Computer Function and Interconnection (Part-2)

I/O Function (1 of 2)

- I/O module can exchange data directly with the processor
- Processor can read data from or write data to an I/O module
  - Processor identifies a specific device that is controlled by a particular I/O module
  - I/O instructions rather than memory referencing instructions

I/O Function (2 of 2)

- In some cases it is desirable to allow I/O exchanges to occur directly with memory
  - The processor grants to an I/O module the authority to read from or write to memory so that the I/O memory transfer can occur without tying up the processor
  - The I/O module issues read or write commands to memory relieving the processor of responsibility for the exchange
  - This operation is known as direct memory access (DMA)

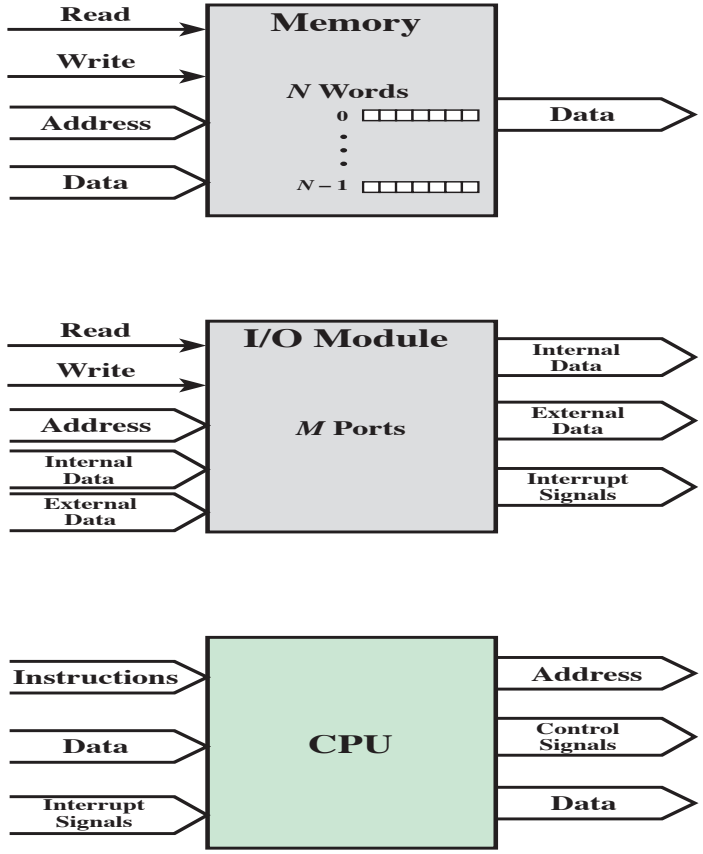
Computer Modules

- Figure suggests the types of exchanges that are needed by indicating the major forms of input and output for each module type:

- **Memory:** Typically, a memory module will consist of *N words of equal length.* Each word is assigned a unique numerical address (0, 1, …, *N-1). A word of* data can be read from or written into the memory. The nature of the operation is indicated by read and write control signals. The location for the operation is specified by an address.

- **I/O module:** From an internal (to the computer system) point of view, I/O is functionally similar to memory. There are two operations, read and write. Further, an I/O module may control more than one external device. We can refer to each of the interfaces to an external device as **a *port*** and give each a unique address (e.g., 0, 1, …, *M - 1)*. In addition, there are external data paths for the input and output of data with an external device. Finally, an I/O module may be able to send interrupt signals to the processor.

- **Processor:** The processor reads in instructions and data, writes out data after processing, and uses control signals to control the overall operation of the system. It also receives interrupt signals.



The Interconnection Structure Must Support the Following Types of Transfers

- Memory to processor
  - Processor reads an instruction or a unit of data from memory
- Processor to memory
  - Processor writes a unit of data to memory
- I/O to processor
  - Processor reads data from an I/O device via an I/O module
- Processor to I/O
  - Processor sends data to the I/O device
- I/O to or from memory
  - An I/O module is allowed to exchange data directly with memory without going through the processor using direct memory access

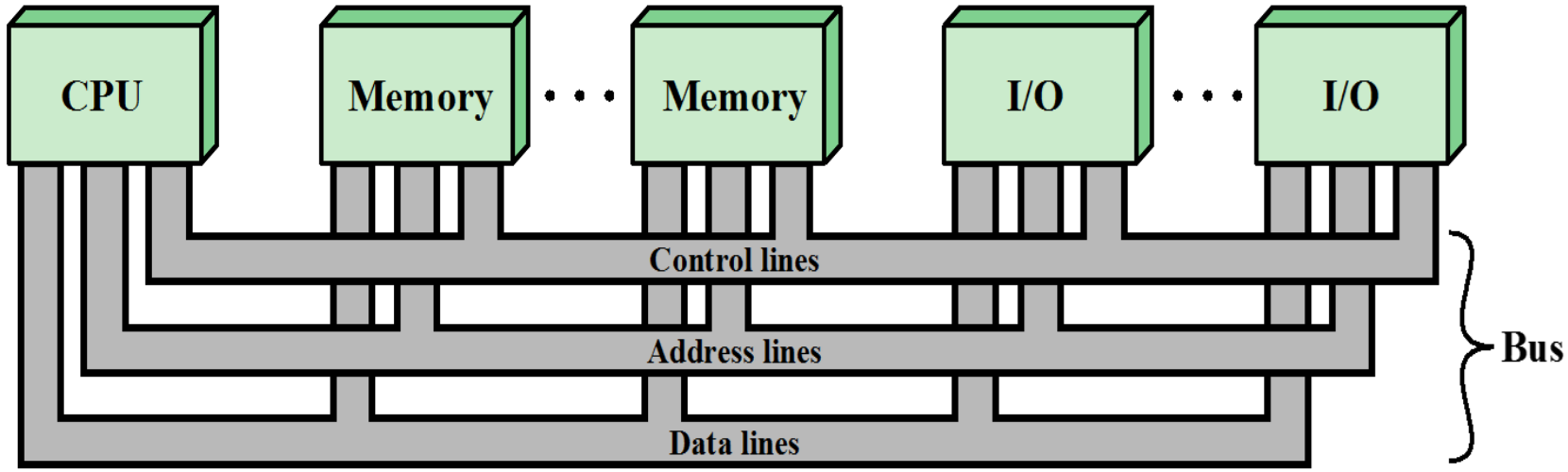
Bus Interconnection (1 of 2)

- A communication pathway connecting two or more devices
  - Key characteristic is that it is a shared transmission medium
- Signals transmitted by any one device are available for reception by all other devices attached to the bus
  - If two devices transmit during the same time period their signals will overlap and become garbled
- Typically consists of multiple communication lines
  - Each line is capable of transmitting signals representing binary 1 and binary 0

Bus Interconnection (2 of 2)

- Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy
- System Bus: A bus that connects major computer components (processor, memory, I/O)
- The most common computer interconnection structures are based on the use of one or more system buses

Bus Interconnection Scheme



The operation of the bus is as follows.

- If one module wishes to send data to another, it must do two things: (1) obtain the use of the bus, and (2) transfer data via the bus.
- If one module wishes to request data from another module, it must (1) obtain the use of the bus, and (2) transfer a request to the other module over the appropriate control and address lines. It must then wait for that second module to send the data

Data Bus

- Data lines that provide a path for moving data among system modules
- May consist of 32, 64, 128, or more separate lines
- The number of lines is referred to as the width of the data bus
- The number of lines determines how many bits can be transferred at a time
- The width of the data bus is a key factor in determining overall system performance

Address Bus

- Used to designate the source or destination of the data on the data bus
  - If the processor wishes to read a word of data from memory it puts the address of the desired word on the address lines
- Width determines the maximum possible memory capacity of the system
- Also used to address I/O ports
  - The higher order bits are used to select a particular module on the bus and the lower order bits select a memory location or I/O port within the module

Control Bus

- Used to control the access and the use of the data and address lines
- Because the data and address lines are shared by all components there must be a means of controlling their use
- Control signals transmit both command and timing information among system modules
- Timing signals indicate the validity of data and address information
- Command signals specify operations to be performed