University of Glasgow

Electronic System Design

Lecture 3-4: OpAmp Imperfections Static Errors

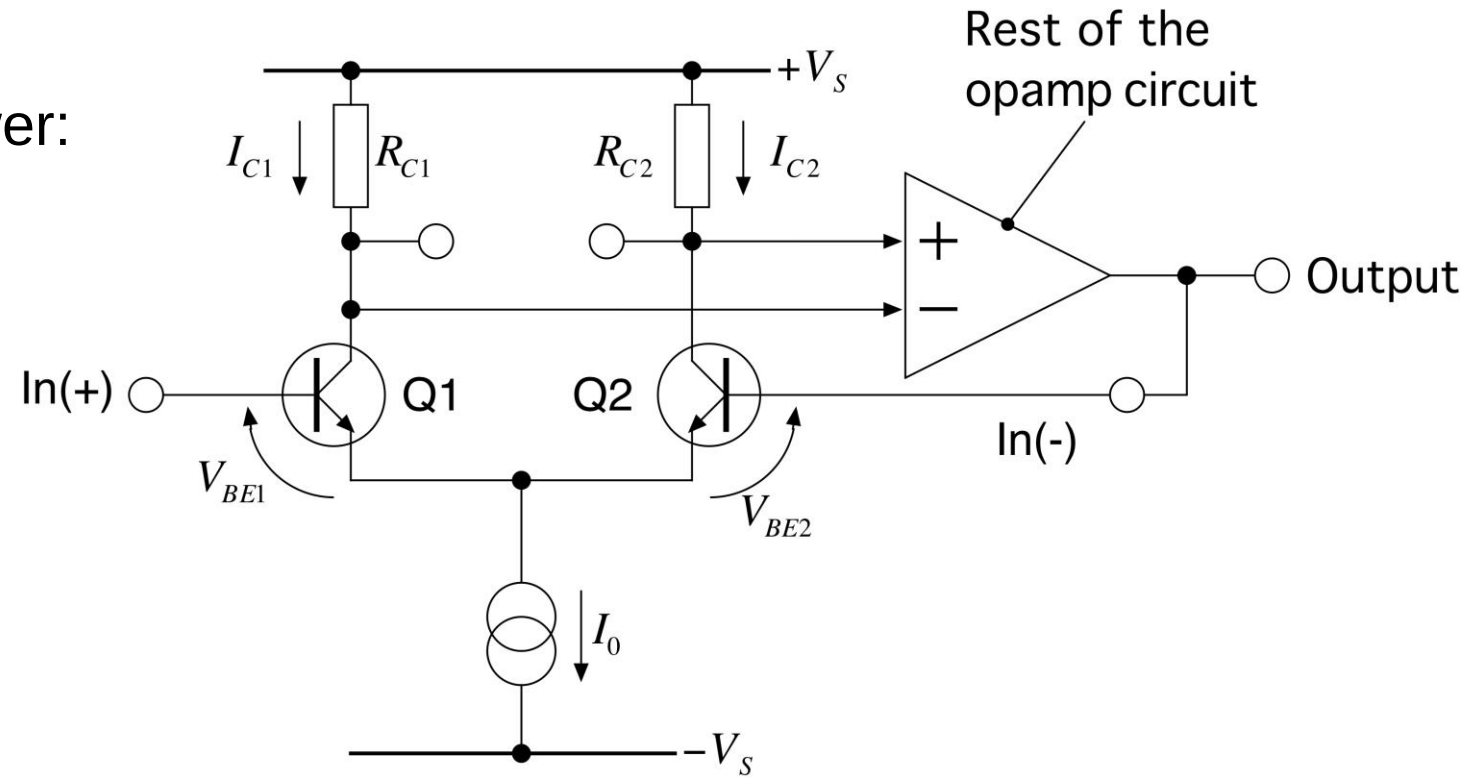
Dr Duncan Bremner

Imperfect opamps (2)

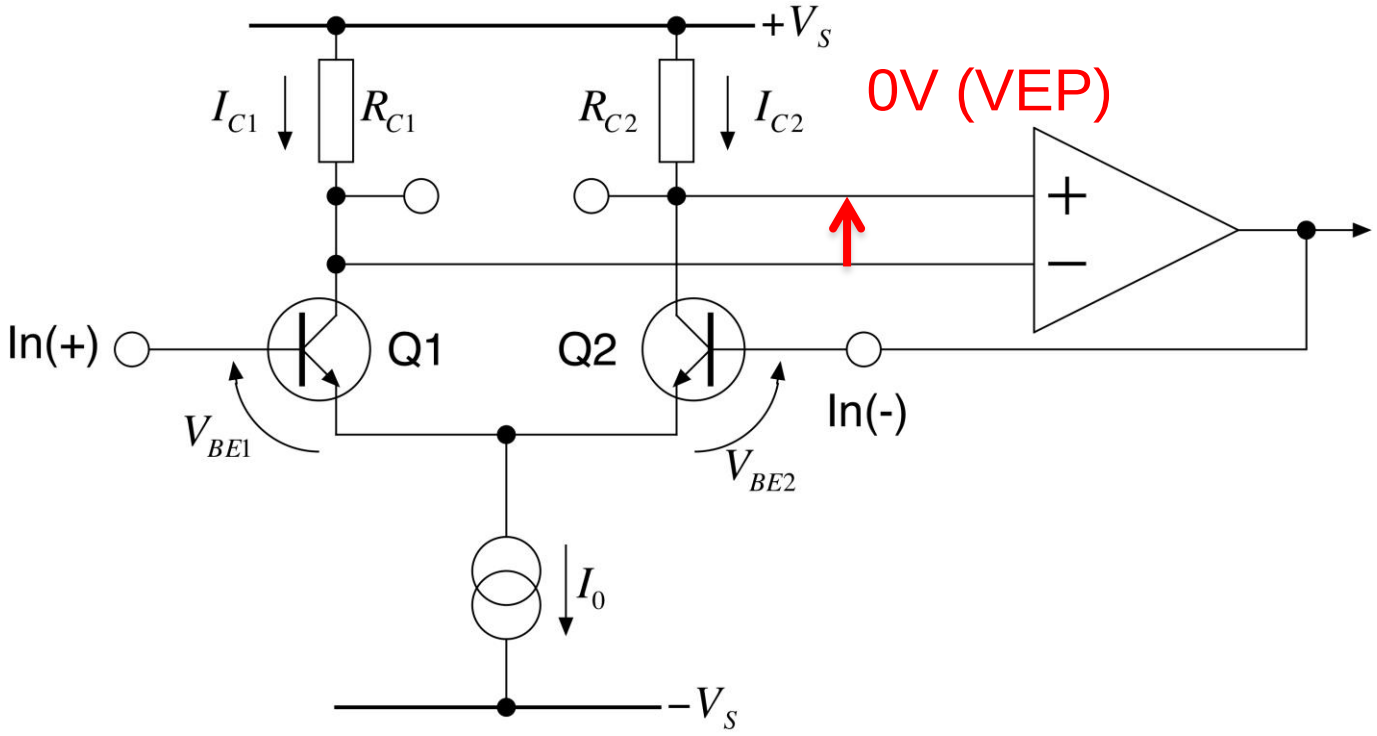
Mismatches in the input stage of an opamp will lead to an error in measuring the input *voltage* difference:

Modelling the opamp as an input stage followed by a high gain differential amplifier (an opamp!)

Voltage follower:



Imperfect Opamps (2)

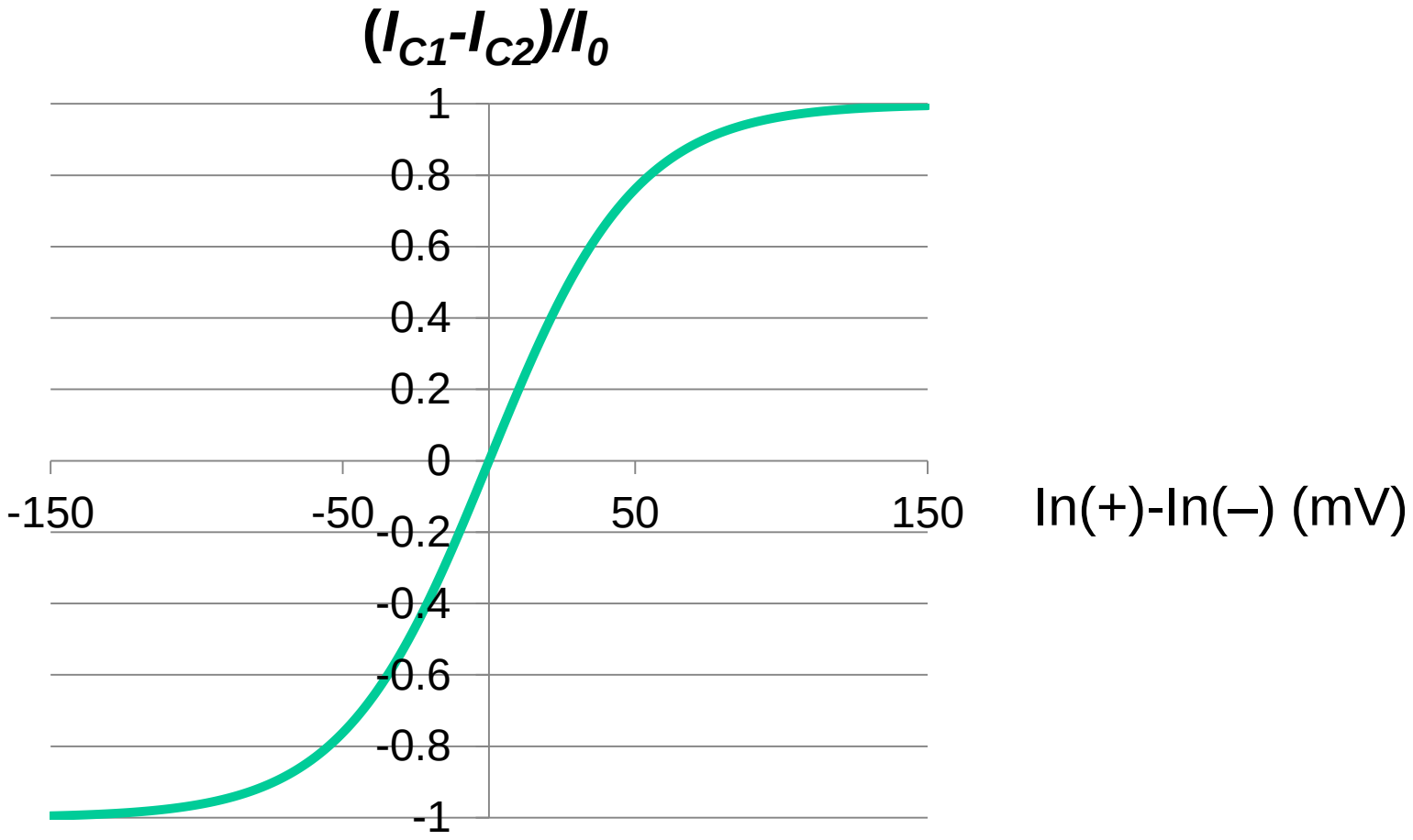


Virtual earth principle makes the two collector voltages equal

If $R_{C1} = R_{C2}$ then it follows that $I_{C1} = I_{C2}$

Imperfect Opamps (2)

For identical transistors $I_{C1} = I_{C2}$ for In(+) = In(–)



Imperfect Opamps (2)

The two transistors are different: $I_{S1} \neq I_{S2}$

$$I_{C1} = I_{S1} \cdot e^{qV_{BE1}/k_BT}$$
$$I_{C2} = I_{S2} \cdot e^{qV_{BE2}/k_BT}$$

Where $\frac{k_BT}{q} \approx 25mV$

If we require that $I_{C1} = I_{C2}$ then we must have $I_{S1} \cdot e^{V_{BE1}/25mV} = I_{S2} \cdot e^{V_{BE2}/25mV}$

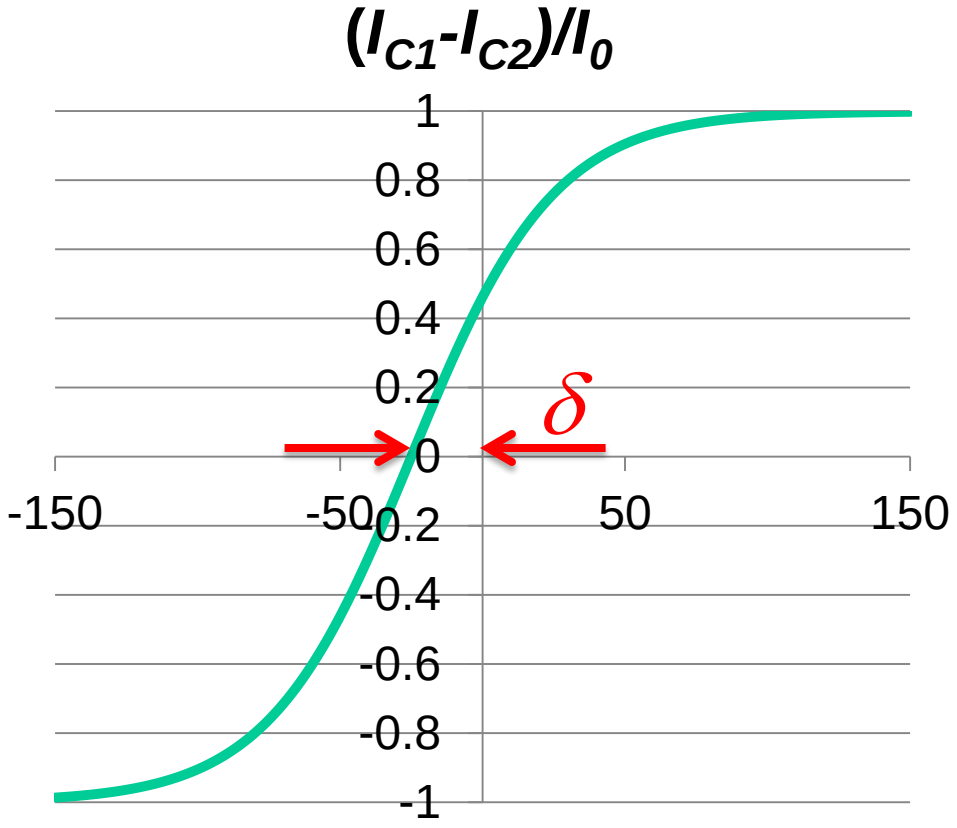
In other words $V_{BE1} \neq V_{BE2}$

To multiply by a constant factor of $\frac{I_{S1}}{I_{S2}}$ we need to add a voltage into the exponential:

$$I_{S1} \cdot e^{V_{BE1} + \frac{\delta}{2} \Big/ 25mV} = I_{S2} \cdot e^{V_{BE2} - \frac{\delta}{2} \Big/ 25mV}$$

Then the feedback loop balances when there is a small difference δ between inputs

Imperfect Opamps (2)



Since the scale of the curve is V_T and the transistor matching is good we expect the value of δ to be less than V_T : 25mV

Offset Voltage (1)

Looking at 110 bipolar opamps from RS:

29 Have offset voltage < 0.1mV

26 Have offset voltage < 0.2mV

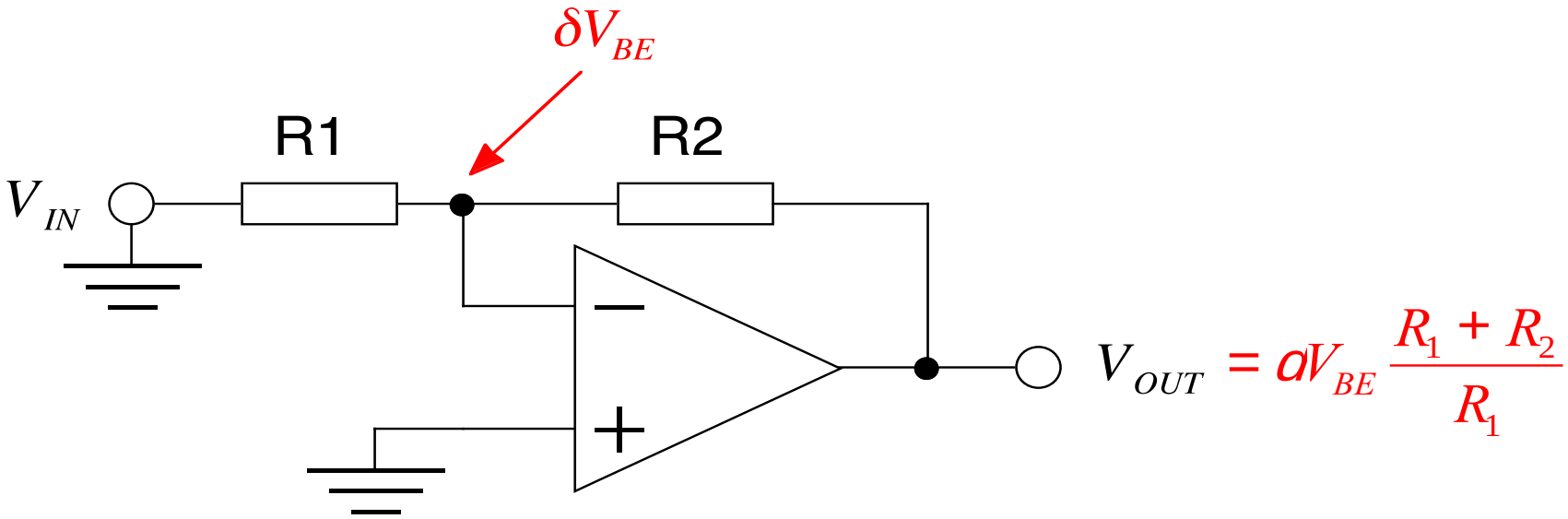
6 Have offset voltage < 1mV

14 Have offset voltage < 5mV

29 Have offset voltage < 25mV

Only 6 have offset voltage > 25mV

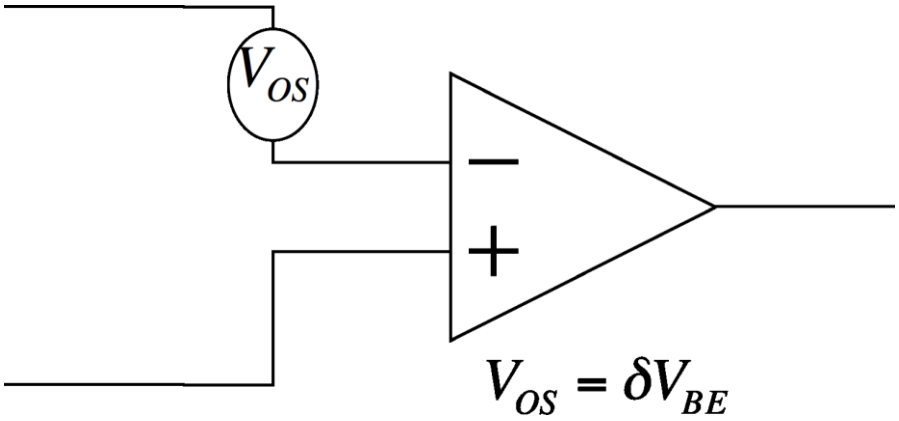
Offset Voltage (2)



Feedback makes In(-) equal to In(+) + an Offset Voltage

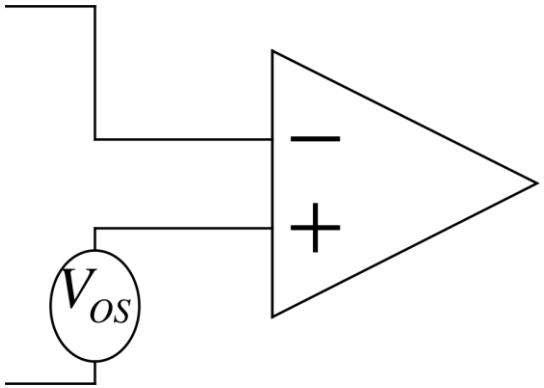
Offset voltage (3)

Equivalent circuit



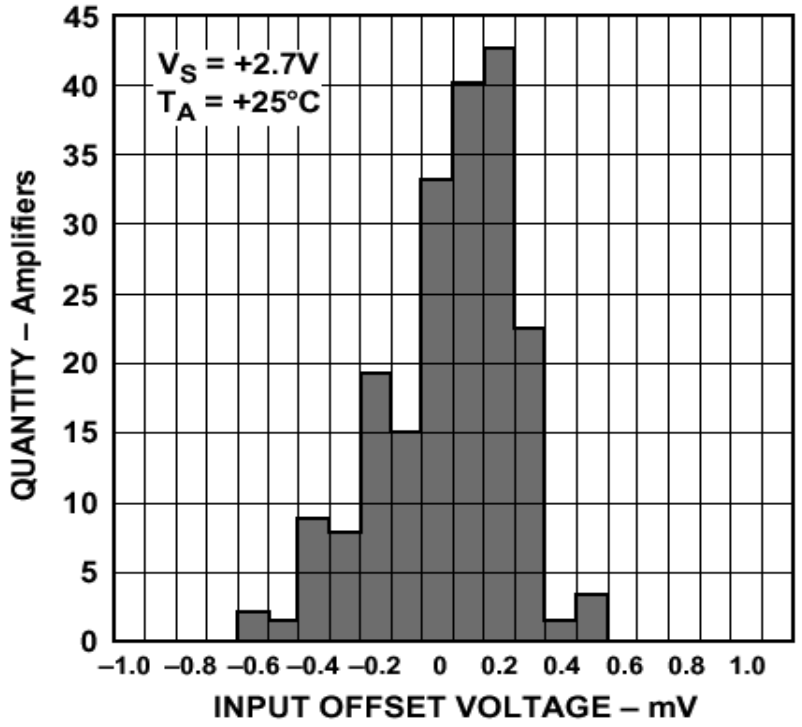
$V_{OS} = \delta V_{BE}$

Note that V_{OS} can be in series with either input
Choose whichever makes analysis easier
Theoretically need to change sign of source but…….



Offset Voltage (4)

OP181/OP281/OP481–Typical



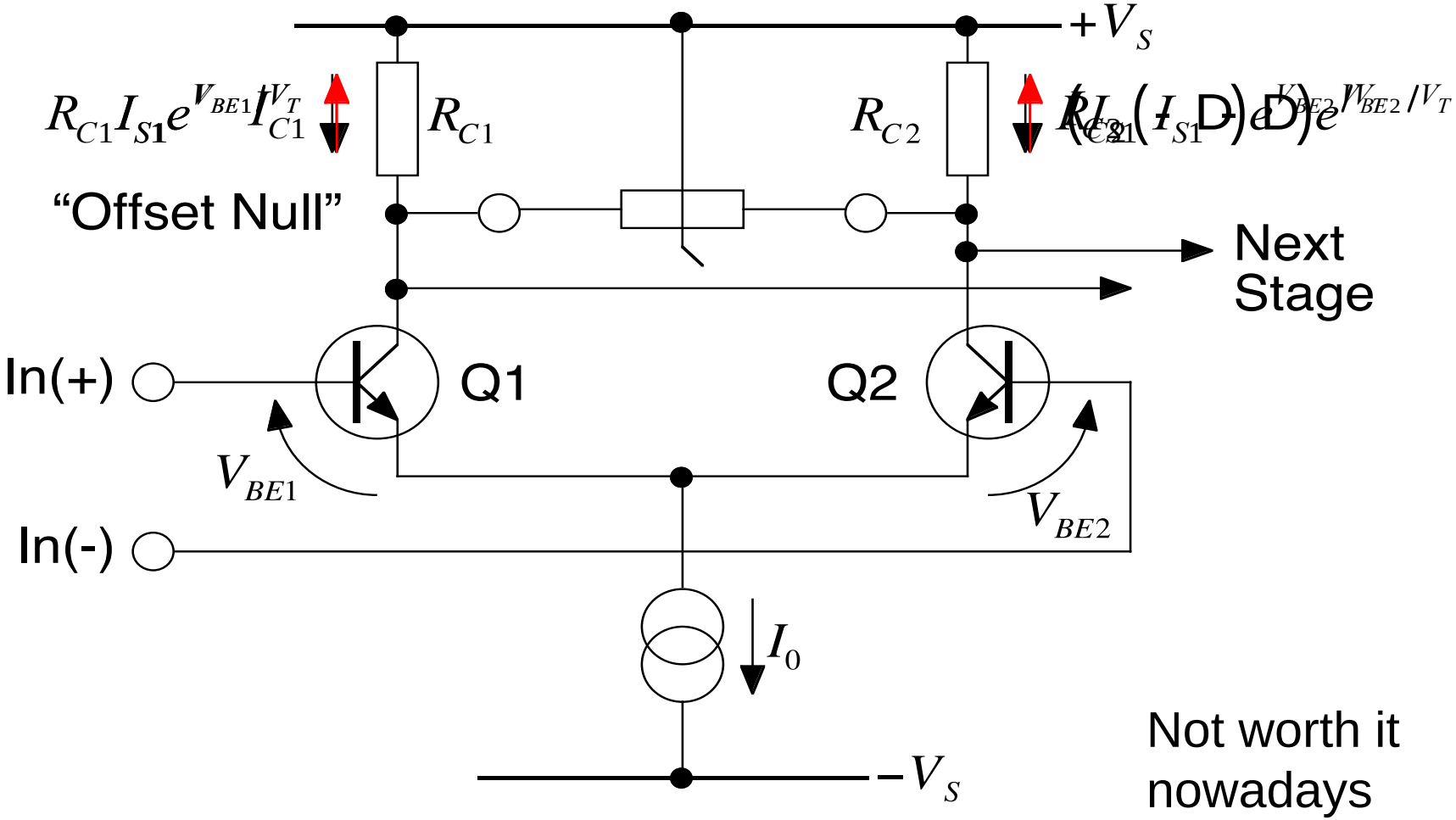
OP181 Spec:
"V_{OS}=1.5mV Max"

6-sigma specification
σ = 250µV

Offset results from inequivalence of input transistors:
Statistical, average is 0: Can have either sign.
Can be in series with either input unchanged, as the sign is undefined.

Offset voltage (5)

How to fix it — Old days: "Offset Nulling"

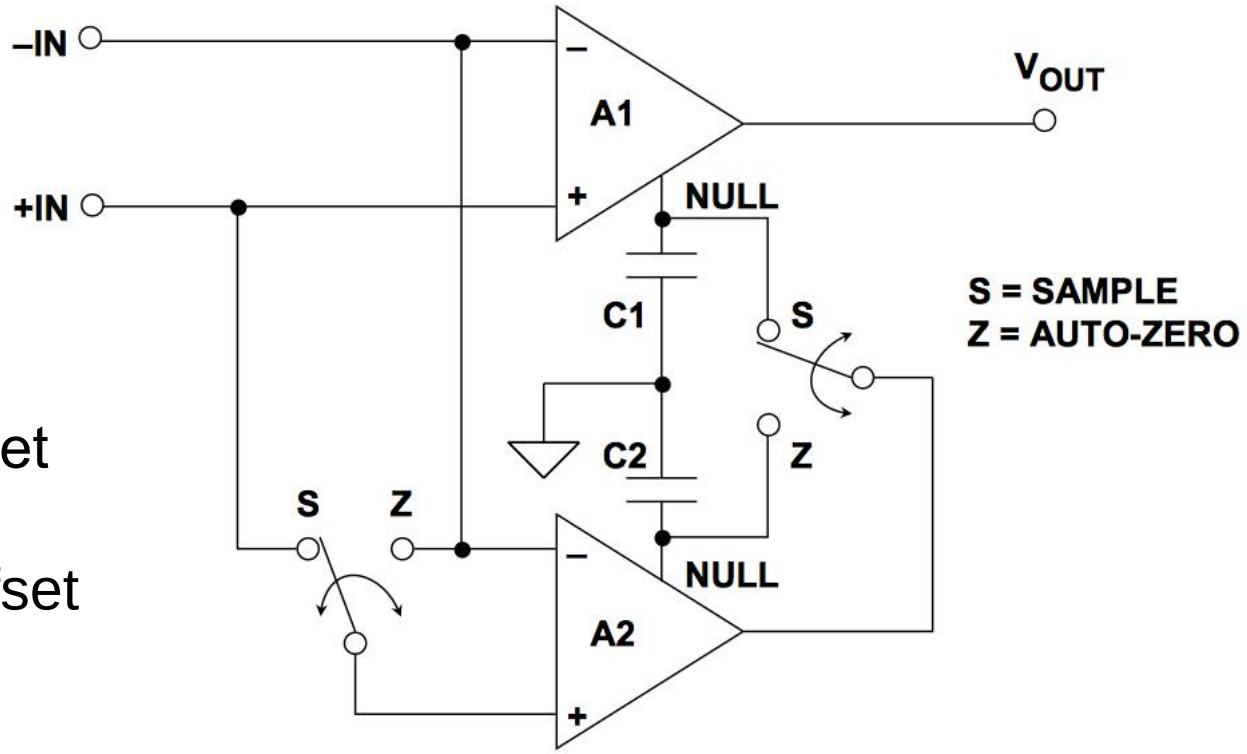


Not worth it nowadays

Offset Voltage (6)

Better methods:

- Buy a better conventional opamp
- In a digitizing system measure offset and subtract in software
- Chopper stabilization:



Z: A2 measures and corrects it's own offset voltage
S: A2 corrects A1 offset voltage

http://www.analog.com/media/en/training-seminars/tutorials/MT-055.pdf

Offset Voltage (7)

Chopper Stabilization:

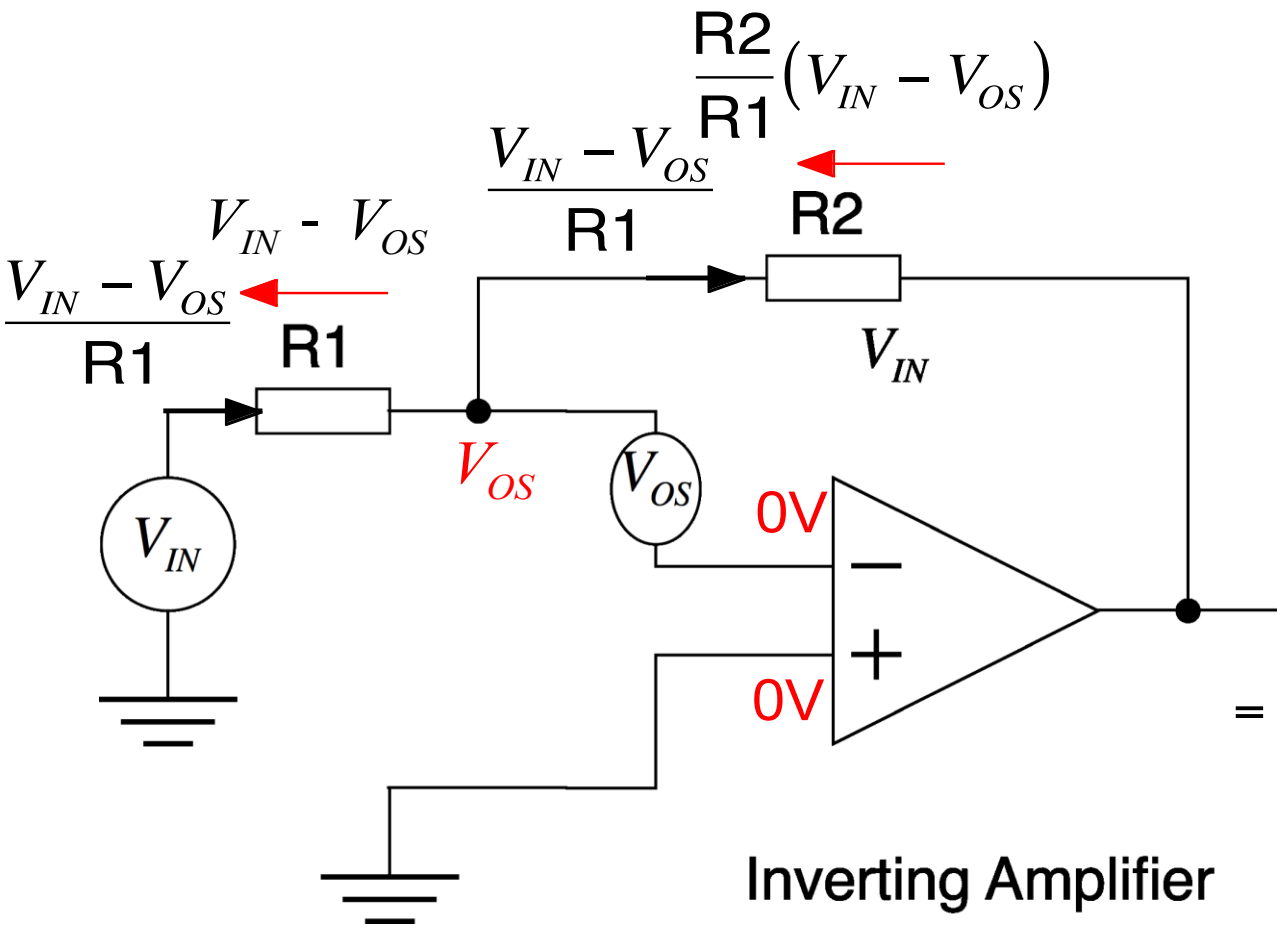
- Lowest V_{OS} (TLC2652 1µV max!)
- Low I_B (CMOS amplifier)
- Zero 1/f noise (will become clear later)
- Compatible with single supply operation / low power
- Full bandwidth linear amplification
- Enormous DC gain (A1 + A2 gains!)

BUT

- Switching noise at ≈ 10kHz
- Multiple chopper amplifiers: Switching noise can beat at low frequencies (needs to be synchronized)
- Saturation of A1 leads to a big voltage difference which A2 tries to correct: Insanely slow recovery from saturation / power-up

Use for special occasions only!

Example 1 Inverting Amplifier



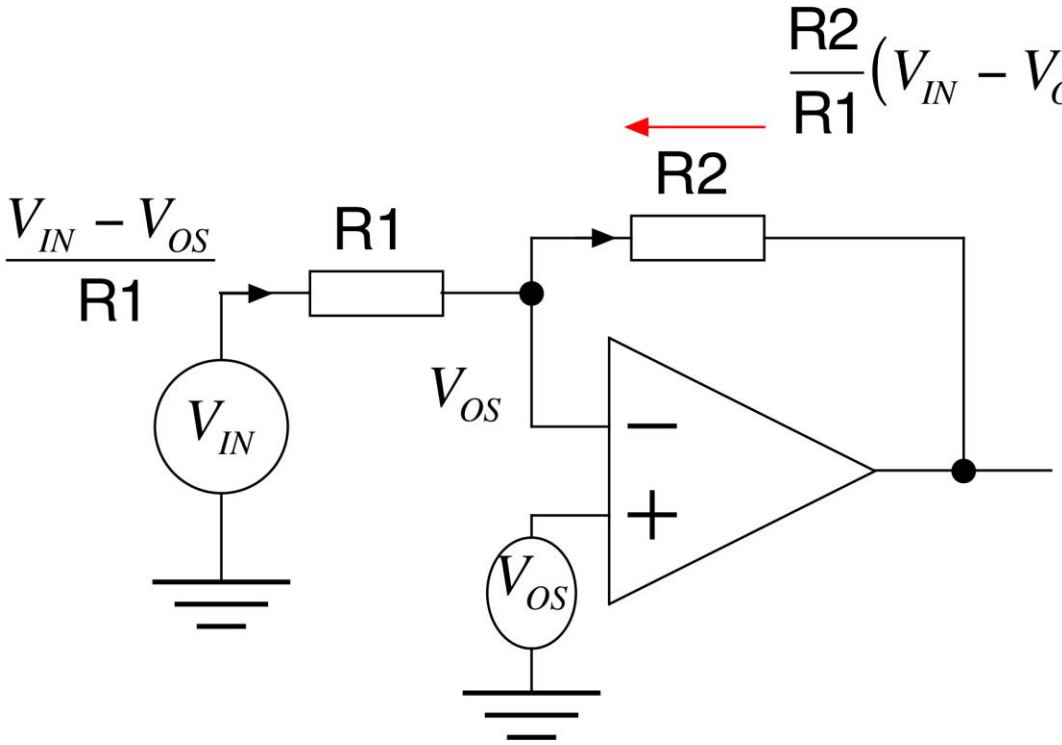
$$V_{OS} - \frac{R2}{R1}(V_{IN} - V_{OS})$$

$$= -\frac{R2}{R1}(V_{IN}) + \frac{R2 + R1}{R1}V_{OS}$$

Noninverting gain for V_{OS} error

Example 1 (again)

V_{OS} is a source representing a lack of symmetry: It can be placed in Series with either input

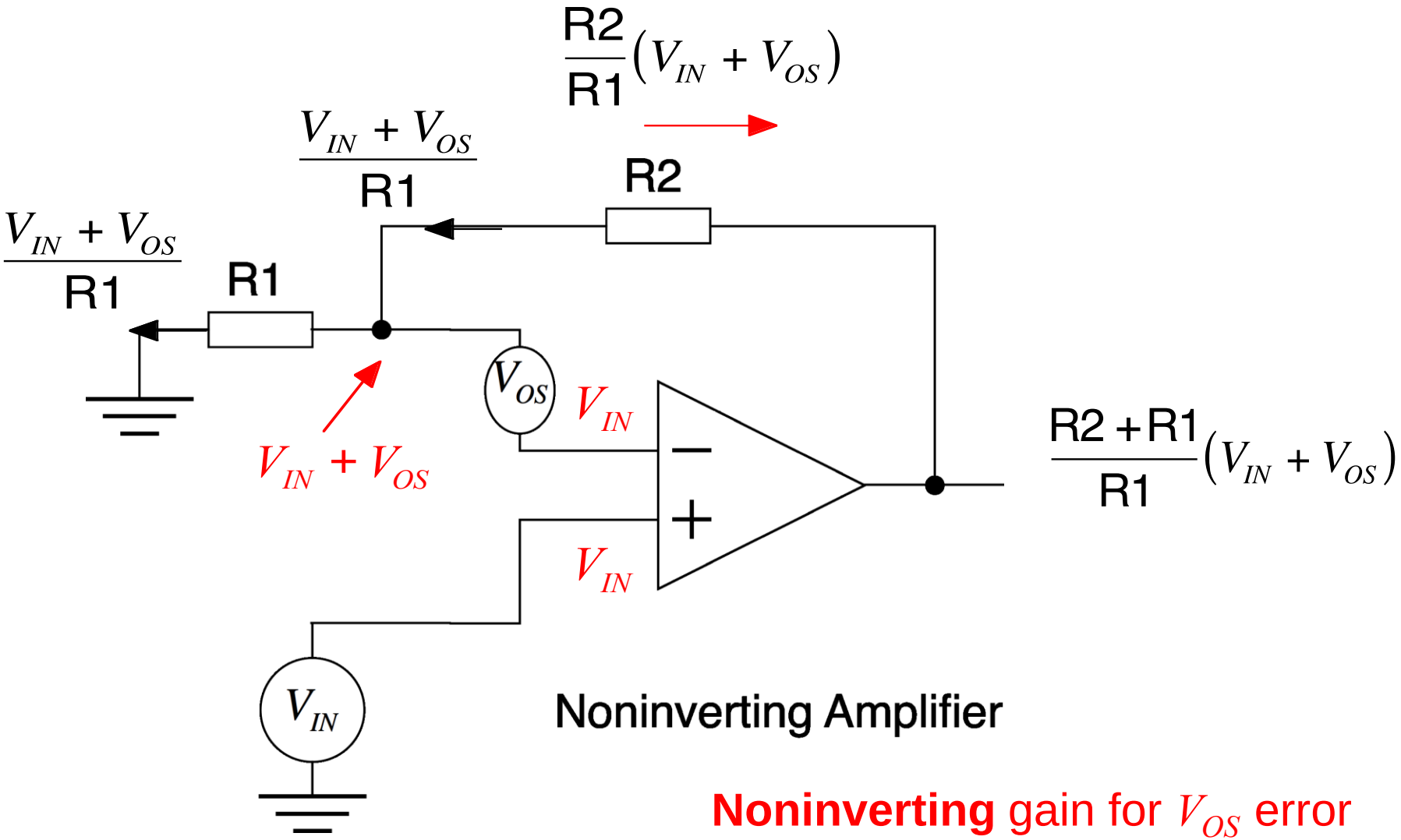


$$V_{OS} - \frac{R2}{R1}(V_{IN} - V_{OS})$$

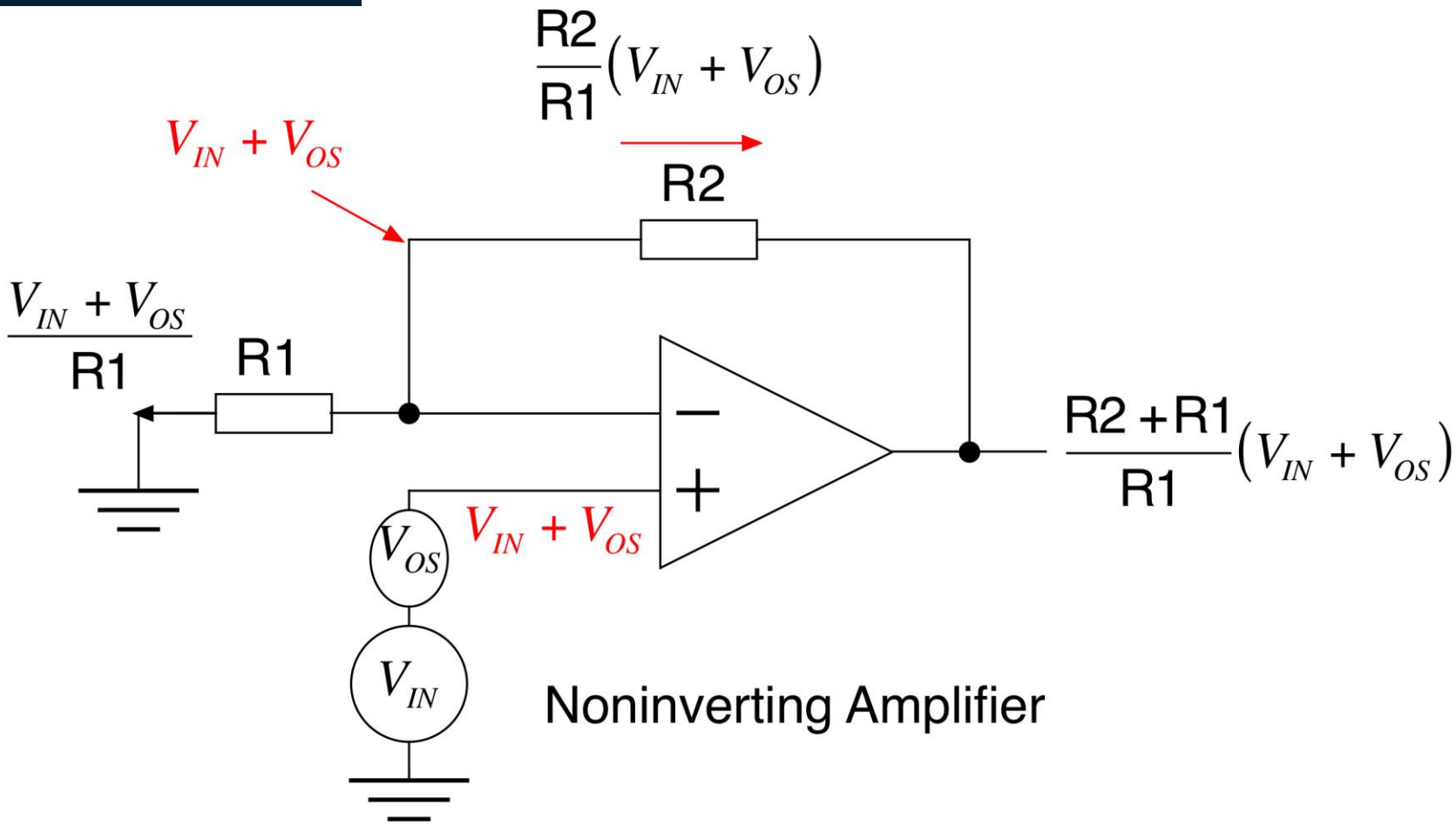
$$= -\frac{R2}{R1}V_{IN} + \frac{R2+R1}{R1}V_{OS}$$

1: Sign doesn't matter 2: Simpler calculation 3: Noninverting gain!

Example 2 Noninverting Amplifier



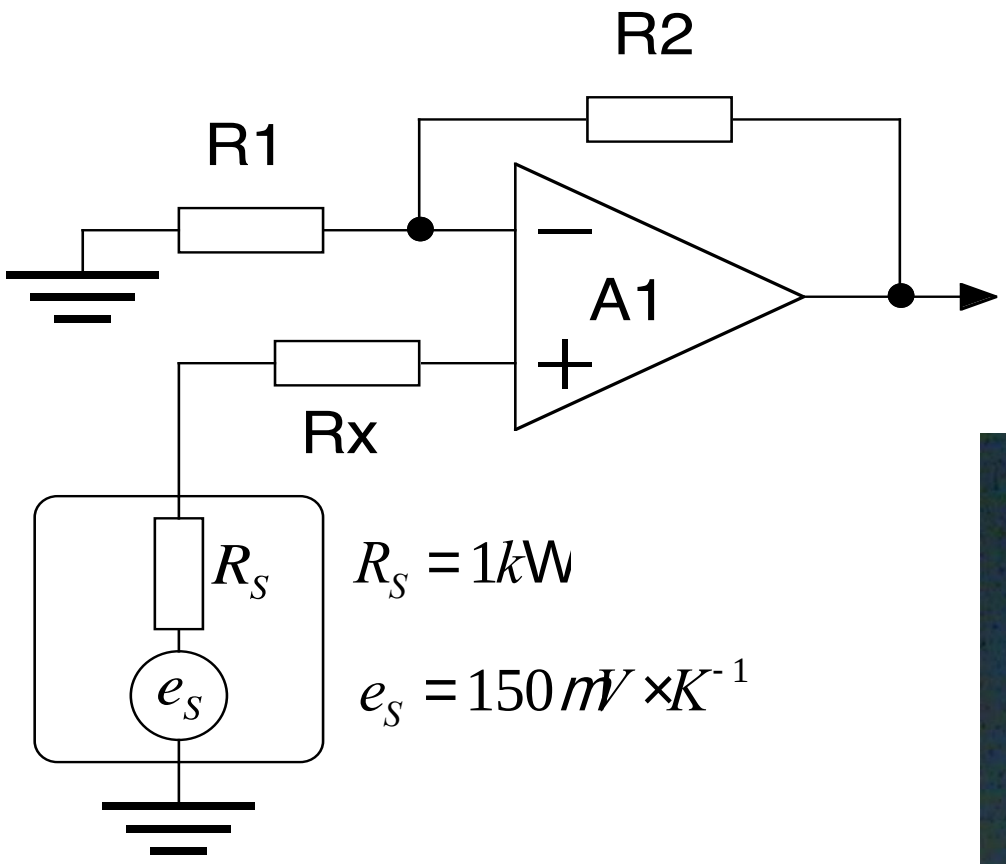
Noninverting gain for V_{OS} error



Same result by a more obvious method

Design example

Thermocouple Amplifier

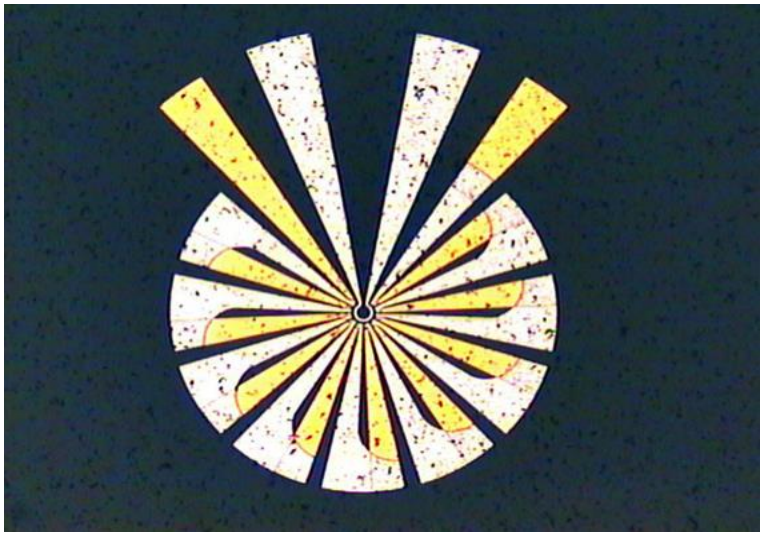


Specification:

O/P = 10mV K^{-1}

Better than 1K accuracy

At 20K difference

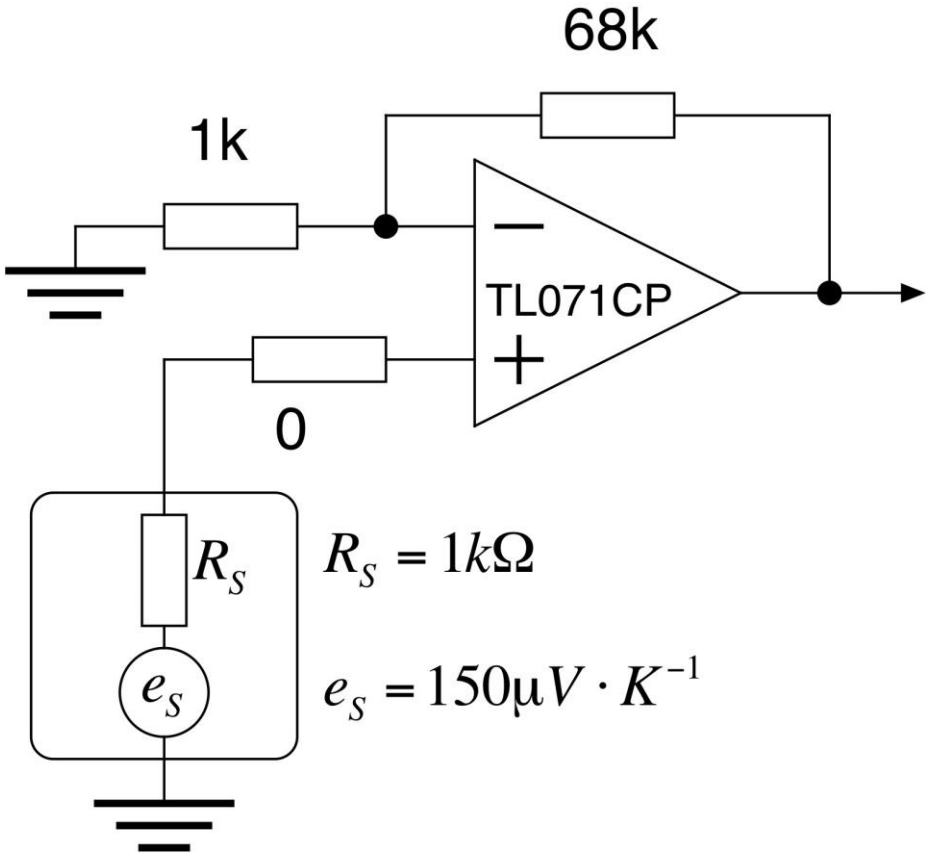


Picture Courtesy Erik Johansson

Design Example (2)

$150\mu V \cdot K^{-1} \rightarrow 10mV \cdot K^{-1} \quad \therefore \text{Gain} = 67$

Naïve Design:



(1% resistors)

Errors to consider

Offset voltage
Bias Current
Offset Current
Gain Error

TL071CP Datasheet

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ			±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full ra				±12			±12			±12			
		R_L ≥ 2 kΩ					±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R	25°C				50	200		50	200		50	200		V/mV
B_1	Unity-gain bandwidth															
r_i	Input resistance															
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R														
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±, V_O = 0, R														
I_{CC}	Supply current (each amplifier)	V_O = 0, N														
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100														

† All characteristics are measured under open-loop
‡ Full range is T_A = 0°C to 70°C for TL07_C,TL07_A
§ Input bias currents of a FET-input operational ampl
that maintain the junction temperature as close to t

LOW-NOISE

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			
				MIN	TYP	MAX	MIN
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10	
			Full range			13	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18		
I_{IO}	Input offset current	V_O = 0	25°C		5	100	
			Full range			10	
I_{IB}	Input bias current§	V_O = 0	25°C		65	200	
			Full range			7	

Design example (3)

Offset Voltage error (Noninverting)

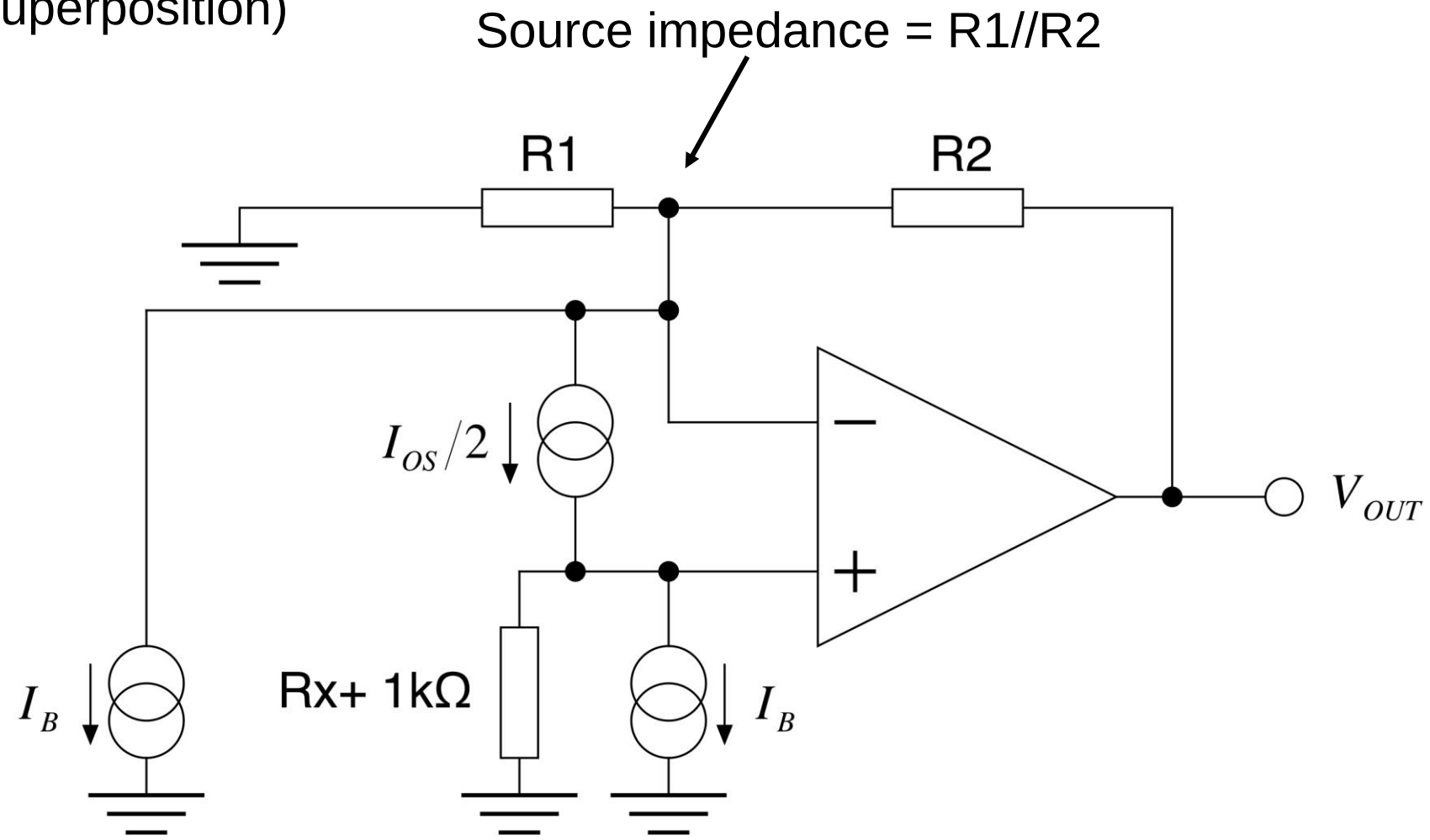
$$V_{OUT} = \frac{R2 + R1}{R1}\left(V_{IN} + V_{OS}\right)$$

$$V_{OUT} = 69\left(V_{IN} + V_{OS}\right) = 69\left(V_{IN} + 10mV\right) = 69\left(V_{IN}\right) + 690mV$$

Error due to input offset voltage = 69K

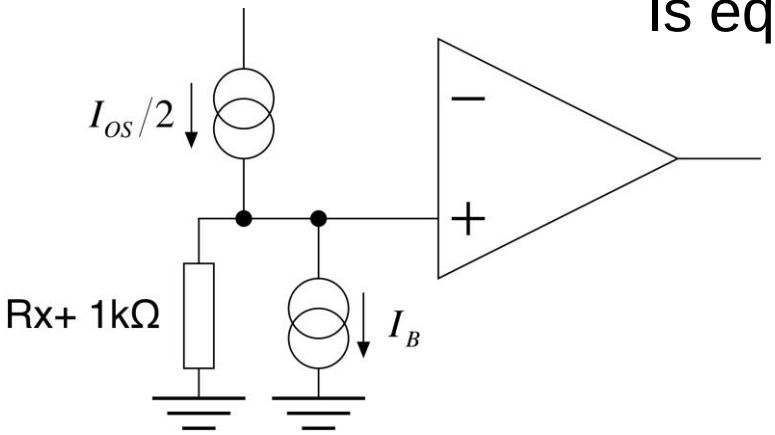
Design Example (4)

Bias and offset current error: Assume all other sources zero (Superposition)

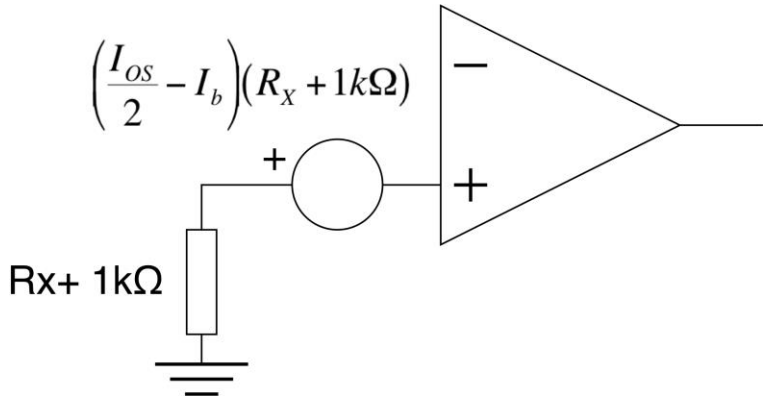


Design Example (5)

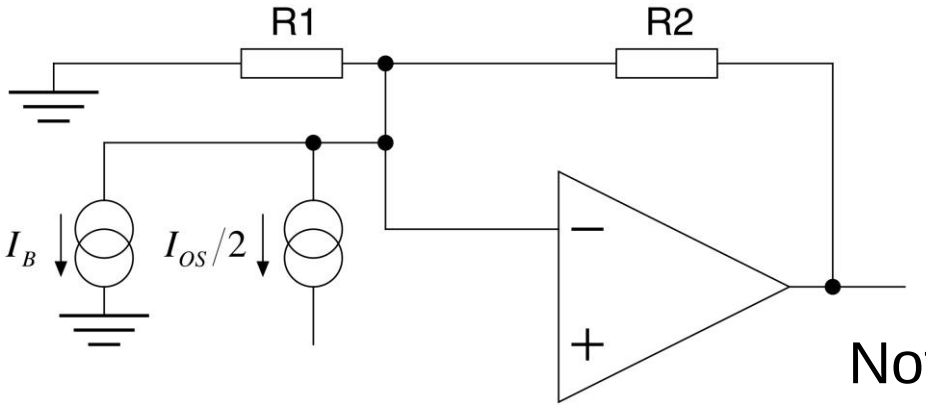
Currents flowing into inputs are equivalent to voltages in series with the inputs:

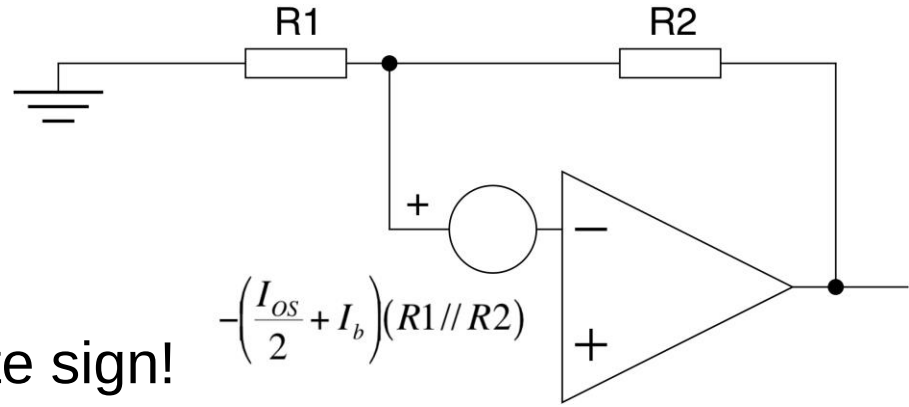


Is equivalent to



Is equivalent to

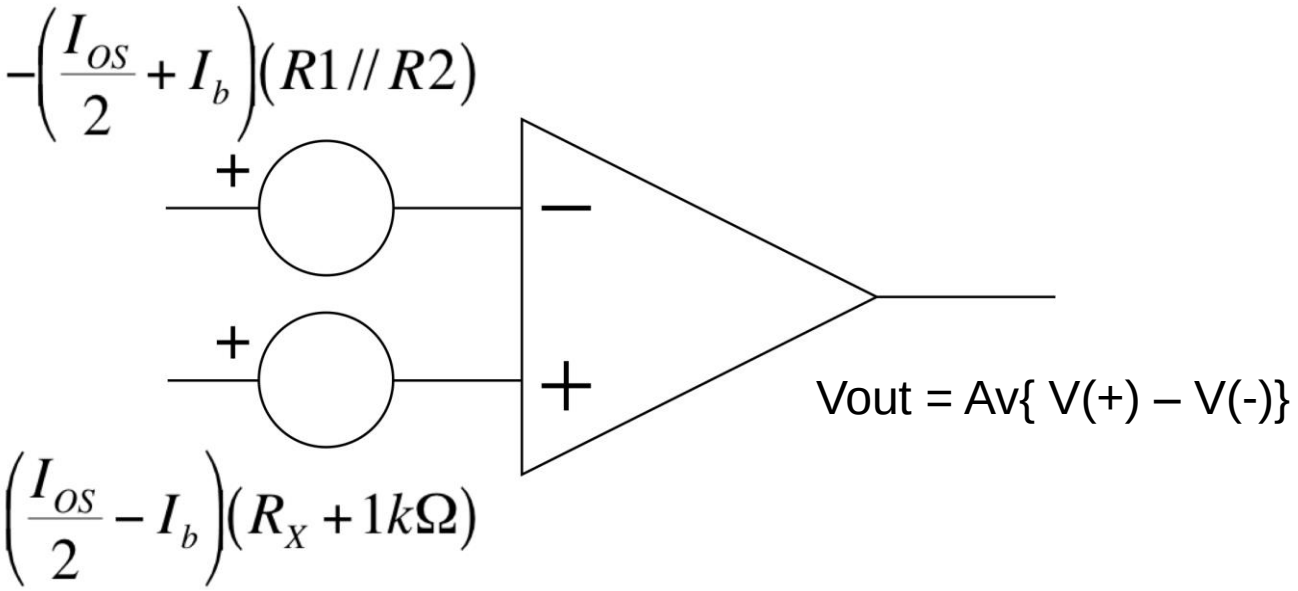




Note sign!

Design example (6)

So the current errors appear as input voltage errors

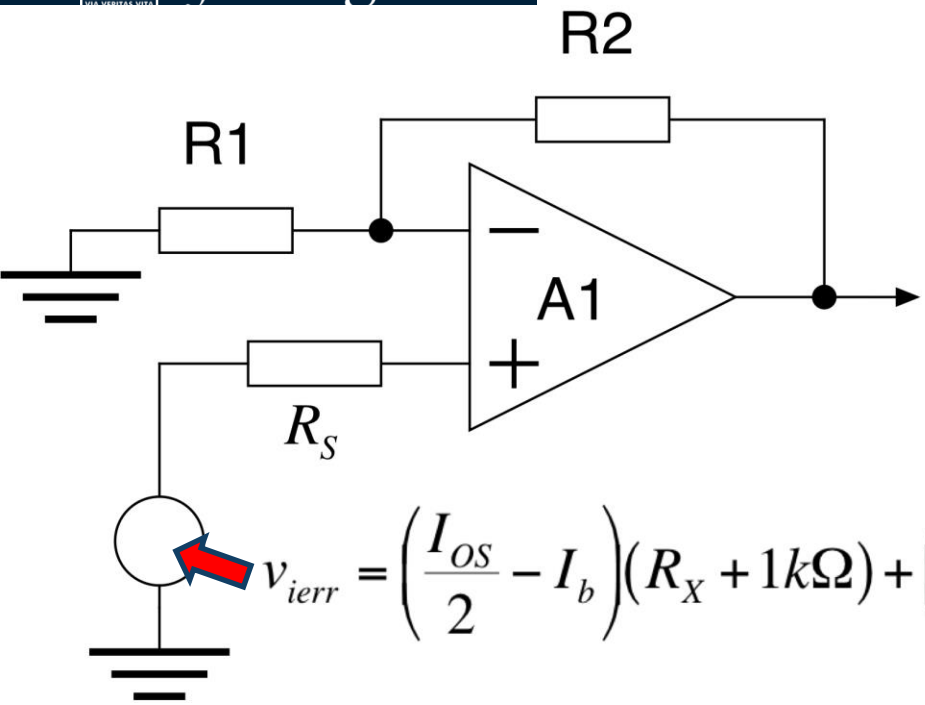


Error due to input current is equivalent to a voltage offset of

$$v_{ierr}=\left[\left(\frac{I_{OS}}{2}-I_b\right)(R_X+1k\Omega)\right]-\left[-\left(\frac{I_{OS}}{2}+I_b\right)(R1//R2)\right]$$

(Note sign)

Design Example (7)



Source resistance R_S = 1kΩ is approximately the same as 1kΩ//69kΩ, so no matching resistor; Rx = 0

$$v_{ierr} = \left(\frac{I_{OS}}{2} - I_b\right)(R_X + 1k\Omega) + \left(\frac{I_{OS}}{2} + I_b\right)(R1 // R2)$$

Error RTO due to current error is

$$v_{iout} = 69 \cdot \left(\left(\frac{I_{OS}}{2} - I_b\right)(1k\Omega) + \left(\frac{I_{OS}}{2} + I_b\right)(0.986k\Omega)\right)$$

$$= 69 \cdot \left(\frac{I_{OS} \cdot 1.986k\Omega}{2} - I_b(1 - 0.986k\Omega)\right)$$

Design Example (8)

Note that **we don't know** the sign of offset current, or the offset voltage, so we just **take the total magnitude** of the error:

$$v_{iout} = 69 \cdot \left(I_{OS} \cdot 0.993k\Omega + I_b \cdot 0.014k\Omega \right)$$

$I_B = 200\,pA \quad \therefore$ error at O/P $= 2.8nV \cdot 69 = 194nV$

Error due to input bias current = 19.4µK

Offset current error:

$I_{OS} = 100\,pA \therefore$ error at $\mathrm{O/P} = 99nV \cdot 69 = 6.8\mu V \equiv 0.7mK$

Corrected

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Design Example (9)

Summary:

Offset voltage error = 69K	Worst error! Kill! Kill! kill!
Bias Current error = 19.4µK	Negligible
Offset Current error = 0.7mK	Negligible
Gain Error (systematic) = 0.68K	Need to do a bit better
Gain error (random) = 0.4K	Maybe OK, maybe not...

Overall error should be no more than 1K

To be continued….

Design Example (10) Error Budgets

From naïve design, V_{OS} is most difficult problem, then gain.

Specification:
O/P = 10mV K^{-1}
Better than 1K accuracy
At 20K difference

Need some way to distribute Errors rationally

Define a budget for the errors

- V_{OS} is worst: Big Budget
- Gain is almost OK. => Moderate budget
- Current errors are negligible. =>Tiny Budget.

Design Example (11) Error Budgets (2)

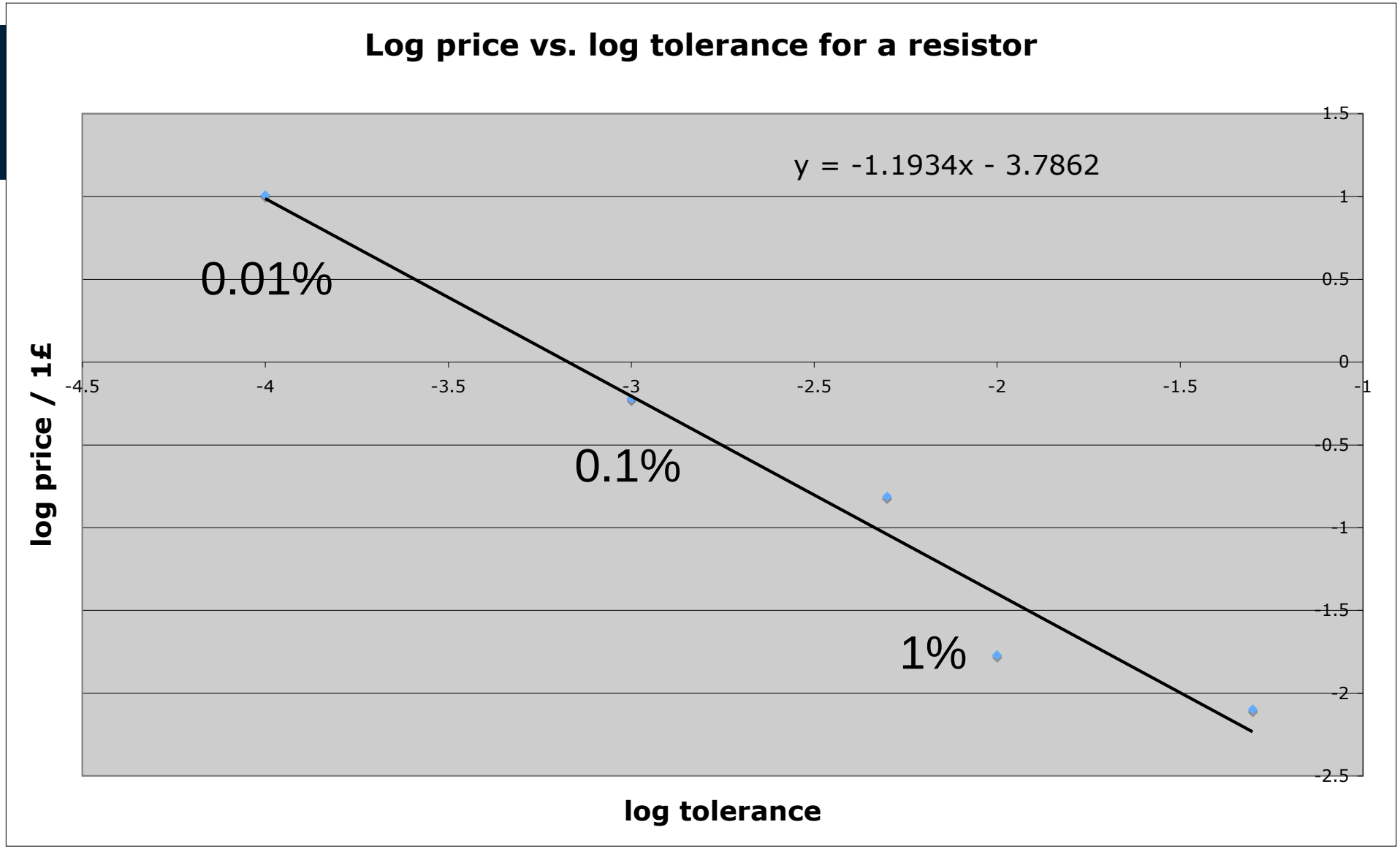
(OK to use background information:) (Prices are indicative)

- 5% Resistor £0.008
- 1% Resistor £0.017
- 0.5% Resistor £0.154
- 0.1% Resistor £0.60
- 0.01% Resistor £10.20

The Budget:

- V_{OS} 0.5K — Implies $V_{OS} \leq 0.5K * 150\mu V/K = 75\mu V$
- Gain 0.35K — Implies 0.5% resistors
- I_B, I_{OS} 0.1K — Implies $I_{OS} * 0.993k\Omega \leq 0.1K * 150\mu V/K = 15\mu V$
  $\Rightarrow I_{OS} \leq 15nA$

Note– The budget is something you **choose**: There is no perfect answer. If necessary you can redistribute later on.



Cost of a resistor is proportional to 1 / tolerance

Design example (12) Error Budgets (3)

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Hunt the Opamp!

Note: Choose one you can actually get: Farnell, RS...

Some technologies are intrinsically bad: ignore (e.g. current feedback)

Ignore things which may be a problem and don't help with the present problem (e.g. fast amps)

Start with cheap components

Limit to available power supply (± 15V in this case)

Eliminate on main spec first $V_{OS} \leq 75\mu V$

Design Example (13) Error budgets (4)

Use design tools; e.g. TI, Analog, Linear or distributors: Digi-Key;

Product Index > Integrated Circuits (ICs) > Linear - Amplifiers - Instrumentation, OP Amps, Buffer Amps

sort on price

Product Index > **Integrated Circuits (ICs)** > **Linear - Amplifiers - Instrumentation, OP Amps, Buffer Amps**

To get the most from Digi-Key's part search:

Only select from one box at a time, click the "Apply Filters" button, and repeat.
To select multiple values within a box, hold down 'Ctrl' while selecting values within the box.

Series	Manufacturer	Amplifier Type	Number of Circuits	Output Type	Slew Rate	Gain Bandwidth Product	-3db Bandwidth	Current - Input Bias	Voltage - Input Offset	Current Supply
*	Advanced Linear Devices Inc	-	-	Buffered	0.0027 V/µs	-	*	*	50µV	*
-	ams	Audio	1	CMOS	0.003 V/µs	1kHz	-	-	60µV	-
Apex Precision Power®	Analog Devices Inc	Auto-Zero	2	CMOS, Rail-to-Rail	0.004 V/µs	1.5kHz	250Hz	0.002pA	65µV	0.33µA
APEX™ 20K	Apex Microtechnology	Buffer	3	Differential	0.0041 V/µs	2kHz	500Hz	0.003pA	70µV	0.35µA
Beyond-the-Rails™	Avago Technologies US Inc.	Chopper (Zero-Drift)	4	Differential, Rail-to-Rail	0.0042 V/µs	2.5kHz	1kHz	0.005pA	74µV	0.4µA
BI-FET II™	CEL	Current Feedback	5	Open Drain	0.0045 V/µs	2.7kHz	1.5kHz	0.01pA	75µV	0.45µA
BI-FET™	Cirrus Logic Inc	Current Sense	6	Phase Reversal Free, Rail to Rail	0.005 V/µs	3kHz	2.5kHz	0.02pA	80µV	0.475µA
C-Load™	Diodes Inc	Differential	8	Push-Pull	0.006 V/µs	3.5kHz	3.1kHz	0.03pA	85µV	0.6µA
CLAMPIN™	Diodes Inc	General Purpose	10	Push-Pull, Rail-to-Rail	0.0077 V/µs	4kHz	5kHz	0.04pA	90µV	680nA
Difet®	Fairchild Optoelectronics Group	Instrumentation	12	Rail-to-Rail	0.01 V/µs	5kHz	7.5kHz	0.05pA	95µV	0.7µA

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Page 1/1,239 (1 2 3 4 5 6 7 8 9 10 ... Last Next)

All prices are in British pound

Image	Digi-Key Part Number	Manufacturer Part Number	Description	Series	Manufacturer	Amplifier Type	Number of Circuits	Output Type	Slew Rate	Gain Bandwidth Product	-3db Bandwidth	Current - Input Bias	Voltage - Input Offset	Current - Supply	Current - Output / Channel	Voltage - Supply, Single/Dual (±)	Operating Temperature	Mounting Type	Package / Case	Supplier Device Package	Packaging	Quantity Available	Minimum Quantity	Unit Price
	296-17440-2-ND	RC4558IDR	IC OPAMP GP 3MHZ DUAL 8SOIC	-	Texas Instruments	General Purpose	2	-	1.7 V/µs	3MHz	-	150nA	500µV	2.5mA	-	10 V ~ 30 V, ±5 V ~ 15 V	-40°C ~ 85°C	Surface Mount	8-SOIC (0.154", 3.90mm Width)	8-SOIC	Tape & Reel (TR) Alternate Packaging	7,500 - Immediate 167,500 - Factory Stock	2,500	0.062
	296-17440-1-ND	RC4558IDR	IC OPAMP GP 3MHZ DUAL 8SOIC	-	Texas Instruments	General Purpose	2	-	1.7 V/µs	3MHz	-	150nA	500µV	2.5mA	-	10 V ~ 30 V, ±5 V ~ 15 V	-40°C ~ 85°C	Surface Mount	8-SOIC (0.154", 3.90mm Width)	8-SOIC	Cut Tape (CT) Alternate Packaging	7,829 - Immediate 167,500 - Factory Stock	1	0.340
	296-17440-6-ND	RC4558IDR	IC OPAMP GP 3MHZ DUAL 8SOIC	-	Texas Instruments	General Purpose	2	-	1.7 V/µs	3MHz	-	150nA	500µV	2.5mA	-	10 V ~ 30 V, ±5 V ~ 15 V	-40°C ~ 85°C	Surface Mount	8-SOIC (0.154", 3.90mm Width)	8-SOIC	Digi-Reel® Alternate Packaging	7,829 - Immediate	1	Calcul

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Design Example (13) Error budgets (5)

OP-07 seems to meet offset voltage spec, and is very cheap.

What about the offset current spec?

Budget: $I_{OS} \leq 15nA$

Download the data sheet and check I_{OS} **and** V_{OS}

V_{OS} = 60µV typical, 150µV max V_{OS} spec ≤ 75µV

I_{OS} = 0.8nA (typical) 6nA max I_{OS} spec ≤ 15nA

So the OP-07 actually **doesn't** work.

Design Example (13) Error budgets (6)

Repeat for other opamps sorted in order of price

Opamp	Price	Vos µV (typ)	Vos µV (max)	Ib pA(typ)	Ib pA(max)	Ios pA(typ)	Ios pA(max)	Comments
OP07C	0.36	60	150	1800	7000	800	6000	"Classic"
LT1013CP	0.778	60	300	15000	30000	200	1500	dual
TLC277CP	0.88	200	500	0.6	40	0.1	7	CMOS dual
TLE2022IP	1.15	150	500	35000	70000	500	6000	dual
OP177GP	1.47	20	60	500	2800	300	2800	Standard
OPA277PA	1.53	20	50	500	2800	500	2800	Improved 177
TLE2021CP	1.57	120	600	25000	70000	200	3000	
TLE2141CP	1.61	225	1400	800000	2000000	8000	100000	
OP37GPZ	2.15	30	100	15000	80000	12000	75000	Min gain 5 OP
TLC2201CP	2.19	100	500	1		0.5		CMOS
OP97FPZ	2.2	30	75	30	150	30	150	
LT1006CN8	2.52	30	80	10000	25000	150	900	
OP27GPZ	2.86	30	100	15000	80000	12000	75000	"Low noise"
LT1097CN8	2.91	10	50	40	250	40	250	
MAX492CPA	3.12	200	500	25000	60000	500	6000	Low power sin
MAX437CPA	3.18	5	15	10000	35000	7000	30000	"Low noise"
LT1057CN8	3.22	200	800	7	75	4	50	JFET
LT1050CN8	3.65	0.5	5	10	75	20	125	Chopper
OP213FPZ	3.84		150	240000	600000		50000	
TLC2652CP	4.32	0.6	3	4		2		Chopper ±5V

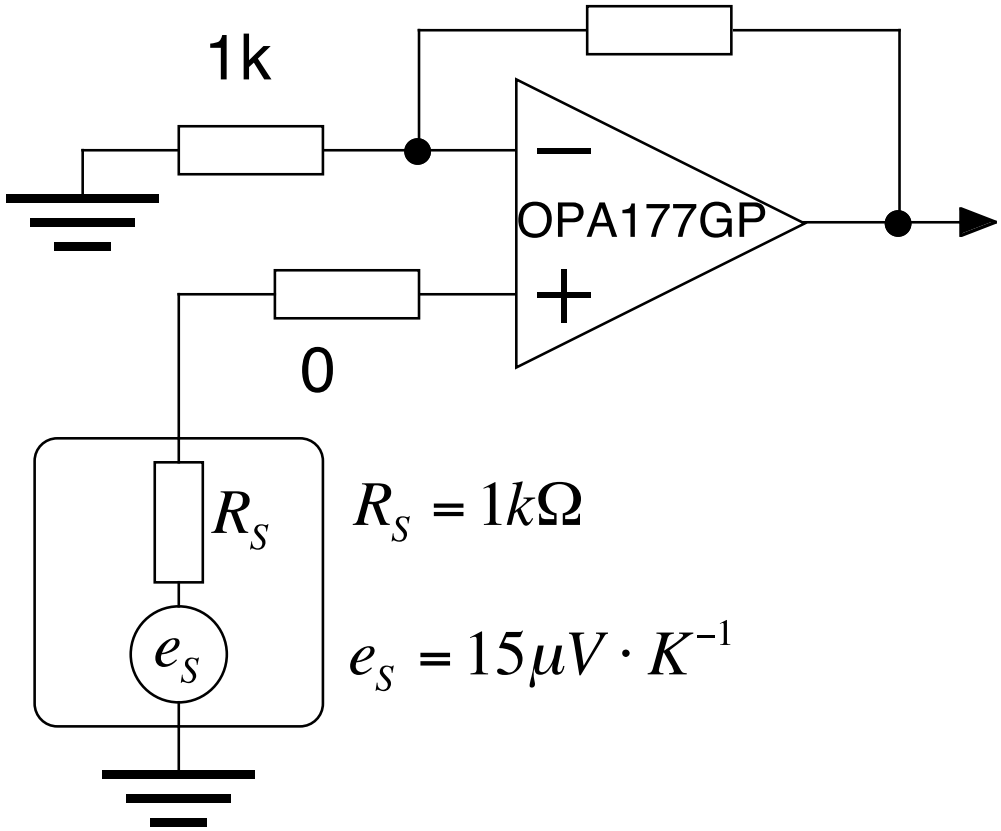
OP177 is the cheapest that works:

V_{OS}=60µV max, I_{OS}=2.8nA max £1.47 each

Design Example (16) Error budgets (7)

Final design, 0.5% resistors

68k1 (Not 64k9) // 1M8 1%



Costs:

- Naïve:
  - Amp: £0.60
  - Rs: £0.066
  - Total £0.67
- Designed:
  - Amp: £1.47
  - Rs: £0.50
  - Total £1.97

Cost x 3, accuracy x 70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Thank you
谢谢
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