Tutorial-3: Real-Time Computer Systems and Architecture

Q 1. What are the typical elements of a machine instruction?

Q 2. List and briefly explain five important instruction set design issues.

Q 3. What is the relationship between the IRA character code and the packed decimal representation?

Q 4. What is the difference between an arithmetic shift and a logical shift?

Q 5. Why are transfer of control instructions needed?

Q 6. What is the difference between big endian and little endian?

Q 7. What is the difference between postindexing and preindexing?

Q 8. What facts go into determining the use of the addressing bits of an instruction?

Q 9. What are the advantages and disadvantages of using a variable-length Instruction format?

Q 10. An address field in an instruction contains decimal value 14. Where is the corresponding operand located for:

a) immediate addressing?
b) direct addressing?
c) indirect addressing?
d) register addressing?
e) e. register indirect addressing?

Q 11. A PC- relative mode branch instruction is stored in memory at address 620_{10}. The branch is made to location 530_{10}. The address field in the instruction is 10 bits long. What is the binary value in the instruction?

Q 12. How many times does the processor need to refer to memory when it fetches and executes an indirect-address-mode instruction if the instruction is:

a) a computation requiring a single operand;
b) a branch?

Q 13. The IBM 370 does not provide indirect addressing. Assume that the address of an operand is in main memory. How would you access the operand?

Q 14. Justify the assertion that a 32-bit instruction is probably much less than twice as useful as a 16-bit instruction.

Q 15. Assume an instruction set that uses a fixed 16-bit instruction length. Operand specifiers are 6 bits in length. There are *K* two-operand instructions and *L* zero-operand instructions. What is the maximum number of one-operand instructions that can be supported?

Processor Struct. & Func.

Q 16. What general roles are performed by processor registers?

Q 17. What is the function of condition codes?

Q 18. Why is a two-stage instruction pipeline unlikely to cut the instruction cycle time in half, compared with the use of no pipeline?

Q 19. List and briefly explain various ways in which an instruction pipeline can deal with conditional branch instructions. (3大 Hazard 中的 Cont. Hazard)

Q 20. A microprocessor is clocked at a rate of 5 GHz.

a) How long is a clock cycle?

b) What is the duration of a particular type of machine instruction consisting of three clock cycles?