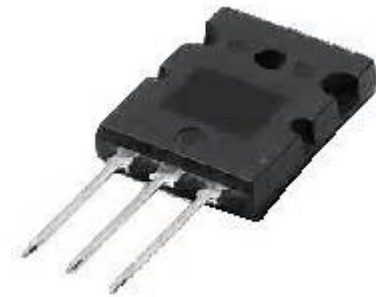
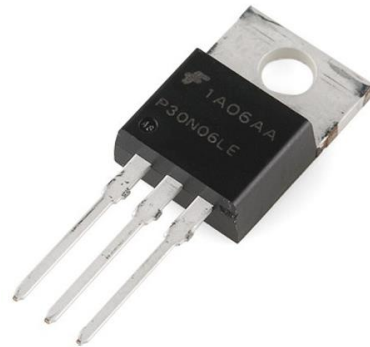


# Field Effect Transistors

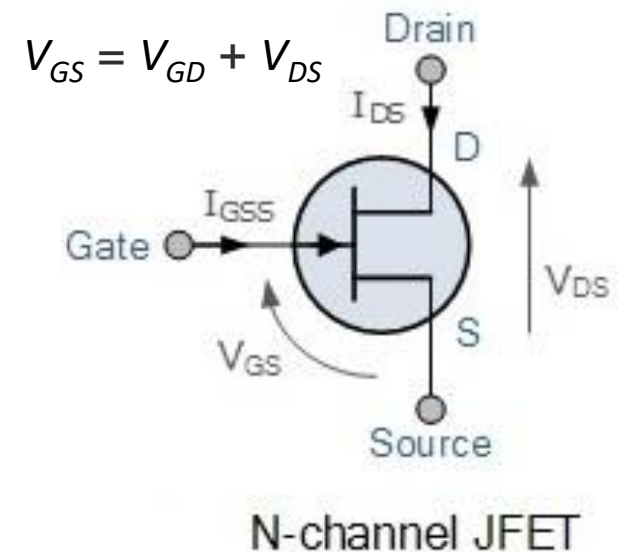
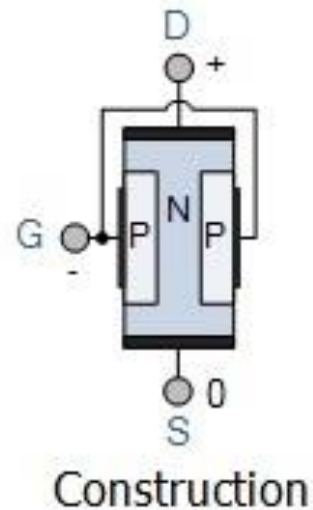
## 3002 Electronic Devices



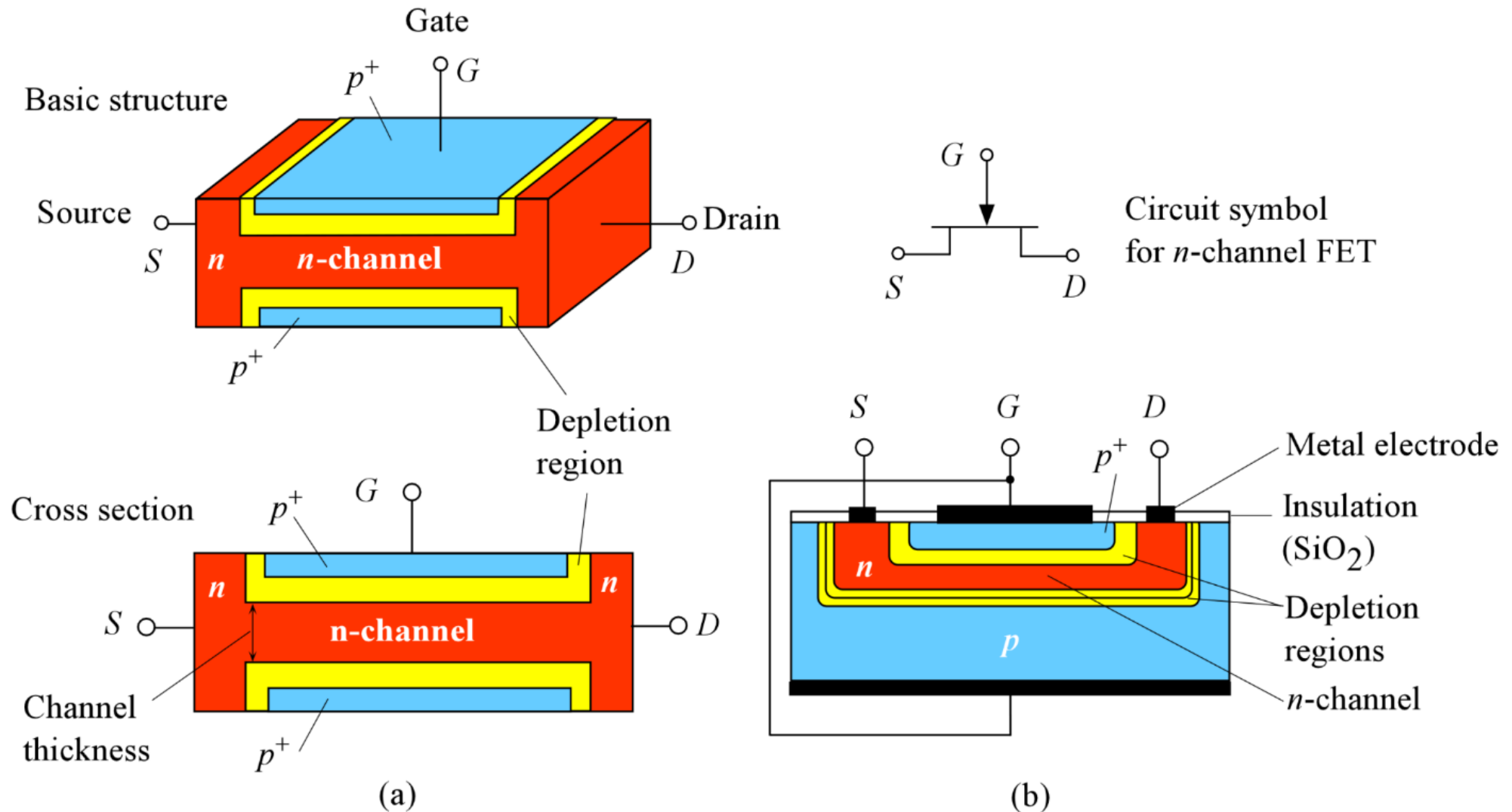
# Junction Field Effect Transistor (JFET)

There are two types:

- n-channel and p-channel.
- Very similar in physical structure to a BJT.
  - It is also a 3 terminal device
  - There are two pn-junctions
- However, JFET is a **Voltage Controlled Device**, as opposed to a **Current Controlled Device** in the case of the BJT.



# Junction Field Effect Transistor (JFET)



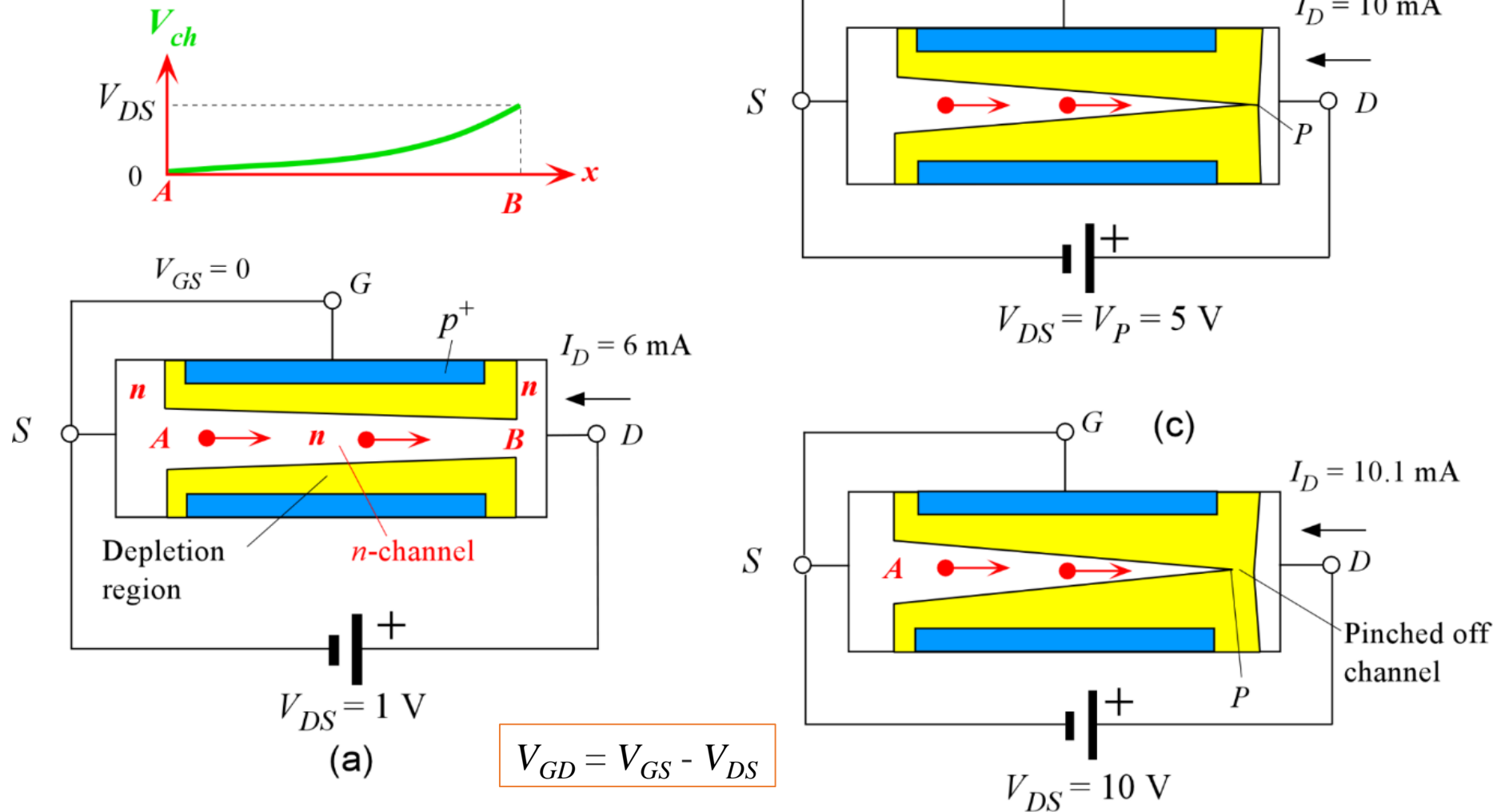
(a) The basic structure of the junction field effect transistor (JFET) with an n-channel. The two  $p^+$  regions are electrically connected and form the gate.

(b) A simplified sketch of the cross section of a more practical  $n$ -channel JFET

From *Principles of Electronic Materials and Devices*, Fourth Edition, S.O. Kasap (© McGraw-Hill Education, 2018)

3002 Electronic Devices

R. Ghannam

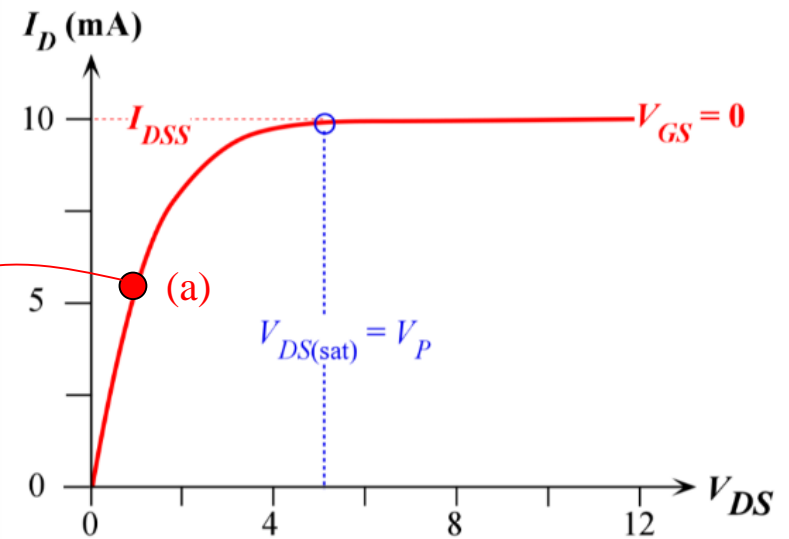
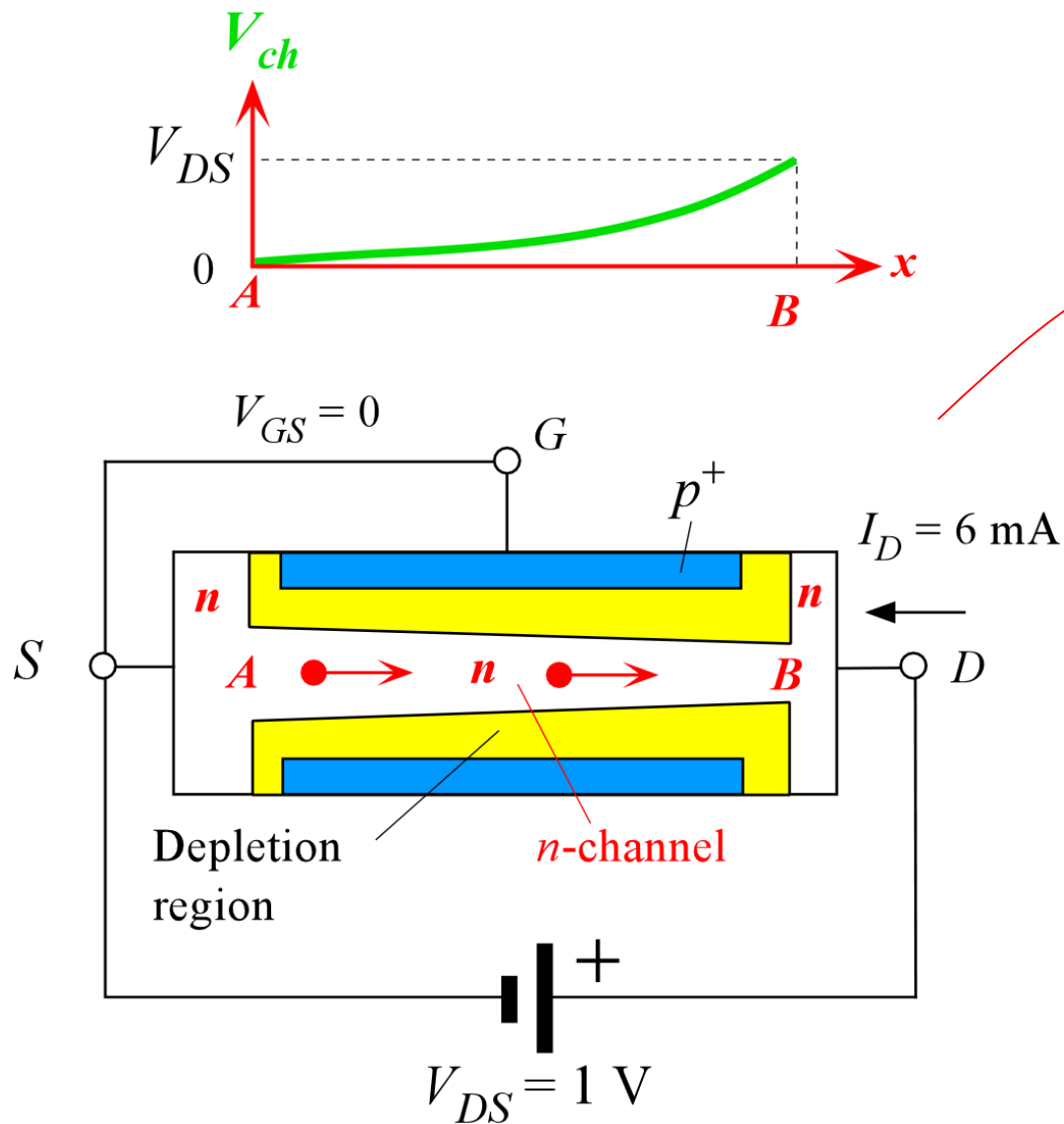


(a) The gate and source are shorted ( $V_{GS} = 0$ ) and  $V_{DS}$  is small,

(b)  $V_{DS}$  has increased to a value that allows the two depletion layers to just touch. This is called pinch-off voltage,  $V_{DS} = V_P (= 5 \text{ V})$ . Since gate to source is short,  $V_{GS} = 0$ ,  $V_{GD} = -V_{DS} = -V_P = -5 \text{ V}$ .

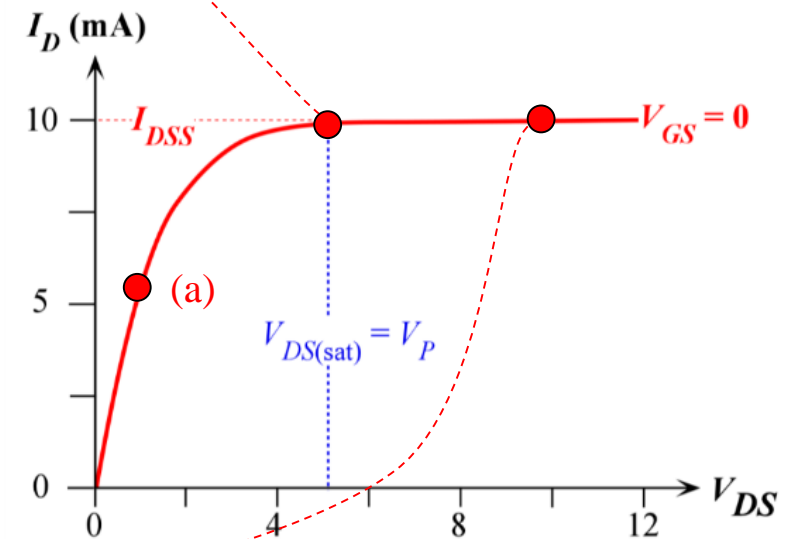
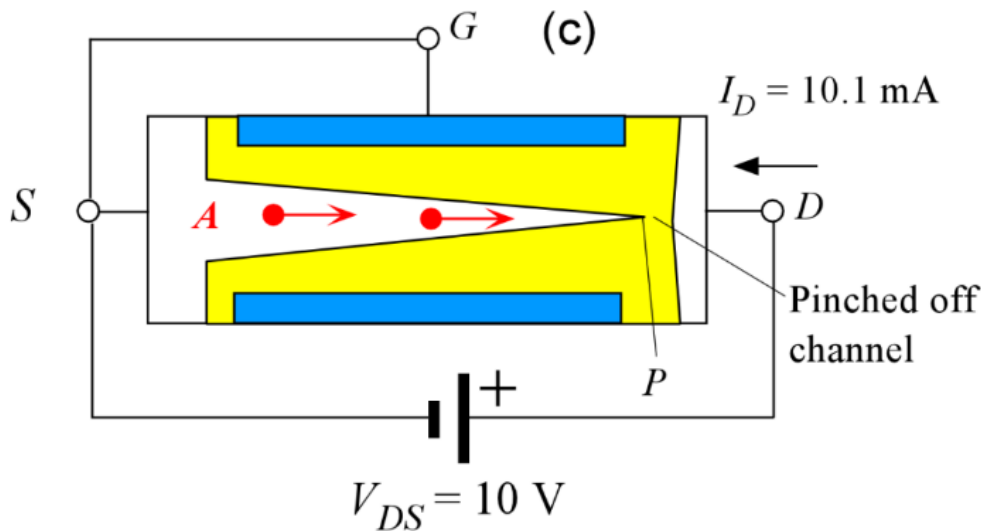
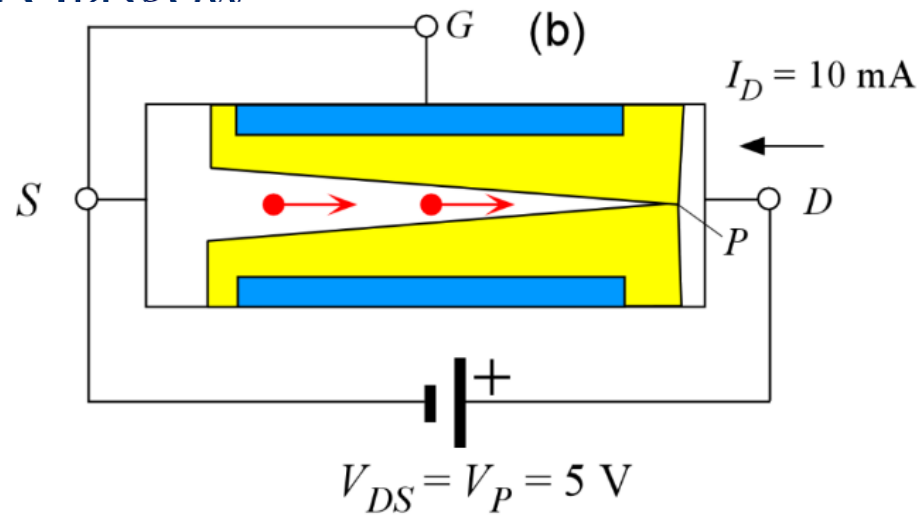
(c)  $V_{DS}$  is large ( $V_{DS} > V_P$ ) so that a short length of the channel is pinched off.

# JFET Principles



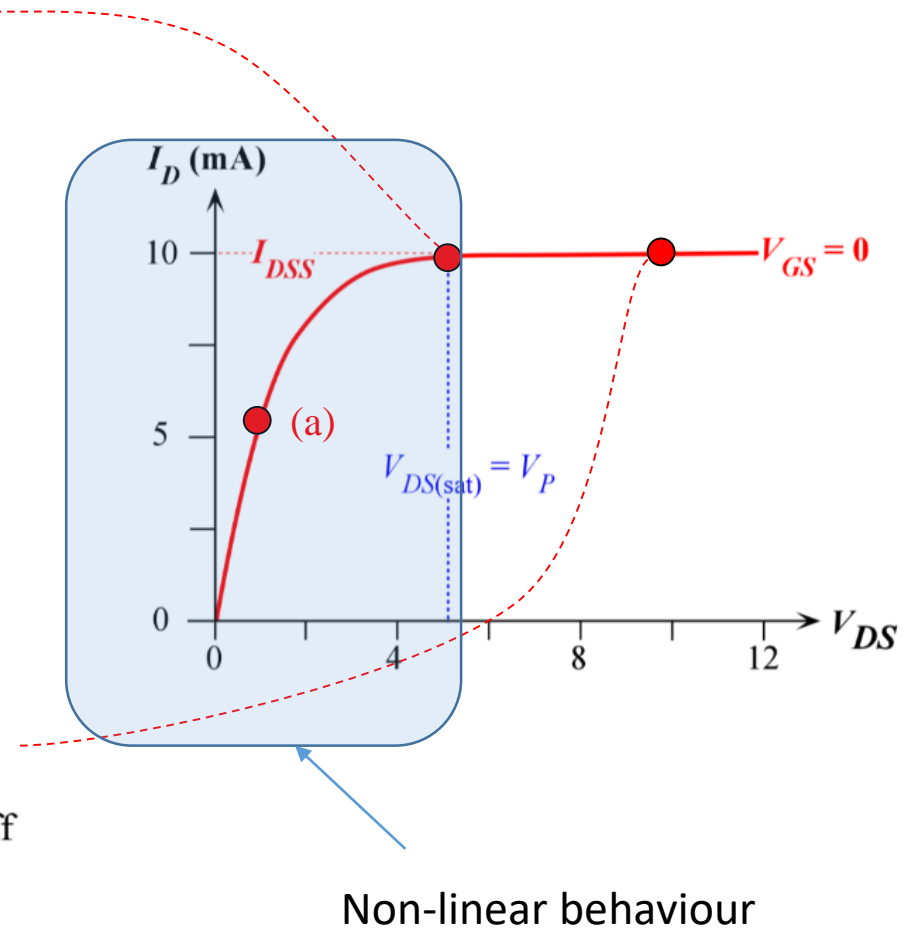
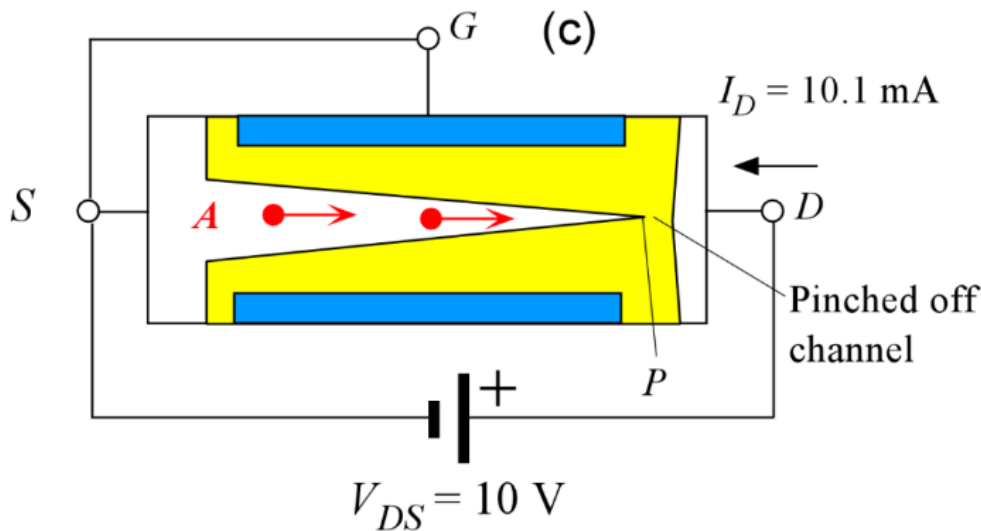
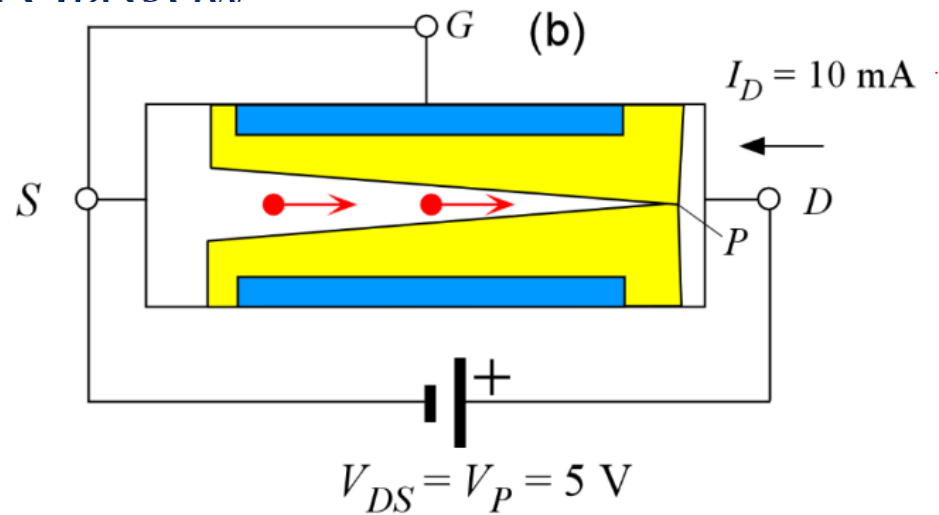
The gate and source are shorted ( $V_{GS} = 0$ ) and  $V_{DS}$  is small

# JFET Principles



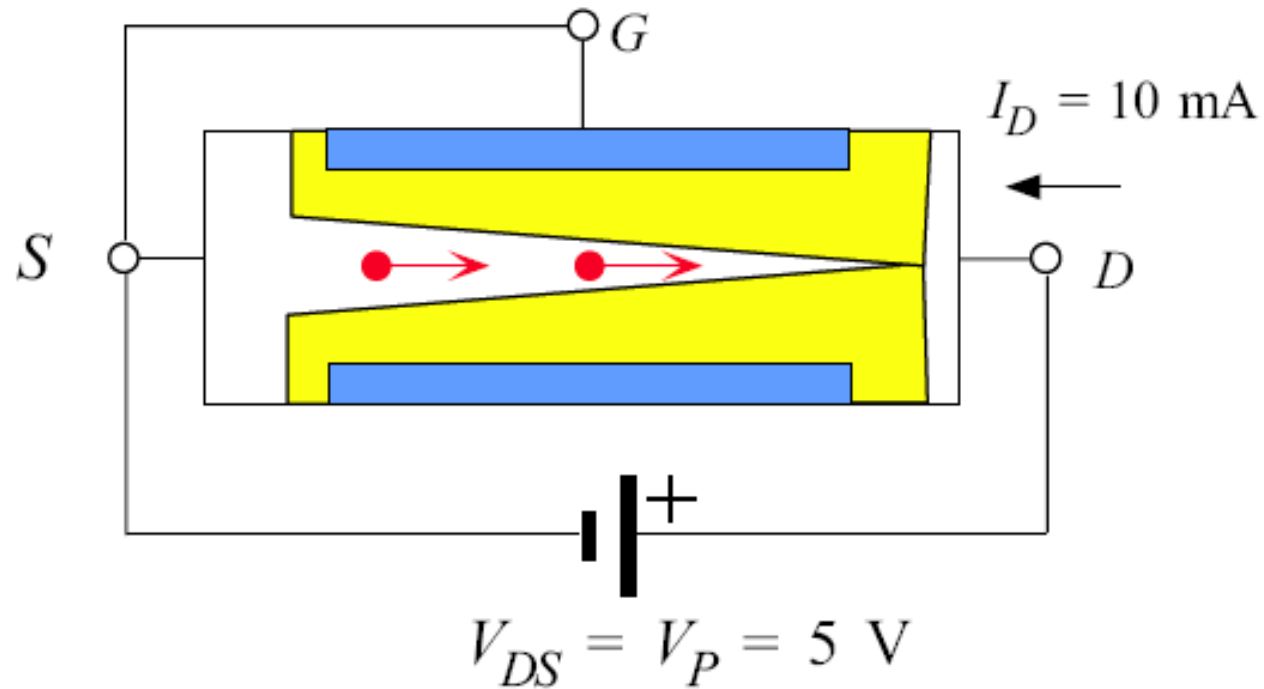
(b)  $V_{DS}$  has increased to a value that allows the two depletion layers to just touch, when  $V_{DS} = V_P (= 5 \text{ V})$  when the  $p^+n$  junction voltage at the drain end,  $V_{GD} = -V_{DS} = -V_P = -5 \text{ V}$ .  
 (c)  $V_{DS}$  is large ( $V_{DS} > V_P$ ) so that a short length of the channel is pinched off.

# JFET Principles



(b)  $V_{DS}$  has increased to a value that allows the two depletion layers to just touch, when  $V_{DS} = V_P (= 5 \text{ V})$  when the  $p^+n$  junction voltage at the drain end,  $V_{GD} = -V_{DS} = -V_P = -5 \text{ V}$ .  
 (c)  $V_{DS}$  is large ( $V_{DS} > V_P$ ) so that a short length of the channel is pinched off.

# JFET Principles: Channel Pinch-off

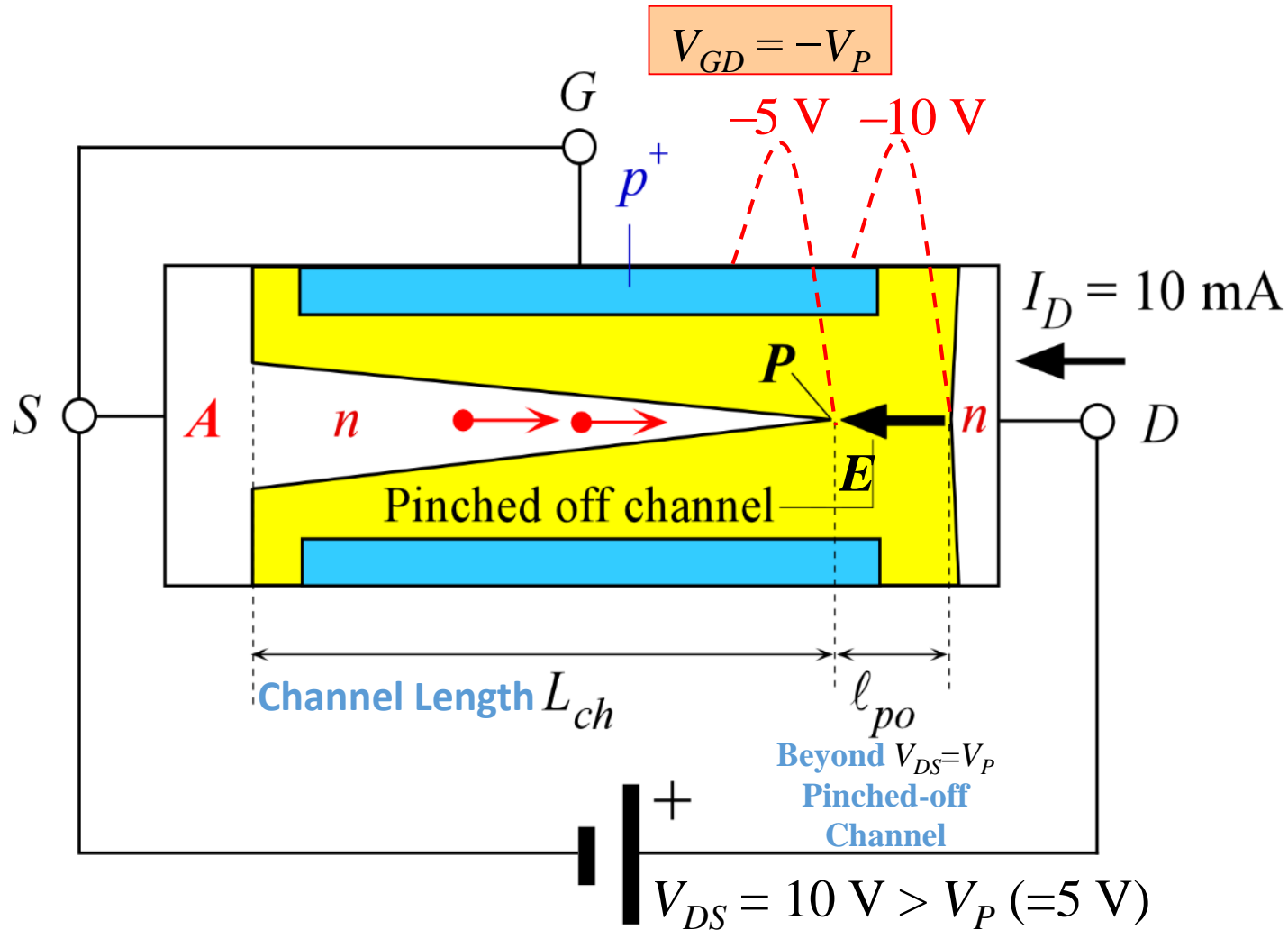


Pinch-off Condition with  $V_{GS} = 0$

$$V_{GD}(\text{pinch-off}) = -V_P$$

$V_{DS}$  has increased to a value that allows the two depletion layers to just touch, when  $V_{DS} = V_P (= 5 \text{ V})$  when the  $p^+n$  junction voltage at the drain end,  $V_{GD} = -V_{DS} = -V_P = -5 \text{ V}$ .

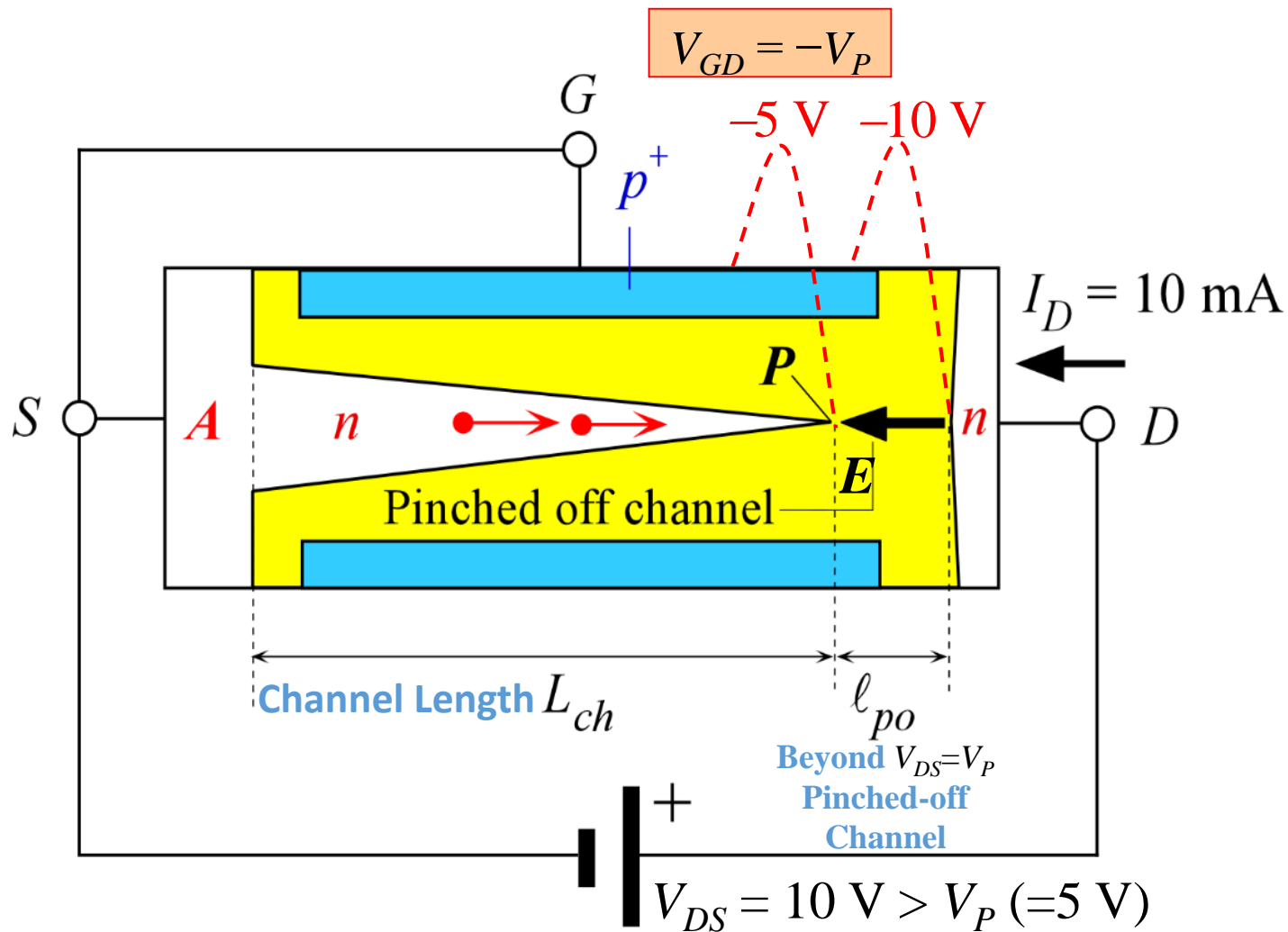




Electrons in the n-channel drift toward P. When they arrive at P, they are swept across the pinched-off channel by E-field. This process is similar to minority carriers in the base of a BJT.

Thus 
$$I_D = \frac{V_P}{R_{AP}} \quad (V_{DS} > V_P)$$



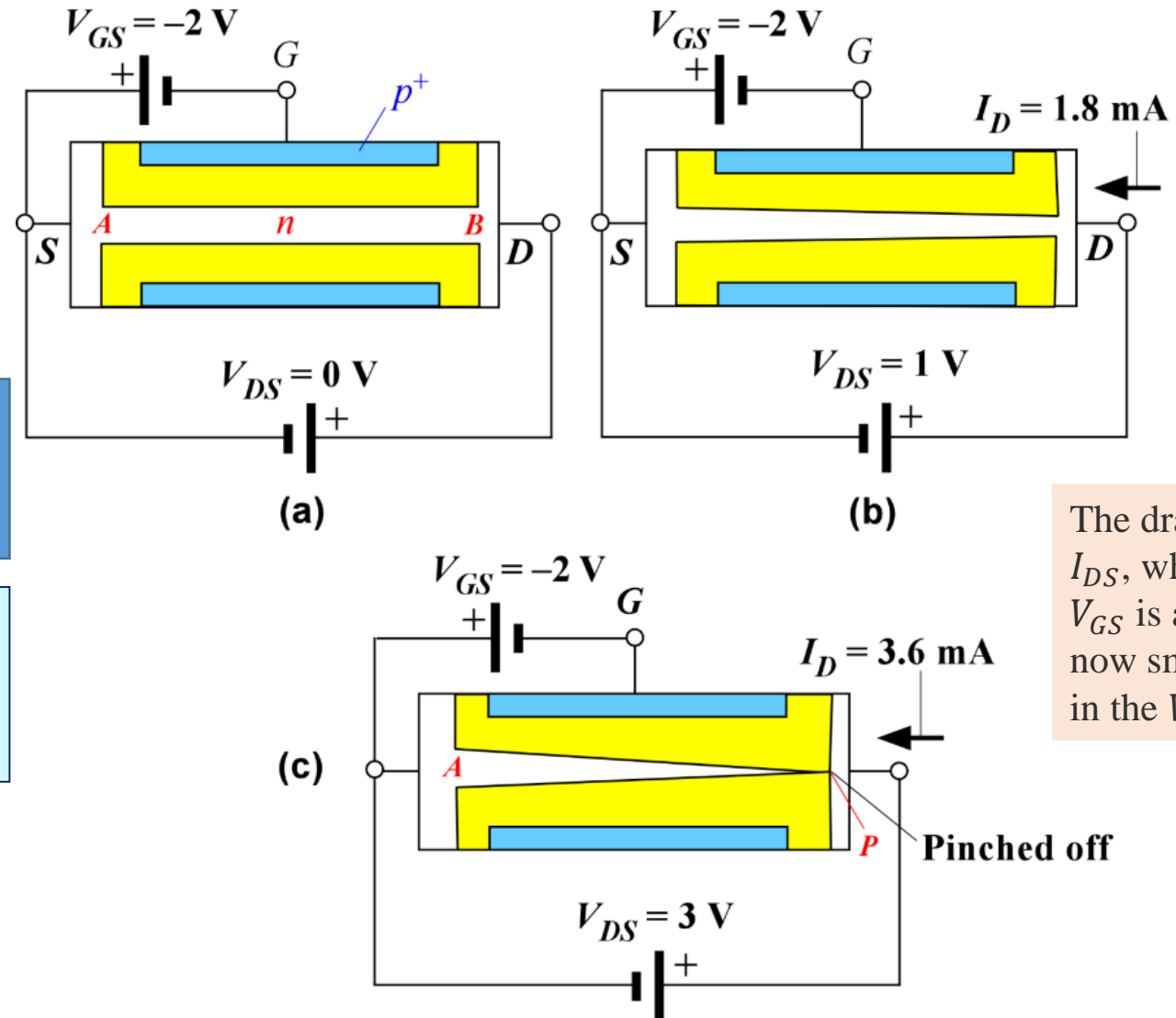


As  $V_{ds}$  increases, most of the additional voltage simply drops across  $l_{po}$  as this region is depleted of carriers and hence highly resistive.

- We first considered the behavior of the JFET with the **gate** and **source** shorted ( $V_{GS} = 0$ ). The resistance between S and D is the resistance of the conducting n-channel between A and B,  $R_{AB}$ .
- When a positive voltage is applied to D with respect to S ( $V_{DS} > 0$ ), then a current flows from D to S which is called the drain current  $I_D$ .
- There is a voltage drop along the channel, between A and B. The voltage in the n-channel is zero at A and  $V_{DS}$  at B.
- As the voltage along the n-channel is positive, the pn junctions between the gates and the n-channel become progressively more reverse-biased from A to B. Consequently the depletion layers extend more into the channel and thereby decrease the thickness of the conducting channel from A to B.
- Increasing  $V_{DS}$  increases the widths of the depletion layers, which penetrate more into the channel and hence result in more channel narrowing toward the drain.
- The resistance of the n-channel  $R_{AB}$  therefore increases with  $V_{DS}$ . The drain current therefore does not increase linearly with  $V_{DS}$ .

$$I_D = \frac{V_{DS}}{R_{AB}}$$

# JFET Principles: Effect of $V_{GS}$



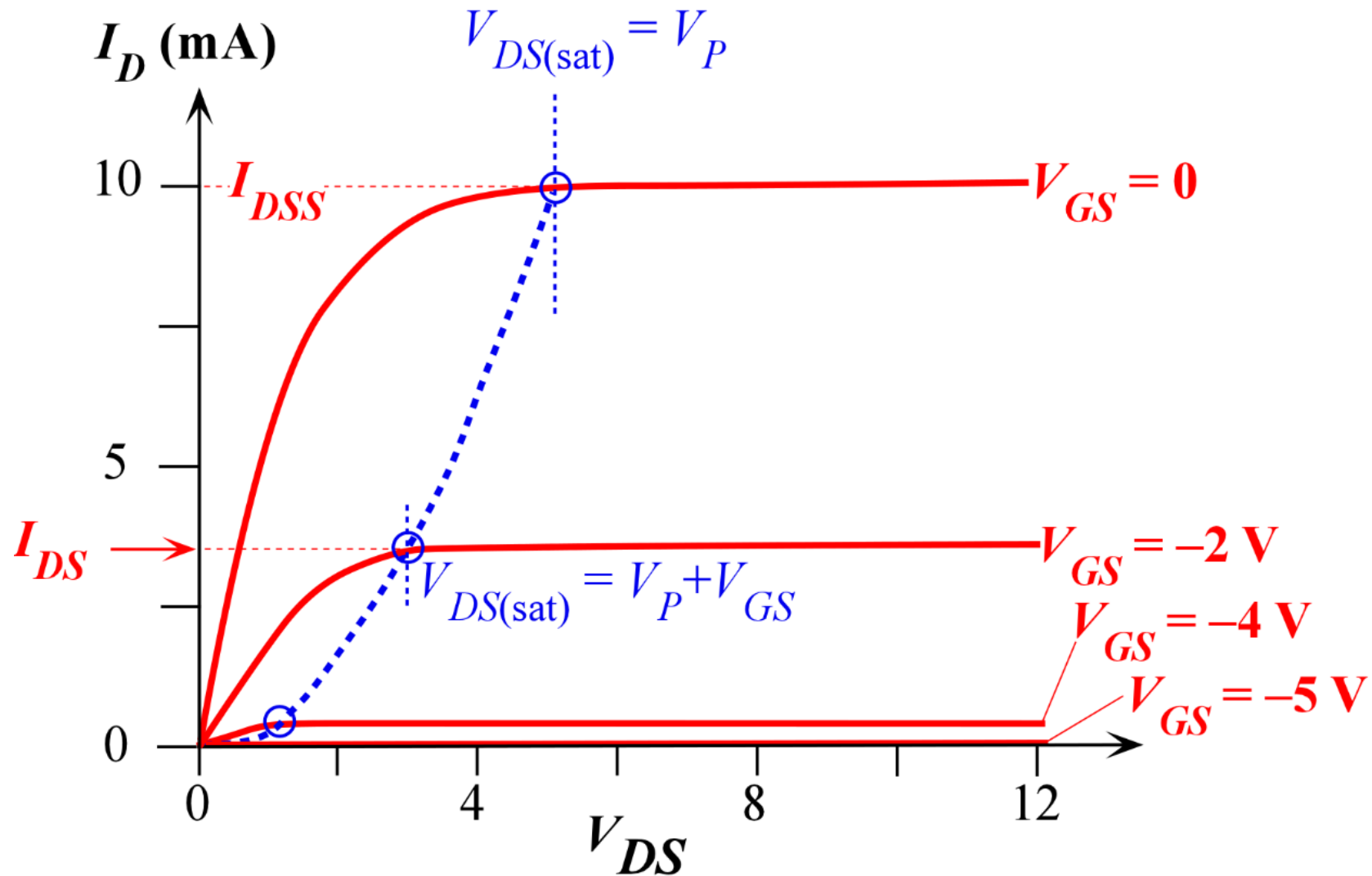
$$V_{DS(sat)} = V_{GS} - V_{GD} \\ = V_{GS} + V_p$$

Thus, a smaller  $V_{DS}$  is needed to pinch off channel ( $V_{DS}=3\text{V}$ )

The drain current,  $I_{DS}$ , when a small  $V_{GS}$  is applied is now smaller than in the  $V_{GS} = 0$  case.

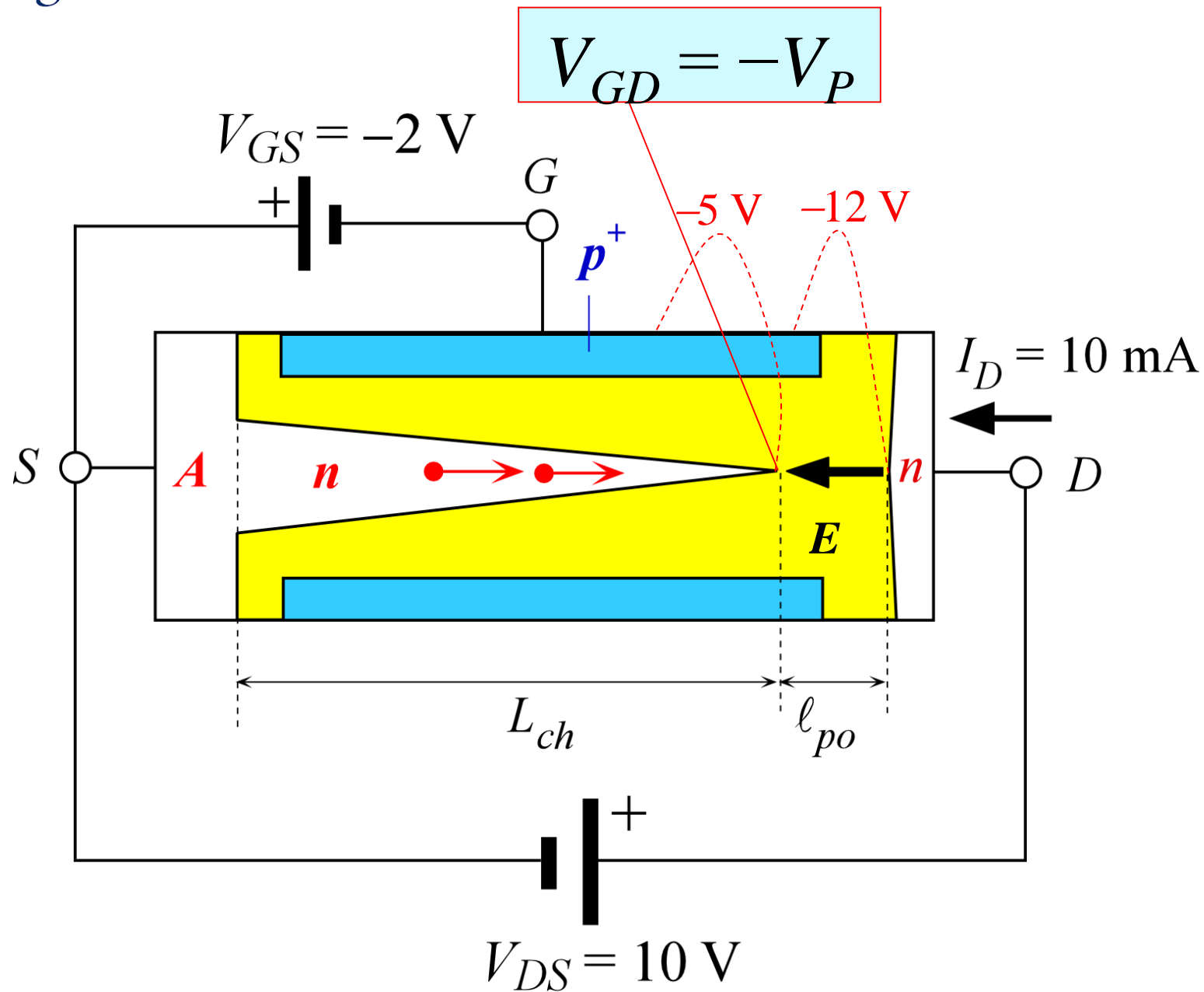
(a) The JFET with a negative  $V_{GS}$  bias has a **narrower**  $n$ -channel at the start. (b) Compared to the  $V_{GS} = 0$  case, the same  $V_{DS}$  gives less  $I_D$  as the channel is narrower. (c) A smaller voltage is required for pinch-off. The channel is pinched off at  $V_{DS} = 3\text{ V}$  sooner than the  $V_{GS} = 0$  case where it was  $V_{DS} = 5\text{ V}$ .

# JFET Characteristics

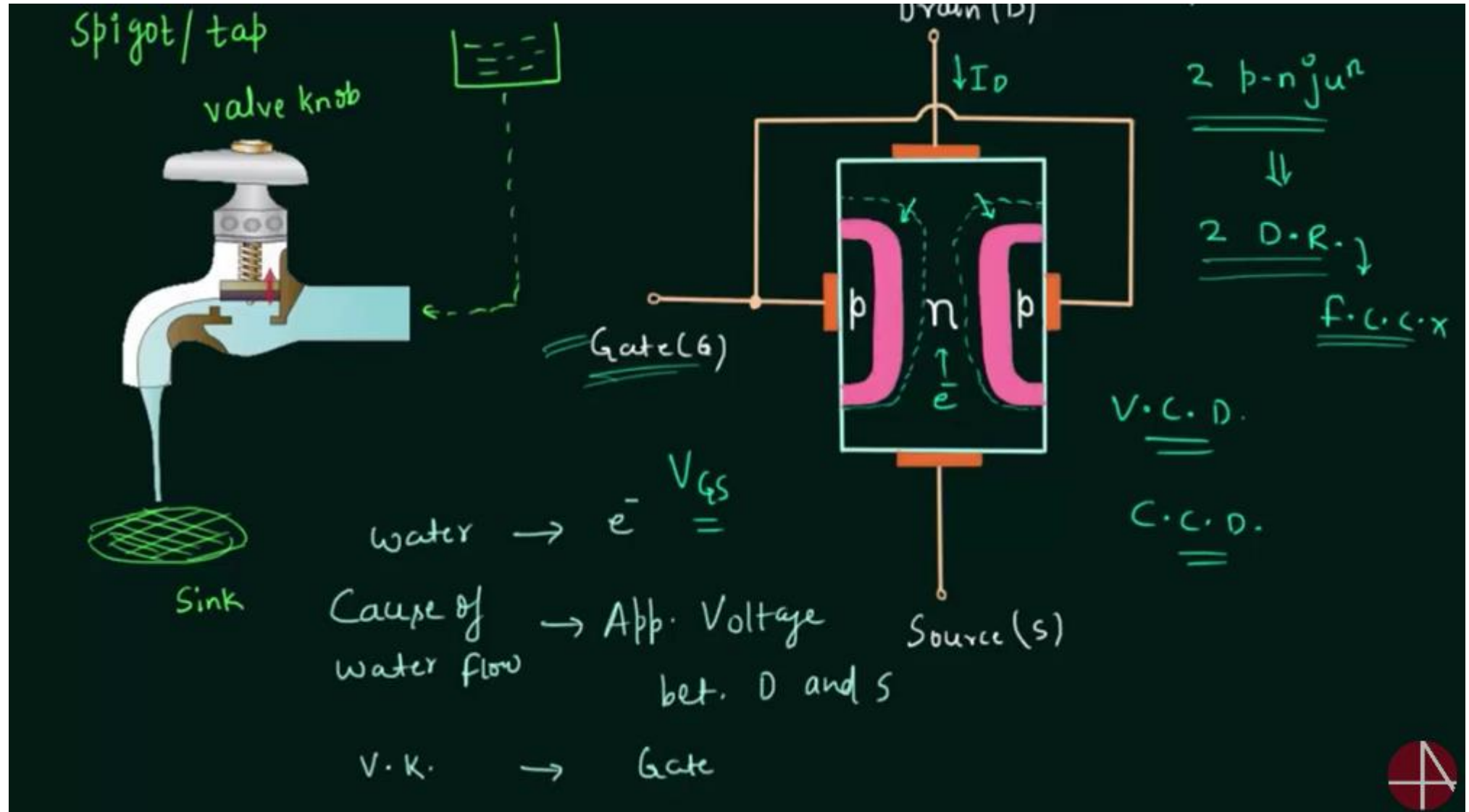


Typical  $I_D$  vs.  $V_{DS}$  characteristics of a JFET for various fixed gate voltages  $V_{GS}$ .

# JFET Principles: Beyond Channel Pinch-off



# Junction Field Effect Transistor (JFET) Analogy



From [https://www.youtube.com/watch?v=\\_DZ7baOhNFQ](https://www.youtube.com/watch?v=_DZ7baOhNFQ)

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# Junction Field Effect Transistor (JFET)

## Pinch-off condition

$$V_{DS(sat)} = V_P + V_{GS}$$

$$I_D \approx I_{DS} \approx \frac{V_{DS(sat)}}{R_{AP}(V_{GS})} = \frac{V_P + V_{GS}}{R_{AP}(V_{GS})}$$

where  $V_{GS}$  is a negative voltage (reducing  $V_P$ ) and  $R_{AP}$  is the effective resistance of the n-channel from A to P (slide 6c).

Beyond pinch-off when  $V_{DS} > V_{DS(sat)}$ , the point  $P$  where the channel is just pinched still remains at potential  $V_{DS(sat)}$ , given by the above equation.

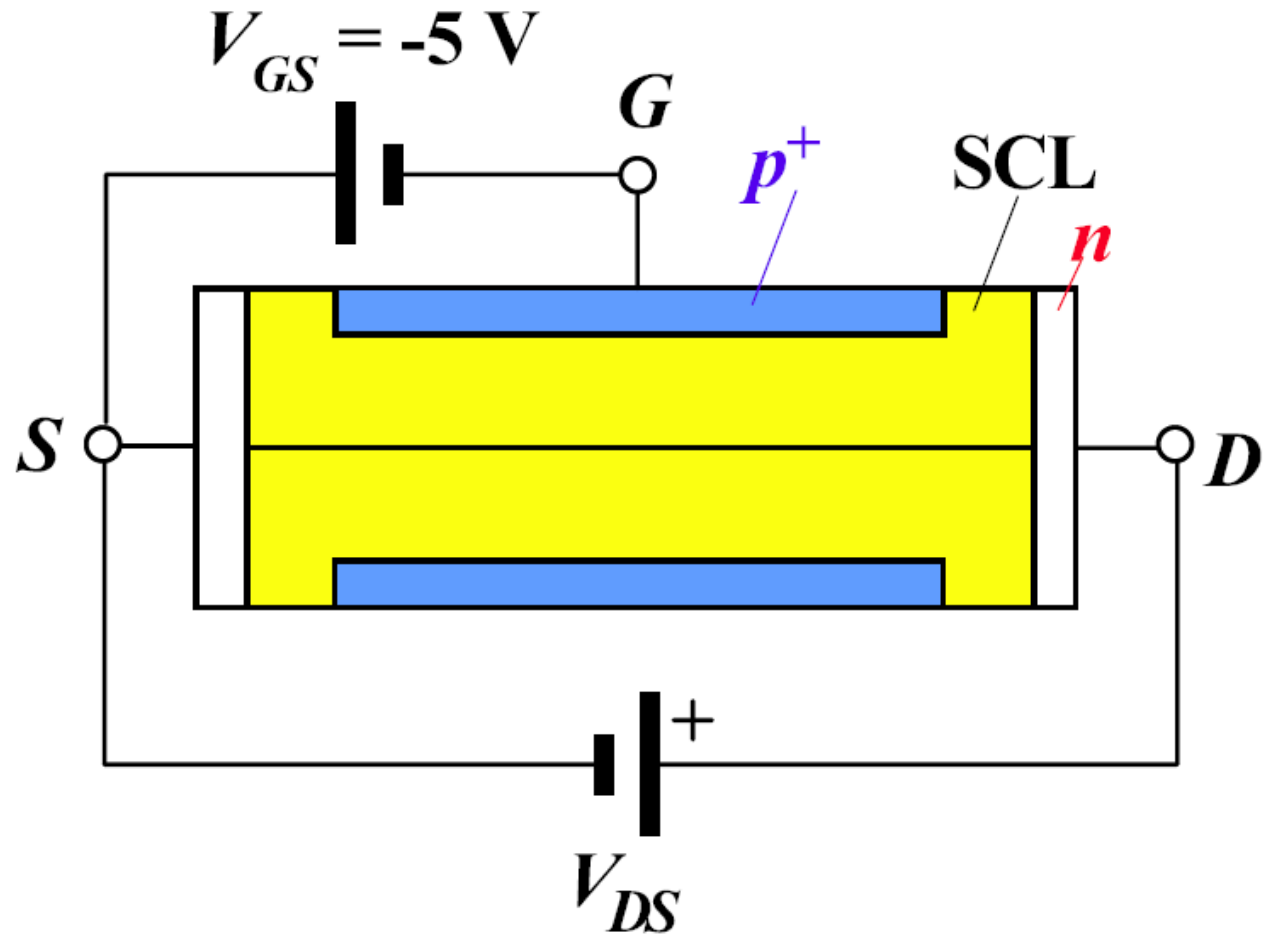
# Junction Field Effect Transistor (JFET)

- The resistance increases with more negative gate voltage as this increases the reverse bias across the pn junction, which leads to the narrowing of the channel.
  - e.g. when  $V_{GS} = -4$  V, the channel thickness at A becomes narrower than in the case with  $V_{GS} = -2$  V, thereby increasing the resistance ( $R_{AP}$ ) of the conducting channel and therefore decreasing  $I_{DS}$ .
- Further, there is a reduction in the drain current by virtue of  $V_{DS(sat)}$  decreasing with negative  $V_{GS}$ . Figure in slide 12 shows the effect of the gate voltage on the  $I_D$  versus  $V_{DS}$  behavior.

These two effects (i.e. from  $V_{DS(sat)}$  and that from  $R_{AP}$ ) lead to  $I_{DS}$  almost decreasing parabolically with  $-V_{GS}$ .

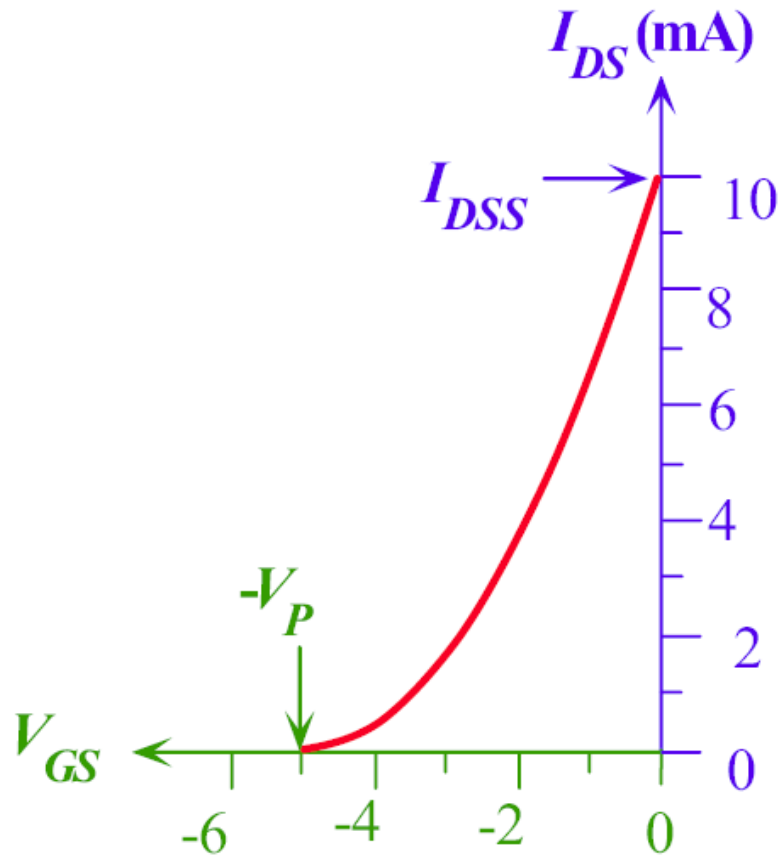
# JFET with Turn-off $V_{GS}$

When the gate voltage is such that  $V_{GS} = -V_p$  ( $= -5 \text{ V}$ ) with the source and drain shorted ( $V_{DS} = 0$ ), then the two depletion layers touch over the entire channel length and the whole channel is closed. **The channel is said to be off.** The only drain current that flows when a  $V_{DS}$  is applied is due to the thermally generated carriers in the depletion layers. This current is very small.

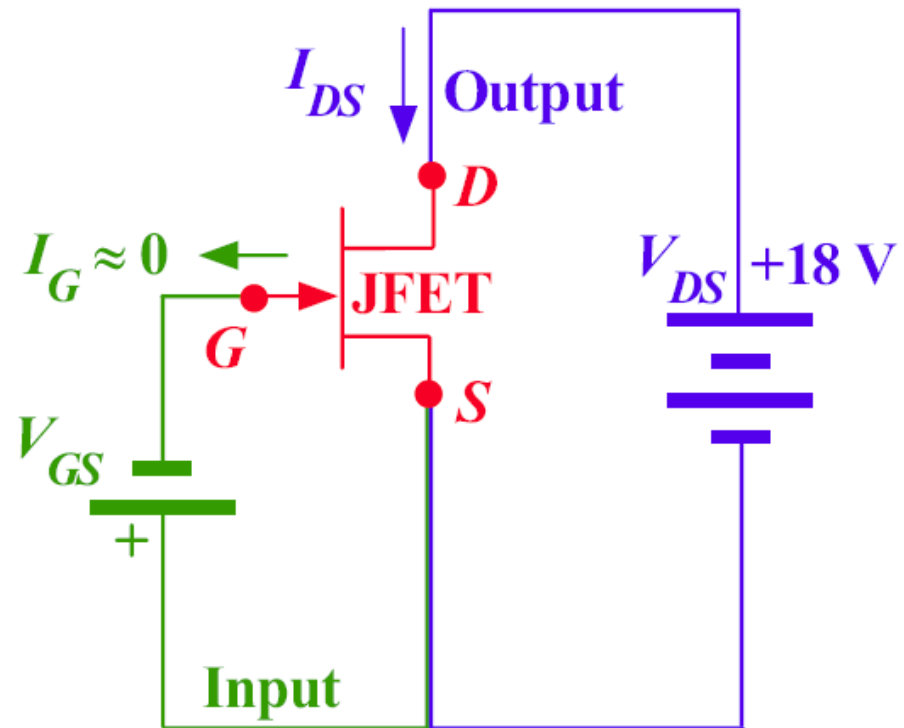


When  $V_{GS} = -5 \text{ V}$  the depletion layers close the whole channel from the start, at  $V_{DS} = 0$ . As  $V_{DS}$  is increased there is a very small drain current which is the small reverse leakage current due to thermal generation of carriers in the depletion layers.

# JFET Transfer Characteristics



(a)



(b)

(a) Typical  $I_{DS}$  versus  $V_{GS}$  characteristics of a JFET. (b) The dc circuit where  $V_{GS}$  in the gate–source circuit (input) controls the drain current  $I_{DS}$  in the drain–source (output) circuit in which  $V_{DS}$  is kept constant and large ( $V_{DS} > V_P$ ).

# Junction Field Effect Transistor (JFET)

## Beyond pinch-off

A simple way to express the relationship between  $I_{DS}$  and  $V_{GS}$  is:

$$I_{DS} = I_{DSS} \left[ 1 - \left( \frac{V_{GS}}{V_{GS(\text{off})}} \right) \right]^2$$

where,

$I_{DSS}$  is the drain current when  $V_{GS} = 0$

$V_{GS(\text{off})} = -V_p$ ; the gate-source voltage that just pinches off the channel

# JFET SUMMARY

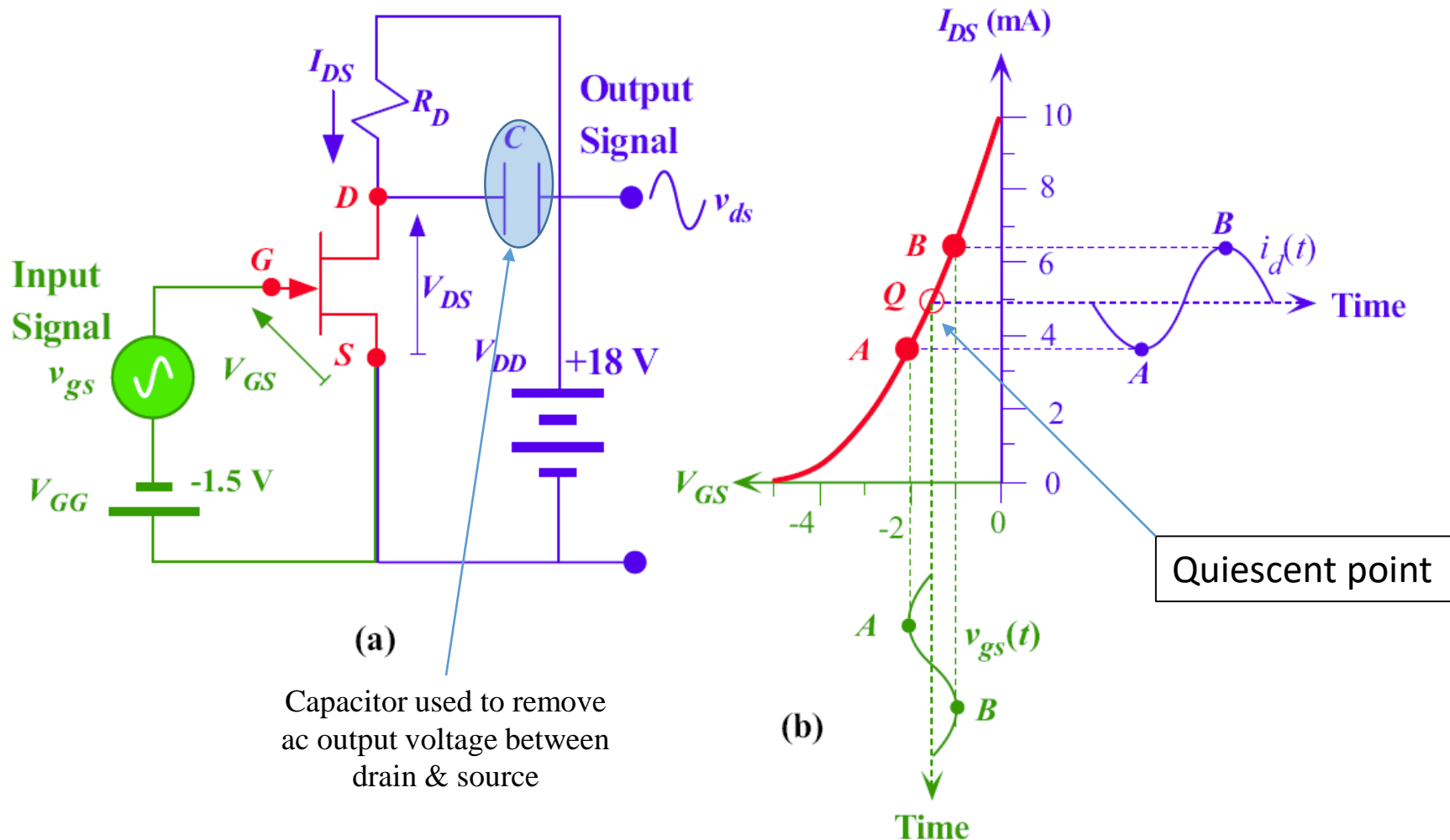
Two important facts about the JFET:

- Modulating the electric field in the reverse-biased depletion layers (**by changing  $V_{gs}$** ) varies the depletion layer penetration into the channel and hence the **resistance** of the channel. **The transistor action hence can be thought of as being based on a field effect.** Since there is a pn junction between the gate and the channel, the name has become **JFET**. This junction in reverse bias provides the isolation between the gate and channel.
- Secondly, the region beyond pinch-off is commonly called the **current saturation region**, as well as **constant current region** and **pentode region**. The term **saturation** should not be confused with similar terms used for **saturation effects in bipolar transistors**. A saturated BJT **cannot** be used as an amplifier, but ***JFETs are invariably used as amplifiers in the saturated current region.***

# JFET Commons Source Amplifier

- The transistor action in the JFET is the control of  $I_{DS}$  by  $V_{GS}$ . The input circuit is the gate-source circuit containing  $V_{GS}$  and the output circuit is the drain-source circuit in which the drain current  $I_{DS}$  flows.
- The JFET is almost never used with the pn junction between the gate and channel forward-biased ( $V_{gs} > 0$ ).
- With  $V_{GS}$  limited to negative voltages, the maximum current in the output circuit can only be  $I_{DSS}$ . The maximum input voltage  $V_{GS}$  should therefore give an  $I_{DS}$  less than  $I_{DSS}$ .

# JFET Commons Source Amplifier

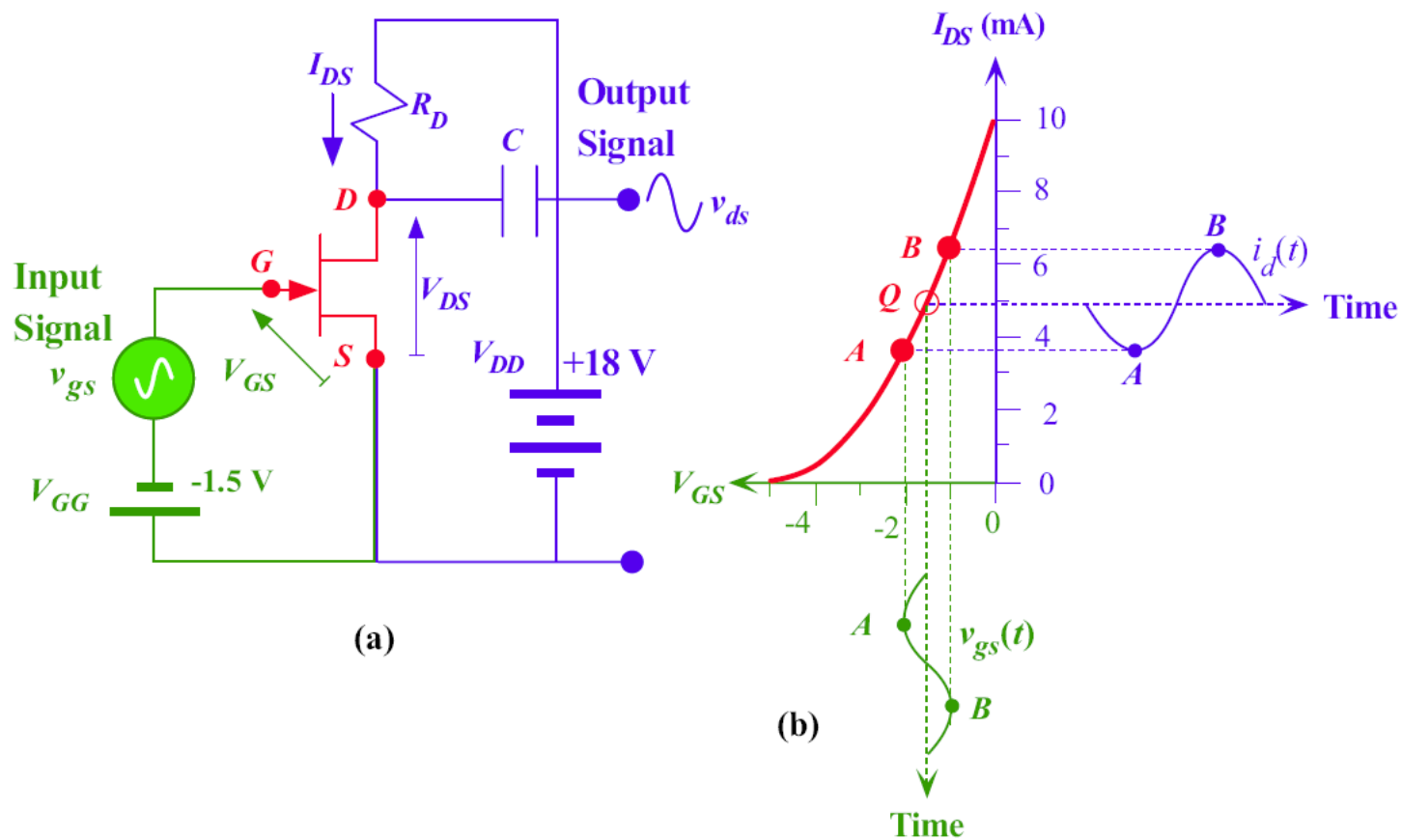


Capacitor used to remove  
ac output voltage between  
drain & source

Quiescent point

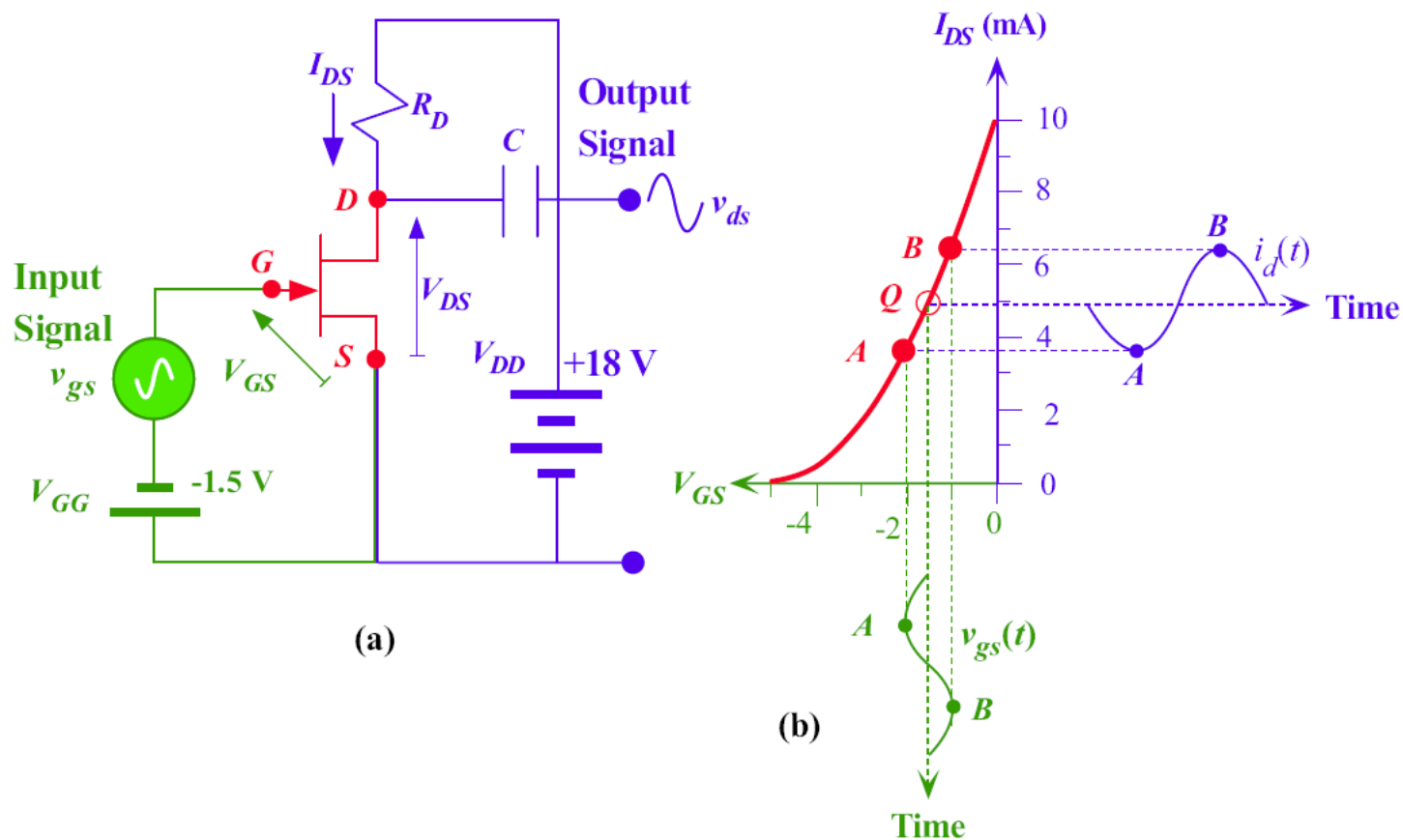
- (a) Common source (CS) ac amplifier using a JFET. **Both input and output circuits are connected to the same source.**
- (b) Explanation of how  $I_D$  is modulated by the signal  $v_{gs}$  in series with the dc bias voltage  $V_{GG}$ , supposing that  $v_{gs}$  varies sinusoidally between  $-0.5\text{ V}$  and  $+0.5\text{ V}$ .





$v_{gs}$ (V)	$V_{GS}$ (V)	$I_{DS}$ (mA)	$i_d = \delta I_{DS}$ (mA)	$V_{DS} = V_{DD} - I_{DS}R_D$	$v_{ds}$ (V)	Voltage Gain	Comment
0	-1.5	4.9	0	8.2	0		dc conditions, point Q
-0.5	-2.0	3.6	-1.3	10.8	+2.6	-5.2	Point A
+0.5	-1.0	6.4	+1.5	5.2	-3.0	-6	Point B

NOTE:  $V_{DD} = 18\text{ V}$  and  $R_D = 2000\ \Omega$ .

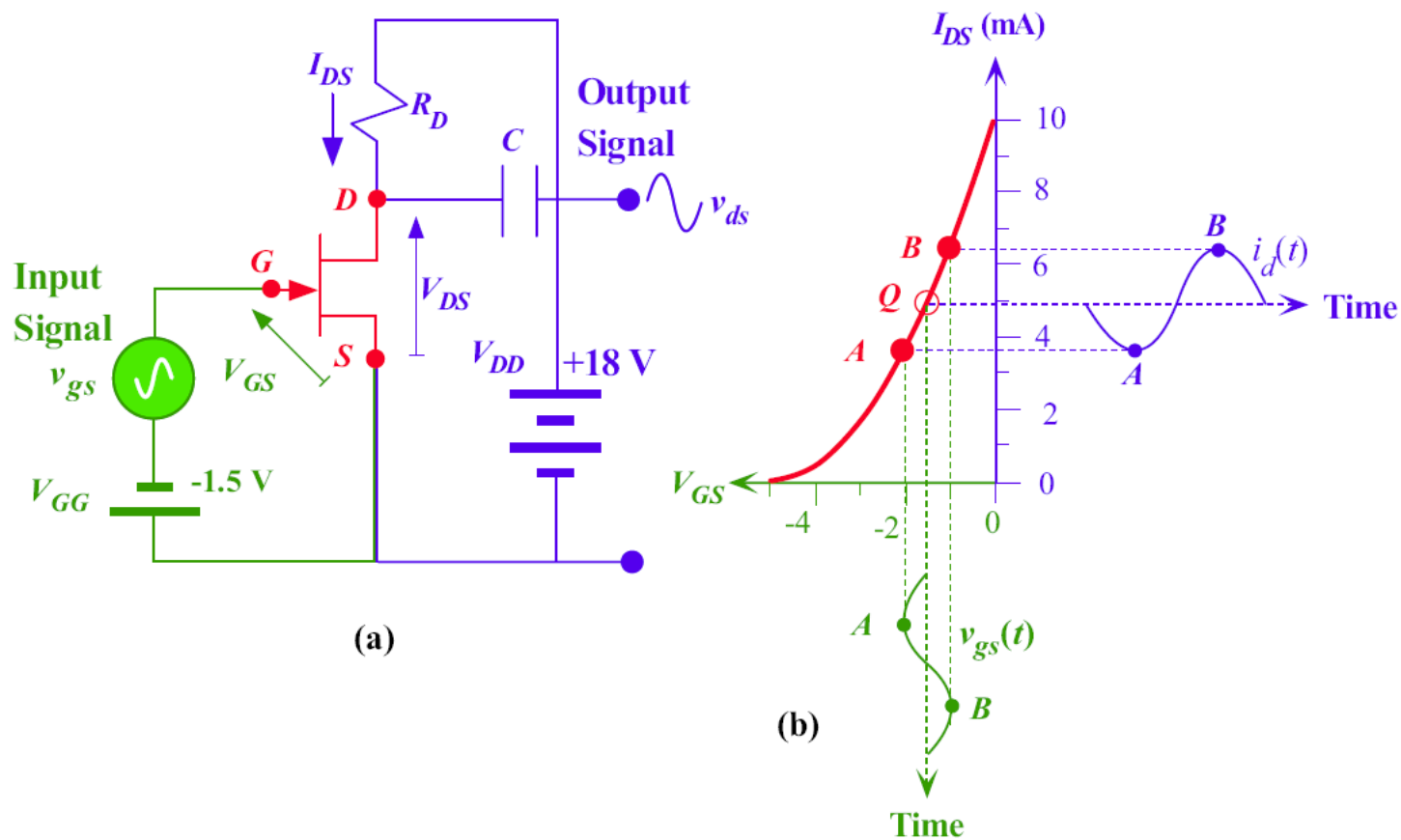


$v_{gs}$ (V)	$V_{GS}$ (V)	$I_{DS}$ (mA)	$i_d$ (mA)	$V_{DS} = V_{DD} - I_{DS}R_D$	$v_{ds}$ (V)	Voltage Gain	Comment
0	-1.5	4.9	0	8.2	0		dc conditions, point Q
-0.5	-2.0	3.6	-1.3	10.8	+2.6	-5.2	Point A
+0.5	-1.0	6.4	+1.5	5.2	-3.0	-6	Point B

Asymmetric due to " $I_{DS} - V_{GS}$ " relationship

NOTE:  $V_{DD} = 18\text{ V}$  and  $R_D = 2000\ \Omega$ .

$$I_{DS} = I_{DSS} \left[ 1 - \left( \frac{V_{GS}}{V_{GS(\text{off})}} \right) \right]^2$$

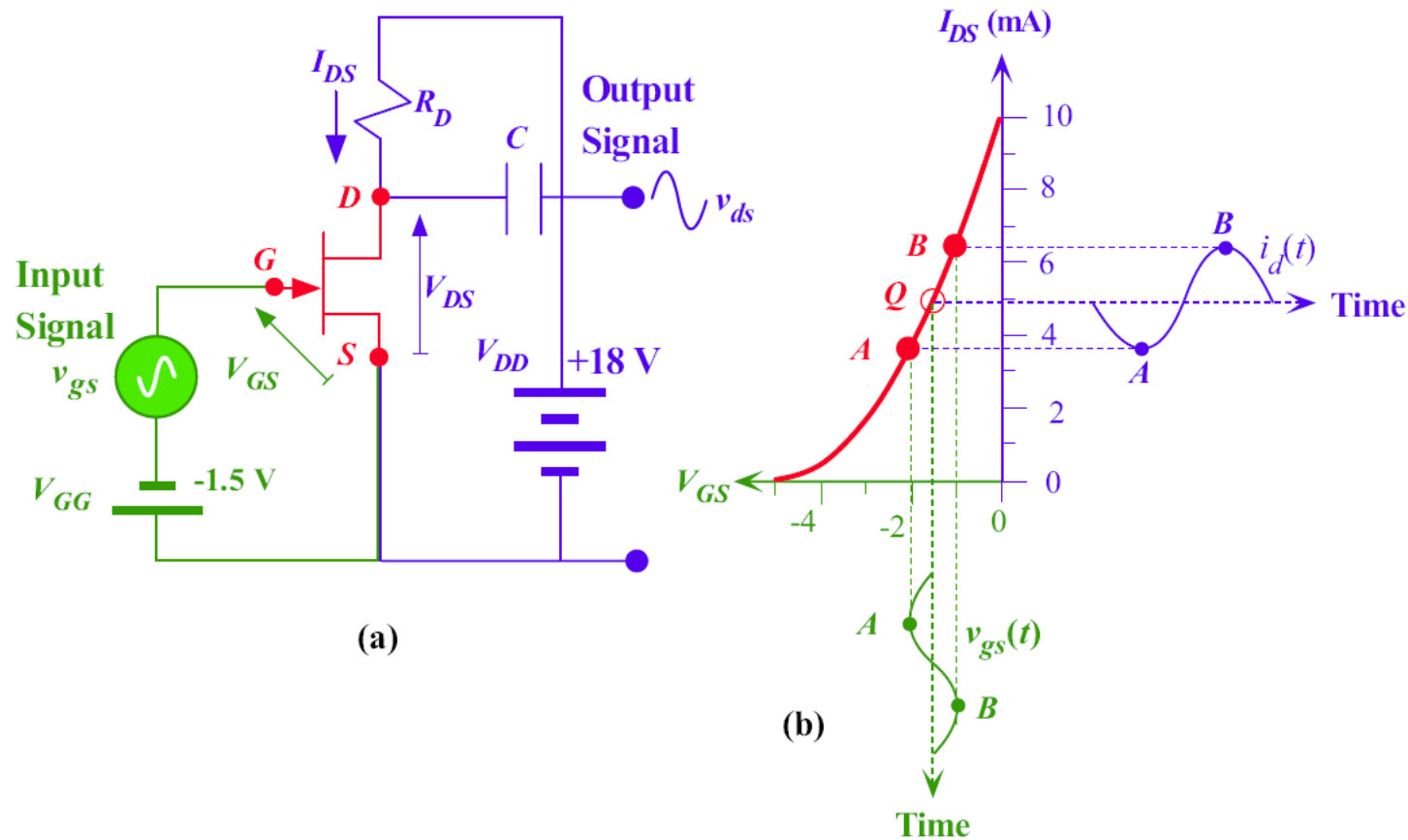


$v_{gs}$ (V)	$V_{GS}$ (V)	$I_{DS}$ (mA)	$i_d$ (mA)	$V_{DS} = V_{DD} - I_{DS}R_D$	$v_{ds}$ (V)	Voltage Gain	Comment
0	-1.5	4.9	0	8.2	0		dc conditions, point Q
-0.5	-2.0	3.6	-1.3	10.8	+2.6	-5.2	Point A
+0.5	-1.0	6.4	+1.5	5.2	-3.0	-6	Point B

Asymmetric due to " $I_{DS} - V_{GS}$ " relationship

$$v_{ds} = -R_D i_d$$

$$I_{DS} = I_{DSS} \left[ 1 - \left( \frac{V_{GS}}{V_{GS(off)}} \right) \right]^2$$



Thus the output,  $v_{ds}$ , changes from  $-3.0\text{ V}$  to  $2.6\text{ V}$ . The peak-to-peak voltage amplification is

$$A_{V(\text{pk-pk})} = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{v_{ds(\text{pk-pk})}}{v_{gs(\text{pk-pk})}} = \frac{-3\text{ V} - (2.6\text{ V})}{0.5\text{ V} - (-0.5\text{ V})} = -5.6$$

The negative sign represents the fact that the output and input voltages are out of phase by  $180^\circ$

# JFET Amplifier

- The amplification can be increased by **increasing  $R_D$** , but we must maintain  $V_{DS}$  at all times above  $V_{DS(sat)}$  (i.e. beyond pinch-off) to ensure that the drain current  $I_{DS}$  in the output circuit is only controlled by  $V_{GS}$  in the input circuit.
- When the signals are small about dc values, we can use differentials to represent small signals. For example,  $v_{gs} = \delta V_{GS}$ ,  $i_d = \delta I_{DS}$ ,  $v_{ds} = \delta V_{DS}$  and so on. The variation  $\delta I_{DS}$  due to  $\delta V_{GS}$  about the dc value may be used to define a **mutual transconductance  $g_m$  for the JFET**.

# JFET Common Source Amplifier

## Definition of the JFET transconductance (small signal)

$$g_m = \frac{dI_{DS}}{dV_{GS}} \approx \frac{\delta I_{DS}}{\delta V_{GS}} = \frac{i_d}{v_{gs}}$$

## JFET transconductance (small signal)

$$g_m = \frac{dI_{DS}}{dV_{GS}} = -\frac{2I_{DSS}}{V_{GS(\text{off})}} \left[ 1 - \left( \frac{V_{GS}}{V_{GS(\text{off})}} \right) \right] = \frac{-2[I_{DSS} I_{DS}]^{1/2}}{V_{GS(\text{off})}}$$

# JFET Common Source Amplifier

## Small-signal voltage gain

$$A_V = \frac{v_{ds}}{v_{gs}} = \frac{-R_D i_d}{v_{gs}}$$

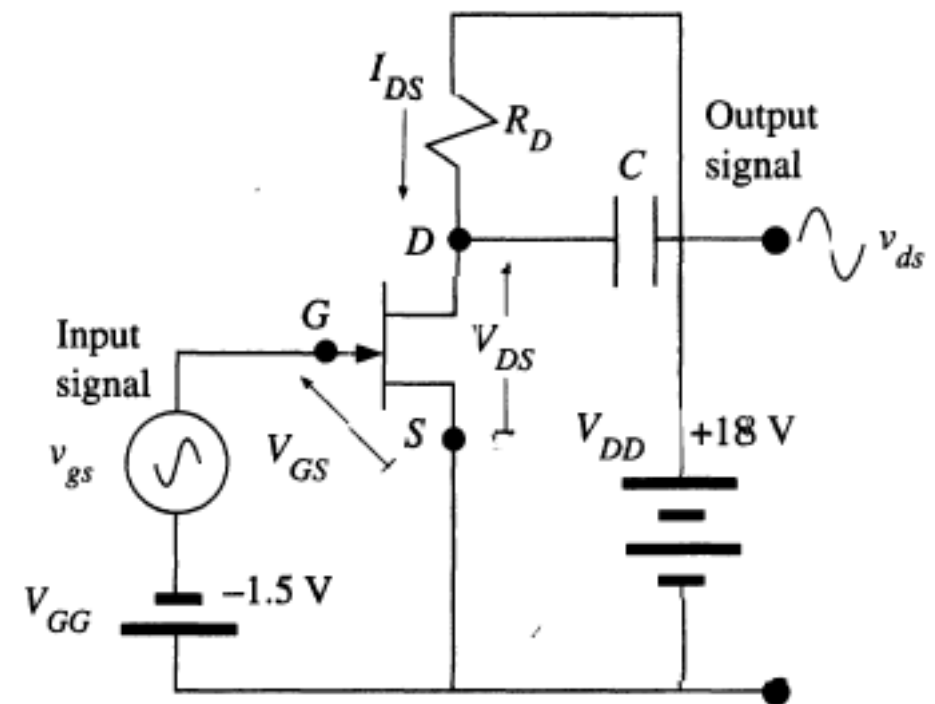
$$\therefore A_V = \frac{-R_D (g_m v_{gs})}{v_{gs}} = -g_m R_D$$

$$\therefore A_V = -g_m R_D$$

The negative sign indicates that the output and input voltages are out of phase by 180°

# JFET – Example 1

**THE JFET AMPLIFIER** Consider the  $n$ -channel JFET common source amplifier shown in Figure 6.34a. The JFET has an  $I_{DSS}$  of 10 mA and a pinch-off voltage  $V_P$  of 5 V as in Figure 6.34b. Suppose that the gate dc bias voltage supply  $V_{GG} = -1.5$  V, the drain circuit supply  $V_{DD} = 18$  V, and  $R_D = 2000 \Omega$ . What is the voltage amplification for small signals? How does this compare with the peak-to-peak amplification of  $-5.6$  found for an input signal that had a peak-to-peak value of 1 V?





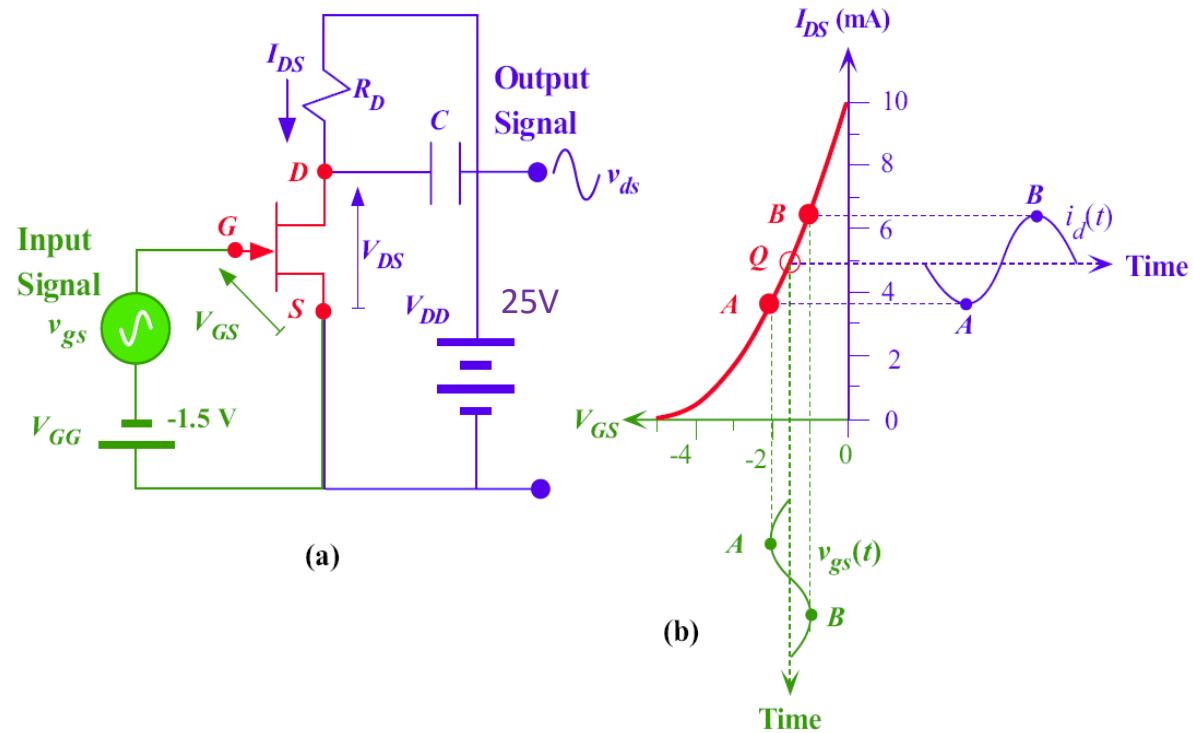




# JFET – Example 2

**The JFET amplifier** Consider an  $n$ -channel JFET that has a pinch-off voltage ( $V_P$ ) of 5 V and  $I_{DSS} = 10$  mA. It is used in a common source configuration as shown, in which the gate to source bias voltage ( $V_{GS}$ ) is  $-1.5$  V. Suppose that  $V_{DD} = 25$  V.

- If a small signal voltage gain of  $-10$  is needed, what should be the drain resistance ( $R_D$ )? What is  $V_{DS}$ ?
- If an ac signal of 1 V peak-to-peak is applied to the gate in series with the dc bias voltage, what will be the ac output voltage peak-to peak? What is the voltage gain for positive and negative input signals? What is your conclusion?



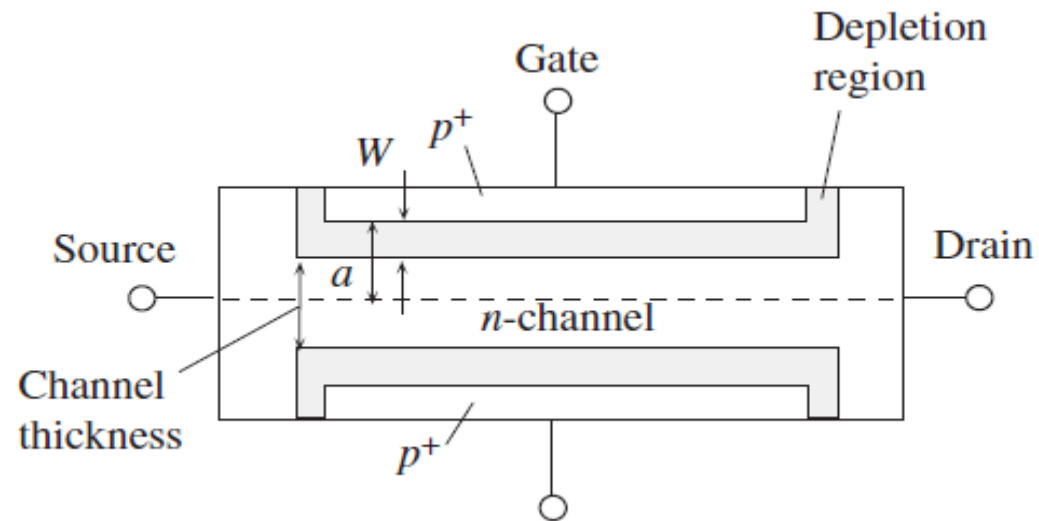




## JFET – Example 3

**The JFET Pinch-off Voltage** Consider the symmetric  $n$ -channel JFET shown below. The width of each depletion region extending into the  $n$ -channel is  $W$ . The thickness, or depth, of the channel, defined between the two metallurgical junctions, is  $2a$ . Assuming an abrupt  $pn$  junction and  $V_{DS} = 0$ , show that when the gate to source voltage is  $-V_p$  the channel is pinched off where

$$V_p = \frac{a^2 e N_d}{2\epsilon} - V_o$$



where  $V_o$  is the built-in potential between  $p^+n$  junction and  $N_d$  is the donor concentration of the channel.

Calculate the pinch-off voltage of a JFET that has an acceptor concentration of  $10^{19} \text{ cm}^{-3}$  in the  $p^+$  gate, a channel donor doping of  $10^{16} \text{ cm}^{-3}$ , and a channel thickness (depth),  $2a$ , of  $2\mu\text{m}$ .

### Solution

Assume we have a Si JFET. The depletion region of a  $p^+n$  junction extends essentially into  $n$ -side.  $W$  depends on the reverse bias  $V_r = -V_{GS}$  between the  $p^+$  and  $n$ -channel,

