Tutorial-4: Real-Time Computer Systems and Architecture

Scheduling

Q 1. What is pre-emptive scheduling and non-preemptive scheduling? Briefly describe the pros and cons of the latter.

☆ **Q 2.** Briefly explain the terms deadlock and starvation. What is/are their difference(s)? scramble resource 的结果 → waiting

$$\begin{tikzcd} 进程A \arrow[d] & 进程B \arrow[d] \arrow[dl] \\ 资源A \arrow[ur] & 资源B \end{tikzcd}$$

Q 3. Our periodic real-time tasks as shown in Table below are to be run on a uniprocessor:

a) Arrange these tasks using Earliest Deadline First (EDF).

b) Determine whether the tasks can be schedule using EDF.

Task	Processing Time (ms)	Period (ms)	Deadline (ms)
T1	25	150	150
T2	7	40	40
T3	10	60	60
T4	10	30	30

Parellelism

Q 4. What is the essential characteristic of the superscalar approach to processor design? multiple pipelines + replicating resource

Q 5. What is the difference between the superscalar and superpipelined approaches? decrease machine cycle

Q 6. Briefly define the following terms:

- True data dependency
- Procedural dependency
- Resource conflicts
- Output dependency
- Antidependency.

Q 7. What are the key elements of a superscalar processor organization?

☆ **Q 8.** List and briefly define three types of computer system organization.

☆ **Q 9.** What are the chief characteristics of an SMP?

Q 10. What are some of the potential advantages of an SMP compared with a uniprocessor?

Q 11. What are some of the key OS design issues for an SMP?

Q 12. What is the difference between software and hardware cache coherent schemes?

Q 13. Consider an SMP with both L1 and L2 caches using the MESI protocol. One of four states is associated with each line in the L2 cache. Are all four states also needed for each line in the L1 cache? If so, why? If not, explain which state or states can be eliminated.

Q 14. Summarize the differences among simple instruction pipelining, superscalar, and simultaneous multithreading. register banks replicate

Q 15. List some examples of applications that benefit directly from the ability to scale throughput with the number of cores.

☆ **Q 16.** At a top level, what are the main design variables in a multicore organization?

Q 17. List some advantages of a shared L2 cache among cores compared to separate dedicated L2 caches for each core.