

RST 55

It is a maskable interrupt. When this interrupt is occurred, the processor content of the PC register into the stack and branches to 002CH address.

INTR

It is a maskable interrupt, having the lowest priority among all interrupts. It is disabled by resetting the microprocessor.

If INTR signal goes high, the following events can occur –

- The microprocessor continuously checks the status of the INTR signal executing each instruction.
- If the INTR signal is active (high), the microprocessor finishes the instruction and sends a low-active Interrupt Acknowledge signal.
- After receiving the interrupt, the microprocessor saves the address of the instruction to the stack and begins executing the received instruction.

Interrupt Processing

Interrupt processing refers to the process by which the microprocessor responds to an interrupt signal. When an interrupt is triggered, the microprocessor temporarily pauses its current task, saves the current state of the program and execution context, and begins executing the Interrupt Service Routine (ISR) associated with the interrupt. The ISR is responsible for processing the interrupt and determining the appropriate action to take. Once the ISR has completed its task, it returns control to the main program, and the microprocessor resumes its previous task. Interrupt processing is a crucial aspect of microprocessing, as it enables the microprocessor to handle external events and respond to them in a timely and efficient manner.

MULTIPLE CHOICE QUESTIONS

- 1. Hexadecimal can express in one digit what is done by following binary number of binary digits**
 - One
 - Four
 - Two
 - Eight
- 2. NAND gates are preferred over others because these have lower fabrication area**
 - Have lower fabrication area
 - Can be used to make any gate
 - Consume less electronic power
 - Provide maximum density in a chip
- 3. According to Demorgan's theorem A + B + C + D =**
 - $\bar{A}\bar{B}\bar{C}\bar{D}$
 - $AB + CD$
 - $A + BC + D$
 - $A + B + C + D$
- 4. According to Demorgan's theorem $\bar{ABC}\bar{D} =$**
 - $A + \bar{B} + \bar{C} + \bar{D}$
 - $A + B + C + D$
 - $A + B + C + D$
 - $A + B + CD$
- 5. The logic unit shown below is as the type**
 - AND
 - NAND
 - OR
 - NOT
- 6. The truth table shown below is for**

Inputs		Outputs
a	b	
0	0	0
0	1	1
1	0	1
1	1	1

 - NAND
 - OR
 - AND
 - NOT
- 7. Odd parity of word can be conveniently tested by**
 - OR gate
 - NOR gate
 - AND gate
 - XOR gate
- 8. A record at the end of file which contains control total is**
 - Pointers
 - Trunk
 - Trailer
 - Trunkey
- 9. Binary means**
 - Three
 - Ten
 - Four
 - Two
- 10. The digits used in a binary number system areand.....**
 - 9 and 0
 - 1 and 2
 - 0 and 1
 - 3 and 4
- 11. Names, numbers and other information needed to solve a problem are called**
 - Program
 - Data
 - Instruction
 - Controls
- 12. The is a sequence of instructions that tells the computer how to process the data**
 - Data
 - Controls
 - Program
 - Instruction
- 13. Computer ICs work reliably because they based on...design**
 - Top-button
 - Two-stage
 - System
 - Two-status
- 14. When a transistor is cut off or saturated, transistor.....have almost no effect**
 - Wave
 - Stage
 - Variations
 - Circuits

15. A.....is group of devices that store digital data
 A. Circuits B. Variations
 C. Register D. Bit
16. is an abbreviation for binary digit
 A. 0 and 1 B. Base
 C. Binary D. Bit
17. A byte is a string of bits
 A. Two B. Eight
 C. Four D. Ten
18. The control and arithmetic-logic sections are called the,
 A. Block diagram
 B. Input output unit
 C. Control unit
 D. Central Processing Unit
19. A microcomputer is a computer that uses afor its CPU
 A. Chips B. Microprocessor
 C. Registers D. Vacuum tube
20. The hexadecimal number system is widely used in analyzing and programming...
 A. Registers
 B. Microprocessors
 C. Chips
 D. Vacuum tube
21. The hexadecimal digits are 0 and 9 and A to...
 A. E B. G
 C. F D. D
22. The main advantage of hexadecimal numbers is the ease of conversion from hexadecimal toand vice versa
 A. Decimal B. ASCII
 C. Binary D. BCD
23. A typical microcomputer may have up to 65,536 registers in its memory. Each of these registers usually called a
 A. Address
 B. Chip
 C. Registers
 D. Memory location
24. Binary - Coded - decimal (BCD) numbers express each digit as a
 A. Bytes
 B. Bit
 C. Nibble
 D. All of the above
25. BCD numbers are useful whenever ...information is transferred into or out a digital system
 A. Decimal B. ASCII
 C. Binary D. Hexadecimal
26. The ASCII code is a 7-bit code for
 A. Letters
 B. Other symbols
 C. Numbers
 D. All of the above
27. The binary number 1100 0101 hasbytes
 A. 1 B. 4
 C. 2 D. 8
28. How many bytes are there in 1011 1001 0110 1110 numbers?
 A. 1 B. 4
 C. 2 D. 8
29. What is the base of F4C316 numbers?
 A. 2 B. 8
 C. 4 D. 16
30. What is the decimal equivalent of 2^{10} ?
 A. 4096 B. 1000
 C. 1024 D. 16
31. What does 4k represent?
 A. 4000 B. 40
 C. 4096 D. 400
32. Express 8192 in K units
 A. 8×10^3 K
 B. 8K
 C. 8,192K
 D. All of the above
33. Solve the following equation for X:
 $X_{10} = 11001001_2$
 A. 201 B. 214
 C. 132 D. 64
34. A micro-processor has memory locations from 0000 to 3FFF. Each memory location stores 1 bytes. How many bytes can the memory store? Express this in kilobytes
 A. 4095,4K B. 32740,32K C.
 16,38416K D. 46,04046K
35. If a microcomputer has 64K memory, what are the hexadecimal notations for the first and last memory location ?
 A. 0000, EEEE B. 0000, FFFF
 C. 0, 64 D. 0000, 9999
36. How many nibbles are there in 1001 0000 0011 number
 A. Two B. One
 C. Three D. Eight
37. What is the ASCII code for T?
 A. 1010100 B. 1011100
 C. 1011010 D. 1011111
38. A gate is a logic circuit with one or more input signals but output signal
 A. Two B. One
 C. Double D. More than one
39. An inverter is a gate with only input; the output is always in the opposite state from the input
 A. One
 B. More than one
 C. Two
 D. All of the above
40. An inverter is also called agate
 A. NOT B. OR
 C. OR D. NAND
41. The OR gate has two or more input signals. If any input is the output is high
 A. Low
 B. 0
 C. High
 D. All of the above
42. The number of input words in a truth table always equals...., where n is the number of input bits
 A. 10^n B. 4^n
 C. 2^n D. 8^n
43. Thegate has two or more input signals. All inputs must be high to get a high output
 A. OR
 B. AND
 C. NAND
 D. NOR
44. In Boolean algebra, the over bar stands for the NOT operation, the plus sign stands for the operation
 A. AND B. NAND
 C. OR D. NOR
45. In Boolean algebra, the dot sign stands for the....operation
 A. AND B. NAND
 C. OR D. NOR

46. The inverter OR gate and AND gate are called decision-making elements because they can recognize some input....while disregarding others. A gate recognizes a word when its output is.....
- Words, high
 - Bytes, high
 - Bytes, low
 - Character low
47. How many inputs signals can a gate have?
- One
 - Two only
 - More than one
 - Both (A) and (B)
48. How many output signals can a gate have?
- One
 - Two only
 - More than one
 - Both (A) and (B)
49. The binary equivalent of the octal number 13.54 is
- 1011.1011
 - 1001.1110
 - 1101.1110
 - All of the above
50. The octal equivalent of 111010 is
- 81
 - 71
 - 72
 - All of the above
51. The octal equivalent of the number 11010.1011 is
- 32.15
 - 32.27
 - 63.51
 - All of the above
52. The decimal equivalent of the binary number 11100001111 is
- 1806
 - 2806
 - 1807
 - All of the above
53. The binary equivalent of the decimal number 135.75 is
- 1101.1
 - 3789.75
 - 1101.0111
 - All of the above
54. The decimal equivalent of binary number 0.0111 is
- 4375
 - 0.5375
 - 0.4375
 - 0.4375
55. The binary code of $(21.115)_{10}$ is
- 10101.001
 - 10101.010
 - 10100.001
 - 10100.100
56. Which of the following gate is two-level logic gate?
- OR gate
 - EXCLUSIVE OR gate
 - NAND gate
 - NOT gate
57. The binary code of $(73)_{10}$ is
- 1010001
 - 1100101
 - 1000100
 - 1001001
58. An AND gate will function as OR if
- All the inputs to the gates are "1"
 - All the inputs are "0"
 - Either of the inputs is "1"
 - All the inputs and outputs are complemented
59. An OR gate has 6 inputs. How many input words are in its truth table?
- 64
 - 16
 - 32
 - 128
60. An OR gate has 6 inputs. What is the only input word that produces a 0 output?
- 000000
 - B. 111000
 - C. 000111
 - D. 111111
61. An AND gate has 7 inputs. How many input word are in its truth?
- 64
 - 16
 - 32
 - 128
62. An AND gate has 7 inputs, what is the only input word that produces a 1 output?
- 0000000
 - B. 1110000
 - C. 0001111
 - D. 1111111
63. A NOR gate has or more input signals. All inputs must be to get a high output
- Low
 - Some low some high
 - High
 - I's
64. A NOR gate recognizes only the input word whose bits are....
- 0's and 1's
 - 0's
 - 1's
 - 0's or 1's
65. The NOR gate is logically equivalent to an OR gate followed by an ...
- AND
 - XOR
 - XAND
 - Inverter
66. De Morgan's first theorem says that a NOR gate is equivalent to a bubbledgate
- AND
 - XOR
 - XAND
 - NOR
67. A NAND gate is equivalent to an AND gate followed by an inverter. All inputs must be....to get a low output
- Low
 - Some low and some high
 - High
 - 0's
68. De Morgan's second theorem says that NAND gate is equivalent to a
- AND
 - XOR
 - XAND
 - OR
69. An XOR gate recognizes only words with annumber of 1's
- Even
 - Different
 - Odd
 - All of the above
70. The 2-input XOR gate has a high output only when the input bits are....
- Even
 - Low
 - Different
 - High
71. The XOR gates are ideal for testing parity because even-parity words produce a Output and odd-parity words produce aoutput
- Low, high
 - Odd, even
 - High, low
 - Even, odd
72. An odd-parity generator produces an odd-parity bit to go along with the data. The parity of the transmitted data is An XOR gate can test each received word for parity rejecting words with Parity
- Odd, even
 - Low, high
 - High, low
 - Even, odd
73. The EXCLUSIVE-NOR gate is equivalent to angate followed by an inverter
- OR
 - NAND
 - AND
 - XOR
74. Small-scale integration, abbreviated refers to fewer than 12 gates on the same chip. Medium-scale integration (MSD) means 12 to 100 gates per chip. And large-scale integration (LST) refers to more thangates per chip
- SSI, 75
 - SSI, 1000
 - SSI, 100
 - SSI, 10000

75. The two basic technologies for digital ICs are bipolar and MOS. Bipolar technology is preferred for and whereas MOS technology is better suited to LSI
- A. SSI, MSI B. SSI, LSI
C. MSI, LSI D. ECL, DTL
76. What is 1's complement of 0000 1111 0010 1101 number?
- A. 1111 0000 0010 1101
B. 1111 0000 1101 0010
C. 1111 0000 0010 1101
D. 1111 1100 1010 1100
77.has become the most widely used bipolar family
- A. DTL B. ECL
C. TTL D. MOS
78.is the fastest logic family' it's used in high-speed applications
- A. DTL B. ECL
C. TTL D. MOS
79.dominates the LSI field andused extensively where lowest power consumption is necessary
- A. NMOS, PMOS
B. NMOS, CMOS
C. PMOS, CMOS
D. MOSFET, PMOS
80. The 7400 series, also called standard TTL, contains a variety of SSI and ... chips that allow us to build all kinds of digital circuits and systems
- A. LSI B. MOS
C. MSI D. MOSFET
81. Standard TTL has a multiple emitter input transistor and a output
- A. Totem-pole B. Register
C. Bipolar D. Transistor
82. The 7400-series devices guaranteed to work reliably over a temperature range of 0 to and over a voltage range of 4.75 to 5.25 V
- A. 80°C B. 100°C
C. 70°C D. 90°C
83. A ... TTL device can sink up to 16 mA and can source up to 400mA
- A. Low-power B. Standard
C. High-power D. Schottky
84. The maximum number of TTL loads that a TTL device can drive reliably over the specified temperature range is
- A. Fanout
B. Chip
C. Bipolar
D. Universal logic circuit
85. Digital design often starts by constructing a table?
- A. Standard
B. Truth
C. Two-Stage
D. Two-dimensional
86. A preliminary guide for comparing the simplicity of logic circuits to count the number of input.....leads
- A. Wires B. Transistors
C. Gates D. Registers
87. A bus is a group ofcarrying digital signals
- A. Wires B. Transistors
C. Gates D. Registers
88. One way to simplify the sum-of-products equation is to use Boolean algebra. Another way is the....map
- A. De Morgan B. Schottky
C. Standard D. Karnaugh
89. What are the fundamental products for inputs words $ABCD = 0010$, $ABCD = 1101$ and $ABCD = 1110$?
- A. ABCD, ABCD, ABCD
C. ABCD, ABCD, ABCD
B. ABCD, ABCD, ABCD
D. ABCD, ABCD, ABCD
90. The ALU carries out arithmetic and numbers rather than decimal numbers
- A. Decimal
B. Binary
C. Hexadecimal
D. All of the above
91. A half-adder adds....bits
- A. 16 B. 19
C. 8 D. 2
92. A full-adder addsbits and producing a SUM and a....
- A. 8, SUBTRACTION
C. 3, CARRY
B. 16, DIVIDE
D. All of the above
93. A binary adder is a logic circuit that can add....binary numbers at a time
- A. Hundreds B. One
C. Thousands D. Two
94. The leading bit stands for theand the remaining bits for the, is known as signed binary numbers
- A. Sign, remainder
B. Value, sign
C. Sign, magnitude
D. Variable, value
95. Signed binary numbers requires too much hardware. This has led to the use of ... complements to represent negative numbers
- A. 1's B. 3's
C. 2's D. No
96. A 2's-complement adder-subtractor can add or subtract binary numbers. Sign-magnitude numbers represent.....decimal numbers and 2's complements stands for
- A. Hexa, sign
B. Positive, negative
C. Sign, hexa
D. Negative, positive
97. How many full and half-adders are required to add 16-bit numbers?
- A. 8 half-adders, 8 full-adders
B. 16 half-adders, no full-adders
C. 1half-adders, 15 full-adders
D. Half-adders, 12 full-address
98. Express-7 as 16-bits signed binary numbers
- A. 0000 0000 0000 0111
B. 0111 0000 0000 0000
C. 1000 0000 0000 0111
D. 0111 0000 0000 0000
99. Convert the 1000 0000 0000 1111 signed binary number to decimal number
- A. +15 B. -30
C. -15 D. +30
100. What is the 2's complement of 0011 0101 1001 1100 number?
- A. 1100 1001 1100 1011
B. 1100 1010 0110 0100
C. 1100 1010 0110 0011
D. 1100 1010 1111 1111
101. What is the 2's-complement presentation of -24 in a 16-bit microcomputer?
- A. 0000 0000 0001 1000
B. 1111 1111 1110 1000
C. 1111,1111 1110 0111
D. 0001 0001 1111 0011

102. A flip-flop is aelement that stores a binary digit as a low or high voltage
 A. Chip B. I/O
 C. Bus D. Memory
103. With an RS latch a high S and low R sets the output to; a low S and a high R....the output to low
 A. No change, set
 B. High, reset
 C. Race, high
 D. Set, Reset
104. With a NAND latch a low R and a low S produce acondition
 A. Race B. Reset
 C. Set D. No change
105. Computers use thousands of flip-flops. To coordinate the overall action, a common signal called theis sent to each flip-flop
 A. Latch B. Master
 C. Clock D. Slave
106. With positive clocking the clock signal must be.....for the flip-flop to respond
 A. High B. Set
 C. Low D. Race
107. With a JK master-slave flip-flop the master is clocked when the clock is, and the slave is triggered when the clock is.....
 A. Set, reset B. High, low
 C. Race, no change D. Set, race
108. When the LOAD input of a buffer register is active, the input word would be stored on the next positive ..edge
 A. Clock B. Register
 C. Pulse D. Transistor
109. A shift register moves theleft or right. Serial loading means storing a word in a shift register by entering a bit per clock pulse. With parallel or broadside loading, it takes only onePulse to load the input word
 A. Light, eight, clock
 C. Right, eight, clock
 B. Bits, one, register
 D. Bits, one, clock
110. One flip-flop divides the clock frequency by a factor of ... in general, n flip-flop divide by 2^n
 A. Two, n+1 B. 12, n+12
 C. Four, n+4 D. Two, 2ⁿ
111. Instead of counting with binary numbers, a ring counter uses words that have a signal high.....
 A. Bytes B. Gate
 C. Bit D. Chip
112. Theis ultraviolet-light erasable and electrically programmable. This allows the user to erase and store until programs and data are perfected
 A. EPROM B. PROM
 C. ROM D. RAM
113. The memory cell of a dynamic RAM is simple and smaller than the memory cell of aRAM
 A. Volatile B. Semiconductor
 C. Static D. Bipolar
114. How many memory locations can 14 address bits access?
 A. 16,384 B. 4096
 C. 8,192 D. 14
115. The 2764 is 65,536-bit EEPROM organized as 8,192 words of 8 bits each. How many address lines does it have?
 A. 12 B. 13
 C. 14 D. 8
116. The 2732 is a 4096x8 EPROM. How many address lines does it have?
 A. 12 B. 13
 C. 14 D. 8
117. Address 200H contains the byte 3FH. What is the decimal equivalent of 3FH
 A. 63 B. 16
 C. 32 D. 38
118. What is the highest address in a 48k memory? Express in hexadecimal and decimal form
 A. 7FFFH, 64387 C. BFFFH, 49,151
 B. BFFFH, 49,152 D. 7FFFH, 64,386
119. Flip-flop output are always
 A. Complementary
 C. The same
 B. Independent of each other
 D. Same as inputs
120. A combinational logic circuit which is used to send data coming from a single source to two or more separate destinations is called as
 A. Decoder B. Multiplexer
 C. Encoder D. Demultiplexer
121. In which of the following adder circuits, the carry look ripple delay is eliminated?
 A. Half adder
 C. Full adder
 B. Parallel adder
 D. Carry-look-ahead adder
122. Consider as RS flip-flop with both inputs set to 0. If a momentary '1' is applied at the input S, then the output
 A. Q will flip from 0 to 1
 C. Q will flip from 0 to 1
 B. Q will flip from 0 to 1 and then back to 0
 D. Q will flip from 0 to 1 and then back to 0
123. How many full addresses are required to construct an m-bit parallel adder?
 A. m/2 B. m
 C. m-1 D. m+1
124. The dynamic race hazard problem occurs in
 A. Combinational circuits only
 C. Both combinational and sequential circuits
 B. Sequential circuits only
 D. None of the above
125. A shift register can be used for
 A. Parallel to serial conversion
 C. Serial to parallel conversion
 B. Digital delay line
 D. All of the above
126. Which of the following flip-flops is free from race around problem?
 A. T flip-flop
 C. SR flip-flops
 B. Master slave JK flip-flop
 D. All of the above
127. For an input pulse train of clock period T, the delay produced by an n stage shift register is
 A. (n + 1)T B. (n + 1)T
 C. Nt D. 2nT

128. The master slave JK flip-flop is effectively a combination of
 A. An SR flip-flop and a T flip-flop
 C. A T flip-flop and a D flip-flop
 B. An SR flip-flop and a D flip-flop
 D. Two T flip-flops
129. The functional difference between SR flip-flop and JK flip flop is faster than SR flip-flop
 A. JK flip-flop is faster than SR flip-flop
 C. JK flip-flop accepts both input 1
 B. JK flip-flop has a feedback path
 D. JK flip-flop does not require external clock
130. The term sum-of-products in Boolean algebra means
 A. The AND function of several OR functions
 C. The OR function of several OR functions
 B. The OR function of several AND functions
 D. The AND function of several AND functions
131. A positive AND gate is also a negative
 A. NAND gate B. AND gate
 C. NOR gate D. OR gate
132. What table shows the electrical state of a digital circuit's output for every possible combination of electrical states in the inputs?
 A. Function table B. Routing table
 C. Truth table D. ASCII table
133. How many bits are required to encode all twenty six letters, ten symbols, and ten numbers?
 A. 5 B. 2
 C. 6 D. 3
134. The number of two-input NAND gates required to produce the two-input OR function is
 A. 1 B. 3
 C. 2 D. 4
135. What logic function is obtained by adding an inverter to the inputs of an AND gate?
 A. OR B. XOR
 C. NAND D. NOR
136. Which of the following Boolean algebra expression is incorrect?
 A. $AB + A(B + C) + B(B + C) = B + AC$
 B. $\overline{AB(C+BD)} + \overline{AB} C = \overline{BC}$
 C. $AB(\overline{C} + \overline{D}) = \overline{A} + B + \overline{CD}$
 D. $(A + C)(ABC + ACD) = ABC + ACD$
137. Which gates is known as universal gate?
 A. NOT gate B. NAND gate
 C. AND gate D. XOR gate
138. What logic function is produced by adding an inverter to the output of an AND gate?
 A. NAND B. XOR
 C. NOR D. OR
139. An OR gate can be imagined as
 A. Switches connected in parallel
 B. MOS transistors connected in series
 C. Switches connected in parallel
 D. All of the above
140. What logic function is produced by adding an inverter to each input and the output of an AND gate?
 A. NAND B. OR
 C. NOR D. XOR
141. Which of the following algebra statements represent commutative law
 A. $(A + B) + CA = (B + C)$
 B. $A + B = B + A$
 C. $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$
 D. $A + AA = A$
142. For what logic gate the output is complement of the input?
 A. NOT B. OR
 C. AND D. XOR
143. ASCII and EBCDIC differ in
 A. Their efficiency in storing data
 B. The random and sequential access method
 C. The number of bytes used to store characters
 D. Their collecting sequences
144. In which code the successive code characters differ in only one bit position?
 A. Gray code B. 8421 code
 C. Excess 3 code D. Algebraic code
145. Cyclic codes are used in
 A. Data transfer
 B. Continuously varying signal
 C. Arithmetic and logical computation
 D. All of the above
146. The 2's compliment of binary number 010111.1100 is
 A. 101001.1100 B. 010111.0011
 C. 101000.0100 D. 101000.0011
147. The ASCII CODE
 A. Is a subset of 8-bit EBCDIC
 B. Is used only in Western Countries
 C. Is version II of the ASC Standard
 D. Has 128 characters, including 32 control characters
148. The Gray code for decimal 7 is
 A. 0111 B. 0100
 C. 1011 D. 1010
149. The octal equivalent of decimal 324.987 is
 A. 504.771 B. 815.234
 C. 640.781 D. 90.987
150. Where an old number is converted into the binary number, the least significant digit (LSD) is
 A. 0
 B. 0 or 1
 C. 1
 D. All of the above
151. Which of the following logic families use bipolar transistors?
 A. TTL B. NMOS
 C. GaAs D. CMOS
152. Which of the following TTL subfamily is the fastest
 A. Standard TTL
 B. Schottky TTL
 C. High-speed TTL
 D. Low-speed TTL
153. The output 0 and 1 levels for TTL logic family is approximately
 A. 0.1 and 5v
 B. 0.9 and 1.75
 C. 0.6 and 3.5 v
 D. -1.75 and -0.9v
154. The functional capacity of SSI devices is
 A. 1 to 11 gates
 B. 100 to 10,000 gates
 C. 12 to 99 gates
 D. More than 10,000 gates

155. The functional capacity for LSI devices is

- A. 1 to 11 gates
- B. 100 to 10,000 gates
- C. 12 to 99 gates
- D. More than 10000 gates

156. The time required for a pulse to decrease from 90 to 10 percent of its maximum value is known as

- A. Rise time
- B. Binary level transition period
- C. Decay time
- D. Propagation delay

157. Which logic family dissipates the minimum power?

- A. DTL
- B. ECL
- C. TTL
- D. CMOS

158. Which TTL sub-family has maximum speed?

- A. Standard TTL
- B. High speed TTL
- C. Schottky-clamped TTL
- D. Low power TTL

159. Which of the following is the first integrated logic family?

- A. RTL
- B. TTL
- C. DTL
- D. MOS

160. Why are digital circuits easier to design than analog circuits?

- A. They do not control electricity precisely over a wide range
- B. They are made in the form of ICs
- C. All elements of digital circuit are from the same family
- D. They are smaller in size

161. Which of the following electronic component is not found in ordinary ICs?

- A. Diodes
- B. Transistors
- C. Resistors
- D. Inductors

162. The fan-out capability of a digital building block can be defined as

- A. The number of inputs that one output can transmit to
- B. The amount of cooling required for fanning the heat out
- C. The number of inputs that can transmit to one input
- D. The maximum power dissipation (heat generation) that the unit can stand

163. What is the main advantage of using MOSFET rather than bipolar transistor circuitry in ICs

- A. Much greater complexity (more components) than bipolar circuits; better economy
- B. Higher operating speed than bipolar circuits
- C. Fewer power supply connections are required with DOS ICs
- D. System designers are more familiar with MOS circuitry

164. FETs are used in linear ICs to

- A. Increase input resistance
- B. Increase device complexity
- C. Provide large resistance
- D. A and B above

165. Resistor Ratio design is used in linear ICs because

- A. Ratio increase input resistance
- B. Ratio increase amplifier gain
- C. Precise resistor values are not possible with IC processes
- D. All of the above

166. A p-channel enhancement type MOSFET performs much the same functions as a PNP transistor, except that

- A. It operates much faster
- B. It is considerably larger
- C. It is controlled by voltage rather than by current, so that it requires very little current at the control terminal
- D. It is controlled by current than voltage like a bipolar transistor

167. What advantages do ICs have over discrete-device circuits due to their greater complexity (i.e. more circuitry in less area),

- A. Smaller size
- B. Lower cost
- C. Higher reliability
- D. All of the above

168. The radix of the binary number is

- A. 3
- B. 2
- C. 1
- D. 10

169. The number of binary bits required to represent a hexadecimal digit is

- A. 3
- B. 6
- C. 4
- D. 8

170. $\bar{A} + \bar{B} + \bar{C} = D$ represents as:

- A. NAND gate
- B. EX-OR gate
- C. OR gate
- D. AND gate

171. The output of the following gate is 1 only if at least one of its inputs is 0

- A. AND gate
- B. NAND gate
- C. OR gate
- D. NOT gate

172. The 1's compliment of binary number 0.01011 is :

- A. 1.10100
- B. 0.0110
- C. 0.0010
- D. 1.1101

173. The 2's complement of binary number 0.01010 is

- A. 1.10101
- B. 1.10100
- C. 0.10101
- D. 0.10100

174. A half-adder is also known as:

- A. AND circuit
- B. NOR circuit
- C. NAND circuit
- D. EX-OR circuit

175. The output of the following gate is 0 only if at least one of the inputs is 1:

- A. AND gate
- B. EX-OR gate
- C. OR gate
- D. NOR gate

176. Which of the following Boolean algebra rules is wrong?

- A. $0+A=A$
- B. $A+A=A$
- C. $1+A=1$
- D. $1 \cdot x = 1$

177. The octal system has the radix of

- A. 2
- B. 8
- C. 4
- D. 10

178. The binary system has the radix of

- A. 0
- B. 2
- C. 1
- D. $\frac{1}{2}$

179. Octal number system uses fundamental digits 0 to 7.124 (octal) in decimal equivalent is equal to

- A. 180
- B. 84
- C. 82
- D. 86

180. 92 (decimal) is octal number system is equivalent to

- A. 128_8
- B. 132_8
- C. 130_8
- D. 134_8

181. Four digit binary quantity 1001 is represented in the decimal system by?

- A. 7
- B. 1
- C. 9
- D. 13

182. Binary number 101101 is equivalent in decimal form to?

- A. 41
- B. 45
- C. 43
- D. 47

183. Number 37310 is equivalent in binary system to
 A. 101110101
 B. 101010101
 C. 100110101
 D. 101110011
184. According to Boolean algebra $A + A = A$ is
 A. A
 B. A/n
 C. NA
 D. 1
185. In Boolean algebra $A \cdot A = A$
 A. 5A
 B. A5
 C. A/5
 D. A
186. In Boolean algebra $A \cdot 0 = 0$ is
 A. 1
 B. A
 C. 0
 D. $1 + A$
187. The simplification of $AB + B\bar{C} + BC$ gives
 A. $AB \pm BC$
 B. $BC + BC$
 C. $AB + BC$
 D. B
188. Which of the following is not functionally a complete set?
 A. AND, OR
 B. NOR
 C. NAND
 D. AND, OR, NOT
189. Which of the following is not true?
 A. $0 \cdot X = 0$
 B. $1 \cdot X = 0$
 C. $0 \cdot X = 1$
 D. $1 \cdot X = 1$
190. The reduced form of the Boolean expression $(A + B)(A + C)$ is:
 A. $AB + AC$
 B. $AC + B$
 C. $A + B + C$
 D. $A + BC$
191. Which of the following is a universal gate?
 A. AND
 B. EX-OR
 C. OR
 D. NAND
192. Which function positive logic is equivalent to OR functions in negative logic?
 A. NOT
 B. OR
 C. AND
 D. NOR
193. Which of the following expression is wrong?
 A. $1 + 0 = 1$
 B. $1 + 0 + 1 = 1$
 C. $1 + 1 = 0$
 D. $1 + 1 + 1 = 1$
194. The m-bit parallel adder consists of
 A. $(m + 1)$ full adders
 B. $m - 1$ full adder
 C. $m/2$ full adders
 D. m full adders
195. A flip can store
 A. 1 bits of data
 B. 3 bits of data
 C. 2 bits of data
 D. 4 bits of data
196. A shift register can be used for:
 A. Parallel to serial conversion
 B. Digital delay line
 C. Serial to parallel conversion
 D. All of the above
197. Semiconductor memory is:
 A. Somewhat larger than magnetic core memory
 B. A volatile memory
 C. Somewhat larger than the magnetic core memory
 D. All of the above
198. The logic 1 in positive logic system is represented by:
 A. Zero voltage
 B. Higher voltage level
 C. Lower voltage level
 D. Negative voltage
199. A combinational logic circuit which is used when it is desired to send data from two or more source through a single transmission line is known as
 A. Encoder
 B. Multiplexer
 C. Decoder
 D. De-multiplexer
200. A logic circuit which is used to change a BCD number into an equivalent decimal number is
 A. Decoder
 B. Multiplexer
 C. Encoder
 D. Code converter
201. A combinational logic circuit which generates particular binary word or number is
 A. Decoder
 B. Encoder
 C. Multiplexer
 D. De-multiplexer
202. Parallel adders are
 A. Combinational logic circuits
 B. Both of the above
 C. Sequential logic circuits
 D. All of the above
203. A de-multiplexer is also known as
 A. Data selector
 B. Multiplexer
 C. Data distributor
 D. Encoder
204. A multiplexer is known as
 A. Coder
 B. Data selector
 C. Decoder
 D. Encoder
205. A flip-flop can store
 A. One bit of data
 B. Three bits of data
 C. Two bits of data
 D. Any number of bits of data
206. Which of the following input combination is not allowed in an SR flip-flop?
 A. S = 0, R = 0
 B. S = 1, R = 0
 C. S = 0, R = 1
 D. S = 1, R = 1
207. When an inverter is placed between both inputs of an SR flip-flop, the resulting flip-flop is
 A. JK flip-flop
 B. T flip-flop
 C. D flip-flop
 D. Master slave k flip-flop
208. The clock signals are used in sequential logic circuits
 A. To tell the time of the day
 B. To tell how much time has elapsed since the system was turned on
 C. To carry serial data signals
 D. To synchronize events in various parts of a system
209. What logic function is obtained by adding an inverter to the output of an AND gate?
 A. OR
 B. XOR
 C. NAND
 D. NOR
210. The simplified form of the Boolean expression $(X + Y + XY)(X + Z)$ is
 A. $X + Y + Z$
 B. $X + YZ$
 C. $XY + YZ$
 D. $XZ + Y$
211. The maximum count which a 6-bit binary word can represent is
 A. 36
 B. 63
 C. 64
 D. 65
212. The highest decimal number that can be represented with 10 binary digits is
 A. 1023
 B. 512
 C. 1024
 D. All of the above
213. What is the hexadecimal equivalent of a binary number 10101111
 A. AF
 B. 8C
 C. 9F
 D. All of the above

214. Which of the following logic families has the highest noise immunity?
A. RTL B. TTL
C. DTL D. HTL

215. Pick up wrong logical expression
A. $1 + 0 = 0 + 1 = 1$ B. $X + Y = X \cdot Y$
C. $0 + 0 = 1.1 = 0$ D. $X + 0 = X$

216. In a four input NAND gate all but one inputs are 1, the output is
A. 4 B. 1
C. $\frac{1}{4}$ D. 0

217. In a four input AND gate all but one inputs are 1, the output is
A. 0 B. 1
C. $\frac{1}{4}$ D. 4

218. According to Indempotent law, $X + X$
A. 1 B. X
C. 0 D. $X \cdot X$

219. According to Indempotent law, $X \cdot X =$
A. 1 B. X
C. 0 D. $X + X$

220. The output will be one in case any input is one in the case of
A. OR gate B. NAND gate
C. AND gate D. NOT gate

221. Which of the following circuit is known as half adder?
A. EXCLUSIVE AND circuit
C. Flip-flop circuit
B. INCLUSIVE OR circuit
D. EXCLUSIVE OR circuit

222. Which of the following function is referred as the complementary?
A. OR function
B. NAND function
C. NOT function
D. AND function

223. Which of the following statement illustrates of the distribution law?

- A. $(A+) + C = A + (B + C) = A + B + C$
- B. $(AB)C = A(BC) = ABC$
- C. $A + B = B + A$
- D. $A(B + C) = (AB) + (AC)$

224. Which of the following is termed as minimum error code?

- A. Binary code B. Excess 3-code
- C. Gray code D. Octal code

225. For which of the following flip-flop the output is clearly defined for all combinations of two inputs?

- A. D-type flip-flop B. JK flip-flop
- C. R-S flip-flop D. T flip-flop

226. A 4-bit shift register can be made by using

- A. 3 JK flip-flop B. 5 JK flip-flop
- C. 4 JK flip-flop D. 8 JK flip-flop

227. Which of the following statements is false

- A. $AB = A + B$ B. $AB = AB$
- C. $A + B = AB$ D. $A + A = A$

228. The minimum form of the expression $(A + B)(A + B + C)$ will be

- A. $A + CB$ B. $AC + B$
- C. $A + BC$ D. $A + BC$

229. One's complement of 1011.01 is

- A. 0100.10 B. 1011.10
- C. 0100.11 D. 0100.01

230. The NAND gate output will be low if the two inputs are

- A. 00 B. 10
- C. 01 D. 11

231. What is the binary equivalent of the decimal number 368

- A. 101110000 B. 111010000
- C. 110110000 D. 111100000

232. The decimal equivalent of hex number 1A53 is

- A. 6793 B. 6973
- C. 6739 D. 6379

233. $(734)_8 = (?)^{16}$

- A. 1 CD B. 1 CD
- C. DC1 D. 1 DC

234. The simplification of the Boolean expression $(\overline{ABC}) + (\overline{\overline{ABC}})$ is

- A. 0 B. A
- C. 1 D. BC

235. The number of control lines for a 8-to-1 multiplexer is

- A. 2 B. 4
- C. 3 D. 5

236. How many Flip-flops are required for mod - 16 Counter is 4

- A. 5 B. 3
- C. 6 D. 4

237. EPROM contents can be erased by exposing it to

- A. Ultraviolet
- B. Burst of microwaves
- C. Infrared rays
- D. Intense heat radiations

238. The hexadecimal number 'A0' has the decimal value equivalent to.....

- A. 80 B. 100
- C. 256 D. 160

239. The Gray code for decimal number 6 is equivalent to

- A. 1100 B. 0101
- C. 1001 D. 0110

240. The Boolean expression $\overline{A} \cdot B + A \cdot \overline{B} + A \cdot B$ is equivalent to

- A. $A + B$ B. $\overline{A + B}$
- C. $\overline{A} \cdot B$ D. $A \cdot B$

241. The digital logic family which has minimum power dissipation is

- A. TTL B. DTL
- C. RTL D. CMOS

242. The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either

- A. A NAND or an EX - OR
- B. An AND or an EX - OR
- C. An OR or an EX - NOR
- D. A NOR or an EX - NOR

243. Data can be changed from special code to temporal code by using

- A. Shift registers
- B. Combinational circuit
- C. Counters
- D. A/D converters

244. A ring counter consisting of five Flip-Flops will have

- A. 5 states B. 32 states
- C. 10 states D. Infinite states

245. The speed of conversion is maximum in

- A. Successive - approximation A/D converter
- B. Parallel - comparative A/D converter
- C. Counter ramp A/D converter
- D. Dual-slope A/D converter

246. The 2's complement of the number 1101101 is

- A. 0101110 B. 0110010
- C. 0111110 D. 0010011

247. The correction to be applied in decimal adder to the generated sum is

- A. 00101 B. 01101
- C. 00110 D. 01010

248. When simplified with Boolean Algebra $(x + y)(x + z)$ simplifies to
 A. X B. $x(1 + yz)$
 C. $x + x(y + z)$ D. $x + yz$
249. The gates required to build a half adder are
 A. EX - OR gate and NOR gate
 B. EX - OR gate and AND gate
 C. EX - OR gate OR gate
 D. Four NAND gates
250. The code where all successive numbers differ from their preceding number by single bit is
 A. Binary code B. Excess - 3
 C. BCD D. Gray
251. Which of the following is the faster logic
 A. TTL B. CMOS
 C. ECL D. LSI
252. If the input to T - flip flop is 100 Hz signal, the final output of the three T - flip-flop in cascade is
 A. 1000Hz B. 333Hz
 C. 500Hz D. 12.5 Hz
253. Which of the memory is volatile memory
 A. ROM B. PROM
 C. RAM D. EEPROM
254. -8 is equal to signed binary number
 A. 10001000 B. 10000000
 C. 00001000 D. 1000000
255. De-Morgan's first theorem shows the equivalence of
 A. OR gate and Exclusive OR gate
 B. NOR gate and Bubbled AND gate
 C. NOR gate and NAND gate
 D. NAND gate and NOT gate
256. The digital logic family which has the lowest propagation delay time is
 A. ECL B. CMOS
 C. TTL D. PMOS
257. The device which changes from serial data to parallel data is
 A. COUNTER
 B. DEMULTIPLEXER
 C. MULTIPLEXER
 D. FLIP-FLOP
258. A device which converts BCD to Seven Segment is called
 A. Encoder B. Multiplexer
 C. Decoder D. De-multiplexer
259. In a JK Flip-Flop, toggle means
 A. Set Q = 1 and $\bar{Q} = 0$
 B. Set Q = 0 and Q = 1
 C. Change the output to the opposite state
 D. No change in output
260. The access time of ROM using bipolar transistors is about
 A. 1 sec B. 1 μ sec
 C. 1msec D. nsec
261. The A/D converter whose conversion time is independent of the number of bits is
 A. Dual slope
 B. Parallel conversion
 C. Counter type
 D. Successive approximation
262. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero
 A. Sign-magnitude B. 2's complement
 C. 1's complement D. 9's complement
263. A hexadecimal odometer display F₅₂F. The next reading will be
 A. F₅₂F B. G₂F
 C. F₅₃F D. F₅₃O
264. Most of the digital computers do not have floating point hardware because
 A. Floating point hardware is costly
 B. It is slower than software
 C. It is not possible to perform floating point addition by hardware
 D. No specific reason
265. In digital ICs Schottky transistors are preferred over normal transistors because of their
 A. Lower Propagation delay
 B. Lower Power dissipation
 C. Higher Propagation delay
 D. Higher Power dissipation
266. The following switching functions are to be implemented using a Decoder f1 = $\sum m(1, 2, 4, 8, 10, 14)$ f2 = $\sum m(2, 5, 9, 11)$ f3 = $\sum m(2, 4, 5, 6, 7)$ The minimum configuration of the decoder should be
 A. 2 - to - 4 line B. 4 - to - 16 line
 C. 3 - to - 8 line D. 5 - to - 32 line
267. A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be
 A. 15 ns B. 45 ns
 C. 30 ns D. 60 ns
268. Words having 8-bits are to be stored into computer memory. The number of lines required for writing into memory are
 A. 1 B. 4
 C. 2 D. 8
269. In successive-approximation A/D converter, offset voltage equal to $\frac{1}{2}$ LSB is added to the D/A converter's output. This is done to
 A. Improve the speed of operation
 B. Reduce the maximum quantization error
 C. Increase the number of bits at the output
 D. Increases the range of input voltage that can be converted
270. The decimal equivalent of Binary number 11010 is
 A. 26 B. 16
 C. 36 D. 23
271. 1's complement representation of decimal number of -17 by using 8 bit representation is
 A. 1110 1110
 B. 1100 1100
 C. 1101 1101
 D. 0001 0001
272. The excess 3 code of decimal number 26 is
 A. 0100 1001 B. 1000 1001
 C. 01011001 D. 01001101
273. How many AND gates are required to realize Y = CD + EF + G
 A. 4 B. 3
 C. 5 D. 2
274. How many select lines will a 16 to 1 multiplexer will have
 A. 4 B. 5
 C. 3 D. 1
275. How many flip flops are required to construct a decade counter
 A. 10 B. 4
 C. 3 D. 2

276. Which TTL logic gate is used for wired ANDing
- Open collector output
 - Tri state output
 - Totem Pole
 - ECL gates
277. CMOS circuits consume power
- Equal to TTL
 - Twice of TTL
 - Less than TTL
 - Thrice of TTL
278. In a RAM, information can be stored
- By the user, number of times
 - By the user, only once
 - By the manufacturer, a number of times
 - By the manufacturer only once
279. The hexadecimal number for $(95.5)_{10}$ is
- $(5F.8)_{16}$
 - $(2E.F)_{16}$
 - $(9AB)_{16}$
 - $(5A.4)_{16}$
280. The octal equivalent of $(247)_{10}$ is
- $(252)_8$
 - $(367)_8$
 - $(350)_8$
 - $(400)_8$
281. The chief reason why digital computers use complemented subtraction is that it
- Simplifies the circuitry
 - is a very simple process
 - Can handle negative numbers easily
 - Avoids direct subtraction
282. In a positive logic system, logic state 1 corresponds to
- Positive voltage
 - Zero voltage level
 - Higher voltage level
 - Lower voltage level
283. The commercially available 8-input multiplexer integrated circuit in the TTL family is
- 7495
 - 74154
 - 74153
 - 74151
284. CMOS circuits are extensively used for ON-chip computers mainly because of their extremely
- Low power dissipation
 - Large packing density
 - High noise immunity
 - Low cost
285. The MSI chip 7474 is
- Dual edge triggered JK flip-flop (TTL)
 - Dual edge triggered D flip-flop (CMOS)
 - Dual edge triggered D flip-flop (TTL)
 - Dual edge triggered JK flip-flop (CMOS)
286. Which of the following memories stores the most number of bits
- A $5M \times 8$ memory
 - A $5M \times 4$ memory
 - A $1M \times 16$ memory
 - A $1M \times 12$ memory
287. The process of entering data into a ROM is called
- Burning in the ROM
 - Changing the ROM
 - Programming the ROM
 - Charging the ROM
288. When the set of input data to an even parity generator is 0111, the output will be
- 1
 - Unpredictable
 - 0
 - Depends on the previous input
289. The number 140 in octal is equivalent to
- $(96)_{10}$
 - $(90)_{10}$
 - $(86)_{10}$
 - None of these
290. The NOR gate output will be high if the two inputs are
- 00
 - 10
 - 01
 - 11
291. Which of the following is the fastest logic?
- ECL
 - CMOS
 - TTL
 - LSI
292. How many flip-flop are required to construct mod 30 counter
- 5
 - 4
 - 6
 - 8
293. How many address bits are required to represent a 32 K memory
- 10 bits
 - 14 bits
 - 12 bits
 - 16 bits
294. The number of control lines for 16 to 1 multiplexer is
- 2
 - 3
 - 4
 - 5
295. Which following requires refreshing?
- SRAM
 - ROM
 - DRAM
 - EPROM
296. Shifting a register content to left by one bit position is equivalent to
- Division by two
 - Multiplication by two
 - Addition by two
 - Subtraction by two
297. For JK flip-flop with $J = 1$, $K = 0$, the output after clock pulse will be
- 0
 - High impedance
 - 1
 - No change
298. Convert decimal 153 to octal. Equivalent in octal will be
- $(231)_8$
 - $(431)_8$
 - $(331)_8$
 - None of these
299. The decimal equivalent of $(1100)_{10}$ is
- 12
 - 18
 - 16
 - 20
300. The binary equivalent of $(FA)_{16}$ is
- $1010\ 1111$
 - 10110011
 - $1111\ 1010$
 - None of these
301. The output of SR flip-flop when $S = 1$, $R = 0$ is
- 1
 - No change
 - 0
 - High impedance
302. The number of flip-flops contained in IC 7490 is
- 2
 - 4
 - 3
 - 10
303. The number of control lines for 32 to 1 multiplexer is
- 4
 - 16
 - 5
 - 6
304. How many two-input AND & OR gates are required to realize $Y = CD + EF + G$
- 2,2
 - 33
 - 23
 - None of these
305. Which of following cannot be accessed randomly
- DRAM
 - ROM
 - SRAM
 - Magnetic tape
306. The excess-3 code of decimal 7 is represented by
- 1100
 - 1011
 - 1001
 - 1010
307. When an input signal $A = 11001$ is applied to a NOT gate serially, its output signal is
- 00111
 - 10101
 - 00110
 - 11001

- 308.** The result of adding hexadecimal number A6 to 3A is
 A. DD B. F0
 C. E0 D. EF
- 309.** A universal logic gate is one, which can be used to generate any logic function. Which of the following is a universal logic gate?
 A. OR
 B. XOR
 C. AND
 D. NAND
- 310.** The logic 0 level of a CMOS logic device is approximately
 A. 1.2 volts B. 5 volts
 C. 0.4 volts D. 0 volts
- 311.** Karnaugh map is used for the purpose of
 A. Reducing the electronic circuits used
 B. To map the given Boolean logic function
 C. To minimize the terms in a Boolean expression
 D. To maximize the terms of a given a Boolean expression
- 312.** A full adder logic circuit will have
 A. Two inputs and one output
 B. Three inputs and three outputs
 C. Two inputs and two outputs
 D. Three inputs and two outputs
- 313.** An eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. Frequency of the input signal which can be used for proper operation of the counter is approximately
 A. 1 MHz B. 2 MHz
 C. 500MHz D. 4 MHz
- 314.** The output of a JK flip-flop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions
 A. By applying J = 0, K = 0 and using a clock
 B. By applying J = 1, K = 0, and using the clock
 C. By applying J = 1, K = 1 and using the clock
 D. By applying a synchronous preset input
- 315.** The information in ROM is stored
 A. By the user any number of times
 B. By the manufacturer during fabrication of the device
 C. By the user using ultraviolet light
 D. By the user once and only once
- 316.** The conversation speed of an analog to digital converter is maximum with the following technique
 A. Dual slope AD converter
 B. Serial comparator AD converter
 C. Successive approximation AD converter
 D. Parallel comparator AD converter
- 317.** A weighted resistor digital to analog converter using N bits required a total of
 A. N precision resistors
 B. N + 1 precision resistors
 C. 2N precision resistors
 D. N - 1 precision resistors
- 318.** The 2's complement of the number 1101110 is
 A. 0010001 B. 0010010
 C. 0010001 D. None
- 319.** The decimal equivalent of Binary number 10101 is
 A. 21 B. 26
 C. 31 D. 28
- 320.** How many two input AND gates and two input OR gates are required to realize $Y = BD + CE + AB$
 A. 1,1 B. 3,2
 C. 4,2 D. 2,3
- 321.** How many select lines will a 32:1 multiplexer will have
 A. 5 B. 9
 C. 8 D. 11
- 322.** How many address bits are required to represent 4K memory
 A. 5 bits B. 8 bits
 C. 12 bits D. 10 bits
- 323.** For JK flip-flop J = 0, K = 1, the output after clock pulse will be
 A. 1
 B. 0
 C. No change
 D. High impedance
- 324.** Which of following are known as universal gates
 A. NAND and NOR
 B. XOR and OR
 C. AND and OR
 D. None
- 325.** Which of the following memories stores the most number of bits
 A. 64Kx8 memory
 B. 32Mx8 memory
 C. 1Mx8 memory
 D. 64x6 memory
- 326.** Which of following consume minimum power
 A. TTL B. DTL
 C. CMOS D. RTL
- 327.** The complement of a variable is always
 A. 0
 B. Equal to the variable
 C. 1
 D. The inverse of the variable
- 328.** The Boolean expression $A+B+C$ is
 A. A sum term
 B. A product term
 C. A literal term
 D. A complement term
- 329.** The Boolean expression $AB'CD'$ is...
 A. A sum term B. A literal
 C. A product term D. Always 1
- 330.** The domain of the expression $AB'CD + AB' + C'D + B$ is...
 A. A and D
 B. A, B, C and D
 C. B only
 D. None of the above
- 331.** According to commutative law of addition
 A. $AB = BA$
 B. $A + (B+C) = (A+B) + C$
 C. $A = A+A$
 D. $A+B = B+A$
- 332.** According to the associative law of multiplication
 A. $B = BB$ B. $A+B = B+A$
 C. $A(BC) = (AB)C$ D. $B + B(B = 0)$
- 333.** According to the distributive law:
 A. $A(B+C) = AB+AC$
 B. $A(A+1) = A$
 C. $A(BC) = (AB) = ABC$
 D. $A + AB = A$
- 334.** Which one of the following is not a valid rule of Boolean algebra?
 A. $A + 1 = 1$ B. $AA = A$
 C. $A = \bar{A}$ D. $A + 0 = A$

335. Which of the following rules states that if one input of an AND gate is always 1, the output is equal to the other input?

- A. $A + 1 = 1$
- B. $A \cdot A = A$
- C. $A + A = A$
- D. $A \cdot 1 = A$

336. According to De-Morgan's theorems, the following equality(s) are correct:

- A. $\overline{AB} = \bar{A} + \bar{B}$
- B. $\overline{A + B + C} = \overline{ABC}$
- C. $\overline{XYZ} = \bar{X} + \bar{Y} + \bar{Z}$
- D. All of the other

337. The Boolean expression $X = AB + CD$ represents

- A. Two ORs ANDed together
- B. Two ANDs ORed together
- C. A 4-input AND gate
- D. An exclusive-OR

338. An example of a sum-of-products expression is

- A. $A + BC + CD$
- B. $\bar{A}B + A\bar{C} + A\bar{B}\bar{C}$
- C. $\bar{A} + \bar{B} + C$ ($A + \bar{B} + C$)
- D. Both answers-OR

339. An example of a sum-of-sums expression is

- A. $A(B + C) + A\bar{C}$
- B. $\bar{A} + \bar{B} + BC$
- C. $(A + B)(\bar{A} + B + \bar{C})$
- D. Both answers A and B

340. An example of a standard SOP expression is

- A. $\bar{A}B + A\bar{B}C + AB\bar{D}$
- B. $A\bar{B} + \bar{A}\bar{B} + AB$
- C. $A\bar{B}C + A\bar{C}D$
- D. $A\bar{B}\bar{C}D + \bar{A}B + \bar{A}$

341. A 3-variable Karnaugh map has

- A. Eight cells
- B. Sixteen cells
- C. Three cells
- D. Four cells

342. In a 4-variable Karnaugh map, a variable product term is produced by

- A. A 2-cell group of 1s
- B. A 4-cell group of 1s
- C. An 8-cell group of 1s
- D. A 4-cell group of 0s

343. On a karnaugh map, a grouping the 0s produces

- A. A product-of-sums expression
- B. A "don't care" condition
- C. A sum-of-products expression
- D. AND-OR logic

344. A 5-variable Karnaugh map has

- A. Sixteen cells
- B. Sixty-four cells
- C. Thirty-two cells
- D. All of the above

345. The output expression for an AND-OR circuit having one AND gate with inputs A, B, C and D and one AND gate with inputs E and F is

- A. ABCDEF
- B. $(A + B + C + D)(E + F)$
- C. $A + B + C + D + E + F$
- D. $BCD + EF$

346. A logic circuit with an output $X = ABC + A\bar{C}$ consists of

- A. Two AND gates and one OR gate
- B. Two AND gates, one OR gate, and two inverters
- C. Two OR gates, one AND gate, and two inverter
- D. Two AND gates, one OR gate, and one inverter

347. To implement the expression $\bar{A}BCD + A\bar{B}CD + A\bar{B}\bar{C}\bar{D}$, it takes one OR gate and

- A. One AND gate
- B. Three AND gates and four inverters
- C. Three AND gates
- D. Three AND gates and three inverters

348. The expression $\bar{A}BCD + ABC\bar{D} + A\bar{B}\bar{C}\bar{D}$

- A. Cannot be simplified
- B. Can be simplified to $ABC\bar{D} + A\bar{B}\bar{C}$
- C. Can be simplified to $\bar{A}BC + A\bar{B}$
- D. None of these answers is correct

349. The input expression for an AND-OR-Invert circuit having one AND gate with inputs, A, B, C and D and one AND gate with inputs E and F is

- A. $ABCD + EF$
- B. $\bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E} + \bar{F}$
- C. $(A + B + C + D)(E + F)$
- D. $(\bar{A} + \bar{B} + \bar{C} + \bar{D})(\bar{E} + \bar{F})$

350. An exclusive-OR function is expressed as

- A. $\bar{A}B + AB$
- B. $(\bar{A} + B)(A + \bar{B})$
- C. $\bar{A}\bar{B} + A\bar{B}$
- D. $(\bar{A} + \bar{B}) + (A + B)$

351. The AND operation can be produced with

- A. Two AND gates
- B. One NOR gates
- C. Three NAND gates
- D. Three NOR gates

352. The OR operation can be produced with

- A. Two NOR gates
- B. Four NAND gates
- C. Three NAND gates
- D. Both answers A and B

353. When using dual symbols in a logic diagram,

- A. Bubble outputs are connected to bubble inputs
- B. The NAND symbol produce the NAND operations
- C. The negative-OR symbol produce the OR operation
- D. All of these answers are true

354. All Boolean expressions can be implemented with

- A. NAND gates only
- B. NOR gates only
- C. Combinations of NAND and NOR gates
- D. Any of these

355. The device used to convert a binary number to a 7-segment display format is

- A. Multiplexer
- B. Decoder
- C. Encoder
- D. Register

356. An example of data storage device is

- A. Two inputs and two outputs
- B. Two inputs and three outputs
- C. Three inputs and two outputs
- D. Two inputs and one output

357. Full-adder is characterized by

- A. Two inputs and two outputs
- B. Two inputs and three outputs
- C. Three inputs and two outputs
- D. Two inputs and one output

358. The inputs to a full-adder are $A = 1$, $B = 1$, $C_{in} = 0$. The outputs are

- A. $\Sigma = 1$, $C_{out} = 1$
- B. $\Sigma = 0$, $C_{out} = 1$
- C. $\Sigma = 1$, $C_{out} = 0$
- D. $\Sigma = 0$, $C_{out} = 0$

359. A 4-bit parallel adder can add

- A. Two 4-bit binary numbers
- B. Four bits at a time
- C. Two 2-bit binary number
- D. Four bits in sequence

360. The 74LS83A is an example of a 4-bit parallel adder, to expand this device to an 8-bit adder, you must
- Use four adders with no interconnections
 - Use two adders and connect the sum outputs of one to the bit inputs of the other
 - Use eight adders with no interconnections
 - Use two adders with the carry output of one connected to the carry input of the other
361. If a 74HC85 magnitude comparator has $A = 1011$ and $B = 1001$ on its inputs, the outputs are
- $A > B = 0$, $A < B = 1$, $A = B = 0$
 - $A > B = 1$, $A < B = A$, $A = B = 0$
 - $A > B = 1$, $A < B = 0$, $A = B = 0$
 - $A > B = 0$, $A < B = 0$, $A = B = A$
362. If a 1-of-16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output, what are the inputs?
- $A_3A_2A_1A_0 = 1010$
 - $A_3A_2A_1A_0 = 1100$
 - $A_3A_2A_1A_0 = 1110$
 - $A_3A_2A_1A_0 = 0100$
363. A BCD-to-7 segment decoder has 0100 on its inputs. The active outputs are
- a, c, f, g
 - b, c, e, f
 - b, c, f, g
 - b, d, e, g
364. If an octal-to-binary priority encoder has its 0, 2, 5, and 6 inputs at the active level, the active-HIGH binary output is
- 110
 - 10
 - 010
 - 000
365. In general, a multiplexer has
- One data input, several data outputs, and selection inputs
 - One data input, one data output, and one selection input
 - Several data inputs, several data outputs, and selection inputs
 - Several data inputs, one data output and selection inputs
366. Data selectors are basically the same as
- Decoders
 - Multiplexers
 - De-multiplexers
 - Encoders
367. Which of the following codes exhibit even parity?
- 10011000
 - 11111111
 - 01111000
 - Both answer (A) and (B)
368. If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be
- Set
 - Invalid
 - Reset
 - Clear
369. The invalid state of an S-R latch occurs when
- $S = 1, R = 0$
 - $S = 1, R = 1$
 - $S = 0, R = 1$
 - $S = 0, R = 0$
370. For a gated D latch, the Q output always equals the D input
- Before the enable pulse
 - Immediately after the enable pulse
 - During the enable pulse
 - Answers (B) and (C)
371. Like the latch, the flip-flop belongs to a category of logic circuits known as
- Monostable multivibrators
 - Astable multivibrators
 - Bistable multivibrators
 - One-shot
372. The purpose of the clock input to a flip-flop is to
- Clear the device
 - Set the device
 - Always cause the output to change state
 - Cause the output to assume a state dependent on the controlling (S-R, J-K or D) inputs
373. For an edge-triggered D flip-flop,
- A change in the state of the flip-flop can occur only at a clock pulse edge
 - The state that the flip-flop goes to depends on the D input
 - The output follows the input at each clock pulse
 - All of these answers
374. A feature that distinguishes the J-K flip-flop from the S-R flip-flop is the
- Toggle condition
 - Type of clock
 - Preset input
 - Clear input
375. A flip-flop is in the toggle condition when
- $J = 1, K = 0$
 - $J = 0, K = 0C$
 - $J = 1, K = 1$
 - $J = 0, K = 1$
376. A J-K flip-flop with $J = 1$ and $K = 1$ has a 10 kHz clock input. The Q output is
- Constantly HIGH
 - A 10 kHz square wave
 - Constantly LOW
 - A 5 kHz square wave
377. Asynchronous counters are known as
- Ripple counters
 - Decade counters
 - Multiple clock counters
 - Modulus counters
378. An asynchronous counter differs from a synchronous counter in
- The number of states in its sequence
 - The type of flip-flop used
 - The method of clocking
 - The value of the modulus
379. The modulus of a counter is
- The number of flip-flops
 - The actual number of times it recycles in a second
 - The number of times it recycles in a second
 - The maximum possible number of states
380. A 3-bit binary counter has a maximum modulus of
- 3
 - 8
 - 6
 - 16
381. A 4-bit binary counter has a maximum modulus of
- 16
 - 8
 - 32
 - 4
382. A modulus-12 counter must have
- 12 flip-flop
 - 4 flip-flop
 - 3 flip-flop
 - Synchronous clocking
383. Which one of the following is an example of counter with a truncated modulus?
- Modulus 8
 - Modulus 16
 - Modulus 14
 - Modulus 32
384. A 4-bit ripple counter consists of flip-flop that each have propagation delay from clock to Q output of 12 ns. For the counter to recycle form 1111 to 0000, it takes a total of
- 12ns
 - 48ns
 - 24ns
 - 36ns

385. A BCD counter is an example of

- A. A full-modulus counters
- B. A truncated-modulus
- C. A decade counter
- D. Answers (A) and (C)

386. Which of the following is an invalid state in an 8421 BCD counter?

- A. 1100
- B. 0101
- C. 0010
- D. 1000

387. Three cascaded modulus-10 counters have an overall modulus of

- A. 30
- B. 1000
- C. 100
- D. 10,000

388. A 10 MHz clock frequency is applied to a cascaded counter consisting of a modulus-5 counter, a modulus-8 counter, and two modulus-10 counters. The lowest output frequency possible is

- A. 10 kHz
- B. 5 kHz
- C. 2.5 kHz
- D. 25 kHz

389. A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is

- A. 0001
- B. 1000
- C. 1111
- D. 1110

390. The terminal count of a modulus-13 binary counter is

- A. 0000
- B. 1101
- C. 1111
- D. 1100

391. A stage in a shift register consists of

- A. A latch
- B. A byte of storage
- C. A flip-flop
- D. Four bits of storage

392. To serially shift a byte of data into a shift register, there must be

- A. One clock pulse
- B. One load pulse
- C. Eight clock pulses
- D. One clock pulse for each 1 in the data

393. To parallel load a byte of data into a shift register with a synchronous load, there must be

- A. One clock pulse
- B. One clock pulse for each 1 in the data
- C. Eight clock pulses
- D. One clock pulse for each 1 in the data

394. The group of bits 101101101 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state of 11100100. After two clock pulse, the register contains.

- A. 01011110
- B. 1111001
- C. 10110101
- D. 00101101

395. With a 1 MHz clock frequency, eight bits can be serially entered into a shift register in

- A. 80 μ s
- B. 80 ms
- C. 8 μ s
- D. 10 μ s

396. With a 1 MHz clock frequency, eight bits can be parallel entered into a shift register

- A. In 80 μ s
- B. In the propagation delay time of eight flip-flops
- C. In 1 μ s
- D. In the propagation delay time of one flip-flop

397. A modulus-10 Johnson counter requires

- A. Ten flip-flop
- B. Five flip-flop
- C. Four flip-flop
- D. Twelve flip-flop

398. A modulus-10 ring counter requires a minimum of

- A. Ten flip-flops
- B. Four flip-flops
- C. Five flip-flops
- D. Twelve flip-flop

399. When an 8-bit serial in/serial out shift register is used for a 24 μ s time delay, the clock frequency must be

- A. 41.67 kHz
- B. 125 kHz
- C. 333 kHz
- D. 8 MHz

400. The bit capacity of a memory that has 1024 addresses and can store 8 bits at each address is

- A. 1024
- B. 8
- C. 8192
- D. 4096

401. A 32-bit data word consists of

- A. 2 byte
- B. 4 bytes
- C. 4 nibbles
- D. 3 bytes and 1 nibbles

402. Data are stored in a random-access memory (RAM) during the

- A. Read operation
- B. Write operation
- C. Enable operation
- D. Addressing operation

403. Data that are stored at a given address in a random-access memory (RAM) is lost when

- A. Power goes off
- B. New data are written at the address
- C. The data are read from the address
- D. Answer (A) and (B)

404. A ROM is a

- A. Nonvolatile memory
- B. Read/write memory
- C. Volatile memory
- D. Byte-organized memory

405. A memory with 256 addresses has

- A. 256 address lines
- B. 4 address lines
- C. 8 address lines
- D. 8 address lines

406. A byte-organized memory has

- A. 1 data output
- B. 8 data output
- C. 4 data output
- D. 16 data output

407. The storage cell in a SRAM is

- A. A flip-flop
- B. A fuse
- C. A capacitor
- D. A magnetic domain

408. A DRAM must be

- A. Replaced periodically
- C. Refreshed periodically
- B. Always enabled
- D. Programmed before each use

409. A flash memory is

- A. Nonvolatile
- B. A read/write memory
- C. A read-only memory
- D. Answers (A) and (B)

410. Hard disk, floppy disk, Zip disk, and Jaz disk are all

- A. Magneto-optical storage devices
- B. Magnetic storage devices
- C. Semiconductor storage devices
- D. Optical storage devices

411. Optical storage devices employ

- A. Ultraviolet light
- B. Optical couplers
- C. Electromagnetic field
- D. Lasers

412. A fixed-function IC package containing four AND gates is an example of

- A. MSI
- B. SOIC
- C. SMT
- D. SSI

- 413.** An LSI device has a circuit complexity of
 A. 12 to 99 equivalent gates
 B. 2000 to 5000 equivalent gates
 C. 100 to 9999 equivalent gates
 D. 10,000 to 99,999 equivalent gates
- 414.** A positive-going pulse is applied to an inverter. The time interval from the leading edge of the input to the leading edge of the output is 7 ns. This parameter is
 A. Speed-power product
 B. Propagation delay t_{PLH}
 C. Propagation delay, t_{PLH}
 D. Pulse width
- 415.** The CMOS family with the fastest switching speed is
 A. AC B. ACT
 C. HC D. ALVC
- 416.** If power were the major criterion in the design of a digital system, the logic family that you would probably use is
 A. HCL B. LV
 C. ALVC D. LVC
- 417.** When the frequency of the input signal to a CMOS gate is increased, the average power dissipation
 A. Decreases
 B. Does not change
 C. Increases
 D. Decreases exponentially
- 418.** CMOS operates more reliably than TTL in a high-noise environment because of its
 A. Lower noise margin
 B. Higher noise margin
 C. Input capacitance
 D. Smaller power dissipation
- 419.** Proper handling of a CMOS device is necessary because of its
 A. Fragile construction
 B. High-noise immunity
 C. Susceptibility to electrostatic discharge
 D. Low power dissipation
- 420.** Which of the following is not a TTL circuit?
 A. 74F00 B. 74HC00
 C. 74AS00 D. 74ALS00
- 421.** An open TTL NOR gate input
 A. Acts as a LOW
 B. Should be grounded
 C. Acts as a HIGH
 D. Answers (B) and (C)
- 422.** An LS TTL gate can drive a maximum of
 A. 20 unit loads
 B. 40 unit loads
 C. 10 unit loads
 D. Unlimited unit loads
- 423.** If two unused inputs of a LS TTL gate are connected to an input being driven by another LS TTL gate, the total number of remaining unit loads that can be driven by this gate is
 A. Seven B. Seventeen
 C. Eight D. Unlimited
- 424.** The main advantage of ECL over TTL or CMOS is
 A. ECL is less expensive
 B. ECL consumes less power
 C. ECL is available in a greater variety of circuit type
 D. ECL is faster
- 425.** ECL cannot be used in
 A. High-noise environments
 B. High-frequency applications
 C. Damp environments
 D. ECL is less expensive
- 426.** The basic mechanism for storing a data bit in an E²CMOS cell is
 A. Control gate B. Floating gate
 C. Floating drain D. Cell current
- 427.** A CPLD is a
 A. CMOS programmable logic device
 B. Capacitive programmable logic device
 C. Complex programmable logic device
 D. Complementary process latching device
- 428.** VHDL is a
 A. Logic device
 B. Computer language
 C. PLD programming language
 D. Very high density logic
- 429.** The types of SPLDs do not include
 A. GAL B. RAM
 C. PROM D. PAL
- 430.** A GAL has
 A. A reprogrammable AND array, a fixed OR array, and programmable output logic
 B. A fixed AND array and a programmable OR array
 C. One-time programmable AND and OR array
 D. Reprogrammable AND and OR array
- 431.** An SPLD that has a programmable AND array and a fixed OR array is a
 A. PROM B. PAL
 C. PLA D. GAL
- 432.** A connection between a row and column in a PAL array is made by
 A. Blowing a fusible link
 B. Leaving a fusible link intact
 C. Connecting an input variable to the input line
 D. Connecting an input variable to the product term line
- 433.** The device number PAL14H indicates
 A. A PAL with fourteen active-HIGH outputs and four inputs
 B. A PAL that implements fourteen AND gates and four OR gates
 C. A PAL with implements and four active-HIGH outputs
 D. Who the manufacturer is
- 434.** A GAL is different from a PAL because
 A. A GAL has more inputs and outputs
 B. A GAL is implemented with a different technology
 C. A GAL can replace several different PALs
 D. All except answer (A)
- 435.** The reprogrammable cells in a GAL array are
 A. TTL B. ECL
 C. E²CMOS D. Bipolar fuses
- 436.** OLMC is an acronym for
 A. Output Logic Main Cell
 B. Output Logic Macrocell
 C. Optimum Logic Multiple Channel
 D. Odd-parity Logic Master Check
- 437.** Two ways in which a GAL output can be configured are
 A. Combinational and I/O
 B. Fixed and variable
 C. Simple and complex
 D. Combinational and registered
- 438.** The device number GAL22V10 means that
 A. The device has 22 dedicated inputs and 10 dedicated outputs
 B. The device has 22 inputs including dedicated inputs and I/Os and 10 outputs either dedicated or I/Os
 C. The device has a variable number of inputs form a maximum of 22 to a minimum of 10
 D. The device has 24 inputs including dedicated inputs and I/Os and 14 outputs either dedicated or I/Os

- 439. To conventionally program an SPLD, you need a**
- Special fixture
 - Special fixture and a master PLD that has been preprogrammed at the factory
 - Computer, a programmer, and HDL software
 - Computer, a programmer, and BASIC software
- 440. ISP stands for**
- In-System Programmable
 - Integrated Silicon Program
 - Integrated System Program
 - In-System Integrated Programming
- 441. The GAL22V10 has**
- 10 inputs and 22 outputs
 - 22 dedicated inputs and 10 outputs
 - 12 dedicated inputs and 10 dedicated outputs
 - 12 dedicated inputs and 10 outputs, any of which can be an input
- 442. The GAL22V10 operates on a dc supply voltage of**
- 5V
 - 3.3V
 - 10V
 - 1.2V
- 443. OLMC stand for**
- Output logic modular circuit
 - Output logic macrocell
 - Output latch memory cell
 - Overall logic matrix circuit
- 444. The three states of a tri-state output buffer are**
- HIGH, LOW, high impedance
 - HIGH, LOW, ground
 - HIGH, LOW, in between
 - Right, left, centre
- 445. The OLMC of the GAL22V10 contains**
- One OR gate, one flip-flop, two multiplexers
 - One OR gate, one flip-flop, one multiplexer
 - One AND gate, one latch, two multiplexers
 - One OR gate, one flip-flop, two decoders
- 446. The GAL16V8 has**
- 16 dedicated inputs and 8 outputs
 - 8 dedicated inputs and 8 inputs /outputs
 - 8 inputs and 16 outputs
 - 16 input/outputs and 8 outputs
- 447. A typical OLMC consists of**
- Gates, multiplexers, and a flip-flop
 - Gates, and a shift register
 - A Gray code counter
 - A fixed logic array
- 448. A CPLD is a**
- CMOS PLD
 - Complementary PLD
 - Complex PLD
 - A fixed logic array
- 449. A CPLD contains**
- Shift registers
 - Logic arrays
 - Programmable interconnections
 - Answers (B) and (C)
- 450. FPGA stands for**
- Fast propagation gate array
 - Field programmable gate array
 - Field presentable gate application
 - File programmable gate array
- 451. $2 \times 10^1 + 8 \times 10^0$ equal to**
- 10
 - 2.8
 - 280
 - 28
- 452. The binary number 1101 is equal to the decimal number**
- 13
 - 49
 - 121
 - 221
 - 11
 - 3
 - 441
 - 256
- 453. The binary number 11011101 is equal to the decimal number**
- 19
 - 41
 - 121
 - 221
 - 11
 - 3
 - 441
 - 256
- 454. The decimal number 17 is equal to the binary number**
- 10010
 - 11000
 - 11000
 - 10001
 - 10001
 - 10001
 - 10001
 - 10001
- 455. The decimal number 175 is equal to the binary number**
- 1100111
 - 1010111
 - 1010111
 - 1101111
 - 1101111
 - 1101111
 - 1101111
 - 1101111
- 456. The sum of 11010 + 01111 equals**
- 101001
 - 101010
 - 101010
 - 101000
 - 101001
 - 101010
 - 101000
 - 101000
- 457. The difference of 110 - 010 equals**
- 001
 - 010
 - 001
 - 010
 - 101
 - 100
 - 101
 - 100
- 458. The 1's complement of 10111001 is**
- 01000111
 - 01000110
 - 01000110
 - 11000110
 - 11000110
 - 11000110
 - 11000110
 - 11000110
- 459. The 2's complement of 11001000 is**
- 00110111
 - 00110001
 - 00110001
 - 01010100
 - 01010100
 - 01010100
 - 01010100
 - 01010100
- 460. The decimal number -34 is expressed in the 2's complement form as**
- 01011110
 - 11011110
 - 10100010
 - 01011110
 - 01011110
 - 01011110
 - 01011110
 - 01011110
- 461. The decimal number +122 is expressed in the 2's complement form as**
- 01111010
 - 11111010
 - 01111010
 - 01000101
 - 01000101
 - 01000101
 - 01000101
 - 01000101
- 462. A single-precision floating-point binary number has a total of**
- 8 bits
 - 16 bits
 - 24 bits
 - 32 bits
 - 11
 - 3
 - 441
 - 256
- 463. In the 2's complement form, the binary number 10010011 is equal to the decimal number**
- 19
 - +109
 - +109
 - 109
 - 19
 - +91
 - +109
 - 109
- 464. The binary number 10110011100101010001 can be written in hexadecimal as**
- 5471238₈
 - 5471241₈
 - 2634521₈
 - 23162501₈
 - 100011100101010001
 - 100011100101010001
 - 100011100101010001
 - 100011100101010001
- 465. The binary number 10001101010001101111 can be written in hexadecimal as**
- AD46₁₆
 - 8C46F₁₆
 - 8D46F₁₆
 - AE46F₁₆
 - 11101110101001
 - 111111010110001
 - 111011110101001
 - 111011110101001
- 466. The binary number for F7A9₁₆ is**
- 111101110101001
 - 111111010110001
 - 111011110101001
 - 111011110101001
 - 1111011010101001
 - 1111011010101001
 - 1111011010101001
 - 1111011010101001
- 467. The BCD number for decimal 473 is**
- 111011010
 - 01000110011
 - 110001110011
 - 010001110011
 - 110001110011
 - 010001110011
 - 110001110011
 - 010001110011
- 468. Refer to Table 2-7. The word STOP in ASCII is**
- 10100110101001001111010000
 - 1001010110101100111010001
 - 1010010100110010011101010000
 - 1010011101010010011101100100
 - 0101011101010010011101010000
 - 0101011101010010011101010000
 - 0101011101010010011101010000
 - 0101011101010010011101010000
- 469. The number of parity bits to be added to an 8-bit word for constructing Hamming code for detection**
- 1
 - 2
 - 3
 - 4
 - 1
 - 3
 - 2
 - 4

470. A 7-bit Hamming code (even parity) 001001 for a BCD digit is known to have single error the encoded BCD digit is

- A. 9
- B. 3
- C. 5
- D. 0

471. When the input to an inverter is HIGH (1), the output is

- A. HIGH or 1
- B. HIGH or 0
- C. LOW or 1
- D. LOW or 0

472. An inverter performs an operation known as

- A. Complementation
- B. Inversion
- C. Assertion
- D. Both answers (A) and (B)

473. The output of an AND gate with inputs A, B, and C is a 1 (HIGH) when

- A. A = 1, B = 1, C = 1
- C. A = 1, B = 0, C = 1
- B. A = 0, B = 0, C = 0
- D. Only answers (A) and (C)

474. A pulse is applied to each input of a 2-input NAND gate. One pulse goes HIGH at t = 0 and goes back LOW at t = 1ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3ms. The output pulse can be described as follows:

- A. It goes LOW at t = 0 and back HIGH at t = 3ms
- B. It goes LOW at t = 0.8 ms and back HIGH at t = 3 ms
- C. It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms
- D. It goes LOW at t = 0.8 ms and back LOW at t = 1 ms

475. A pulse is applied to each input of a 2-input NOR gate, one pulse goes HIGH at t = 0 and goes back LOW at t = 1ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:

- A. It goes LOW at t = 0 and back HIGH at t = 3 ms.
- B. It goes LOW at t = 0.8 ms and back HIGH at t = 3ms
- C. It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms
- D. It goes HIGH at t = 0.8 ms and back LOW at t = 1 ms

476. A pulse is applied to each input of an exclusive-OR gate. One pulse goes HIGH at t = 0 and goes back LOW at t = 1 ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:

- A. It goes HIGH at t = 0 and back LOW at t = 3 ms
- B. It goes HIGH at t = 0 and back LOW at t = 0.8ms
- C. It goes HIGH at t = 1 ms and back LOW at t = 3ms
- D. Both answers (B) and (C)

477. For an AND gate

- A. All LOW input produce a HIGH output
- B. Output is HIGH if and only if all inputs are HIGH
- C. Output is LOW if and only if all inputs are HIGH
- D. Output is LOW if and only if all inputs are LOW

478. The output of a gate is LOW when atleast one of its inputs is HIGH. This is true for

- A. AND
- B. OR
- C. NAND
- D. NOR

479. The output of a gate is LOW when atleast one of its inputs is LOW. It is true for

- A. AND
- B. NAND
- C. OR
- D. NOR

480. The output of a gate is HIGH when atleast one of its inputs is LOW. It is true for

- A. XOR
- B. NOR
- C. NAND
- D. OR

481. The output of a gate is HIGH when atleast one of its inputs is HIGH. It is true for

- A. NAND
- B. OR
- C. AND
- D. XOR

482. The output of a gate is HIGH if and only if all its inputs are HIGH. It is true for

- A. XOR
- B. OR
- C. AND
- D. NAND

483. The output of a gate is LOW if and only if all its inputs are HIGH. It is true for

- A. AND
- B. NOR
- C. XNOR
- D. NAND

484. The output of a gate is HIGH if and only if all its inputs are LOW. It is true for

- A. NOR
- B. NAND
- C. XOR
- D. XNOR

485. The output of a gate is LOW if and only if all its inputs are LOW. It is true for

- A. XOR
- B. OR
- C. AND
- D. NOR

486. The output of a 2-input gates is 1 if and only if its inputs are unequal. It is true for

- A. OR
- B. XNOR
- C. XOR
- D. NOR

487. The output of a 2-input gates is 0 if and only if its inputs are unequal. It is true for

- A. XNOR
- B. NOR
- C. AND
- D. NAND

488. The output of a 2-input gates is 1 if and only if its inputs are equal. It is true for

- A. AND
- B. OR
- C. XOR
- D. XNOR

489. The output of a 2-input gates is 0 if and only if its inputs are unequal. It is true for

- A. AND
- B. OR
- C. XOR
- D. NOR

490. The most suitable gate for comparing two bits is

- A. AND
- B. NAND
- C. OR
- D. XOR

491. Which of the following gates can be used as an inverter?

- A. AND
- B. XOR
- C. OR
- D. None of the above

492. Which of the following gates cannot be used as an inverter?

- A. NAND
- B. NOR
- C. AND
- D. XNOR

493. The maximum number of 3-inputs gates in a 16-pin IC will be

- A. 2
- B. 4
- C. 3
- D. 5

494. A quality having continuous values is

- A. A digital quantity
- B. A binary quantity
- C. An analog quantity
- D. A natural quantity

495. The term bit means

- A. A small amount of data
- B. Binary digit
- C. A 1 or a 0
- D. Both answers (B) and (C)

496. The time interval on the leading edge of a pulse between 10% and 90% of the amplitude is the

- A. Rise time
- B. Pulse width
- C. Fall time
- D. Period

497. A pulse in a certain waveform occurs every 10 ms. The frequency is

- A. 1 kHz
- B. 100Hz
- C. 1 Hz
- D. 10 Hz

498. In a certain digital waveform, the period is twice the pulse width. The duty cycle is

- A. 100%
- B. 50%
- C. 200%
- D. 150%

499. An inverter

- A. Performs the NOT operation
- B. Changes a LOW to a HIGH
- C. Changes a HIGH to a LOW
- D. Does all of the above

500. The output of an AND gate is HIGH when

- A. Any input is HIGH
- B. No inputs are HIGH
- C. All inputs are HIGH
- D. Both answers (A) and (C)

501. The output of an OR gate is HIGH when

- A. Any input is HIGH
- B. No inputs are HIGH
- C. All inputs are HIGH
- D. Both answers (A) and (C)

502. How many 3 lines to 8 line decoder are required for a 1 of 32 decoder?

- A. 1
- B. 4
- C. 8
- D. 16

503. Convert BCD 0001 0010 0110 to binary

- A. 1111110
- B. 111101
- C. 1111000
- D. 1111111

504. How many data select lines are required for selecting eight inputs?

- A. 1
- B. 2
- C. 3
- D. 4

505. How many 1-of-16 decoders are required for decoding a 7 bit binary number?

- A. 5
- B. 6
- C. 7
- D. 8

506. The implementation of simplified sum-of-products expressions may be easily implemented into actual logic circuits using all universal gates with little or no increase in circuit complexity.

- A. AND/OR
- B. NAND
- C. NOR
- D. OR/AND

507. Which of the following combinations cannot be combined into k-map groups?

- A. Corners in the same row
- B. Corners in the same column
- C. Diagonal corners
- D. Overlapping combinations

508. Which gate is best used as a basic comparator?

- A. NOR
- B. OR
- C. XOR
- D. AND

509. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

- A. A > B = 1, A < B = 0, A <= B = 1
- B. A > B = 0, A < B = 1, A = B = 0
- C. A > B = 1, A < B = 0, A = B = 0
- D. A > B = 1, A < B = 0, A = B = 1

510. A logic probe is placed on each of the input terminals, but the output indication does not change. What is wrong?

- A. The output of the gate appears to be open
- B. The dim indication on the logic probe indicates that the supply voltage is probably low
- C. The dim indication is a result of a bad ground connection on the logic probe
- D. The gate may be a tri state logic.

511. Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output?

- A. $\Sigma_1 \Sigma_2 \Sigma_3 \Sigma_4 = 0111$, $C_{out} = 0$
- B. $\Sigma_1 \Sigma_2 \Sigma_3 \Sigma_4 = 1111$, $C_{out} = 1$
- C. $\Sigma_1 \Sigma_2 \Sigma_3 \Sigma_4 = 1011$, $C_{out} = 1$
- D. $\Sigma_1 \Sigma_2 \Sigma_3 \Sigma_4 = 1100$, $C_{out} = 1$

512. Each "1" entry in a K-map square represents:

- A. A HIGH for each input truth table condition that produces a HIGH output.
- B. A HIGH output on the truth table for all LOW input combinations.
- C. A LOW output for all possible HIGH input conditions.
- D. A DON'T CARE condition for all possible input truth table combinations.

513. Looping on a k-map always results in the elimination of:

- A. Variables within the loop that appear only in their complemented form
- B. Variables that remain unchanged within the loop
- C. Variables within the loop that appear in both complemented and uncomplemented form
- D. Variables within a loop that appear only in their uncomplemented form

514. The carry output of a half-adder circuit can be expressed as.....

- A. $C_{out} = AB$
- B. $C_{out} = A + B$
- C. $C_{out} = A \oplus B$
- D. None of the above

515. What is the major difference between half-adders and full-adders?

- A. Nothing basically; full-adders are made up of two half-adders.
- B. Full adders can handle double-digit numbers.
- C. Full adders have a carry input capability.
- D. Half adders can handle only single-digit numbers.

516. Manipulation of individual bits of a word is often referred to as

- A. Bit twiddling
- B. Bit swapping
- C. Micro operation
- D. None of the above

517. The ASCII code for letter A is

- A. 1100011
- B. 100000
- C. 1111111
- D. 0010011

518. Which gate can be used as anti-coincidence detector?

- A. X-NOR
- B. NAND
- C. X-OR
- D. NOR

519. Which of the following is a self-complementing code?
 A. 8421 code B. 5211 code
 C. Gray code D. Binary code
520. Excess 3 code is also known as:
 A. Weighted code
 B. Self-complementing code
 C. Cyclic redundancy code
 D. Algebraic code
521. Binary equivalent of gray code number 101 is
 A. 101 B. 110
 C. 100 D. 111
522. Which of the following expression is in the product-of-sums form?
 A. $(A + B)(C + D)$ B. $(AB)(CD)$
 C. $AB(CD)$ D. $B + CD$
523. Which of the following expressions is in the sum-of-products form?
 A. $(A + B)(C + D)$ B. $(AB)(CD)$
 C. $AB(CD)$ D. $AB + CD$
524. Which statement below best describes a Karnaugh map?
 A. A Karnaugh map can be used to replace Boolean rules.
 B. The Karnaugh map eliminates the need for using NAND and NOR gates.
 C. Variable complements can be eliminated by using Karnaugh maps.
 D. Karnaugh maps provide a visual approach to simplifying Boolean expressions.
525. A decoder can be used as a demultiplexer by
 A. tying all enable pins LOW
 B. tying all data-select lines LOW
 C. tying all data-select lines HIGH
 D. using the input lines for data selection and an enable line for data input

526. How many 4-bit parallel adders would be required to add two binary numbers each representing decimal numbers up through 300_{10} ?
 A. 1 B. 2
 C. 3 D. 4
527. A certain BCD-to-decimal decoder has active-HIGH inputs and active LOW outputs. Which output goes LOW when the inputs are 1001?
 A. 0
 B. 3
 C. 9
 D. None of the above
528. A full-adder has a $Cin = 0$. What are the sum (Σ) and the carry ($Cout$) when $A = 1$ and $B = 1$?
 A. $\Sigma = 0, C_{out} = 0$ B. $\Sigma = 0, C_{out} = 1$
 C. $\Sigma = 1, C_{out} = 0$ D. $\Sigma = 1, C_{out} = 1$
529. Which of the following gates is a series circuit gate?
 A. AND GATE
 B. OR GATE
 C. XOR GATE
 D. None of the above
530. $A+B$ can be implemented by
 A. NAND gate alone
 B. Both (A) and (B)
 C. NOR gate alone
 D. None of the above
531. Which of the following logic expression is incorrect?
 A. $1 \oplus 0 = 1$ B. $\oplus 1 \oplus 0 = 1$
 C. $1 \oplus 1 \oplus 1 = 1$ D. $1 \oplus 1 = 0$
532. Let x and y be the input and z be the output of NAND gate. The value of z is given by:
 A. $x \cdot y$
 B. $x+y$
 C. $x \cdot y$
 D. None of the above

533. $(NOR)(XOR)(NAND) =$
 A. NOR B. XOR
 C. NAND D. XNOR
534. The total number of Boolean functions which can be realized with four variables is
 A. 4 B. 256
 C. 17 D. 65,536
535. The Boolean function $A + BC$ is reduced form of....
 A. $AB + BC$ B. $A + ABC$
 C. $(A+B)(A+C)$ D. $(A+C)B$
536. The logical expression $y = A + A B$ is equivalent to...
 A. $Y = AB$ B. $Y = A + B$
 C. $Y = A+B$ D. $Y = A B$
537. What is the maximum number of different Boolean functions involving n Boolean variables?
 A. n^2 B. 2^{2^n}
 C. 2^n D. 2^{n^2}
538. With three variables maximum possible logical expression is:
 A. 6 B. 512
 C. 256 D. 65536
539. In n variables maximum possible dual expression is:
 A. n^2 B. $2^{2^{n-1}}$
 C. 2^n D. 2^{n^2}
540. Which of the following expression is not equivalent to x ?
 A. $X \text{NAND } x$ B. $X \text{NAND } 1$
 C. $X \text{NOR } X$ D. $X \text{NOR } 1$
541. The address bus width of a memory of size 1024×8 bits is
 A. 8 bits B. 13 bits
 C. 10 bits D. 15 bits
542. The final step in designing the combinational circuit is
 A. To determine the input and output variables
 B. To draw the truth table
 C. To minimize the Boolean function for each output obtained
 D. To draw the minimized logic diagram
543. The fetching, decoding and executing of an instruction is broken down into several time intervals. Each of these intervals, involving one or more clock period is called
 A. Instruction cycle
 B. Machine cycle
 C. Process cycle
 D. None of the above
544. A combinational circuit consist of
 A. Logic gate and memory elements
 B. Logic gates only
 C. Memory elements only
 D. None of the above
545. Full adder circuit can be implemented by
 A. Multiplexer
 B. AND and OR gates
 C. Half adders
 D. Decoders
546. How many full adders are required to construct an m -bit parallel adders?
 A. m
 B. $m/2$
 C. $m-1$
 D. $m+1$

547. select the statement that best describes the parity method of error detection:

- A. Parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.
- B. Arity checking is not suitable for detecting single-bit errors in transmitted codes.
- C. Parity checking is best suited for detecting single-bit errors in transmitted codes
- D. Parity checking is not suitable for detecting single-bit errors in transmitted codes.

548. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n)

- A. EX-NOR gate
- B. OR gate
- C. EX-OR gate
- D. NAND gate

549. A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):

- A. EX-NOR gate
- B. OR gate
- C. EX-OR gate
- D. NAND gate

550. Identify the type of gate below from the equation $X = A \oplus B = \bar{A}B + A\bar{B}$

- A. OR GATE
- B. NOR GATE
- C. EX-OR GATE
- D. NAND GATE

551. Parity systems are defined as either ____ or ____ and will add an extra ____ to the digital information being transmitted.

- A. Positive, negative, byte
- C. Upper, lower, digit
- B. Odd, even, bit
- D. On, off, decimal

552. Which type of gate can be used to add two bits?

- A. EX-OR
- B. EX-NOR
- C. EX-NAND
- D. None of the above

553. Why is an exclusive-NOR gate also called an equality gate?

- A. The output is false if the inputs are equal.
- B. The output is true if the inputs are opposite.
- C. The output is true if the inputs are equal.
- D. None of the above

554. Show from the truth table how an exclusive-OR gate can be used to invert the data on one input if the other input is a special control function.

- A. Using A as the control, when A = 0, X is the same as B. When A = 1, X is the same as B.
- B. Using a as the control, when a = 0, X is the same as B. When A = 1, X is the inverse of B
- C. Using A as the control, when A = 0, X is the inverse of B. When A = 1, X is the same as B
- D. Using A as the control, when A = 0, X is the inverse of B. When A = 1, X is the inverse of B.

555. Determine odd parity for each of the following data words:

- | | | |
|------------------------|----------|---------|
| 1011101 | 11110111 | 1001101 |
| A. P = 1, P = 1, P = 0 | | |
| B. P = 0, P = 0, P = 0 | | |
| C. P = 1, P = 1, P = 1 | | |
| D. P = 0, P = 0, P = 1 | | |

556. The EX-NOR is sometimes called the _____.

- A. Parity gate
- B. Equality gate
- C. Inverted gate
- D. Parity gate or the equality gate

557. Determine the values of A, B, C, and D that make the sum term $\bar{A} + B + \bar{C} + D$ equal to zero.

- A. A = 1, B = 0, C = 0, D = 0
- B. A = 1, B = 0, C = 1, D = 0
- C. A = 0, B = 1, C = 0, D = 0
- D. A = 1, B = 0, C = 1, D = 1

558. An AND gate with schematic "bubbles" on its inputs performs the same function as a(n) _____ gate.

- A. NOT
- B. OR
- C. NOR
- D. NAND

559. For the SOP expression, how many 1s are in the truth table's output column

- A. 1
- B. 2
- C. 3
- D. 4

560. A truth table for the SOP expression has how many input combinations?

- A. 1
- B. 2
- C. 4
- D. 8

561. How many gates would be required to implement the following Boolean expression before simplification? $XY + X(X+Z) + Y(X+Z)$

- A. 1
- B. 2
- C. 3
- D. 5

562. In canonical SOP form, the number of min terms in logical expression, A + B'C is:

- A. 4
- B. 5
- C. 6
- D. 7

563. How many gates would be required to implement the following Boolean expression after simplification? $XY + X(X+Z) + Y(X+Z)$

- A. 1
- B. 2
- C. 3
- D. 5

564. Which Boolean algebra property allows us to group operands in an expression in any order without affecting the results of the operation [for example, $A + B = B + A$]?
A. Associative B. Commutative
C. Boolean D. Distributive

565. Applying DeMorgan's theorem to the expression $\overline{(X+Y)} + \overline{Z}$, we get _____

- A. $(X+Y)Z$
- B. $(X'+Y')Z$
- C. $(X+Y)Z'$
- D. $(X'+Y')Z'$

566. Use Boolean algebra to find the most simplified SOP expression for $F = ABD + CD + ACD + ABC + A'BCD$.

- A. $F = ABD + ABC + CD$
- B. $F = CD + AD$
- C. $F = BC + AB$
- D. $F = AC + AD$

567. In a sequential circuit the next state is determinedand.....

- A. State variable, current state
- B. Current state, flip-flop output
- C. Current state and external input
- D. Input and clock signal applied

568. The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- A. Mod-6, Mod-10
- B. Mod-50, Mod-10
- C. Mod 10, Mod-50
- D. Mod-50, Mod-6

569. The minimum time for which the input signal has to be maintained at the input of flip-flop is called ____ of the flip-flop.

- A. Set-up time
- B. Hold time
- C. Pulse interval time
- D. Pulse stability time (PST)

570. ____ is said to occur when multiple internal variables change due to change in one input variable

- A. Race condition
- B. Hold delay
- C. Hold and wait
- D. Clock skew

571. A decade counter is.....

- A. Mode-3 counter
- B. Mod- 5 counter
- C. Mod -8 counter
- D. Mod-10 counter

572. A nibble consist of.....bits

- A. 2
- B. 4
- C. 8
- D. 16

573. Excess-8 code assigns to “-8”

- A. 1110
- B. 1100
- C. 1000
- D. 0000

574. The three fundamentals gates are:

- A. AND, NAND, NOR
- B. NOT, NOR, XOR
- C. NOT, OR, AND
- D. NOT, NOR, XOR

575. The amount of memory that is supported by any digital system depends upon....

- A. The organization of memory
- B. The structure of memory
- C. The size of decoding unit
- D. The size of the address bus of the microprocessor

576. Stack is an acronym for....

- A. LIFO memory
- B. FIFO memory
- C. Flash memory
- D. Bust flash memory

577. Addition of two octal numbers “36” and “71” results....

- A. 213
- B. 123
- C. 127
- D. 345

578. Addition of two octal numbers “56” and “243” results

- A. 2013
- B. 1023
- C. 1027
- D. 1032

579.is one of the examples of synchronous inputs.

- A. J-K input
- B. EN input
- C. Preset input (PRE)
- D. Clear Input (CLR)

580.occurs when the same clock signal arrives at different times at different clock input due to propagation delay.

- A. Race condition
- B. Ripple effect
- C. Clockskew
- D. None of the above

581. In a state diagram, the transition from a current state to the next state is determined by....

- A. Current state and the input
- B. Previous state and inputs
- C. Current state and output
- D. Previous state and output

582. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- A. 1100
- B. 0011
- C. 0000
- D. 1111

ANSWERSSHEET

1.B	2.C	3.A	4.A	5.A	6.B	7.D	8.C	9.D	10.C
11.B	12.C	13.D	14.C	15.C	16.D	17.B	18.D	19.B	20.B
21.C	22.C	23.D	24.C	25.A	26.D	27.A	28.C	29.D	30.C
31.C	32.B	33.A	34.C	35.B	36.C	37.A	38.B	39.A	40.A
41.C	42.C	43.B	44.C	45.A	46.A	47.D	48.A	49.A	50.C
51.A	52.C	53.A	54.C	55.A	56.B	57.D	58.D	59.A	60.A
61.D	62.D	63.A	64.B	65.D	66.A	67.C	68.D	69.C	70.C
71.A	72.A	73.D	74.C	75.A	76.B	77.C	78.B	79.B	80.C
81.A	82.C	83.B	84.A	85.B	86.B	87.A	88.D	89.C	90.B
91.D	92.C	93.D	94.C	95.C	96.B	97.C	98.C	99.C	100.B
101.B	102.D	103.B	104.A	105.C	106.A	107.B	108.A	109.D	110.A
111.C	112.A	113.C	114.A	115.B	116.A	117.A	118.C	119.A	120.D
121.D	122.A	123.B	124.D	125.D	126.B	127.A	128.A	129.C	130.B
131.D	132.A	133.C	134.B	135.D	136.B	137.B	138.A	139.C	140.B
141.B	142.A	143.D	144.A	145.B	146.C	147.D	148.B	149.A	150.C
151.A	152.B	153.C	154.A	155.B	156.C	157.D	158.C	159.A	160.B
161.D	162.A	163.A	164.B	165.C	166.D	167.A	168.B	169.C	170.D

171.B	172.A	173.B	174.D	175.D	176.D	177.B	178.B	179.B	180.D
181.C	182.B	183.A	184.A	185.D	186.C	187.D	188.A	189.C	190.D
191.D	192.C	193.B	194.D	195.A	196.D	197.B	198.B	199.B	200.A
201.C	202.A	203.C	204.B	205.A	206.D	207.C	208.D	209.C	210.B
211.B	212.A	213.A	214.D	215.C	216.D	217.A	218.B	219.B	220.A
221.D	222.C	223.D	224.C	225.B	226.C	227.B	228.D	229.A	230.D
231.A	232.C	233.D	234.C	235.C	236.D	237.A	238.D	239.B	240.A
241.D	242.D	243.A	244.A	245.B	246.D	247.C	248.D	249.B	250.D
251.C	252.D	253.C	254.A	255.B	256.A	257.B	258.C	259.C	260.B
261.B	262.A	263.D	264.A	265.A	266.B	267.A	268.D	269.B	270.A
271.A	272.C	273.D	274.A	275.B	276.A	277.C	278.A	279.A	280.B
281.C	282.C	283.C	284.B	285.C	286.A	287.C	288.C	289.A	290.A
291.A	292.A	293.D	294.C	295.C	296.B	297.C	298.A	299.A	300.C
301.A	302.A	303.C	304.A	305.D	306.D	307.C	308.C	309.D	310.D
311.C	312.D	313.A	314.C	315.B	316.D	317.A	318.B	319.A	320.B
321.A	322.C	323.B	324.A	325.B	326.C	327.D	328.A	329.C	330.B
331.D	332.C	333.A	334.C	335.D	336.D	337.B	338.B	339.C	340.B
341.A	342.B	343.A	344.C	345.D	346.B	347.B	348.A	349.D	350.C
351.A	352.D	353.D	354.D	355.B	356.A	357.C	358.B	359.A	360.D
361.C	362.B	363.C	364.A	365.D	366.B	367.D	368.A	369.B	370.D
371.D	372.D	373.D	374.A	375.C	376.D	377.A	378.C	379.B	380.B
381.B	382.B	383.C	384.B	385.D	386.A	387.B	388.C	389.C	390.D
391.C	392.B	393.A	394.B	395.A	396.D	397.B	398.A	399.C	400.C
401.B	402.B	403.D	404.A	405.D	406.B	407.A	408.C	409.D	410.B
411.D	412.D	413.D	414.C	415.D	416.D	417.C	418.B	419.C	420.B
421.D	422.A	423.B	424.D	425.A	426.B	427.C	428.C	429.B	430.A

431.B	432.B	433.C	434.D	435.C	436.B	437.D	438.B	439.C	440.A
441.D	442.B	443.C	444.A	445.A	446.B	447.A	448.C	449.D	450.B
451.D	452.A	453.C	454.B	455.B	456.A	457.D	458.C	459.D	460.B
461.A	462.D	463.D	464.C	465.B	466.A	467.B	468.A	469.D	470.A
471.D	472.D	473.D	474.C	475.A	476.D	477.B	478.D	479.A	480.C
481.B	482.C	483.D	484.A	485.B	486.C	487.A	488.D	489.C	490.D
491.B	492.C	493.C	494.C	495.D	496.A	497.B	498.B	499.D	500.C
501.D	502.B	503.A	504.C	505.D	506.B	507.C	508.C	509.C	510.A
511.C	512.A	513.C	514.C	515.C	516.A	517.B	518.C	519.A	520.B
521.B	522.A	523.D	524.D	525.D	526.C	527.C	528.B	529.A	530.B
531.B	532.A	533.B	534.D	535.C	536.C	537.B	538.C	539.B	540.D
541.C	542.D	543.B	544.B	545.A	546.A	547.C	548.A	549.C	550.C
551.B	552.A	553.C	554.B	555.D	556.B	557.B	558.C	559.C	560.D
561.D	562.B	563.B	564.B	565.A	566.A	567.C	568.A	569.B	570.A
571.D	572.B	573.D	574.C	575.D	576.A	577.C	578.D	579.D	580.B
581.A	582.C								