

MCQS (SET-III)

1. The most common addressing techniques employed by a CPU is:
 - A. Direct
 - B. Indirect
 - C. Immediate
 - D. All of these
2. _____ have been developed specifically for pipelined systems.
 - A. Utility software
 - B. Speed up utilities
 - C. Optimizing compilers
 - D. None of the mentioned
3. The pipelining process is also called as _____
 - A. Superscalar operation
 - B. Assembly line operation
 - C. Von Neumann cycle
 - D. None of the mentioned
4. Each stage in pipelining should be completed within _____ cycle.
 - A. 1
 - B. 2
 - C. 3
 - D. 4
5. To increase the speed of memory access in pipelining, we make use of _____
 - A. Special memory locations
 - B. Special purpose registers
 - C. Cache
 - D. Buffers
6. The contention for the usage of a hardware device is called _____
 - A. Structural hazard
 - B. Stale
 - C. Deadlock
 - D. None of the mentioned
7. The situation wherein the data of operands are not available is called _____
 - A. Data hazard
 - B. Stock
 - C. Deadlock
 - D. Structural hazard
8. The CISC stands for _____
 - A. Computer Instruction Compliment Set
 - B. Complete Instruction Set
 - C. Computer Indexed Set Components
 - D. Complex Instruction set computer
9. The computer architecture aimed at reducing the time of execution of instructions is _____
 - A. CISC
 - B. RISC
 - C. ISA
 - D. ANNA
10. The iconic feature of the RISC machine among the following is _____
 - A. Reduced number of addressing modes
 - B. Increased memory size
 - C. Having a branch delay slot
 - D. All of the mentioned
11. Both the CISC and RISC architectures have been developed to reduce the _____
 - A. Cost
 - B. Time delay
 - C. Semantic gap
 - D. All of the mentioned
12. Pipe-lining is a unique feature of _____
 - A. RISC
 - B. CISC
 - C. ISA
 - D. IANA
13. In CISC architecture most of the complex instructions are stored in _____
 - A. Register
 - B. Diodes
 - C. CMOS
 - D. Transistors
14. In _____ the operand is specified in the instruction itself
 - A. Immediate addressing
 - B. Register mode
 - C. Implied addressing
 - D. Register Indirect
15. In which mode the operand is placed in one of 8 bit or 16 bit general purpose registers?
 - A. Immediate addressing
 - B. Register mode
 - C. Implied addressing
 - D. Register Indirect
16. An offset is determined by adding any combination of _____ address elements
 - A. 3
 - B. 4
 - C. 5
 - D. 6
17. Zero address instruction are designed with implied addressing mode.
 - A. TRUE
 - B. FALSE
 - C. Can be true or false
 - D. Cannot say
18. In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____
 - A. EA = 5+R1
 - B. EA = R1
 - C. EA = [R1]
 - D. EA = 5+[R1]
19. The addressing mode/s, which uses the PC instead of a general purpose register is _____
 - A. Indexed with offset
 - B. Relative
 - C. Direct
 - D. Both indexed with offset and direct
20. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
 - A. Relative
 - B. Indirect
 - C. Index with Offset
 - D. Immediate
21. Sign magnitude is a very simple representation of?
 - A. Positive number
 - B. Negative numbers
 - C. Infinity
 - D. Zero
22. Sign bit 1 represents
 - A. Positive number
 - B. FALSE
 - C. TRUE
 - D. Negative Number
23. The logic 1 in positive logic system is represented by?
 - A. Zero voltage
 - B. Lower voltage level
 - C. Higher voltage level
 - D. Negative voltage
24. The m-bit parallel adder consists of
 - A. m full adders
 - B. m+1 full adders
 - C. m-1 full adders
 - D. m/2 full adders
25. Input or output devices that are connected to computer are called _____
 - A. Input/Output Subsystem
 - B. Peripheral Devices
 - C. Interfaces
 - D. Interrupt

26. How many types of modes of I/O Data Transfer?
 A. 2 B. 3
 C. 4 D. 5
27. The method which offers higher speeds of I/O transfers is _____.
 A. Interrupts
 B. Memory mapping
 C. Program-controlled I/O
 D. DMA
28. In memory-mapped I/O _____.
 A. The I/O devices have a separate address space
 B. The I/O devices and the memory share the same address space
 C. A part of the memory is specifically set aside for the I/O operation
 D. The memory and I/O devices have an associated address space
29. The ISA is an architectural standard developed by _____.
 A. IBM B. AT&T Labs
 C. Microsoft D. Oracle
30. The SCSI BUS is used to connect the video devices to a processor by providing a _____.
 A. Single Bus B. USB
 C. SCSI D. Parallel BUS.
31. The registers of the controller are _____.
 A. 16 bit B. 32 bit
 C. 64 bit D. 128 bit
32. Auxillary memory access time is generally ____ times that of the main memory.
 A. 10 B. 100
 C. 1000 D. 10000
33. What is the formula for Hit Ratio?
 A. Hit/(Hit + Miss)
 B. Miss/(Hit + Miss)
 C. (Hit + Miss)/Miss
 D. (Hit + Miss)/Hit
34. Which of the following is correct example for Auxiliary Memory?
 A. Magnetic disks B. Tapes
 C. Flash memory D. Both A and B
35. The fastest data access is provided using _____.
 A. Cache B. DRAM's
 C. SRAM's D. Registers
36. The next level of memory hierarchy after the L2 cache is _____.
 A. Secondary storage
 B. Main memory
 C. Register
 D. TLB
37. Which Processors includes multi-clocks?
 A. Complex Instruction Set Computer
 B. Reduced Instruction Set Computer
 C. ISA
 D. ANNA
38. Which Processors Data transfer Register to register?
 A. Complex Instruction Set Computer
 B. Reduced Instruction Set Computer
 C. ISA
 D. ANNA
39. Which of the following is true?
 A. The RISC processor has a more complicated design than CISC.
 B. Risc Focus on software
 C. Cisc Focus on software
 D. Risc has Variable sized instructions
40. Which processor requires more number of registers?
 A. CISC
 B. ISA
 C. RISC
 D. ANNA
41. Both the CISC and RISC architectures have been developed to reduce the _____.
 A. Semantic gap B. Time Delay
 C. Cost D. Reduced Code
42. Which of the following is true about CISC processor?
 A. Micro programmed control unit is found in CISC.
 B. Data transfer is from memory to memory.
 C. In this instructions are not register based.
 D. All of the above
43. What is the high speed memory between the main memory and the CPU called?
 A. Register Memory
 B. Cache Memory
 C. Storage Memory
 D. Virtual Memory
44. Cache Memory is implemented using the DRAM chips.
 A. True
 B. False
45. Whenever the data is found in the cache memory it is called as _____.
 A. HIT B. MISS
 C. FOUND D. ERROR
46. LRU stands for _____.
 A. Low Rate Usage
 B. Least Rate Usage
 C. Least Recently Used
 D. Low Required Usage
47. When the data at a location in cache is different from the data located in the main memory, the cache is called _____.
 A. Unique B. Inconsistent
 C. Variable D. Fault
48. Which of the following is not a write policy to avoid Cache Coherence?
 A. Write through B. Write within
 C. Write back D. Buffered write
49. Which of the following is an efficient method of cache updating?
 A. Snoopy writes B. Write through
 C. Write within D. Buffered write
50. In _____ mapping, the data can be mapped anywhere in the Cache Memory.
 A. Associative B. Direct
 C. Set Associative D. Indirect
51. The number of sign bits in a 32-bit IEEE format is _____.
 A. 1 B. 11
 C. 9 D. 23
52. The transfer between CPU and Cache is _____.
 A. Block transfer
 B. Word transfer
 C. Set transfer
 D. Associative transfer
53. What is Interprocess communication?
 A. Allows processes to communicate and synchronize their actions when using the same address space
 B. Allows processes to communicate and synchronize their actions
 C. Allows the processes to only synchronize their actions without communication
 D. None of the mentioned

54. Message passing system allows processes to _____
 A. Communicate with each other without sharing the same address space
 B. Communicate with one another by resorting to shared data
 C. Share data
 D. Name the recipient or sender of the message
55. Which of the following two operations are provided by the IPC facility?
 A. Write & delete message
 B. Delete & receive message
 C. Send & delete message
 D. Receive & send message
56. Messages sent by a process _____
 A. Have to be of a fixed size
 B. Have to be a variable size
 C. Can be fixed or variable sized
 D. None of the mentioned
57. The link between two processes P and Q to send and receive messages is called _____
 A. Communication link
 B. Message-passing link
 C. Synchronization link
 D. All of the mentioned
58. Which memory storage is widely used in PCs and Embedded Systems?
 A. EEPROM B. Flash memory
 C. SRAM D. DRAM
59. How is the protection and security for an embedded system made?
 A. Security chips
 B. Memory disk security
 C. IPR
 D. OTP

60. Which of the following task swapping method is a better choice in the embedded systems design?
 A. Time slice
 B. RMS
 C. Cooperative multitasking
 D. Pre-emptive
61. Which type of memory is suitable for low volume production of embedded systems?
 A. Non-volatile B. RAM
 C. Volatile D. ROM
62. Which level simulates the algorithms that are used within the embedded systems?
 A. Algorithmic level
 B. Switch level
 C. Gate level
 D. Circuit level
63. How an embedded system communicate with the outside world?
 A. Memory B. Output
 C. Peripherals D. Input
64. What does MESI stand for?
 A. Modified exclusive system input
 B. Modifies embedded shared invalid
 C. Modified exclusive shared invalid
 D. Modified exclusive stale invalid
65. Which of the following is the pin efficient method of communicating between other devices?
 A. Memory port B. Peripheral port
 C. Parallel port D. Serial port
66. Which of the following is a traditional method for emulating the processor?
 A. CPU simulator
 B. SDS
 C. ICE
 D. Low-level language simulator
67. Which of the following unit protects the memory?
 A. Memory management unit
 B. Peripheral unit
 C. Execution unit
 D. Bus interface unit
68. Identify the standard software components that can be reused in an embedded system design?
 A. Memory
 B. Application software
 C. Application manager
 D. Operating system
69. What does ICE stand for?
 A. In-circuit EPROM
 B. In-code emulation
 C. In-circuit emulation
 D. In-code EPROM
70. Which of the following offers external chips for memory and peripheral interface circuits?
 A. Embedded system
 B. Peripheral system
 C. Microcontroller
 D. Microprocessor
71. What kind of socket does an external EPROM to be plugged in for prototyping?
 A. Piggyback reset socket
 B. Multi-socket
 C. Piggyback
 D. Single socket
72. Which is the single device capable of providing prototyping support for a range of microcontroller?
 A. Umbrella device
 B. OTP
 C. RAM
 D. ROM
73. What does PCM stand for?
 A. Peculiar code modulation
 B. Pulse codec machine
 C. Pulse code modulation
 D. Peripheral code machine
74. Which one of the following offers CPUs as integrated memory or peripheral interfaces?
 A. Memory system
 B. Embedded system
 C. Microcontroller
 D. Microprocessor
75. Which of the following language can describe the hardware?
 A. C B. C++
 C. JAVA D. VHDL
76. What do VHDL stand for?
 A. Verilog hardware description language
 B. VHSIC hardware description language
 C. Very hardware description language
 D. VMEbus description language
77. Each unit to be modelled in a VHDL design is known as
 A. Behavioural model
 B. Design architecture
 C. Design entity
 D. Structural model
78. Which of the following are capable of displaying output signal waveforms resulting from stimuli applied to the inputs?
 A. VHDL simulator
 B. VHDL emulator
 C. VHDL debugger
 D. VHDL locator

79. Which of the following describes the connections between the entity port and the local component?
- Port map
 - One-to-one map
 - Many-to-one map
 - One-to-many maps
80. Which of the following is an abstraction of the signal impedance?
- Level
 - Strength
 - Size
 - Nature
81. Which level simulates the algorithms that are used within the embedded systems?
- Gate level
 - Circuit level
 - Switch level
 - Algorithmic level
82. Which level model components like ALU, memories registers, muxes and decoders?
- Switch level
 - Register-transfer level
 - Gate level
 - Circuit level
83. Which of the following is the most frequently used circuit-level model?
- SPICE
 - VHDL
 - Verilog
 - System Verilog
84. Which model includes geometric information?
- Switch-level model
 - Layout model
 - Gate level model
 - Register-transfer level
85. Which model cannot simulate directly?
- Circuit level model
 - Switch-level model
 - Gate level model
 - Layout model
86. Which models communicate between the components?
- Transaction level modelling
 - Fine-grained modelling
 - Coarse-grained modelling
 - Circuit level model
87. How many kinds of wait statements are available in the VHDL design?
- 3
 - 4
 - 5
 - 6
88. Which wait statement does follow a condition?
- Wait for
 - Wait until
 - Wait
 - Wait on
89. Which of the following is a C++ class library?
- C++
 - C
 - JAVA
 - SystemC
90. Which model of SystemC uses floating point numbers to denote time?
- SystemC 1.0
 - SystemC 2.0
 - SystemC 3.0
 - SystemC 4.0
91. Which model of SystemC uses the integer number to define time?
- SystemC 1.0
 - SystemC 2.0
 - SystemC 3.0
 - SystemC 4.0
92. What does ESL stand for?
- EEPROM system level
 - Electronic-system level
 - Electrical system level
 - Electron system level
93. What to TLM stand for?
- Transfer level modelling
 - Triode level modelling
 - Transaction level modelling
 - Transistor level modelling
94. Which of the following provides a buffer between the user and the low-level interfaces to the hardware?
- Operating system
 - Kernel
 - Software
 - Hardware
95. Which of the following enables the user to utilise the system efficiently?
- Kernel
 - Operating system
 - Software
 - Hardware
96. Which of the following can make the application program hardware independent?
- Software
 - Application manager
 - Operating system
 - Kernel
97. Which of the following speed up the testing process?
- Kernel
 - Software
 - Application manager
 - Program debugging tools
98. Which of the following includes its own I/O routine?
- Hardware
 - Kernel
 - Operating system
 - Application manager
99. Which forms the heart of the operating system?
- Kernel
 - Applications
 - Hardware
 - Operating system
100. Which of the following are not dependent on the actual hardware performing the physical task?
- Applications
 - Hardware
 - Registers
 - Parameter block
101. Which of the following bus can easily upgrade the system hardware?
- Control bus
 - Data bus
 - VME bus
 - Bus interface unit
102. Which of the following is the first widely used operating system?
- MS-DOS
 - Windows XP
 - Android
 - CP/M
103. Which of the following is an example of a single task operating system?
- Android
 - Windows
 - IOS
 - CP/M
104. Which of the following becomes a limiting factor while an application program has to be complete?
- Memory
 - Peripheral
 - Input
 - Output
105. Which of the following cannot carry implicit information?
- Semaphore
 - Message passing
 - Threads
 - Process
106. What is the Real-time systems?
- Used for monitoring events as they occur
 - Primarily used on mainframe computers
 - Used for real-time interactive users
 - Used for program development

- 107.** The _____ Operating System pays more attention to the meeting of the time limits.
 A. Network B. Distributed
 C. Online D. Real-time
- 108.** In real time operating system is _____
 A. Kernel is not required
 B. Process Scheduling can be done only once task
 C. Must be serviced by its deadline period
 D. All processes have the same priority
- 109.** The interrupt latency should be _____ for real time operating systems.
 A. Maximum
 B. Minimal
 C. Dependent on the scheduling
 D. Zero
- 110.** Which scheduling amount of CPU time is allocated to each process?
 A. Equal share scheduling
 B. None of the mentioned
 C. Earliest deadline first scheduling
 D. Proportional share scheduling
- 111.** What is the Use of the robot by car manufacturing companies the example of...
 A. Applicant controlled computers
 B. User-controlled computers
 C. Machine controlled computers
 D. Network controlled computers
- 112.** When the System processes data instructions without any delay is called as
 A. Online system
 B. Real-time system
 C. Instruction system
 D. Offline system

- 113.** Which single task of a particular application is process is a type of processor...
 A. Applicant processor
 B. One task processor
 C. Real Time processor
 D. Dedicated processor
- 114.** The Designing of system take into considerations of _____
 A. Operating system
 B. Communication system
 C. Hardware
 D. All of the above
 E. None of these
- 115.** The Time duration required for scheduling dispatcher to stop one process and start another is called...
 A. Dispatch latency
 B. Process latency
 C. Interrupt latency
 D. Execution latency
- 116.** Which of the following is correct in real time?
 A. Non-preemptive kernels
 B. Preemptive kernels
 C. Neither preemptive nor non-preemptive kernels
 D. Preemptive kernels or non-preemptive kernels
- 117.** Which of the following is Preemptive, priority-based scheduling guarantees?
 A. Protection of memory
 B. Hard real-time functionality
 C. Soft real-time functionality
 D. All of the above
 E. None of these
- 118.** Which of the following is a coprocessor of 80386?
 A. 80387
 C. 8089
- 119.** Name the processor which helps in floating point calculations.
 A. Microprocessor
 C. Coprocessor
- 120.** Which is the coprocessor of 8086?
 A. 8087
 C. 8086
- 121.** Which of the following is a Motorola 68000 family?
 A. 68001
 C. 68881
- 122.** Which of the following processors can perform exponential, logarithmic and trigonometric functions?
 A. 8086
 C. 8080
- 123.** How many stack register does an 8087 have?
 A. 4
 C. 16
- 124.** Which of the following processor can handle infinity values?
 A. 8080
 C. 8087
- 125.** Which coprocessor supports affine closure?
 A. 80187
 C. 80387
- 126.** Which one is the floating point coprocessor of 80286?
 A. 8087
 C. 80287
- 127.** How many pins does 8087 have?
 A. 40 pin DIP
 C. 40 pins
- 128.** What is the clock frequency of 8087?
 A. 10 MHz
 C. 6 MHz
- 129.** How are negative numbers stored in a coprocessor?
 A. 1's complement
 C. Decimal
- 130.** How many bits are used for storing signed integers?
 A. 2
 C. 8
- 131.** Which of the processor has an internal coprocessor?
 A. 8087
 C. 80387
- 132.** What are the two major sections in a coprocessor?
 A. Control unit and numeric control unit
 B. Integer unit and control unit
 C. Floating point unit and coprocessor unit
 D. Coprocessor unit and numeric control unit
- 133.** Which are the processors based on RISC?
 A. SPARC
 C. MC68030
- 134.** What is 80/20 rule?
 A. 80% instruction is generated and 20% instruction is executed
 B. 80% instruction is executed and 20% instruction is generated
 C. 80% instruction is executed and 20% instruction is not executed
 D. 80% instruction is generated and 20% instructions are not generated

135. Which of the architecture is more complex?
 A. SPARC B. MC68030
 C. MC68030 D. 8086
136. Which is the first company who defined RISC architecture?
 A. Intel B. IBM
 C. Motorola D. MIPS
137. Which of the following processors execute its instruction in a single cycle?
 A. 8086 B. 8088
 C. 8087 D. MIPS R2000
138. How is memory accessed in RISC architecture?
 A. Load and store instruction
 B. Opcode instruction
 C. Memory instruction
 D. Bus instruction
139. Which of the following has a Harvard architecture?
 A. EDSAC B. SSEM
 C. PIC D. CSIRAC
140. Which of the following statements are true for von Neumann architecture?
 A. Shared bus between the program memory and data memory
 B. Separate bus between the program memory and data memory
 C. External bus for program memory and data memory
 D. External bus for data memory only
141. What is CAM stands for?
 A. Content-addressable memory
 B. Complex addressable memory
 C. Computing addressable memory
 D. Concurrently addressable memory
142. Which of the following uses Harvard architecture?
 A. TEXAS TMS320
 B. 80386
 C. 80286
 D. 8086
143. Which company further developed the study of RISC architecture?
 A. Intel
 B. Motorola
 C. University of Berkeley
 D. MIPS
144. Princeton architecture is also known as
 A. Von Neumann architecture
 B. Harvard
 C. RISC
 D. CISC
145. Who coined the term RISC?
 A. David Patterson B. Von Neumann
 C. Michael J Flynn D. Harvard
146. Which of the following is an 8-bit RISC Harvard architecture?
 A. AVR B. Zilog80
 C. 8051 D. Motorola 6800
147. Which of the following processors has CISC architecture?
 A. AVR B. Atmel
 C. Blackfin D. Zilog Z80
148. Which is the most basic non-volatile memory?
 A. Flash memory B. PROM
 C. EPROM D. ROM
149. Who has invented flash memory?
 A. Dr. Fujio Masuoka
 B. John Ellis
 C. Josh Fisher
 D. John Ruttenberg
150. Which of the following is serial access memory?
 A. RAM B. Flash memory
 C. Shifters D. ROM
151. Which is the early form of non-volatile memory?
 A. Magnetic core memory
 B. Ferrimagnetic memory
 C. Anti-magnetic memory
 D. Anti-ferromagnetic
152. Which of the following memories has more speed in accessing data?
 A. SRAM B. DRAM
 C. EPROM D. EEPROM
153. In which memory, the signals are multiplexed?
 A. DRAM B. SRAM
 C. EPROM D. EEPROM
154. How many main signals are used with memory chips?
 A. 2 B. 4
 C. 6 D. 8
155. What is the purpose of address bus?
 A. To provide data to and from the chip
 B. To select a specified chip
 C. To select a location within the memory chip
 D. To select a read/write cycle
156. Which are the two main types of processor connection to the motherboard?
 A. Sockets and slots
 B. Sockets and pins
 C. Slots and pins
 D. Pins and ports
157. Which of the following has programmable hardware?
 A. Microcontroller B. Microprocessor
 C. Coprocessor D. FPGA
158. Who invented TriMedia processor?
 A. Intel
 B. IBM
 C. Apple
 D. NXP Semiconductor
159. Which of the following have a 16 Mbytes addressed range?
 A. PowerPC B. M68000
 C. DSP56000 D. TMS 320
160. Which of the following can destroy the accuracy in the algorithms?
 A. Delays B. Error signal
 C. Interrupt D. mmu
161. How many numbers of ways are possible for allocating the memory to the modular blocks?
 A. 1 B. 2
 C. 3 D. 4
162. Which of the following is replaced with the absolute addressing mode?
 A. Relative addressing mode
 B. Protective addressing mode
 C. Virtual addressing mode
 D. Temporary addressing mode
163. What is the main purpose of the memory management unit?
 A. Address translation
 B. Large storage
 C. Reduce the size
 D. Provides address space
164. Which of the following provides stability to the multitasking system?
 A. Memory
 B. DRAM
 C. SRAM
 D. Memory partitioning
165. Which of the following is used by the M68000 family?
 A. M68000 B. 80386
 C. 8086 D. 80286

166. What can be done for the fine grain protection of the processor?
- Add extra description bit
 - Add error signal
 - Add wait stage
 - Remains unchanged
167. Which of the following technique is used by the UNIX operating system?
- Logical address memory
 - Physical address memory
 - Virtual memory technique
 - Translational address
168. Which of the following consist two lines of legs on both sides of a plastic or ceramic body?
- SIMM
 - DIMM
 - Zig-zag
 - Dual in-line
169. Which of the following can transfer multiple bits of data simultaneously?
- Serial port
 - Sequential port
 - Concurrent unit
 - Parallel port
170. Which of the following are interfaced as inputs to the parallel ports?
- LEDs
 - Switch
 - Alphanumeric display
 - Seven segmented display
171. Which of the following are interfaced as the outputs to the parallel ports?
- Keyboards
 - Switches
 - LEDs
 - Knobs
172. How many registers are there to control the parallel port in the basic form?
- 1
 - 3
 - 2
 - 5
173. Which of the following is also known as tri-state?
- Output port
 - Input port
 - Parallel port
 - Output-input port
174. How buffers are enabled in the parallel ports?
- By the data register
 - By data direction register
 - By individual control register
 - By data and individual control register
175. Which of the following registers offers high impedance?
- Data register
 - Data direction register
 - Individual control bit
 - Data register and data direction register
176. Which of the following can be used as a chip select?
- Multifunction I/O port
 - Parallel port
 - DMA port
 - Memory port
177. Which of the following is necessary for the parallel input-output port?
- Inductor
 - Pull-up resistor
 - Push-up resistor
 - Capacitor
178. Which of the following can be described as general-purpose?
- Multifunction I/O port
 - Input port
 - DMA port
 - Output port
179. What does UART stand for?
- Universal asynchronous receiver transmitter
 - Unique asynchronous receiver transmitter
 - Universal address receiver transmitter
 - Unique address receiver transmitter
180. How is data detected in a UART?
- Counter
 - Timer
 - Clock
 - First bit
181. Which of the signal is set to one, if no data is transmitted?
- READY
 - START
 - STOP
 - TXD
182. What rate can define the timing in the UART?
- Bit rate
 - Baud rate
 - Speed rate
 - Voltage rate
183. How is baud rate supplied?
- Baud rate voltage
 - External timer
 - Peripheral
 - Internal timer
184. Which is the most commonly used UART?
- 8253
 - 8254
 - 8259
 - 8250
185. Which company developed 16450?
- Philips
 - Intel
 - National semiconductor
 - IBM
186. What does ADS indicate in 8250 UART?
- Address signal
 - Address terminal signal
 - Address strobe signal
 - Address generating signal
187. Which of the following signals are active low in the 8250 UART?
- BAUDOUT
 - DDIS
 - INTR
 - MR
188. Which of the signal can control bus arbitration logic in 8250?
- MR
 - DDIS
 - INTR
 - RCLK
189. Which of the following can be used for long distance communication?
- I2C
 - Parallel port
 - SPI
 - RS232
190. Which of the following can affect the long distance communication?
- Clock
 - Resistor
 - Inductor
 - Capacitor
191. Which are the serial ports of the IBM PC?
- COM1
 - COM4 and COM1
 - COM1 and COM2
 - COM3
192. Which of the following can provide hardware handshaking?
- RS232
 - Parallel port
 - Counter
 - Timer
193. Which of the following have an asynchronous data transmission?
- SPI
 - RS232
 - Parallel port
 - I2C
194. How many areas does the serial interface have?
- 1
 - 3
 - 2
 - 4
195. The RS232 is also known as
- UART
 - SPI
 - Physical interface
 - Electrical interface

196. How much voltage does the MC1489 can take?

- A. 12V
- B. 5V
- C. 3.3V
- D. 2.2V

197. Which of the following is not a serial protocol?

- A. SPI
- B. I2C
- C. Serial port
- D. RS232

198. Which of the following is an ideal interface for LCD controllers?

- A. SPI
- B. Parallel port
- C. Serial port
- D. M-Bus

199. Which of the following works by dividing the processor's time?

- A. Single task operating system
- B. Multitask operating system
- C. Kernel
- D. Applications

200. Which of the following decides which task can have the next time slot?

- A. Single task operating system
- B. Applications
- C. Kernel
- D. Software

201. Which of the following controls the time slicing mechanism in a multitasking operating system?

- A. Kernel
- B. Single tasking kernel
- C. Multitasking kernel
- D. Application manager

202. Which of the following provides time period for the context switch?

- A. Timer
- B. Counter
- C. Time slice
- D. Time machine

203. Which of the following can periodically trigger the context switch?

- A. Software interrupt
- B. Hardware interrupt
- C. Peripheral
- D. Memory

204. Which interrupt provides clock in the context switching system?

- A. Software interrupt
- B. Hardware interrupt
- C. Peripheral
- D. Memory

205. The special table in the multitasking operating system is also known as

- A. Task control block
- B. Task access block
- C. Task address block
- D. Task allocating block

206. Which of the following stores all the task information that the system requires?

- A. Task access block
- B. Register
- C. Accumulator
- D. Task control block

207. Which of the following contains all the task and their status?

- A. Register
- B. Ready list
- C. Access list
- D. Task list

208. Which determines the sequence and the associated task's priority?

- A. Scheduling algorithm
- B. Ready list
- C. Task control block
- D. Application register

209. Which of the following can be used to refer to entities within the RTOS?

- A. Threads
- B. Kernels
- C. System
- D. Options

210. Which of the following defines the set of instructions loaded into the memory?

- A. Process
- B. Task
- C. Thread
- D. System hardware

211. Which of the following uses its own address space?

- A. Thread
- B. Process
- C. Task
- D. Kernel

212. Which of the following does not use a shared memory?

- A. Process
- B. Thread
- C. Task
- D. Kernel

213. Which of the following can own and control the resources?

- A. Thread
- B. Task
- C. System
- D. Peripheral

214. Which can be supported if the task or process maintains a separate data area for each thread?

- A. Single thread system
- B. Mono thread system
- C. Multiple threads
- D. Dual threads

215. Which of the following possesses threads of execution?

- A. Process
- B. Thread
- C. Kernel
- D. Operating system

216. Which of the following is inherited from the parent task?

- A. Task
- B. Process
- C. Thread
- D. Kernel

217. Which term is used to encompass more than a simple context switch?

- A. Process
- B. Single thread system
- C. Thread
- D. Multithread

218. Which can be considered as the lower level in the multitasking operating system?

- A. Process
- B. Task
- C. Threads
- D. Multi threads

219. Which of the following are the pin efficient method of communicating between other devices?

- A. Serial port
- B. Parallel port
- C. Peripheral port
- D. Memory port

220. Which of the following depends the number of bits that are transferred?

- A. Wait statement
- B. Ready statement
- C. Time
- D. Counter

221. Which of the following is the most commonly used buffer in the serial porting?

- A. LIFO
- B. FIFO
- C. FILO
- D. LILO

222. What does SPI stand for?

- A. Serial parallel interface
- B. Serial peripheral interface
- C. Sequential peripheral interface
- D. Sequential port interface

223. Which allows the full duplex synchronous communication between the master and the slave?

- A. SPI
- B. Serial port
- C. I2C
- D. Parallel port

224. Which of the following processor uses SPI for interfacing?
 A. 8086 B. 8253
 C. 8254 D. MC68HC11
225. In which register does the data is written in the master device?
 A. Index register B. Accumulator
 C. SPDR D. Status register
226. What happens when 8 bits are transferred in the SPI?
 A. Wait statement
 B. Ready statement
 C. Interrupt
 D. Remains unchanged
227. Which signal is used to select the slave in the serial peripheral interfacing?
 A. Slave select B. Master select
 C. Interrupt D. Clock signal
228. How much time period is necessary for the slave to receive the interrupt and transfer the data?
 A. 4 clock time period
 B. 8 clock time period
 C. 16 clock time period
 D. 24 clock time period
229. Which of the following allows a lower priority task to run despite the higher priority task is active and waiting to preempt?
 A. Message queue
 B. Message passing
 C. Semaphore
 D. Priority inversion
230. What happens to the interrupts in an interrupt service routine?
 A. Disable interrupt
 B. Enable interrupts
 C. Remains unchanged
 D. Ready state
231. Which of the following is a part of RTOS kernel?
 A. Memory B. Input
 C. ISR D. Register
232. Which of the following is an industrial interconnection bus?
 A. Bus interface unit
 B. Data bus
 C. Address bus
 D. VMEbus
233. Which of the following supports seven interrupt priority level?
 A. Kernel
 B. Operating system
 C. VMEbus
 D. Data bus
234. Which allows the parallel development of the hardware and software in the simulation?
 A. High-level language simulation
 B. Low-level language simulation
 C. CPU simulator
 D. Onboard simulator
235. Which of the following are used to test the software?
 A. Data entity B. Data entry
 C. Data table D. Data book
236. Which allows the UNIX software to be ported using a simple recompilation?
 A. pSOS+
 B. UNIX compatible library
 C. pSOS+m
 D. pOS+kernel
237. Which of the following can simulate the processor, memory, and peripherals?
 A. Input simulator
 B. Peripheral simulator
 C. Memory simulator
 D. CPU simulator
238. How many categories are there for the low-level simulation?
 A. 2 B. 3
 C. 4 D. 5
239. Which of the following can simulate the LCD controllers and parallel ports?
 A. Memory simulator
 B. SDS
 C. Input simulator
 D. Output tools
240. Which of the following provides a low-level method of debugging software?
 A. High-level simulator
 B. Low-level simulator
 C. Onboard debugger
 D. CPU simulator
241. Which of the following has the ability to download code using a serial port?
 A. CPU simulator
 B. High-level language simulator
 C. Onboard debugger
 D. Low-level language simulator
242. What does the processor fetches from the EPROM if the board is powered?
 A. Reset vector
 B. Ready vector
 C. Start vector
 D. Acknowledge vector
243. Which of the following device can transfer the vector table from the EPROM?
 A. ROM B. RAM
 C. CPU D. Peripheral
244. Which of the following allows the reuse of the software and the hardware components?
 A. Platform based design
 B. Memory design
 C. Peripheral design
 D. Input design
245. Which of the following is the design in which both the hardware and software are considered during the design?
 A. Platform based design
 B. Memory based design
 C. Software/hardware codesign
 D. Peripheral design
246. What does API stand for?
 A. Address programming interface
 B. Application programming interface
 C. Accessing peripheral through interface
 D. Address programming interface
247. Which activity is concerned with identifying the task at the final embedded systems?
 A. High-level transformation
 B. Compilation
 C. Scheduling
 D. Task-level concurrency management
248. In which design activity, the loops are interchangeable?
 A. Compilation
 B. Scheduling
 C. High-level transformation
 D. Hardware/software partitioning
249. Which design activity helps in the transformation of the floating point arithmetic to a fixed point arithmetic?
 A. High-level transformation
 B. Scheduling
 C. Compilation
 D. Task-level concurrency management
250. Which design activity is in charge of mapping operations to hardware?
 A. Scheduling
 B. High-level transformation
 C. Hardware/software partitioning
 D. Compilation

251. Which of the following is approximated during hardware /software partitioning, during task level concurrency management?
- Scheduling
 - Compilation
 - Task-level concurrency management
 - High-level transformation
252. Which of the following is a process of analyzing the set of possible designs?
- Design space exploration
 - Scheduling
 - Compilation
 - Hardware/software partitioning
253. Which of the following is a meet-in-the-middle approach?
- Peripheral based design
 - Platform based design
 - Memory based design
 - Processor design
254. A software program that serves as an interface between the user of a computer and computer hardware is called
- Application software
 - Utility system
 - Compiler
 - Operating system
255. Which of the following was the first single user command based operating system (OS) for PC?
- Windows 9X
 - VMS
 - Windows 95
 - PC-DOS
256. Which of the following is/are multitasking operating system?
- Linux
 - Unix
 - Windows 95
 - All of the above
257. Which of the following system is responsible for scheduling tasks according to priority and resource required?
- Time Sharing Operating System
 - Real time Operating System
 - Multi User Operating System
 - Batch Processing Operating System
258. Which of the following is a batch processing operating system?
- Linux
 - VMS
 - Unix
 - Mac OS
259. Which of the following is also known as Command Line Interface (CLI)?
- Character User Interface
 - Command User Interface
 - Command User Intercom
 - None of these
260. Microsoft Windows operating system is and
- Multitasking, Multiuser
 - Multiuser, Single tasking
 - Single user, Multitasking
 - Single user, Single tasking
261. The process which is used to load the operating system in the memory of computer is called
- Processing
 - Booting
 - Starting
 - Synchronizing
262. Which program is typically stored in ROM (read only memory) of a computer system?
- Application program
 - Operating system program
 - Bootstrap program
 - Both b and c
263. The process of choosing a task among several tasks in the pool and loading it into the main memory, is
- Single processing
 - Job scheduling
 - Single programming
 - Single tasking
264. What is the full form of POST?
- Power On Self Test
 - Power Off Self Test
 - Power On/Off Self Test
 - None
265. The _____ Operating System pays more attention to the meeting of the time limits.
- Network
 - Distributed
 - Online
 - Real-time
266. The interrupt latency should be for real time operating systems.
- Maximum
 - Minimal
- C. Dependent on the scheduling
D. Zero
267. The Time duration required for scheduling dispatcher to stop one process and start another is called...
- Dispatch latency
 - Process latency
 - Interrupt latency
 - Execution latency
268. Which single task of a particular application is process is a type of processor...
- Applicant processor
 - One task processor
 - Real Time processor
 - Dedicated processor
269. Which one of the following is a real time operating system?
- RTLinux
 - VxWorks
 - Windows CE
 - All of the mentioned

ANSWER SHEET

I.D	2.C	3.B	4.A	5.C	6.A	7.A	8.D	9.B	10.C
II.C	12.A	13.D	14.C	15.B	16.A	17.A	18.D	19.B	20.A
III.B	22.D	23.C	24.A	25.B	26.B	27.D	28.B	29.A	30.D
III.B	32.C	33.A	34.D	35.D	36.C	37.A	38.B	39.B	40.C
III.A	42.D	43.B	44.B	45.A	46.C	47.B	48.B	49.A	50.A
III.A	52.B	53.B	54.A	55.D	56.C	57.A	58.D	59.C	60.D
III.A	62.A	63.C	64.C	65.D	66.C	67.A	68.D	69.C	70.D

71.C	72.A	73.C	74.C	75.D	76.B	77.C	78.A	79.A
81.D	82.B	83.A	84.B	85.D	86.A	87.B	88.B	89.D
91.B	92.B	93.C	94.A	95.B	96.C	97.D	98.C	99.A
101.C	102.D	103.D	104.A	105.A	106.A	107.D	108.C	109.B
111.C	112.B	113.D	114.D	115.A	116.B	117.C	118.A	119.C
121.C	122.B	123.B	124.C	125.B	126.C	127.A	128.	129.B
131.D	132.A	133.A	134.A	135.A	136.B	137.D	138.A	139.C
141.A	142.A	143.C	144.A	145.A	146.A	147.D	148.D	149.A
151.A	152.A	153.A	154.B	155.C	156.A	157.D	158.D	159.B
161.C	162.A	163.A	164.D	165.A	166.A	167.C	168.D	169.D
171.C	172.C	173.A	174.B	175.C	176.A	177.B	178.A	179.A
181.D	182.B	183.B	184.D	185.C	186.B	187.A	188.B	189.D
191.C	192.A	193.B	194.C	195.D	196.B	197.D	198.D	199.B
201.C	202.C	203.B	204.B	205.A	206.D	207.B	208.A	209.A
211.A	212.A	213.B	214.C	215.A	216.C	217.A	218.C	219.A
221.B	222.B	223.A	224.D	225.C	226.C	227.A	228.B	229.D
231.C	232.D	233.C	234.A	235.C	236.B	237.D	238.A	239.B
241.C	242.A	243.B	244.A	245.C	246.B	247.D	248.C	249.A
251.A	252.A	253.B	254.D	255.D	256.D	257.D	258.C	259.A
261.B	262.C	263.B	264.A	265.D	266.B	267.A	268.D	269.D

REFERENCES

- Hamacher, V. C., Vranesic, Z. G., & Zaky, S. A. (2017). Computer organization and embedded systems. McGraw-Hill Education.
- Patterson, D. A., & Hennessy, J. L. (2013). Computer organization and design: The hardware/software interface. Morgan Kaufmann.
- Lee, E. A., & Seshia, S. A. (2017). Introduction to embedded systems: A cyber-physical systems approach. MIT Press.
- Mazidi, M. A., Naimi, S., & Naimi, S. (2010). AVR microcontroller and embedded systems: Using Assembly and C for ATMEL AVR. Prentice Hall.
- Valvano, J. W. (2012). Embedded systems: Real-time operating systems for ARM Cortex-M Microcontrollers. Cengage Learning.