

MULTIPLE CHOICE QUESTIONS

1. A time-sharing system implies

 - More than one processor in the memory
 - More than one program in the memory
 - More than one memory in the system
 - None of above

2. A multiprocessor computer is of the type

 - SISD
 - MIMD
 - SIMD
 - All of the above

3. Microprocessor is a device which has at least

 - Memory
 - Registers
 - I/O devices
 - CPU

4. A supercomputer has the capabilities of execution

 - Pipeline instruction
 - Floating point arithmetic operation
 - Vector instruction
 - All of the above

5. The maximum stages in pipelining architecture are

 - 4
 - 6
 - 2
 - 5

6. Instruction pipelining has minimum stages

 - 4
 - 6
 - 2
 - 3

7. Systems do not have parallel processing capabilities are

 - SISD
 - MIMD
 - SIMD
 - All of the above

8. Memory access in RISC architecture is limited to instructions

 - CALL & RET
 - STA&LDA
 - PUSH&POP
 - MOV&JMP

9. Interrupt which are initiated by an I/O device are

 - Internal
 - Software
 - External
 - All of the above

10. Interrupt which are initiated by an instruction are

 - Hardware
 - Internal
 - External
 - Software

11. States bit of the CPU are stored in a flag

 - Carry
 - Zero
 - Sign
 - All of the above

12. The effective address is the address of the operand in an instruction of type

 - Immediate
 - Register
 - Indirect
 - Computational

13. Program counter of a CPU store the address of the instruction

 - Currently executed
 - Just executed
 - To be executed next
 - None of the above

14. A stack organized computer has

 - Three-address instruction
 - One-address instruction
 - Two-address instruction
 - Zero-address instruction

15. The operation performed on stack are

 - IN & OUT
 - PUSH & POP
 - CALL & RET
 - POP&OUT

16. C. LILU

C. microprocessor consists of

 - Control unit
 - ALU
 - Program counter
 - All of the above

17. A microprocessor sequencer performs the operation

 - Read
 - Execute
 - Write
 - Read and execute

18. A micro program written as string of 0's and 1's is a

 - Symbolic microinstruction
 - Binary micro program
 - Binary microinstruction
 - All of the above

19. The branch logic that provides decision making capabilities in the control unit is known as

 - Controlled transfer
 - Unconditional transfer
 - Conditional transfer
 - None of the above

20. A control unit whose binary control variable are stored in memory is known as:

 - Hardwired control unit
 - Software control unit
 - Micro-programmed control unit
 - Hardware control unit

21. During execution subroutine return address is stored in

 - Control address register
 - Stack pointer
 - Subroutine address
 - Memory

22. The control data register holds the present microinstructions is some time is called

 - Instruction register
 - Sequence register
 - Microinstruction register
 - Pipeline register

23. A memory that is a part of a control unit is referred to as

 - External memory
 - Cache memory
 - Internal memory
 - Control memory

24. Whenever POP H instruction is executed,

 - Data byte in the HL pair are stored on the stack
 - Two data bytes at the top of the stack are transferred to the HP register pair.
 - Two data bytes at the top of the stack are transferred to the program counter
 - Two data bytes from the HL register that were previously stored on the stack are transferred back to the HL pointer

25. When the RET instruction at the end of a subroutine is executed,

 - The information where the stack is initialized is transferred to the stack pointer
 - The memory address of the RET instructions is transferred to the program counter
 - Two data bytes stored in the top two locations of the stack are transferred to the program counter.
 - Two data bytes stored in the top two locations of the stack are transferred to the stack pointer

28. When a subroutine is called, the address of the instruction following the CALL is stored in/on the
- Stack pointer
 - Program counter
 - Accumulator
 - Stack
29. A stack pointer is
- A 16-bit register in the microprocessor that indicated the beginning of the stack memory.
 - A register that decodes and executes 16-bit arithmetic expressions
 - The first memory locations where a subroutine address is stored
 - A register in which flag bits are stored.
30. A stack is
- An 8-bit register in the microprocessor
 - A set of memory locations in R/W/M reserved for storing information temporarily during the execution of a program
 - A 16-bit memory address stored in the program counter.
 - A 16-bit register in the microprocessor
31. A third and last component of CPU is
- ALU
 - Supervisor -control unit
 - Input device
 - Register unit
32. The section of the CPU that selects, interprets and sees to the execution of program instructions
- Memory
 - Control unit
 - Register unit
 - ALU
33. A device used to bring information into a computer is
- ALU
 - Control unit
 - Input device
 - Output device
34. A microprocessor is a..... on a chip
- Computer
 - ALU
 - CPU
 - Control unit
35. Part of the computer where the data and instructions are held is
- Register unit
 - Memory unit
 - Accumulator
 - CPU
36. Backing storage is so named because
- Is always kept at the back of the CPU
 - Backs up the computer's main memory
 - Lags behind the main memory
 - Is slow and backward
37. The ALU and control unit of most of the microcomputers are combined and manufactured on a single silicon chip. What is it called?
- Monochip
 - ALU
 - Microprocessor
 - Control unit
38. Which of the following code used in present day computing was developed by IBM corporation?
- ASCII
 - Baudot code
 - Hollerith code
 - EBCDIC CODE
39. Which parts of the computer were is used for calculating and comparing?
- Disk unit
 - ALU
 - Control unit
 - Modem
40. Instruction LXI in 8085 loads
- Stack pointer
 - None of the above
 - Register pair
 - All of the above
41. A CALL instruction is always encountered by instructions
- IN
 - OUT
 - RET
 - JNTR
42. In I/O mapped I/O 8085 duplicate the I/O address on
- Address and data line
 - Lower byte of address and control line
 - Lower and higher byte of address
 - Higher byte of address and data line
43. Address and data line in 8085 are
- Separate lines
 - Only lower byte of address is multiplexed
 - Common line
 - Shared line
44. The 16-bit register in 8085 is
- General purpose register
 - Stack pointer and program counter
 - Accumulator
 - All of the above
45. Microprocessor 8085 can address location up to
- 32K
 - 64K
 - 128K
 - 1M
46. Pipeline processing implement
- Fetch instructions
 - Fetch operand
 - Decode instruction
 - All of the above
47. Pipeline strategy is called implement
- Instruction execution
 - Instruction decoding
 - Instruction pre fetch
 - Instruction manipulation
48. Intel 80486 pipelining implements stages
- 6
 - 5
 - 4
 - 3
49. Pipeline processing uses the technique
- Sharing the memory
 - Pre fetching
 - Bit slicing
 - Parallel processing
50. Micro instructions are stored in
- Computer memory
 - Secondary storage
 - Primary memory
 - Control memory
51. Hardwired control unit is implemented by
- Software routines
 - Stacks
 - Logic circuits
 - Registers
52. Control unit operation is performed
- Hardwired control only
 - Micro program control only
 - Hardwired or micro program control
 - None of the above
53. Micro instructions are stored in the
- Internal storage
 - Cache
 - External storage
 - Control memory
54. The register are essential to instruction execution
- Program counter
 - Memory buffer register
 - Instruction register
 - All of the above
55. In immediate addressing the operand is placed
- In the CPU register
 - After op-code in the instruction
 - In the memory
 - In the stack

56. The most common addressing technique employed by a CPU is
 A. Immediate B. Indirect
 C. Direct D. All of the above
57. CPU does not perform the operation
 A. Data transfer
 B. Arithmetic operation
 C. Logic operation
 D. All of the above
58. Branch instructions are used to
 A. Manipulate numeric data
 B. Transfer control
 C. Logical data
 D. Manage data
59. Arithmetic instructions provide
 A. Data processing capabilities
 B. Computational capabilities
 C. Data storage capabilities
 D. Control capabilities
60. The ALU of a central processing unit does the essential math work for the computer. What does the control unit do?
 A. Communicates its results
 B. Activates the output device
 C. Monitors the flow of information
 D. Control the printer
61. Which type of computers use the 8-bit code called EBCDIC?
 A. Minicomputers
 B. Mainframe
 C. Microcomputers
 D. Supercomputers
62. The ALU of a computer responds to the commands coming from
 A. Primary memory
 B. External memory
 C. Control section
 D. Cache memory
63. The microprocessor of a computer cannot operate on any information if that information is not in its
 A. Secondary storage
 B. ALU
 C. Main storage
 D. Logic unit
64. Who coordinates the sequencing of events within the central processor of computer?
 A. Logic unit
 B. Register unit
 C. Arithmetical unit
 D. Control unit
65. A computer program that converts an entire program into machine language at one time is called a/an
 A. Interpreter B. Compiler
 C. Simulator D. Commander
66. What is meant by a dedicated computer?
 A. Which is used by one person only
 B. Which is assigned one and only one task
 C. Which does on kind of software
 D. Which is meant for application software only
67. A complete microcomputer system consists of
 A. Microprocessor
 B. Peripheral equipment
 C. Memory
 D. All of the above
68. Which major development led to the production of microcomputers?
 A. Magnetic tapes
 B. Logic gates
 C. Floppy disks
 D. Integrated circuits
69. The word size of a microprocessor refers to:
 A. The amount of information that can be stored in a byte
 B. The amount of an information that can be stored in a cycle
 C. The number of machine operations performed in a second
 D. The maximum length of an English word that can be input to a computer
70. One computer that is not considered a portable computer is
 A. Minicomputer
 B. Notebook computer
 C. Laptop computer
 D. All of the above
71. Which of the following require large computer memory?
 A. Imaging B. Voice
 C. Graphics D. All of the above
72. A computer enthusiast is:
 A. User friendly B. computer
 C. A hacker D. All of the above
73. Most of the inexpensive personal computers do not have any disk or diskette drive. What is the name of such computers?
 A. Home computers
 B. Dedicated computers
 C. Diskless computers
 D. None of the above
74. A computer has no more sense than a light
 A. Bulb B. Switch
 C. Pen D. Pad
75. How many address lines are needed to address each memory locations in a 2048×4 memory chip?
 A. 10
 B. 8
 C. 11
 D. 12
76. The stack pointer in the 8085 microprocessor is a
 A. 16-bit registers that points to stack memory locations
 B. 16-bit accumulator
 C. Memory locations in the stack
 D. Flag register used for the stack
77. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?
 A. Memory address register
 B. Instruction register
 C. Memory data register
 D. Program counter
78. Which of the following registers is loaded with the content of memory location pointed by the PC?
 A. Memory address register
 B. Instruction register
 C. Memory data register
 D. Program counter
79. In which addressing mode, the effective address of the operand is generated by adding a constant value to the contents of a register?
 A. Absolute mode
 B. Immediate mode
 C. Indirect mode
 D. Index mode
80. The unit of a computer system that executes program, communicates with and often controls the operation of other subsystems of the computer is known as
 A. CPU
 B. I/O unit
 C. Control unit
 D. Peripheral unit

81. Super computers are primarily useful for
 A. Input-output intensive processing
 B. Data-retrieval operations
 C. Mathematical-intensive scientific applications
 D. All of the above
82. The heart of any computer is the
 A. CPU B. I/O units
 C. Memory D. Disks
83. The central processing unit (CPU) consists of:
 A. Input, output and processing
 B. Control unit, primary storage, and secondary storage
 C. Control unit, arithmetical logic unit, and primary storage
 D. None of the above
84. Which is not an input device?
 A. CRT
 B. Optical scanners
 C. Voice recognition
 D. COM (Computer Output Microfilm)
85. The ascending order of a data hierarchy is:
 A. Bit-bytes-field-record-file-database
 B. Bytes-bit-fields-record-file-database
 C. Bit-bytes-record-field- file-database
 D. Bytes-bit-record-fields-file-database
86. What is the control unit's function in the CPU?
 A. To transfer data to primary storage
 B. To store program instruction
 C. To perform logic operations
 D. To decode program instructions
87. The most common input device used today is
 A. Motherboard B. Scanner
 C. Track ball D. Keyboard

88. Which is not a factor categorizing a computer?
 A. Speed of the output device
 B. Amount of main memory the CPU can use
 C. Cost of the system
 D. Where it was purchased
89. Which is not true for primary storage?
 A. Information must be transferred to primary storage
 B. It is relatively more expensive data
 C. It allows very fast access to data
 D. All of the above
90. Which is the most powerful type of computer?
 A. Microcomputer
 B. Mainframe computer
 C. Minicomputer
 D. Super computer
91. Which kind of storage device can be carried around?
 A. Floppy disk B. System cabinet
 C. Hard disk D. Hard disk drive
92. Which kind of devices allows the user to add components and capabilities to a computer system?
 A. System board B. Input devices
 C. Storage devices D. Expansion slots
93. Group of instructions that direct a computer is called
 A. Storage B. Logic
 C. Memory D. Program
94. The basic components of a modern digital computer are:
 A. Input device
 B. Central processing unit
 C. Output device
 D. All of the above

95. A collection of eight bits is called:
 A. Byte B. Record
 C. Word D. File
96. Processor of all computer, whether micro, mini or mainframe must have
 A. ALU B. Control unit
 C. Primary storage D. All of the above
97. Where does a computer add and compare data?
 A. Hard disk B. CPU chip
 C. Floppy disk D. Memory chip
98. If a particular idea can be implemented in hardware or software, the factor(s) that favor hardware implementation is/are
 A. Cost-effectiveness
 B. Reliability
 C. Speed of operation
 D. Frequent changes expected
99. Tera is 2^{30}
 A. 3^2 B. 40
 C. 30 D. 25
100. Von Neumann architecture is
 A. SISD B. MIMD
 C. SIMD D. MISD
101. To achieve parallelism, one needs a minimum of
 A. 2 processors
 B. 4 processors
 C. 3 processors
 D. None of the above
102. SIMD can be used for
 A. Railway reservation
 B. Matrix multiplication
 C. Weather forecasting
 D. Both B and C
103. A typical application of MIMD is
 A. Railway reservation
 B. Matrix multiplication
 C. Weather forecasting
 D. All of the above

104. Let * be defined as $a^b = a \cdot b$. Let $m = a^b$. The value of m^a is
 A. $a^b + b$ B. 0
 C. a D. 1
105. RST 7.5 interrupt in 8085 microprocessor executes services from interrupt vector location
 A. 0000h B. 003Ch
 C. 0075h D. 0034h
106. Three main components of a digital computer system are
 A. Memory, I/O, DMA
 B. Memory, CPU, I/O
 C. ALU, CPU, memory
 D. Control circuits, ALU, registers
107. Micro program is
 A. The name of a source program in micro computers
 B. The set of instructions indicating the primitive operations in a system
 C. A primitive form of macros used in assembly language programming
 D. A program of very small size
108. A toggle operation cannot be performed using a single
 A. NOR gate B. NAND gate
 C. AND gate D. XOR gate
109. 'n' flip-flops will divide the clock frequency by a factor of
 A. N^2 B. 2^n
 C. N D. Log(N)
110. Most of the digital computers do not have floating-point hardware because
 A. It is costly
 B. It is slower than software
 C. Floating-point addition cannot be performed by hardware
 D. None of the above

111. An assembler that runs on one machine but produces machine code for another machine is called
 A. Simulator
 B. Cross-compiler
 C. Emulator
 D. Boot-strap loader
112. Which of the following is not typically found in the status register of a microprocessor?
 A. Overflow
 B. Negative result
 C. Zero result
 D. None of the above
113. When even-parity ASCII text is transmitted asynchronously at a rate of 10 character per second over a line, what percentage of the received bits actually contain data (as opposed to overhead)?
 A. 7/11 B. 700/11
 C. 8/11 D. 80/11
114. A subtractor is not usually present in a computer because
 A. It is expensive
 B. It is not possible to design it
 C. The adder will take care of subtraction
 D. None of the above
115. Let an $a_1 \dots a_1 a_0$ be the binary representation of an integer b . The integer b is divisible by 3 if
 A. The number of one's is divisible by 3
 B. The number of one's is divisible by 3 but not by 9
 C. The number of zeroes is divisible by 3
 D. The difference of alternate sum, i.e., $(a_0 + a_2 + \dots) - (a_1 + a_3 + \dots)$ is divisible by 3
116. Which of the following 4-bit numbers equals its 2's complement?
 A. 1010
 B. 1000
 C. No such no. exists
 D. None of the above
 [Note: 1's complement of 1000 is 0111
 0111+1=1000]
117. Which of the following 4-bit numbers equals its 1's complement?
 A. 1010
 B. No such number exists
 C. 1000
 D. None of the above
118. FFFF will be the last memory location in a memory of size
 A. 1 K B. 16 K
 C. 32 K D. 64 K
 [64 K is $64 \times 1K = 2^6 \times 2^{10} = 2^{16}$ bytes
 ...i.e., 10000 bytes in Hex code. So last accessible address is 10000-1=FFFF]
119. If you want to design a boundary counter, you should prefer a flip flop of
 A. D-type B. Latch
 C. SR-type D. JK type
120. Suppose the largest n-bit binary number ' d ' digits in decimal representation. Which of the following relations between 'n' and ' d ' is approximately correct?
 A. $D=2^n$ B. $D < n \log_{10} 2$
 C. $N=2^d$ D. $D > n \log_{10} 2$
121. A computer uses 8-digit mantissa and 2-digit exponent. If $a=0.052$ and $b=28E+11$, then $b+a-b$ will
 A. Result in an overflow error
 B. 0
 C. Result in an underflow error
 D. 5.28E+11
122. Which of the following binary numbers are not divisible by 4?
 A. 10101010101010
 B. 1110001110001
 C. 100101100
 D. Both A and C
123. A computer with a 32-bit wide data bus uses 4K x8 static RAM memory chips. The smallest memory this computer can have is
 A. 32 Kb
 B. 16 Kb
 [4 Kx8=4*1K*8=2^2*2^10*2^3=2^15]
 C. 8 Kb
 D. 24 Kb
124. Which of the following instructions requires the greatest number of T-states?
 A. MOV A, B B. LDAX B
 C. MOV A, M D. DAD D
125. The 8085 microprocessor enters into wait state after the recognition of
 A. HOLD B. *RESET-IN
 C. *READY D. INTER
126. Maximum number of I/O devices that can be addressed by Intel 8085 is
 A. 65,536 B. 512
 C. 255 D. 256
127. The microprocessor may be made to exit from HALT state by asserting
 A. RESET
 B. Any of the five interrupt lines
 C. READY LINE
 D. Option (A) or option (B) or HOLD line
128. The number of RAM chips of size (256 K x 1) required to build a 1 M byte memory is
 A. 8 B. 10
 C. 32 D. 24
129. The instruction used to shift right the accumulator contents by one bit through the carry flag bit is
 A. RLC B. RRC
 C. RAL D. RAR
130. The stack is nothing but a set of
 A. Reserved ROM address spaces
 B. Reserved I/O address space
 C. Reserved RAM address spaces
 D. None of the above
131. The execution of RST instructions causes the stack pointer to
 A. Increment by two
 B. Remain unaffected
 C. Decrement by two
 D. None of the above
132. Which one of the following instructions may be used to clear the accumulator content (i.e. A=0h) irrespective of its initial value?
 A. CLR A B. SUB A
 C. ORA A D. MOV A, 00h
133. The only interrupt that is edge-triggered is
 A. INTR B. RST 7.5
 C. TRAP D. RST 5.5
134. Which of the following peripheral ICs is used to interface keyboard and display?
 A. 8251 B. 8259
 C. 8279 D. 8253
135. The contents of the A15- A8(higher order address lines) while executing "IN addr" instructions are
 A. Same as the contents of A7-A0
 B. All bits reset (i.e. 00h)
 C. Irrelevant
 D. All bits set (i.e. FFh)

136. Which one of the following instructions will never affect the zero flag?

- A. DCR reg
- B. DCX rp
- C. ORA reg
- D. XRA reg

137. Which one of the following interrupts is non-maskable?

- A. TRAP
- B. INTER
- C. RST 7.5
- D. RST 6.5

138. RST 3 instruction will cause the processor to branch to the location

- A. 0000h
- B. 0024h
- C. 0018h
- D. 8018h

139. The minimum number of bits required to represent a character from ASCII code set is

- A. 2
- B. 7
- C. 5
- D. 8

140. S0 and S1 pins are used for

- A. Serial communication
- B. Acknowledgement the interrupt
- C. Indicating the processor's status
- D. None of the above

141. Pick out the matching pair

- A. READY; RIM
- B. SID; SIM
- C. HOLD; DMA
- D. S0, S1; WAIT states

142. Which of the following is unipolar, difficult to fabricate, has very high speed and offers good resistance to radiation?

- A. ECL
- B. TTL
- C. GaAs
- D. CMOS

143. Multiplexing of data/address lines in 8085 microprocessor reduces the instructions execution time. This statement is

- A. True
- B. Most likely to be true
- C. False
- D. None of the above

144. The number of flip-flops needed to construct a binary modulo N counter is

- A. N
- B. N^2
- C. 2^N
- D. $\log_2 N$

145. To change an upper-case character to a lower-case character in ASCII, the correct mask and operation should be

- A. 0100000 and NOR
- B. 0100000 and NAND
- C. 0100000 and OR
- D. 1011111 and NAND

146. PCHL is an instruction in 8085 which transfers the contents of the register pair HL to PC. This is not a commonly used instruction as it changes the flow of control in a rather unstructured fashion. This instruction cannot be used in implementing

- A. If.....then.....else statement
- B. Case.....structure
- C. While.....do construct
- D. Call....statements

147. In an 11-bit computer instruction format, the size of address field is 4 bits. The computer uses expanding OP code technique and has 5 two-address instructions and 32 one-address instructions. The number of zero address instructions it can support is

- A. 256
- B. 16
- C. 2048
- D. 272

148. Which of the following instructions may be used to save the accumulator value onto the stack?

- A. PUSH PSW
- B. PUSH SP
- C. PUSH A
- D. POP PSW

149. Which of the following statements is true?

- A. ROM is a read/write memory
- B. PC points to the last instruction that was executed
- C. Stack works on the principle of LIFO
- D. All instructions affect the flag

150. A single instruction to clear the lower four bits of the accumulator in 8085 assembly language is

- A. XRI 0FH
- B. XRI FOH
- C. ANI FOH
- D. ANI OFH

151. In a vectored interrupt

- A. Branch address is assigned to a fixed location in memory
- B. Interrupting source supplies the branch information to the processor through an interrupt vector
- C. Branch address is obtained from a register in the processor
- D. None of the above

152. A sequence of two instructions that multiplies the contents of the DE register pair by 2 and stores the result in the HL register pair (in 8085 assembly language) is

- A. XCHG and DAD B
- B. XTHL and DAD H
- C. PCHL and DAD D
- D. XCHG and DAD H

153. The most relevant addressing mode to write position independent code is

- A. Direct mode
- B. Relative mode
- C. Indirect mode
- D. Indexed mode

154. Which of the following are CISC machines?

- A. IBM 360
- B. 68030
- C. 80386
- D. All of the above

155. The working of a staircase switch is a typical example of the logical operation

- A. OR
- B. Exclusive-OR
- C. NOR
- D. Exclusive-NOR

156. Which of the following are typical characteristics of a RISC machines?

- A. Instruction taking multiple cycles
- B. Multiple register set
- C. Highly pipelined
- D. Both B and C

157. A micro programmed control unit

- A. Is faster than a hard-wired control unit
- B. Facilitates easy implementation of new instructions
- C. Is useful when very small programs are to be run
- D. Usually refers to the control unit of a microprocessor

158. Parallel printer uses

- A. RS-232C interfaces
- B. Handshake mode
- C. Centronics interface
- D. Both B and C

159. The ASCII code 56, represents the character

- A. V
- B. A
- C. 8
- D. Carriage return

160. The number of possible Boolean function that can be defined for n Boolean variables over n-valued Boolean algebra is

- A. 2^{2^n}
- B. 2^{n^2}
- C. n^{2^n}
- D. n^{n^n}

[Hint: There are n Boolean variables. Each can take one of the n possible values 0, 1, 2, 3n-1.]

So, the truth table will have n^n rows. Now each row can take one of the ' n ' values as the output value. So, the possible number of functions are $n \times n^x$ n.....(n^n times). That is, n^{n+1}

161. The advantage of a single bus over a multi-bus is the

- A. Low cost
- B. Flexibility in attaching peripheral devices
- C. Both A and B
- D. High operating speed

162. Which of the following rules regarding the addition of 2 given numbers is correct, if negative numbers are represented in 2's complement form?

- A. Add sign bit and discard carry, if any.
- B. Add sign bit and add carry, if any.
- C. Do not add sign bit and discard carry, if any.
- D. Do not add sign bit and add carry, if any.

163. When INTR is encountered, the processor branches to the memory location, which is

- A. 0024H
- B. Determined by the "call address" instruction issued by the I/O device
- C. Determined by the "RST N" instructions issued by the I/O device
- D. Both B and C

164. In which of the following instructions bus idle situation occurs?

- A. EI
- B. INX H
- C. DAD rp
- D. DAA

165. Any instructions should have at least

- A. 2 operands
- B. 3 operands
- C. 1 operands
- D. None of the above

166. If the cache needs an access time of 20ns and the main memory 120 ns, then the average access time of a CPU is (assume hit-ratio is 80%)

- A. 30ns
- B. 35ns
- C. 40ns
- D. 45ns

167. The number of clock cycles necessary to complete 1 fetch cycle in 8085 (excluding wait state) is

- A. 3 or 4
- B. 4 or 6
- C. 4 or 5
- D. 3 or 5

168. The seek time of a disk is 30ms, it rotates at the rate of 30 rotations per second. Each track has a capacity of 300 words. The access time is approximately

- A. 47ms
- B. 60ms
- C. 50ms
- D. 62ms

169. Motorola's 68040 is comparable to

- A. 8085
- B. 80386
- C. 80286
- D. 80486

170. The possible number of Boolean functions of 3 variables X, Y and Z such that $f(X, Y, Z) = f(X', Y', Z')$ is

- A. 8
- B. 64
- C. 16
- D. 32

171. Which of the following interrupt is both level and edge sensitive?

- A. RST 5.5
- B. RST7.5
- C. INTR
- D. TRAP

172. The difference between 80486 and 80386 is/are

- A. Presence of floating-point co-processor
- B. Speed of operation
- C. Presence of 8 K cache on chip
- D. All of the above

173. The addressing mode used in the instruction PUSH B is

- A. Direct
- B. Register direct
- C. Register
- D. Immediate

174. Which of the following architecture is/are not suitable for realizing SIMD?

- A. Vector processor
- B. Von Neumann
- C. Array processor
- D. All of the above

175. The total number of possible Boolean functions involving 'n' Boolean variables is

- A. Infinitely many
- B. n^2
- C. n^n
- D. None of the above

[Hint: A single Boolean variable can take the values either 0 or 1, i.e., 2 possible ways. So, n Boolean variable can take $2 \times 2 \times 2 \times \dots \times (n \text{ times})$ values i.e., 2^n times. So, Truth table will have 2^n rows. Each row can be assigned one of the 2 values 0 or 1. So, totally 2^{2^n} functions are possible. So, none of the given choices are true.]

176. If $(11A1B)_2 = (12C9)_{16}$ (C stands for decimal 12), then the value of A and B are:

- A. 5,1
- B. 5,7
- C. 7,5
- D. None of the above

177. Which of the following operations(s) is/are not closed as regards to computers?

- A. Addition
- B. Multiplication
- C. Subtraction
- D. All of the above

178. Which of the following units can be used to measure the speed of a computer?

- A. SYPS
- B. FLOPS
- C. MIPS
- D. Both B and C

179. If $A \oplus B = C$, THEN

- A. $A \oplus B = B$
- B. $A \oplus B \oplus C = 0$
- C. $B \oplus C = A$
- D. All of the above

180. Addressing capability of 8086/88 are

- A. 64 K
- B. 2 MB
- C. 512 K
- D. 1 MB

181. Bubble memories are preferable to floppy disks because

- A. Of their higher transfer rate
- B. Of their reliability
- C. They consume less power
- D. Both B and C

182. The XOR operation is

- A. Commutative
- B. Associative
- C. Both (A) and (B)
- D. Distributive over AND operator

183. Which of the following logic families is well suited for high speed operation?

- A. TTL
- B. MOS
- C. ECL
- D. CMOS

184. Which of the following does not have 8 data lines?

- A. 8085
- B. 8088
- C. 8086
- D. Z-80

185. Negative numbers cannot be represented in

- A. Signed magnitude form
- B. 2's complement form
- C. 1's complement form
- D. None of the above

186. The addressing mode used in an instruction of the form ADD X, Y is
A. Absolute B. Indirect
C. Immediate D. Index

187. Which of the following are register?
A. Accumulator
B. Program counter
C. Stack pointer
D. All of the above

188. IBM developed a bus standard for their line of computers 'PC AT' called _____.
A. IB bus B. ISA
C. M-bus D. None of these

189. Which of the following is the programmable internal timer?
A. 8251 B. 8253
C. 8250 D. 8275

190. Bipolar devices are desirable in the fabrication of which of the following components?
A. Main memory
B. Micro program memory
C. Cache memory
D. All of the above

191. A+B can be implemented by
A. NAND gates alone
B. NOR gate alone
C. Both (A) and (B)
D. None of the above

192. Which of the following are the correct statements?
A. Bus is a group of information carrying wires
B. Bus is needed to achieve reasonable speed of operation
C. Bus can carry data or address lines, a bus can be shared by more than one device
D. All of the above

193. A number system uses 20 as the radix. The excess code that is necessary for its equivalent binary coded representation is
A. 4 B. 6
C. 5 D. 7

194. Any given truth table can be represented by a
A. Karnaugh map
B. Sum of product of Boolean expressions
C. Product of sum of Boolean expressions
D. All of the above

195. Which of the following remarks about PLA is/are true?
A. It produces product of sum as the output
B. It produces sum of products as the output
C. It is general
D. Both B and C

196. The first operating system used in microprocessor is
A. Zenix B. CP/M
C. DOS D. Multics

197. Which of the following does not need extra hardware for DRAM refreshing?
A. 8085
B. Z-80
C. Motorola-6800
D. None of the above

198. The advantage of MOS device s over bipolar devices is
A. It allows higher bit densities and also cost-effective
B. It is easy to fabricate
C. Its higher impedance
D. All of the above

199. Which of the following comments about the Program Counter (PC) are true?
A. It is a register
B. It is a cell in ROM
C. During execution of the current instruction, its content are changes
D. Both A and C

200. Choose the correct statements from the following
A. By scanning a bit pattern, one can say whether, it represents data or form
B. Whether a given piece of information is a data or not depends on the particular applications
C. Positive number cannot be represented in 1's complement form
D. Both B and C

201. Property of locality of reference may fail if a program has
A. Many conditional jumps
B. Many operands
C. Many unconditional jumps
D. All of the above

202. In Reverse Polish notation, expression A*B+C*D is written as
A. AB*CD+* B. AB*CD+*
C. A*BCD+* D. A*B*CD+

203. SIMD represents an organization that _____.
A. Refers to a computer system capable of processing several programs at the same time.
B. Represents organization of single computer containing a control unit, processor unit and a memory unit.
C. Includes many processing units under the supervision of a common control unit
D. None of the above

204. Floating point representation is used to store
A. Boolean values B. Real integers
C. Whole numbers D. Integers

205. Suppose that a bus has 16 data lines and required 4 cycles of 250 nano seconds each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?

A. 1 Megabyte/sec
B. 8 Megabytes/sec
C. 4 Megabytes/sec
D. 2 Megabytes/sec

206. Assembly language

A. Uses alphabetic codes in place of binary numbers used in machine language
B. Is the easiest language to write programs
C. Need not be translated into machine language
D. None of the above

207. In computers, subtraction is generally carried out by

A. 9's complement
B. 1's complement
C. 10's complement
D. 2's complement

208. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to

A. The time it takes for the platter to make a full rotation
B. The time it takes for the read-write head to move into position over the appropriate track
C. The time it takes for the platter to rotate the correct sector under the head
D. None of the above

209. What characteristic of RAM memory makes it not suitable for permanent storage?
- Too slow
 - It is a volatile
 - Unreliable
 - Too bulky
210. Computers use addressing mode techniques for:
- Giving programming versatility to the user by providing facilities as pointers to memory counters for loop control
 - To reduce no. of bits in the field of instruction
 - Specifying rules for modifying or interpreting address field of the instruction
 - All the above
211. The circuit used to store one bit of data is known as
- Register
 - Decoder
 - Encoder
 - Flip-flop
212. $(2FA0C)_{16}$ is equivalent to:
- $(195\ 084)_{10}$
 - Both A and B
 - $(00101111010\ 0000\ 1100)_2$
 - None of these
213. The average time required to reach a storage location in memory and obtain its contents is called the:
- Seek time
 - Turnaround time
 - Access time
 - Transfer time
214. Which of the following is not a weighted code?
- Decimal number system
 - Binary Number System
 - Excess-3 code
 - None of the above
215. _____ register keeps track of the instructions stored in program stored in memory.
- AR (Address Register)
 - PC (Program Counter)
 - XR (Index Register)
 - AC (Accumulator)
216. The addressing mode used in an instruction of the form $ADD\ X\ Y$, is
- Absolute
 - Index
 - Indirect
 - None of the above
217. In a memory-mapped I/O system, which of the following will not be there?
- LDA
 - ADD
 - IN
 - OUT
218. In a vectored interrupt:
- The branch address is assigned to a fixed location in memory
 - The interrupting source supplies the branch information to the processor through an interrupt vector
 - The branch address is obtained from a register in the processor
 - None of the above
219. Cache memory acts between
- CPU and RAM
 - CPU and HARSDIK
 - RAM and ROM
 - None of the above
220. Write Through technique is used in which memory for updating the data:
- Virtual memory
 - Auxiliary memory
 - Main memory
 - Cache memory
221. Generally Dynamic RAM is used as main memory in a computer system as it
- Consumes less power
 - Has lower cell density
 - Has higher speed
 - Needs refreshing circuitry
222. In signed-magnitude binary division, if the dividend is $(11100)_2$ and divisor is $(1001)_2$, then the result is
- $(00100)_2$
 - $(11001)_2$
 - $(10100)_2$
 - $(01100)_2$
223. Virtual memory consists up:
- Static RAM
 - Magnetic memory
 - Dynamic RAM
 - None of the above
224. In a program using subroutine call instruction, it is necessary
- Initialize program counter
 - Reset the microprocessor
 - Clear the accumulator
 - Clear the instruction register
225. When CPU is executing a Program that is part of the Operating System, it is said to be in
- Interrupt mode
 - Half mode
 - System mode
 - Simplex mode
226. A Flip Flop can be converted into T-Flip Flop by using additional logic circuit
- $A = T, Q_n$
 - $D = T, Q_n$
 - $C, D = T$
 - $D = T \bar{A} Q_n$
227. Logic X-OR operation of $(4AC0)_{16}$ & $(B53F)_{16}$ results
- $AACB$
 - $FFFF$
 - 0000
 - $ABCD$
228. An n-bit microprocessor has
- n-bit program counter
 - n-bit ALU
 - n-bit address register
 - n-bit instruction register
229. Cache memory works on the principle of:
- Locality of data
 - Locality of reference
 - Locality of memory
 - Locality of reference and memory
230. The main memory in a Personal Computer (PC) is made of:
- Cache memory
 - Dynamic RAM
 - Static RAM
 - Both A and B
231. The circuit converting binary data in to decimal is
- Encoder
 - Decoder
 - Multiplexer
 - Code converter
232. PSW is saved in stack when there is a
- Interrupt recognized
 - Execution of CALL instruction
 - Execution of RST instruction
 - All of these
233. A combinational logic circuit which sends data coming from a single source to two or more separate destinations is:
- Decoder
 - Multiplexer
 - Encoder
 - Demultiplexer
234. In which addressing mode the operand is given explicitly in the instruction:
- Absolute
 - Indirect
 - Immediate
 - Direct
235. The gray code equivalent of $(1011)_2$ is
- 1101
 - 1110
 - 1010
 - 1111

236. A system program that translates and executes an instruction simultaneously is:
 A. Compiler
 B. Assembler
 C. Interpreter
 D. Operating system
237. When necessary, the results are transferred from the CPU to main memory by
 A. I/O devices
 B. Shift registers
 C. CPU
 D. None of the above
238. A successive A/D converter is:
 A. A medium speed converter
 B. A low speed converter
 C. A high-speed converter
 D. None of these
239. The memory unit that communicates directly with the CPU is called the
 A. Main memory
 B. Shared memory
 C. Secondary memory
 D. Auxiliary memory
240. The average time required to reach a storage location in memory and obtains its content is called:
 A. Latency time
 B. Turnaround time
 C. Access time
 D. Response time
241. A k-bit field can specify:
 A. 3^k register B. K^2 register
 C. 2^k register D. K^3 register
242. The time interval between the adjacent bits is called:
 A. Word-time
 B. Turnaround time
 C. Bit-time
 D. Slice time
243. A group of bits that tell the computer to perform a specific operation is known as:
 A. Instruction code
 B. Accumulator
 C. Micro-operation
 D. Register
244. The load instruction is mostly used to designate a transfer from memory to a processor register known as:
 A. Accumulator
 B. Program counter
 C. Instruction register
 D. Memory address register
245. The communication between the components in a microcomputer takes place via:
 A. I/O bus B. Address bus
 C. Data bus D. Control lines
246. An instruction pipeline can be implemented by means of:
 A. LIFO buffer B. Stack
 C. FIFO buffer D. None of above
247. Data input command is just the opposite of a:
 A. Test command
 B. Data output
 C. Control command
 D. Data channel
248. The operation executed on data stored in registers is called:
 A. Macro-operation
 B. Bit-operation
 C. Micro-operation
 D. Byte-operation
249. MRI indicates:
 A. Memory Reference Information
 B. Memory Register Instruction
 C. Memory Reference Instruction
 D. Memory Register Information
250. Self-contained sequence of instructions that performs a given computational task is:
 A. Function B. Sub routine
 C. Procedure D. Routine
251. Microinstructions are stored in control memory groups with each group specifying a:
 A. Routine B. Vector
 C. Subroutine D. Address
252. An interface that provides a method for transferring binary information between internal storage and external devices is called:
 A. I/O interface
 B. Output interface
 C. Input interface
 D. I/O bus
253. Status bit is also called:
 A. Binary bit B. Signed bit
 C. Flag bit D. Unsigned bit
254. An address in main memory is called:
 A. Physical address
 B. Memory address
 C. Logical address
 D. Word address
255. If the value $V(x)$ of the target operand is contained in the address field itself, the addressing mode is:
 A. Immediate B. Indirect
 C. Direct D. Implied
256. (-27)₁₀ can be represented in a signed magnitude format and in a 1's complement format as:
 A. 111011 & 100100
 B. 011011 & 100100
 C. 100100 & 111011
 D. 100100 & 011011
257. The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called:
 A. Data transfer instructions
 B. Input-output instructions
 C. Program control instructions
 D. Logical instructions
258. A device/circuit that goes through a predefined sequence of states upon the application of input pulses is called:
 A. Register B. Transistor
 C. Flip-flop D. Counter
259. The performance of cache memory is frequently measured in terms of a quantity called:
 A. Miss ratio B. Latency ratio
 C. Hit ratio D. Read ratio
260. The information available in a state table may be represented graphically in a:
 A. Simple diagram
 B. Complex diagram
 C. State diagram
 D. Data flow diagram
261. Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called:
 A. Relative address mode
 B. Register mode
 C. Index addressing mode
 D. Implied mode
262. An interface that provides I/O transfer of data directly to and from the memory unit and peripheral is termed as:
 A. DDA B. BR
 C. Serial interface D. DMA

263. The 2's compliment form (Use 6-bit word) of the number 1010 is
 A. 111100 B. 110111
 C. 110110 D. 1011
264. A register capable of shifting its binary information either to the right or the left is called a:
 A. Parallel register B. Shift register
 C. Serial register D. Storage register
265. What is the content of stack pointer (SP)?
 A. Address of current instruction
 B. Address of the next instruction
 C. Address of the top element of the stack
 D. Size of the stack
266. Which of the following interrupt is non-maskable?
 A. INTR B. RST 6.5
 C. RST 7.5 D. TRAP
267. Which of the following is a main memory?
 A. Secondary memory
 B. Cache memory
 C. Auxiliary memory
 D. Virtual memory
268. Which of the following are not a machine instruction?
 A. MOV B. END
 C. ORG D. Both B and C
269. In Assembly language programming, minimum number of operands required for an instruction is/are
 A. Zero B. Two
 C. One D. Both B and C
270. The maximum addressing capacity of a microprocessor which uses 16-bit database & 32-bit address base is:
 A. 64 K
 B. Both A and B
 C. 4 GB
 D. None of the above
271. A combinational logic circuit which sends data coming from a single source to two or more separate destination is:
 A. Decoder B. Multiplexer
 C. Encoder D. Demultiplexer
272. A Program Counter contains a number 825 and address part of the instruction contains the number 24. The effective address in the relative address mode, when an instruction is read from the memory is:
 A. 849 B. 801
 C. 850 D. 802
273. A system program that translates and executes an instruction simultaneously is:
 A. Compiler
 B. Assembler
 C. Interpreter
 D. Operating system
274. The cache memory of 1K words uses direct mapping with a block size of 4 words. How many blocks can the cache accommodate?
 A. 256 words B. 1024 words
 C. 512 words D. 128 words
275. Logic gates with a set of input and outputs is arrangement of:
 A. Combinational circuits
 B. Design circuits
 C. Logic circuit
 D. Register
276. The BSA instruction is:
 A. Branch and store accumulator
 B. Branch and shift address
 C. Branch and save return address
 D. Branch and show accumulator
277. A floating-point number that has an O in the MSB of mantissa is said to have:
 A. Overflow
 B. Important number
 C. Underflow
 D. Undefined
278. Aging registers are:
 A. Counters which indicate how long ago their associated pages have been referenced
 B. Registers which keep track of when the program was last accessed
 C. Counters to keep track of last accessed instruction
 D. Counters to keep track of the latest data structure referred.
279. The instruction "ORG 0" is a:
 A. Machine instruction
 B. High level instruction
 C. Pseudo instruction
 D. Memory instruction
280. Translation from symbolic program into binary is done in:
 A. Two passes B. Three passes
 C. Directly D. Four passes
281. To put the microprocessor in the wait state
 A. Lower the HOLD input
 B. Raise the HOLD input
 C. Lower the READY input
 D. Raise the READY input
282. A basic instruction that can be interpreted by a computer generally has:
 A. An operand and an address
 B. Sequential register and decoder
 C. A decoder and an accumulator
 D. An address and decoder
283. In a microprocessor system with memory mapped I/O:
 A. Devices have 8-bit addresses
 B. Devices are accessed using IN and OUT instructions
 C. There can be a maximum of 256 input devices
 D. Arithmetic and logic operations can be directly performed with the I/O data
284. Which of the following information holds the information before going to the decoder?
 A. Control register B. Accumulator
 C. Data register D. Address register
285. The device which is used to connect a peripheral to bus is called.....
 A. Control register
 B. Communication
 C. Interface
 D. None of these
286. Which of the following is the set of general-purpose internal registers?
 A. Stack
 B. Address register
 C. Scratch pad
 D. Status register
287. The register used as a working area in CPU is.....
 A. Program counter
 B. Instruction decoder
 C. Instruction register
 D. Accumulator
288. Which of the following is used as storage location both in the ALU and the control section of a computer?
 A. Accumulator B. Adder
 C. Register D. Decoder

289. The register which holds the address of the location to or from which data are to be transferred is called...
- Index register
 - Memory address register
 - Instruction register
 - Memory data register
290. The register which contains the data to be written into or read out of the address location is called?
- Memory address register
 - Program counter
 - Memory data register
 - Index register
291. Which of the following register is used in the control unit of the CPU to indicate the next instruction which is to be executed?
- Accumulator
 - Instruction decoder
 - Index register
 - Program counter
292. An interrupt can be temporarily ignored by counter is called?
- Vectored interrupt
 - Maskable interrupt
 - Non-maskable interrupt
 - Low priority interrupt
293. The ability to temporarily halt the CPU and used this time to send information on buses is called...
- Direct memory access
 - Polling
 - Vectoring the interrupt
 - Cycle stealing
294. Number of machine cycle required for RET instruction in 8085 microprocessors is.....
- One
 - Three
 - Two
 - Five
295. In a microprocessor system, the RST instruction will cause an interrupt if
- Only if an interrupt service routine is not being executed
 - Only if a bit in the interrupt mask is made zero
 - Only if interrupt have been enabled by an EI instruction
 - None of the above
296. An instruction used to set the carry flag in a computer can be classified as;
- Data transfer group
 - Logical
 - Process control
 - Program control
297. Microprocessor 8085 is the enhanced version ofwith essentially the same construction set.
- 6800
 - 8080
 - 68000
 - 8000
298. In a generic microprocessor instruction cycle time is:
- Shorter than machine cycle time
 - Larger than machine cycle time
 - Exactly double the machine cycle time
 - Exactly same as the machine cycle time
299. If we use 3 bits in the instruction word to indicate if an index register is to be used and if necessary, which one is to be used, and then the number of index register to be used in the machine will be.....
- Three
 - Seven
 - Six
 - Eight
300. In a multi-processor configuration, two processor are connected to the host 8086 processor. The two-processor instruction set.....
- Must be the same
 - Must be disjoint
 - May overlap
 - Must be the same as that of the host
301. A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor?
- Pointers
 - Records
 - Arrays
 - All of the above
302. The 8085 microprocessor responds to the presence of an interrupt
- As soon as the TRAP pin becomes high
 - By checking the TRAP pin for high status at the end of each instruction fetch
 - By checking the TRAP pin for high status at the end of the execution of each instruction
 - By checking the TRAP pin for high status at regular intervals
303. Which of the following need not necessarily be saved on a context switch between processes?
- General purpose registers
 - Program counter
 - Translation look aside buffer
 - All of these
304. If a processor does not have any stack pointer register then...
- It cannot have subroutine call instruction
 - It can have subroutine call instruction, but no nested subroutine calls
 - Nested subroutine calls are possible, but interrupts are not
 - All sequence of subroutine calls and also interrupts are possible
305. CPU has two modes-privileged and non-privileged. In order to change the mode from privileged to non-privileged
- A hardware interrupt is needed
 - A software interrupt is needed
 - A privileged instruction (which does not generate an interrupt) is needed
 - A non-privileged instruction (which does not generate an interrupt) is needed
306. In the absolute addressing mode
- An operand is inside the instruction
 - Address of the operand is inside the instruction
 - Register containing the address of the operand is specified inside the instruction
 - Location of the operand is implicit
307. The capacity of program counter (PC) is....
- 8 bits
 - 16 bits
 - 12 bits
 - 32 bits
308. The function of program counter (PC) holds
- Temporary
 - Memory operand
 - Address for memory
 - Address for instruction
309. The Program Counter (PC).....
- Is a register
 - During execution of the current instruction, its content changes
 - Both (A) and (B)
 - None of the above
310. The TRAP interrupt mechanism of the 8085 microprocessor executes
- An RST by hardware
 - The instructions supplied by external device through the INTA signal
 - An instruction from memory location 20H
 - None of the above

- 311. Pseudo-instructions are:**
- Assembler directives
 - Instructions in any program that have no corresponding machine code instruction
 - Instruction in any program whose presence or absence will not change the output for any input
 - None of the above
- 312. *The number of instructions needed to add 'n' numbers and store the result in memory using only one address instructions is:**
- n
 - n-1
 - n+1
 - Independent of n
- [Hint:** A typical one address instructions use that address to specify one operand. The other operand will be in the accumulator by default. So, to add "n" given numbers, a1, a2... an, first transfer a1 to accumulator. Next, the instruction ADD a2- adds the content of a2 to the accumulator and leaves the sum there. Continuing this way, we need "n" instructions to add "n" numbers and place the result in the accumulator. Finally, to store the result in memory 1 more instructions is needed. So, (n+1) instructions are needed.
- 313. The addressing mode used in the instruction PUSH B is....**
- Direct
 - Register indirect
 - Register
 - Immediate
- 314. The process of fetching and executing instructions one at a time, in order to increasing an address is called....**
- Instruction execution
 - Instruction fetch
 - Straight line sequencing
 - Random sequencing
- 315. The CPU of a computer takes instruction from the memory and executes them. This process is called.....**
- Load cycle
 - Fetch-execute cycle
 - Time sequence
 - Clock cycle
- 316. In a microprocessor, WAIT states are used to.....**
- Make the processor wait during a DMA operation
 - Make the processor wait during a power interrupt processing
 - Make the processor wait during a power shutdown
 - Interface slow peripheral to the processor
- 317. When a program is being executed in an 8085 microprocessor, its program counter contains**
- Number of instructions in the current program that have already been executed
 - The total number of instructions in the program being executed
 - Memory address of the instructions that is being currently executed
 - Memory address of the instructions that is to be executed next.
- 318. When the HLT instructions of an 8085 microprocessor is executed, the microprocessor**
- Is disconnected from the system bus till the reset is pressed
 - Halt execution of the program and returns to monitor
 - Enters into a halt-state and the buses are tri-stated
 - Reloads the program from the location 0024 and 0025
- 319. Serial input data of 8085 can be loaded into bit 7 of the accumulator by.....**
- Executing a RIM instruction
 - Using TRAP
 - Executing RST 1
 - None of the above
- 320. Which of the following interrupts are unmaskable interrupts?**
- RST 5.5
 - TRAP
 - RST 7.5
 - INTR I
- 321. The memory address ranges to which RAM will respond.....**
- 0000 H to 1 FFF H
 - 4000 H to 5 FFF H
 - 0000 H to 5 FFF H
 - 3000 H to FFFF H
- 322. The address range to which I/O chip will respond is.....**
- 0000 H to FFFF H
 - 4000 H to 5FFF H
 - 0000H to 5FFFH
 - 3000 H to FFFF H
- 323. Both the arithmetic logic unit (ALU) and control section of CPU employ special purpose storage location called**
- Decoder
 - Multiplexer
 - Buffers
 - Registers
- 324. A basic instruction that can be interpreted by a computer generally has**
- An operand and an address
 - Sequence register and decoder
 - A decoder and an accumulator
 - An address and decoder
- 325. The differences between PLA and ROM is**
- PLA is combination ROM is sequential
 - PLA economizes on the number of minterms
 - PLA has fixed AND array, ROM has fixed OR array
 - None of these
- 326. The control unit of computer**
- Performs ALU operations on the data devices
 - Controls the operation of the output devices
 - Is a device for manually operating the computer?
 - Directs the other unit of computers
- 327. The ALU of a computer normally contains a number of high-speed storage elements called**
- Semiconductor memory
 - Hard disk
 - Registers
 - Magnetic disks
- 328. The unit of a computer system which executes program, communication with and often controls the operation of other subsystems of the computer is the**
- CPU
 - Flo unit
 - Control unit
 - Peripheral unit
- 329. The ability of a medium size computer system to increase in data processing capability by addition of such devices as mass storage device, I/O device etc. is called**
- Computer expandability
 - Computer enhancement
 - Computer mobility
 - Computer upward capability

330. The technique which repeatedly uses the same block of internal storage during different stage of problem is called
 A. Overlay B. Swapping
 C. Overlapping D. Reuse
331. The registers used as a working area in CPU is
 A. Program counter
 B. Instruction decoder
 C. Instruction register
 D. Accumulator
332. Which of the following information holds the information before going to the decoder?
 A. Control register B. Accumulator
 C. Data register D. Address register
333. Which of the following unit is used to supervise each instruction in the CPU?
 A. Control logic unit
 B. ALU
 C. Accumulator
 D. Control register
334. The bus which is used to transfer data from main memory to peripheral device is
 A. Data bus B. DMA bus
 C. Input bus D. Output bus
335. The device which is used to connect a peripheral to bus is called
 A. Control register
 B. Communication protocol
 C. Interface
 D. None of these
336. The bus connected between the CPU and main memory that permits transfer of information between main memory and the CPU is called
 A. DMA bus B. Address bus
 C. Memory bus D. Control bus
337. What is the storage capacity of a Hollerith card which is organized into nibbles?
 A. 32 B. 120
 C. 64 D. 240
338. How many addresses are required for 25x40 video RAM?
 A. 1020 B. 1000
 C. 1920 D. 2000
339. Microprogramming is a technique for
 A. Writing small program effectively
 B. Programming output/input routines
 C. Programming the microprocessor
 D. Programming the control steps of a computer
340. A device that works in conjunction with a computer but not as part of it is called
 A. Microprocessor B. Hardware
 C. Peripheral device D. Memory
341. A system of letters, numbers symbols adopted by computer manufacturer as an abbreviation form of instruction sets is called
 A. Mesh B. Modern
 C. Monitor D. Mnemonic
342. When a subroutine is called, then address of the instruction following the CAL instruction is stored in/on the
 A. Stack pointer
 B. Program counter
 C. Accumulator
 D. Stack
343. In 8085 microprocessors, the value of the most significant bit of the result following the execution of any arithmetic or Boolean instruction is stored in the
 A. Carry status flag
 B. Sign status flag
 C. Auxiliary carry status flag
 D. Zero status flag
344. PLA
 A. Produces sum of products as the outputs
 B. Is dedicated for a particular operation
 C. Is general
 D. Both A and B
345. The sequence of events that happen during a typical fetch operation is
 A. PC-MAR-Memory-MDR-IR
 B. PC-Memory-IR
 C. PC-Memory-MDR-IR
 D. PC-MAR-Memory-IR
346. Which of the following is not a form of memory?
 A. Instruction cache
 B. Instruction opcode
 C. Instruction register
 D. Translation lookaside buffer
- [HINT: Explanation: Instruction Cache – Used for storing instructions that are frequently used
 Instruction Register – Part of CPU's control unit that stores the instruction currently being executed.
 Instruction Op code – It is the portion of a machine language instruction that specifies the operation to be performed
 Translation Lookaside Buffer – It is a memory cache that stores recent translations of virtual memory to physical addresses for faster access. So, all the above except Instruction Op code are memories. Thus, C is the correct choice.]
347. Which memory is difficult to interface with processor?
 A. Static memory
 B. ROM
 C. Dynamic memory
 D. RAM
348. Desirable characteristic(s) of a memory system is/are
 A. Speed and reliability
 B. Durability and compactness
 C. Low power consumption
 D. All of these
349. The minimum time delay required between initiation of two successive memory operation is called
 A. Memory cycle time
 B. Transmission time
 C. Memory access time
 D. Skip time
350. Which of the following statement is wrong?
 A. RAM is a type of volatile
 B. Magnetic tape is non-volatile
 C. Magnetic core and semiconductor memories are used as mass memory medium
 D. An EPROM can be programmed, erased and reprogrammed by user with an EPROM programming instruction
351. The refreshing rate of dynamic RAMs is approximately once in
 A. Two micro seconds
 B. Fifty milli seconds
 C. Two milli seconds
 D. Two seconds
352. In comparison with static RAM memory, the dynamic RAM memory has
 A. Lower bit density and higher power consumption
 B. Higher bit density and higher power consumption
 C. Lower bit density and lower power consumption
 D. Higher bit density and lower power consumption

353. Disadvantage of dynamic RAM over static RAM is

- A. Higher power consumption
- B. Variable speed
- C. Need to refresh the capacitor charge every once in two milliseconds
- D. Higher bit density

354. The access time of magnetic bubble memory is approximately

- A. 30 nano seconds
- B. 30 milli seconds
- C. 30 micro seconds
- D. 0.3 seconds

355. Serial access memories are useful in applications where

- A. Data consists of number
- B. Short access time is required
- C. Each stored word is processed differently
- D. Data naturally needs to flow in and out in serial form

356. What is the main advantage of magnetic core memory over semiconductor RAM memory?

- A. More compact and smaller
- B. More economical
- C. A bit does not have to be written after reading
- D. Non-volatile

357. Fastest types of memory from the following list is

- A. Tape
- B. Disk
- C. Semiconductor
- D. Bubble memory

358. The use of hardware in Memory management is through segment relocation and protection is

- A. To perform address translation to reduce size of the memory
- B. To perform address translation to reduce execution time overhead
- C. Both A and B
- D. None of these

359.

359. Memory refreshing may be done by the CPU that contains a special regressive counter, only

- B. By an external refresh counter, only
- C. Either by CPU or by an external refresh counter
- D. None of the above

360. Choose the correct statement from the following:

- A. PROM contains a programmable AND array and a fixed OR array
- B. PLA contains a fixed AND array and a programmable OR array
- C. PROM contains a fixed AND array and a programmable OR array
- D. None of the above

361. Which of the following is not true of primary storage?

- A. It represents the decimal number through string of binary digits
- B. It stores operating system program
- C. It stores data while they are being processed by CPU
- D. It stores the bulk of data used by computer application

362. A dynamic RAM consist up:

- A. Six transistors
- B. One transistor and one capacitor
- C. Two transistors and two capacitors
- D. Two capacitors only

363. Semiconductor memory is:

- A. Somewhat slower than magnetic core memory
- B. A volatile memory
- C. Somewhat longer than magnetic core memory
- D. All of the above

364. Which of the following is the internal memory of the system (computer)?

- A. CPU registers
- B. Main memory
- C. Cache memory
- D. All of the above

365. A software program stored in a ROM that cannot be changed easily is called.....

- A. Hardware
- B. Editor
- C. Linker
- D. Firmware

366. An advantage of memory interfacing is that:

- A. A large memory is obtained
- B. Effective speed of the memory is increased
- C. The cost of the memory is reduced
- D. Non volatile memory is obtained

367. In a virtual memory system, the address space specified by the address line of the CPU must bethan the physical memory size andthan the secondary storage size.

- A. Smaller, smaller
- B. Larger, smaller
- C. Smaller, larger
- D. Larger, larger

368. Which of the following is /are advantage of virtual memory?

- A. Faster access to memory on an average
- B. Processes can be given protected address space
- C. Both A and B
- D. Program larger than the physical memory size can be run

369. Which of the following need extra hardware for DRAM refreshing?

- A. 8085
- B. Motorola 68000
- C. Both (A) and (B)
- D. None of the above

370. Nonvolatile is an important advantage of.....

- A. CCD's
- B. Magnetic bubbles
- C. RAM
- D. PROM

371. Memory consisting of electronic circuit attached into silicon chip is known as:

- A. Magnetic core memory
- B. Thin film memory
- C. Semiconductor memory
- D. MOS memory

372. Which of the following memory is capable of operating at electronic speed?

- A. Semiconductor memory
- B. Magnetic drums
- C. Magnetic disks
- D. Magnetic tapes

373. The larger the RAM of a computer, the faster is its speed, since it eliminates

- A. Need of ROM
- B. Frequency disk I/O
- C. Need for external memory
- D. Need for a data-wide path

374. What is the average access time for a drum rotating at 4000 revolution per minute?

- A. 2.5 milli seconds
- B. 7.5 milli seconds
- C. 5.0 milli seconds
- D. 4.0 milli seconds

375. How many input lines are needed to construct 1024-bit coincident core plan?

- A. 10
- B. 32
- C. 16
- D. 64

376. What is the byte capacity of a drum which is 5-inch-high, 10-inch diameter, and which has 60 racks per inch bit density of 800 bits per inch?
A. 942000 bytes
B. 188400 bytes
C. 471000 bytes
D. 16384 bytes

377. The main advantage of multiple bus organization over single bus is,
A. Reduction in the number of cycles for execution
B. Increase in size of the registers
C. Better Connectivity
D. None of these

378. Property of locality of reference may fail, if a program has
A. Many conditional jumps
B. Many operand
C. Many unconditional jumps
D. All of the above

379. How many RAM chips of size (256x1 bit) are required to build 1M byte memory?
A. 8 B. 24
C. 10 D. 32

380. If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4x6 array, where each chip is 8K x 4 bits?
A. 13 B. 16
C. 15 D. 17

381. Four memory chips of 16x4 size have their address bases connected together. The system will be of size
A. 64x64 B. 32x8
C. 16x16 D. 256x1

382. Arrange the following for CPU in decreasing operating speeds:

- A. Hard wired control, vertical programming, horizontal programming
- B. Hard wired control, micro-programming, vertical programming
- C. Horizontal micro-programming, vertical micro-programming, wired control
- D. Vertical micro-programming, horizontal micro-programming, wired control

383. The main difference (a) between CISC and a RISC processor is that a RISC processor typically

- A. Has fewer instructions addressing modes
- B. Has more registers
- C. Is easier to implement using wired control logic
- D. All of the above

384. Comparing the time T1 taken for single instruction on a pipelined CPU with time T2 taken on a non-pipelined identical CPU, we can say that
A. T1=T2
B. T1>T2
C. T1<T2
D. T1 is T2 plus time taken for instruction fetch cycle

385. Performance of a pipelined processor suffers if

- A. The pipeline stages have different delays
- B. Consecutive instructions dependent on each other
- C. The pipeline stages share hardware resources
- D. All of the above

386. A micro-programmed control unit

- A. Is faster than a hard-wired control unit
- B. Facilitates easy implementation of new instruction
- C. Is useful when very small programs are to be run
- D. Usually refers to the control unit of a microprocessor

387. Which of the following are typical characteristics of a RISC machine?

- A. Highly pipelined
- B. Multiple register sets
- C. Both (A) and (B)
- D. None of these

388. In an 8085-microprocessor system with memory mapped I/O

- A. I/O device have 8-bit addresses
- B. I/O devices are accessed using IN and OUT instruction
- C. There can be a maximum of 256 input devices and 256 output devices
- D. Arithmetic and logic operations can be directly performed with the I/O data

389. How many types of storage loops exist in magnetic bubble memory?

- A. 8 B. 3
C. 4 D. 2

390. How many wires are threaded through the cores in a coincident current core memory?

- A. 2 B. 4
C. 3 D. 6

391. When we move from the outermost track to the innermost track in a magnetic disk, then density (bits per linear inch)

- A. Increases
- B. Remains the same
- C. Decreases
- D. Either remains constant or decreases

392. The use of hardware in Memory management is through segment relocation and protection is

- A. To perform address translation to reduce size of the memory
- B. To perform address translation to reduce execution time overhead
- C. Both A and B
- D. None of the above

393. The parallel operation is preferred because

- A. Circuitry is simple
- B. It is faster than series operation
- C. It requires less memory
- D. All of the above

394. In comparison to the internal (main) memory, tape or disk memory is

- A. Slower and more expensive
- B. Faster and more expensive
- C. Slower and less expensive
- D. Faster and less expensive

395. The number of records contained within a block of data on magnetic tape is defined by the

- A. Block definition
- B. Blocking factor
- C. Record contain clause
- D. Record per block factor

396. Transfer of information from main storage is typically n times faster than the transfer from auxiliary storage, where n is about

- A. 5 B. 100
C. 10 D. 200

397. Which access method is used for obtaining a record from a cassette tape?

- A. Direct B. Random
C. Sequential D. Parallel

- 398. An advantage of blocking a tape is that**
- The additional processing time is consumed
 - The direct file method can be emulated
 - The tapes contains less data and longer tapes
 - Less tape is used to store the same amount of data
- 399. The ISA standard Buses are used to connect.**
- RAM and processor
 - Hard disk and Processor
 - GPU and processor
 - CD/DVD drives and Processor
- 400. Which of the following is not true of primary storage?**
- It represents the decimal number through string of binary digits.
 - It stores operating system programs
 - It stores data while they are being processed by CPU.
 - It stores the bulk of data used by computer application
- 401. In modern computers bipolar semiconductor chips are often used in the arithmetic logic unit. What material is used for the slower and less expensive primary storage section?**
- Gallium arsenide (GaAs)
 - Silicon
 - Metal oxide semiconductor
 - Gallium arsenide chips
- 402. Which type of memory chips are likely to be used in the primary storage of the future generation of computers?**
- Selenium chips
 - Bio chips
 - Optical chips
 - Gallium arsenide chips
- 403. How many bits can be stored in the capital?**
- 8000
 - 4000
 - 8192
 - 4096
- 404. If a computer has a 1024 K memory, then what does the letter K stands for?**
- Kilometer
 - 1024
 - Thousand
 - Core
- 405. What was the amount of memory required by the earliest operating system called dos 1.0?**
- 4K
 - 16K
 - 8K
 - 32K
- 406. The storage device which is used to compensate for the difference in rates of flow of data from one device to another is called**
- Cache
 - Buffer
 - Concentrator
 - I/O device
- 407. As a secondary storage medium, what is the most important advantage of a video disk?**
- Laser disk
 - Durability
 - Potential capacity
 - Cost effectiveness
- 408. What is the size of optical compact disk which is used for recording high quality music?**
- 4.7-inch
 - 5½ inch
 - 3½ inch
 - 8 inch
- 409. Which part of the diskette never be touched?**
- Hub
 - Oval slot
 - Ole in the center
 - Corner
- 415. The seek time of a disk is 30 ms. It rotates at the rate of 30 rotations /second. The capacity of each track is 300 words. The access time is (approximately)**
- 62 ms
 - 50 ms
 - 60 ms
 - 47 ms
- 416. How many RAM chips of size (256K x 1 bit) are required to build 1 M byte memory?**
- 8
 - 24
 - 10
 - 32
- 417. If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4 x 6 array, where each chip is 8K x 4 bits?**
- 13
 - 16
 - 15
 - 17
- 418. In a memory system, four 256 x 8 PROM chips are used to make total memory of size 1024 x 4. What is the number of address bus lines?**
- 4
 - 10
 - 8
 - 16
- 419. Consider a high speed 40 ns memory cache with a successful hit ratio of 80%. The regular memory has an access time of 100 ns. What is the average effective time for CPU to access memory?**
- 52 ns
 - 70 ns
 - 60 ns
 - 80 ns
- 420. What is the hit ratio of a cache if a system performs memory access at 30 nano seconds with the cache and 150 nano seconds without it? Assume that the each uses 20 nano sec memory, choose the closest approximate**
- 81%
 - 92%
 - 75%
 - 87%

421. Consider a disk with the following characteristics

Track size: 10,000 bytes

Rotational latency: 10 ms / revaluation

Block size: 1,000 bytes

What is the maximum transfer rate per track measured in bits per second as is conventional for this disk unit?

- A. 400 Mbps
- B. 6,400 Mbps
- C. 8 Mbps
- D. 4,250 Mbps

422. Increasing the RAM of a computer typically improves the performance because:

- A. Virtual memory increases
- B. Larger RAMs are faster
- C. Fewer page faults occurs
- D. Fewer segmentation faults occur

423. Which of the following requires a device driver?

- A. Register
- B. Cache
- C. Main memory
- D. Disk

424. Which one of the following statements is false?

- A. Virtual memory implements the translation of a programs address space into physical memory address
- B. Virtual memory allows each program to exceed the size of the primary memory
- C. Virtual memory increases the degree of multiprogramming
- D. Virtual memory reduces the context switching overhead

425. The advantage of CMOS technology over a MOS is

- A. Lower power dissipation
- B. Greater speed
- C. Smaller chip size
- D. All of the above

426. The advantage of synchronous circuits over asynchronous one is...

- A. Faster operation
- B. Better noise immunity
- C. Both A and B
- D. Lower hardware equipment

427. Which of the following is not a form of memory?

- A. Instruction cache
- B. Instruction register
- C. Instruction code
- D. Translation lookaside buffer

428. In 2's complement, addition overflow

- A. Is tagged whenever there is a carry for sign bit addition
- B. Cannot occur when a positive value is added to a negative value
- C. Is flagged when the carries from sign bit and previous bit match
- D. None of the above

429. The performance of the pipelined processor suffers if...

- A. The pipeline stage has different delay
- B. Consecutive instructions depend on each other
- C. The pipeline stages share hardware resources
- D. All of the above

430. In absolute addressing mode...

- A. The operand is inside the instruction
- B. The address of the operand is inside the instruction
- C. The register containing the address of the operand is specified in the instruction
- D. Location of the operand is implicit

431. A processor needs software interrupt to

- A. Test the interrupt system of the processor
- B. Implement co routines
- C. Obtain system services which need execution of privileged instructions
- D. Return from subroutine

432. Horizontal microprogramming...

- A. Does not require use of signal decoders
- B. Results in larger sized micro-instructions than vertical micro-programming
- C. Use one bit for each control signal
- D. All of the above

433. The main difference (s) between a CISC and RISC processor is/are that a RISC processor typically has

- A. A fewer instruction
- B. A fewer addressing mode
- C. A more register, an ease to implement using hardwired control logic
- D. All of the above

434. The exponent of a floating-point number is represented in excess -N code so that

- A. The dynamic range is large
- B. The precision is high
- C. The smallest number is represented by all zeros
- D. Overflow is avoided

435. If negative numbers are stored in 2's complement form, the range of numbers that can be stored in 8 bits is.....

- A. -128 to +128
- B. -128 to +127
- C. -127 to +128
- D. -127 to +127

436. On receiving an interrupt from an I/O device, the CPU

- A. Halts for a pre-determined time
- B. Hands over control of address bus and data bus to the interrupting device
- C. Branches off to the interrupt service routine immediately
- D. Branches off to the interrupt service routine after completion of the current instruction

437. In serial communication, an extra clock is needed

- A. To synchronize the devices
- B. For programmed baud rate control
- C. To make efficient use of RS-232
- D. None of the above

438. Which of the following rules regarding the addition of 2 given numbers is correct, if negative numbers are represented in 2's complement form?

- A. Add sign bit and discard carry, if any
- B. Add sign bit and add carry, if any
- C. Don't add sign bit and discard carry, if any
- D. Don't add sign bit and add carry, if any

439. The difference between 80486 and 80386 is/are...

- A. Presence of floating-point co-processor
- B. Speed of operation
- C. Presence of 8 K cache on chip, presence of memory controller
- D. All of the above

440. In virtual memory system, the addresses used by the programmer belongs to

- A. Memory space
- B. Physical addresses
- C. Address space
- D. Main memory address

441. The method for updating the main memory as soon as word is removed from the cache is called

- A. Write-through
- B. Write-back
- C. Protected-write
- D. Cache write

442. Which is true for a typical RISC architecture?

- A. Micro programmed control unit
- B. Instruction takes multiple clock cycle
- C. Have fewer register in CPU
- D. Emphasis on optimizing instruction pipelines.

443. After reset, CPU begins execution of instruction from memory address

- A. 0101H
- B. 8000H
- C. 0000H
- D. FFFFH

444. In 8085 microprocessors how many I/O devices can be interfaced in I/O mapped I/O technique?

- A. Either 256 input devices or 256 output devices.
- B. 256 I/O devices.
- C. 256 input devices & 256 output devices.
- D. 512 input-output devices.

445. DMA interface unit eliminates the need to use CPU registers to transfer data from

- A. MAR to MBR
- B. I/O units to memory
- C. MBR to MAR
- D. Memory to I/O units

446. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

- A. 8
- B. 16
- C. 24
- D. 32

447. What is the bit storage capacity of a ROM with a 512¹ 4-organization?

- A. 2049
- B. 2048
- C. 2047
- D. 2046

448. How many different addresses are required by the memories that contain 16K words?

- A. 16,380
- B. 16,382
- C. 16,384
- D. 16,386

449. The content of a 4-bit register is initially 1101. The register is shifted 2 times to the right with the serial input being 1011101. What is the content of the register after each shift?

- A. 1110, 0111
- B. 0001, 1000
- C. 1101, 1011
- D. 1001, 1001

450. ABCD - seven segment decoder / driver is connected to an LED display. Which segments are illuminated for the input code DCBA = 0001?

- A. b,c
- B. c,b
- C. a,b,c
- D. a,b,c,d

451. Address symbol table is generated by

- A. Memory management software
- B. Assembler
- C. Match logic of associative memory
- D. Generated by operating system

452. When an instruction is read from the memory, it is called

- A. Memory read cycle
- B. Fetch cycle
- C. Instruction cycle
- D. Memory write cycle

453. Which activity does not take place during execution cycle?

- A. ALU performs the arithmetic and logical operation
- B. Effective address is calculated
- C. Next instruction is fetched
- D. Branch address is calculated and branching conditions are checked

454. The time for which the D-input of a D-FF must not change after the clock is applied is known as

- A. Hold time
- B. Set-up time
- C. Transition time
- D. Delay time

455. How many memory chips of (128 x 8) are needed to provide a memory capacity of 4096 x 16?

- A. 64
- B. 16
- C. 32
- D. 128

[Hint: Chip size 128 x 8, 8 bits = 1 byte. To find for 4096 x 16 memory capacity. So now, each chip has 64 x 1 byte = 64]

456. In addition of two signed numbers, represented in 2's complement form generates an overflow if

- A. A = B = 0
- B. A = 0
- C. A = B = 1
- D. A + B = 1

457. In DMA the data transfer is controlled by....

- A. Microprocessor
- B. RAM
- C. Memory
- D. I/O devices

458. Synchronous means....

- A. At irregular intervals
- B. At same time
- C. At variable time
- D. None of the above

459. Excess-3 equivalent representation of (1234) H is

- A. (1237) Ex-3
- B. (4567) Ex-3
- C. (7993) Ex-3
- D. (4663) Ex-3

460. Which of the memory holds the information when the Power Supply is switched off?

- A. Static RAM
- B. Dynamic RAM
- C. EEPROM
- D. None of the above

461. Minimum no. of NAND gate required implementing an Ex-OR function is

- A. 2
- B. 3
- C. 4
- D. 5

462. Which of the following expression is not equivalent to x?

- A. x NAND x
- B. x NOR x
- C. x NAND 1
- D. x NOR 1

463. BCD equivalent of Two's complement is

- A. Nine's complement
- B. One's complement+1
- C. Ten's complement
- D. None of the above

464. Associative memory is sometimes called as...

- A. Virtual memory
- B. Cache memory
- C. Main memory
- D. Content addressable memory

465. When CPU is not fully loaded, which of the following method of data transfer is preferred?

- A. DMA
- B. Interrupt
- C. Polling
- D. None of the above

466. 8085 microprocessor carryout the subtraction by

- A. BCD subtraction method
- B. Hexadecimal subtraction method
- C. 2's complement method
- D. Floating Point subtraction method

467. PAL circuit consists of

- A. Fixed OR & programmable AND logic
- B. Programmable OR & Fixed AND Logic
- C. Fixed OR & fixed AND logic
- D. Programmable OR & programmable AND logic

- | | | | |
|--|--|---|--|
| 468. CPU checks for an interrupt signal during | 474. If the stack pointer is initialized with (4FEB) H, then after execution of Push operation in 8085 microprocessors, the Stack Pointer shall be | 480. During a write operation if the required block is not present in the cache then..... occurs | 487. The addressing mode, where you directly specify the operand value is |
| A. Starting of last Machine cycle
B. First T-State of interrupt cycle
C. Last T-State of instruction cycle
D. Fetch cycle | A. 4FEA
B. 4FEC
C. 4FED
D. 4FE9 | A. Write latency
B. Write hit
C. Write delay
D. Write miss | A. Immediate
B. Direct
C. Definite
D. Relative |
| 469. Which of the following is not a characteristic of RISC architecture.....? | 475. A more efficient way to organize a Page Table is by means of an associative memory having | 481. In..... protocol the information is directly written into main.... | 488.addressing mode is most suitable to change the normal sequence of execution of instructions. |
| A. Larger instruction set
B. Simple addressing mode
C. One instruction per cycle
D. Register to register operation | A. Number of words equal to number of pages
B. Number of words more than the number of pages
C. Number of words less than the number of pages
D. Any one of the above | A. Write through
B. Write back
C. Write first
D. None of the above | A. Relative
B. Indirect
C. Index with offset D. Immediate |
| 470. Memory interleaving technique is used to address the memory modules in order to have | 476. If there are four ROM ICs of 8K and two RAM ICs of 4K words, then the address range of 1st RAM is (Assume initial addresses correspond to ROMs) | 482. The method of mapping the consecutive memory blocks to consecutive cache blocks is called.... | 489. The pipelining process is also called as.... |
| A. Higher average utilization
B. Faster access to a block of data
C. Reduced complexity in mapping hardware
D. Both (A) and (B) | A. (8000) H to (9FFF) H
B. (8000) H to (8FFF) H
C. (6000) H to (7FFF) H
D. (9000) H to (9FFF) H | A. Set associative B. Associative
C. Direct D. Indirect | A. Superscalar operation
B. Assembly line operation
C. Von Neumann cycle
D. None of the mentioned |
| 471. In a multiprogramming system, which of the following is used? | 477. A.B.C is equal to A B C for | 490. The fetch and execution cycles are interleaved with the help of..... | A. Modification in processor architecture |
| A. Data parallelism
B. L1 cache
C. Paging concept
D. None of the above | A. A=0, B=1, C=0 B. A=1, B=0, C=1
C. A=1, B=1, C=1 D. All of the above | A. Tag B. Block
C. Word D. Id | B. Clock
C. Special unit
D. Control unit |
| 472. Cycle stealing technique is used in | 478. Gray code equivalent of $(1000)_2$ is | 491. The situation where in the data of operands are not available is called... | A. Data hazard
B. Stock
C. Deadlock
D. Structural hazard |
| A. Interrupt based data transfer
B. DMA based data transfer
C. Polling mode data transfer
D. None of the above | A. 1111
B. 1100
C. 1000
D. None of the above | A. Linear search
B. Binary search
C. Associative search
D. None of the above | 492. The reason for the implementation of the cache memory is |
| 473. During DMA acknowledge cycle, CPU relinquishes | 479. The memory blocks are mapped on to the cache with the help of..... | A. Register B. Accumulators
C. Push down stack D. Cache | A. To increase the internal memory of the system
B. The difference in speeds of operation of the processor and memory
C. To reduce the memory access and cycle time
D. All of the above |
| A. Address bus only
B. Control bus and data bus
C. Address bus and control bus
D. Data bus and address bus | A. Hash functions
B. Vectors
C. Mapping functions
D. None of the above | A. Indirect addressing mode
B. Index addressing mode
C. Relative addressing mode
D. Offset addressing mode | |

493. The effectiveness of the cache memory is based on the property of _____.

- A. Locality of reference
- B. Memory localization
- C. Memory size
- D. None of the above

494. The temporal aspect of the locality of reference means

- A. That the recently executed instruction won't be executed soon
- B. That the recently executed instruction is temporarily not referenced
- C. That the recently executed instruction will be executed soon again
- D. None of the above

495. The spatial aspect of the locality of reference means

- A. That the recently executed instruction is executed again next
- B. That the recently executed won't be executed again
- C. That the instruction executed will be executed at a later time
- D. That the instruction in close proximity of the instruction executed will be executed in future

496. The algorithm to remove and place new contents into the cache is called _____.

- A. Renewal algorithm
- B. Updating
- C. Replacement algorithm
- D. None of the above

497. The key factor/s in commercial success of a computer is/are.....

- A. Performance
- B. Cost
- C. Speed
- D. Both A and B

498. The main objective of the computer system is

- A. To provide optimal power operation cost
- B. To provide best performance at low power consumption
- C. To provide speedy operation at low power consumption
- D. All of the above

499. A common measure of performance is:

- A. Price/performance ratio
- B. Performance /price ratio
- C. Operation/price ratio
- D. None of the above

500. The main purpose of having memory hierarchy is to

- A. Reduce access time
- B. Provide large capacity
- C. Reduce propagation time
- D. Both A and B

501. Who developed the basic architecture of computer?

- A. Blaise Pascal
- B. Charles Babbage
- C. John Von Neumann
- D. None of the above

502. Which of the following allows simultaneous write and read operations?

- A. ROM
- B. EROM
- C. RAM
- D. None of the above

503. Which of the following is not considered as a peripheral device?

- A. CPU
- B. Keyboard
- C. Monitor
- D. All of the above

504. Which of the following computer memory is fastest?

- A. Register
- B. Hard disk
- C. RAM
- D. None of the above

505. Which of the following operations is/are performed by the ALU?

- A. Data manipulation
- B. Exponential
- C. Square root
- D. All of the above

506. Which of the following format is used to store data?

- A. Decimal
- B. Octal
- C. BCD
- D. Hexadecimal

507. Which of the following memory of the computer is used to speed up the computer processing?

- A. Cache memory
- B. RAM
- C. ROM
- D. None of the above

508. Computer address bus is -

- A. Multidirectional
- B. Bidirectional
- C. Unidirectional
- D. None of the above

509. Which of the following circuit is used to store one bit of data?

- A. Flip Flop
- B. Decoder
- C. Encoder
- D. Register

510. Which of the following is a way in which the components of a computer are connected to each other?

- A. Computer parts
- B. Computer architecture
- C. Computer hardware
- D. None of the above

511. Which of the following circuit convert the binary data into a decimal?

- A. Decoder
- B. Encoder
- C. Code converter
- D. Multiplexer

512. The address in the main memory is known as -

- A. Logical address
- B. Physical address
- C. Memory address
- D. None of the above

513. Subtraction in computers is carried out by -

- A. 1's complement
- B. 2's complement
- C. 3's complement
- D. 9's complement

514. Which of the following computer bus connects the CPU to a memory on the system board?

- A. Expansion bus
- B. Width bus
- C. System bus
- D. None of the above

515. Which of the following memory unit communicates directly with the CPU?

- A. Auxiliary memory
- B. Main memory
- C. Secondary memory
- D. None of the above

516. The collection of 8-bits is called as -

- A. Byte
- B. Nibble
- C. Word
- D. Record

517. Which of the following register can interact with the secondary storage?

- A. PC
- B. MAR
- C. MDR
- D. IR

518. In which of the following form the computer stores its data in memory?

- A. Hexadecimal form
- B. Octal form
- C. Binary form
- D. Decimal form

519. Which of the following is a combinational logic circuit which sends data from a single source to two or more separate destinations?
 A. Multiplexer B. Demultiplexer
 C. Encoder D. Decoder
520. Which of the following is a group of bits that tells the computer to perform a particular operation?
 A. Accumulator
 B. Register
 C. Instruction code
 D. None of the above
521. Where is the document temporarily stored during working on a document on PC?
 A. ROM B. CPU
 C. RAM D. Flash memory
522. Where is the decoded instruction stored?
 A. Registers B. MDR
 C. PC D. IR
523. What does MIMD stand for?
 A. Multiple Instruction Memory Data
 B. Multiple Instruction Multiple Data
 C. Memory Instruction Multiple Data
 D. Memory Information Memory Data
524. The status bit is also called as -
 A. Unsigned bit
 B. Signed bit
 C. Flag bit
 D. None of the above
525. Which of the following register keeps track of the instructions stored in the program stored in memory?
 A. Accumulator
 B. Address Register
 C. Program Counter
 D. Index Register
526. The Program Counter is also called as _____
 A. Instruction Pointer
 B. Data Counter
 C. Memory pointer
 D. None of the above
527. Which of the following topology is used in Ethernet?
 A. Ring topology B. Bus topology
 C. Mesh topology D. Star topology
528. Which of the following is correct about memory and storage?
 A. Memory is temporary, Storage is temporary
 B. Memory is temporary, Storage is permanent
 C. Memory is permanent, Storage is temporary
 D. Memory is slow, Storage is fast
529. Which of the following is equal to 4 bits?
 A. Byte B. Nibble
 C. Record D. All of the above
530. What does one thousand bytes represent?
 A. Kilobyte (KB) B. Megabyte (MB)
 C. Gigabyte (GB) D. Terabyte (TB)
531. What is the content of stack pointer (SP)?
 A. Address of the top element in the stack
 B. Address of current instruction
 C. Address of next instruction
 D. None of the above
532. An n-bit microprocessor has -
 A. n-bit instruction register
 B. n-bit address register
 C. n-bit program counter
 D. None of the above
533. Which of the following is the operation executed on data stored in registers?
 A. Byte operation B. Bit operation
 C. Macrooperation D. Microoperation
534. What does a computer bus line consist of?
 A. Set of parallel lines
 B. Accumulators
 C. Registers
 D. None of the above
535. Which of the following is performed by half adder?
 A. Binary addition operation for 2 decimal inputs
 B. Binary addition operation for 2 binary inputs
 C. Decimal addition operation for 2 decimal inputs
 D. Binary addition operation for 2 binary inputs
536. Which of the following is a combinational logic circuit which converts binary information from n coded inputs to a maximum of 2^n unique outputs?
 A. Multiplexer B. Demultiplexer
 C. Encoder D. Decoder
537. Which of the following is a combinational logic circuit that change the binary information into N output lines?
 A. Multiplexer B. Demultiplexer
 C. Encoder D. Decoder
538. Which of the following is a combinational logic circuit that has 2^n input lines and a single output line?
 A. Multiplexer B. Demultiplexer
 C. Encoder D. Decoder
539. Which of the following building block can be used to implement any combinational logic circuit?
 A. AND
 B. OR
 C. NAND
 D. None of the above
540. Which of the following is the circuit board on which chips and processor are placed?
 A. Master circuit
 B. Motherboard
 C. Big board
 D. None of the above
541. Which of the following computer register collects the result of computation?
 A. Accumulator
 B. Instruction Pointer
 C. Storage register
 D. None of the above
542. CISC stands for -
 A. Complex Instruction Set Computer
 B. Complete Instruction Sequential Compilation
 C. Complex Instruction Sequential Compiler
 D. None of the above
543. Which of the following is the function of the control unit in the CPU?
 A. It stores program instruction
 B. It decodes program instruction
 C. It performs logic operations
 D. None of the above
544. What does EEPROM stands for?
 A. Electrically Erasable and Programmable Read-Only Memory
 B. Electronically Erasable and Programmable Read-Only Memory
 C. Electrically Enabled and Programmable Read-Only Memory
 D. None of the above

545. In which of the following term the performance of cache memory is measured?
- Cache ratio
 - Hit ratio
 - Copy ratio
 - Data ratio

546. RISC stands for -

- Reduce Instruction Set Computer
- Risk Instruction Sequential Compilation
- Risk Instruction Source Compiler
- None of the above

547. Which of the following is an essential data transfer technique?

- MMA
- DMA
- CAD
- CAM

548. Which of the following is page fault?

- Page fault occurs when a program accesses a page of another program
- Page fault occurs when a program accesses a page in main memory

- C. Page fault occurs when there is an error in particular page
D. Page fault occurs when a program accesses a page which is not present in main memory

549. What does DRAM stand for?

- Dynamic Read Access Memory
- Digital Random-Access Memory
- Dynamic Random-Access Memory
- Dynamic Read Allocation Memory

550. Which of the following is known as the step by step procedure to solve a problem?

- Graph
- Table
- Algorithm
- None of the above

ANSWER SHEET

1.B	2.B	3.D	4.D	5.D	6.C	7.A	8.B	9.C	10.D
11.D	12.D	13.C	14.D	15.B	16.A	17.D	18.D	19.B	20.B
21.C	22.C	23.C	24.D	25.D	26.B	27.C	28.D	29.A	30.B
31.B	32.B	33.C	34.B	35.B	36.B	37.C	38.D	39.B	40.D
41.C	42.C	43.B	44.C	45.B	46.D	47.C	48.B	49.B	50.D
51.C	52.C	53.D	54.D	55.B	56.D	57.D	58.B	59.B	60.C
61.B	62.C	63.C	64.D	65.B	66.B	67.D	68.D	69.B	70.A
71.D	72.C	73.A	74.B	75.C	76.A	77.D	78.B	79.D	80.A
81.C	82.A	83.C	84.D	85.A	86.D	87.D	88.D	89.D	90.D
91.A	92.A	93.D	94.D	95.A	96.D	97.B	98.C	99.B	100.A

101.D	102.D	103.A	104.C	105.B	106.B	107.B	108.C	109.B	110.A
111.B	112.D	113.B	114.C	115.D	116.B	117.B	118.D	119.A	120.D
121.B	122.D	123.B	124.D	125.C	126.D	127.D	128.C	129.D	130.C
131.C	132.B	133.B	134.C	135.A	136.B	137.A	138.C	139.B	140.C
141.C	142.C	143.C	144.D	145.C	146.D	147.A	148.A	149.C	150.C
151.A	152.D	153.B	154.D	155.B	156.D	157.B	158.D	159.C	160.D
161.C	162.A	163.D	164.C	165.D	166.C	167.B	168.A	169.D	170.C
171.D	172.D	173.B	174.B	175.D	176.D	177.D	178.D	179.D	180.D
181.D	182.B	183.C	184.C	185.D	186.A	187.D	188.B	189.B	190.D
191.B	192.D	193.B	194.D	195.D	196.B	197.B	198.D	199.D	200.D
201.D	202.A	203.C	204.B	205.D	206.A	207.D	208.A	209.B	210.D
211.D	212.C	213.C	214.C	215.B	216.B	217.A	218.B	219.A	220.D
221.C	222.B	223.A	224.D	225.C	226.D	227.B	228.D	229.B	230.D
231.D	232.A	233.D	234.C	235.B	236.B	237.C	238.A	239.A	240.C
241.C	242.C	243.A	244.A	245.C	246.C	247.B	248.C	249.C	250.A
251.A	252.A	253.C	254.C	255.C	256.A	257.A	258.D	259.C	260.C
261.A	262.D	263.C	264.B	265.C	266.D	267.B	268.D	269.A	270.C
271.D	272.C	273.B	274.A	275.A	276.C	277.C	278.A	279.C	280.A
281.C	282.A	283.A	284.C	285.C	286.C	287.D	288.C	289.B	290.C
291.D	292.C	293.D	294.B	295.C	296.C	297.B	298.D	299.A	300.D
301.D	302.C	303.C	304.D	305.D	306.D	307.C	308.D	309.C	310.A
311.A	312.C	313.B	314.C	315.B	316.D	317.D	318.C	319.A	320.B
321.B	322.C	323.D	324.A	325.B	326.D	327.C	328.A	329.A	330.A
331.D	332.C	333.A	334.B	335.C	336.B	337.D	338.B	339.D	340.B
341.D	342.C	343.C	344.D	345.A	346.B	347.C	348.D	349.C	350.D
351.A	352.A	353.C	354.C	355.D	356.D	357.C	358.C	359.B	360.C