ı.ich	the	5/0. Stack is all acronve							
and for which	at	A. LIFO memory							
minimum to be maintainee	of	B. FIFO memory							
569. The minimum time for which input signal has to be maintained the input of filp-flop is called the input of filp-flop.	-	C. Flash memory							
int coult of the									
the flip-flop.		Addition of							
. Set - UP		and "71" result							
n Hold Illie wine		D. Bust flash memory  577. Addition of two octal numbers  A. 213							
B. Hold time C. Pulse interval time (PST) D. Pulse stability time (PST)		Α. 213							
n lee stauting than muiti	pie	B. 123							
is sale to change the	to	C. 127							
internal variables change in one input variable change in one input variable		D. 345							
change in the B. Hold delay		578. Addition of two octal numbers							
A Race condition		and "243" results							
- ti-ld and war.		A. 2013							
571. A decade counter is		B. 1023							
A. Mode-3 counter		C. 1027							
B. Mod- 5 counter		D. 1032							
C. Mod -8 counter D. Mod-10 counter	5	579is one of the example							
D. Mod-10 counter  572. A nibble consist ofbits		synchronous inputs.							
n 1		A. J-K input							
A. 2 B. 4 C. 8 D. 16		B. EN input							
573. Excess-8 code assigns to "-8"		C. Preset input (PRE)							
A 1110 B. 1100		D. Clear Input (CLR)							
C. 1000 D. 0000	50	0occurs when the same							
	30	signal arrives at different time							
574. The three fundamentals gates are:		different clock input du							
A. AND, NAND, NAND		propagation delay.							
B. NOT, NOR, XOR	A. Race condition								
C. NOT, OR, AND		C. Ripple effect							
D. NOT, NOR XOR		B. Clockskew							
575. The amount of memory that is		D. Nana of the above							
supported by any digital system depends upon	581	the trans							
A. The organization of memory	from a current state to the next								
The SHIPPING AC		is determined by							
The SIZE Of day 11		A. Current state and the input							
SIZE Of the 1:		C. Previous state and inputs							
D. The size of the address bus of the		B Current state and output							
166   Dinital Las	•	D. Provious state and output							

D. Previous state and output

582. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

A. 1100

C. 0000

B. 0011

D. 1111



ben,												
	1				5.A	6.B	. 7.D	8.C	9.D	10.C		
ımpk	1.B	2.C	3.A	4.A	15.C	16.D	17.B	18.D	19.B	20.B		
	11.B	12.C	13.D	14.C		26.D	27.A	28.C	29.D	30.C		
	21.C	22.C	23.D	24.C	25.A	36.C	37.A	38.B	39.A	40.A		
	31.C	32.B	33.A	34.C	35.B		47.D	48.A	49.A	50.C		
	41.C	42.C	43.B	44.C	45.A	46.A	57.D	58.D	59.A	60.A		
	51.A	52.C	53.A	54.C	· 55.A	56.B		68.D	69.C	70.C		
	61.D	62.D	63.A	64.B	65.D	66.A	67.C		79.B	80.C		
ne d tima	15	72.A	73.D	74.C	75.A	76.B	77.C	78.B	89.C	90.B		
	71.A	82.C	83.B	84.A	85.B	86.B	87.A	88.D		100.B		
lue	81.A		93.D	94.C	95.C	96.B	97.C	98.C	99.C			
	91.D	92.C		104.A	105.C	106.A	107.B	108.A	109.D	110.A		
	101.B	102.D	103.B		115.B	116.A	117.A	118.C	119.A	120.D		
nia t Ø	111.C	112.A	113.C	114.A		126.B	127.A	128.A	129.C	130.B		
	121.D	122.A	123.B	124.D	125.D	136.B	137.B	138.A	139.C	140.B		
	131.D	132.A	133.C	134.B	135.D		147.D	148.B	149.A	150.C		
	141.B	142.A	143.D	144.A	145.B	146.C	157.D	158.C	159.A	160.A		
	151.A	152.B	153.C	154.A	155.B	156.C		168.B	169.C	170.A		
	161.D	162.A	163.A	164.D	165.C	166.C	167.D			1 (07 )		
	161.D 162.A 163.A 164.D 164.D 165.A											

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			-					1	
171.B	172.A	173.B	174.D	175.D	176.D	177.B	178.B	179.F	3 180
181.C	182.B	183.A	184.A	185.D	186.C	187.D	188.A	189.0	180.0
191.D	192.C	193.B	194.D	195.A	196.D	197.B	198.B	199.E	190.D 200.A
201.C	202.A	203.C	204.B	205.A	206.D	207.C	208.D	209.0	210.A
211.B	212.A	213.A	214.D	215.C	216.D	217.A	17.A 218.B		220 <sub>.A</sub>
221.D	231.A     232.C     233.2       241.D     242.D     24.2       251.C     252.D     25.2       261.B     262.A     26.2       271.A     272.C     27.2       281.C     282.C     28.2       291.A     292.A     29.2		224.C	225.B	226.C	227.B	227.B 228.D		230.D
231.A			234.C	235.C	236.D	237.A	238.D	239.B	
241.D			244.A	245.B	246.D	247.C	248.D	249.B	
251.C			254.A	255.B	256.A	257.B	258.C	259.C	260.B
261.E			264.A	265.A	266.B	267.A	268.D	269.B	270.A
271.			274.A	275.B	276.A	277.C	278.A	279.A	280.B
281.0			284.B	285.C	286.A	287.C	288.C	289.A	290.A
			294.C	295.C	296.B	297.C	298.A	299.A	300.C
301.	280,000	S. S. A.	304.A	305.D	306.D	307.C	308.C	309.D	310.D
311.0			314.C	315.B	316.D	317.A	318.B	319.A	320.B
321.				325.B	326.C	327.D	328.A	329.C	330.B
	331.D 332.C		334.C		336.D	337.B	338.B	339.C	340.B
341.4			11 1 100		346.B	347.B	348.A	349.D	350.C
351.A			-			357.C	358.B	359.A	360.D
361.0						367.D	368.A	369.B	370.D
371.D	-			375.C		377.A	378.C	379.B	380.B
381.B		_		385.D	_	387.B	388.C	389.C	390.D
391.C	392.B	-		395.A	396.D	397.B	398.A	399.C	400.C
401.B	402.B	403.D		405.D	406.B	407.A	408.C	409.D	410.B
411.D	412.D	413.D 423.B	414.C 424.D	415.D	416.D	417.C	418.B	419.C	420.B
421.D	422.A	423.B	424.D	425.A	426.B	427.C	428.C	429.B	430.A

			g 433.	C 434	.D 4	35.C	436.	R	122					
1	131	B 432.			A 4	45.A			437.	150.		9.C	440.4	7
1	441	0 442.			_	55.B	456.	_	447./		C 449	9.D	450.E	_
	451	D 452.7				55.B	466.4		457.[		459	).D	460.B	
-	161	A 462.1	172 F	_	4-	5.A			467.E	700.7	469	.D	470.A	_
	171	D 472.L		_	4	5.A	476.0	_	477.B	., 0.1	479	.A	480.C	Ų
	481.1	482.C	- 0	-	4—	5.D	486.C	4	487.A	100.1	489	.C	490.D	J
	191.1	3 492.C		_	╬		496.A	╬	497.B	498.B	499.	D	500.C	1
	501.E	-02 B			-	o.D	506.B		507.C	508.C	509.	С	510.A	i
	511.0	10.0		514.C	-		516.A	L	517.B	518.C	519.,	A	520.B	i
	521.B	7	523.D	524.D	525	-4	526.C	Ŀ	527.C	528. B	529.7	4	530.B	
	531.B	T	533.B	534.D	535	-	536.C	5	37.B	538.C	539.E	3	540.D	
	541.C		543.B	544.B	545.	Α	546.A	5	47. C	548. A	549. (		550.C	
	551.B	552.A	553.C	554.B	555.	D	556.B	5	57.B	558.C	559.C		60.D	
	561.D	562.B	563.B	564.B	565.	Α :	566.A	50	67.C	568.A	569.B	4-	70.A	
	571.D	572.B	573.D	574.C	575.1	) :	576.A	57	77.C	578.D	579.D		80.B	
	581.A	582.C										T		
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