### 545. In which of the following term the performance of cache memory is

measured?

B. Hit ratio

D. Data ratio A. Chat ratio

C. Copy ratio

546. RISC stands for -

A. Reduce Instruction Set Computer Sequential Instruction

B. Risk C. Risk Instruction Source Compiler Compilation

D. None of the above

547. Which of the following is an essential data transfer technique?

A. MMA

B. DMA

D. CAM

C. CAD 548. Which of the following is page fault?

A Page fault occurs when a program accesses a page of another program

B. Page fault occurs when a program accesses a page in main memory

C. Page fault occurs when the narricular page 1 error in particular page

D. Page fault occurs when a page which is a high accesses a page which is holy

549. What does DRAM stand for

A. Dynamic Read Access Menon

B. Digital Random-Access Mentol C. Dynamic Random-Access Men.

D. Dynamic Read Allocation Men

550. Which of the following is known the step by step procedure to sol problem?

A. Graph

B. Table

C. Algorithm

D. None of the above

#### ANSWER SHEET

1.B	2.B	3.D	4.D	5.D	6.C	7.A	8.B	9.C	10.D
11.D	12.D	13.C	14.D	15.B	16.A	17.D	18.D	19.B	20.B
21.C	22.C	23.C	24.D	25.D	26.B	27.C	28.D	29.A	30.B
31.B	32.B	33.C	34.B	35.B	36.B	3.7.C	38.D	39.B	40.D
41.C	42.C	43.B	44.C	45.B	46.D	47.C	48.B	49.B	50.D
51.C	52.C	53.D	54.D	55.B	56.D	57.D	58.B	59.B	60.0
61.B	62.C	63.C	64.D	65.B	66.B	67.D	68.D	69.B	70.A
71.D	72.C	73.A	74.B	75.C	76.A	77.D	78.B	79.D	80.A
81.C	82.A	83.C	84.D	85.A	86.D	87.D	88.D	89.D	90.0
91.A	92.A	93.D	94.D	95.A	96.D	97.B	98.C	99.B	100.A

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	102.D	103.A	104.C	105.B	106.B	107.B	108.C	109.B	110.A
101.0	112.D	113.B	114.C	115.D	H6.B	117.B	118.D	119.A	120.D
111.B	122.D	123.B	124.D	125.C	126.D	127.D	128.C	129.D	130.C
121.B	132.B	133.B	134.C	135.A	136.B	137.A	138.C	139.B	140.C
131.C	142.C	143.C	144.D	145.C	146.D	147.A	148.A	149.C	150.C
141.C	152.D	153.B	154.D	155.B	156.D	157.B	158.D	159.C	160.D
151.A	162.A	163.D	164.C	165.D	166.C	167.B	168.A	169.D	170.C
161.C	172.D	173.B	174.B	175.D	176.D	177.D	178.D	179.D	180.D
171.D	182.B	183.C	184.C	185.D	186.A	187.D	188.B	189.B	190.D
181.D	192.D	193.B	194.D	195.D	196.B	197.B	198.D	199.D	200.D
191.B	192.B	.203.C	204.B	205.D	206.A	207.D	208.A	209.B	210.D
201.D	212.C	213.C	214.C	215.B	216.B	217.A	218.B	219.A -	220.D
211.D	212.C	223.A	224.D	225.C	226.D	227.B	228.D	229.B	230.D
221.C	232.A	233.D	234.C	235.B	236.B	237.C	238.A	239.A	240.C
231.D	232.71 242.C	243.A	244.A	245.Ċ	246.C	247.B	248.C	249.C	250.A
241.C	252.A	253.C	254.C	255.C	256.A	257.A	258.D	259.C	260.C
251.A	160 D	263.C	264.B	265.C	266.D	267.B	268.D	269.A	270.C
261.A		273.B	274.A	275.A	276.C	277.C	278.A	279.C	280.A
271.D		283.A	284.C	285.C	286.C	287.D	288.C	289.B	290.C
281.C		293.D	294.B	295.C	296.C	297.B	298.D	299.A	300.D 310.A
291.D 301.D		303.C	304.D	305.D	306.D	307.C	308.D	309.C	320.B
301.D	-	313.B	314.C	315.B	316.D	317.D	318.C	319.A	320.B
321.B		323.D	324.A	325.B	326.D	327.C	328.A	329.A	340.B
331.D		333.A	334.B	335.C	336.B	337.D	338.B	339.D	350.D
341.D	002.0	F 100 (17 - 1)	344.D	345.A	346.B	347.C	348.D	. 349.C	360.C
351.A		343.C	354.C		356.D	357.C	358.C	359.B	
331.A	352.A	353.C	334.C	300.5		Cogineerin	g Licensur	e Examina	itians   291

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361.D	362.B	363.B	364.D	365.D	366.B	367.B	368.0	369.1	
371.C	372.A	373.B	374.A	375.D	376.D	377.A	378.E		3/0.0
381.C	382.B	383.D	384.A	385.D	386.B	387.B	388.D		380.0
39Į.A	392.C	393.A	394.B	395.B	396.C	397.C	398.D		390.A
401.C	402.B	403.C	404.B	405.C	406.B	407.C	408.A		400.C
411.B	412.D	413.A	414.C	415.D	416.D	417.D	418.B	419.A	#10.B
421.C	422.C	423.D	424.D	425.D	426.C	427.C	428.B	429.D	120.B
431.C	432.D	433.D	434.C	435.B	436.D	437.B	438.A	439.D	430.B
441.B	442.A	443.C	444:C	445.D	446.B	447.B	448.C	449.A	450.A
451.B	452.B	453.D	454.A	455.A	456.C	457.D	458.B	459.B	460.C
461.C	462.D	463.C	464.D	465.D	466.C	467.A	468.B	469.A	470.C
471.C	472.B	473.D	474.C	475.A	476.B	477.D	478.A	479.C	480.D
481.A	482.C	483.A	484.C	485.C	486.A	487.A	488.A	489.A	490. B
491.A	492. B	493. A	494.C	495.D	496.C	497. D	498. B	499.A	500.D

	501 (	Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and later it Arithmetic, and Logical Memory Unit (ALLI) Particular design, and Logical Memory Unit (ALLI) Particular design
	502 C	RAM, stands for Random Access Memory. It is a hardware device generally CPU. It is the read and writes memory of a computer and acts as an internal memory of the can be written to it as well as read from it.
5	03 A	The CPU is not considered as a peripheral device as it is the primary component of the computer, and a computer system cannot work without a CPU. Peripheral devices are not the essential parts of the computer and can be defined as an keyboard, etc.
50-	4 A	Register memory is the smallest and fastest memory in a computer. It is not a part of the main memory and is located in the CPU in the form of registers, which are the smallest data holding elements.

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Android is a software package and Linux-based operating system for mobile Android 13 as tablet computers and smartphones. devices.

The BCD stands for Binary Coded Decimal Number.

The BCD stands for Binary Coded Decimal Number. The BCD or Cache memory (RAM). The CPU can access it more quickly than the primary main So, it is used to synchronize with a high-speed CPU and the primary main memory. So, it is used to synchronize with a high-speed CPU and to improve its performance address of data (but not the data) between the processor amory. Address bus is 16-bit which can address Address bus and the memory. Address bus is 16-bit which can address up to 64 kb. Address identificational. bus is unidirectional. bus is a digital memory circuit, and with the help of the flip-flop, we can Flip-flop is a store one bit of information. The fundamental blocks of various sequential circuits store one of various sequential circuits are flip-flops. Flip-flop is also called a bistable multivibrator or one-bit or binary. Computer Architecture is concerned with the way hardware components are connected together, to form a computer system. It acts as the interface between hardware and software. Physical address space in a system can be defined as the size of the main memory. It is really important to compare the process size with the physical address space. The process size must be less than the physical address space. 2's complement is used for representing signed numbers and performing arithmetic operations such as subtraction, addition, etc. A system bus is a single bus that connects the major components of the computer 514 C The main memory acts as the central storage unit in a computer system. Main memory is the memory unit that directly communicates with the CPU. It is a relatively large and fast memory that is used to store programs and data during runtime operations. which contain '0' or '1'. A byte is represented as upper-case 'B' whereas a bit is represented by small-case "b". A Byte is a unit of data measurement which mainly consists of eight bits. A byte is a series of binary digits, The Memory Address Register (MAR) contains 12 bits that hold the address for the memory location. The MAR holds the address of the main memory to or from which data is to be transferred. In a computer, the data is stored in binary form that is in the form of binary digit 0, and 1. 0 means OFF, and 1 means ON. A binary number is a base 2 number because it is either 0 or 1. Any combination of 0 and 1 is a binary number such as 1001, 101, 11111, 101010, etc. Salal's Committee /1-1-

	A De-multiplexer has a single input, 'n' selection lines of the sele	1 50	one from
	A De-multiplexer has a single input, 'n' selection lines, and referred to as a demux. A De-multiplexer has a single input, 'n' selection lines, and referred to as a demux.	do	one from performed on the data stored in registers are called Micro-
519 B	Corred 10 as a		erations performed on the authority
	maximum of 2 in the computer to perform a particular operation	1	the operations period operations period on the operations of a set of common lines, one for each bit of register, through which operation is transferred one at a time. Control signals determine which a bus information is transferred one at a time.
	- group of bits that the Code instructs the computer to perform	A	of All Collinion into a
520 C	an Instruction Code. The complements, etc.	0	bus consists of a stransferred one at a time. Control signals determine which
320 C	such as subtractions, developed as subtractions, developed as subtractions current	1.:0	really in the stand by the stands of
	RAM stands for Random Promise hard drives because data 6.	A	A bus consists of a set of a s
	used on a device are stored than the hard drives. RAM is a volatile	1	The adder is a basic out to perform OR operation of two single
521 C	RAM are loaded much laster than the material are loaded much laster than the material which means it does not store data or instructions permanently.	1	The rank out two outputs. The augent and addent bits are two input states, and 'carry'
	which means it does not store data of more which means the more which me		The Half-Adder is a basic early states of the half adder.  The Half-Adder is a basic early states of the half adder.  The Half-Adder is a basic early states of the half adder.  The hippers information is passed in the
	which means it does not see that which means it does not see that the instruction code. The instructions read the instruction Register (IR).		produce out two input states. The augent and addent bits are two input states, and carry bit binary numbers. The augent and addent bits are two input states of the half adder.  bit binary are two output states of the half adder.  and sum are two output states of the half adder.  to a maximum of 2^n different outputs. The binary information is passed in the to a maximum of 1 input lines. The output lines define the 2N-bit code for the binary input lines.
522 D	The instruction Register (IR) in the Instruction Register (IR). from memory are placed in the Instruction and Multiple Data Stream Inc.	35 A	and sum of 2 <sup>n</sup> different outputs. The omaty information of property lines define the 2N-bit code for the binary
	mimD stands for 'Multiple Instruction and Multiple Data Stream'. In this organization, all processors in a parallel computer can execute different		and sum are two 52n different outputs. The binary information is passed in the to a maximum of 2nd different output lines define the 2N-bit code for the binary form of N input lines. The output lines define the 2N-bit code for the binary form of N input lines. The Decoder performs the reverse operation of the Encoder.
523 B	organization, all processors in a parametric comparison and operate on various data at the same time.		to a maximum of N input lines. The output lines define the 2N-bit code for the binary form of N input lines. The Decoder performs the reverse operation of the Encoder.  Information. The Decoder performs as a combinational circuit that converts binary
	instructions and operate on various data at the same		form of N inportation. The Decoder performs the reverse operation of the Encoder.  Information. The Decoder performs the reverse operation of the Encoder.  A Decoder can be described as a combinational circuit that converts binary from 'n' coded inputs
524 C	t in a fination of known treat		A Decoder can be described in A Decoder from 'n' coded inputs information from 'n' coded inputs that change the binary information into N output lines
	which instruction is being executed and what the next instruction will be. The	536 D	The combinational circuits that change the binary information into N output lines  The combinational circuits that change the binary information into N output lines  Exceders. The output lines define the N-bit code for the binary
525 (	Program Counter (PC) also contains 12 bits that hold the address of the next		The combinational circuits that change the binary information into N output lines are known as Encoders. The output lines define the N-bit code for the binary are known as Encoder performs the reverse operation of the Decoder.
		537 C	are known as Encoders. The output lines define the N-bit code for the output are known as Encoder performs the reverse operation of the Decoder.
	The program counter is also called an instruction pointer or instruction address		A multiplexer is a combinational circuit that has 2n input lines and a single output a multiplexer is a multi-input and single-output combinational
526	Cal - 1- action of the	-	A multiplexer is a combinational circuit that the Amultiplexer is a combinational
	next instruction.		line. Simply, the multiplexer is received from the input lines and directed to the
	The bus topology is designed in such a way that an the stations are	538 A	circuit. The binary information is received as
52	and the same time that are carried the same time to the same time time time time time time time ti		output line.
	used in 802.3 (ethernet) and 802.4 standard networks.		output line.  The NAND gate is a special type of logic gate in the digital logic circuit. The NAND gate is the universal gate. It means all the basic gates such as AND, OR, NAND gate is the universal gate. The NAND gate is the
	The data and the information stored in the storage are permanent. It holds the high-	539 C	NAND gate is the universal gate. It means all the basic gates such
52	capacity data which are not held in the computer memory.  In computer systems, memory is a RAM, which stores the data and information	339 C	and NOT gate can be constructed using a rate of
	temporarily. RAM contains everything which is currently running on our		and in the after a Calca NIOT A NII ) gale
	computer.		The motherboard is generally a thin circuit board that holds together almost all
	A group of four bits (half of the byte) is called a nibble, and a group of eight bits	1	The motherboard is generally a thin circuit board that holds a parts of a computer except input and output devices. Each motherboard has a parts of a computer except input and output devices. All crucial hardware like
5	29 B (11001010) is called a byte. A nibble is a data unit that comes before the Byte, and	540	parts of a computer except input and output devices. Each mark and chipset, which is the collection of controllers and chips. All crucial hardware like chipset, which is the collection of controllers and output devices are located on
	a kilobyte comes after it. The smallest unit of storage consisting of either 0 or 1 is called a bit. The arrangement of the constant of the storage consisting of either 0 or 1 is		CPU, memory, hard drive, and ports for input and output
	called a bit. The arrangement of such 4 bits is known as a nibble.  A KB is the unit symbol for the 'Kilobyte'. In SI (International System of units), the prefix kilosystem.		Ult Mothorhean J
-	the pictix kilo in Kilobyte means 1000. So, one kilobyte is 1000 bytes. In Decimal		The accumulator is an 8-bit register associated with the ALU. The register 'A' is
5	(i.e., with base 10). I kilobyte is equal to 1000 bytes, and in hinary (with base 2).	14	The accumulator is an 8-bit register associated with the ALC. The arithmetic an accumulator in the 8085. It is used to hold one of the operands of an arithmetic and locity and locity and locity and locity arithmetic or logical operation is also
	1 killohyte is equivalent to 1024 butes. A killohyte is that unit, which is larger thall		logical operation. The final result of an aritimetre of
100	(MB).		in the accumulator.
29	4   Computer Organization and Embedded System		Setal's Communications   295
			المانة Computer/Information Technology/Software Engineering Licensure Examinations   295

542 A	The CISC Stands for Complex Instruction Set Computer, developed by the last that a large collection of complex instructions that range from simple to to execute the instructions.
543 B	instructions. It controls and coordinates the functioning of all parts of the computer. The Control Unit's main task is to maintain and regulate the floring across the processor.
544 A	EEPROM stands for "Electrically Erasable and Programmable Read Only Memory". It is used to erase stored data using a high voltage electrical charge and re-programmed it. It is erased and reprogrammed electrically without using ultraviolet light.
545 B	The performance of the cache memory is frequently measured in terms of a quantity called hit ratio. When the CPU refers to memory and finds the word in cache, it is said to produce a hit. The ratio of the number of hits divided by the total CPU references to memory (hits plus misses) is the hit ratio.
546 A	RISC stands for Reduced Instruction Set Computer Processor, a microprocessor architecture with a simple collection and highly customized set of instructions. It is built to minimize the instruction execution time by optimizing and limiting the number of instructions.
547 B	DMA stands for Direct Memory Access. In the DMA data transfer scheme, data is directly transferred from an I/O device to RAM or from RAM to an I/O device.
548 D	If the referred page is not present in the main memory, then there will be a miss, and the concept is called Page miss or page fault. The CPU has to access the missed page from the secondary memory. If the number of page fault is very high, then the effective access time of the system will become very high.
549 C	DRAM stands for "Dynamic Random-Access Memory". DRAM is a type of RAM that is used for the dynamic storage of data in RAM. In DRAM, each cell carries one-bit information.
550 C	A finite set of instructions that specifies a sequence of operations is to be carried out to solve a specific problem or class of problems called an Algorithm.

## MCQS (SET-I)

# What is the purpose of an instruction what is the purpose of an instruction register (IR) in a computer system?

- register (IK) in a compact system.

  A To hold the address of the next instruction to be executed
- B. To hold the current instruction being executed
- C. To hold the data being processed by the ALU
- p. To hold the results of ALU operations

### What is a control unit in a computer system responsible for?

- A Performing arithmetic and logical operations
- B. Storing and retrieving data
- C. Coordinating the activities of other computer components
- D. Processing data into useful information

#### 3. What type of computer organization uses a Harvard architecture?

- A. Von Neumann B. Harvard
- C. Princeton D. RISC
- What is the purpose of a cache in a computer system?
  - A. To store frequently used data for quick access
- B. To store data that is no longer needed
- C. To store the results of arithmetic operations
- D To store the instructions being executed

#### 5. What is an embedded system?

- A. A computer system designed for use in automobiles
- B. A computer system designed for use in space missions
- C. A computer system integrated into a device to perform specific tasks
- D. A computer system designed for use in scientific experiments

#### 6. What is the purpose of a micro-controller in an embedded system?

- A. To control the flow of data in the system
- B. To perform arithmetic and logical operations
- C. To coordinate the activities of other embedded system components
- D. To process data into useful information

### 7. What is the difference between an embedded system and a general-purpose computer?

- A. An embedded system is designed for a specific task, while a generalpurpose computer is not
- B. A general-purpose computer has a larger memory than an embedded system
- C. An embedded system has a faster processing speed than a general-purpose computer
- D. A general-purpose computer has more input/output devices than an embedded system

