MCQS (SET-II)

chip	8. The min	_
A microprocessor is a chip all the functions of a CPU	8. The microprocessor can read/write	٥
A microprocessor is a chip A microprocessor is a chip integrating all the functions of a CPU integrating all the functions of a CPU of a computer. of a computer. B. Single	16-bit data from or to A. Memory	
	B 1/0.4	
D Triple	D Pagist	
c Dolloic in a/a aircuit	Microprocessors 45	l.a
C. Double One of the concions as the CPU of the	Dit wide	19
Lat Tunet	A. 12 bit B. 10 bit	
miller	C. 16 bit . D. 20 hit	
A. Electronic D. Processing	10. The work of EU is	
A. Electronic C. Integrating D. Processing of the	A. Encoding B. Decoding	
C. Integrating Microprocessor is the of the of the	C. Processing D. Calculations	
Microprocessor is the or the	III. The 16 Lie on	
LATINIIAI CASILL	microprocessor is responsible t	0
Main D. Heart	indicate	.U
o Important D. Simple	A. The condition of result of AL	Ιī
The purpose of the microprocessor is	operation of AL	U
to control	B. Condition of memory	
Memory B. Switches	C. The result of addition	
C. Processing D. Tasks	D. The result of subtraction	
The first digital electronic computer	12. The CF is known as	
was built in the year	A. Carry flag	
A. 1950 B. 1960	B. Condition flag	
C. 1940 D.1930	C. Common flag	
In 1960's taxes institute invented	D. Single flag	
A. Integrated circuits	13. The SF is called as	
	A. Service flag B. Sign flag	
B. Vacuum tubes	C. Single flag D. Condition flag	,
C. Microprocessor	14. The OF is called as	
D. Transistors	A. Overflow flag B. Overdue flag	
The Intel 8086 microprocessors	C. One flag D. Overflag	
_processor.	15. The IF is called as	
A. 8 bit B. 16 bit	A. Initial flag B. Indicate flag	
C. 32 bit D. 4 bit	C. Interrupt flag D. Enter flag	
D, 7 011	C. Interrupt ring D. 2.	

16. The register AX is formed to	y 25. The CS register stor	determines determines	44. The address L.
grouping	code segment A. Stream	microprocessor determines microprocessor determines fighter the specified condition exists the needbar the specified the specif	44. The address bits are sent out on lines
A. AH & AL B. BH & BL	A. Stream	6 bether the spring the	A. 16-10
C. CH & CL D. DH & DL	D, P ₂₄		C. D0-D17 B. A0-17
17. The SP is indicated by	D. Str.	A Conditional flag D. Sign flag Conditional flag to words from	45. is used a D. C0-C17
A. Single pointer		A Commissional flag D. Sign flag C Conditional flag D. Sign flag C copies to words from The LES copies and	45is used to write into memory A. RD
B. Source pointer	C. 16bits B. 4bits	toter and	D 11/D
C. Stack pointer	D. 32hita	The LES copies to head and the LES register and B. CS	C. RD/WR
	27. The push source copies a way	A. DS D. DS	The functions of D:
D. Destination pointer	27. The push source copies a word from A. Stack	C. ES translates a byte from one	
18. The BP is indicated by	B. Memor		
A. Base pointer B. Binary pointer	C. Register D. Destination 28. LDs copies to consecution	The translate of the code to another code. B. XCHNG	A. 8085A B. 80835
C. Bit pointer D. Digital pointer	28. LDs copies to consecutive words from	A XLAT D. PUSH	C. 8086 D. 80845
19. The SS is called as	memory to register and A. ES	C. POP contains an offset instead	47. The RD, WR, M/IO is the heart of
A. Single stack B. Stack segment	B. DS	Contession	mode mode
C. Sequence stack D. Random stack	D. CS	cactilal audi	A. Minimum
20. The index register is used to hold.	29. INC destination increments the content of destination by	, SP	B. Compatibility mode
A. Memory register	Λ 1		C. Maximum
B. Segment memory	D. 20	The 8086 fetches instruction one after	D. Control mode
C. Offset address	30. IMUL source is assigned	thar for III	48. In a minimum mode there is aon
D. Offset memory	A Multiplication D	A. Code segment B. ES	the system bus
21. The BIU contains FIFO register of	C. Addition D. Division	D. SS	A. Single B. Multiple
bytes.	31destination inverts each bit	1. The BIU contains FIFO register of	C. Double D. Triple
A. 8 B. 6	of destination.	size 6 bytes called	49. If MN/MX is low the 8086operatesin
C. 4 D. 12	A. NOT B. NOR	A. Queue B. Stack	mode
22. The BIU prefetches the instruction	C. AND D.OR	C. Segment D. Register	A. Minimum
from memory and store them in A. Queue B. Register	32. The JS is called as	4. Theis required to	B. Both (A) and (B)
D. Register	A. Jump the signed bit	synchronize the internal operands in	C. Maximum
C. Memory D. Stack 23. The 1 MB byte of memory can be	B. Jump simplicit	the processor CLK Signal	D. Medium
divided intosegment.	1 810 011	A. UR Signal B. Vcc	50. In max mode, control bus signal So,S1
A. 1 Kbyte B. 64 Kbyte	D. Jump signalit	C. AIE D. Ground	and S2 are sentoutin_form
C. 33 Kbyte D. 34 Kbyte	33. Instruction providing both segment	The pin of minimum modeAD0-	
24. The DS is called as	base and offset address are called	AD15hasaddress.	A. Decoded
A. Data segment	A. Below type B. Far type C. Low type D. High type	A. 16bit B. 20bit	C. Encodes
B. Divide segment	C. Low type D. High type	C. 32bit D. 4bit	51. Thebus controller device
C. Digital segment	34. The conditional branch instruction specify for branching.	AD15has data bus	decodes the signals to produce the
D. Decode segment	A. Conditions B. Instruction	A. 4bit P. 201-it	control bus signal A Jeternal B. External
Decade segment	C. Address D. Memory	C. 16bit B. 20bit	A. Internal
? Computer Organization and Embedded System	m	D. 32bit	C. Data D. Address



52	A Instruction at the end of	59.	Microprocess	the microprocessor	75.	8086 and8088com.
34.	interrupt service program takes the		Microprocessor provides signal like A. LOW B. MCA	signal prevent the microprocessor signal prevent the same data more than B. Controlling		8086 and8088contains_transistors. A. 29000
			to indicate the read one signal is	signading the sa		C 24000
	execution back to the interrupted		A. LOW	B. Controlling	76	C. 44000
	program		C. MCMW B. MCMR D. MCMR	AC :00 1'	, O.	stands for
	A. Forward B. Data	60.	To interface memory	A pipeling D. Signaming		A. Address latch enable
	C. Return D. Line			A pipelining D. Signaling A liphelining D. Signaling C Handshaking		B. Address leak enable
53.	The main concerns of the are to		microprocessor, connect register the	18 July B. 200p		C. Address level enable
	define a flexible set of commands		microprocessor, connect register the lines of the address bus must be added to address lines of the chip.	A Reset D. Start		D. Address leak extension
	A. Memory interface		to address lines of the_chip.	C Sel ete interrupt signal to micro-	77.	What is DEN?
	B. Both A and B		A. Single B. Mulc.	C Set D. Start C Set control of the senerate interrupt signal to micro- generate interrupt signal to micro- generate interrupt signal to micro- processor and receive acknowledge processor and receive acknowledge		Y D.
			C. Memory D. Triple	a persor and receive		C D
	C. Peripheral interface	61.	I De remaining 1.	processor and processor and A. Priority resolver	78.	In 8086 Francis C. Data encoding
	D. Control interface		is decoded to generate chip select	intillities		In 8086, Example for Non mask able interrupts are
54.	Primary function of memory		signal select			
	interfacing is that they		A. Data B. Control bus	C. Control rogister D. Interrupt register pin is used to select		C. Domi
	should be able to read from and write		C. Address D base	pin is used to select	70	
	into register	62.	C: Address D. both A and B signal is generated by combining RD and WR signals with a combining	1 The word	13.	In 8086 the overflow flag is set when
	A. Multiprocessor B. Dual Processor		RD and WR signals with IO/M			
	C. Microprocessor D. Coprocessor		A. Control B Register	A A0 D. AD7-AD6		A. The sum is more than 16bits.
55.	To perform any operations, the MP		- register	C. D7-D6 is used to connect more		B. Signed numbers go out of their range
	should identify the	63		11 The microprocessor		after an arithmetic operation.
	A. Register B. Interface		Memory is an integral part of asystem	A. Peripheral device		C. Carry and sign flags are set.
	C. Memory D. System		A. Supercomputer	B. I/O devices		D. Subtraction
56.	The Microprocessor places		B. Minicomputer	C. Cascade	80.	In 8086 microprocessor the following
	address on the address bus			D. control unit		has the highest priority among all type
	A. 4 bit B. 16 bit		C. Microcomputer	2. CS connects the output of		interrupts?
	C. 8 bit D. 32 bit		D. Mainframe computer	A. Encoder B. Slave program		A. NMI B. TYPE255
57.	The Microprocessor places 16 bit	04.	has certain signal requirements	C. Decoder D. Buffer	71	C. DIV0 D. OVERFLOW
	address on the add lines from that		write into and read from its registers	13. In which year, 8086 was introduced?	81.	In 8086 microprocessor one of the
	address by register should		A. Memory	A. 1978 B. 1977		following statements is not true?
	be selected		B. Both A and B	C. 1979 D. 1981		A. Coprocessor is interfaced in
	A. Address B. Two		C. Register	Expansion for HMOS technology		maxmode.
	C. One D. Three		D. Control	A. High level mode oxygen		B. Coprocessor is interfaced in
58.			Anis used to fetch one address	semiconductor		minmode.
	identify and select the register for the EPROM		A. Internal decoder B. Encoder	D III 1		C. I /O can be interfaced in max
			C. External decoder D. Register	semiconductor semiconductor		/minmode.
	A. Internal decoder	06.	The primary function of theis			D. Supports pipelining
	3. Address decoder		to accept data from I/O devices	C. High performance medium oxide semiconductor	01	Address line for TRAP is?
	. external decoder		A. Multiprocessor B. Peripherals	D. High page	02	A 0023H B. 003311
D	. Data decoder		C. Microprocessor D. Interfaces	D. High performance metal oxide semiconductor		C. 0024H D. 0099H
314 C	omputer Organization and Embedded Syste	TI .		The conductor		(1. 002411
	,			Safal's Computer /Information To-backgry/S	Snftw:	are Engineering Licensure Examinations 315
				Take / mormation recondingy/	301141	

83. Access time is fa	aster for
A. ROM	B. DRAM
C. SRAM	D. ERAM
84. The First Micro	processor was
A. Intel 4004	B. 8085
C. 8080	D. 4008
85. Status register is	
A. Accumulator	B. Counter
C. Stack	D. Flags
	D. Flags llowing is not a bas
element within t	he microprocessor?
A. Microcontroll	er microprocessor?
B. Register array	
C. Arithmetic log	ic unit (ALLI)
D. Control unit	gie unit (ALU)
	Dypasses the CPU for
certain types of o	data transfer?
 A. Software inter- 	rupts
B. Polled I/O	•
C. Interrupt-drive	en I/O
D. Direct memory	access (DMA)
oo. Which bus is bid	irectional?
A. Address bus	
B. Data bus	
C. Control bus	
D. None of the abo	ove
89. The first micropi	rocessor has a (n)
A. I – bit data bus	B. 4 - Bit data but
C. 2 - Oit data bus	S D. 8 – bit data bus
90. Which micr	oprocessor has
A. 8086	and address lines?
C. 80286	B. 80386
91. Which is not an o	D. Pentium
A. Variable	perand?
B. Memory location) n
C. Register	лі
D. Assembler	
16 Computer Organizat	tion and Embedded Syst

92.	Which is not n	9rt
	(EU)?	art of the execution
	A A 1.1	aoitu

- A. Arithmetic logic unit (ALU)
- B. General registers
- C. Clock
- D. Flags
- 93. A 20-bit address bus can locate A. 1,048,576locations
 - B. 4,194,304locations
 - C. 2,097,152locations
 - D. 8,388,608locations
- 94. Which of the following is not an arithmetic instruction?
 - A. INC (increment)
 - B. DEC (decrement)
 - C. CMP (compare)
 - D. ROL (rotate left)
- 95. During a read operation the CPU fetches_
 - A. A program instruction
 - B. Data itself
 - C. Another address
- D. All of the above
- 96. Which of the following is not an 8086/8088 general-purpose register?
 - A. Code segment (CS)
 - B. Stack segment (SS)
 - C. Data segment (DS)
 - D. Address segment (AS)

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M.	SHEET
CR	SHELD
WELL	

1.51	VD.		STATE OF THE OWNER, WHEN						
13		3.B	4.A	5.C	6.A	7.B	8.A		
18	2.A	17:C	18.A	19.B	20.A	21.B		9.D	10.B
15.C	16.A	31.A	32.A	33.B	34.A	35.C	22.A	23.B	⁻ 24.A
19.A	30.A	43.C.	44.A	45.B	46.C		36.C	37.A	38.B
11.A	42.B		58.A	59.B		47.A	48.A	49.C	50.C
55.A	56.B	57.C) desided		60.C	61.C	62.A	63.C	64.A
69.C	70.A	.71.C	72.C	73.A	74.D	75.A	76.A	77.B	78.A
83.C	84.A	85.D	86.A	87.D	88.B	89.B	90.A	91.D	92.C
97.A	98.D	99.B	100.D	11.A	12.A	13.B	14.A	25.C	26.C
97.A 27.A	28.B	39.A	40.A	31.A	32.A	51.B	52.C	53.A	54.C
65.A	66.C	67.C	68.C	79.B	80.A	81.B	82.C	93.A	94.A
95.D	96.D		. W						