FACULTY OF COMPUTING

SEMSTER 1 2025/2026

ELEVATOR CONTROLLER SYSTEM

SECR1013-02 DIGITAL LOGIC

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GROUP'S NAME: THE JULIA'S

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DEDICATION AND ACKNOWLEDGEMENT

First and foremost, praises and thanks to the Allah SWT, the Almighty, for His blessings and giving us strengths to accomplish this mini project successfully.

Therefore, we would express our deepest and sincere gratitude to our Digital Logic lecturer, Mr. Ahmad Fariz bin Ali, for giving us opportunity to carry out this project. His valuable guidance, continuous support and advice throughout the project have greatly contributed to its successful completion. Without his dedication and encouragement, this project would not have achieved its intended outcome.

We also wish to extend our appreciation to the Faculty of Computing and the institution for providing the necessary facilities, resources and a learning environment that supported the execution of this mini project.

Furthermore, this project would not have been completed without the effort, cooperation and strong commitment of our group members, Farah Adilah binti Azman, Najla Auni binti Mohamad Asri, Nurul Izzati Liyana binti Hashim and Nur Nazirah Hanis binti Nazri. Each member played an important role, fulfilled their responsibilities and contributed effectively to ensure the successful completion of this project.

Last but not least, all assistance and contributions, whether direct or indirect, are sincerely appreciated. Thank you.

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1.0 BACKGROUND AND OVERVIEW

An electronic controller is a vital device that governs the operation of an elevator in a building. It plays a crucial role in managing elevator movement, ensuring precision, safety, and overall efficiency in vertical transportation systems. The design and implementation of this project involve integrating various components, including counters, comparators, clocks, and other digital logic elements to achieve accurate and reliable control of the elevator system. For the elevator to move from one floor to another, the controller must receive an input signal and process it to generate the appropriate output. Our inputs for this project are the determinant of the counting direction, X and Q2, Q1, and Q0 that comes from the 3-bit JK flip-flops. A 3-bit synchronous counter using JK flip-flops is implemented to manage the counting sequence, allowing the elevator to operate efficiently across an 8-floor hotel elevator, either counting up or down as required.

The usage of synchronous counter in this project is for its ability to produce an output simultaneously while having a clock input that comes from a single source. This ability suits the mechanism of the operation of an elevator where all outputs for each flip-flop must be generated at the same time to enable the operation of the elevator. Inputs from PRESET and CLEAR with the highest priority needs to be used for the synchronous counter to operate, where they will both be set to high. The complete design of the system should demonstrate how the counting will go up or down by each level until the desired level is reached and continue to remain at the same level until an input is changed, validating the counter as a saturated counter.

2.0 PROBLEM STATEMENT

The project challenged our ability to enhance the previous design of a 4-floor elevator system to support 8 floors integration. This requires the judgement and modification on each aspect and perspectives, especially on the usage of a 3-bit synchronous of JK flip-flops compared to the previous design of using D flip-flop. The execution of creating state tables, K-Maps, and deriving equations will become more complex with a higher attention to details to ensure no error is made. In addition, the introduction of several new features into the system such as a PIN-based access control, visitor card hotel identification and opening or closing of the elevator door indication will be integrated as the input, showcasing a high-level security of the system. All inputs including the Power and Start need to be validated as high in order for the elevator to start functioning, as they will all be connected to an AND gate that leads to the clock input. The solution to this problem will involves the implementation in DEEDS design, drawing of several diagrams and the demonstration of our whole solution, ensuring the system can work functionally and fulfilling the requirement of the project.

3.0 SUGGESTED SOLUTION

The suggested solution for the 8-floor hotel elevator controller is centred on a 3-bits up-down synchronous counter design implemented with JK flip-flops. To manage the navigation between Level 0 and Level 7, a state diagram and state table are begun with by the design process to map transitions based on the direction input X. As noted by Adnan et al. (2017), digital logic implementation is essential for creating structured and dependable operational flows in elevator systems. These are then converted into a transition table to determine flip-flop excitation, which is simplified using 4-input K-maps incorporating variables X, Q2, Q1, and Q0. This systematic approach ensures an efficient gate configuration that eliminates "glitches" and ensures synchronized state changes across all bits during floor transitions.

The operational flow involves a target floor being selected by the user via 3-bit input switches, while the counter's real-time output is continuously monitored against this target by a comparator. To comply with the hotel's safety measures, a "Clock Enabler" logic is incorporated, so movement is activated by the pulse generator only if the visitor card is tapped, the right passcode is entered, and the closure of the door sensor is confirmed. As soon as a match between the present floor and the target input is identified by the comparator, a clock disabler is activated that stops the counter, thereby bringing the elevator exactly to the wanted floor with precision.

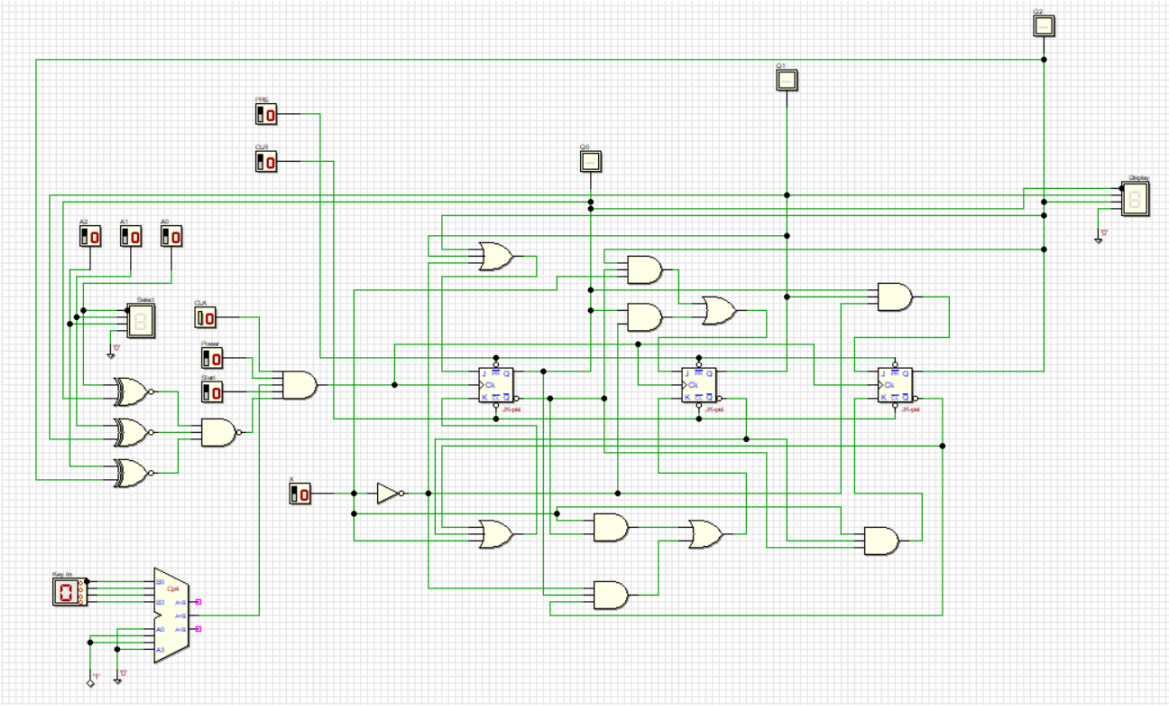

Figure 1.0: Circuit using Deeds Simulator

For our DEEDS implementation, a single integrated circuit was designed by us that combines the counter logic with the security and control systems. In our circuit design, three JK flip-flops were opted for by us because three bits were required, and the MOD 8 was especially suited for this lift project, thus enabling the system to indicate 8 different states. For all the flip-flops, they are made by us as up-down synchronous counters to make certain that the elevator moves through the binary states 000, 001, 010, 011, 100, 101, 110, and 111 corresponding to Level 0 to Level 7. With these states, a state diagram was created with transitions marked as 0 and 1. A 0 input leads to the counting up sequence which means the lift is ascending, whereas a 1 input activates the counting down sequence indicating the lift is descending. For the realization of this, the excitation equations were obtained by us through 4-input K-maps, and the flip-flop inputs were connected by us so that the whole transitions are perfectly in sync with the clock pulse.

Within the same circuit, the control and security logic was integrated by us to interact directly with the counter. This includes a 3-bit digital comparator that matches the counter's current state with the user's target floor switch. Furthermore, an AND-gate logic network was incorporated that worked as a clock disabler and allows the pulse to reach the flip-flops only if the visitor card is tagged, the passcode is correct and the door is closed. After that, it is determined by the comparator that the lift has reached the required level, and a signal is sent to stop the pulse thus the lifting is stopped. Meanwhile, the outputs are wired to a 7-segment display and status LEDs, thereby giving the user a clear visual representation of the current floor and door status.

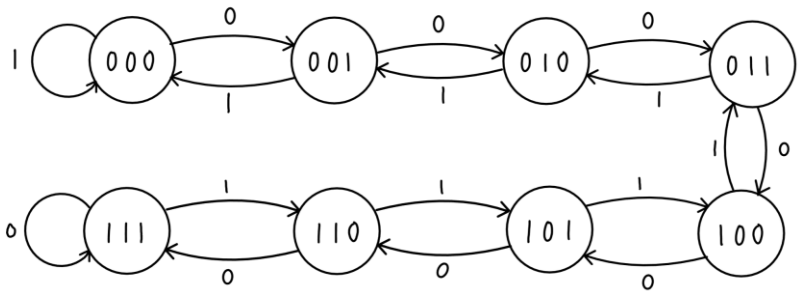

Figure 1.1: State Diagram

The making of a transition table is the next step in the counter design process, and the way to the K-maps and Boolean expressions for the J and K inputs of all three flip-flops, Flip-Flop 1, 2, and 3, is shown to us. The minimized logic necessary for every terminal was created by us by reducing these 4-input K-maps as detailed below. The blueprint for our final circuit design is served by these expressions, enabling the implementation of a precise and 3-bit up-down synchronous counters for the elevator system.

Input X	Present State			Next State			JKFF					
	Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	1	1	1	X	0	X	0	X	0
1	0	0	0	0	0	0	0	X	0	X	0	X
1	0	0	1	0	0	0	0	X	0	X	X	1
1	0	1	0	0	1	0	0	X	X	1	1	X
1	0	1	1	0	1	1	0	X	X	0	X	1
1	1	0	0	1	0	0	X	1	1	X	1	X
1	1	0	1	1	0	1	X	0	0	X	X	1
1	1	1	0	1	1	0	X	0	X	1	1	X
1	1	1	1	1	1	1	X	0	X	0	X	1

Figure 1.2: Transition Table

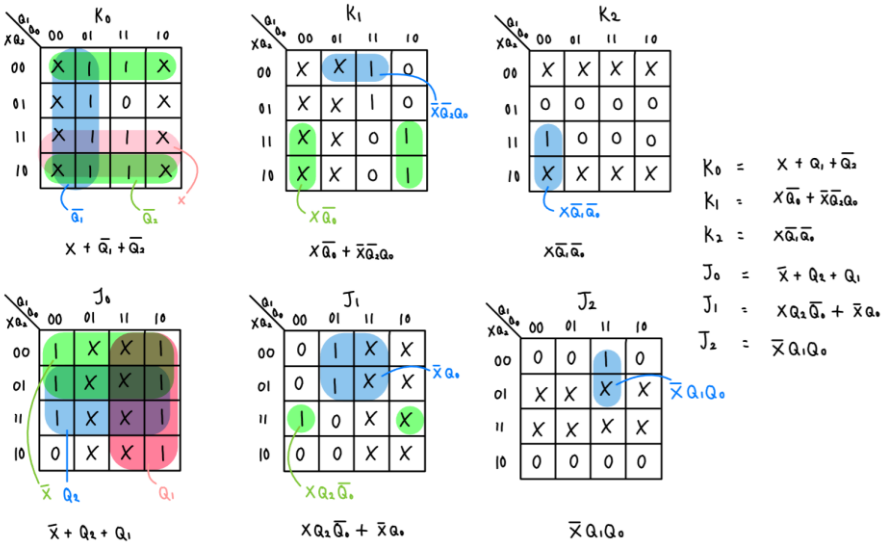

Figure 1.3: 4-input Karnaugh Maps (K-maps)

In the case of the comparator section, the XNOR gate was opted for by us to function as a comparator since it is indicated by the XNOR gate truth table to be an output HIGH (1) only when both inputs are identical. To achieve this, three (3) XNOR gates were cascaded by us to measure the 3-bit target level, set by the input switches, against the present state output of each JK flip-flop. The desired floor is represented by the input switches, while our current position is represented by the flip-flop outputs. The outputs from these three (3) XNOR gates are then fed into a NAND gate. If all bits match, meaning the current floor is identical to the target floor, a LOW output (0) will be sent by the NAND gate to the clock disabler to stop the pulse and halt the circuit.

As described by Mushtaq (2021), the coordination between the motor represented by our counter and user inputs is the core of elevator functionality. The system needs to be initialized by applying PRE (Preset) and CLR (Clear) inputs to get the circuit working in this case. After initializing, the input for X is set by us, where 0 makes the lift go up and 1 makes the lift go down. Next, the floor is specified by us using the input switches, which is shown on the 7-segment display. The last step is to give the clock pulses so that the elevator states are changed, meaning a match will be identified by the comparator, at which time the clock is turned off, denoting that the desired floor has been reached by us.

4.0 SYSTEM IMPLEMENTATION

1. **Initialize the system**

   Set the **PRE**, **CLR**, **Power** and **Start** input to 1. This enables the counter and resets the **Display** output to **0**.

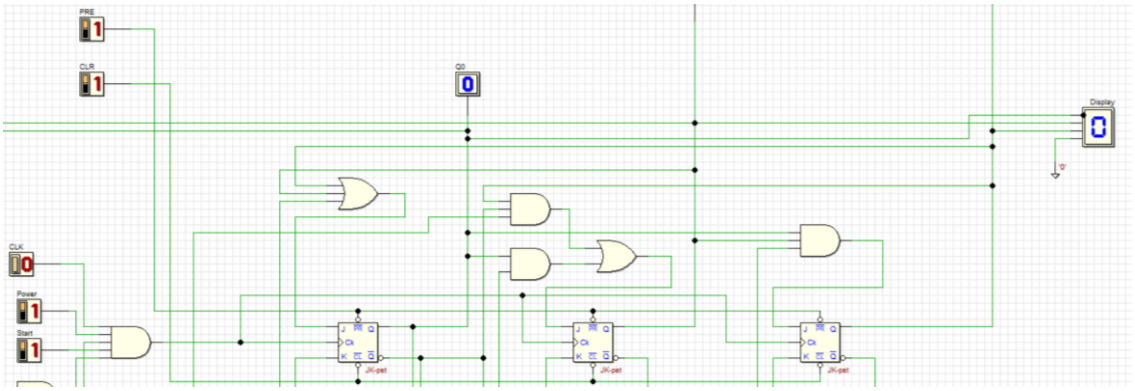

Figure 2.0

2. **Enter the password**

   Input the correct password using the **hex 'Key In' input** to activate the elevator. In this demo, the password is **0110**, which is **6** in decimal.

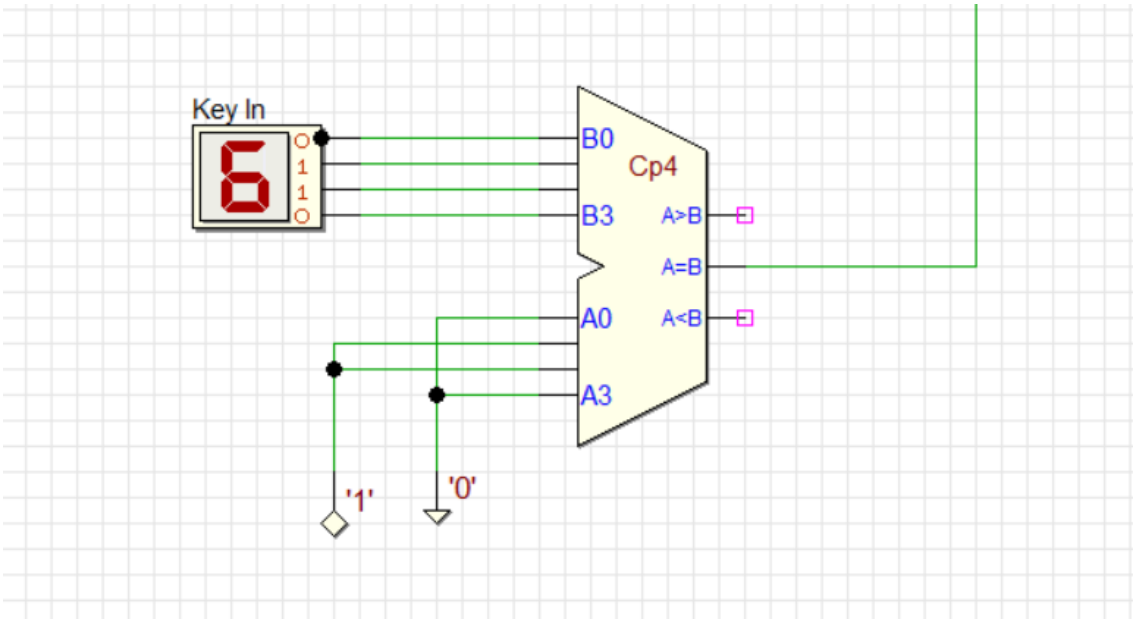

Figure 2.1

3. Choose the destination

Set the X input to choose the direction of movement enter 0 to go up and enter 1 to go down.

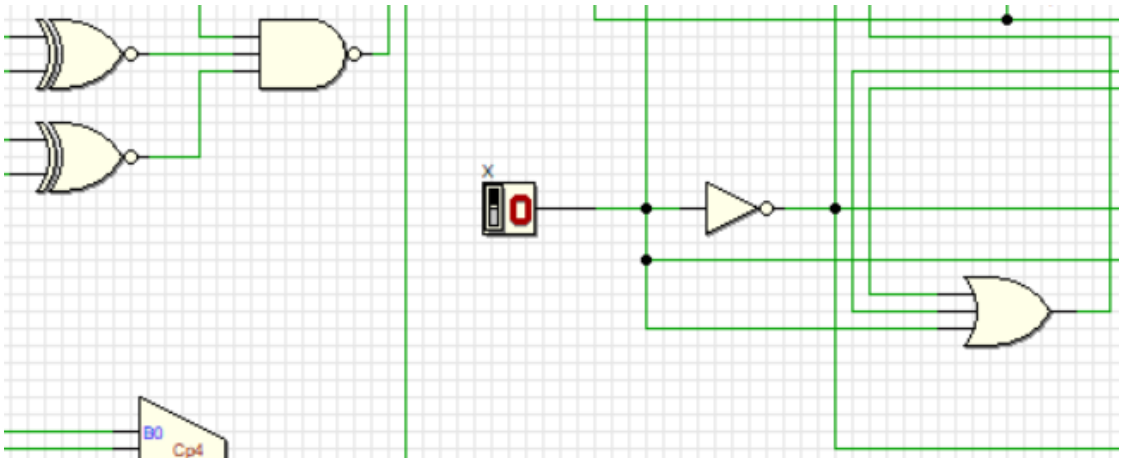

Figure 2.2

4. Select desired floor

Decide which floor you want to go and enter its **binary value** into **A0**, **A1**, and **A2** input and the **hex 'Select' output** will display its **decimal value**.

Example: If the elevator is at **level 2** and you want to go up to **level 7**, then you need to enter the binary value of 7 which is **111** into **A0**, **A1**, and **A2** input respectively.

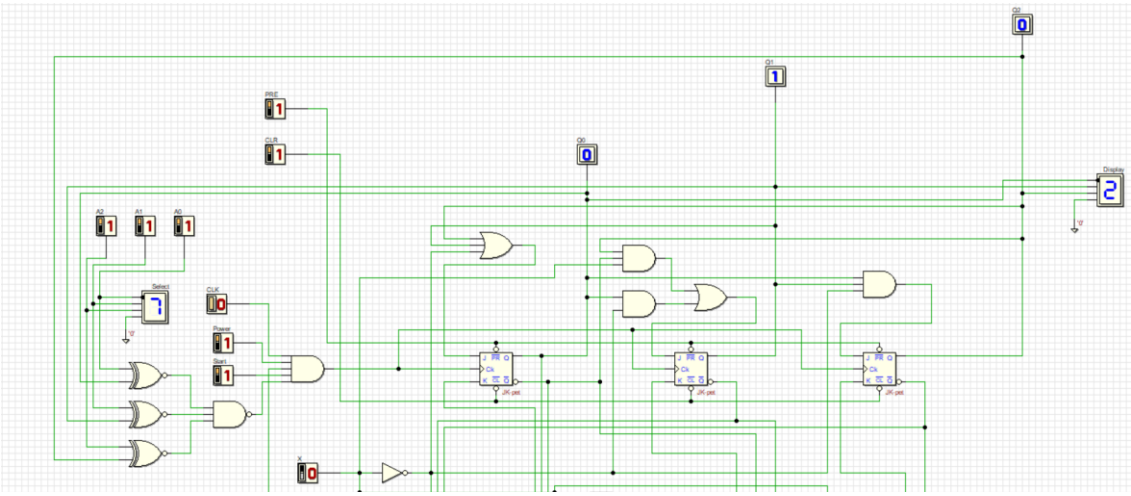

Figure 2.3

5. **Run the elevator**

Apply clock pulse until the Display output is the same as the level output (e.g.: 7). At this point, the output Q0, Q1 and Q2 will match A0, A1, and A2 respectively indicating that we have reached the selected floor.

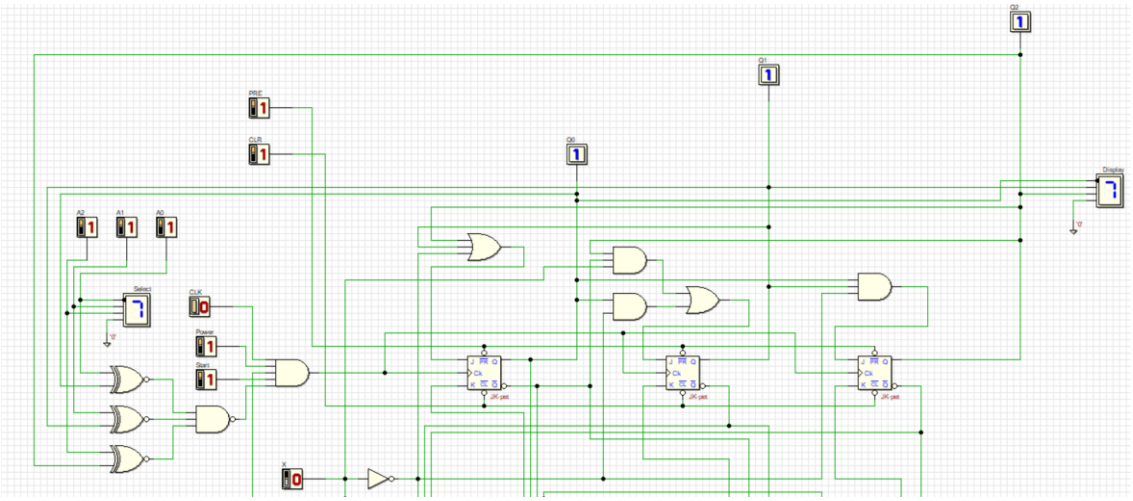

Figure 2.4

5.0 CONCLUSION & REFLECTIONS

5.1 CONCLUSION

In conclusion, the digital logic design and implementation used in our 8-floor Elevator Controller project have been proven to be crucial to the achievement of dependable and effective lift operation across levels 0 through 7. A system that successfully addresses the complex requirements of multi-floor navigation and security has been developed by us by making use of digital logic concepts, meticulous planning, and thoughtful circuit design. With the help of logic gates, JK flip-flops, and a 3-bit up-down synchronous counter, how to integrate these parts to create a responsive and secure lift control system that incorporates visitor card detection and passcode verification has been successfully shown by our project. For the elevator to seamlessly move between different states while ensuring safety and precision, the application of finite state logic, transition tables, and 4-input K-map simplifications has been necessary to ensure the system operates without error in the DEEDS (Digital Electronics Education and Design Suite) simulation environment.

REFLECTION

FARAH ADILAH BINTI AZMAN: Working on the elevator simulation in DEEDS helped me better understand how digital circuits work in a more practical way. Instead of just learning the theory, I was able to see how different inputs and signals control a system, like how a real elevator operates. When the circuit did not behave as expected, I had to troubleshoot and test different settings. This process helped me realize how important proper initialization is for any digital system to function correctly. One of the challenging parts was making sure the elevator stopped at the correct floor. This required patience and close attention to the display and output values. Overall, this project improved my confidence in using DEEDS and helped me connect classroom concepts to a real-life application. It showed me that even simple logic components can be combined to create a useful and realistic system.

NAJLA AUNI BINTI MOHAMAD ASRI: This project significantly deepened my understanding of sequential logic design and its practical application in real-world scenarios. Moving from 2-bit to 3-bit logic spoiled the critical need of accuracy in K-map simplification for me, as it was found out that one mistake only might ruin the whole 8-floor elevator system's sequence of floors. The more I could do with a group, the more imaginative answers for the passcode and card detection logic were able to be come up with by me, thus, the working atmosphere of a professional engineering project was perfectly reflected by our activities. A considerable amount of confidence in the use of the Deeds Simulator for troubleshooting, designing, and visualizing complex digital systems has been gained by me through this hands-on experience. However, the door has been opened for me by this trip to move from the theoretical concepts taught in class to the practical side of it and, thus, my digital logic problem-solving skills have become more versatile as classic.

NURUL IZZATI LIYANA BINTI HASHIM: Completing this project was a valuable opportunity for me as I was able to obtain many takeaways that can help my overall understanding of this course. Working on a practical example while applying the theoretical knowledge that I had learned from slides and lectures gave me a clearer view on the objective of several topics being applied in this project. Furthermore, designing a solution to this project has developed my critical thinking and problem-solving skills as well as my team-working ability by the conduction of work in group environment through meticulous discussion and planning. One of the important aspects in this project is the thinking process on how to apply the requirements instructed into the circuit, such as the clock enabler and the passcode system, as several trial and errors were tested to obtain the final verdict. Moreover, this project has also enhanced my ability to troubleshoot especially in the DEEDS simulator and during creating K-Maps and table diagram. Safe to say that one should be extra cautious especially involving project with a lot of details to ensure one overlooked mistake wouldn't ruin the whole circuit. Thankfully, working in group has given us the advantage when dealing with any troubleshooting problems.

NUR NAZIRAH HANIS BINTI NAZRI: This project required me to work on an elevator simulation using DEEDS. It helped me understand the theory of sequential logic and how it is applied in real-world contexts. It also strengthened and expanded my knowledge of sequential logic as I was able to observe how each input and signal affected the system's output. Through this project, I learned the importance of every step, from designing the state table to testing the circuit, in ensuring that the circuit functions accurately. The project also required focus and patience to verify that all outputs were correct. Furthermore, this project helped in enhancing problem-solving skills especially in debugging circuit errors. Lastly, since the project was completed in a group, it improved my communication and teamwork skills, as my team and I collaborated to successfully complete the assigned tasks.

5.2 ACHIEVEMENTS

The main achievement of this project is the successful design and simulation of an 8-floor hotel elevator control system based on a 3-bit up-down synchronous counter implemented using JK flip-flops in DEEDS. This project allowed us to effectively apply the theoretical knowledge acquired in class to the design and implementation of the elevator control system. We utilized DEEDS for simulation, K-maps for logic simplification, and developed state diagrams and transition tables to systematically represent and analyze the sequential behaviour of the system.

Another achievement is that we successfully integrated the state transitions and input buttons for floor selection to manage floor requests and control elevator movement across all eight levels. We also implemented up and down indicators to provide clear elevator's direction, and incorporated passcode to ensure restricted access to enhance the safety and security features of the elevator.

The next achievement is that through this project, we gained a practical understanding of flip-flops, counters, and logic components used in sequential circuit design. The implementation reinforced theoretical concepts learned in class and strengthened our understanding of synchronous systems.

Another achievement is that we improved our problem-solving skills in debugging circuit errors through repeated testing and refinement. Errors encountered during simulation were analysed and corrected to ensure the accurate and reliable outcome.

5.3 STRENGTHS & WEAKNESSES

Strengths

One of the main strengths of our project was our teamwork and persistence. Even when we faced difficulties, especially with the K-map simplification, we did not give up easily. We attempted the K-map several times and reviewed our logic until the circuit started to make sense. Through this process, we gained a deeper understanding of how Boolean expressions affect the overall system design.

Another strength was our willingness to seek guidance when we were stuck. With the help of our lecturer, **Sir Ahmad Fariz**, we were able to identify our mistakes and correct the K-map. His explanations helped us understand where we went wrong and how to approach the problem more systematically. This guidance allowed us to get the correct solution and improve the functionality of our elevator simulation.

Weaknesses

One weakness of our project was our initial lack of accuracy in designing the K-map. We underestimated its complexity, which led to multiple errors and caused delays in designing the circuit. Having to redo the K-map and the circuit several times showed that we needed a stronger foundation in logic simplification before starting the implementation.

Additionally, the repeated revisions took up a lot of time, which could have been used to further enhance the project. This highlighted the importance of careful planning and verification at an early stage to avoid redoing the whole project repeatedly.

Overall, these weaknesses became valuable learning points. By overcoming them, we improved our understanding on K-maps, strengthened our problem-solving skills, and learned the importance of asking for help when needed.

5.4 IMPROVEMENTS

Several improvements can be made as successful completion of our project were achieved, which can serve as a side note for our future projects. First and foremost, improvement on the circuit operation, where a feature such as the LED lights can be added for us to check whether our output for each element is functioning as intended or the otherwise. This can lead to an easier modification on the circuit as we can easily spot where our circuit has gone wrong and minimize the time usage on the production of the whole circuit, providing more time to focus on other difficult aspects.

Other than that, improvement can also be made on the production of the whole circuit, whereas several other elements can be added to further improve our design simulation. For example, more comparators can be added for the passcode section to enable the passcode to have more digits, which can increase the security level of the building to have higher efficiency.

Not only that, specific section for each input such as the identification of the visitor card hotel and opening or closing of the elevator door indication can be added to add more details to our whole project. This can be done through the use of sensors, more comparators and other elements that can serve the purpose.

One final improvement to be added into this project is the security major, as said by Masila Jane Mwelu (2009) in her research report, no one would dare to use an elevator system without safety mechanism. Hence, a few examples of safety measure can be taken, such as the feature to detect the weight limit, door blockage detector or fire detector.

6.0 REFERENCES

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7.0 APPENDICES

TASK DISTRIBUTION

No.	Team Members	Task
1.	Farah Adilah binti Azman A25CS0217	• Report writing (System Implementation, Strengths & Weaknesses) •
2.	Najla Auni binti Mohamad Asri A25CS0117	• Report writing (Suggested Solution (Explanation), Conclusion) •
3.	Nurul Izzati Liyana binti Hashim A25CS0336	• Report writing (Background & Overview, Problem Statement, Improvements) •
4.	Nur Nazirah Hanis binti Nazri A25CS0319	• Report writing (Suggested Solution (Drawings), Acknowledgement, Achievements) •

Table 1.0: Task distribution between team members

PROOF OF MEETING/DISCUSSION

Figure 3.0: Physical discussion on the project