Parallel Computing for GPUs using CUDA Homework 4

Mustafa İzzet Muştu 504211564

June 2, 2023

Development and Test Environment

The operating system on the host machine is Ubuntu 22.04 and nvcc version is V12.1.105. Hardware information is as follows: AMD Ryzen 7 5800X, 32 GB 3400 MHz, MSI RTX 3060 12 GB.

1 Optimized Dense Matrix-Matrix Multiplication using GPUs

Algorithm 1 Tiled dense matrix-matrix multiplication kernel pseudocode

```
Require: A, B, TILE WIDTH, Width
Ensure: C = AB
  shared_A[TILE\_WIDTH][TILE\_WIDTH]
  shared_B[TILE\_WIDTH][TILE\_WIDTH]
  bx \leftarrow blockIdx.x
  by \leftarrow blockIdx.y
  tx \leftarrow threadIdx.x
  ty \leftarrow threadIdx.y
  row \leftarrow tv + blockDim.v \cdot bv
  column \leftarrow tx + blockDim.x \cdot bx
  result \leftarrow 0
  for i = 0, i < (Width-1)/TILE_WIDTH + 1, i += 1 do
       shared_A[ty][tx] \leftarrow A[row \cdot Width + i \cdot TILE_WIDTH + tx]
       shared_B[ty][tx] \leftarrow B[(i \cdot TILE_WIDTH + ty) \cdot Width + column]
       syncthreads()
       for j = 0, i < TILE_WIDTH, j += 1 do
           result + = shared_A[ty][j] \cdot shared_B[j][tx]
       end for
       __syncthreads()
  end for
  C[row \cdot Width + column] \leftarrow result
```

Trial/Run Time (s)	2 Matrices Initialization on Host	1 Matrix Initialization on GPU	Matrix Multiplication Kernel on GPU	Matrix Multiplication on CPU (1 thread)
1	0.0122	0.0006	0.0038	4.1031
2	0.0123	0.0006	0.0039	3.9985
3	0.0119	0.0005	0.0035	3.8982
4	0.0121	0.0006	0.0039	4.0941
5	0.0122	0.0006	0.0036	3.9992

Table 1: Results when the tile width is 32.

1.1 Measure the running time of your kernel with a matrix size of N=1024x1024, M=1024x1024.

I implemented the tiling optimization only. The Pseudocode of the used kernel is shown in Algorithm 1. I set the block dimension which is also tile width as 32x32 (maximum number of threads per block) and utilized CUDA unified memory model. At first, I created 3 matrices with cudaMallocManaged() function. I filled the first two between 0 and 100 on the host code. Then, I initialized the third matrix with an initializer kernel to improve the matrix multiplication kernel performance by removing the overhead of copying. (Only 1 matrix copy operation is removed, not all of them). To measure the running time of the kernel, I used clock() function from time header and set the precision as 5. I also measured the initialization times on the host and the GPU. Results can be seen in Table 1.

One thing to notice is that for the previous homework, I had the same configuration for the CPU multiplication function but I had better results (3.5 seconds). So, I realized that CPU performance is better with nvcc V12.1.105 on Windows 11. However, this situation may be unrelated to the OS, it may result better only because of further compiler optimizations. For the CUDA kernels, run times are very similar.

1.2 Do a performance profiling using NVVP/nvprof/NSight profiling tool and discuss the performance bottlenecks and identify opportunities for performance optimizations. If the occupancy is a problem work on the Block size to make sure you have enough occupancy per SM, then re-do the profiling. Compare your results against the very first version of your dense matrix-matrix multiplication implemented as part of homework 3.

I profiled the application using Nsight Compute. For the matrix multiplication kernel, I got 81.1% SM and memory throughput. For the occupancy, I achieved 66.75% occupancy. These results can be seen in Figure 1. Occupancy is the ratio of the number of active warps per multiprocessor to the maximum number of possible active warps. To increase this value, we can decrease the register and shared memory usage in threads and adjust the block size. Since tile width determines the shared memory usage and block size, we can decrease tile width to 16.

After reducing the tile width, I achieved 98.47% occupancy and 95.35% throughput. These

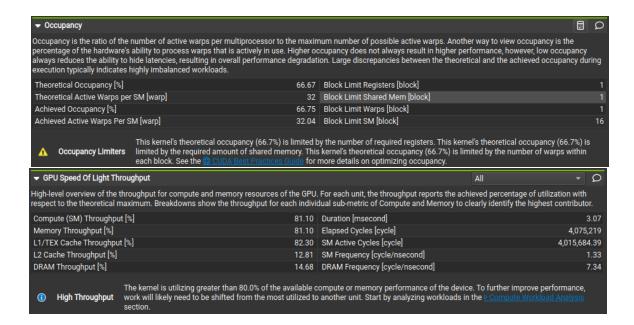


Figure 1: N=M=1024, tile width is 32.

results can be seen in Figure 2. For the run time, I did not notice any difference, so it is not included in the report.

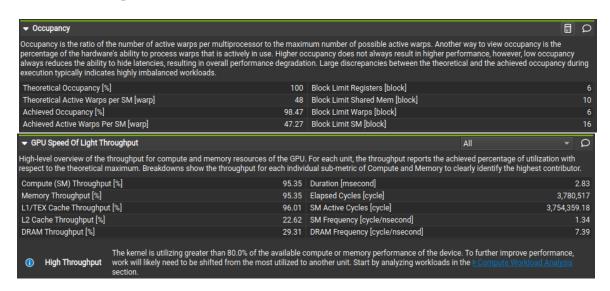


Figure 2: N=M=1024, tile width is 16.

1.3 Repeat the steps in (a) and (b) with matrix sizes of N=2048x2048, M=2048x2048 and N=4096x4096, M=4096x4096.

I set the tile width as 16 and did performance profiling. The throughput and the occupancy results can be seen in Figure 3 and Figure 4. For the run times, I run the kernel several times and measure the times. When N=M=2048, kernel time is approximately 33 seconds which is 2 seconds worse than the kernel time in homework 3. I discussed this situation in Section 1.1. Similarly, when N=M=4096, kernel time is approximately 286 seconds which is 30 seconds worse than the kernel time in homework 3.

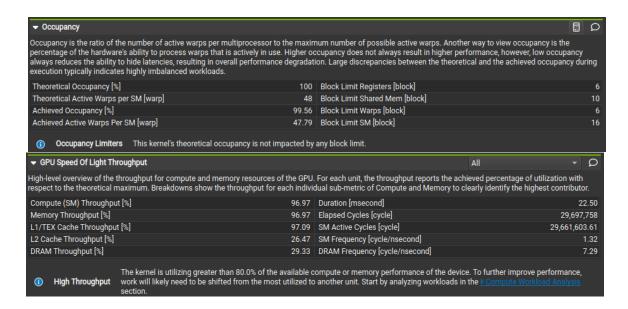


Figure 3: N=M=2048, tile width is 16.

Trial/Run	Nonoptimized	Optimized
Time (s)	Kernel	Kernel
1	0.0279	0.0226
2	0.0283	0.0232
3	0.0284	0.0235
4	0.0276	0.0232
5	0.0282	0.0238

Table 2: Nonoptimized and optimized kernel run time comparison.

To compare these results with the homework 3 results, I set the tile width as 16, N=M=2048, and rerun both kernels on the same OS after compiling them with the same nvcc version. I did not any difference when it comes to the throughput and the occupancy. However, the run time for the optimized GPU kernel is slightly better than the nonoptimized kernel. The difference is shown in Table 2.

2 Sparse Matrix-Matrix Multiplication using GPUs

I utilized the cuSPARSE library for this part of the homework. I downloaded 494_bus, 685_bus, and 1138_bus matrices from the given link. These matrices contain 1666, 3249, and 4054 nonzero values respectively. For implementation, I read the second and the third arguments of the program as input matrix names. After, I read the input matrices by using these file names to the COO sparse matrix structure I created and then I convert these structures to the cuSPARSE COO format. To be able to multiply 2 sparse matrices, I also convert matrices from cuSPARSE COO to cuSPARSE CSR because only CSR matrix format is supported for multiplication.

2.1 Measure the running time of your kernel.

The running times for the CPU code and cuSPARSE library kernel are shown in Table 3. One thing to notice is that the GPU kernel run times do not change between N=M=494 and



Figure 4: N=M=4096, tile width is 16.

N,M/Run Time (s)	Sparse Matrix Multiplication on CPU	Sparse Matrix Multiplication on GPU
494	0.0363	0.0003
685	0.1575	0.0003
1138	0.2234	0.0003

Table 3: The run times for the CPU code and cuSPARSE library kernel.

N=M=1138 even though the latter contains almost as twice much as the former.

2.2 Do a performance profiling using NVVP/nvprof/NSight profiling tool and discuss the performance bottlenecks and identify opportunities for performance optimizations. If the occupancy is a problem work on the Block size to make sure you have enough occupancy per SM, then re-do the profiling.

Although kernel run times seem too low compared to the CPU implementation, the occupancy and throughput results are much worse. When I did performance profiling, I encountered 30 different kernels in Nsight Compute. Since the cuSPARSE library does not share the kernel names and does not let us change the block size, I could not continue the further optimizations. Kernels used in cuSPARSE library and information about them is shared in Figure 5.

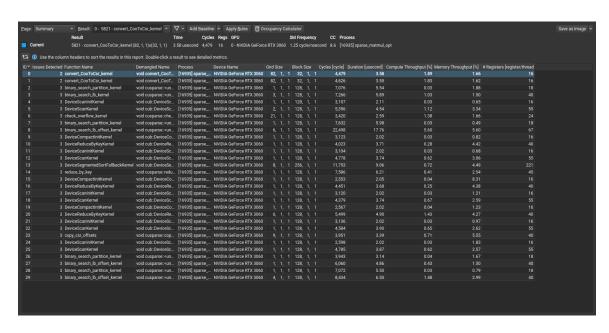


Figure 5: The cuSPARSE kernels and related information.