Penn Trigger Board Mk2

Jonathon Sensenig
University Of Pennsylvania
Dept. of Physics

April 18, 2017

Chapter 1

Intro

Penn Trigger Board Mk2 (PTB Mk2) is the second generation general purpose trigger board which builds of the first generation PTB. This board implements lessons learned in the first generation board along with utilizing more of the MicroZed (MZ) input/outputs (I/O).

The physical boaard design is straightforward due to the fact none of the logic operations on the input signals are performed on the board. The board simply performs logic translation to 3.3V LVCMOS logic for the incoming signals and from the aforementioned logic to whatever desired logic.

Chapter 2

Hardware: I/O

2.1

The board provides a number of I/Os, greater than the 115 I/Os on the MZ. This is handled by implementing I/Os on the board which cannot be used simultaneously. The signals are separate up to the interface which is simply a bank of resistors. The resistors can be stuffed for whichever I/O is needed, while the unused I/O is unstuffed. This allows the PTBMk2's total number of possible I/Os to rise to 185.

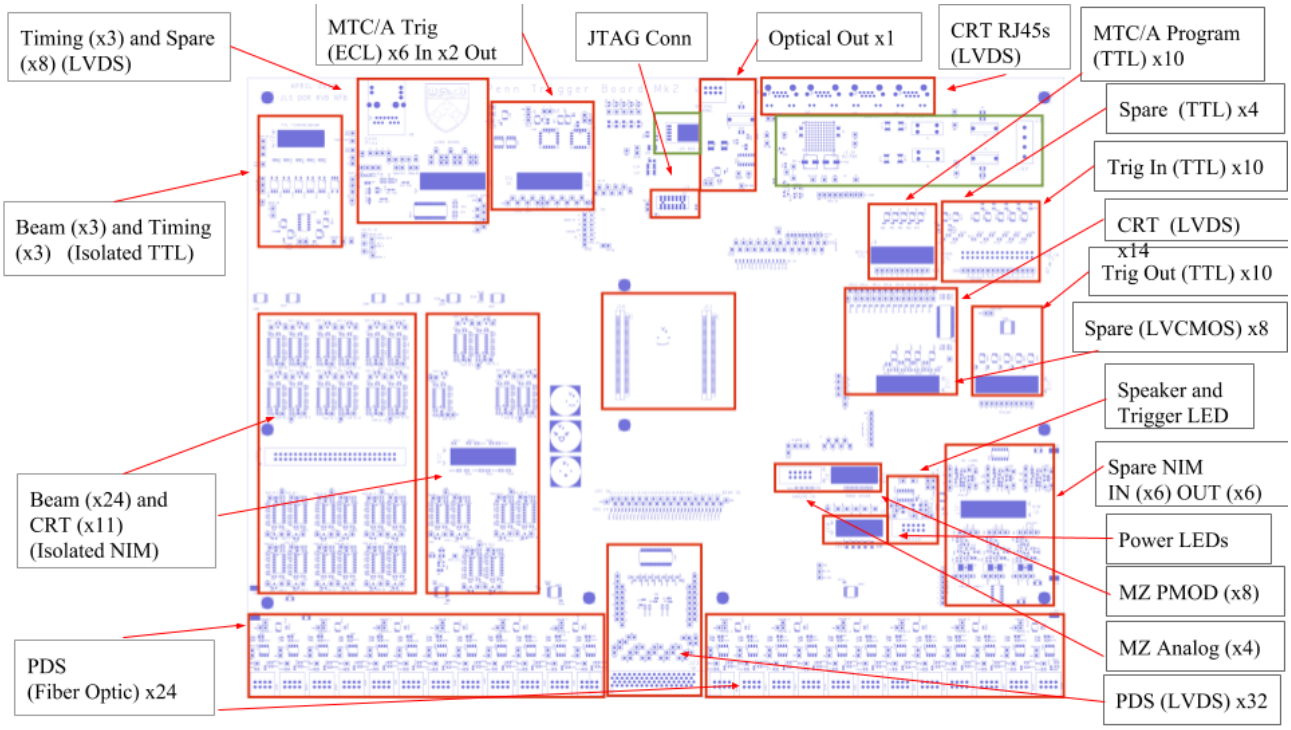


Figure 2.1: An overview of the physical location of the I/Os on the board.

2.2 Isolated TTL

Due to different GND references, building and detector in this case, there are 5 inputs and 1 output which are optically isolated from the board. This is meant for the beam (x3) and timing (x2) input and (x1) output, all for SBND. The output is somewhat of a "cheat" in the sense that the optoisolators are meant for signals coming into the board, incoming. To avoid having a separate power to drive the 1 outgoing timing signal,

the optoisolator is connected to the board's VCC and GND via 1k resistors. This allows small differences VCC and GND on the receiving end without causing any trouble.

2.3 Isolated NIM

This circuit capacitively isolates the NIM signal and amplifies it to 3.3V. The incoming signal is terminated to the GND of the driver and signal capacitively coupled via a resistor. A long-tailed pair of NPN transistors works to amplify and invert the NIM signal, negative going 800mV, to a positive going 3.3V signal which is buffered before entering the MZ LVCOMS I/O bank.

2.4 Isolated LVDS

LVDS is is very forgiving of GND differences, providing up to 1V of potential difference between driver and receiver GNDs, difference could vary with component. Here we use the TI SN65LVDM1666 which provides up to 16 channels of LVDS $\leftrightarrow$ LVCMOS, functioning as a driver and/or receiver. All the LVDS connections are fixed as either a driver or a receiver with the exception of the 8 spare channels. These channels are arranged in 2 banks of 4 channels where each bank can be configured as either a drive or receiver.

2.5 Optical

The optical consists of 24 inputs and 1 output. The optical receivers are Broadcom HFBR-2416, an analog receiver with ST connection. The transmitter is from the same family, an HFBR-1412 driven with a TTL signal, also with an ST connector. These are relatively slow optical components with a propagation delay of about 48 ns from the input of the transmitter to the output of the receiver, neglecting the light travel time through the fiber.

The analog signal from the receivers is converted to a digital signal with a fast comparator (LT1016). The thresholds for each of the 24 channels is set with a DAC, programmed from the MZ via an I^2C link.

2.6 LVCMOS

The 8 LVCMOS connections are spares and are almost directly from the MZ. They go through the SN74LVC2T45 which basically acts as a buffer. These are bidirectional chips where the direction is set by holding the DIR pin (pin 4) either high or low. This is practically accomplished by stuffing one of the 2 resistors connected to either GND or 3.3V.

2.7 TTL Stuff

The trigger has 10 TTL inputs and outputs. However, the outputs are controlled by a single signal from the MZ then run through a 1:10 fanout chip. The inputs are bidirectional and thus can be configured as in or outputs with a simple resistor swap, as described in Sec. 2.6.

There are 10 channels dedicated to program the MTC/A's, five per MTC/A. The channels are unidirectional since they share MZ pins with other logic conversion channels so therefore it is unlikely they will be used for something other than their intended purpose.

There are 4 spare TTL channels provided which rises to 8, repurposing 4 of the *Trigger In* channels, if it is not being used for the SBND experiment. These are bidirectional with the directional again set by a resistor.

2.8 ECL

The ECL connections are meant for the MTC/A's with 6 inputs and 2 outputs. The MTC/A's require and provide single ended ECL signals so the negative signals are held to the common-mode voltage via 50Ω

resistors. The aforementioned resistor can be removed and the termination resistor stuffed if differential signals are desired. Similarly, the output routes the differential signal pair to the connector, but will only use the positive signal for the MTC/A.

2.9 Configurations

Table 2.1: The available I/Os for the PTBMk2, although only 113 (123 if the 1:10 TTL fanout is used) of the 180 I/O possibilities can be used simultaneously.

		ECL	LVCMOS	LVDS	NIM	Optical	TTL
Regular	In	6	-	32	-	24	10
	Out	2	-	-	-	1	20*
Isolated GND	In	-	-	16	35	-	5
	Out	-	-	1	-	-	1
Spare	In	-	-	-	6	-	
	Out	-	-	-	6	-	
	I/O	-	8	8	-	-	4
Total: 185		8	8	57	47	25	40

(*) 10 of these signals are from a 1:10 fanout so they cannot be separately controlled.

Table 2.2: The SBND configuration of the board.

		ECL	LVCMOS	LVDS	NIM	Optical	TTL
Regular	In	6	-	32	-	-	10
	Out	2	-	-	2	-	20*
Isolated GND	In	-	-	14	-	-	5
	Out	-	-	-	-	-	1
Spare	In	-	-	-	6	-	
	Out	-	-	-	4	1	
	I/O	-	8	8	-	-	4
Total: 123		8	8	54	12	1	40

(*) 10 of these signals are from a 1:10 fanout so they are not separately controlled.

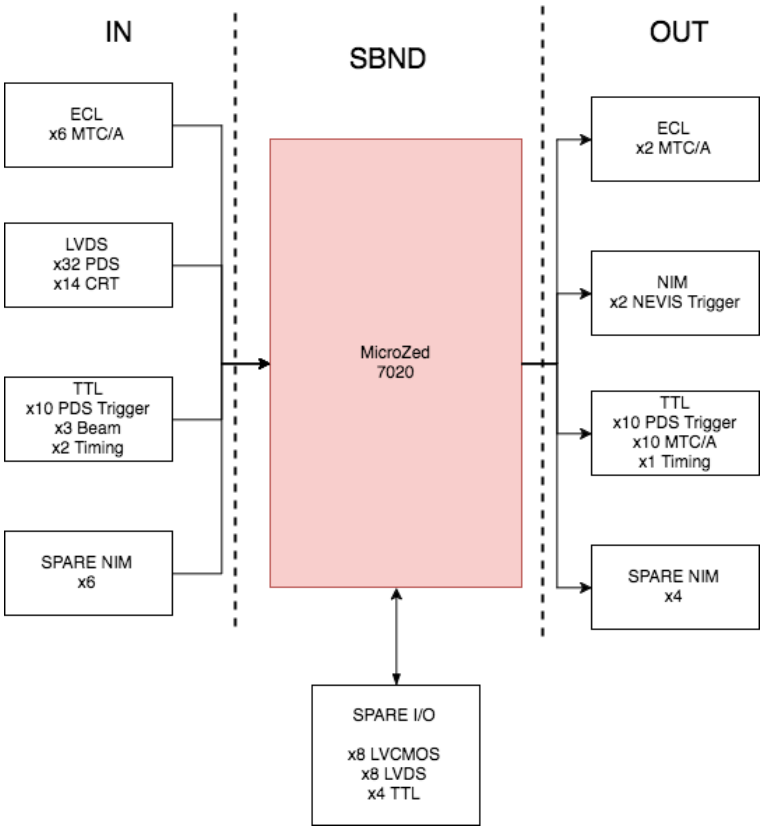


Figure 2.2: The MicroZed 7020 with IOs.

Table 2.3: The ProtoDUNE configuration of the board.

		ECL	LVCMOS	LVDS	NIM	Optical	TTL
Regular	In	-	-	-	-	24	-
	Out	-	-	-	-	1	-
Isolated GND	In	-	-	2	35	-	-
	Out	-	-	1	-	-	-
Spare	In	6	-	-	6	-	
	Out	2	-	-	6	-	10*
	I/O	-	8	8	-	-	8
Total: 117		8	8	11	47	25	18

(*) 10 of these signals are from a 1:10 fanout so they are not separately controlled.

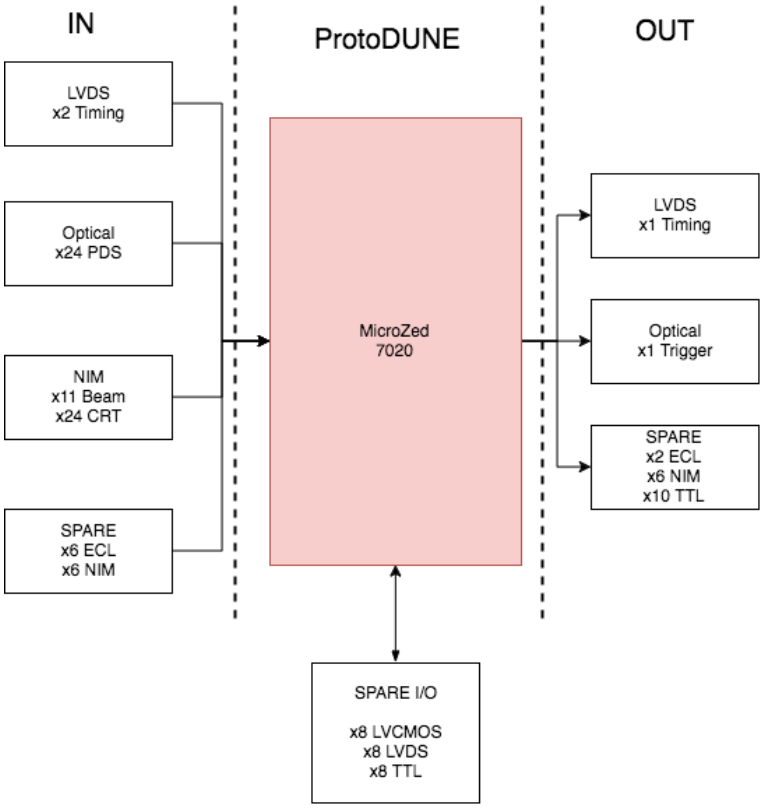


Figure 2.3: The MicroZed 7020 with IOs.

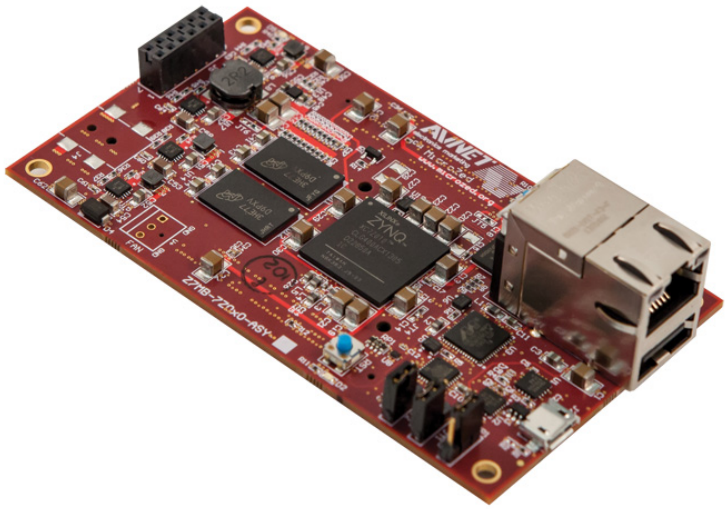


Figure 2.4: The MicroZed 7020 with a Xilinx FPGA and running a Linux distro.

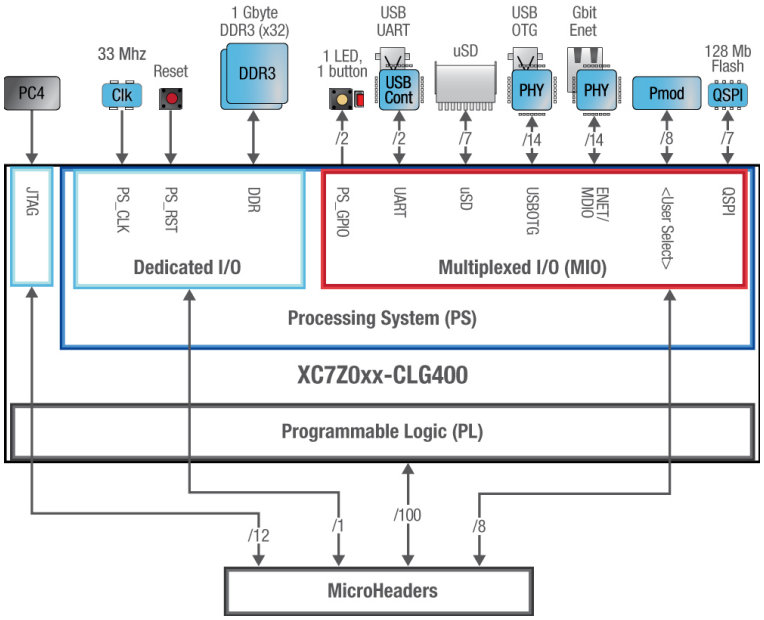


Figure 2.5: The MicroZed 7020 I/Os. The I/Os with dedicated connections on the PTBMK2 are addressed to the PL connections. The JTAG can be connected to for programming of the PL and

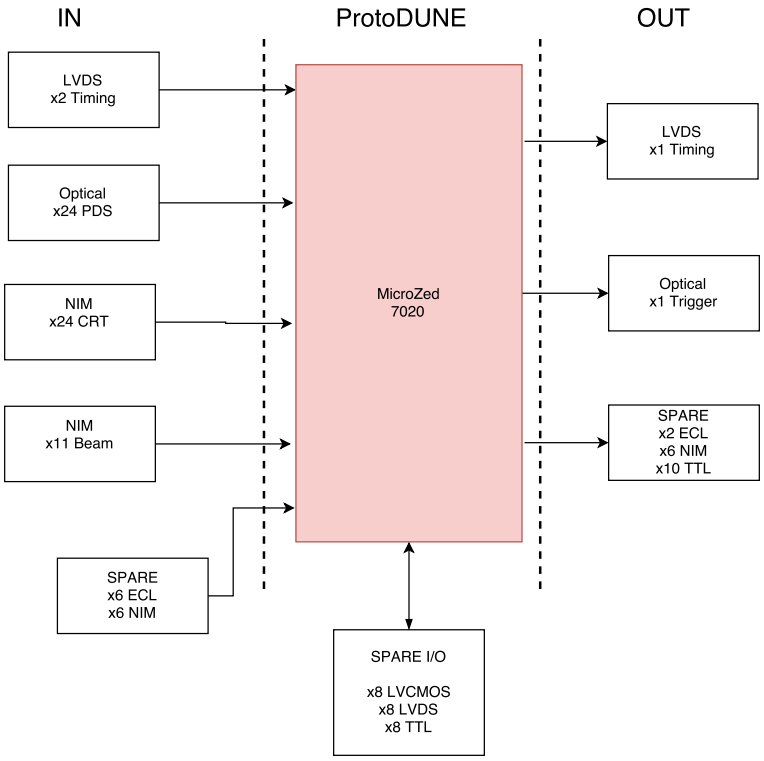


Figure 2.6

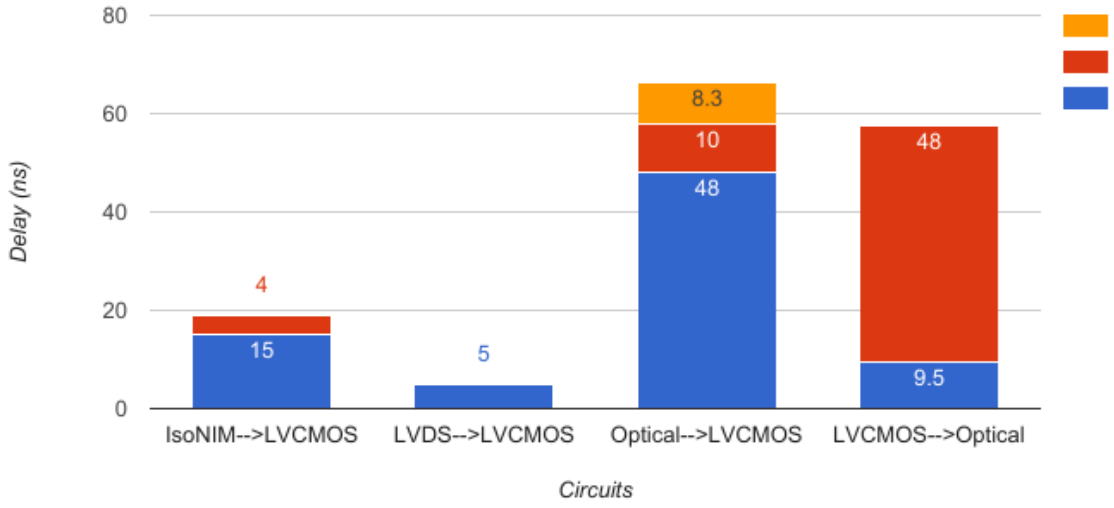


Figure 2.7: Circuit delay estimates.

Table 2.7: Physics requirements for the PDS electronics

Performance Parameter	Target
Time Resolution	Better than 30 ns wrt event time zero ("t0")
Charge Resolution	0.25 photo-electron equivalent
Dynamic Range	$\sim \times 10$ better than detector (1000:1)
Linearity	Sufficient to resolve 1 photo-electron signals
Multi-Hit Capability	Sufficient to measure Triplet (late) Photons
Dead Time	Live up to 2 drift times either side of beam spill
Bias Control	0.1 V resolution up to 30 V per channel
Calibration	On-board Charge Injection
Timing	Events time-stamped via ProtoDUNE Timing System

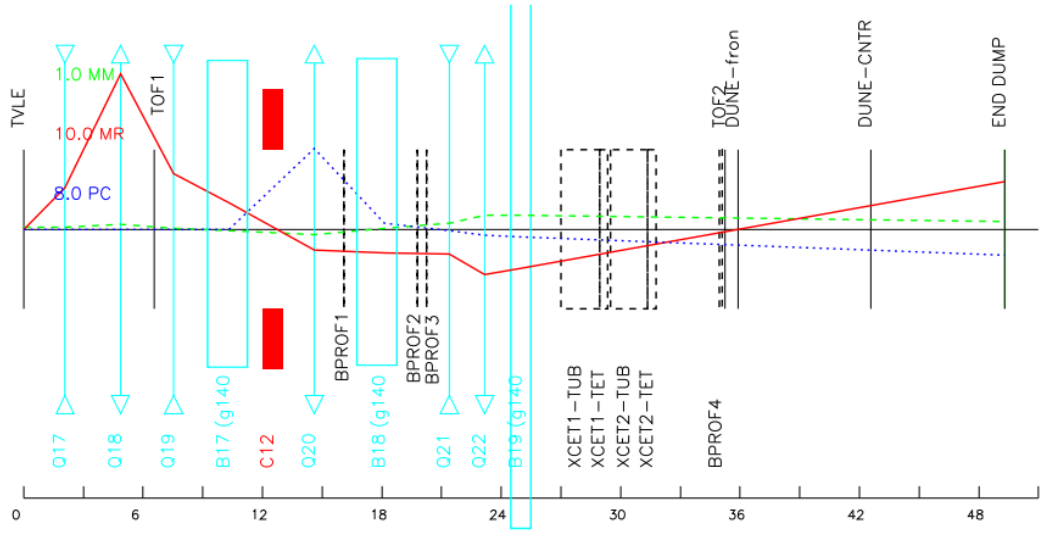
Figure 2.8: .

Table 6.1: Particle beam requirements. (Kaon rate is low for beam momentum below 2 GeV/c.)

Parameter	Requirements
Particle Types	$e^{\pm}, \mu^{\pm}, \pi^{\pm}, (K), p$
Momentum Range	0.5 - 7 GeV/c
Momentum Resolution	$\Delta p/p \leq 3$ %
Transverse Beam Size	RMS(x,y) $\approx$ 1 cm (At the entrance face of the LAr cryostat)
Beam Entrance Position	Beam # 3 (Figure 6.1) - Saleve side TPC
Rates	$\sim 25 - \sim 100$ Hz

#fig:beamwindow_loc

Figure 2.9: .



H4-VLE beam to Single Phase ProtoDune

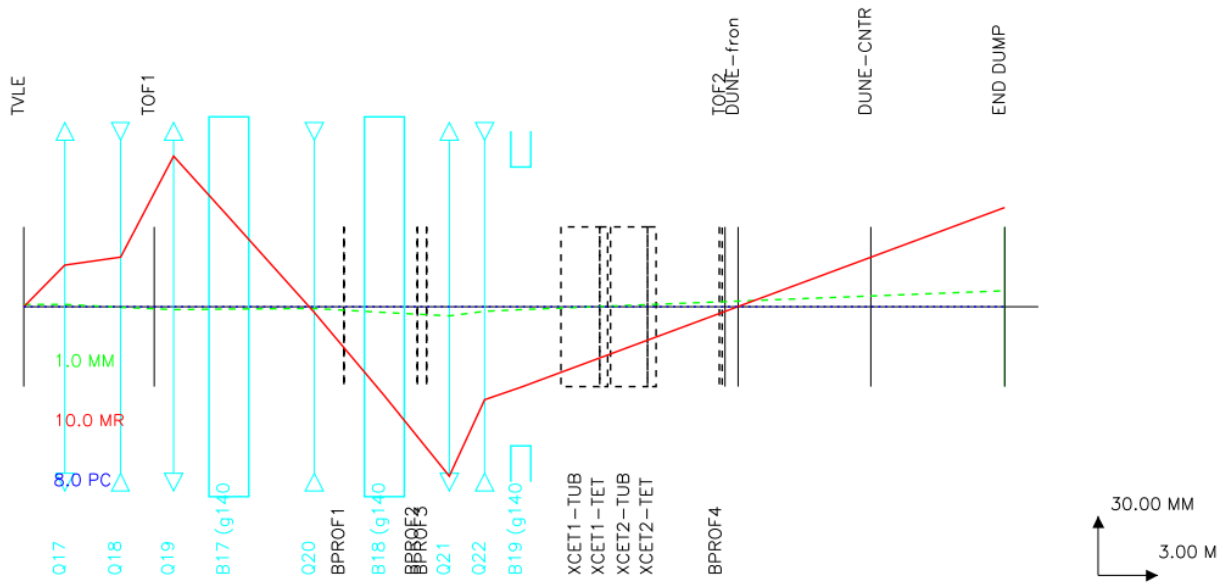


Figure 6.3: H4 beamline extension optics for the horizontal (top) and vertical (bottom) planes. The secondary target is located on the left side of the plots and the front of the ProtoDUNE-SP cryostat is located at the beam focus point, at about 37 m from the secondary target. Q17-Q22 are the quadrupole magnets. B17-B19 are the dipole bending magnets. TOF1-2 are the Time-of-Flight detectors, BPROF1-4 are the beam profile monitors, and XCET1-2 are the threshold Cherenkov counters.

Figure 2.10: .

Chapter 3

Crate