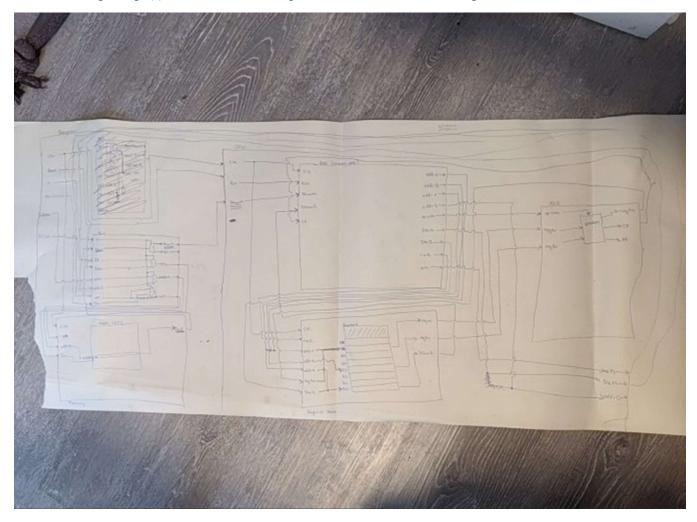
## ECE 4273 VLSI design

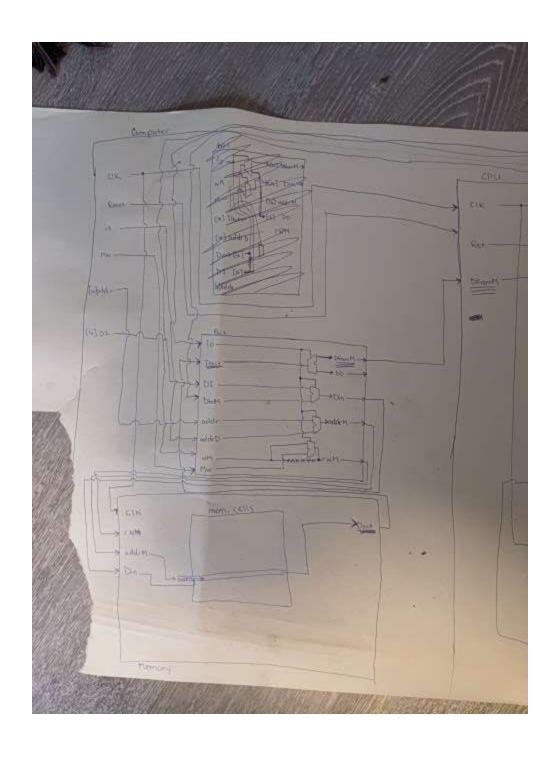
**Julie Brown, 3499594** 

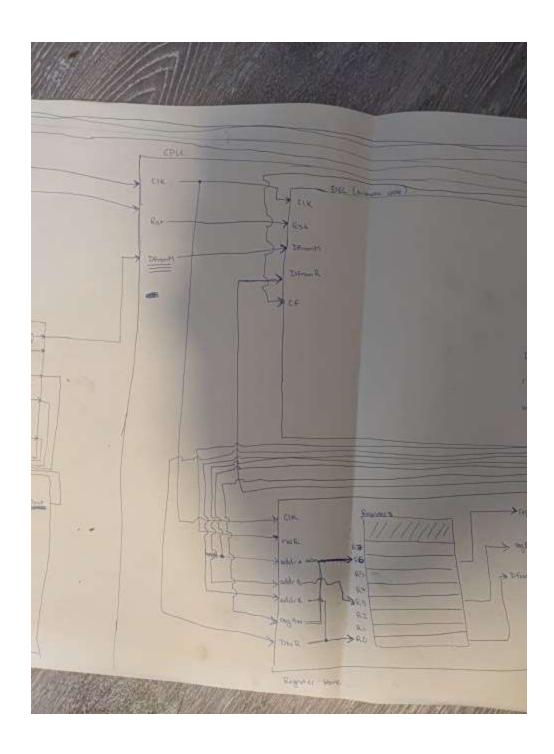
**Project Draft** 

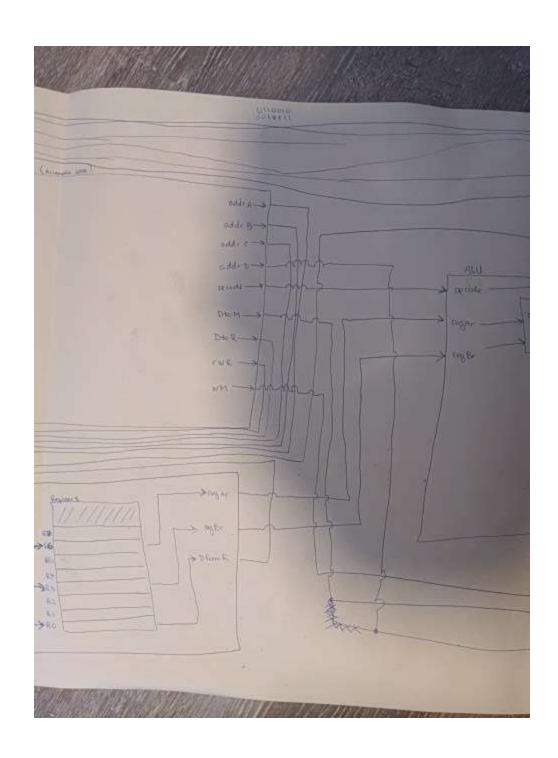
Nov. 21 2020

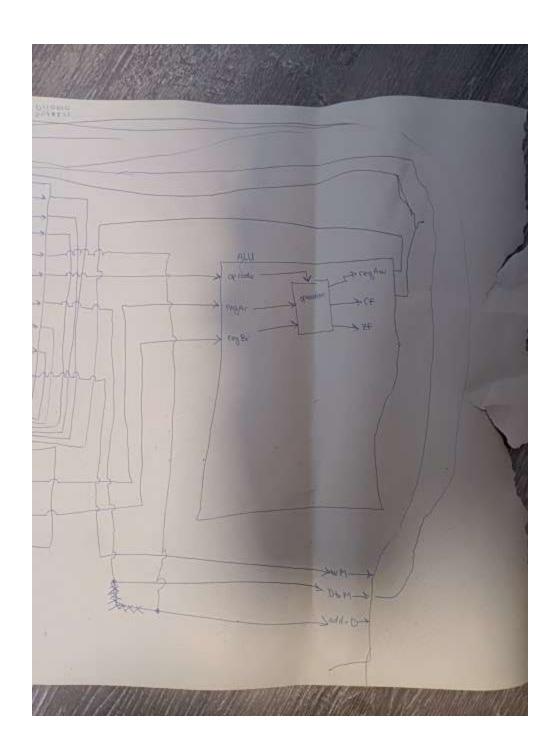
The following image(s) is a draft block diagram of the 16-bit microcomputer architecture:











The following Verilog code is the initial draft of a 16-bit microcomputer. The implementation is not complete as the code does not perform as expected and some debugging is still required.

```
`define reg ADD 1
`define reg_SUB 2
`define reg_AND 3
`define reg OR 4
`define reg_XOR 5
`define addr_ADD 6
`define addr_SUB 7
`define addr_AND 8
`define addr_OR 9
`define addr XOR 10
`define JZ 11
`define LOAD 12
`define STORE 13
module ALU (
    input [3:0] opcode,
    input [15:0] regAr, regBr, op2,
    output reg [15:0] regAw,
    output reg CF, ZF
);
    always @(opcode, regAr, regBr, op2)
    begin
        case (opcode)
             reg_ADD: {CF, regAw} = regAr + regBr;
             `reg_SUB: {CF, regAw} = regAr - regBr;
             `reg_AND: {CF, regAw} = regAr & regBr;
             `reg_OR: {CF, regAw} = regAr | regBr;
             `reg_XOR: {CF, regAw} = regAr ^ regBr;
             `addr_ADD: {CF, regAw} = regAr + op2;
`addr_SUB: {CF, regAw} = regAr - op2;
`addr_AND: {CF, regAw} = regAr & op2;
             `addr_OR: {CF, regAw} = regAr | op2;
             `addr_XOR: {CF, regAw} = regAr ^ op2;
        endcase
        ZF \le (regAw == 16'b0) ? 1 : 0;
    end
endmodule
module REGS (
    input clk, rwR,
    input [3:0] addrA, addrB, addrC,
    input [15:0] regAw, DtoR,
    output [15:0] regAr, regBr, DfromR
);
    reg [15:0] RegFile [7:0]; //8 16 bit registers
    assign regAr = RegFile[addrA];
    assign regBr = RegFile[addrB];
    assign DfromR = RegFile[addrC];
    always @(posedge clk)
    begin
        if (rwR) begin
```

```
RegFile[addrA]=regAw;
            RegFile[addrC]=DtoR;
        end
    end
endmodule
module EXEC (
    input clk, R, CF,
    input [15:0] DfromM, DfromR,
    output reg [15:0] addrD, DtoM, DtoR,
    output reg [15:0] op2,
    output reg [3:0] addrA, addrB, addrC, opcode,
    output reg rwR, wM
);
    localparam fetch = 0;
    localparam decode = 1;
    localparam execute = 2;
    localparam increment_PC = 3;
    localparam next = 4;
    reg [15:0] IR, PC;
    reg [2:0] S;
    reg rwRM;
    always @(posedge clk)
    begin
        if(R) begin
            S = fetch;
            rwR = 0;
            wM = 0;
            opcode = 4'b0;
            addrD = 16'b0;
            PC = 16'b0;
        end else begin
            case (S)
                fetch:
                begin
                    IR = DfromM;
                    rwR = 0;
                    wM = 0;
                    S = decode;
                    opcode = 4'b0;
                end
                decode:
                begin
                    S = execute;
                    case (IR[15:12])
                         `reg_ADD, //fallthrough
                        `reg_SUB, //fallthrough
                        `reg_AND, //fallthrough
                        `reg_OR, //fallthrough
                        `reg_XOR:
                        begin
                            addrA = IR[11:8];
                             addrB = IR[7:4];
                            rwR = 0;
                            wM = 0;
                        end
                         addr_ADD, //fallthrough
                        `addr_SUB, //fallthrough
                         `addr_AND, //fallthrough
                        `addr_OR, //fallthrough
```

```
`addr_XOR:
        begin
            addrA = IR[11:8];
            if(IR[7:0] == 8'b0) begin
                //immediate value will follow
                addrD = PC+1; //get the next line for the immediate
            end else begin
                addrD = \{8'b0, IR[7:0]\};
            end
            rwR = 0;
            wM = 0;
        end
        `JZ:
        begin
            addrC = IR[11:8];
            rwR = 0;
            wM = 0;
        end
        `LOAD, //fallthrough
        `STORE:
        begin
            addrC = IR[11:8];
            addrD = \{8'b0, IR[7:0]\};
            rwR = 0;
            wM = 0;
        end
    endcase
end
execute:
begin
   S = increment_PC;
    case(IR[15:12])
         reg_ADD, //fallthrough
        `reg_SUB, //fallthrough
        `reg_AND, //fallthrough
        `reg_OR, //fallthrough
        `reg_XOR:
        begin
            op2 = 0;
            rwR = 0;
            wM = 0;
        end
         {\tt addr\_ADD,\ //fallthrough}
        `addr_SUB, //fallthrough
         addr_AND, //fallthrough
         addr_OR, //fallthrough
         `addr_XOR:
        begin
            op2 = DfromM;
            rwR = 0;
            wM = 0;
        end
        `JZ:
        begin
            if(DfromR == 16'b0) begin
                PC = PC + IR[7:0];
            end
        end
        `LOAD:
        begin
            DtoR = DfromM;
            rwR = 1;
            wM = 0;
        end
```

```
begin
                                  DtoM = DfromR;
                                  rwR = 0;
                                  wM = 1;
                             end
                        endcase
                   end
                   increment_PC:
                   begin
                        S = next;
                        opcode = IR[15:12];
                        PC = PC + 1;
                        case (IR[15:12])
                             reg_ADD, //fallthrough
reg_SUB, //fallthrough
reg_AND, //fallthrough
reg_OR, //fallthrough
reg_XOR, //fallthrough
                             `addr_ADD, //fallthrough
                             `addr_SUB, //fallthrough
                             `addr_AND, //fallthrough
                             `addr_OR, //fallthrough
                             `addr_XOR:
                             begin
                                  rwR=1;
                                  wM=0;
                             end
                             `LOAD:
                             begin
                                  rwR=0;
                                  wM=0;
                             end
                             `STORE:
                             begin
                                  rwR=0;
                                  wM=1;
                             end
                             `JZ:
                             begin
                                  rwR=0;
                                  wM=0;
                             end
                        endcase
                   end
                   next:
                   begin
                        S = fetch;
                        addrD = PC;
                        wM = 0;
                        rwR = 0;
                   end
              endcase
         end
    end
endmodule
module CPU (
     input clk, R,
     input [15:0] DfromM,
    output wM,
    output [15:0] DtoM, addrD
);
```

`STORE:

```
wire [15:0] op2;
    wire [3:0] addrA, addrB, addrC, opcode;
   wire [15:0] regAr, regBr, regAw, DtoR, DfromR;
    wire rwR, CF, ZF;
    EXEC ex (
                .clk(clk),
                .R(R),
                .opcode(opcode),
                .CF(CF),
                .addrD(addrD),
                .DfromM(DfromM),
                .DtoM(DtoM),
                .op2(op2),
                .addrA(addrA),
                .addrB(addrB),
                .addrC(addrC),
                .DtoR(DtoR),
                .DfromR(DfromR),
                .rwR(rwR),
                .wM(wM)
            );
    ALU alu1 (
                .opcode(opcode),
                .regAr(regAr),
                .regBr(regBr),
                .op2(op2),
                .regAw(regAw),
                .CF(CF),
                .ZF(ZF)
            );
    REGS rg (
                .clk(clk),
                .rwR(rwR),
                .addrA(addrA),
                .regAr(regAr),
                .regAw(regAw),
                .addrB(addrB),
                .regBr(regBr),
                .addrC(addrC),
                .DfromR(DfromR),
                .DtoR(DtoR)
            );
endmodule
module MEM (
    clk, rwM, addrM, Din, Dout
    parameter address_space = 16;
    parameter width = 16;
    input wire clk;
    input wire rwM;
    input wire [address_space-1:0] addrM;
    input wire [width-1:0] Din;
    output wire [width-1:0] Dout;
    reg [width-1:0] mem [(2**address_space)-1:0];
    assign Dout = mem[addrM];
   always @(posedge clk)
```

```
begin
        if (rwM) begin
           mem[addrM]=Din;
        end
    end
endmodule
module BUS (
    input io, wM, Mw,
    input [15:0] DtoM, addrD, Dout, DI, addr,
    output reg [15:0] DfromM, Din, addrM, DO,
    output reg rwM
);
    always @(io or DtoM or addrD or Dout or DI or addr or wM or Mw)
    begin
        if (io) begin
            DO = Dout;
            Din = DI;
            addrM = addr;
            rwM = Mw;
        end else begin
            DfromM = Dout;
            Din = DtoM;
            addrM = addrD;
            rwM = wM;
        end
    end
endmodule
module comp001 (
    input wire clk, R, Mw,
    input io,
    input wire [15:0] addr, DI,
    output wire [15:0] DO
);
    wire wM, rwM;
    wire [15:0] DfromM, DtoM, addrD, Din, Dout, addrM;
    CPU cpu001 (
                .clk(clk),
                .R(R),
                .DfromM(DfromM),
                .addrD(addrD),
                .wM(wM),
                .DtoM(DtoM)
            );
    MEM mem001 (
                .clk(clk),
                .Din(Din),
                .Dout(Dout),
                .addrM(addrM),
                .rwM(rwM)
            );
    BUS bus001 (
                 .io(io),
                .DfromM(DfromM),
                .DtoM(DtoM),
                .addrD(addrD),
                .Din(Din),
                .Dout(Dout),
```

```
.addrM(addrM),
.D0(D0),
.DI(DI),
.addr(addr),
.wM(wM),
.Mw(Mw),
.rwM(rwM)
);
Endmodule
```

The following Verilog code is the initial draft of the test bench required to simulate the 16-bit microcomputer:

```
module comp001_comptest_v_tf();
    integer i;
    parameter prog_start = 300;
    // Inputs
    reg clk;
    reg R;
    reg io;
    reg Mw;
    reg [15:0] addr;
    reg [15:0] DI;
    // Outputs
    wire [15:0] DO;
    // Bidirs
    // Instantiate the UUT
    comp001 uut (
                 .clk(clk),
                .R(R),
                .io(io),
                .Mw(Mw),
                .addr(addr),
                .DI(DI),
                .DO(D0)
    );
    initial begin
        $monitor ("time=%t, clk=%b, R=%b, io=%b, Mw=%b, addr=%b, DI=%b, D0=%b", $realtime, clk,
R, io, Mw, addr, DI, DO);
    end
    initial begin
        clk = 0;
        R = 0;
        io = 0;
        Mw = 0;
        addr = 16'b0;
        DI = 16'b0;
    end
    always
        #20 clk = \simclk;
    initial begin
```

```
R = 1; // Reset high
io = 1; // Store our program in memory
addr = prog_start; // start at the beginning of program memory
#40; //full clock cycle
Mw = 1;
//***********************************//
// Set all registers to 0
                                        //
DI = 16'b0;
addr = 20;
#40; //full clock cycle
addr = prog_start;
DI = 16'b1100000000010100; // LOAD r1, 00010100 -- r0 = 0
#40; //full clock cycle
addr = addr + 1:
DI = 16'b1100000100010100; // LOAD r1, 00010100 -- r1 = 0
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1100001000010100; // LOAD r2, 00010100 -- r2 = 0
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1100001100010100; // LOAD r3, 00010100 -- r3 = 0
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1100010000010100; // LOAD r4, 00010100 -- r4 = 0
#40; //full clock cycle
addr = addr + 1;
DI = 16'b11000101000101000; // LOAD r5, 00010100 -- r5 = 0
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1100011000010100; // LOAD r6, 00010100 -- r6 = 0
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1100011100010100; // LOAD r7, 00010100 -- r7 = 0
//start program
//
//***********************************//
//
      Test immediate values
//
           Populate registers
//
                                         //
//
                                         //
//
           Store result of each
                                         //
           operation in memory for
//
                                         //
          verifying result
DI = 16'b01100001000000000; // ADD r1, 30
#40; //full clock cycle
addr = addr + 1;
DI = 30; // imm16
```

```
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000100110010; // STORE r1, 00110010
#40; //full clock cycle
addr = addr + 1;
DI = 16'b01100010000000000; // ADD r2, 50
#40; //full clock cycle
addr = addr + 1;
DI = 20; // imm16
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101001000110011; // STORE r2, 00110011
#40; //full clock cycle
addr = addr + 1;
DI = 16'b01100011000000000; // ADD r3, 1
#40; //full clock cycle
addr = addr + 1;
DI = 1; // imm16
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101001100110100; // STORE r3, 00110100
#40; //full clock cycle
addr = addr + 1;
DI = 16'b01100100000000000; // ADD r4, 25
#40; //full clock cycle
addr = addr + 1;
DI = 25; // imm16
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101010000110101; // STORE r4, 00110101
#40; //full clock cycle
addr = addr + 1;
DI = 16'b01110001000000000; // SUB r1, 16 -- r1 now should equal 14
#40; //full clock cycle
addr = addr + 1;
DI = 16; // imm16
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000100110111; // STORE r1, 00110111
#40; //full clock cycle
addr = addr + 1;
DI = 16'b10000010000000000; // AND r2, 30 -- r2 now should equal 18
#40; //full clock cycle
addr = addr + 1;
DI = 30; // imm16
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101001000111000; // STORE r2, 00111000
#40; //full clock cycle
addr = addr + 1;
DI = 16'b10010001000000000; // OR r3, 30 -- r3 should now be 31
#40; //full clock cycle
```

```
addr = addr + 1;
DI = 30; // imm16
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101001100111001; // STORE r3, 00111001
#40; //full clock cycle
addr = addr + 1;
DI = 16'b10100001000000000; // XOR r4, imm16 --r4 should now be 6
#40; //full clock cycle
addr = addr + 1;
DI = 31; // imm16
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101010000111010; // STORE r4, 00111010
#40; //full clock cycle
addr = addr + 1;
//***********************************//
           Test register values
//
//
                                             //
             Store result of each
//
                                             //
            operation in memory for
//
                                             //
              verifying result
//
                                             //
DI = 16'b000100010010ZZZZ; // ADD r1, r2 -- r1 should now be 32
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000100111011; // STORE r1, 00111011
#40; //full clock cycle
addr = addr + 1;
DI = 16'b001000010010ZZZZ; // SUB r1, r3 -- r1 should now be 1
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000100111100; // STORE r1, 00111100
#40; //full clock cycle
addr = addr + 1;
DI = 16'b001100010010ZZZZ; // AND r2, r4 -- r2 should now be 2
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101001000111101; // STORE r2, 00111101
#40; //full clock cycle
addr = addr + 1;
DI = 16'b010000010010ZZZZ; // OR r3, r1 -- r3 remains at 31
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101001100111110; // STORE r3, 00111110
#40; //full clock cycle
addr = addr + 1;
DI = 16'b010100010010ZZZZ; // XOR r4, r2 -- r4 should now be 27
#40; //full clock cycle
```

```
addr = addr + 1;
DI = 16'b11010100001111111; // STORE r4, 00111111
// Test LOAD and STORE
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101010101000000; // STORE r5, 01000000 (to see the before value)
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000101000001; // STORE r1, 01000001
                                              -- store r1 in memory
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1100010101000001; // LOAD r5, 01000001
                                              -- load it back, into r5
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101010101000010; // STORE r5, 01000010
                                              -- verify result
//************************************//
          Test opcode with addr8
#40; //full clock cycle
addr = addr + 1;
DI = 16'b0110000100110010; // ADD r1, [00111100]
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000101000011; // STORE r1, 01000011
#40; //full clock cycle
addr = addr + 1;
DI = 16'b0111000100110011; // SUB r1, [00111101]
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000101000100; // STORE r1, 01000100
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1000000100110100; // AND r1, [00111110]
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000101000101; // STORE r1, 01000101
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1001000100110101; // OR r1, [00111111]
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1101000101000110; // STORE r1, 01000110
#40; //full clock cycle
addr = addr + 1;
DI = 16'b1010000100110111; // XOR r1, [00111011]
#40; //full clock cycle
addr = addr + 1;
```

```
DI = 16'b1101000101000110; // STORE r1, 01000111
        #40; //full clock cycle
        addr = addr + 1;
        DI = 16'b1011000111110001; // JZ r1, address
                                                             Jump back 15 instructions
        /* Wait for last 15 instructions to repeat */
        for (i=0; i<15; i=i+1) begin
            #40;
        end
        Mw = 0;
        io = 0;
        R = 1;
        #40;
        R = 0;
        /* Wait for instructions to be executed by computer */
        for (i=0; i<60; i=i+1) begin
            #40;
        end
        io = 1;
        addr = prog_start;
        /* Read program from memory */
        for (i=0; i<60; i=i+1) begin
            #40 addr = addr + 1;
        end
        addr = 20;
        /* Read results of operations */
        for (i=0; i<30; i=i+1) begin
            #40 addr = addr + 1;
        end
        $finish;
        $stop;
    end
endmodule
```

The following is the current output from the simulated 16-bit microcomputer:

```
time=
      time=
      time=
     time=
     time=
time=
     100000, clk=1, R=1, io=1, Mw=1, addr=0000000100101100, DI=1100000000010100, D0=1100000000010100
     time=
     140000, clk=1, R=1, io=1, Mw=1, addr=0000000100101101, DI=1100000100010100, D0=1100000100010100
time=
time=
     180000, clk=1, R=1, io=1, Mw=1, addr=0000000100101110, DI=1100001000010100, D0=1100001000010100
time=
     time=
time=
time=
     260000, clk=1, R=1, io=1, Mw=1, addr=0000000100110000, DI=1100010000010100, D0=1100010000010100
time=
     time=
time=
     300000, clk=1, R=1, io=1, Mw=1, addr=0000000100110001, DI=1100010100010100, D0=1100010100010100
     time=
     340000, clk=1, R=1, io=1, Mw=1, addr=0000000100110010, DI=1100011000010100, D0=1100011000010100
time=
     time=
     380000, clk=1, R=1, io=1, Mw=1, addr=0000000100110011, DI=0110000100000000, D0=01100001000000000
time=
time=
     time=
     time=
     460000, clk=1, R=1, io=1, Mw=1, addr=0000000100110101, DI=1101000100110010, D0=1101000100110010
time=
     time=
     500000, clk=1, R=1, io=1, Mw=1, addr=0000000100110110, DI=0110001000000000, D0=01100010000000000
time=
time=
     time=
     540000, clk=1, R=1, io=1, Mw=1, addr=0000000100110111, DI=000000000010100, D0=0000000000010100
     time=
     580000, clk=1, R=1, io=1, Mw=1, addr=0000000100111000, DI=1101001000110011, D0=1101001000110011
time=
     time=
time=
     time=
     660000, clk=1, R=1, io=1, Mw=1, addr=0000000100111010, DI=00000000000001, D0=000000000000001
time=
     time=
     700000, clk=1, R=1, to=1, Mw=1, addr=0000000100111011, DI=1101001100110100, D0=1101001100110100
time=
time=
     740000, clk=1, R=1, io=1, Mw=1, addr=0000000100111100, DI=0110010000000000, D0=0110010000000000
time=
     time=
     780000, clk=1, R=1, io=1, Mw=1, addr=0000000100111101, DI=000000000011001, D0=000000000011001
time=
     time=
     820000, clk=1, R=1, io=1, Mw=1, addr=0000000100111110, DI=1101010000110101, D0=1101010000110101
time=
time=
     time=
time=
     900000, clk=1, R=1, io=1, Mw=1, addr=0000000101000000, DI=000000000010000, D0=000000000010000
time=
     time=
     940000, clk=1, R=1, io=1, Mw=1, addr=0000000101000001, DI=1101000100110111, D0=1101000100110111
time=
     time=
     980000, clk=1, R=1, io=1, Mw=1, addr=0000000101000010, DI=1000001000000000, D0=10000010000000000
time=
    time=
    1020000, clk=1, R=1, io=1, Mw=1, addr=0000000101000011, DI=0000000000011110, D0=000000000011110
time=
    time=
time=
    time=
    1100000, clk=1, R=1, io=1, Mw=1, addr=0000000101000101, DI=100100010000000, D0=1001000100000000
time=
    time=
time=
    1140000, clk=1, R=1, io=1, Mw=1, addr=0000000101000110, DI=0000000000011110, D0=000000000011110
time=
    time=
    1180000, clk=1, R=1, io=1, Mw=1, addr=0000000101000111, DI=1101001100111001, D0=1101001100111001
    time=
```

```
1220000, clk=1, R=1, io=1, Mw=1, addr=0000000101001000, DI=101000010000000, D0=1010000100000000
time=
time=
       1260000, clk=1, R=1, io=1, Mw=1, addr=0000000101001001, DI=000000000011111, D0=000000000011111
time=
       time=
       1300000, clk=1, R=1, io=1, Mw=1, addr=0000000101001010, DI=1101010000111010, D0=11010101000111010
time=
time=
       1340000, clk=1, R=1, io=1, Mw=1, addr=0000000101001011, DI=000100010010zzzz, D0=000100010010zzzz
time=
       time=
time=
       1380000, clk=1, R=1, io=1, Mw=1, addr=0000000101001100, DI=1101000100111011, D0=1101000100111011
       time=
       1420000, clk=1, R=1, io=1, Mw=1, addr=0000000101001101, DI=001000010010zzzz, D0=001000010010zzzz
time=
time=
       1460000, clk=1, R=1, io=1, Mw=1, addr=0000000101001110, DI=1101000100111100, D0=1101000100111100
time=
       time=
       time=
time=
       1540000, clk=1, R=1, io=1, Mw=1, addr=0000000101010000, DI=1101001000111101, D0=1101001000111101
time=
       1560000, clk=0, R=1, io=1, Mw=1, addr=0000000101010001, DI=010000010010zzzz, D0=xxxxxxxxxxxxxxxxxxx
time=
       1580000, clk=1, R=1, io=1, Mw=1, addr=0000000101010001, DI=010000010010zzzz, D0=010000010010zzzz
time=
       time=
       1620000, clk=1, R=1, io=1, Mw=1, addr=0000000101010010, DI=1101001100111110, D0=1101001100111110
time=
time=
       1660000, clk=1, R=1, io=1, Mw=1, addr=0000000101010011, DI=010100010010zzzz, D0=010100010010zzzz
time=
       time=
       time=
time=
time=
       time=
       1780000, clk=1, R=1, io=1, Mw=1, addr=00000001010101010, DI=1101000101000001, D0=1101000101000001
time=
       time=
       1820000, clk=1, R=1, io=1, Mw=1, addr=0000000101010111, DI=1100010101000001, D0=1100010101000001
time=
       time=
       1860000, clk=1, R=1, io=1, Mw=1, addr=0000000101011000, DI=11010101000010, D0=1101010101000010
time=
       time=
       1900000, \ \text{clk=1}, \ \text{R=1}, \ \text{io=1}, \ \text{Mw=1}, \ \text{addr=000000001011001}, \ \text{DI=0110000100110010}, \ \text{D0=0110000100110010}
time=
       time=
time=
       1940000, \ \text{clk=1}, \ \text{R=1}, \ \text{io=1}, \ \text{Mw=1}, \ \text{addr=000000010101010}, \ \text{DI=1101000101000011}, \ \text{D0=1101000101000011}
       time=
       1980000, clk=1, R=1, io=1, Mw=1, addr=00000001010111, DI=0111000100110011, D0=0111000100110011
time=
       time=
time=
       2020000, clk=1, R=1, io=1, Mw=1, addr=0000000101011100, DI=1101000101000100, D0=1101000101000100
       time=
       2060000, clk=1, R=1, io=1, Mw=1, addr=0000000101011101, DI=1000000100110100, D0=1000000100110100
time=
       time=
       2100000, clk=1, R=1, io=1, Mw=1, addr=0000000101011110, DI=1101000101000101, D0=1101000101000101
time=
time=
       time=
time=
       2180000, clk=1, R=1, io=1, Mw=1, addr=0000000101100000, DI=1101000101000110, D0=1101000101000110
time=
       time=
       2220000, clk=1, R=1, io=1, Mw=1, addr=0000000101100001, DI=1010000100110111, D0=1010000100110111
time=
       time=
time=
       2260000, clk=1, R=1, io=1, Mw=1, addr=0000000101100010, DI=1101000101000110, D0=1101000101000110
       time=
       2300000, \ \text{clk=1}, \ \text{R=1}, \ \text{io=1}, \ \text{Mw=1}, \ \text{addr=00000000101100011}, \ \text{DI=1011000111110001}, \ \text{D0=1011000111110001}
time=
       2320000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
       2340000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 2360000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 2380000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
time=
       2400000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
       2420000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
       2440000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
       2460000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
       2480000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
```

```
2500000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                2520000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                2540000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2560000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2580000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2600000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 2620000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                2640000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                2660000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                2680000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2700000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                2720000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                2740000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2760000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2780000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 2800000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                2820000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2840000, clk=0, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2860000, clk=1, R=1, io=1, Mw=1, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2880000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2900000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                2920000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                2940000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                2960000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                2980000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                time=
time=
                3040000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3060000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3080000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                3100000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                3120000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3140000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3160000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3180000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=1011000111110001, \ D0=1011000111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=1011000111110001, \ D0=1011000111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ D1=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ D1=10110001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ D1=101100001111110001, \ D0=10110001111110001 \\ 3200000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ D1=101100001111110001, \ D1=10110001111110001, \ D1=1011000111111110001, \ D1=10110001111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=10110001111110001, \ D1=101100011111110001, \ D1=10110001111110001, \ D1=10110001111110001, \ D1=10110001111110001, \ D1=10110001111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=101100011111110001, \ D1=10110001111111000
time=
time=
                3220000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 3240000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                3260000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3280000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                3300000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                3320000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3340000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3360000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3380000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3400000, \ \text{clk=0}, \ \text{R=0}, \ \text{io=0}, \ \text{Mw=0}, \ \text{addr=00000000101100011}, \ \text{DI=1011000111110001}, \ \text{D0=1011000111110001}
time=
                3420000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 3440000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                3460000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3480000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3500000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3520000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                3540000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                3560000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3580000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=1011000111110001, \ D0=1011000111110001 \\ 3600000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=1011000111110001, \ D0=1011000111110001
time=
time=
               3620000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 3640000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 3660000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
time=
                3680000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3700000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
                3720000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
                3740000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
                3760000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
```

```
3780000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
               3800000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
               3820000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               3840000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               3860000, \ \text{clk=1}, \ \text{R=0}, \ \text{io=0}, \ \text{Mw=0}, \ \text{addr=0000000101100011}, \ \text{DI=1011000111110001}, \ \text{D0=1011000111110001}
time=
              3880000, \ clk=0, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=1011000111110001, \ D0=1011000111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=1011000111110001, \ D0=1011000111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=1011000111110001, \ D0=1011000111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ DI=10110001111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ DI=1011000111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ DI=1011000111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ D1=1011000111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ D1=1011000111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=00000000101100011, \ D1=10110001111110001, \ D0=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000011100011, \ D1=10110001111110001, \ D1=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=000000001100011, \ D1=101100001111110001, \ D1=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=000000001100011, \ D1=10110001111110001, \ D1=10110001111110001 \\ 3900000, \ clk=1, \ R=0, \ io=0, \ Mw=0, \ addr=0000000001100011, \ D1=101100001111110001, \ D1=10110001111110001 \\ 3900000, \ clk=1, \ Mw=0, \ addr=0000000001100011, \ D1=10110001111110001, \ D1=10110001111110001 \\ 3900000, \ clk=1, \ Mw=0, \ addr=0000000001100011, \ D1=10110001111110001, \ D1=10110001111110001 \\ 3900000, \ clk=1, \ Mw=0, \ addr=0000000001100001100011111100001 \\ 3900000, \ clk=1, \ Mw=0, \ addr=00000000011000111111000
time=
time=
               3920000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               3940000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               3960000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               3980000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
               4000000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
               4020000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4040000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
              time=
time=
               4100000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4120000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4140000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4160000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4180000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
               4200000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
               4220000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4240000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
               4260000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
              4280000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001 4300000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
               4320000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4340000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4360000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
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               4400000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
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time=
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time=
              time=
time=
              time=
time=
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time=
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time=
time=
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               4600000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
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time=
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time=
               4660000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4680000, \ \text{clk=0}, \ \text{R=0}, \ \text{io=0}, \ \text{Mw=0}, \ \text{addr=00000000101100011}, \ \text{DI=1011000111110001}, \ \text{D0=1011000111110001}
time=
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time=
time=
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time=
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time=
               4780000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
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time=
time=
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               4840000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
              4860000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
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time=
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time=
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time=
time=
               4960000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               4980000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
               5000000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
               5020000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
               5040000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
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5060000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
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time=
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           5100000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
           5120000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
           5140000, \ \text{clk=1}, \ \text{R=0}, \ \text{io=0}, \ \text{Mw=0}, \ \text{addr=00000000101100011}, \ \text{DI=1011000111110001}, \ \text{D0=1011000111110001}
time=
time=
           5160000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
           5180000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
           5200000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
           5220000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
           5240000, clk=0, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
           5260000, clk=1, R=0, io=0, Mw=0, addr=0000000101100011, DI=1011000111110001, D0=1011000111110001
time=
time=
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           5300000, clk=1, R=0, io=1, Mw=0, addr=0000000100101100, DI=1011000111110001, D0=1100000000010100
time=
           5320000, clk=0, R=0, io=1, Mw=0, addr=0000000100101101, DI=1011000111110001, D0=1100000100010100
time=
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time=
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time=
           5400000, clk=0, R=0, io=1, Mw=0, addr=0000000100101111, DI=1011000111110001, D0=1100001100010100
time=
           5420000, clk=1, R=0, io=1, Mw=0, addr=0000000100101111, DI=1011000111110001, D0=1100001100010100
time=
           5440000, clk=0, R=0, io=1, Mw=0, addr=0000000100110000, DI=1011000111110001, D0=1100010000010100
time=
           5460000, clk=1, R=0, io=1, Mw=0, addr=0000000100110000, DI=1011000111110001, D0=1100010000010100
time=
time=
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           5500000, clk=1, R=0, io=1, Mw=0, addr=0000000100110001, DI=1011000111110001, D0=1100010100010100
time=
           5520000, clk=0, R=0, io=1, Mw=0, addr=0000000100110010, DI=1011000111110001, D0=1100011000010100
time=
time=
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          time=
time=
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time=
           5620000, clk=1, R=0, io=1, Mw=0, addr=0000000100110100, DI=1011000111110001, D0=000000000011110
time=
           5640000, clk=0, R=0, io=1, Mw=0, addr=0000000100110101, DI=1011000111110001, D0=1101000110010
time=
           5660000, clk=1, R=0, io=1, Mw=0, addr=0000000100110101, DI=1011000111110001, D0=1101000100110010
time=
           5680000, clk=0, R=0, io=1, Mw=0, addr=0000000100110110, DI=1011000111110001, D0=01100010000000000
time=
           5700000, clk=1, R=0, io=1, Mw=0, addr=0000000100110110, DI=1011000111110001, D0=01100010000000000
time=
           5720000, clk=0, R=0, io=1, Mw=0, addr=0000000100110111, DI=1011000111110001, D0=000000000010100
time=
          5740000, \ clk=1, \ R=0, \ io=1, \ Mw=0, \ addr=0000000100110111, \ DI=1011000111110001, \ D0=0000000000101000 \\ 5760000, \ clk=0, \ R=0, \ io=1, \ Mw=0, \ addr=00000001001110000, \ DI=1011000111110001, \ D0=1101001000110011
time=
time=
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time=
time=
           5820000, clk=1, R=0, io=1, Mw=0, addr=0000000100111001, DI=1011000111110001, D0=0110001100000000
time=
           time=
time=
           5880000, clk=0, R=0, io=1, Mw=0, addr=0000000100111011, DI=1011000111110001, D0=1101001100110100
time=
time=
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           5920000, clk=0, R=0, io=1, Mw=0, addr=0000000100111100, DI=1011000111110001, D0=0110010000000000
time=
           5940000, clk=1, R=0, io=1, Mw=0, addr=0000000100111100, DI=1011000111110001, D0=0110010000000000
time=
time=
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          5980000, clk=1, R=0, io=1, Mw=0, addr=0000000100111101, DI=1011000111110001, D0=000000000011001 6000000, clk=0, R=0, io=1, Mw=0, addr=0000000100111110, DI=1011000111110001, D0=1101010101010101
time=
time=
           6020000, clk=1, R=0, io=1, Mw=0, addr=0000000100111110, DI=1011000111110001, D0=1101010000110101
time=
           6040000, clk=0, R=0, io=1, Mw=0, addr=0000000100111111, DI=1011000111110001, D0=0111000100000000
time=
           6060000, clk=1, R=0, io=1, Mw=0, addr=0000000100111111, DI=1011000111110001, D0=0111000100000000
time=
           6080000, clk=0, R=0, io=1, Mw=0, addr=0000000101000000, DI=1011000111110001, D0=000000000010000
time=
time=
           6100000, clk=1, R=0, io=1, Mw=0, addr=0000000101000000, DI=1011000111110001, D0=000000000010000
           6120000, clk=0, R=0, io=1, Mw=0, addr=0000000101000001, DI=1011000111110001, D0=1101000110111
time=
          time=
time=
           time=
          6200000, \ clk=0, \ R=0, \ io=1, \ Mw=0, \ addr=0000000101000011, \ DI=1011000111110001, \ D0=0000000000111106220000, \ clk=1, \ R=0, \ io=1, \ Mw=0, \ addr=0000000101000011, \ DI=1011000111110001, \ D0=00000000000011110
time=
time=
           6240000, clk=0, R=0, io=1, Mw=0, addr=0000000101000100, DI=1011000111110001, D0=110100010101000
time=
           6260000, clk=1, R=0, io=1, Mw=0, addr=0000000101000100, DI=1011000111110001, D0=11010001000111000
time=
           6280000, clk=0, R=0, io=1, Mw=0, addr=0000000101000101, DI=1011000111110001, D0=1001000100000000
time=
           6300000, clk=1, R=0, io=1, Mw=0, addr=0000000101000101, DI=1011000111110001, D0=1001000100000000
time=
           6320000, clk=0, R=0, io=1, Mw=0, addr=0000000101000110, DI=1011000111110001, D0=000000000011110
time=
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6340000, clk=1, R=0, io=1, Mw=0, addr=0000000101000110, DI=1011000111110001, D0=000000000011110
time=
time=
         6360000, clk=0, R=0, io=1, Mw=0, addr=0000000101000111, DI=1011000111110001, D0=1101001100111001
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time=
         6400000, clk=0, R=0, io=1, Mw=0, addr=0000000101001000, DI=1011000111110001, D0=1010000100000000
time=
         time=
time=
         6440000, clk=0, R=0, io=1, Mw=0, addr=0000000101001001, DI=1011000111110001, D0=000000000011111
         6460000, clk=1, R=0, io=1, Mw=0, addr=0000000101001001, DI=1011000111110001, D0=000000000011111
time=
         6480000, clk=0, R=0, io=1, Mw=0, addr=0000000101001010, DI=1011000111110001, D0=1101010000111010
time=
         6500000, clk=1, R=0, io=1, Mw=0, addr=0000000101001010, DI=1011000111110001, D0=11010101010101010
time=
         6520000, clk=0, R=0, io=1, Mw=0, addr=0000000101001011, DI=1011000111110001, D0=000100010010zzzz
time=
         6540000, clk=1, R=0, io=1, Mw=0, addr=0000000101001011, DI=1011000111110001, D0=000100010010zzzz
time=
         6560000, clk=0, R=0, io=1, Mw=0, addr=0000000101001100, DI=1011000111110001, D0=110100011011
time=
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time=
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time=
         time=
time=
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time=
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time=
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time=
         6720000, clk=0, R=0, io=1, Mw=0, addr=0000000101010000, DI=1011000111110001, D0=1101000100111101
time=
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time=
time=
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         6780000, clk=1, R=0, io=1, Mw=0, addr=0000000101010001, DI=1011000111110001, D0=010000010010zzzz
time=
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time=
time=
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         6840000, \ \text{clk=0}, \ \text{R=0}, \ \text{io=1}, \ \text{Mw=0}, \ \text{addr=0000000101010011}, \ \text{DI=1011000111110001}, \ \text{D0=0101000100102zzz}
time=
         6860000, clk=1, R=0, io=1, Mw=0, addr=0000000101010011, DI=1011000111110001, D0=010100010010zzzz
time=
         6880000, clk=0, R=0, io=1, Mw=0, addr=0000000101010100, DI=1011000111110001, D0=1101010000111111
time=
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time=
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time=
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time=
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time=
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time=
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time=
         time=
time=
         time=
time=
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time=
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time=
time=
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         7160000, clk=0, R=0, io=1, Mw=0, addr=0000000101011011, DI=1011000111110001, D0=0111000110011
time=
         7180000, clk=1, R=0, io=1, Mw=0, addr=0000000101011011, DI=1011000111110001, D0=0111000110011
time=
         7200000, clk=0, R=0, io=1, Mw=0, addr=0000000101011100, DI=1011000111110001, D0=1101000101000100
time=
         7220000, clk=1, R=0, io=1, Mw=0, addr=0000000101011100, DI=1011000111110001, D0=1101000101000100
time=
time=
         7240000, clk=0, R=0, io=1, Mw=0, addr=0000000101011101, DI=1011000111110001, D0=1000000100110100
         7260000, \ clk=1, \ R=0, \ io=1, \ Mw=0, \ addr=0000000101011101, \ DI=1011000111110001, \ D0=100000010011010007280000, \ clk=0, \ R=0, \ io=1, \ Mw=0, \ addr=0000000101011110, \ DI=1011000111110001, \ D0=11010000101000101
time=
time=
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time=
         7320000, clk=0, R=0, io=1, Mw=0, addr=0000000101011111, DI=1011000111110001, D0=1001000100110101
time=
         7340000, clk=1, R=0, io=1, Mw=0, addr=0000000101011111, DI=1011000111110001, D0=1001000100110101
time=
         7360000, clk=0, R=0, io=1, Mw=0, addr=0000000101100000, DI=1011000111110001, D0=1101000101000110
time=
time=
         7380000, clk=1, R=0, io=1, Mw=0, addr=0000000101100000, DI=1011000111110001, D0=1101000101000110
         7400000, clk=0, R=0, io=1, Mw=0, addr=0000000101100001, DI=1011000111110001, D0=1010000100110111
time=
         7420000, clk=1, R=0, io=1, Mw=0, addr=0000000101100001, DI=1011000111110001, D0=1010000100110111
time=
time=
         7440000, clk=0, R=0, io=1, Mw=0, addr=0000000101100010, DI=1011000111110001, D0=1101000101000110
         time=
         time=
time=
         time=
         time=
time=
         time=
         time=
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time=
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