4.4 Pin muxing

Table 12 defines the pin list and muxing for this device.

Each entry of *Table 12* shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by ALT0.

Note: Pins labeled "NC" are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

Pins labeled "Reserved" are to be tied to ground. Not doing so may cause unpredictable device behavior.

Table 12. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
Port A												
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	—	M	S	51	73	T14
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0						
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0						
		SIUL	—	—	EIRQ[0]	—						
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	—	M	S	52	74	R14
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0						
		DSPI_2	SOUT	ALT2	—	—						
		SIUL	—	—	EIRQ[1]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S	57	84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						
A[3]	PCR[3]	SIUL	GPIO[3]	ALT0	GPIO[3]	—	Pull down	M	S	64	92	K17
		eTimer_0	ETC[3]	ALT1	ETC[3]	PSMI[38]; PADSEL=0						
		DSPI_2	CS0	ALT2	CS0	PSMI[3]; PADSEL=0						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=0						
		MC_RGM	—	—	ABS[2]	—						
		SIUL	—	—	EIRQ[3]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[4]	PCR[4]	SIUL	GPIO[4]	ALT0	GPIO[4]	—	Pull down	M	S	75	108	C16
		eTimer_1	ETC[0]	ALT1	ETC[0]	PSMI[9]; PADSEL=0						
		DSPI_2	CS1	ALT2	—	—						
		eTimer_0	ETC[4]	ALT3	ETC[4]	PSMI[7]; PADSEL=0						
		MC_RGM	—	—	FAB	—						
		SIUL	—	—	EIRQ[4]	—						
A[5]	PCR[5]	SIUL	GPIO[5]	ALT0	GPIO[5]	—	—	M	S	8	14	H4
		DSPI_1	CS0	ALT1	CS0	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=0						
		DSPI_0	CS7	ALT3	—	—						
		SIUL	—	—	EIRQ[5]	—						
A[6]	PCR[6]	SIUL	GPIO[6]	ALT0	GPIO[6]	—	—	M	S	2	2	G4
		DSPI_1	SCK	ALT1	SCK	—						
		SIUL	—	—	EIRQ[6]	—						
A[7]	PCR[7]	SIUL	GPIO[7]	ALT0	GPIO[7]	—	—	M	S	4	10	F3
		DSPI_1	SOUT	ALT1	—	—						
		SIUL	—	—	EIRQ[7]	—						
A[8]	PCR[8]	SIUL	GPIO[8]	ALT0	GPIO[8]	—	—	M	S	6	12	F4
		DSPI_1	—	—	SIN	—						
		SIUL	—	—	EIRQ[8]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[9]	PCR[9]	SIUL	GPIO[9]	ALT0	GPIO[9]	—	—	M	S	94	134	B6
		DSPI_2	CS1	ALT1	—	—						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=0						
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	—	M	S	81	118	A13
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1						
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0						
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0						
		SIUL	—	—	EIRQ[9]	—						
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	—	M	S	82	120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	—	M	S	83	122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	—	M	S	95	136	C6
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1						
		SIUL	—	—	EIRQ[12]	—						
A[14]	PCR[14]	SIUL	GPIO[14]	ALT0	GPIO[14]	—	—	M	S	99	143	B4
		FlexCAN_1	TXD	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=0						
		SIUL	—	—	EIRQ[13]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
A[15]	PCR[15]	SIUL	GPIO[15]	ALT0	GPIO[15]	—	—	M	S	100	144	D3
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=0						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=0						
		SIUL	—	—	EIRQ[14]	—						
Port B												
B[0]	PCR[16]	SIUL	GPIO[16]	ALT0	GPIO[16]	—	—	M	S	76	109	B15
		FlexCAN_0	TXD	ALT1	—	—						
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=0						
		SSCM	DEBUG[0]	ALT3	—	—						
		SIUL	—	—	EIRQ[15]	—						
B[1]	PCR[17]	SIUL	GPIO[17]	ALT0	GPIO[17]	—	—	M	S	77	110	C14
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=0						
		SSCM	DEBUG[1]	ALT3	—	—						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=1						
		SIUL	—	—	EIRQ[16]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
B[2]	PCR[18]	SIUL	GPIO[18]	ALT0	GPIO[18]	—	—	M	S	79	114	A14
		LINFlexD_0	TXD	ALT1	—	—						
		SSCM	DEBUG[2]	ALT3	—	—						
		SIUL	—	—	EIRQ[17]	—						
B[3]	PCR[19]	SIUL	GPIO[19]	ALT0	GPIO[19]	—	—	M	S	80	116	B13
		SSCM	DEBUG[3]	ALT3	—	—						
		LINFlexD_0	—	—	RXD	PSMI[31]; PADSEL=0						
B[4](2)	PCR[20]	SIUL	GPIO[20]	ALT0	GPIO[20]	—	—	F	S	61	89	L17
		JTAGC	TDO	ALT1	—	—						
B[5]	PCR[21]	SIUL	GPIO[21]	ALT0	GPIO[21]	—	Pull up	M	S	58	86	M15
		JTAGC	—	—	TDI	—						
B[6]	PCR[22]	SIUL	GPIO[22]	ALT0	GPIO[22]	—	—	F	S	96	138	B3
		MC_CGM	clk_out	ALT1	—	—						
		DSPI_2	CS2	ALT2	—	—						
		SIUL	—		EIRQ[18]	—						
B[7]	PCR[23]	SIUL	—	ALT0	GPI[23]	—	—	—	—	30	43	R5
		LINFlexD_0	—	—	RXD	PSMI[31]; PADSEL=1						
		ADC_0	—	—	AN[0](3)	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
B[8]	PCR[24]	SIUL	—	ALT0	GPI[24]	—	—	—	—	31	47	P7
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=2						
		ADC_0	—	—	AN[1](3)	—						
B[9]	PCR[25]	SIUL	—	ALT0	GPI[25]	—	—	—	—	35	52	U7
		ADC_0 ADC_1	—	—	AN[11](3)	—						
B[10]	PCR[26]	SIUL	—	ALT0	GPI[26]	—	—	—	—	36	53	R8
		ADC_0 ADC_1	—	—	AN[12](3)	—						
B[11]	PCR[27]	SIUL	—	ALT0	GPI[27]	—	—	—	—	37	54	T8
		ADC_0 ADC_1	—	—	AN[13](3)	—						
B[12]	PCR[28]	SIUL	—	ALT0	GPI[28]	—	—	—	—	38	55	U8
		ADC_0 ADC_1	—	—	AN[14](3)	—						
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—	43	60	R10
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=0						
		ADC_1	—	—	AN[0](3)	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—	44	64	P11
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2						
		SIUL	—	—	EIRQ[19]	—						
		ADC_1	—	—	AN[1](3)	—						
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—	—	62	R11
		SIUL	—	—	EIRQ[20]	—						
		ADC_1	—	—	AN[2](3)	—						
Port C												
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—	45	66	R12
		ADC_1	—	—	AN[3](3)	—						
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—	—	41	T4
		ADC_0	—	—	AN[2](3)	—						
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—	—	45	U5
		ADC_0	—	—	AN[3](3)	—						
C[4]	PCR[36]	SIUL	GPIO[36]	ALT0	GPIO[36]	—	—	M	S	5	11	H3
		DSPI_0	CS0	ALT1	CS0	—						
		FlexPWM_0	X[1]	ALT2	X[1]	PSMI[28]; PADSEL=0						
		SSCM	DEBUG[4]	ALT3	—	—						
		SIUL	—	—	EIRQ[22]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[5]	PCR[37]	SIUL	GPIO[37]	ALT0	GPIO[37]	—	—	M	S	7	13	G3
		DSPI_0	SCK	ALT1	SCK	—						
		SSCM	DEBUG[5]	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=0						
		SIUL	—	—	EIRQ[23]	—						
C[6]	PCR[38]	SIUL	GPIO[38]	ALT0	GPIO[38]	—	—	M	S	98	142	D4
		DSPI_0	SOUT	ALT1	—	—						
		FlexPWM_0	B[1]	ALT2	B[1]	PSMI[25]; PADSEL=0						
		SSCM	DEBUG[6]	ALT3	—	—						
		SIUL	—	—	EIRQ[24]	—						
C[7]	PCR[39]	SIUL	GPIO[39]	ALT0	GPIO[39]	—	—	M	S	9	15	K4
		FlexPWM_0	A[1]	ALT2	A[1]	PSMI[21]; PADSEL=0						
		SSCM	DEBUG[7]	ALT3	—	—						
		DSPI_0	—	—	SIN	—						
C[10]	PCR[42]	SIUL	GPIO[42]	ALT0	GPIO[42]	—	—	M	S	78	111	A15
		DSPI_2	CS2	ALT1	—	—						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=0						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[11]	PCR[43]	SIUL	GPIO[43]	ALT0	GPIO[43]	—	—	M	S	55	80	M14
		eTimer_0	ETC[4]	ALT1	ETC[4]	PSMI[7]; PADSEL=1						
		DSPI_2	CS2	ALT2	—	—						
C[12]	PCR[44]	SIUL	GPIO[44]	ALT0	GPIO[44]	—	—	M	S	56	82	N15
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=0						
		DSPI_2	CS3	ALT2	—	—						
C[13]	PCR[45]	SIUL	GPIO[45]	ALT0	GPIO[45]	—	—	M	S	71	101	F15
		eTimer_1	ETC[1]	ALT1	ETC[1]	PSMI[10]; PADSEL=0						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=0						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=0						
C[14]	PCR[46]	SIUL	GPIO[46]	ALT0	GPIO[46]	—	—	M	S	72	103	E15
		eTimer_1	ETC[2]	ALT1	ETC[2]	PSMI[11]; PADSEL=1						
		CTU_0	EXT_TGR	ALT2	—	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[15]	PCR[47]	SIUL	GPIO[47]	ALT0	GPIO[47]	—	—	SYM	S	85	124	A8
		FlexRay	CA_TR_EN	ALT1	—	—						
		eTimer_1	ETC[0]	ALT2	ETC[0]	PSMI[9]; PADSEL=1						
		FlexPWM_0	A[1]	ALT3	A[1]	PSMI[21]; PADSEL=1						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=1						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=1						
Port D												
D[0]	PCR[48]	SIUL	GPIO[48]	ALT0	GPIO[48]	—	—	SYM	S	86	125	B8
		FlexRay	CA_TX	ALT1	—	—						
		eTimer_1	ETC[1]	ALT2	ETC[1]	PSMI[10]; PADSEL=1						
		FlexPWM_0	B[1]	ALT3	B[1]	PSMI[25]; PADSEL=1						
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	—	M	S	3	3	E3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexRay	—	—	CA_RX	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	—	M	S	—	140	C5
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0						
		FlexRay	—	—	CB_RX	—						
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	—	SYM	S	89	128	A7
		FlexRay	CB_TX	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2						
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	—	SYM	S	90	129	B7
		FlexRay	CB_TR_EN	ALT1	—	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2						
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	—	M	S	22	33	N3
		DSPI_0	CS3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[6]	PCR[54]	SIUL	GPIO[54]	ALT0	GPIO[54]	—	—	M	S	23	34	P3
		DSPI_0	CS2	ALT1	—	—						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=1						
D[7]	PCR[55]	SIUL	GPIO[55]	ALT0	GPIO[55]	—	—	M	S	26	37	R4
		DSPI_1	CS3	ALT1	—	—						
		DSPI_0	CS4	ALT3	—	—						
		SWG	analog output	—	—	—						
D[8]	PCR[56]	SIUL	GPIO[56]	ALT0	GPIO[56]	—	—	M	S	21	32	M3
		DSPI_1	CS2	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=2						
		DSPI_0	CS5	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=1						
D[9]	PCR[57]	SIUL	GPIO[57]	ALT0	GPIO[57]	—	—	M	S	15	26	L3
		FlexPWM_0	X[0]	ALT1	X[0]	—						
		LINFlexD_1	TXD	ALT2	—	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
D[10]	PCR[58]	SIUL	GPIO[58]	ALT0	GPIO[58]	—	—	M	S	53	76	T15
		FlexPWM_0	A[0]	ALT1	A[0]	PSMI[20]; PADSEL=1						
		eTimer_0	—	—	ETC[0]	PSMI[35]; PADSEL=1						
D[11]	PCR[59]	SIUL	GPIO[59]	ALT0	GPIO[59]	—	—	M	S	54	78	R16
		FlexPWM_0	B[0]	ALT1	B[0]	PSMI[24]; PADSEL=1						
		eTimer_0	—	—	ETC[1]	PSMI[36]; PADSEL=1						
D[12]	PCR[60]	SIUL	GPIO[60]	ALT0	GPIO[60]		—	M	S	70	99	G14
		FlexPWM_0	X[1]	ALT1	X[1]	PSMI[28]; PADSEL=1						
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=1						
D[14]	PCR[62]	SIUL	GPIO[62]	ALT0	GPIO[62]	—	—	M	S	73	105	D16
		FlexPWM_0	B[1]	ALT1	B[1]	PSMI[25]; PADSEL=2						
		eTimer_0	—	—	ETC[3]	PSMI[38]; PADSEL=1						
Port E												
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—	46	68	T13
		ADC_1	—	—	AN[5](3)	—						
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—	32	49	U6
		ADC_0	—	—	AN[5](3)	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
E[4]	PCR[68]	SIUL	—	ALT0	GPI[68]	—	—	—	—	—	42	U4
		ADC_0	—	—	AN[7](3)	—						
E[5]	PCR[69]	SIUL	—	ALT0	GPI[69]	—	—	—	—	—	44	T5
		ADC_0	—	—	AN[8](3)	—						
E[6]	PCR[70]	SIUL	—	ALT0	GPI[70]	—	—	—	—	—	46	R6
		ADC_0	—	—	AN[4](3)	—						
E[7]	PCR[71]	SIUL	—	ALT0	GPI[71]	—	—	—	—	—	48	T6
		ADC_0	—	—	AN[6](3)	—						
E[9]	PCR[73]	SIUL	—	ALT0	GPI[73]	—	—	—	—	—	61	T10
		ADC_1	—	—	AN[7](3)	—						
E[10]	PCR[74]	SIUL	—	ALT0	GPI[74]	—	—	—	—	—	63	T11
		ADC_1	—	—	AN[8](3)	—						
E[11]	PCR[75]	SIUL	—	ALT0	GPI[75]	—	—	—	—	—	65	U11
		ADC_1	—	—	AN[4](3)	—						
E[12]	PCR[76]	SIUL	—	ALT0	GPI[76]	—	—	—	—	—	67	T12
		ADC_1	—	—	AN[6](3)	—						
E[13]	PCR[77]	SIUL	GPIO[77]	ALT0	GPIO[77]	—	—	M	S	—	117	D12
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=1						
		DSPI_2	CS3	ALT2	—	—						
		SIUL	—	—	EIRQ[25]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
E[14]	PCR[78]	SIUL	GPIO[78]	ALT0	GPIO[78]	—	—	M	S	—	119	B12
		eTimer_1	ETC[5]	ALT1	ETC[5]	PSMI[14]; PADSEL=3						
		SIUL	—	—	EIRQ[26]	—						
E[15]	PCR[79]	SIUL	GPIO[79]	ALT0	GPIO[79]	—	—	M	S	—	121	B11
		DSPI_0	CS1	ALT1	—	—						
		SIUL	—	—	EIRQ[27]	—						
Port F												
F[0]	PCR[80]	SIUL	GPIO[80]	ALT0	GPIO[80]	—	—	M	S	—	133	D7
		FlexPWM_0	A[1]	ALT1	A[1]	PSMI[21]; PADSEL=2						
		eTimer_0	—	—	ETC[2]	PSMI[37]; PADSEL=1						
		SIUL	—	—	EIRQ[28]	—						
F[3]	PCR[83]	SIUL	GPIO[83]	ALT0	GPIO[83]	—	—	M	S	—	139	B5
		DSPI_0	CS6	ALT1	—	—						
F[4]	PCR[84]	SIUL	GPIO[84]	ALT0	GPIO[84]	—	—	F	S	—	4	D2
		NPC	MDO[3]	ALT2	—	—						
F[5]	PCR[85]	SIUL	GPIO[85]	ALT0	GPIO[85]	—	—	F	S	—	5	D1
		NPC	MDO[2]	ALT2	—	—						
F[6]	PCR[86]	SIUL	GPIO[86]	ALT0	GPIO[86]	—	—	F	S	—	8	E2
		NPC	MDO[1]	ALT2	—	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
F[7]	PCR[87]	SIUL	GPIO[87]	ALT0	GPIO[87]	—	—	F	S	—	19	J1
		NPC	MCKO	ALT2	—	—						
F[8]	PCR[88]	SIUL	GPIO[88]	ALT0	GPIO[88]	—	—	F	S	—	20	K2
		NPC	$\overline{\text{MSEO[1]}}$	ALT2	—	—						
F[9]	PCR[89]	SIUL	GPIO[89]	ALT0	GPIO[89]	—	—	F	S	—	23	K1
		NPC	$\overline{\text{MSEO[0]}}$	ALT2	—	—						
F[10]	PCR[90]	SIUL	GPIO[90]	ALT0	GPIO[90]	—	—	F	S	—	24	L1
		NPC	$\overline{\text{EVTO}}$	ALT2	—	—						
F[11]	PCR[91]	SIUL	GPIO[91]	ALT0	GPIO[91]	—	—	M	S	—	25	L2
		NPC	—	ALT2	$\overline{\text{EVTI}}$	—						
F[12]	PCR[92]	SIUL	GPIO[92]	ALT0	GPIO[92]	—	—	M	S	—	106	C17
		eTimer_1	ETC[3]	ALT1	ETC[3]	PSMI[12]; PADSEL=2						
		SIUL	—	—	EIRQ[30]	—						
F[13]	PCR[93]	SIUL	GPIO[93]	ALT0	GPIO[93]	—	—	M	S	—	112	B14
		eTimer_1	ETC[4]	ALT1	ETC[4]	PSMI[13]; PADSEL=3						
		SIUL	—	—	EIRQ[31]	—						
F[14]	PCR[94]	SIUL	GPIO[94]	ALT0	GPIO[94]	—	—	M	S	—	115	C13
		LINFlexD_1	TXD	ALT1	—	—						
F[15]	PCR[95]	SIUL	GPIO[95]	ALT0	GPIO[95]	—	—	M	S	—	113	D13
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=2						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
FCCU												
FCCU_F[0]	—	FCCU	F[0]	ALT0	—	—	—	S	S	27	38	R2
FCCU_F[1]	—	FCCU	F[1]	ALT0	—	—	—	S	S	97	141	C4
Port G												
G[2]	PCR[98]	SIUL	GPIO[98]	ALT0	GPIO[98]	—	—	M	S	—	102	E16
		FlexPWM_0	X[2]	ALT1	X[2]	PSMI[29]; PADSEL=1						
		DSPI_1	CS1	ALT2	—	—						
G[3]	PCR[99]	SIUL	GPIO[99]	ALT0	GPIO[99]	—	—	M	S	—	104	D17
		FlexPWM_0	A[2]	ALT1	A[2]	PSMI[22]; PADSEL=2						
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=3						
G[4]	PCR[100]	SIUL	GPIO[100]	ALT0	GPIO[100]	—	—	M	S	—	100	F17
		FlexPWM_0	B[2]	ALT1	B[2]	PSMI[26]; PADSEL=2						
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=3						
G[5]	PCR[101]	SIUL	GPIO[101]	ALT0	GPIO[101]	—	—	M	S	—	85	N17
		FlexPWM_0	X[3]	ALT1	X[3]	PSMI[30]; PADSEL=2						
		DSPI_2	CS3	ALT2	—	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
G[6]	PCR[102]	SIUL	GPIO[102]	ALT0	GPIO[102]	—	—	M	S	—	98	G17
		FlexPWM_0	A[3]	ALT1	A[3]	PSMI[23]; PADSEL=3						
G[7]	PCR[103]	SIUL	GPIO[103]	ALT0	GPIO[103]		—	M	S	—	83	P17
		FlexPWM_0	B[3]	ALT1	B[3]	PSMI[27]; PADSEL=3						
G[8]	PCR[104]	SIUL	GPIO[104]	ALT0	GPIO[104]	—	—	M	S	—	81	P16
		FlexRay	DBG0	ALT1	—	—						
		DSPI_0	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=2						
		SIUL	—	—	EIRQ[21]	—						
G[9]	PCR[105]	SIUL	GPIO[105]	ALT0	GPIO[105]	—	—	M	S	—	79	R17
		FlexRay	DBG1	ALT1	—	—						
		DSPI_1	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=2						
		SIUL	—	—	EIRQ[29]	—						
G[10]	PCR[106]	SIUL	GPIO[106]	ALT0	GPIO[106]	—	—	M	S	—	77	P15
		FlexRay	DBG2	ALT1	—	—						
		DSPI_2	CS3	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=1						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
G[11]	PCR[107]	SIUL	GPIO[107]	ALT0	GPIO[107]	—	—	M	S	—	75	U15
		FlexRay	DBG3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=2						
G[12]	PCR[108]	SIUL	GPIO[108]	ALT0	GPIO[108]	—	—	F	S	—	—	F2
		NPC	MDO[11]	ALT2	—	—						
G[13]	PCR[109]	SIUL	GPIO[109]	ALT0	GPIO[109]	—	—	F	S	—	—	H1
		NPC	MDO[10]	ALT2	—	—						
G[14]	PCR[110]	SIUL	GPIO[110]	ALT0	GPIO[110]	—	—	F	S	—	—	A6
		NPC	MDO[9]	ALT2	—	—						
G[15]	PCR[111]	SIUL	GPIO[111]	ALT0	GPIO[111]	—	—	F	S	—	—	J2
		NPC	MDO[8]	ALT2	—	—						
Port H												
H[0]	PCR[112]	SIUL	GPIO[112]	ALT0	GPIO[112]	—	—	F	S	—	—	A5
		NPC	MDO[7]	ALT2	—	—						
H[1]	PCR[113]	SIUL	GPIO[113]	ALT0	GPIO[113]	—	—	F	S	—	—	F1
		NPC	MDO[6]	ALT2	—	—						
H[2]	PCR[114]	SIUL	GPIO[114]	ALT0	GPIO[114]	—	—	F	S	—	—	A4
		NPC	MDO[5]	ALT2	—	—						
H[3]	PCR[115]	SIUL	GPIO[115]	ALT0	GPIO[115]	—	—	F	S	—	—	G1
		NPC	MDO[4]	ALT2	—	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
H[4]	PCR[116]	SIUL	GPIO[116]	ALT0	GPIO[116]	—	—	M	S	—	—	L16
		FlexPWM_1	X[0]	ALT1	X[0]	—						
		eTimer_2	ETC[0]	ALT2	ETC[0]	PSMI[39]; PADSEL=0						
H[5]	PCR[117]	SIUL	GPIO[117]	ALT0	GPIO[117]	—	—	M	S	—	—	M17
		FlexPWM_1	A[0]	ALT1	A[0]	—						
		DSPI_0	CS4	ALT3	—	—						
H[6]	PCR[118]	SIUL	GPIO[118]	ALT0	GPIO[118]	—	—	M	S	—	—	H17
		FlexPWM_1	B[0]	ALT1	B[0]	—						
		DSPI_0	CS5	ALT3	—	—						
H[7]	PCR[119]	SIUL	GPIO[119]	ALT0	GPIO[119]	—	—	M	S	—	—	K16
		FlexPWM_1	X[1]	ALT1	X[1]	—						
		eTimer_2	ETC[1]	ALT2	ETC[1]	PSMI[40]; PADSEL=0						
H[8]	PCR[120]	SIUL	GPIO[120]	ALT0	GPIO[120]	—	—	M	S	—	—	K15
		FlexPWM_1	A[1]	ALT1	A[1]	—						
		DSPI_0	CS6	ALT3	—	—						
H[9]	PCR[121]	SIUL	GPIO[121]	ALT0	GPIO[121]	—	—	M	S	—	—	G16
		FlexPWM_1	B[1]	ALT1	B[1]	—						
		DSPI_0	CS7	ALT3	—	—						
H[10]	PCR[122]	SIUL	GPIO[122]	ALT0	GPIO[122]	—	—	M	S	—	—	A11
		FlexPWM_1	X[2]	ALT1	X[2]	—						
		eTimer_2	ETC[2]	ALT2	ETC[2]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
H[11]	PCR[123]	SIUL	GPIO[123]	ALT0	GPIO[123]	—	—	M	S	—	—	C11
		FlexPWM_1	A[2]	ALT1	A[2]	—						
H[12]	PCR[124]	SIUL	GPIO[124]	ALT0	GPIO[124]	—	—	M	S	—	—	B10
		FlexPWM_1	B[2]	ALT1	B[2]	—						
H[13]	PCR[125]	SIUL	GPIO[125]	ALT0	GPIO[125]	—	—	M	S	—	—	G15
		FlexPWM_1	X[3]	ALT1	X[3]	—						
		eTimer_2	ETC[3]	ALT2	ETC[3]	PSMI[42]; PADSEL=0						
H[14]	PCR[126]	SIUL	GPIO[126]	ALT0	GPIO[126]	—	—	M	S	—	—	A12
		FlexPWM_1	A[3]	ALT1	A[3]	—						
		eTimer_2	ETC[4]	ALT2	ETC[4]	—						
H[15]	PCR[127]	SIUL	GPIO[127]	ALT0	GPIO[127]	—	—	M	S	—	—	J17
		FlexPWM_1	B[3]	ALT1	B[3]	—						
		eTimer_2	ETC[5]	ALT2	ETC[5]	—						
Port I												
I[0]	PCR[128]	SIUL	GPIO[128]	ALT0	GPIO[128]	—	—	M	S	—	—	C9
		eTimer_2	ETC[0]	ALT1	ETC[0]	PSMI[39]; PADSEL=1						
		DSPI_0	CS4	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[0]	—						

Table 12. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	—	M	S	—	—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	—	M	S	—	—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	—	M	S	—	—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$	PCR[132]	SIUL	GPIO[132]	ALT0	GPIO[132]	—	—	F	S	—	—	K3
		NPC	$\overline{\text{RDY}}$	ALT2	—	—						

1. Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)
2. The default function of this pin out of reset is ALT1 (TDO).
3. Analog