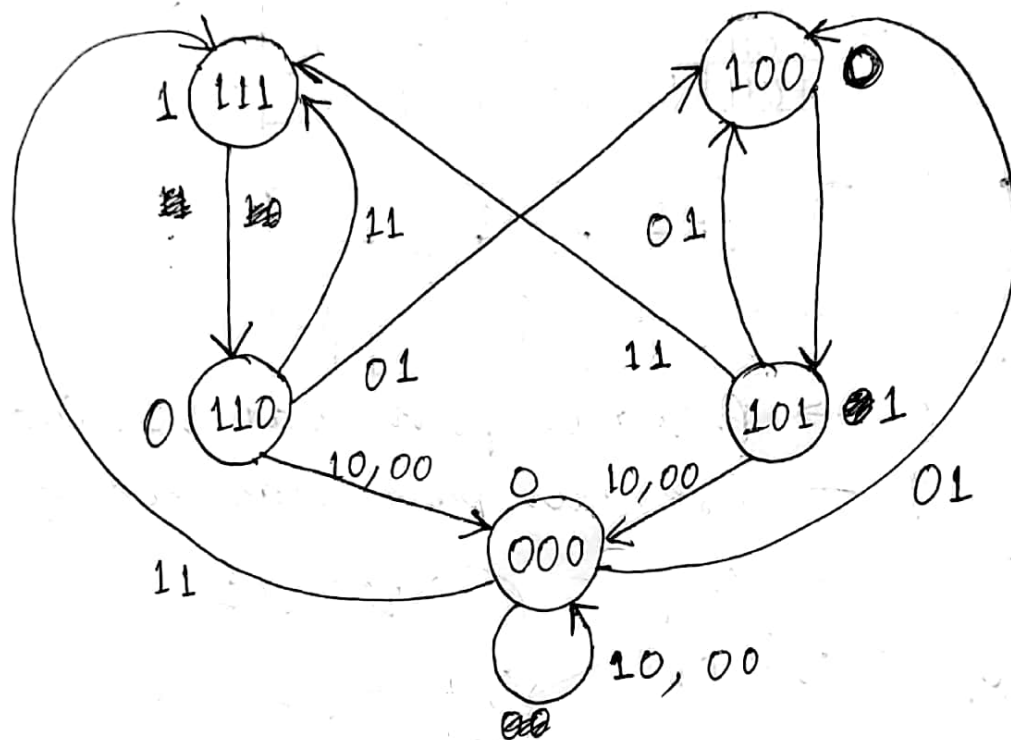NAME: SHUBHRANEEL PAL, SANYUKTA DEOGADE,
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Group 24

Part 1

The FSM of Manchester encoding is
as follows. This is a moore output
as the output depends only on present state.

The state 000 represents the state when
valid = 0;
The input is 2 bit = D, V (in this order)
The upper states represent start of clock
cycles and the lower states, the second
half of clock cycle. The output is for
each state is written beside the state. It
is produced at double the input rate.

Outputs (for states)

$100 \rightarrow 0$, $101 \rightarrow 1$, $111 \rightarrow 1$, $110 \rightarrow 0$

The ~~right~~ left states are used when data is 1
and the right states when data is 0.

Part 2

Input (FSM) = 3-bit → H, V, T
Output (FSM) = 3-bit → PH, PV, ST

Output table

	000	001	011	010	110	111	101	100
0	000	000	101	011	011	101	101	101
1	000	000	011	011	101	011	011	101

Transition table

	000	001	011	010	110	111	101	100
0	0	0	0	0	1	0	0	1
1	1	1	1	0	0	1	1	1

States → 0 → Previous pass was vertical
         1 → Previous pass was horizontal

010/111
110/101
100/101
100/101
000/010
010/011
110/011
xx1/010
000/100
xx1/100