浙江大学

本科实验报告

课程名称：	数字逻辑设计
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2022 年　10　月　24　日

浙江大学实验报告

课程名称：数字逻辑设计 实验类型：绘图实验

实验项目名称：7 段数码管显示译码器设计与应用

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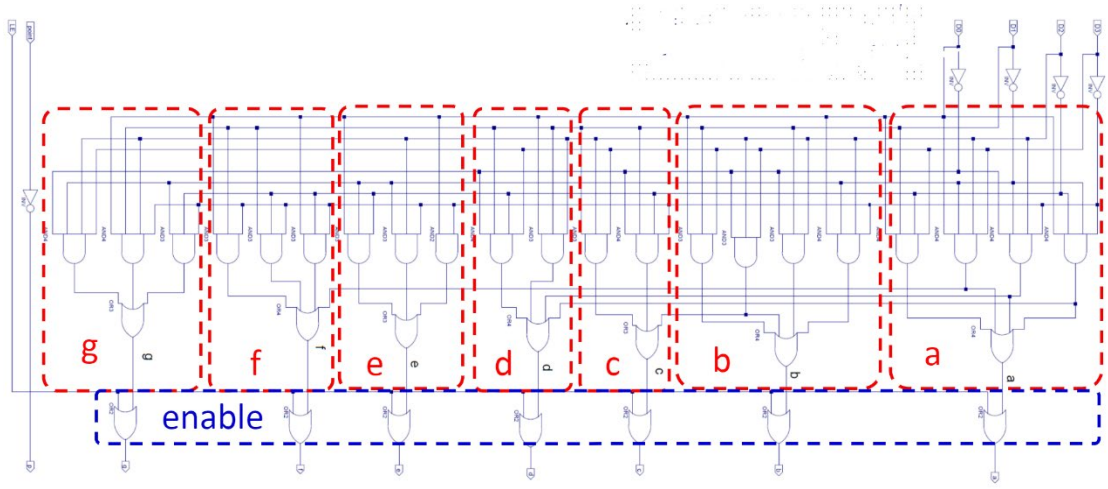
实验地点：东 4-509 实验日期：2022 年 10 月 24 日

一、 实验目的：

① 掌握七数码管显示原理
② 掌握七段码显示译码设计
③ 进一步熟悉 ISE 平台及下载实验平台物理验证

实验一：原理图设计实现显示译码 MyMC14495 模块

新建工程，工程名称用 MyMC14495。新建 Schematic 源文件，文件名称用 MyMC14495。用如下原理图进行设计。



用 ISE 的 Edit 的 Change Sheet Size 菜单项来改变原理图绘图区的尺寸。Check Design Rules，检查错误。View HDL Functional Model，查看并学习 Verilog HDL 代码

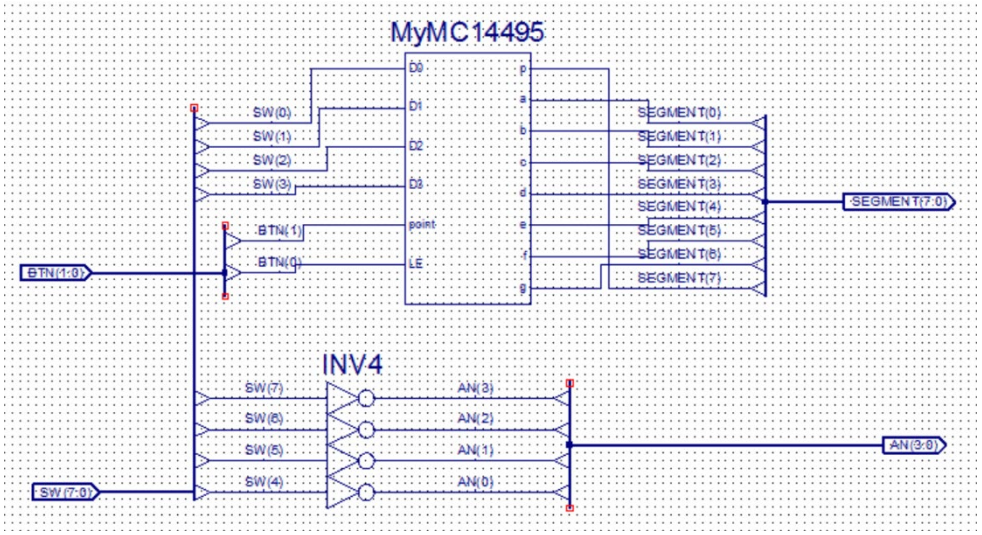
对 MyMC14495 模块进行仿真，激励代码如下

```
integer i;                      for (i=0; i<=15;i=i+1) begin
initial begin                       #50;
    D3 = 0;                         {D3,D2,D1,D0}=i;
    D2 = 0;                         point = i;
    D1 = 0;                     end
    D0 = 0;
    LE = 0;                     #50;
    point = 0;                  LE = 1;
                            end
```

Create Schematic Symbol，系统生成 MyMC14495 模块的逻辑符号图文件，文件后缀.sym。同时利用波形进行仿真。

实验二：用 MyMC14495 模块实现数码管显示

① 新建工程 DispNumber_sch。新建 schematic 文件 DispNumber_sch，复制 MyMC14495.sym 和.sch 到工程根目录，在 symbols 框里的第一个元件，就是 MyMC14495。根据前面原理，用如下原理图方式输入。



② 仿真下载

UCF 引脚定义

输入

SW[7:4]=AN[3:0]，SW[3:0]=D3D2D1D0，SW[14]=LE，SW[15]=point

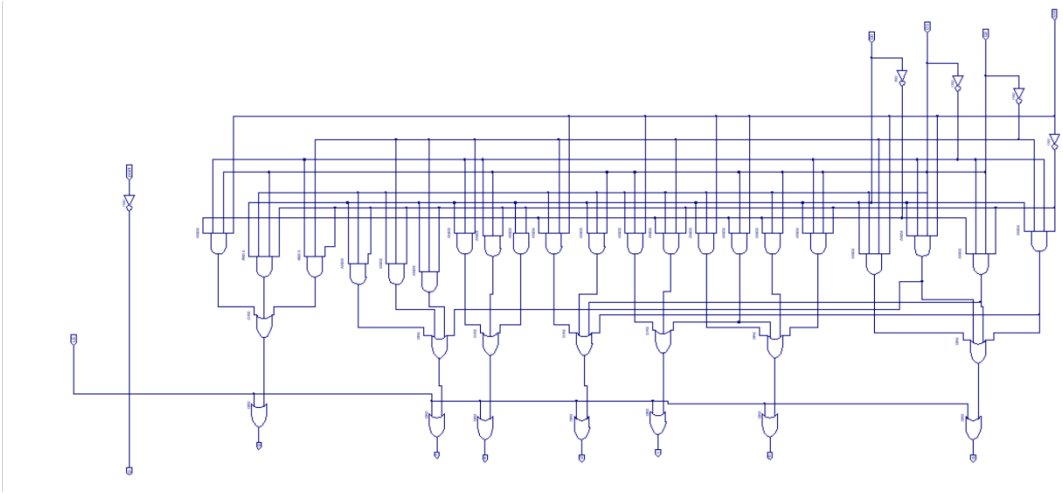
输出

a-g，p

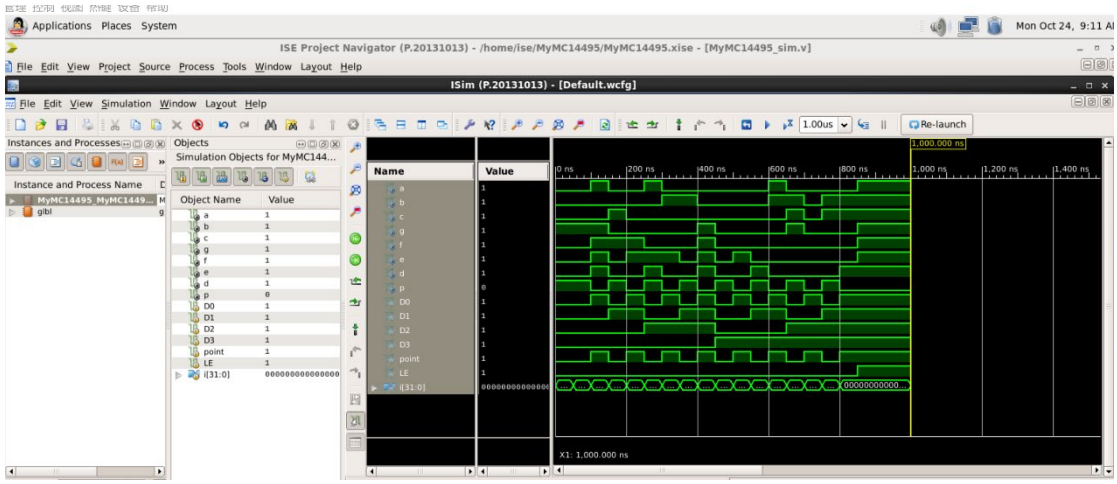
建立 k7.ucf 进行验证

二、实验数据记录和处理

实验一：原理图设计实现显示译码 MyMC14495 模块



自主作图如上



实验仿真波形如上

实验得到的 Verilog 代码如下

```
////////////////////////////////////////////////////////////////////////////////
// Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
////////////////////////////////////////////////////////////////////////////////
//   ____  ____
//  /   /\/   /
// /___/  \  /    Vendor: Xilinx
// \   \   \/     Version : 14.7
//  \   \         Application : sch2hdl
//  /   /         Filename : MyMC14495.vf
// /___/   /\     Timestamp : 10/24/2022 09:05:55
// \   \  /  \
//  \___\/\___\
//
//Command: /opt/Xilinx/14.7/ISE_DS/ISE/bin/lin64/unwrapped/sch2hdl -
intstyle ise -family kintex7 -verilog MyMC14495.vf -
w /home/ise/MyMC14495/MyMC14495.sch
//Design Name: MyMC14495
//Device: kintex7
//Purpose:
//    This verilog netlist is translated from an ECS schematic.It can be
//    synthesized and simulated, but it should not be modified.
```

```
//
`timescale 1ns / 1ps
module MyMC14495(D0, D1, D2, D3, LE, point, a, b, c, d, e, f, g, p);
      input D0;
      input D1;
      input D2;
      input D3;
      input LE;
      input point;
    output a;
    output b;
    output c;
    output d;
    output e;
    output f;
    output g;
    output p;
    wire XLXN_7;
    wire XLXN_9;
    wire XLXN_16;
    wire XLXN_19;
    wire XLXN_25;
    wire XLXN_26;
    wire XLXN_27;
    wire XLXN_28;
    wire XLXN_30;
    wire XLXN_31;
    wire XLXN_33;
    wire XLXN_34;
    wire XLXN_35;
    wire XLXN_36;
    wire XLXN_37;
    wire XLXN_38;
    wire XLXN_39;
    wire XLXN_40;
    wire XLXN_41;
    wire XLXN_43;
    wire XLXN_44;
    wire XLXN_45;
    wire XLXN_46;
    wire XLXN_48;
    wire XLXN_49;
    wire XLXN_52;
    wire XLXN_54;
    wire XLXN_57;
    wire XLXN_58;
    wire XLXN_59;
    wire XLXN_60;
    wire XLXN_65;
    INV   XLXI_1 (.I(D3),
                  .O(XLXN_7));
    INV   XLXI_2 (.I(D2),
                  .O(XLXN_9));
    INV   XLXI_3 (.I(D1),
                  .O(XLXN_16));
    INV   XLXI_4 (.I(D0),
                  .O(XLXN_19));
    AND4   XLXI_5 (.I0(D0),
                   .I1(XLXN_9),
```

```
                .I2(XLXN_16),
                .I3(XLXN_7),
                .O(XLXN_45));
AND4   XLXI_6 (.I0(XLXN_19),
                .I1(XLXN_16),
                .I2(D2),
                .I3(XLXN_7),
                .O(XLXN_46));
AND4   XLXI_7 (.I0(D0),
                .I1(XLXN_16),
                .I2(D1),
                .I3(D3),
                .O(XLXN_49));
AND4   XLXI_8 (.I0(D0),
                .I1(D1),
                .I2(XLXN_9),
                .I3(D3),
                .O(XLXN_48));
AND4   XLXI_9 (.I0(D0),
                .I1(XLXN_16),
                 .I2(D2),
                .I3(XLXN_7),
                .O(XLXN_44));
AND3   XLXI_10 (.I0(XLXN_19),
                 .I1(D1),
                 .I2(D2),
                 .O(XLXN_43));
AND3   XLXI_11 (.I0(XLXN_19),
                 .I1(D2),
                 .I2(D3),
                 .O(XLXN_40));
AND3   XLXI_12 (.I0(D0),
                 .I1(D1),
                 .I2(D3),
                 .O(XLXN_41));
AND3   XLXI_13 (.I0(D1),
                 .I1(D2),
                 .I2(D3),
                 .O(XLXN_38));
AND4   XLXI_14 (.I0(XLXN_19),
                 .I1(D1),
                 .I2(XLXN_9),
                 .I3(XLXN_7),
                 .O(XLXN_39));
AND4   XLXI_15 (.I0(XLXN_19),
                 .I1(D1),
                 .I2(XLXN_9),
                 .I3(D3),
                 .O(XLXN_36));
AND3   XLXI_16 (.I0(D0),
                 .I1(D1),
                 .I2(D2),
                 .O(XLXN_37));
AND2   XLXI_17 (.I0(D0),
                 .I1(XLXN_7),
                 .O(XLXN_35));
AND3   XLXI_18 (.I0(XLXN_16),
                 .I1(D2),
                 .I2(XLXN_7),
```

```
                .O(XLXN_34));
AND3   XLXI_19 (.I0(D0),
                .I1(XLXN_16),
                .I2(XLXN_9),
                .O(XLXN_33));
AND3   XLXI_20 (.I0(D0),
                .I1(XLXN_9),
                .I2(XLXN_7),
                .O(XLXN_31));
AND3   XLXI_21 (.I0(D1),
                .I1(XLXN_9),
                .I2(XLXN_7),
                .O(XLXN_30));
AND3   XLXI_22 (.I0(D0),
                .I1(D1),
                .I2(XLXN_7),
                .O(XLXN_28));
AND3   XLXI_23 (.I0(XLXN_16),
                .I1(XLXN_9),
                .I2(XLXN_7),
                .O(XLXN_27));
AND4   XLXI_24 (.I0(D0),
                .I1(D1),
                .I2(D2),
                .I3(XLXN_7),
                .O(XLXN_26));
AND4   XLXI_25 (.I0(XLXN_19),
                .I1(XLXN_16),
                .I2(D2),
                .I3(D3),
                .O(XLXN_25));
OR3    XLXI_26 (.I0(XLXN_25),
                .I1(XLXN_26),
                .I2(XLXN_27),
                .O(XLXN_57));
OR4    XLXI_27 (.I0(XLXN_28),
                .I1(XLXN_30),
                .I2(XLXN_31),
                .I3(XLXN_49),
                .O(XLXN_58));
OR3    XLXI_28 (.I0(XLXN_33),
                .I1(XLXN_34),
                .I2(XLXN_35),
                .O(XLXN_59));
OR4    XLXI_29 (.I0(XLXN_36),
                .I1(XLXN_37),
                .I2(XLXN_46),
                .I3(XLXN_45),
                .O(XLXN_60));
OR3    XLXI_30 (.I0(XLXN_38),
                .I1(XLXN_39),
                .I2(XLXN_40),
                .O(XLXN_54));
OR4    XLXI_31 (.I0(XLXN_41),
                .I1(XLXN_40),
                .I2(XLXN_43),
                .I3(XLXN_44),
                .O(XLXN_52));
OR4    XLXI_32 (.I0(XLXN_48),
```

```
                    .I1(XLXN_49),
                    .I2(XLXN_46),
                    .I3(XLXN_45),
                    .O(XLXN_65));
    OR2   XLXI_33 (.I0(LE),
                    .I1(XLXN_65),
                    .O(a));
    OR2   XLXI_34 (.I0(LE),
                    .I1(XLXN_52),
                    .O(b));
    OR2   XLXI_35 (.I0(LE),
                    .I1(XLXN_54),
                    .O(c));
    OR2   XLXI_36 (.I0(LE),
                    .I1(XLXN_60),
                    .O(d));
    OR2   XLXI_37 (.I0(LE),
                    .I1(XLXN_59),
                    .O(e));
    OR2   XLXI_38 (.I0(LE),
                    .I1(XLXN_58),
                    .O(f));
    OR2   XLXI_39 (.I0(LE),
                    .I1(XLXN_57),
                    .O(g));
    INV   XLXI_40 (.I(point),
                    .O(p));
endmodule
```

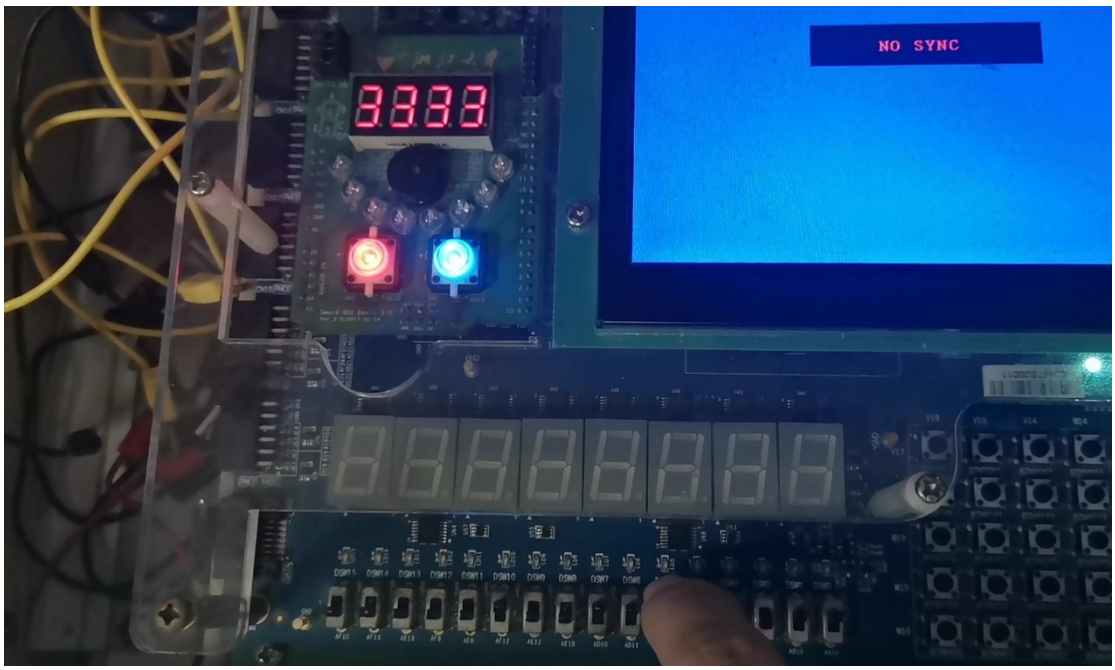
实验二：用 MyMC14495 模块实现数码管显示

K7.ucf 如下

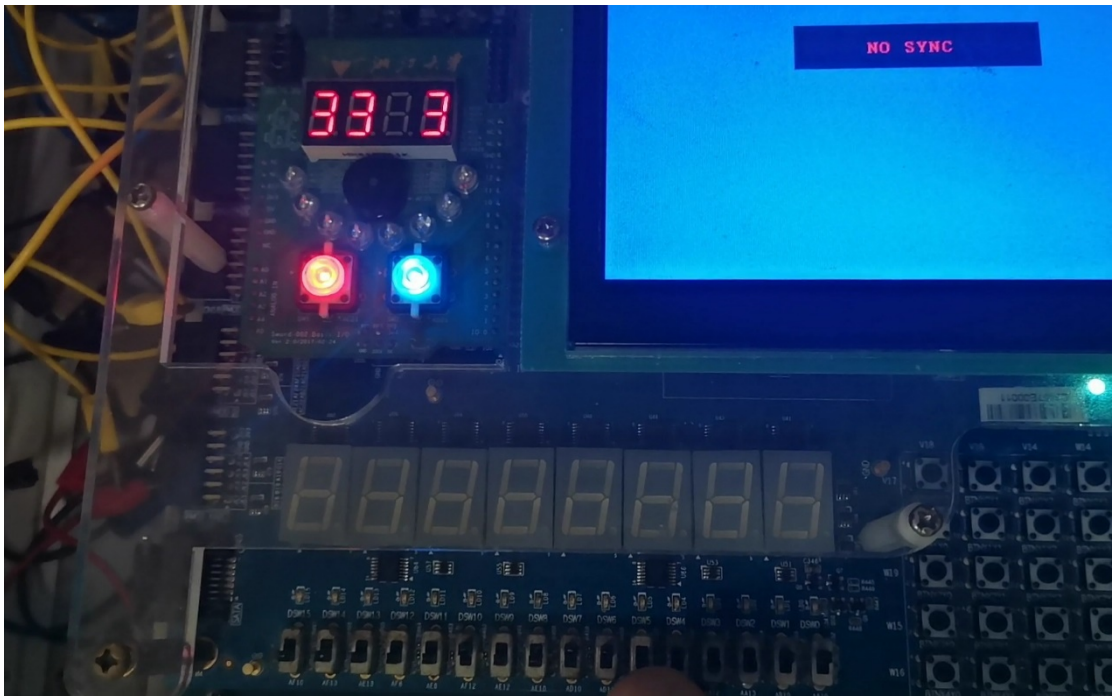
```
NET "BTN[0]"LOC = AF13 | IOSTANDARD = LVCMOS15;#SW[14]
NET "BTN[1]"LOC = AF10 | IOSTANDARD = LVCMOS15;#SW[15]
NET "SEGMENT[0]"LOC = AB22 | IOSTANDARD = LVCMOS33;#a
NET "SEGMENT[1]" LOC = AD24 | IOSTANDARD = LVCMOS33;#b
NET "SEGMENT[2]" LOC = AD23 | IOSTANDARD = LVCMOS33;#c
NET "SEGMENT[3]" LOC = Y21 | IOSTANDARD = LVCMOS33;#d
NET "SEGMENT[4]" LOC = W20 | IOSTANDARD = LVCMOS33;#e
NET "SEGMENT[5]" LOC = AC24 | IOSTANDARD = LVCMOS33;#f
NET "SEGMENT[6]" LOC = AC23 | IOSTANDARD = LVCMOS33;#g
NET "SEGMENT[7]" LOC = AA22 | IOSTANDARD = LVCMOS33;#point
NET "AN[0]" LOC = AD21 | IOSTANDARD = LVCMOS33;
NET "AN[1]" LOC = AC21 | IOSTANDARD = LVCMOS33;
NET "AN[2]" LOC = AB21 | IOSTANDARD = LVCMOS33;
NET "AN[3]" LOC = AC22 | IOSTANDARD = LVCMOS33;
NET "SW[0]" LOC = AA10 | IOSTANDARD = LVCMOS15;
NET "SW[1]" LOC = AB10 | IOSTANDARD = LVCMOS15;
NET "SW[2]" LOC = AA13 | IOSTANDARD = LVCMOS15;
```

```
NET "SW[3]" LOC = AA13 | IOSTANDARD = LVCMOS15;
NET "SW[4]" LOC = AA12 | IOSTANDARD = LVCMOS15;
NET "SW[5]" LOC = Y13 | IOSTANDARD = LVCMOS15;
NET "SW[6]" LOC = AB10 | IOSTANDARD = LVCMOS15;
NET "SW[7]" LOC = AD10 | IOSTANDARD = LVCMOS15;
```

实验过程照片如下

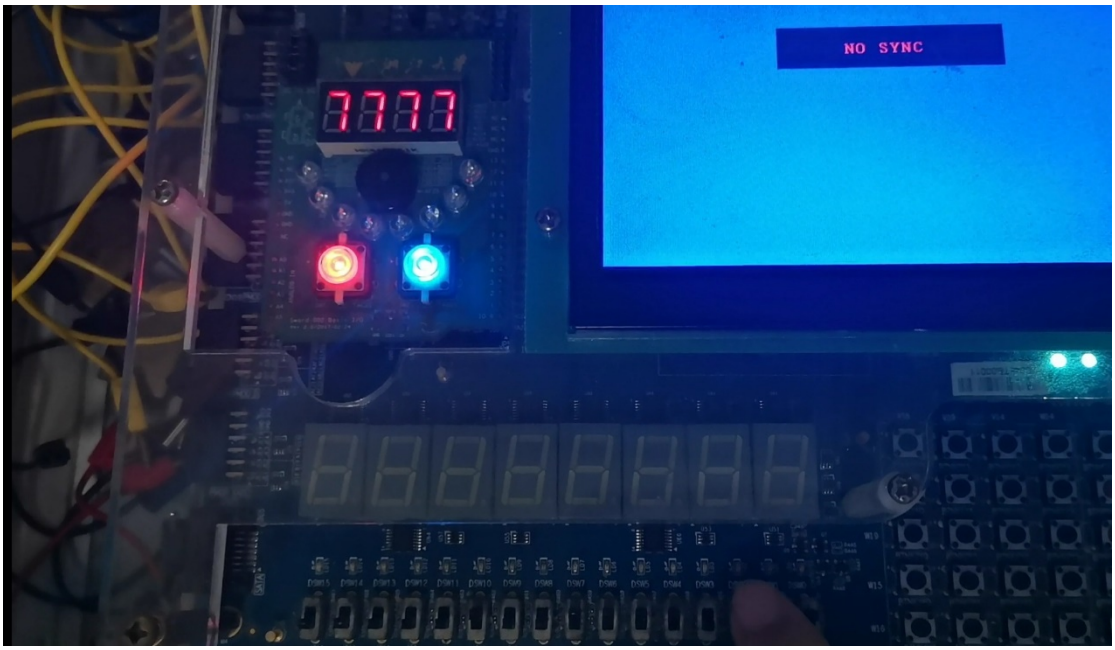


改变其中某一个数字是否显示

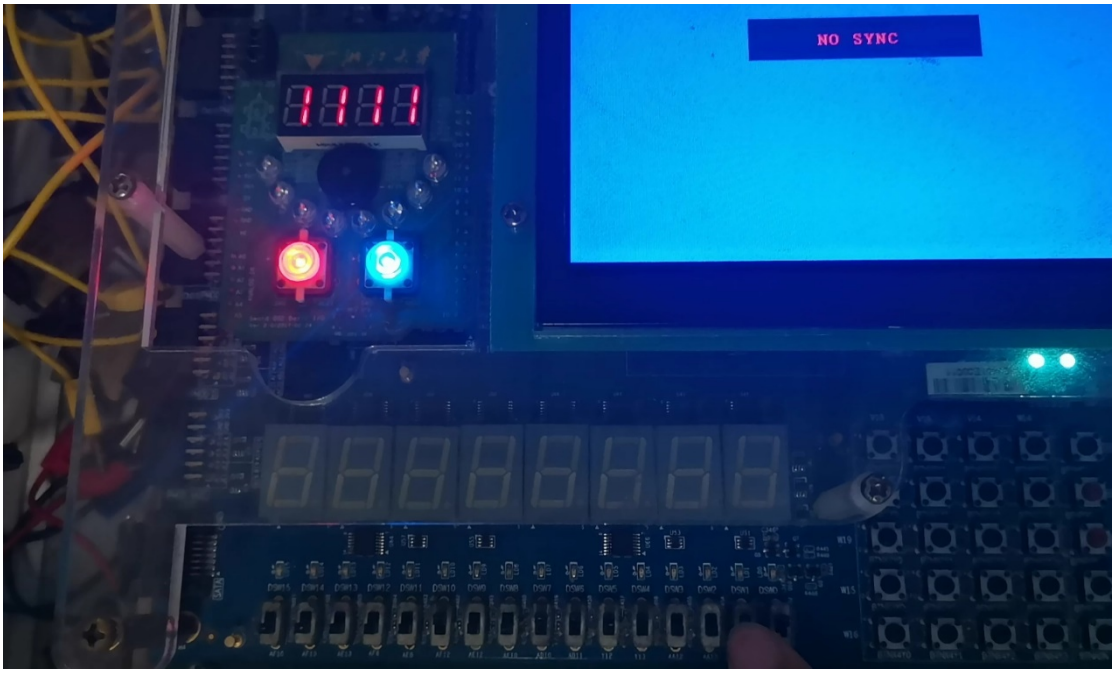


改变显示出来的数字

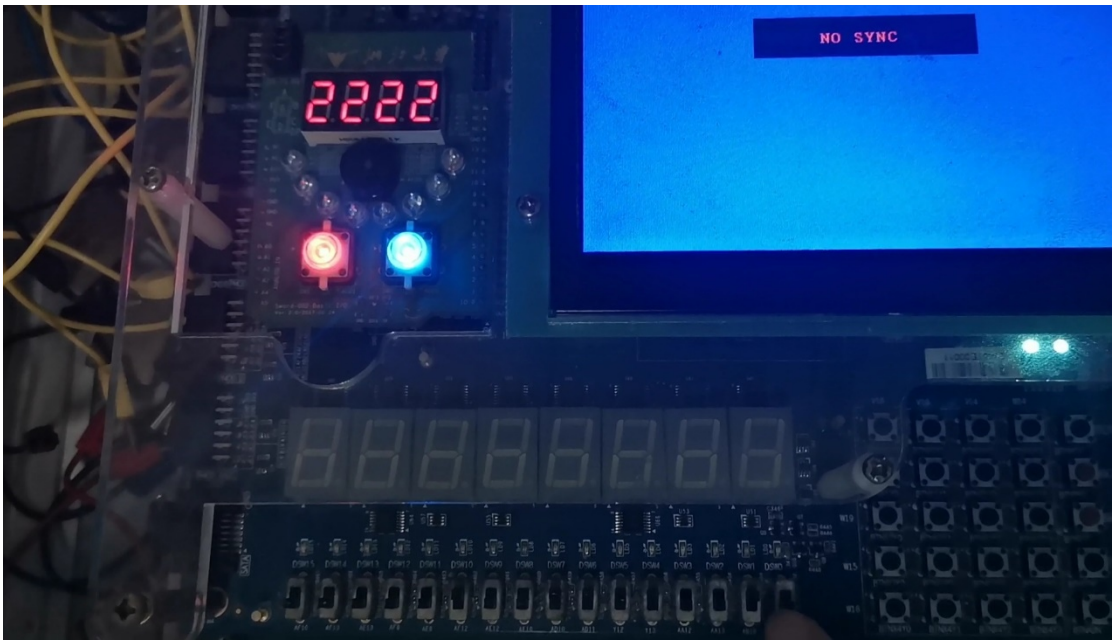
改变数字例 1



改变数字例 2



改变数字例 3



注：该实验已经在 2022.10.24 晚由助教验收通过

三、实验结果与分析

实验结果和预测结果一样，实验操作正确无误。

四、讨论、心得 （选填）

实验过程中我体会到要认真对待每一次操作，正如我多次因为不小心而操作不熟练使得实验进程受阻。