Weeks 3 & 4 Outline

- Multiple output SOP designs
- Verilog implementations
 - using SOP
 - using conditional statements
 - using case statements
- Logic operations on number systems
- More examples of combinational logic
- Exam 1 Tuesday, Sept. 25th

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Part 2 – Slide 50



Addition Tables

Decimal										
+	0	1	2	3	4	5	6	7	8	9
0	0	1	2	3	4	5	6	7	8	9
1	1	2	3	4	5	6	7	8	9	0
2	2	3	4	5	6	7	8	9	0	1
3	3	4	5	6	7	8	9	0	1	2
4	4	5	6	7	8	9	0	1	2	3
5	5	6	7	8	9	0	1	2	3	4
6	6	7	8	9	0	1	2	3	4	5
7	7	8	9	0	1	2	3	4	5	6
8	8	9	0	1	2	3	4	5	6	7
9	9	0	1	2	3	4	5	6	7	8

Binary 1

Denotes Carry Operation

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Addition Table for Hexadecimal																		
	+	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F	Ī
	0	0	1	2	3	4	5	6	7	8	9	Α	В	O	D	Ш	F	
	1	1	2	3	4	5	6	7	8	တ	Α	В	O	ם	Е	F	0	
	2	2	3	4	5	6	7	8	9	Α	В	O	D	Е	F	0	1	I
	3	3	4	5	6	7	8	9	Α	В	С	D	Е	F	0	1	2	
ı	4	4	5	6	7	8	9	Α	В	С	D	Е	F	0	1	2	3	
ı	5	5	6	7	8	9	Α	В	С	D	Е	F	0	1	2	3	4	
	6	6	7	8	9	Α	В	С	D	Е	F	0	1	2	3	4	5	
L	7	7	8	9	Α	В	С	D	Е	F	0	1	2	3	4	5	6	
ı	8	8	9	Α	В	С	D	Е	F	0	1	2	3	4	5	6	7	
L	9	9	Α	В	С	D	Е	F	0	1	2	3	4	5	6	7	8	
L	Α	Α	В	С	D	Е	F	0	1	2	3	4	5	6	7	8	9	
	В	В	C	Δ	Е	F	0	1	2	3	4	5	6	7	8	တ	Α	
	С	C	D	Е	F	0	1	2	ვ	4	5	6	7	8	9	Α	В	
	D	D	Е	F	0	1	2	3	4	5	6	7	8	9	Α	В	С	I
	Ε	Е	F	0	1	2	3	4	5	6	7	8	9	Α	В	O	D	1
	F	F	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	
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One Bit Addition (Half Adder)

• Arithmetically:

$$Z = A + B$$

• Logically (Verilog):

$$Z = A \wedge B;$$
 (xor)

$$C = A \& B;$$

Inp	uts	Outputs			
Α	В	Z	U		
0	0	0	0		
1	0	1	0		
0	1	1	0		
1	1	0	1		

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Multi-bit (Binary) Addition

- Compare to decimal addition
- Binary addition (expand to 5 bits)

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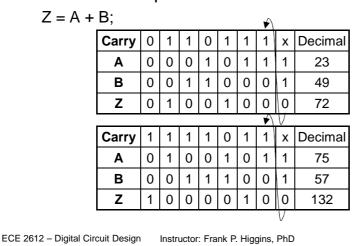
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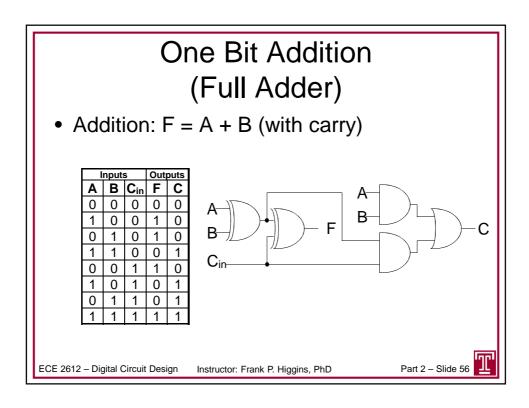
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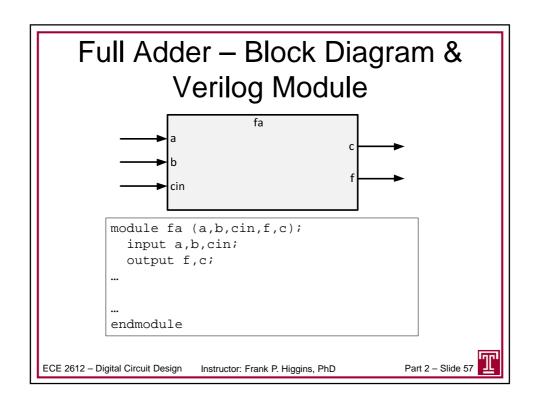


Multi-bit (Binary) Addition (cont.)

• Addition examples:





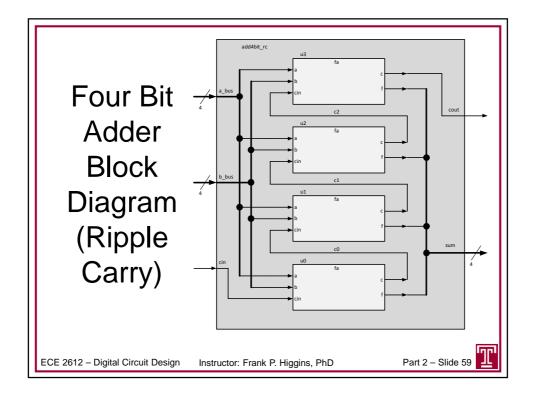


Full Adder – Block Diagram & Verilog Module

• Implementation in class or as homework

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Four Bit Adder Block Diagram (Ripple Carry)

Implementation in class or as homework

```
module add4bit_rc (a_bus, b_bus, cin, sum, cout);
    input [3:0]a_bus, b_bus;
    input cin;
    output [3:0]sum;
    output cout;

    // define the nets needed for interconnection
    // instantiate the full adders
...
...
endmodule
```

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Signed Integers

- Binary numbers can represent both positive and negative values.
- For an *n-bit* number, there are still 2ⁿ
 possible values, but now they are divided
 as half positive (including 0) and half
 negative.

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Signed Integer Representations

 Signed magnitude: the most significant bit is used as the sign bit, e.g.:

$$3_{10} = 0011_2$$
 $-3_{10} = 1011_2$

1's complement: change 0's to 1's and 1's to 0's (C code symbol: ~)

$$3_{10} = 0011_2$$
 $-3_{10} = 1100_2$

- Many problems with both:
 - have two representations for 0
 - difficult to do simple binary arithmetic

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Signed Integer Representations

- All processors use what is called 2's complement representation
- The conversion rule:
 - take the 1's complement of the binary number
 - add 1 to the binary number

$$3_{10} = 0011_2$$
 $\sim 0011_2 = 1100_2$ $-3_{10} = 1101_2$

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2's Complement Notation

- Example, 4 bit number:
 - 16 values
 - Unsigned: 0 to 15
 - Signed: -8 to +7
- One minor problem:
 - asymmetric in max & min values:
 - max: 2ⁿ⁻¹ 1
 - min: -2ⁿ⁻¹

Value	Unsigned Integer	Signed Integer
0000	0	0
0001	1	1
0010	2	2
0011	3	3
0100	4	4
0101	5	5
0110	6	6
0111	7	7
1000	8	-8
1001	9	-7
1010	10	-6
1011	11	-5
1100	12	-4
1101	13	-3
1110	14	-2
1111	15	-1

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2's Complement Notation

- A major advantage: arithmetic works seamlessly
 - addition
 - subtraction
- Examples:

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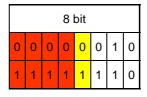


2's Complement Sign Extension

- To extend a signed number from *n* bits to *m* bits:
 - add m-n bits to the msb side
 - fill the extra bits with the value of the original msb
- Examples 4 bits to 8 bits:







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2's Complement in Hexadecimal

- Same rules, but different symbols
 - find the complement (~) of each symbol
 - add 1 to the hexadecimal number

Hex Symbol	~(Hex Symbol)	~(Hex Symbol) + 1
0	F	0
1	Е	F
3	E D C	E
	С	D
4	В	С
5	Α	В
6	9	Α
7	8	9
8	7	8
9	6	7
Α	5	6
B C	4	5
С	3	4
D	2	3
E	1	2
F	0	1
-	-	

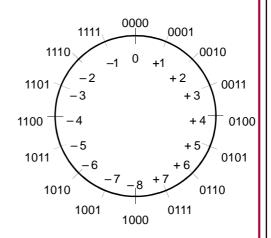
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Circular Representation of 2's complement, 4-bit numbers.

- 4-bit range, 16 numbers: -8 to +7
- Clockwise for addition; CCW for subtraction



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Parity

- Easiest implemented with XOR gates (remember our adders)
 - Example: 4 bit data to generate parity bit:
 - $P = a[3] ^ a[2] ^ a[1] ^ a[0]; // for even$
 - $P = \sim (a[3] \land a[2] \land a[1] \land a[0]);$ // for odd
 - Data checking 5 bit data checking bit: $check_bit = P ^a[3] ^a[2] ^a[1] ^a[0];$
- If even parity: check_bit should be 0
- If odd parity: check_bit should be 1

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Gate Completeness

- For any Boolean function need: AND, OR, NOT
- What can be done with a NAND gate?
 - NOT operation:
 - Connect both inputs together
 - AND operation
 - Connect output of NAND to input of NOT
 - OR operation
 - Connect NOT's to inputs of NAND

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Binary Addition (cont.)

• Addition - expressions

A/B/C_{in} result (carry)

$$0 + 0 + 0 = 0$$
 (0)

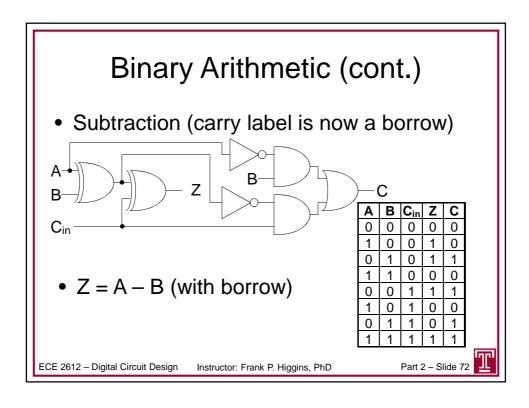
$$1 + 0 + 0 = 1$$
 (0)

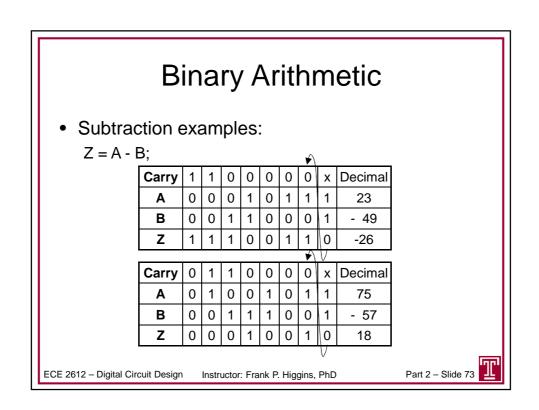
$$1 + 1 + 0 = 0$$
 (1)

$$1 + 1 + 1 = 1$$
 (1)

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- Use:
 - a) tables or
 - b) converting to decimal, and operating one digit at a time.
- Example of b):

Z = 0xBC4A + 0x3879

...

Z = 0xF4C3

Hex table 🧳									
Carry	1	0	1		X				
Α	В	O	4	4	٦				
В	3	8	7	9	9				
С	F	4	C	**	3				
-				\neg					

Decimal conversion									
Carry	1	0	1	Х					
Α	11	12	4	10					
В	3	8	7	9					
С	15	20	12	19					

C mod 16 15 4 12

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End of combinational logic lectures

• Review ... Exam 1

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