Jeonghyun Woo

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Education

University of British Columbia, Vancouver, BC Canada
Ph.D. in Electrical and Computer Engineering (Advisor: Prof. Prashant Nair) Sep. 2022 - Dec. 2026 (Expected)

Hanyang University, Seoul, Korea
M.S. in Electronics and Computer Engineering (Advisor: Prof. Ki-Seok Chung) Mar. 2018 - Feb. 2020
Dissertation: Row-hammering Mitigation Architecture for High Reliable DRAM
Cumulative GPA: 4.0/4.0

Hanyang University, Seoul, Korea
B.S. in Electronic Engineering (Advisor: Prof. Ki-Seok Chung) Mar. 2012 - Feb. 2018
Dissertation: Implementation of an FPGA-based CNN Accelerator using SDSoC
Cumulative GPA: 3.89/4.0 (Graduating with Honors - Summa Cum Laude)

Research Interests

Computer Architecture/Systems, Memory Systems, Security, and Reliability

Publications

Conferences

[2] **Jeonghyun Woo**, Gururaj Saileshwar, and Prashant Nair. "Scalable and Secure Row-Swap: Efficient and Safe Row Hammer Mitigation in Memory Systems", in ***29th International Symposium on High-Performance Computer Architecture (HPCA'23)***, Feburuay 2023. (acceptance rate: 25.0%) [Paper][Code][Slides]
Best Paper Award

[1] Kwangrae Kim, **Jeonghyun Woo**, Junsu Kim, and Ki-Seok Chung. "HammerFilter: Robust Protection and Low Hardware Overhead Method for RowHammer", in ***39th International Conference on Computer Design (ICCD'21)***, October 2021. (acceptance rate: 24.4%) [Paper][Slides][Video]

Posters

[1] Kwangrae Kim, Junsu Kim, **Jeonghyun Woo**, and Ki-Seok Chung. "HammerFilter: Robust Protection and Low Hardware Overhead Method for Row-Hammering", in ***58th ACM/IEEE Design Automation Conference (DAC'21)***, December 2021. [Poster]

Domestic (Korean) Conferences

[2] **Jeong-Hyun Woo**, and Ki-Seok Chung. "A Method to Find the Optimal Probability for Probability-driven Additional Row Refresh to Prevent DRAM Row Hammering", in ***The Korean Institute of Communications and Information Sciences Winter Conference***, January 2019.

[1] Chang-Woo Lee*, **Jeong-Hyun Woo***, Sang-Soo Park, and Ki-Seok Chung. "Implementation of an FPGA-based CNN Accelerator using SDSoC", in ***The Korean Institute of Communications and Information Sciences Fall Conference***, November 2017. (*Equal Contribution)**(Outstanding Paper Award)** [Code]

Honors and Awards

- ◇ **HPCA 2023 Best Paper Award (Top 2 of 91 accepted papers)** 2023
- ◇ HPCA 2023 Student Travel Grant 2023
- ◇ Faculty of Applied Science Graduate Award, University of British Columbia 2022
- ◇ President's Academic Excellence Initiative PhD Award, University of British Columbia 2022
- ◇ Hanyang Graduate School Scholarship - 70% of Tuition (4 Semesters) 2018 - 2019
- ◇ Hanyang Academic Excellence Award - Top 1% ranked in University 2016, 2017
- ◇ Hanyang Academic Excellence Award - Top 3% ranked in University 2016
- ◇ Hanyang Alumni Association Scholarship - Full Tuition (4 Semesters) 2016 - 2017
- ◇ Excellent Tutor Award in Engineering Mathematics Tutoring Program, Hanyang University 2016
- ◇ Hanyang University Scholarship - Full Tuition (4 Semesters) 2012 - 2013

Professional Experience

Micron Technology, Folsom, CA, USA
Sytems Research Engineering Intern May. 2023 - Aug. 2023
Supervisor: Ameen Akel
Explored Row Hammer Solutions for Future High-Bandwidth Memory

University of British Columbia, Vancouver, BC, Canada
Graduate Research Assistant at Systems and Architectures (STAR) Lab Sep. 2022 - Present
Graduate Teaching Assistant
◇ Computer Architecture (CPEN 411) Fall 2022, Fall 2023

University of Illinois Urbana-Champaign, Champagin, IL, USA
Graduate Research Assistant at Systems Platform Research Group Aug. 2020 - Jan. 2021

Hanyang University, Seoul, South Korea
Graduate Research Assistant at Embedded System on Chip (ESoC) Lab Mar. 2018 - Feb. 2020
Graduate Teaching Assistant
◇ VLSI Engineering (ELE 3081) Fall 2019
◇ SoC Design (ITE 4003) Spring 2018

Research Experience

Scalable and Secure Row-Swap: Efficient and Safe Row Hammer Mitigation in Memory Systems
Advisor: Prof. Prashant Nair, University of British Columbia Feb. 2022 - Aug. 2022
◇ Proposed a new Row Hammer attack pattern called Juggernaut that breaks the state-of-the-art Row Hammer protection "Randomized Row Swap" under 1 day
◇ Proposed a simple and robust defense against Juggernaut and other future unknown attacks
◇ Developed a significantly low-overhead and scalable Row Hammer mitigation
◇ Published a paper as the first author in HPCA 2023 and won **the Best Paper Award**

HammerFilter: Robust Protection and Low Hardware Overhead Method for RowHammer
Advisor: Prof. Ki-Seok Chung, Hanyang University Sep. 2020 - Jun. 2021
◇ Collaborative project with master's and undergraduate research students from Hanyang University
◇ Proposed a robust and low overhead RowHammer protection method using a modified version of the counting bloom filter
◇ Served as a mentor to master's and undergraduate research students, led the paper write-up, and discussed the idea
◇ Published a paper as the second author in ICCD 2021 and presented a poster as the third author in DAC 2021

Integrating Non-volatile Memory into Programmable Switches' Data Plane
Advisor: Prof. Jian Huang, UIUC Aug. 2020 - Dec. 2020
◇ Collaborative project with Ph.D. students
◇ Worked on integrating NVM into the data plane of programmable switches while maintaining line-rate packet processing
◇ Designed a light-weight accelerator to avoid high latency operations on the critical path
◇ Demonstrated 2× lower packet latency compared to the previous work TEA

Integrating Non-volatile Memory into GPUs
Advisor: Prof. Jian Huang, UIUC and Prof. Yifan Sun, William & Mary Aug. 2020 - Nov. 2020
◇ Conducted motivational experiments to show that ensuring crash consistency when integrating NVM into GPUs is much more complicated than in the case of CPUs due to the high communication overhead between many memory controllers and the high logging overhead because of the high parallelism of GPUs
◇ Performed architectural simulations using MGPUSim and Accel-Sim to demonstrate that exploiting non-volatile write-pending-queues in memory controllers cannot be worked in GPUs, and undo logging with two-phase commit cause high overhead

Row-hammering Mitigation Architecture for High Reliable DRAM, M.S. Dissertation
Advisor: Prof. Ki-Seok Chung, Hanyang University Nov. 2018 - Nov. 2019
◇ Proposed a RowHammer mitigation method that can adaptively change the probability of additional row refreshes according to the threat level of each memory access
◇ Performed architectural simulations using DRAMSim2, SPEC CPU 2006 benchmark, and synthetically generated RowHammer attack models to demonstrate the most reliable protection with the lowest performance and energy overheads compared to two previous probabilistic schemes PARA and PRoHIT
◇ Published a paper as the first author in KICS 2019

Efficient Retention-aware Refresh Schemes for Highly Scaled-down DRAMs
Advisor: Prof. Ki-Seok Chung, Hanyang University Aug. 2018 - May. 2019
◇ Collaborative project with a senior Ph.D. student
◇ Proposed a new retention-aware refresh method that combines strong rows and weak rows refreshes into single auto-refresh command

- ◇ Performed architectural simulations using Gem5, DRAMSim2, and SPEC CPU 2006 benchmark to demonstrate performance and energy benefit over previous solutions

Foveated Rendering Technique for Virtual Reality
Advisor: Prof. Ki-Seok Chung, Hanyang University — Dec. 2018 - Jan. 2019
- ◇ Industry project, funded by LG Display
- ◇ Implemented an FPGA-based Foveated Rendering decoder using Verilog

FPGA-based CNN Accelerator, Undergraduate Dissertation
Advisor: Prof. Ki-Seok Chung, Hanyang University — Mar. 2017 - Nov. 2017
- ◇ Implemented an FPGA-based hardware accelerator for LeNet-5 using High-level Synthesis
- ◇ Source code: `github.com/changwoolee/lenet5_hls` **(Current stars: 257)**
- ◇ Published a paper as the co-first author in KICS 2017, and won an outstanding paper award

Academic Projects

Implementing Forward Operation of a Modified LeNet-5 in CUDA — Nov. 2020 - Dec. 2020
University of Illinois at Urbana-Champaign — ECE 408 (Applied Parallel Programming)
- ◇ Implemented five optimized forward-pass of convolutional layers using CUDA by exploiting methods such as shared memory, constant memory, and loop unrolling
- ◇ Performed performance analysis with GPU performance profiling tools Nsight-Systems and Nsight-Compute
- ◇ Source Code: `https://github.com/jeonghyunwoo0306/ece408PJ_Fa2020`

32-Bit 5-Stage Pipelined MIPS Processor — Apr. 2016 - Jun. 2016
Hanyang University — ENE9019 (Computer Architecture)
- ◇ Implemented a 32-bit 5-stage pipelined MIPS processor using Verilog and performed an FPGA demonstration

8-Bit LCD Password Timer — Nov. 2013 - Dec. 2013
Hanyang University — CSE2010 (Microprocessor)
- ◇ Implemented a 8-bit LCD password timer using Assembly Language

Teaching and Mentoring Experience

Teaching Assistant for *Computer Architecture*, University of British Columbia — Fall 2022, Fall 2023
- ◇ Led tutorials, implemented auto graders for assignments, and held office hours

Teaching Assistant for *VLSI Engineering*, Hanyang University — Fall 2019
- ◇ Led labs, graded exams and assignments, and held office hours

Teaching Assistant for *SoC Design*, Hanyang University — Spring 2018
- ◇ Developed lab assignments on Altera FPGA boards, led labs, and graded exams and assignments

Talks

- ◇ "Scalable and Secure Row-Swap: Efficient and Safe Row Hammer Mitigation in Memory Systems", at HPCA 2023
- ◇ "Implementation of an FPGA-based CNN Accelerator using SDSoC", at the Korean Institute of Communications and Information Sciences Fall Conference in Nov. 2017

Service

- ◇ Student Volunteer at ASPLOS 2023

Skills

Relevant Coursework
- ◇ UBC CPEN 511 Advanced Computer Architecture
- ◇ UBC CPSC 508 Graduate Operating Systems
- ◇ UIUC ECE 408 Applied Parallel Programming
- ◇ HYU ITE 4003 SoC Design
- ◇ HYU EIS 1015 Embedded System Design
- ◇ HYU ELE 3081 VLSI Engineering
- ◇ HYU ENE 9019 Computer Architecture
- ◇ HYU ELE 3021 Operating Systems
- ◇ HYU CSE 2011 Microprocessor
- ◇ HYU CSE 2010 Data Structures
- ◇ HYU ECN 1001 Digital Logic Design

Programming Languages: `C/C++, Python, Perl, CUDA, Verilog, Bash Script, Assembly Language, Go`
Simulators: `Ramulator, ChampSim, Gem5, DRAMSim2, GPGPU-Sim, MGPUSim`
Tools: `Pin, SimPoint, Xilinx Vivado, Xilinx SDSoC, Intel Quartus`