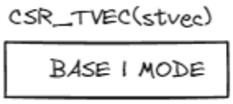
riscv 异常处理

中断模式

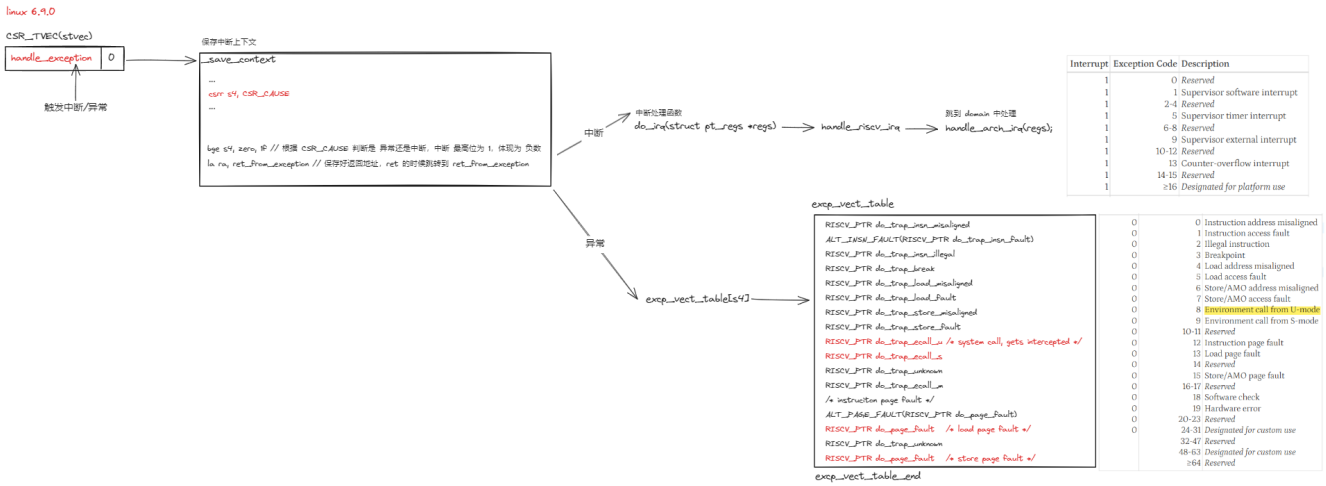


exceptions_handle==BASE

interrupts_handle==BASE + MODE * cause * 4

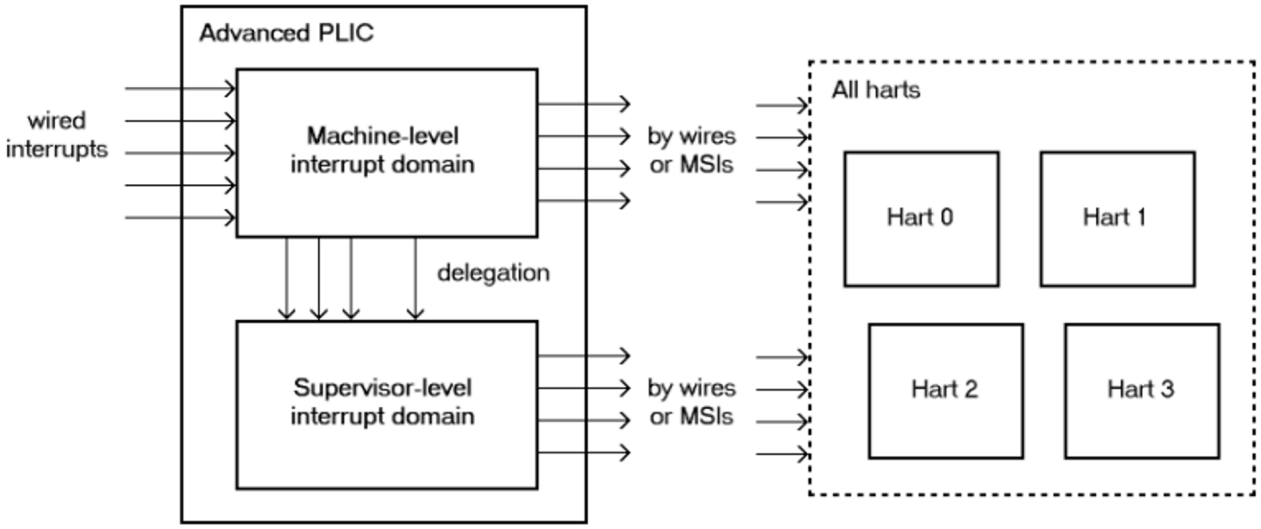
Interrupt	Exception Code	Description
1	0	*Reserved*
1	1	Supervisor software interrupt
1	2-4	*Reserved*
1	5	Supervisor timer interrupt
1	6-8	*Reserved*
1	9	Supervisor external interrupt
1	10-12	*Reserved*
1	13	Counter-overflow interrupt
1	14-15	*Reserved*
1	≥16	*Designated for platform use*

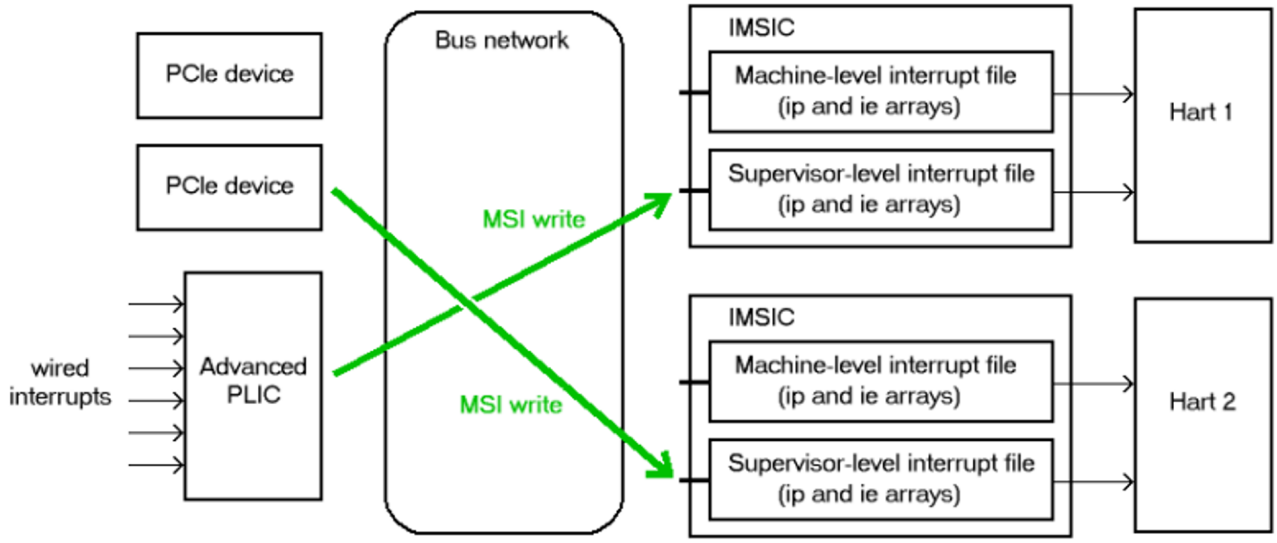
中断处理流程

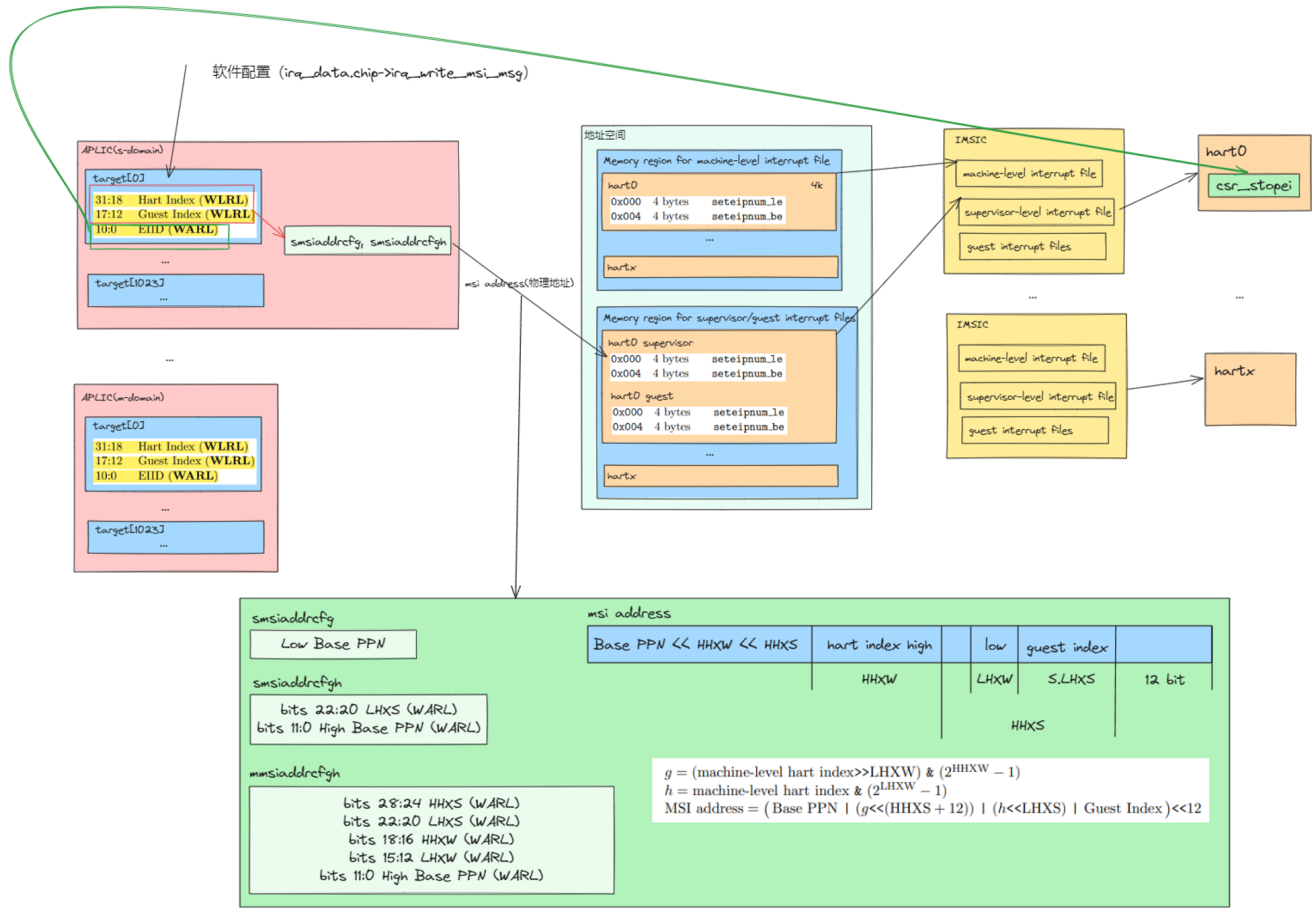



```
handle_exception
|- .Lsave_context //
        |- move a0, sp /* pt_regs */
        |- la ra, ret_from_exception // ret  ret_from_exception
        |- bge s4, zero, 1f //  CSR_CAUSE    1
        |- tail do_irq // do_irq  domain
                |- call_on_irq_stack(regs, handle_riscv_irq); //  irq_stack_ptr
                        |- riscv_intc_aia_irq
                                |- generic_handle_domain_irq(intc_domain, topi >> TOPI_IID_SHIFT); //
aia  hw irq  CSR_TOPI
                                                ...
                                                |- riscv_timer_interrupt // RV_IRQ_TIMER
                                                |- imsic_handle_irq // RV_IRQ_EXT
                                                        |- ipi_mux_process(); // ipi
                                                        |- generic_handle_domain_irq(imsic-
>base_domain, vec->hwirq); // aplic
        |- jr t0 // t0 = excp_vect_table[csr_cause]
```

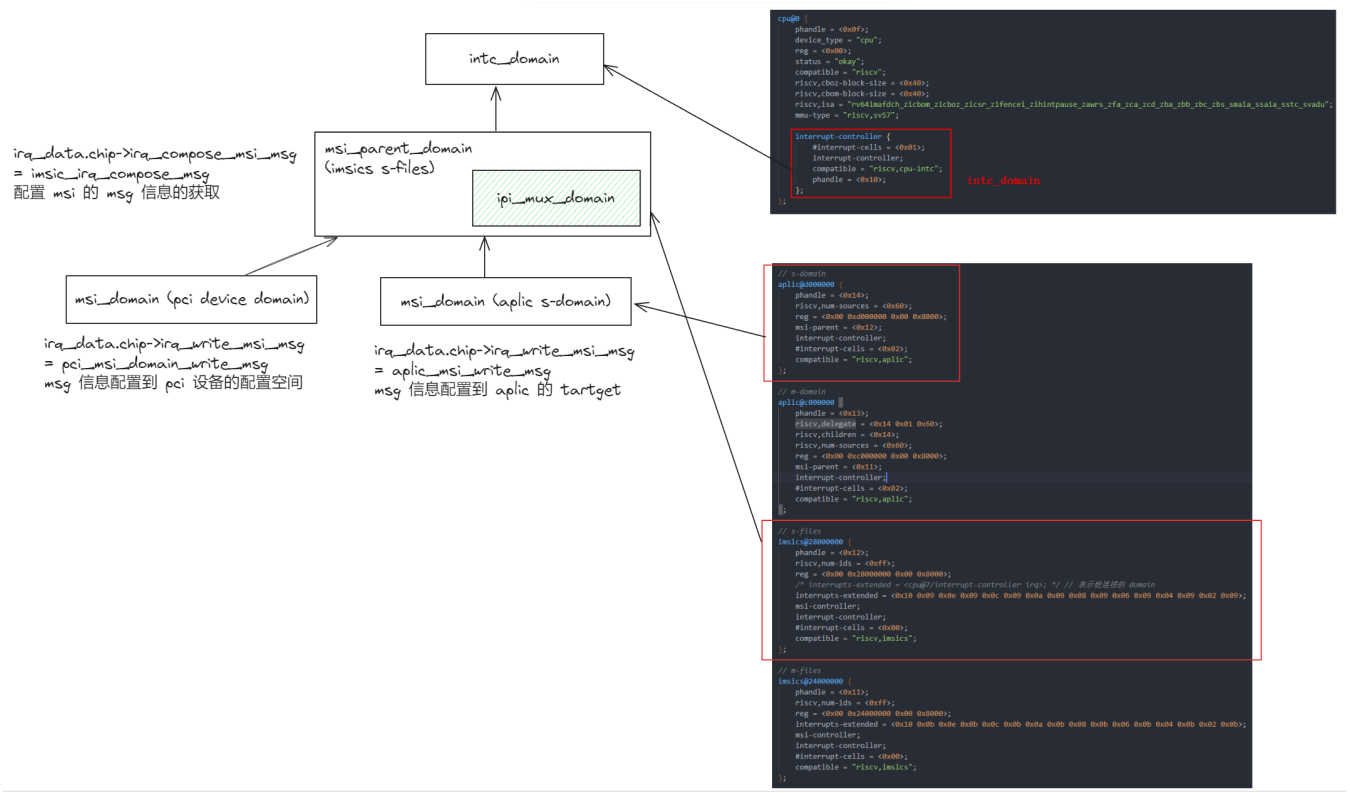
IMSIC 中断配置框架


Advanced PLIC
wired interrupts
Machine-level interrupt domain
delegation
Supervisor-level interrupt domain
by wires or MSIs
by wires or MSIs
All harts
Hart 0
Hart 1
Hart 2
Hart 3


PCIe device
PCIe device
wired interrupts
Advanced PLIC
Bus network
MSI write
MSI write
IMSIC
Machine-level interrupt file (ip and ie arrays)
Supervisor-level interrupt file (ip and ie arrays)
IMSIC
Machine-level interrupt file (ip and ie arrays)
Supervisor-level interrupt file (ip and ie arrays)
Hart 1
Hart 2



linux domain 连接关系



virq 和 target[i] 的关系