

# riscv 异常处理

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- linux domain 连接关系
- virq 和 target[i] 的关系

## 中断模式

CSR\_TVEC(stvec)

BASE | MODE

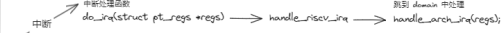
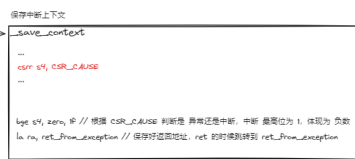
exceptions\_handle==BASE

interrupts\_handle==BASE + MODE \* cause \* 4

Interrupt	Exception Code	Description
1	0	Reserved
1	1	Supervisor software interrupt
1	2-4	Reserved
1	5	Supervisor timer interrupt
1	6-8	Reserved
1	9	Supervisor external interrupt
1	10-12	Reserved
1	13	Counter-overflow interrupt
1	14-15	Reserved
1	≥16	Designated for platform use

## 中断处理流程

linux 6.9.0



Interrupt	Exception Code	Description
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异常

excp\_vect\_table[4]

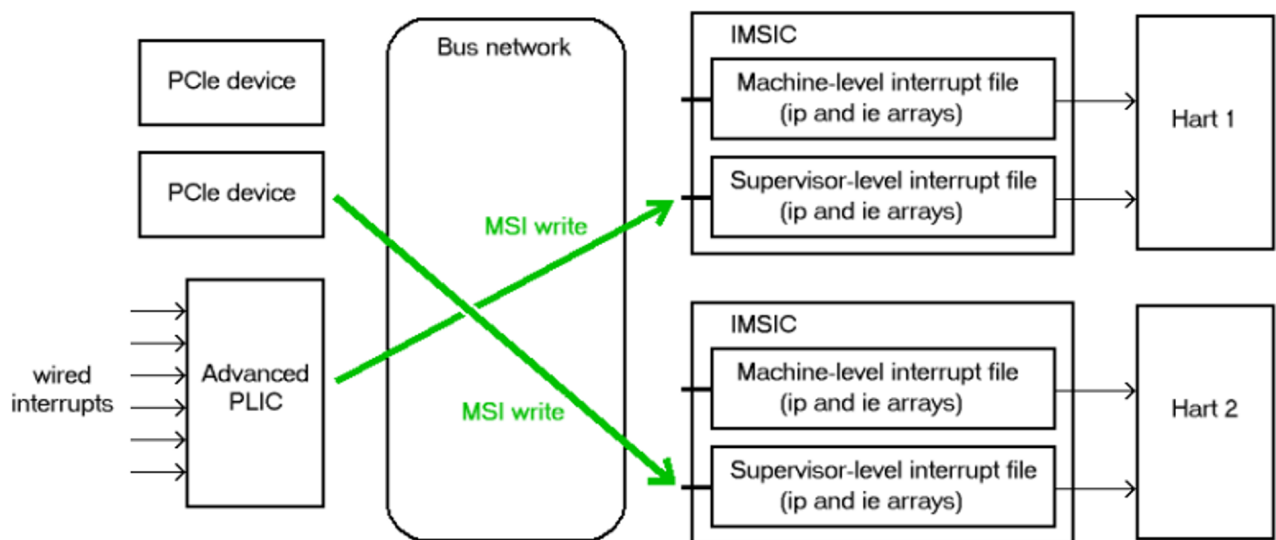
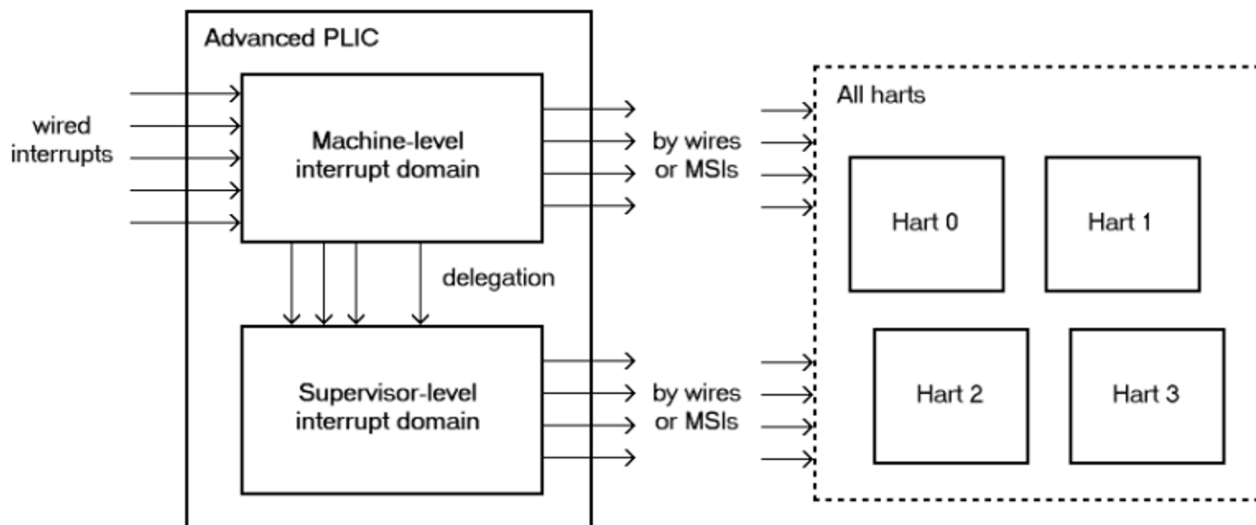
excp_vect_table	
RISCV_PTR de_trap_insn_misaligned	0
ALT_INSN_FAULT(RISCV_PTR de_trap_insn_fault)	0
RISCV_PTR de_trap_insn_illegal	0
RISCV_PTR de_trap_break	0
RISCV_PTR de_trap_load_misaligned	0
RISCV_PTR de_trap_load_fault	0
RISCV_PTR de_trap_store_misaligned	0
RISCV_PTR de_trap_store_fault	0
RISCV_PTR de_trap_ecall_u // system call gets intercepted u/	0
RISCV_PTR de_trap_ecall_s	0
RISCV_PTR de_trap_unknown	0
RISCV_PTR de_trap_ecall_m	0
/u instruction page fault u/	0
ALT_PAGE_FAULT(RISCV_PTR de_page_fault)	0
RISCV_PTR de_page_fault // load page fault u/	0
RISCV_PTR de_trap_unknown	0
RISCV_PTR de_page_fault // store page fault u/	0
excp_vect_table_end	

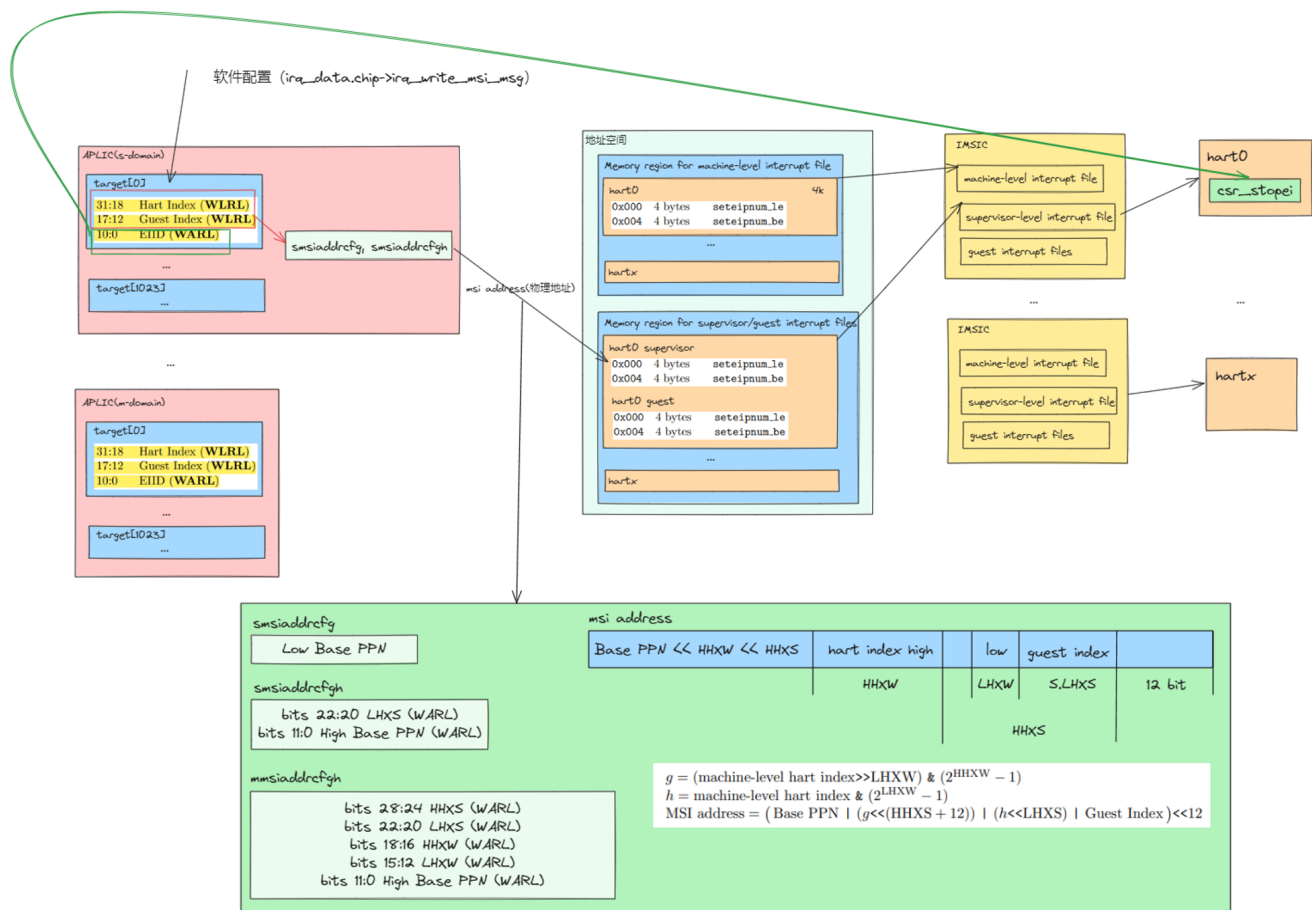
Interrupt	Exception Code	Description
0	0	Instruction address misaligned
0	1	Instruction access fault
0	2	Illegal instruction
0	3	Breakpoint
0	4	Load address misaligned
0	5	Load access fault
0	6	Store/AMO address misaligned
0	7	Store/AMO access fault
0	8	Environment call from U-mode
0	9	Environment call from S-mode
0	10-11	Reserved
0	12	Instruction page fault
0	13	Load page fault
0	14	Reserved
0	15	Store/AMO page fault
0	16-17	Reserved
0	18	Software check
0	19	Hardware error
0	20-31	Reserved
0	24-31	Designated for custom use
0	32-47	Reserved
0	48-63	Designated for custom use
0	≥64	Reserved

```
handle_exception
|- .Lsave_context //
|   |- move a0, sp /* pt_regs */
|   |- la ra, ret_from_exception // ret ret_from_exception
|   |- bge s4, zero, 1f // CSR_CAUSE 1
|   |- tail do_irq // do_irq domain
|       |- call_on_irq_stack(regs, handle_riscv_irq); // irq_stack_ptr
|       |- riscv_intc_aia_irq
|           |- generic_handle_domain_irq(intc_domain, topi >> TOPI_IID_SHIFT); //
aia hw irq CSR_TOPI

...
|- riscv_timer_interrupt // RV_IRQ_TIMER
|- imsic_handle_irq // RV_IRQ_EXT
|   |- ipi_mux_process(); // ipi
|   |- generic_handle_domain_irq(imsic-
>base_domain, vec->hwirq); // aplic
|   |- jr t0 // t0 = excp_vect_table[csr_cause]
```

## IMSIK 中断配置框架





## linux domain 连接关系



