Mengwei Si

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Education

Purdue University, West Lafayette, IN Sept 2012-present

- **Ph.D.** in School of Electrical and Computer Engineering (Expected before July 2018)
- Dissertation: "Explore Future CMOS Devices: from High Mobility Material to Steep-slope Transistor." Resulted in more than 60 journal/conference publications.
- Committee: Profs. Peide Ye, Mark Lundstrom, Joerg Appenzeller, and Zhihong Chen.

Shanghai Jiao Tong University, Shanghai, China Sept 2008-Jul 2012

- **B.S.** in Department of Electronic Science and Technology

Research Highlights

2-Dimensional Materials Based Negative Capacitance Field-effect Transistor

- Breakthroughs on sub-thermionic/non-hysteretic 2D MoS_2 NC-FETs (Published on *Nature Nanotechnology*, *IEDM*, *etc.*).
- First demonstration of p-type sub-thermionic 2D NC-FETs on WSe_2.

III-V High Mobility Compound Semiconductor MOSFET/TFET

- High performance 3D InGaAs MOSFET/TFET development (FinFET, GAA).
- Interface passivation technology for 3D InGaAs GAA MOSFETs.
- Low frequency noise/RTN characterization on III-V 3D MOSFETs/TFET.

Research Experience

***Ph.D. Research,* Purdue University**, West Lafayette, IN Sept 2012-present

- III-V high mobility transistors for high speed and low power applications.
- Steep-slope transistors: tunneling FETs, negative-capacitance FETs and novel steep-slope concepts.
- Advanced technology on device characterization and reliability.

***Undergraduate Research,* Shanghai Jiao Tong University**, Shanghai, China Sept 2009-Jul 2012

- Printed Electronics & Flex Integration Lab: Noise margin analysis and optimization for zero-V_{gs} load inverter.
- MediaSoC Lab: Development of cloud-recording based intelligent feedback system of voice information.
- UDS-SJTU Joint Research Lab for Language Technology: Development for domain-independent sentiment analysis system.

Teaching Experience

***Graduate Teaching Assistant,* Purdue University**, West Lafayette, IN

- Linear circuit analysis (ECE 201) Jan 2015-May 2015/Aug 2013-Dec 2013
- Introduction to electronic analysis and design (ECE 255) Jan 2014-May 2014

Honors and Awards

- Bilsland Dissertation Fellowship (2017)
  - Two outstanding PhD candidates are awarded in department of ECE
- Ross Fellowship (2012)
- Shanghai Scholarship (2011)
- National Scholarship (2010)

- 0.2% Chinese undergraduates are awarded
- Academic Excellence Scholarship (first-class) (Shanghai Jiao Tong University, 2010)
  - 1% undergraduate students are awarded

Conference Presentations

1. "Steep-slope MoS_2 Negative Capacitance Field-effect Transistor without Hysteresis," in *48th IEEE Semiconductor Interface Specialists Conference (SISC)*, to be presented, 2017 (**Talk**).
2. "Sub-60 mV/dec Ferroelectric HZO MoS_2 Negative Capacitance Field-effect Transistor with Internal Metal Gate: the Role of Parasitic Capacitance," in *2017 IEEE International Electron Devices Meeting (IEDM)*, to be presented, Dec 2017 (**Talk**).
3. "Black Phosphorus Field-effect Transistor with Record Drain Current Exceeding 1 A/mm," in *75th Annual Device Research Conference (DRC)*, Jun 2017 (**Talk**).
4. "Anomalous Bias Temperature Instability on Accumulation-Mode Ge and III-V MOSFETs," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, Apr 2017 (**Talk**).
5. "Random Telegraph Noise on InGaAs Tunneling Field Effect Transistor," in *47th IEEE Semiconductor Interface Specialists Conference (SISC)*, Dec 2016 (**Talk**).
6. "Interface Trap Density Extraction of Ultra-scaled MOSFETs," in *46th IEEE Semiconductor Interface Specialists Conference (SISC)*, Dec 2015 (Poster).
7. "Low Frequency Noise of near-ballistic III-V nanowire MOSFET," in *45th IEEE Semiconductor Interface Specialists Conference (SISC)*, Dec 2014 (Poster).
8. "III-V Gate-all-around Nanowire MOSFET: From 3D to 4D," in *MRS Spring Meeting*, Apr 2014 (**Talk**).
9. "Performance enhancement of gate-all-around InGaAs nanowire MOSFETs by raised source and drain structure," in *71st Annual Device Research Conference (DRC)*, Jun 2013 (**Talk**).
10. "Ultimately Scaled Sub-10 nm V-Gate InGaAs MOSFETs," in *44th IEEE Semiconductor Interface Specialists Conference (SISC)*, DeC 2013 (Poster).

Publication

Journal

1. M. Si, L. Yang, H. Zhou, and P. D. Ye, "β-Ga_2O_3 Nano-membrane Negative Capacitance Field-effect Transistor with Steep Subthreshold Slope for Wide Bandgap Logic Applications," *In Review*, 2017.
2. M. Si, W. Chung, Y. Du, and P. D. Ye, "Steep-slope Negative Capacitance WSe_2 Field-Effect Transistor," *In Review*, 2017.
3. M. Si, C.-J. Su, C. Jiang, N. J. Conrad, H. Zhou, K. Mazie, G. Qiu, C.-T. Wu, A. Shakouri, M. A. Alam, and P. D. Ye, "Steep Slope Hysteresis-free Negative Capacitance MoS_2 Transistors," ***Nat. Nanotechnol.*** *(In press)*, 2017.
4. M. Si, N. J. Conrad, S. Shin, J. Gu, J. Zhang, M. A. Alam, and P. D. Ye, "Low-Frequency Noise and Random Telegraph Noise on Near-Ballistic III-V MOSFETs," ***IEEE Trans. Electron Devices***, vol. 62, no. 11, pp. 3508–3515, 2015 (**Invited**).
5. M. Si, J. J. Gu, X. Wang, J. Shao, X. Li, M. J. Manfra, R. G. Gordon, and P. Ye, "Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 102, no. 9, p. 93505, 2013.
6. H. Tian, W. Ahn, K. Maize, M. Si, P. D. Ye, M. A. Alam, A. Shakouri and P. Bermel, "Thermoreflectance Imaging of Electromigration Evolution in Asymmetric Aluminum Constrictions," *In Review*, 2017.

7. C. Jiang, M. Si, R. Liang, J. Xu, P. D. Ye and M. A. Alam, "A Closed Form Analytical Model of Back-Gated 2D Semiconductor Negative Capacitance Field Effect Transistors," *In Review*, 2017.
8. Y. Du, G. Qiu, Y. Wang, M. Si, X. Xu, W. Wu, and P. D. Ye, "1D van der Waals Material Tellurium: Raman Spectroscopy under Strain and Magneto-transport" ***Nano Lett.***, vol. 17, no. 6, pp. 3965-3973, 2017.
9. S. Ren, M. A. Bhuiyan, J. Zhang, X. Lou, M. Si, X. Gong, R. Jiang, K. Ni, X. Wan, E. X. Zhang, R. G. Gordon, R. A. Reed, D. M. Fleetwood, P. D. Ye and T.-P. Ma, "Total Ionizing Dose (TID) Effects in GaAs MOSFETs with La-Based Epitaxial Gate Dielectrics," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 164-169, 2017.
10. S.-J. Chang, H. Zhou, N. Gong, D.-M. Kang, J.-W. Lim, M. Si, P. D. Ye, and T. P. Ma, "Fin-width Effects on Characteristics of InGaAs-Based Vertical Independent Double-Gate Transistor," ***IEEE Electron Device Lett.***, vol. 38, no. 4, pp. 441-444, 2017.
11. H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang, and P. Ye, "High-Performance Depletion/Enhancementmode β-Ga_2O_3 on Insulator (GOOI) Field-Effect Transistors With Record Drain Currents of 600/450 mA/mm," ***IEEE Electron Device Lett.***, vol. 38, no. 1, pp. 103–106, 2017.
12. H. Zhou, X. Lou, N. J. Conrad, M. Si, H. Wu, S. Alghamdi, S. Guo, R. G. Gordon, and P. Ye, "High Performance InAlN/GaN MOSHEMTs Enabled by Atomic Layer Epitaxy MgCaO as Gate Dielectric," ***IEEE Electron Device Lett.***, vol. 37, no. 5, pp. 556–559, 2016.
13. X. Li, Y. Du, M. Si, L. Yang, S. Li, T. Li, X. Xiong, P. Ye, and Y. Wu, "Mechanisms of current fluctuation in ambipolar black phosphorus field-effect transistors," *Nanoscale*, vol. 8, pp. 3572–3578, 2016.
14. H. Wu, W. Wu, M. Si, and P. Ye, "Demonstration of Ge Nanowire CMOS Devices and Circuits for Ultimate Scaling," ***IEEE Trans. Electron Devices***, vol. 63, no. 8, pp. 3049–3057, 2016.
15. H. Zhou, S. Alghmadi, M. Si, G. Qiu, and P. Ye, "Al_2O_3/β-Ga_2O_3(-201) Interface Improvement Through Piranha Pretreatment and Postdeposition Annealing," ***IEEE Electron Device Lett.***, vol. 37, no. 11, pp. 1411–1414, 2016.
16. X. Li, L. Yang, M. Si, S. Li, M. Huang, P. Ye, and Y. Wu, "Performance Potential and Limit of MoS_2 Transistors," ***Adv. Mater.***, vol. 27, no. 9, pp. 1547–1552, 2015.
17. S. Shin, M. A. Wahab, M. Masuduzzaman, K. Maize, J. Gu, M. Si, A. Shakouri, P. D. Ye, and M. A. Alam, "Direct observation of self-heating in III-V gate-all-around nanowire MOSFETs," ***IEEE Trans. Electron Devices***, vol. 62, no. 11, pp. 3516–3523, 2015.
18. J. Zhang, X. Lou, M. Si, H. Wu, J. Shao, M. J. Manfra, R. G. Gordon, and P. Ye, "Inversion-mode GaAs wave-shaped field-effect transistor on GaAs (100) substrate," *Appl. Phys. Lett.*, vol. 106, no. 7, p. 73506, 2015.
19. H. Wu, M. Si, L. Dong, J. Gu, J. Zhang, and P. D. Ye, "Germanium nMOSFETs with recessed channel and S/D: Contact, scalability, interface, and drain current exceeding 1 A/mm," ***IEEE Trans. Electron Devices***, vol. 62, no. 5, pp. 1419–1426, 2015.
20. S. Ren, M. Si, K. Ni, X. Wan, J. Chen, S. Chang, X. Sun, E. X. Zhang, R. A. Reed, D. M. Fleetwood, and others, "Total Ionizing Dose (TID) Effects in Extremely Scaled Ultra-Thin Channel Nanowire (NW) Gate-All-Around (GAA) InGaAs MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2888–2893, 2015.
21. H. Liu, A. T. Neal, M. Si, Y. Du, and P. D. Ye, "The effect of dielectric capping on few-layer phosphorene transistors: tuning the Schottky barrier heights," ***IEEE Electron Device Lett.***, vol. 35, no. 7, pp. 795–797, 2014.

22. H. Liu, M. Si, S. Najmaei, A. T. Neal, Y. Du, P. M. Ajayan, J. Lou, and P. D. Ye, "Statistical study of deep submicron dual-gated field-effect transistors on monolayer chemical vapor deposition molybdenum disulfide films," ***Nano Lett.***, vol. 13, no. 6, pp. 2640–2646, 2013.
23. H. Liu, M. Si, Y. Deng, A. T. Neal, Y. Du, S. Najmaei, P. M. Ajayan, J. Lou, and P. D. Ye, "Switching mechanism in single-layer molybdenum disulfide transistors: an insight into current flow across Schottky barriers," ***ACS Nano***, vol. 8, no. 1, pp. 1031–1038, 2013.
24. N. Conrad, S. Shin, J. Gu, M. Si, H. Wu, M. Masuduzzaman, M. Alam, P. D. Ye, and others, "Performance and Variability Studies of InGaAs Gate-all-Around Nanowire MOSFETs," *IEEE Trans. Device Mater. Reliab.*, vol. 13, no. 4, pp. 489–496, 2013.
25. Y. Du, H. Liu, A. T. Neal, M. Si, and P. D. Ye, "Molecular Doping of Multilayer Field-Effect Transistors: Reduction in Sheet and Contact Resistances," ***IEEE Electron Device Lett.***, vol. 34, no. 10, pp. 1328–1330, 2013.
26. Q. Cui, M. Si, R. A. Sporea, and X. Guo, "Simple noise margin model for optimal design of unipolar thin-film transistor logic circuits," ***IEEE Trans. Electron Devices***, vol. 60, no. 5, pp. 1782–1785, 2013.

Conference

1. M. Si, C.-J. Su, and P. Ye, "Steep-slope MoS_2 Negative Capacitance Field-effect Transistor without Hysteresis," in *48th IEEE Semiconductor Interface Specialists Conference (SISC)*, (to be presented) 2017.
2. M. Si, C. Jiang, C.-J. Su, Y.-T. Tang, L. Yang, W. Chung, M. A. Alam and P. D. Ye, "Sub-60 mV/dec Ferroelectric HZO MoS_2 Negative Capacitance Field-effect Transistor with Internal Metal Gate: the Role of Parasitic Capacitance," in ***2017 IEEE International Electron Devices Meeting (IEDM)***, p. 23.5 (to be presented), 2017.
3. M. Si, L. Yang, Y. Du, and P. D. Ye, "Black Phosphorus Field-effect Transistor with Record Drain Current Exceeding 1 A/mm," in *2017 75th Annual Device Research Conference (DRC)*, 2017.
4. M. Si, H. Wu, S. Shin, W. Luo, N. J. Conrad, W. Wu, J. Zhang, M. A. Alam, and P. D. Ye, "Anomalous Bias Temperature Instability on Accumulation-Mode Ge and III-V MOSFETs," in ***2017 IEEE International Reliability Physics Symposium (IRPS)***, 2017, p. 6A-5.
5. M. Si, C.-J. Su, and P. Ye, "Random Telegraph Noise on InGaAs Tunneling Field Effect Transistor," in *47th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2016.
6. M. Si, J. J. Gu, and P. D. Ye, "Interface Trap Density Extraction of Ultra-scaled MOSFETs," in *46th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2015.
7. M. Si, S. Shin, N. J. Conrad, J. Gu, J. Zhang, M. A. Alam, and P. D. Ye, "Characterization and reliability of III-V gate-all-around MOSFETs," in ***2015 IEEE International Reliability Physics Symposium (IRPS)***, 2015, p. 4A-1.
8. M. Si, J. J. Gu, S. Ren, E. X. Zhang, D. M. Fleetwood, S. Cui, T. P. Ma, and P. D. Ye, "Performance and Radiation Response of InGaAs Gate-all-around Nanowire MOSFETs," in *GOMACTech*, 2014.
9. M. Si, N. Conrad, J. J. Gu, J. Zhang, and P. D. Ye, "Low Frequency Noise of near-ballistic III-V nanowire MOSFET," in *45th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2014.
10. M. Si, X. Lou, X. Li, J. J. Gu, H. Wu, X. Wang, J. Zhang, R. G. Gordon, and P. D. Ye, "Performance enhancement of gate-all-around InGaAs nanowire MOSFETs by raised source and drain structure," in *2013 71st Annual Device Research Conference (DRC)*, 2013, pp. 19–20.
11. M. Si, X. Li, H. Wu, J. Zhang, H. Liu, J. J. Gu, and P. D. Ye, "Ultimately Scaled Sub-10 nm V-Gate InGaAs MOSFETs," in *44th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2013.

12. W. Chung, H. Wu, M. Si, and P. D. Ye, "Experimental extraction of Ballistic Efficiency of Germanium Nanowire NMOSFETs," in *48th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2017.
13. W. Chung, M. Si, and P. D. Ye, "Hysteresis-free Negative Capacitance Germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec," in ***2017 IEEE International Electron Devices Meeting (IEDM)***, p. 15.3, 2017.
14. L. Yang, M. Si, Q. Paduano, M. Snure, and P. D. Ye, "Asymmetric S/D contacts with BN tunneling barrier on black phosphorous FETs", *2017 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*.
15. A. Ziabari, A. Shakouri, Y. Xuan, J.-H. Bahk, Y. Koh, M. Si, P. D. Ye and A. Shakouri, "Non-Diffusive Heat Transport in Twin Nanoheater Lines On Silicon," in *IEEE ITherm 2017*, 2017.
16. H. Zhou, M. Si, S. Alghmadi, G. Qiu, L. Yang, and P. Ye, "High Performance Depletion/Enhancement-Mode β-Ga_2O_3 on Insulator (GOOI) Field-Effect Transistors with Record Drain Currents of 600/450 mA/mm," in *47th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2016.
17. W. Wu, H. Wu, M. Si, N. Conrad, Y. Zhao, and P. Ye, "RTN and low frequency noise on ultra-scaled near-ballistic Ge nanowire nMOSFETs," in ***2016 IEEE Symposium on VLSI Technology (VLSI)***, 2016, pp. 978–979.
18. L. Yang, G. Qiu, M. Si, A. R. Charnas, C. A. Milligan, D. Y. Zemlyanov, H. Zhou, Y. Du, Y. M. Lin, W. Tsai, Q. Paduano, and P. Ye, "Few-Layer Black Phosphorus PMOSFETs with BN/Al_2O_3 Bilayer Gate Dielectric: Achieving I_{on}=850uA/um,g_m=340uS/um and R_c=0.58kOhm.um," in ***2015 IEEE International Electron Devices Meeting (IEDM)***, 2016, pp. 127–130.
19. J. Zhang, M. Si, W. Wu, R. G. Gordon, and P. D. Ye, "InGaAs Bulk FinFET with Vertical Sidewalls," in *46th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2015.
20. S. Ren, J. Zhang, M. Si, K. Ni, X. Wan, J. Chen, X. Sun, E. X. Zhang, J. Chen, D. M. Fleetwood, P. D. Ye, S. Cui, and T. P. Ma, "Total Ionizing Dose Effects on GaAs MOSFETs with Epitaxial High-k Gate Dielectrics," in *46th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2015.
21. S.-J. Chang, H. Zhou, N. Gong, M. Si, P. D. Ye, and T. P. Ma, "Fin Width Effect on the Performance of InGaAs-based Independent Double-Gate Transistors," in *46th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2015.
22. W. Wu, H. Wu, J. Zhang, M. Si, Y. Zhao, J. Zhang, H. Zhou, and P. D. Ye, "Back Gate Bias induced Carrier Mobility Enhancement in Ge-on-insulator MOSFETs," in *46th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2015.
23. H. Wu, W. Wu, M. Si, and P. Ye, "First demonstration of Ge nanowire CMOS circuits: Lowest SS of 64 mV/dec, highest gmax of 1057 uS/um in Ge nFETs and highest maximum voltage gain of 54 V/V in Ge CMOS inverters," in ***2015 IEEE International Electron Devices Meeting (IEDM)***, 2015, pp. 16–19.
24. J. Zhang, M. Si, X. B. Lou, W. Wu, R. G. Gordon, and P. D. Ye, "InGaAs 3D MOSFETs with drastically different shapes formed by anisotropic wet etching," in ***2015 IEEE International Electron Devices Meeting (IEDM)***, 2015, pp. 12–15.
25. H. Wu, N. Conrad, M. Si, and P. D. Ye, "Demonstration of Ge CMOS inverter and ring oscillator with 10 nm ultra-thin channel," in *2015 73rd Annual Device Research Conference (DRC)*, 2015, pp. 281–282.
26. S. Ren, M. Si, K. Ni, S. Chang, X. Sun, E. Zhang, D. M. Fleetwood, P. Ye, S. Cui, and T.-P. Ma, "Radiation Hardness of InGaAs Nanowire Gate-All-Around MOSFETs," in *GOMACTech*, 2015.

27. S. Ren, M. Si, K. Ni, S. Chang, X. Sun, E. X. Zhang, J. Chen, D. M. Fleetwood, P. D. Ye, S. Cui, and T. P. Ma, "Radiation Hardness of InGaAs Nanowire Gate-All-Around MOSFETs," in *45th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2014.
28. H. Wu, W. Luo, M. Si, J. Zhang, H. Zhou, and P. D. Ye, "Deep sub-100 nm Ge CMOS devices on Si with the recessed S/D and channel," in ***2014 IEEE International Electron Devices Meeting (IEDM)***, 2014, pp. 16–17.
29. H. Wu, X. B. Lou, M. Si, J. Y. Zhang, R. G. Gordon, V. Tokranov, S. Oktyabrsky, and P. D. Ye, "InAs gate-all-around nanowire MOSFETs by top-down approach," in *2014 72nd Annual Device Research Conference (DRC)*, , 2014, pp. 213–214.
30. N. Conrad, M. Si, S. H. Shin, J. J. Gu, J. Zhang, M. A. Alam, and P. D. Ye, "Low-frequency noise and RTN on near-ballistic III-V GAA nanowire MOSFETs," in ***2014 IEEE International Electron Devices Meeting (IEDM)***, 2014, pp. 502–505.
31. H. Wu, M. Si, L. Dong, J. Zhang, and P. D. Ye, "Ge CMOS: Breakthroughs of nFETs (I_{max}= 714 mA/mm, g_{max}= 590 mS/mm) by recessed channel and S/D," in ***2014 IEEE Symposium on VLSI Technology (VLSI)***, 2014, pp. 978–979.
32. S. Shin, M. A. Wahab, M. Masuduzzaman, M. Si, J. Gu, P. D. Ye, M. Alam, and others, "Origin and implications of hot carrier degradation of gate-all-around nanowire III-V MOSFETs," in ***2014 IEEE International Reliability Physics Symposium***, 2014, p. 4A-3.
33. S. Khandelwal, J. P. Duarte, N. Paydavosi, Y. S. Chauhan, J. J. Gu, M. Si, P. D. Ye, and C. Hu, "InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG," in *NSTI Nanotech*, 2014.
34. J. Zhang, X. B. Lou, X. W. Wang, L. Dong, X. F. Li, N. J. Conrad, M. Si, R. G. Gordon, and P. D. Ye, "Hot Carrier Injection Study of GaAs (111)A MOSFETs with Atomic Layer Epitaxial La_2O_3 as Gate Dielectric," in *45th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2014.
35. H. Wu, M. Si, J. Zhang, H. Zhou, and P. D. Ye, "A Study on Interface and Contact Resistance," in *45th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2014.
36. H. Liu, M. Si, S. Najmaei, A. T. Neal, Y. Du, P. M. Ajayan, J. Lou, and P. D. Ye, "Dual-gate MOSFETs on monolayer CVD MoS2 films," in *2013 71st Annual Device Research Conference (DRC)*, 2013, pp. 163–164.
37. S. Ren, X. Sun, M. Si, E. X. Zhang, J. Chen, D. M. Fleetwood, P. D. Ye, S. Cui, and T. P. Ma, "Total Ionizing Dose (TID) Effects on Ultra-thin InGaAs Nanowire Gate-AllAround MOSFETs with ALD Al_2O_3 Gate Dielectrics," in *44th IEEE Semiconductor Interface Specialists Conference (SISC)*, 2013.

References

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