Instruction flow & extension from *hasHazard* to *L2Cache*

Instruction flow for *hasHazrd*: (nb=number in sequence)

- generate sequence (0, 1, 1, ….) #loop r3 = nb -2
- bubble sort (swap) #loop r7 = 4*(nb-1)
- output series (21, 13, 8, ….) #loop r7 = 4*nb

Extension from *hasHazard* to *L2Cache*:

add +1,+2,+3 number in sequence while generating FibunacciSeries

(**0**, **1**, **1**,2,3,4, **2**,3,4,5, ….)

The reason why modify version hasHazrd:

The number of sequence must large enough to see the effect of L2 Cache (size of L1 Cache =32)

the value of FibunacciSeries will out of 32bit while nb=45

Instruction flow for L2Cache:

- generate sequence #loop r3 = nb -2

增加行數 L=5*3 =15 行:

add instruction in I_mem:

```
addi r4   r4    0004
addi r8   r2    0001   (+1)
sw   r8   r4    0000
add   r30   r8   r0
jal   OutputTestPort
```

影響 jump, jal

```
jal   35+5X, X=3 / jal BubbleSort
beq $3 $0 B+5X, X=3 / beq r3, r0, FibunacciLoopExit
j 39+5X, X=3 / j BubbleInLoop
j 37+5X, X=3 / j BubbleOutLoop
j 52+5X, X=3 / j OutputSortedSeries
j 58+5X, X=3 / j Trap
```

- bubble sort #loop r7 = 4*[(nb-2)-1+(nb-2)*3]
- output series #loop r7 = 4*[(nb-2)+(nb-2)*3]

modify testoutput: store register $30 to memory xx

as large as possible, 否則會覆蓋到原本 sorting 好的數列

in I_mem

3FC(255x4) [31:0]

sw r30, r0, 0x03FC

in TestBed.v

FF(255) for TestPort[29:0]

`define TestPort 30'hFF

(check if the program go right)

generate I_mem_L2Cache & TestBed_L2Cache **for any nb** with L2Cache_generate.py

詳細請見 file ptt or jupyter notebook

20170614 TA ENDpj

特別感謝 B02901094 陳冠宇同學 協助完成教材