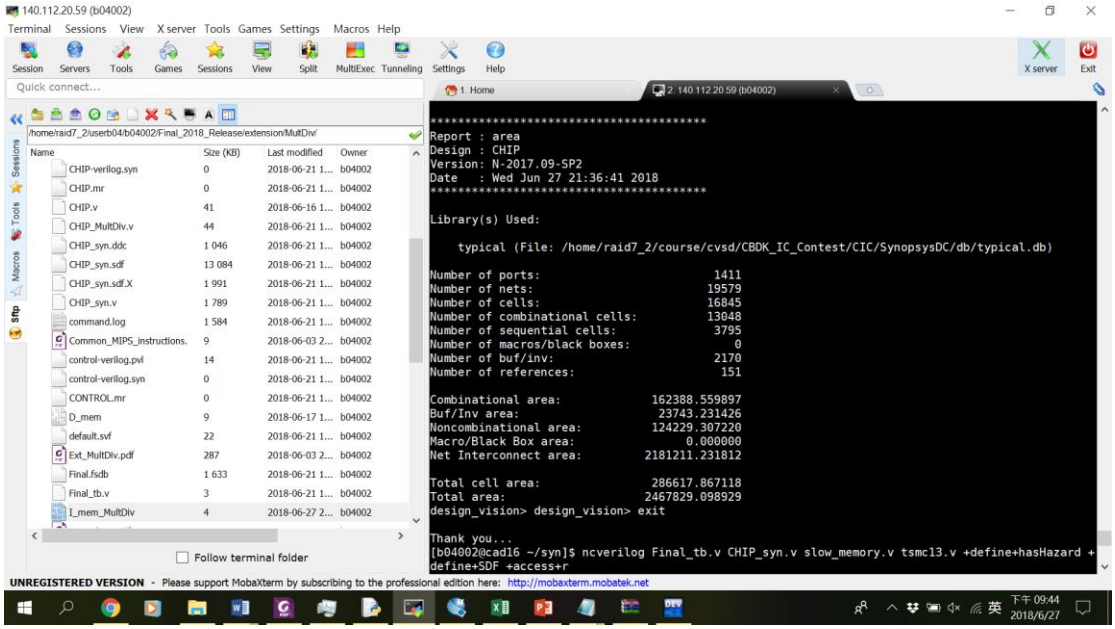
DSD Final Project Scores

1. Baseline

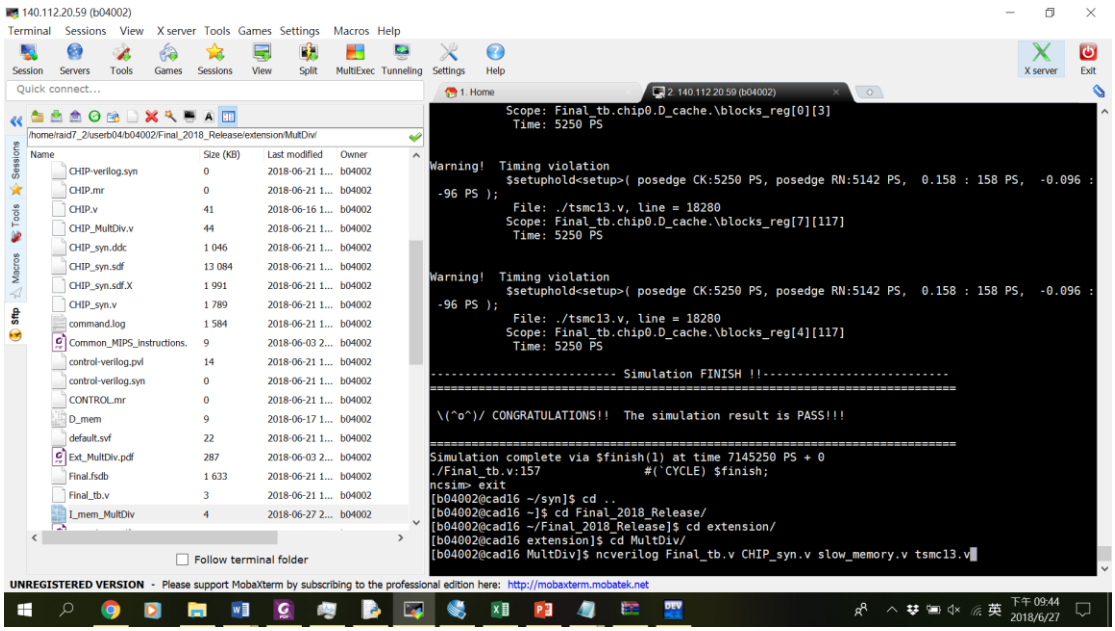
(1) Area: 286617.867118(um^2)

截圖:



(2) Total Simulation Time (hasHazard testbench):7145.25 (ns)

截圖:



(3) Area*Total Simulation Time: 2047878465 (um^2 * ns)

(4) Clock cycle for post-syn simulation: 3.5(ns)

2. BrPred

(1) Total execution cycles of I_mem_BrPred: 432

截圖:

總執行時間 1643.5ns 除以每個 cycle 時間為 3.8ns，所以共約 432 cycles

```
Warning!  Timing violation
          $setuphold<setup>( posedge CK:5700 PS, posedge RN:5564 PS,  0.156 : 1
56 PS,  -0.097 : -97 PS );
           File: ./tsmc13.v, line = 18280
          Scope: Final_tb.chip0.I_cache.\blocks_reg[0][54]
           Time: 5700 PS


Warning!  Timing violation
          $setuphold<setup>( posedge CK:5700 PS, posedge RN:5564 PS,  0.156 : 1
56 PS,  -0.097 : -97 PS );
           File: ./tsmc13.v, line = 18280
          Scope: Final_tb.chip0.I_cache.\blocks_reg[0][48]
           Time: 5700 PS

================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 1643500 PS + 0
./Final_tb.v:157              #(`CYCLE) $finish;
ncsim> exit
[b04111@cad29 ~/a1b2c3]$
```

(2) Total execution cycles of I_mem_hasHazard: 2006

截圖:

總執行時間 7624.7ns 除以每個 cycle 時間為 3.8ns，所以共約 2006 cycles

```
Data:         5     ans:         5

Data:         3     ans:         3

Data:         2     ans:         2

Data:         1     ans:         1

Data:         1     ans:         1

Data:         0     ans:         0

Data:      3421     ans:      3421

------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 7624700 PS + 0
./Final_tb.v:157              #(`CYCLE) $finish;
ncsim> exit
[b04111@cad29 ~/a1b2c3]$
```

(3) Synthesis area of BPU(Total area of BrPred minus baseline design, two design clock cycle need to be same):2697.16883 (um^2)

(4) Clock cycle for post-syn simulation: 3.8(ns)

我們有嘗試用 3.5ns 去執行，會出現 congratulation，但 reset 之後也會有 violation，不知道這樣可不可以，保險起見我們最後還是用沒有 violation 的 3.8ns 去跑，此外，有嘗試調整合成時的 clock cycle，但不管怎麼調低，3.5ns 就都不會過，因此最後仍然維持這個版本。

截圖:

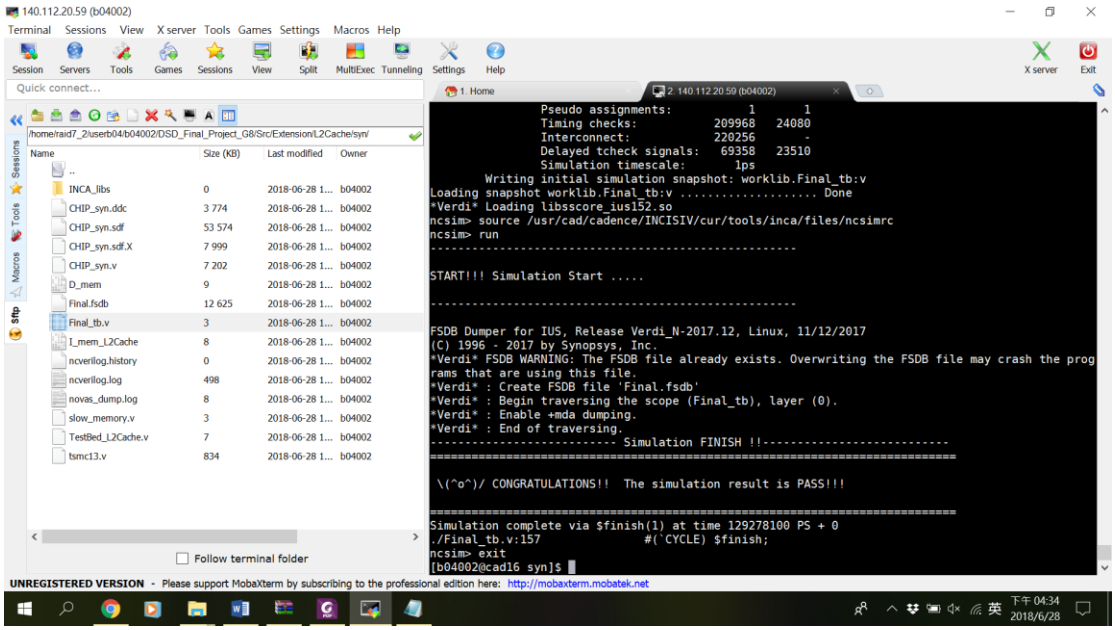
```
// this is a test bench feeds initial instruction and data
// the processor output is not verified

`timescale 1 ns/10 ps

`define CYCLE 3.8 // You can modify your clock frequency

`define DMEM_INIT "D_mem"
`define SDFFILE    "./CHIP_syn.sdf"      // Modify your SDF file name

// For different condition (I_mem, TestBed)
`ifdef noHazard
    `define IMEM_INIT "I_mem_noHazard"
    `include "./TestBed_noHazard.v"
`endif
`ifdef hasHazard
        `define IMEM_INIT "I_mem_hasHazard"
        `include "./TestBed_hasHazard.v"
`endif
`ifdef BrPred
        `define IMEM_INIT "I_mem_BrPred"
        `include "./TestBed_BrPred.v"
`endif
`ifdef L2Cache
        `define IMEM_INIT "I_mem_L2Cache"
        `include "./TestBed_L2Cache.v"
`endif
`ifdef Assembly
        `define IMEM_INIT "I_mem_Assembly"
        `include "./TestBed_Assembly.v"
`endif
`ifdef MultDiv
```

3. L2Cache

(1) Avg. memory access time:7.85 (ns)

(2) Total execution time: 129278.1(ns)

截圖:

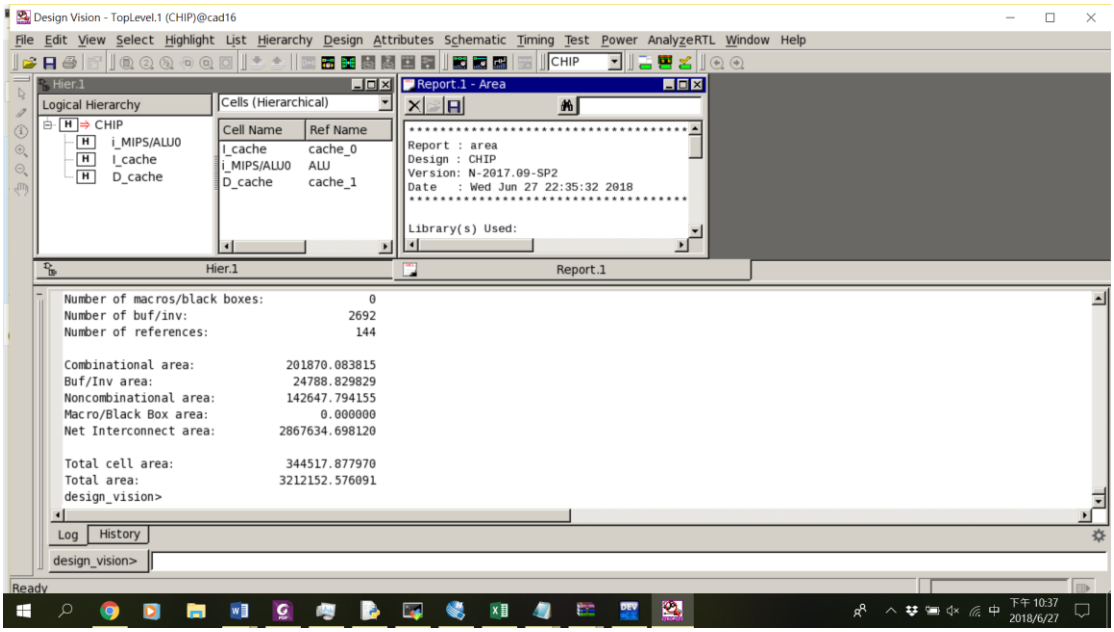


(3) Clock cycle for post-syn simulation: 4.2 (ns)

4. MultDiv

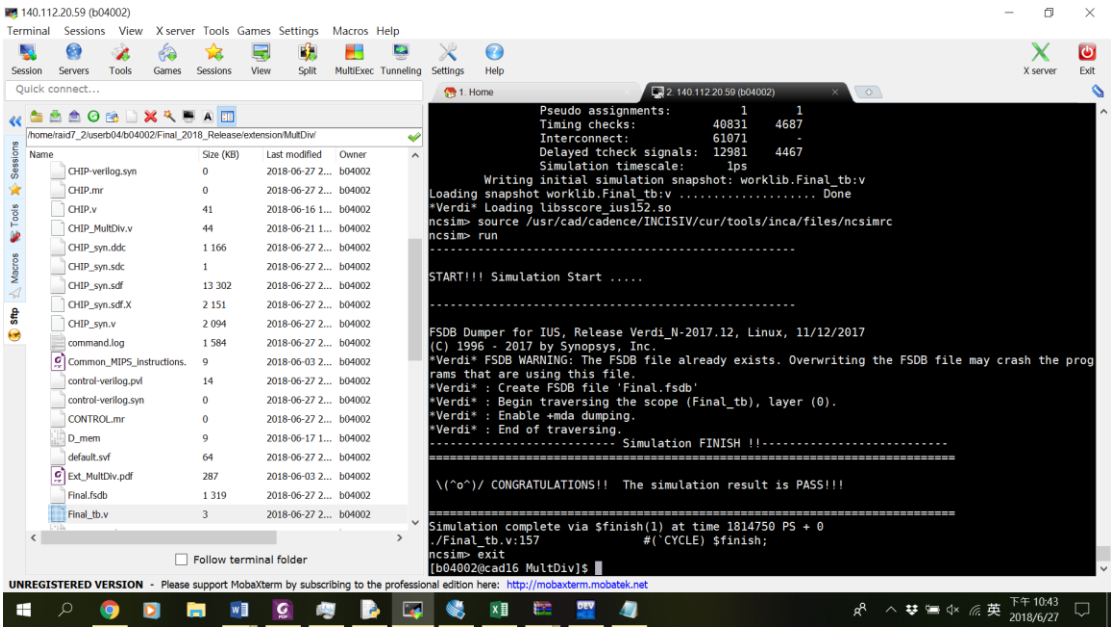
(1) Total synthesis area: 344517.879(um^2)

截圖:



(2) Total execution time: 1814.75(ns)

截圖:



(3) Minimum clock period: 3.5(ns)

截圖:


Final_tb - 記事本
檔案(F) 編輯(E) 格式(O) 檢視(V) 說明(H)
// this is a test bench feeds initial instruction and data
// the processor output is not verified
`timescale 1 ns/10 ps
`define CYCLE 3.5 // You can modify your clock frequency
`define DMEM_INIT "D_mem"
`define SDFFILE "./CHIP_syn.sdf" // Modify your SDF file name
// For different condition (I_mem, TestBed)
`ifdef noHazard
`define IMEM_INIT "I_mem_noHazard"
`include "./TestBed_noHazard.v"
`endif
`ifdef hasHazard
`define IMEM_INIT "I_mem_hasHazard"
`include "./TestBed_hasHazard.v"
`endif
`ifdef BrPred
`define IMEM_INIT "I_mem_BrPred"
`include "./TestBed_BrPred.v"
`endif
`ifdef L2Cache
`define IMEM_INIT "I_mem_L2Cache"
`include "./TestBed_L2Cache.v"
`endif
`ifdef Assembly
`define IMEM_INIT "I_mem_Assembly"
`include "./TestBed_Assembly.v"
`endif
`ifdef MultDiv
`define IMEM_INIT "I_mem_MultDiv"
`include "./TestBed_MultDiv.v"
`endif
module Final_tb;
reg clk;
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2018/6/27