Jason Yuchi Tsao

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Portfolio: https://j7tsao.github.io/portfolio | Github: https://github.com/j7tsao

Objective

- Self-taught learner looking to switch to a full time job working as a software engineer.

Technical Skills

Programming Languages: Python, JavaScript, HTML5/CSS3, C++, MySQL, bash **OS:** Linux/Unix, MS Windows

Certificate/Projects (Hyperlink)

- freeCodeCamp Scientific Computing with Python Oct. 2021
- freeCodeCamp Responsive Web Design Sep. 2020
- freeCodeCamp JavaScript Algorithms and Data Structure Oct. 2020
- freeCodeCamp Front End Development Libraries Jan. 2021
- Travel Agency Administration System using C++ Dec. 2021
- Portfolio Webpage (HTML5 / CSS3 / JavaScript) Mar. 2022

Work Experience

Qualcomm Technologies **San Diego, CA**
EngIT Engineer (Consultant) **Feb 2021 – Present**

- Verified Engineering flow (NBF) through Cloud provisioning (AWS EC2)
- Refurbished automation script (bash, Python) for Amazon Machine Images (AMI)
- Cross-site infrastructure provisioning for Qualcomm Vendor Remote Access & Debug (QVRAD)

ASIC Implementation Engineer **2012 – June 2018**

- ASIC implementation for Snapdragon GPU cores: Gandalf, Elessar, Istari, Nazgul, Napali, Poipu, Hana, Kona
- Formal Verification (Cadence Conformal LEC), Physical Aware Synthesis (Synopsys Design Compiler Graphical)
- Static Timing Analysis (STA), fixing setup violation (Synopsys DCG/Prime Time)
- Owner of the 2nd biggest hard macro in GPU core (Texture Pipe, TP Wrapper, 5.1 Million gates, 3X TP)

Illinois Institute of Technology **Chicago, IL**
Research Assistant **2007 – 2011**

- Area-efficient VLSI implementation for parallel linear-phase digital FIR filter of even and odd length
- VLSI pipeline system (Multimedia processor) power reduction for via single comparator-based clock gating

Teaching Assistant **2007 – 2011**

- ECE212: Circuit Analysis
- ECE429: Introduction to VLSI Design

ProMOS Technologies **Hsinchu, Taiwan**
Wafer Sort Engineer **2003 – 2005**

- Wafer testing troubleshooting and wafer prober maintenance in fab
- Die testing data analysis and wafer yield improvement

Education

Illinois Institute of Technology **Chicago, IL**
Ph.D. Electrical Engineering (GPA: 3.51 / 4.0) **Dec 2011**

- PhD Dissertation Title**:**
  Hardware-Efficient VLSI Implementation for Parallel Linear-Phase Digital FIR Filter

New York University Tandon School of Engineering **New York, NY**
M.S. Electrical Engineering (GPA: 3.75 / 4.0) **Jun 2007**

Dayeh University **Changhua, Taiwan**
B.S. Electrical Engineering **Jun 2001**

Awards

Qualstar (Qualcomm Recognition & Reward Program for Outstanding Contributions)

- 2015 – Extra efforts and dedication to incorporate very challenging last minute USP changes for successful Istari V3.0 TO.
- 2017 – Dedication to deliver the highest quality netlist as a GPU hard macro owner for Hana/Poipu V1.