Jason Yuchi Tsao

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Portfolio: https://j7tsao.github.io/portfolio | GitHub: https://github.com/j7tsao

Objective

- Looking for a full time job as a software engineer.

Technical Skills

Python, JavaScript, HTML5, CSS3, C++, bash, GIT, Django, React JS, SQL, Selenium, Linux/Unix, MS Windows

Projects / Certificate

- Project of Fortune Teller using Python [GitHub]
- Project of Travel Agency Administration System using C++ [GitHub]
- Portfolio Webpage (HTML5 / CSS3 / JavaScript) [Link|GitHub]
- freeCodeCamp Scientific Computing with Python Certification [Link] –
  Projects: Arithmetic Formatter, Time Calculator, Budget App, Polygon Area Calculator, Probability Calculator
- freeCodeCamp Responsive Web Design Certification [Link] –
  Projects: Survey Form, Tribute Page, Documentation Page, Product Landing Page, Personal Page
- freeCodeCamp Front End Development Libraries using React JS Certification [Link] –
  Projects: Random Quote Machine, Markdown Previewer, Drum Machine, Calculator, 25 + 5 Clock
- freeCodeCamp JavaScript Algorithms and Data Structure Certification [Link]

Work Experience

Qualcomm Technologies — **San Diego, CA**
EngIT Engineer (Consultant) — **2021 – 05.2022**

- Verified Engineering flow (NBF) through Cloud provisioning (AWS EC2)
- Scripting (bash, Python) for Amazon Machine Images (AMI) automation
- Cross-site infrastructure provisioning for Qualcomm Vendor Remote Access & Debug (QVRAD)

Self-Employed (E-Commerce, Realtor) — **2019 – 2020**

Qualcomm Technologies — **San Diego, CA**
ASIC Implementation Engineer — **2012 – 2018**

- ASIC implementation for Snapdragon GPU cores: Gandalf, Elessar, Istari, Nazgul, Napali, Poipu, Hana, Kona
- Formal Verification (Cadence Conformal LEC), Physical Aware Synthesis (Synopsys Design Compiler Graphical)
- Static Timing Analysis (STA), fixing setup violation (Synopsys DCG/Prime Time)
- Owner of the 2nd biggest hard macro in GPU core (Texture Pipe, TP Wrapper, 5.1 Million gates, 3X TP)

Illinois Institute of Technology — **Chicago, IL**
Research Assistant — **2007 – 2011**

- Area-efficient VLSI implementation for parallel linear-phase digital FIR filter of even and odd length
- VLSI pipeline system (Multimedia processor) power reduction for via single comparator-based clock gating

Teaching Assistant — **2007 – 2011**

- ECE212: Circuit Analysis
- ECE429: Introduction to VLSI Design

ProMOS Technologies — **Hsinchu, Taiwan**
Wafer Sort Engineer — **2003 – 2005**

- Wafer testing troubleshooting and wafer prober maintenance in fab
- Die testing data analysis and yield improvement

Education

Illinois Institute of Technology — **Chicago, IL**
Ph.D. Electrical Engineering (GPA: 3.51 / 4.0) — **Dec 2011**

- PhD Dissertation Title**:**
  Hardware-Efficient VLSI Implementation for Parallel Linear-Phase Digital FIR Filter

New York University Tandon School of Engineering — **New York, NY**
M.S. Electrical Engineering (GPA: 3.75 / 4.0) — **Jun 2007**

Dayeh University — **Changhua, Taiwan**
B.S. Electrical Engineering — **Jun 2001**

Awards

Qualstar (Qualcomm Recognition & Reward Program for Outstanding Contributions)

- 2015 – Extra efforts and dedication to incorporate very challenging last minute USP changes for successful Istari V3.0 TO.
- 2017 – Dedication to deliver the highest quality netlist as a GPU hard macro owner for Hana/Poipu V1.