------ LAB 4 -----

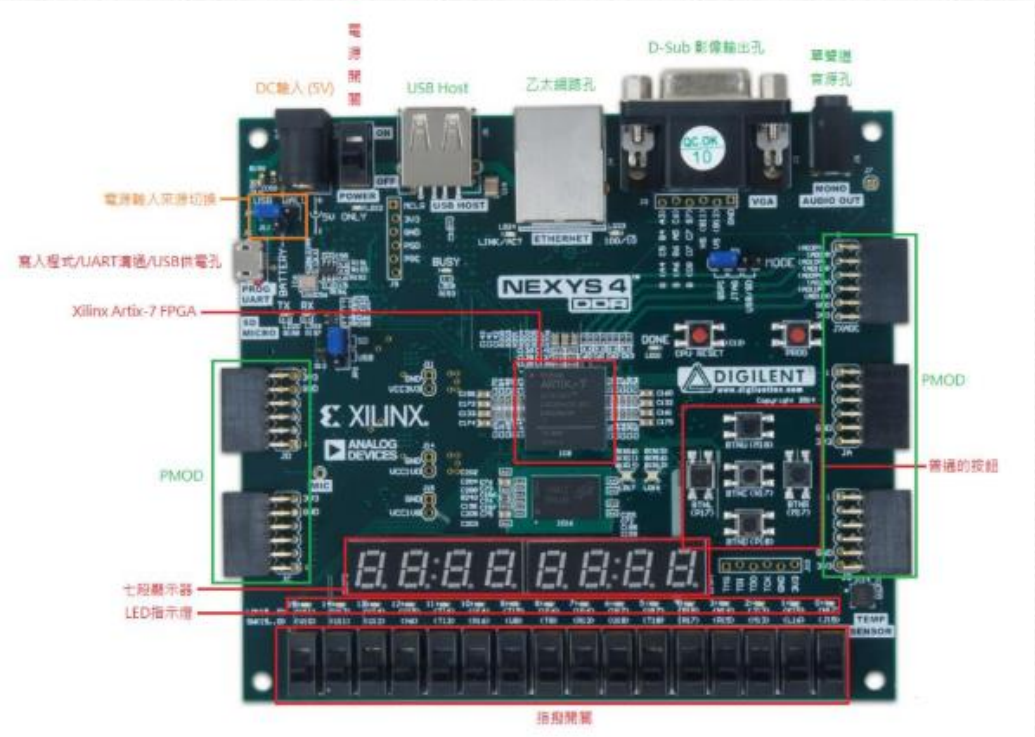
FPGA Implementation (Nexys4)

洪銘佑

2018/11/28

實驗工具

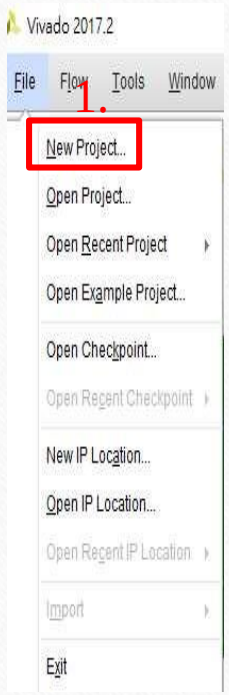
- Nexys 4 DDR FPGA
- Vivado

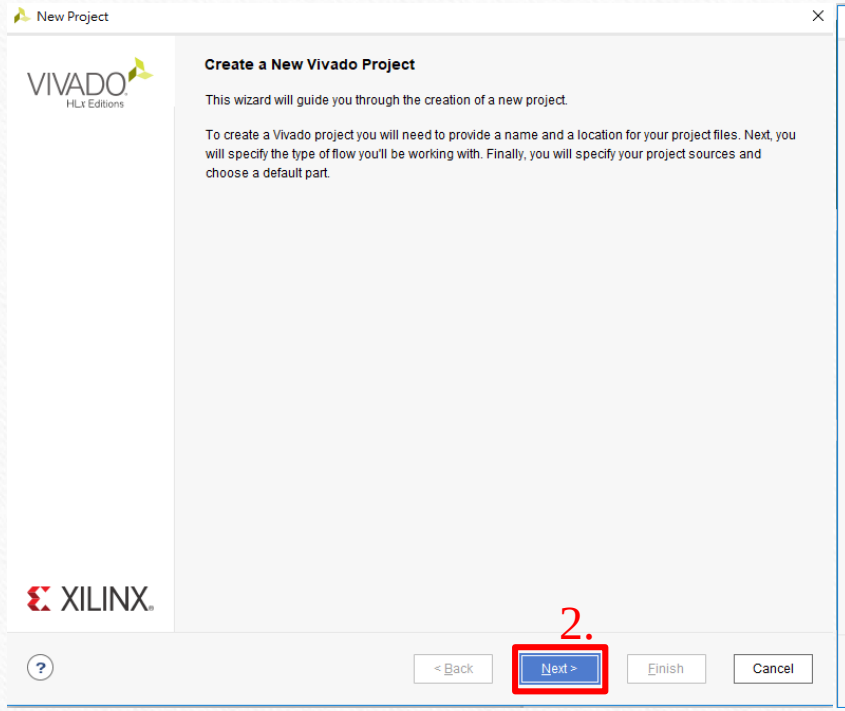


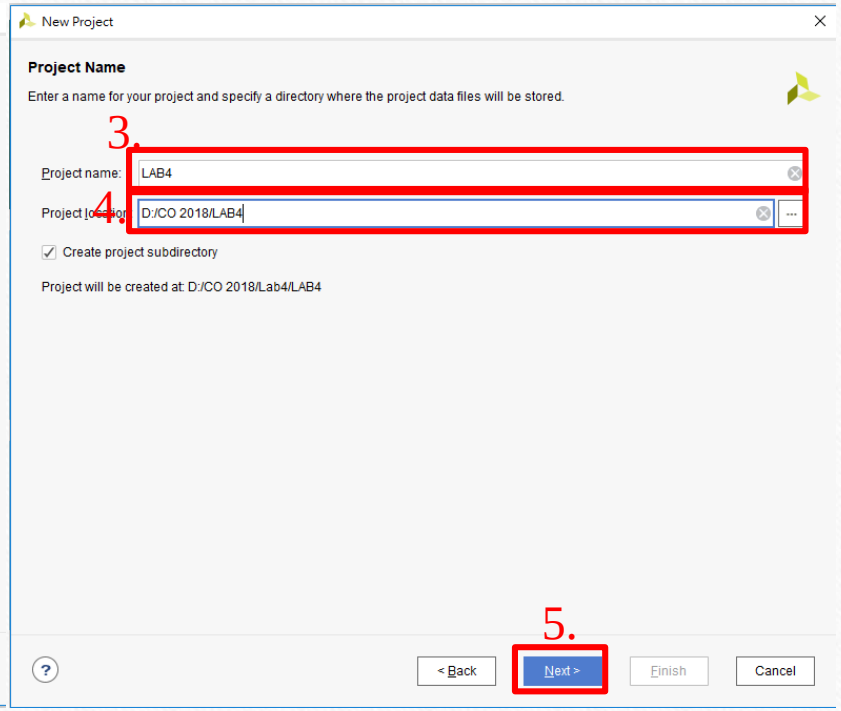
Nexys-4 DDR FPGA 開發板

- 請同學愛惜使用
- 本堂課程結束前請填寫財產借用單

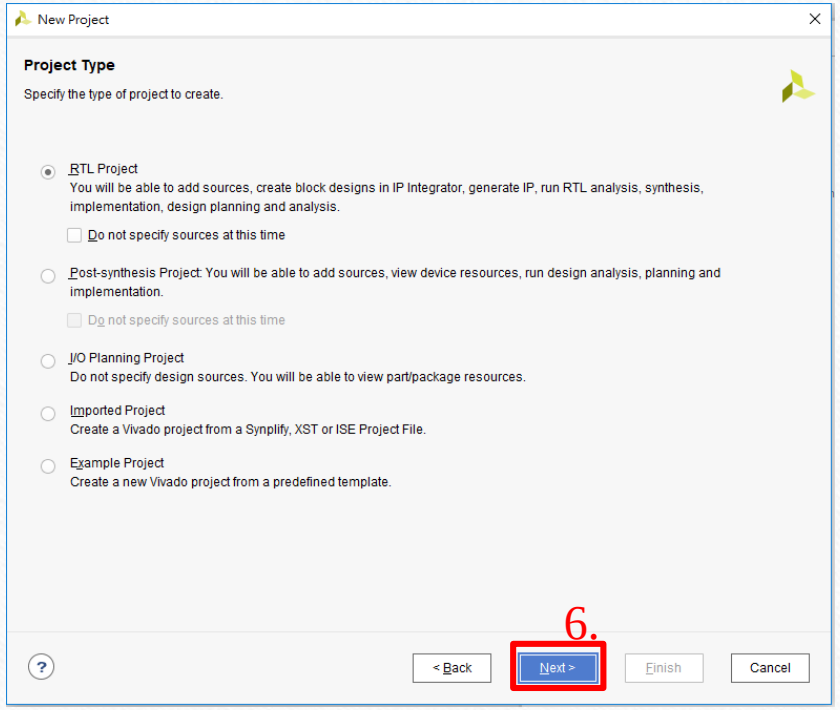
Vivado教學-開新專案

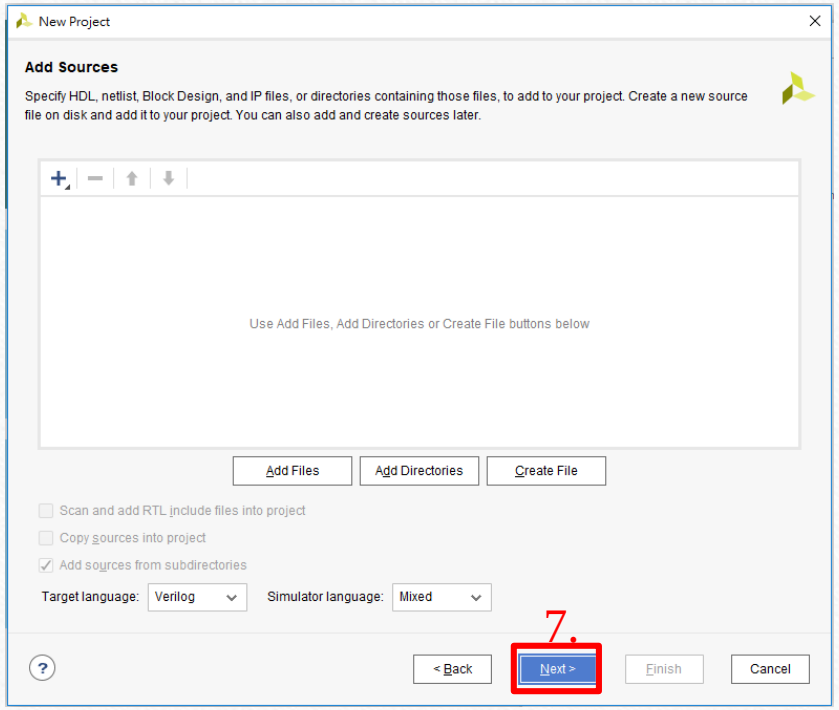




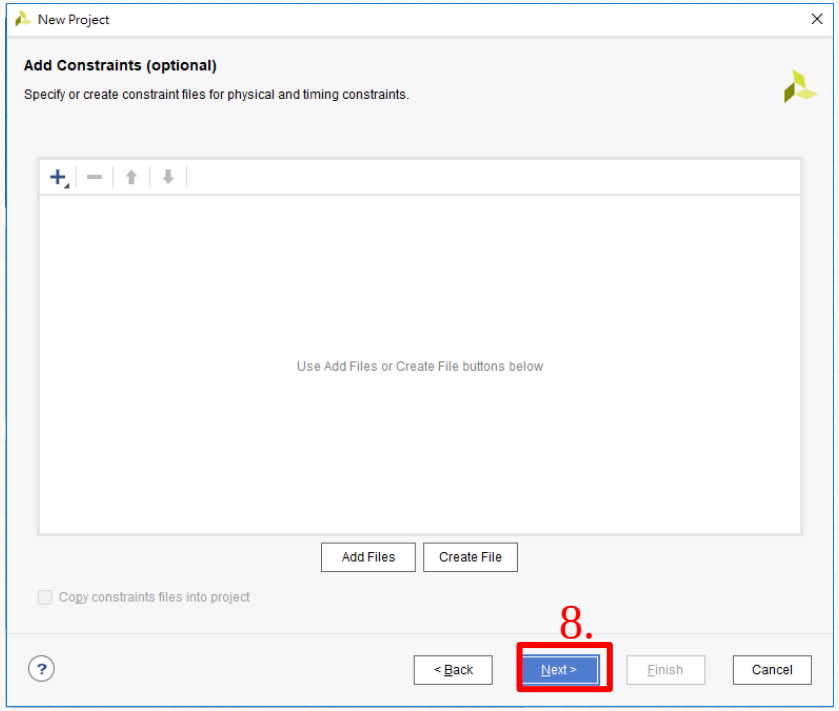


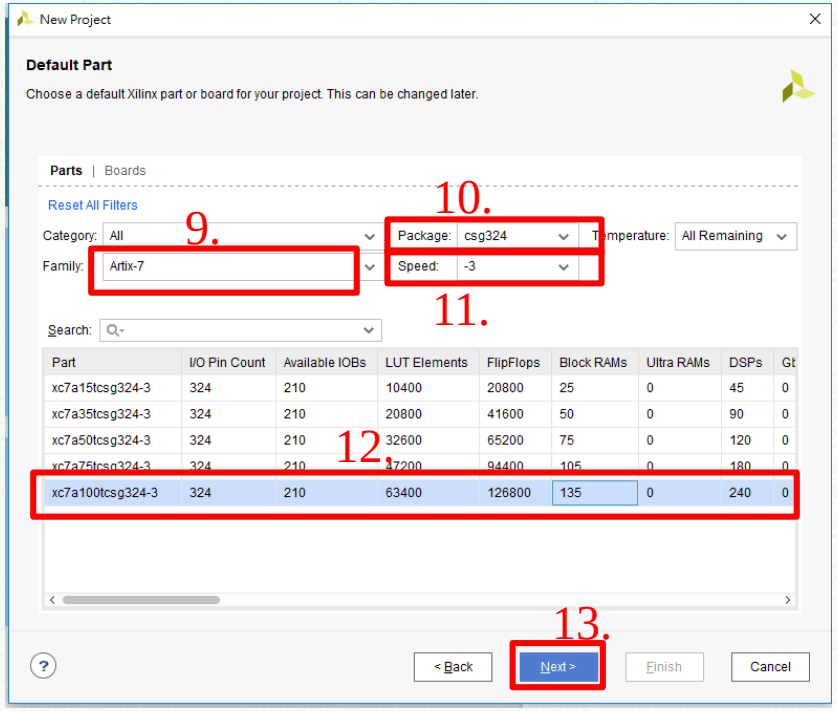
Vivado教學-開新專案



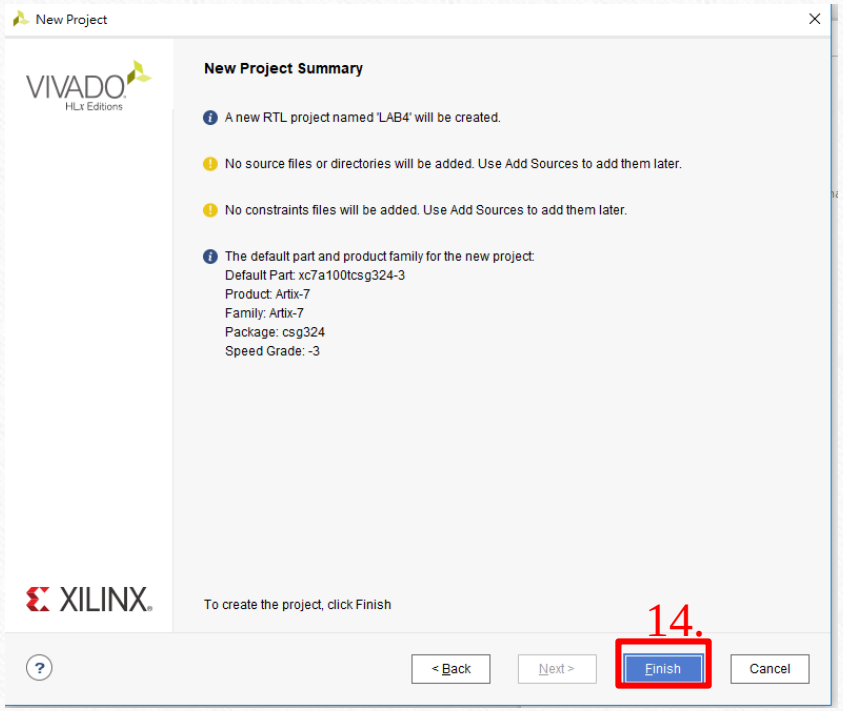


Vivado教學-開新專案





Vivado教學-開新專案

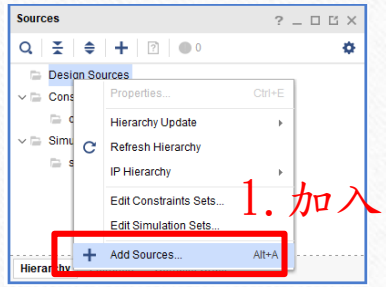


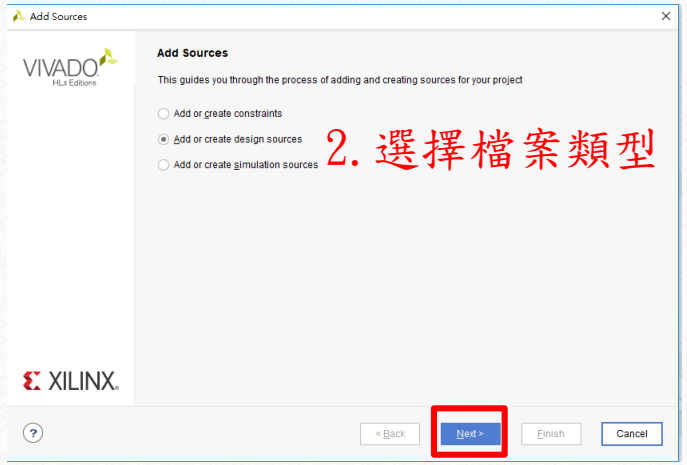
Vivado教學-創建專案原始檔

- 按右鍵新增檔案
- 選擇檔案類型：

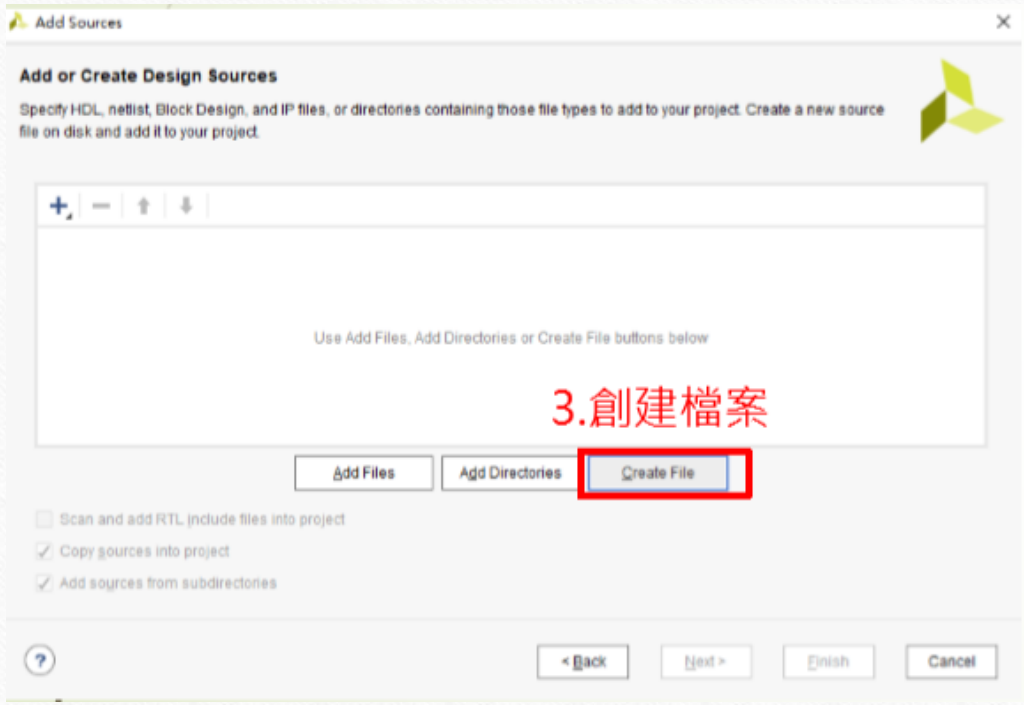
  constraints 可以新增.xdc檔

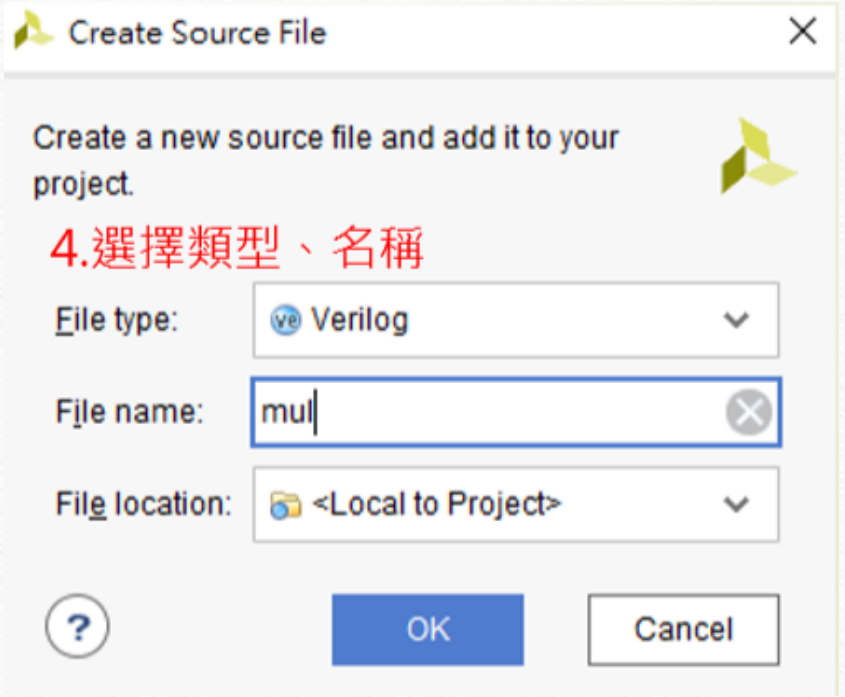
  design sources 可以新增.v檔
- .xdc用來描述.
- v與實體線路的連接關係
- .v用來描述硬體行為
- 也可以從現有檔案匯



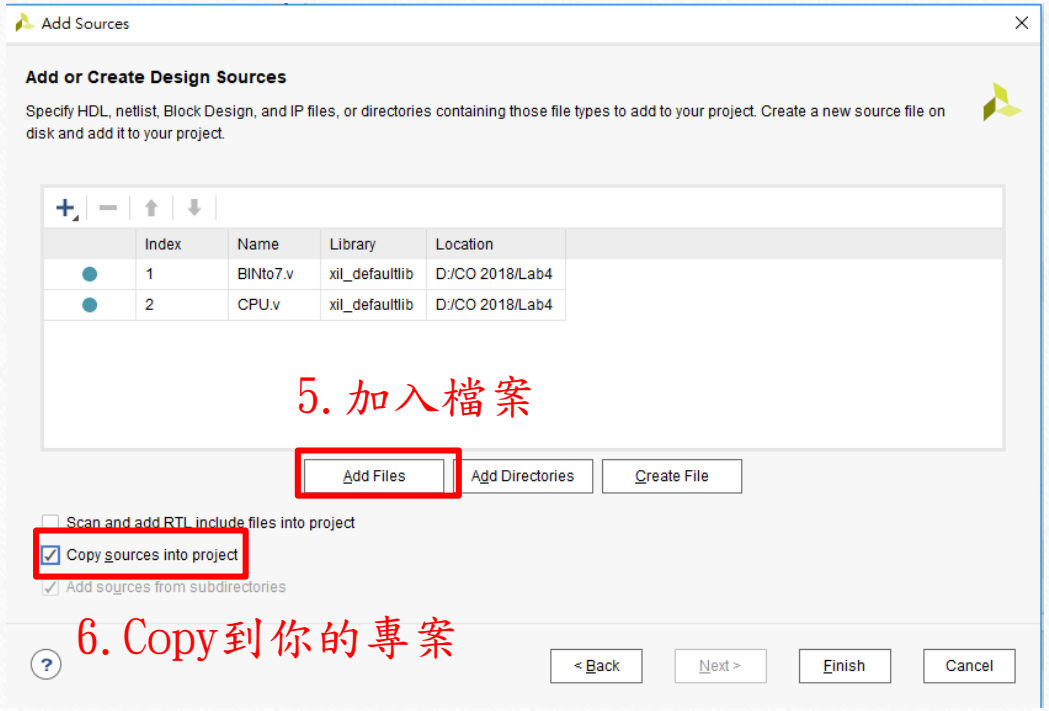


Vivado教學-創建專案原始檔

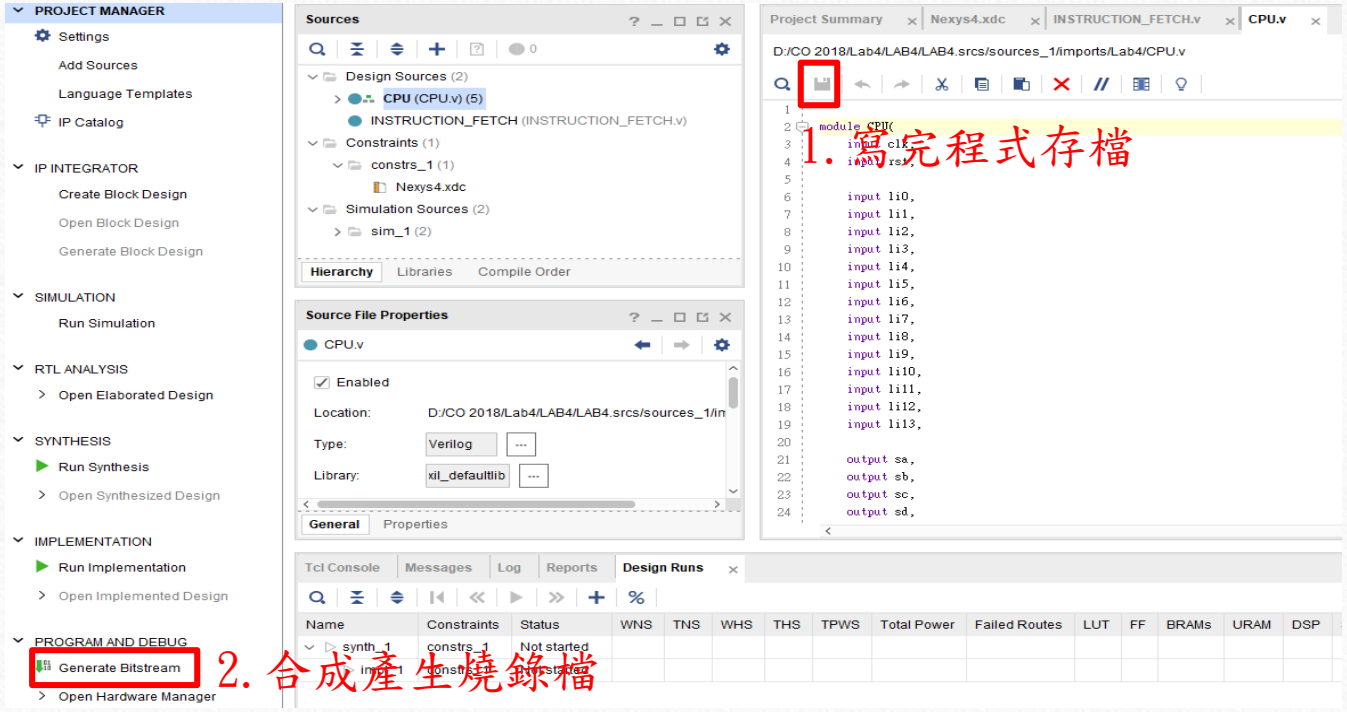




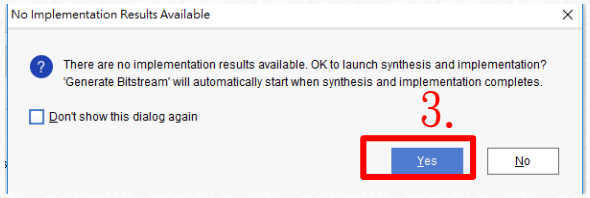
Vivado教學-加入專案原始檔

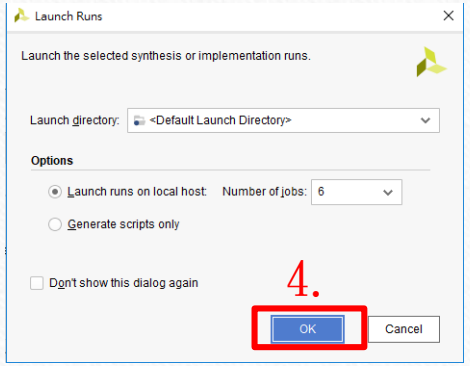


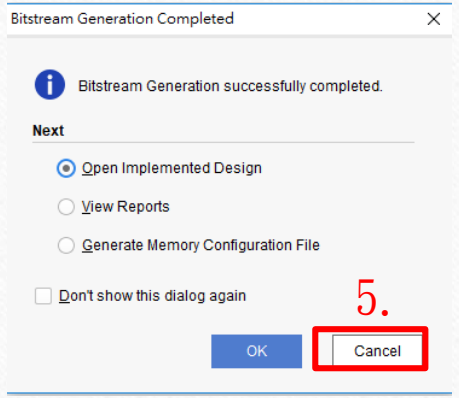
Vivado教學-將程式寫入FPGA板

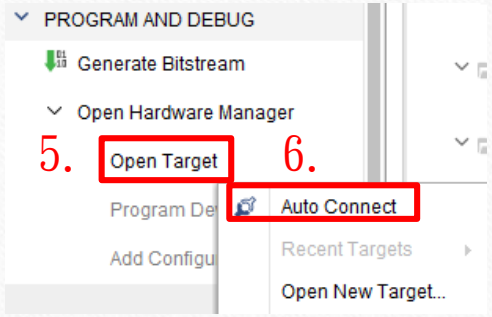


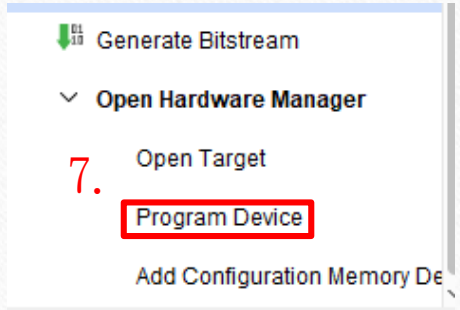
Vivado教學-將程式寫入FPGA板

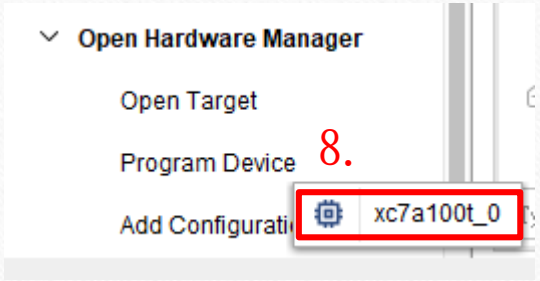




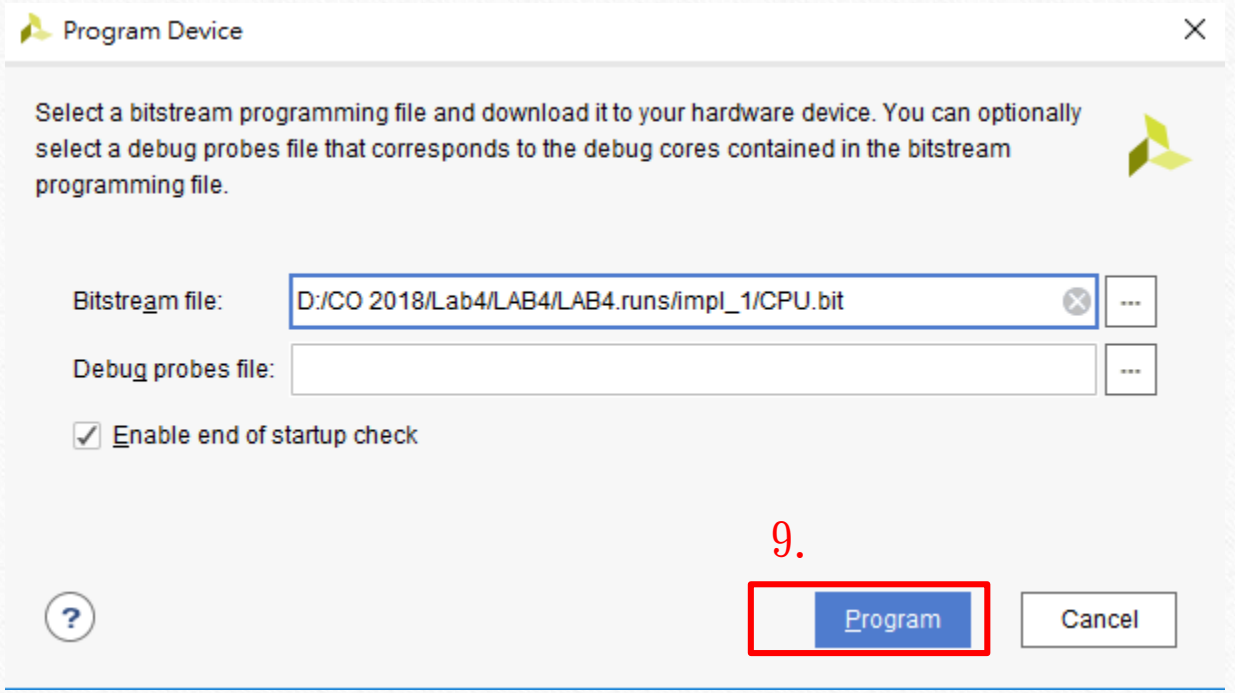








Vivado教學-將程式寫入FPGA板



課堂練習

- 將實驗壓縮包裡面的CO_lab4example其中的專案寫入到 Nexys4中，並了解其運作
- 修改 “top.v” 及 “Nexy4.xdc”，新增2個指撥按鈕使其能運算加 法、乘法以及減法
- 向助教Demo結果
- 佔Lab4成績30

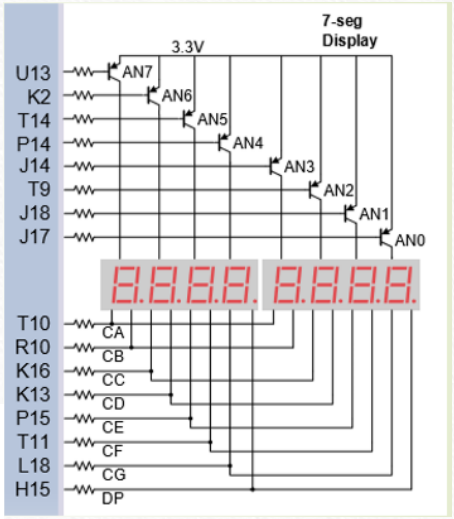
作業驗收說明

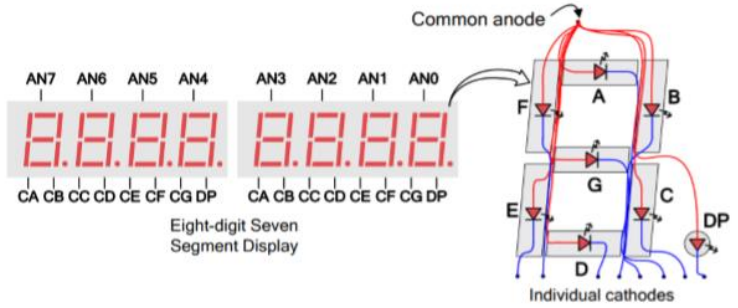
- 把作業三完成的CPU及求最相近的兩個質數寫入Nexys4 需要包含：
  - 13個指撥作為輸入值(sw0~sw12)
  - 運算結果分別以前、後4個七段顯示器顯示
  - 使用reset重新計算新值
  - 說明文件(PDF)、CPU及求最相近兩個質數的專案

  ※說明文件需包含：程式說明、如何控制顯示器
- 正確運算(50%)
- 能正確運算且.bit檔檔案大小排序最小的二十個人(20%)
- 作業驗收時間為12/12(三) 以前上傳

Nexys4的七段顯示器

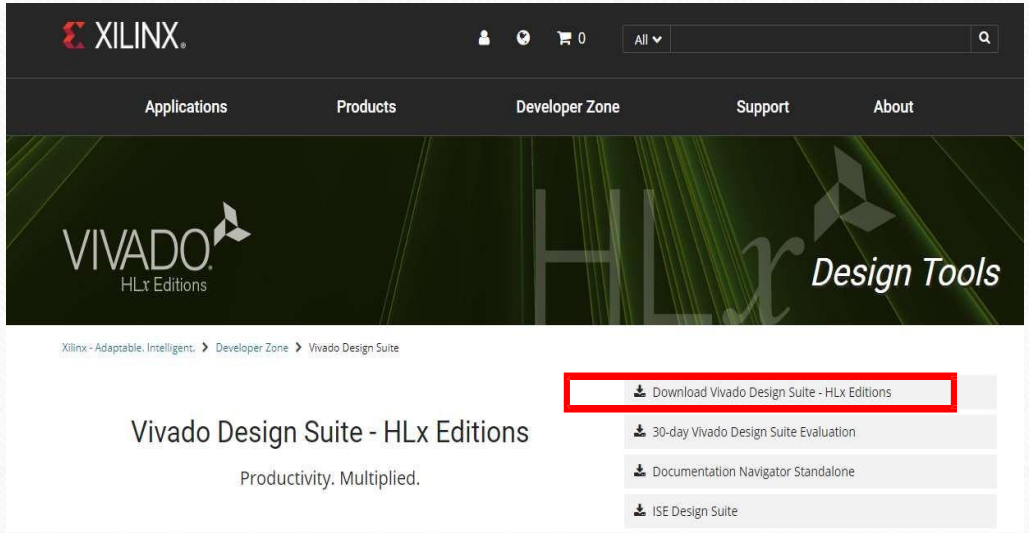
- 不能同時讓八個七段顯示器顯示出不同的數字
- 利用視覺暫留，讓七段顯示器顯示數值
- 課堂練習裡面的Code能提供想法
- 接線部分可以參考.xdc檔





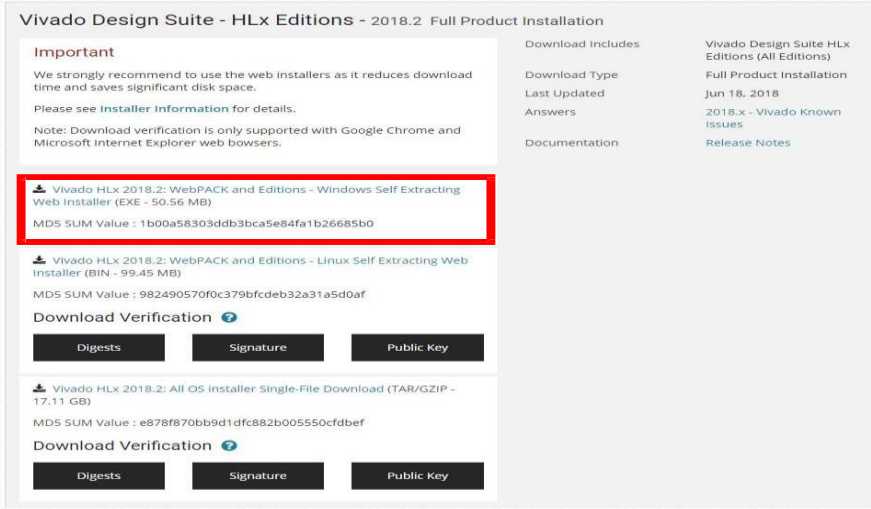
Install Vivado (1/9)

- 點選 Download Vivado Design Suite



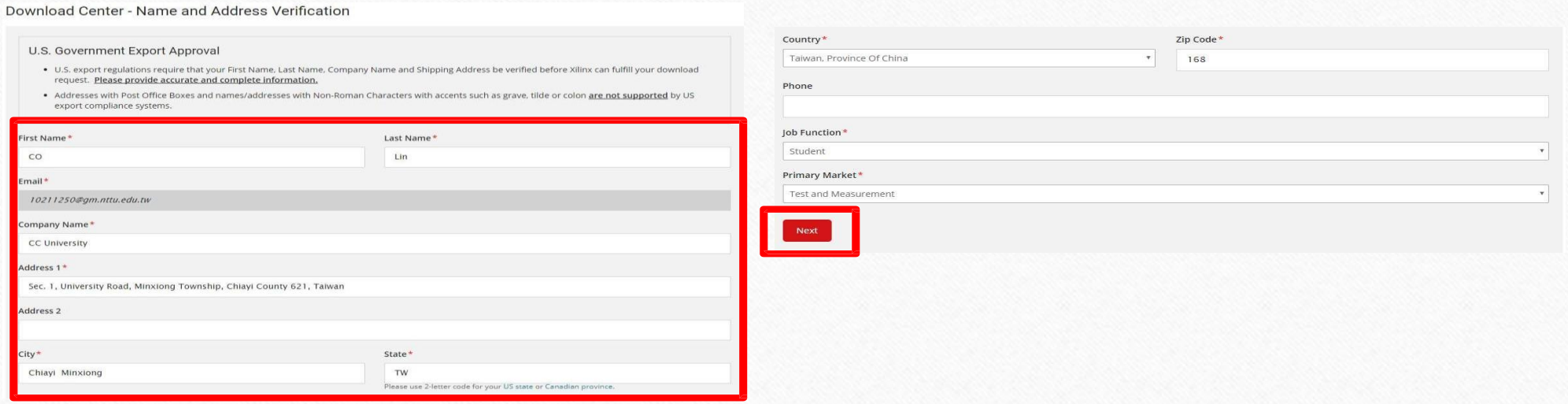
Install Vivado (2/9)

- 點選Vivado HLx 2018.2:WebPACK and Editions



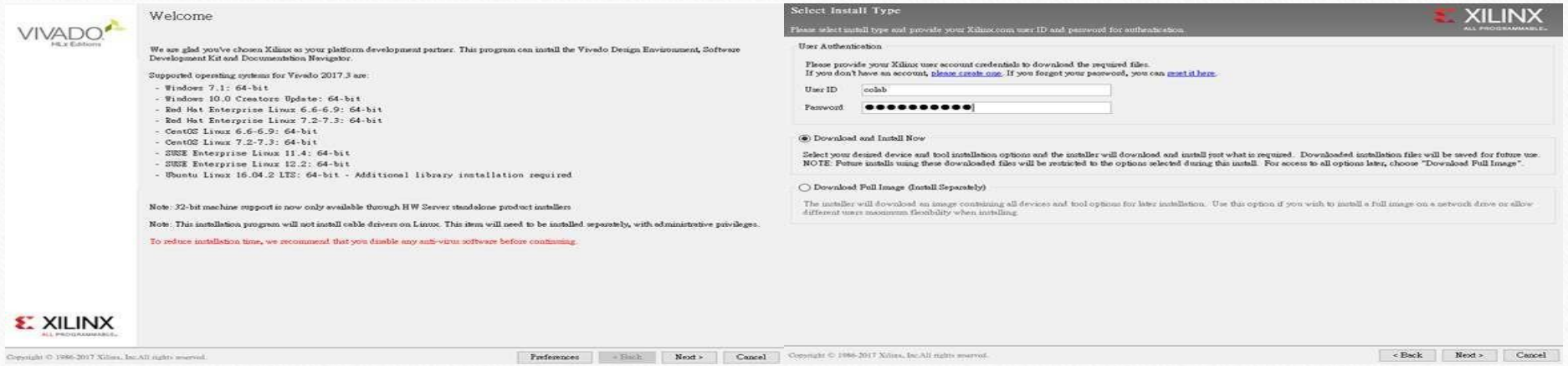
Install Vivado (3/9)

- 完善個人資料後下載(此範例不需要修改)



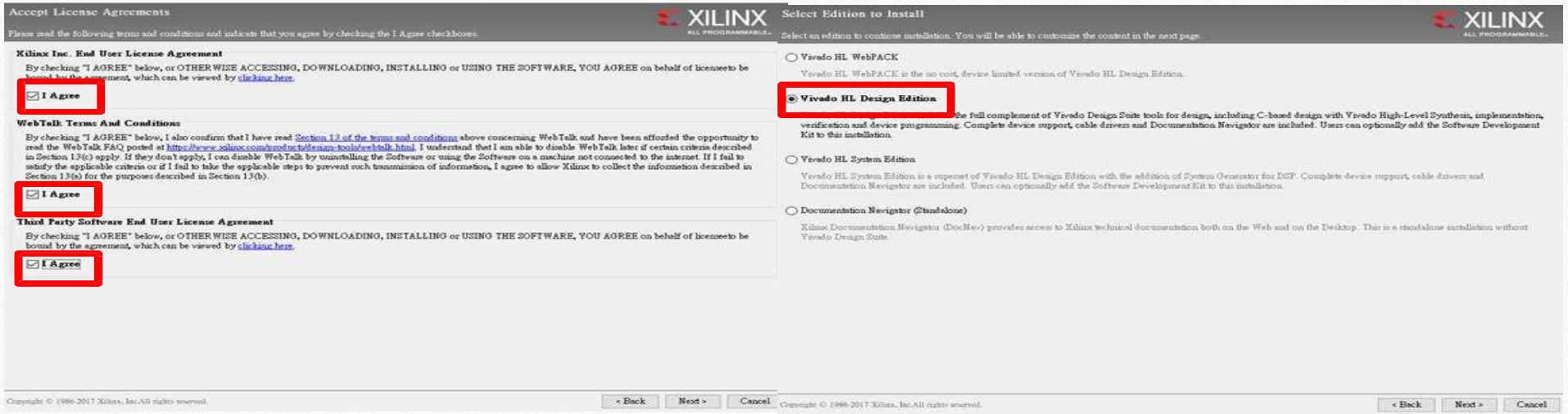
Install Vivado (4/9)

- 點擊EXE檔開始安裝



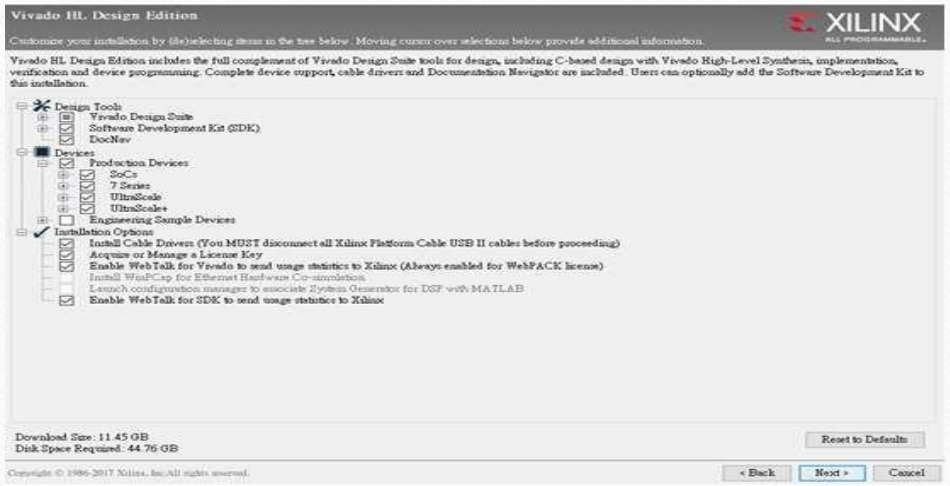
Install Vivado (5/9)

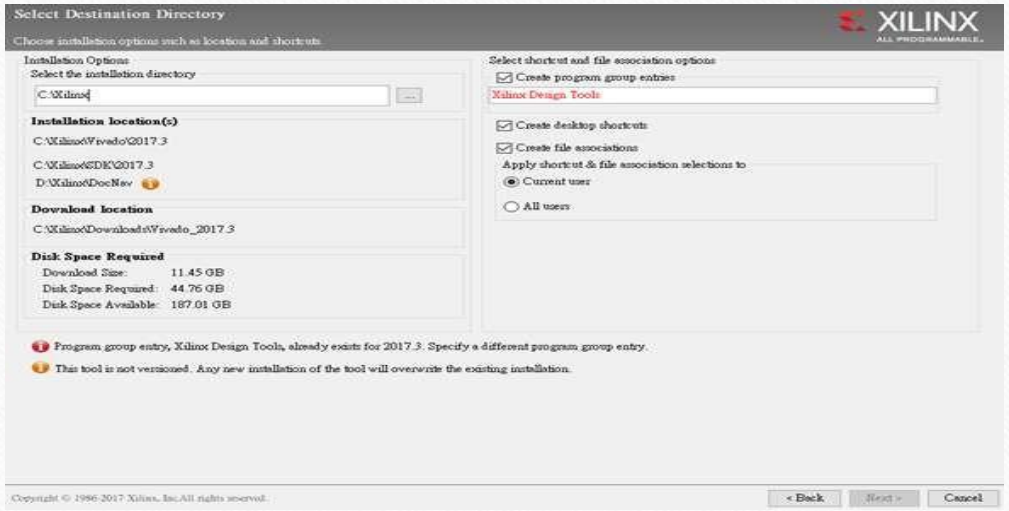
- 開始安裝



Install Vivado (6/9)

- 開始安裝





Install Vivado (7/9)

- 等待安裝

Install Vivado (8/9)

- USERNAME: colab
- password : cocococo4*
- LICENSE:
- https://drive.google.com/file/d/1ddZw3QlqKx_4s5ate7_dDbikZX7GN5h-/view?usp=sharing

備註：請大家不要修改帳號相關資料

Install Vivado (9/9)

- 加入LICENSE