

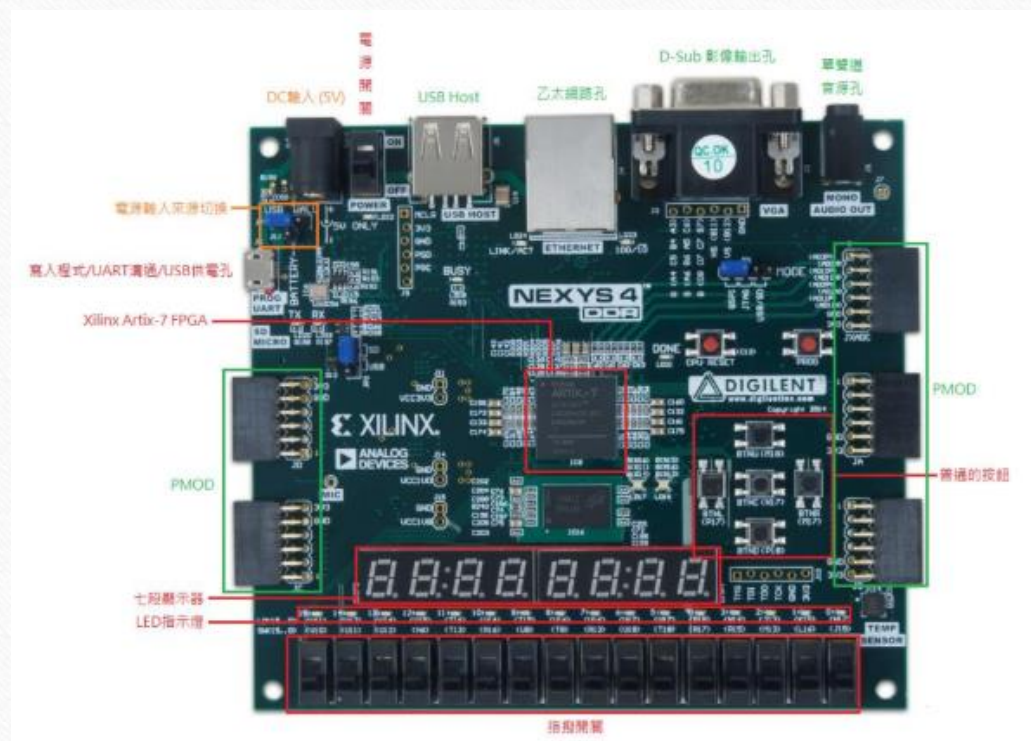
----- LAB 4 -----

FPGA Implementation (Nexys4)

洪銘佑
2018/11/28

實驗工具

- Nexys 4 DDR FPGA
- Vivado



Nexys-4 DDR FPGA 開發板

- 請同學愛惜使用
- 本堂課程結束前請填寫財產借用單

Nexys4-DDR Artix-7 FPGA 開發板 學習板 Xilinx XUP Diligent



全新

原標價：14,200 開賣者

數量：1 ☐ 不公開交易內容 (說明)

尚餘數量：3 (說明)

已售數量：2

付款方式： PChomePay 支付通 現金 (ATM、餘額、銀行支付)
銀行或郵局轉帳
郵局無摺存款
货到付款

☒ 請賣家開通支付通信用卡刷卡

運送方式：郵寄寄遞 40元
宅配/快遞 40元
货到付款 60元
[合併運費規則](#)

商品編號：11090613953389

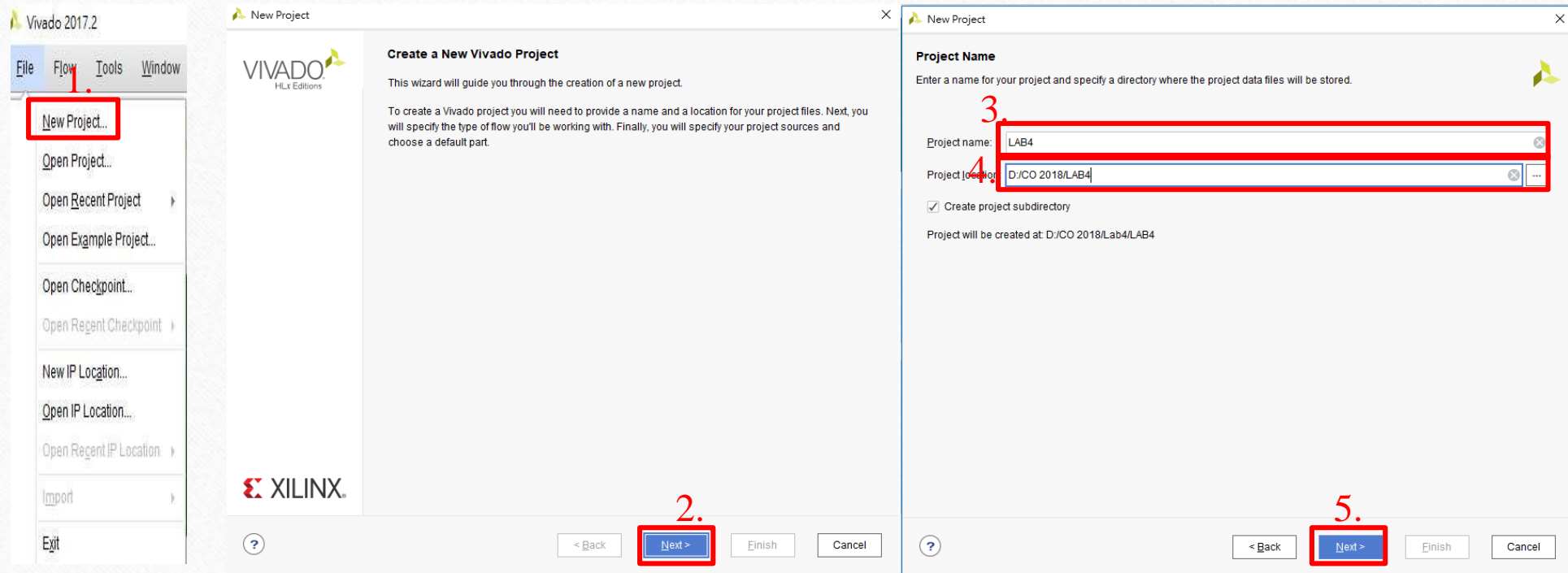
商品備註

- 物品狀況：全新
- 物品所在地：台灣 台北市
- 上架時間：2009-06-13 13:15:39
- 物品開始價格：14200元
- 可能會提前結束拍賣

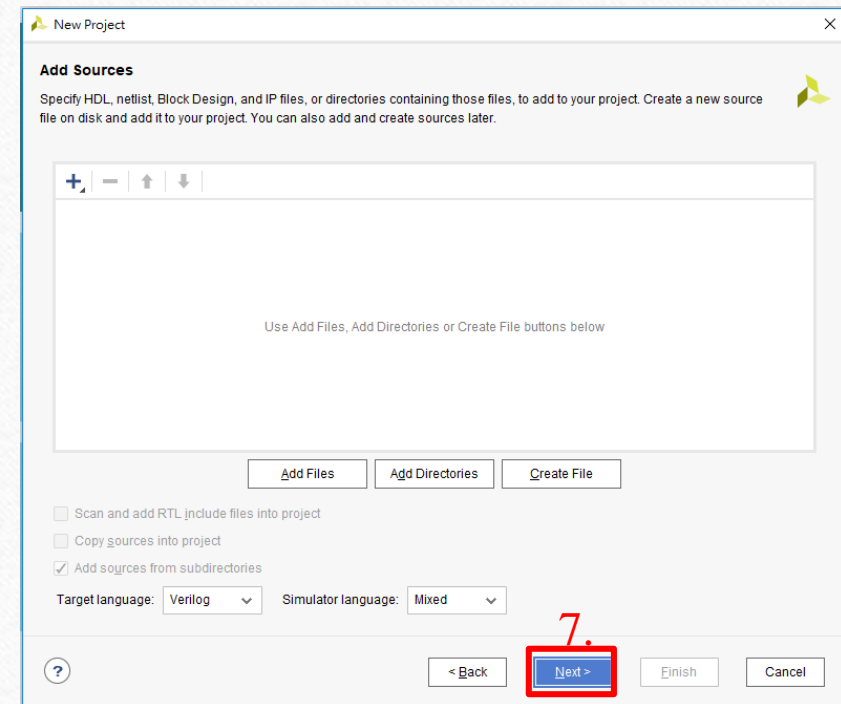
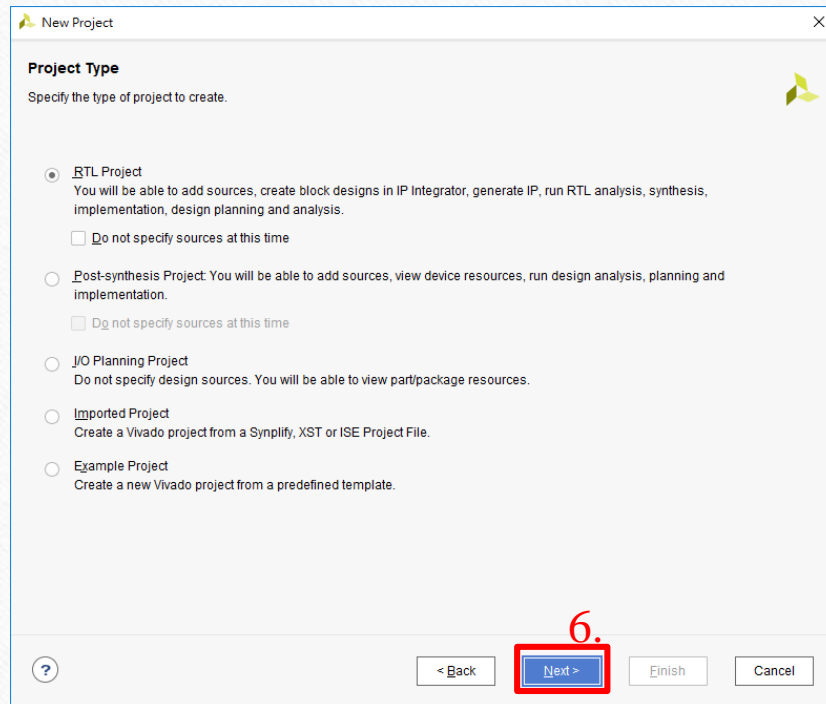
喜歡這商品嗎? 按讚及+1推薦給你的朋友吧! 0

商品價目

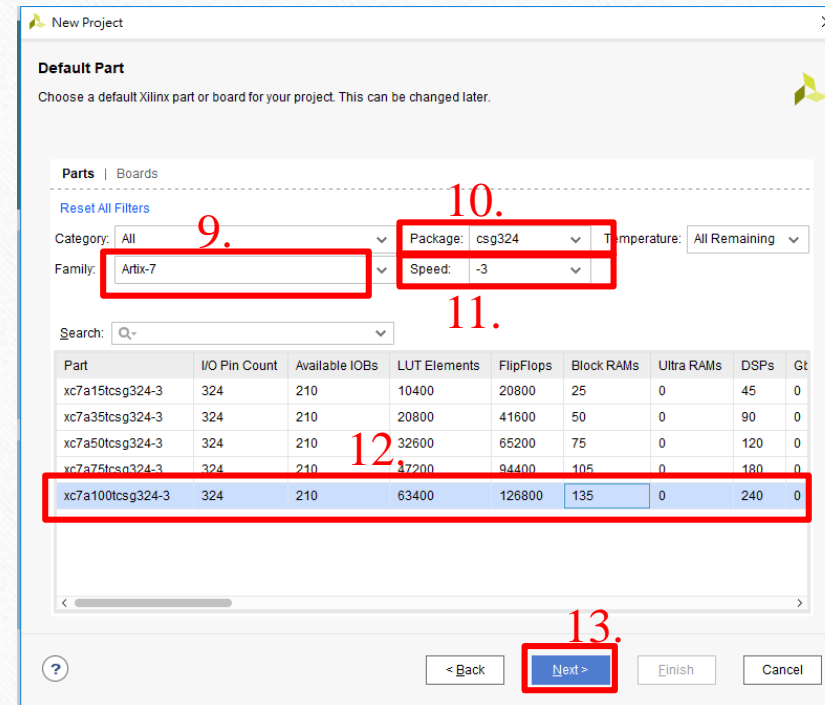
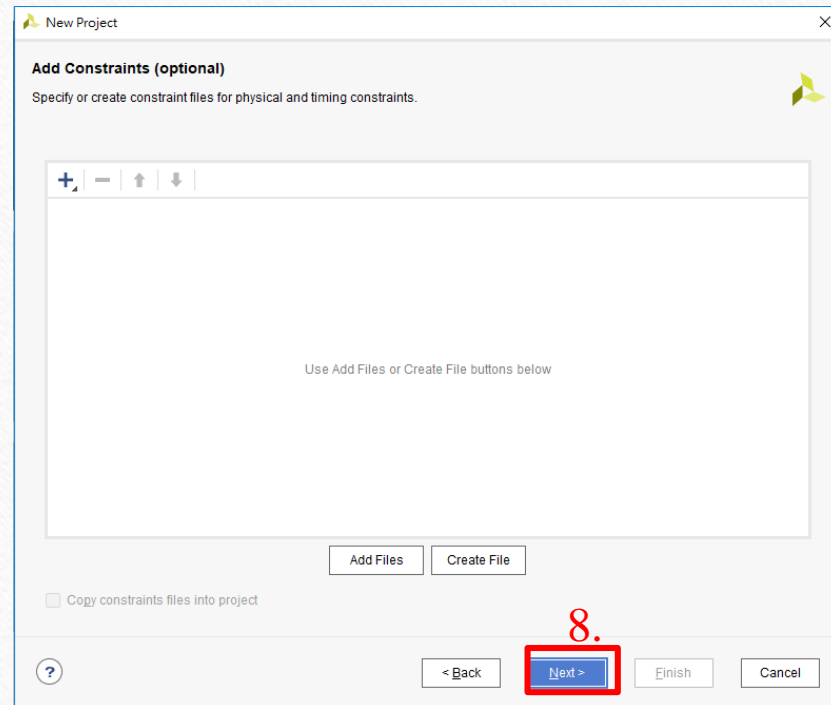
Vivado教學-開新專案



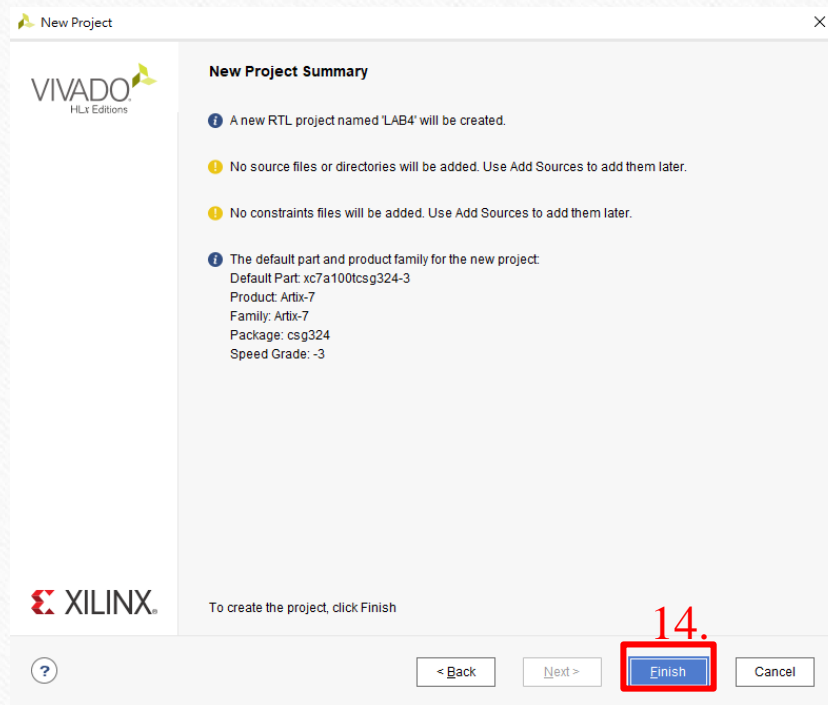
Vivado教學-開新專案



Vivado教學-開新專案

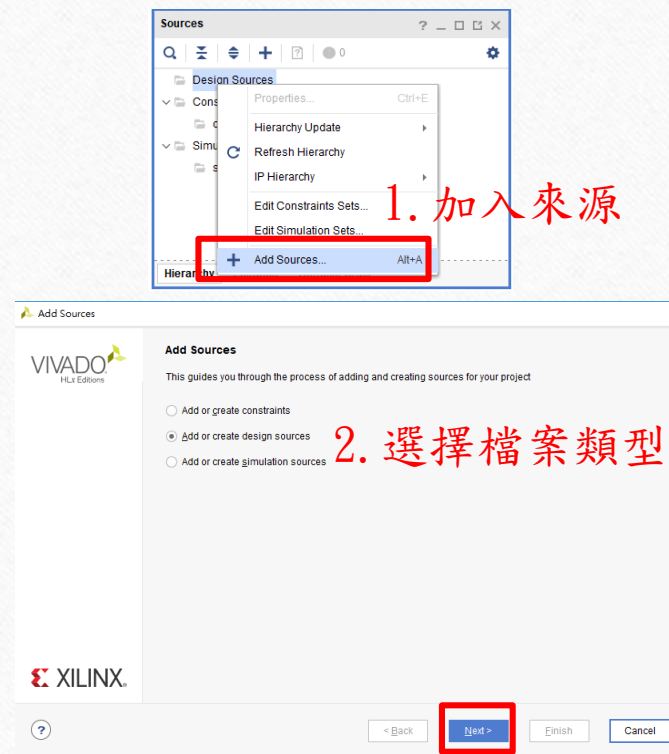


Vivado教學-開新專案

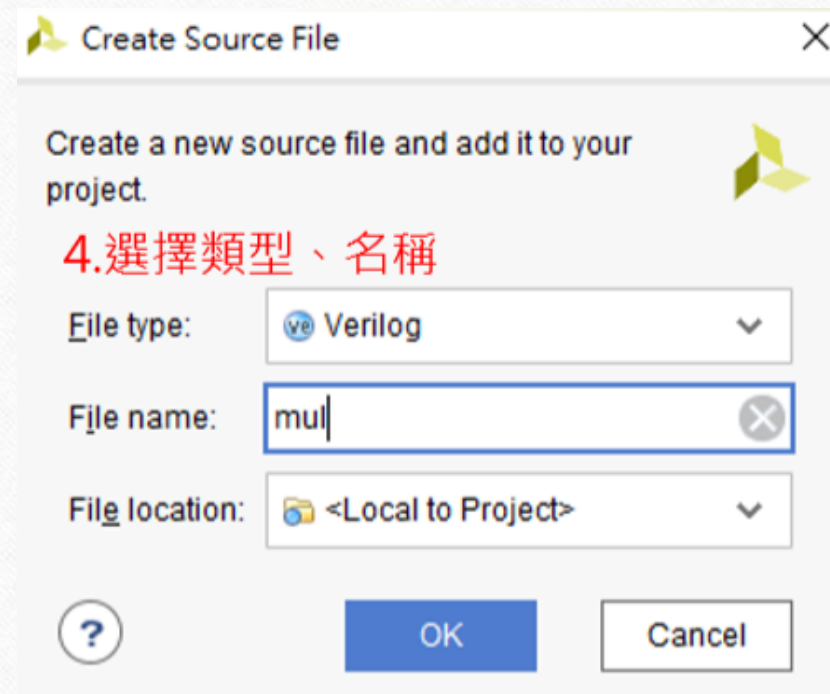
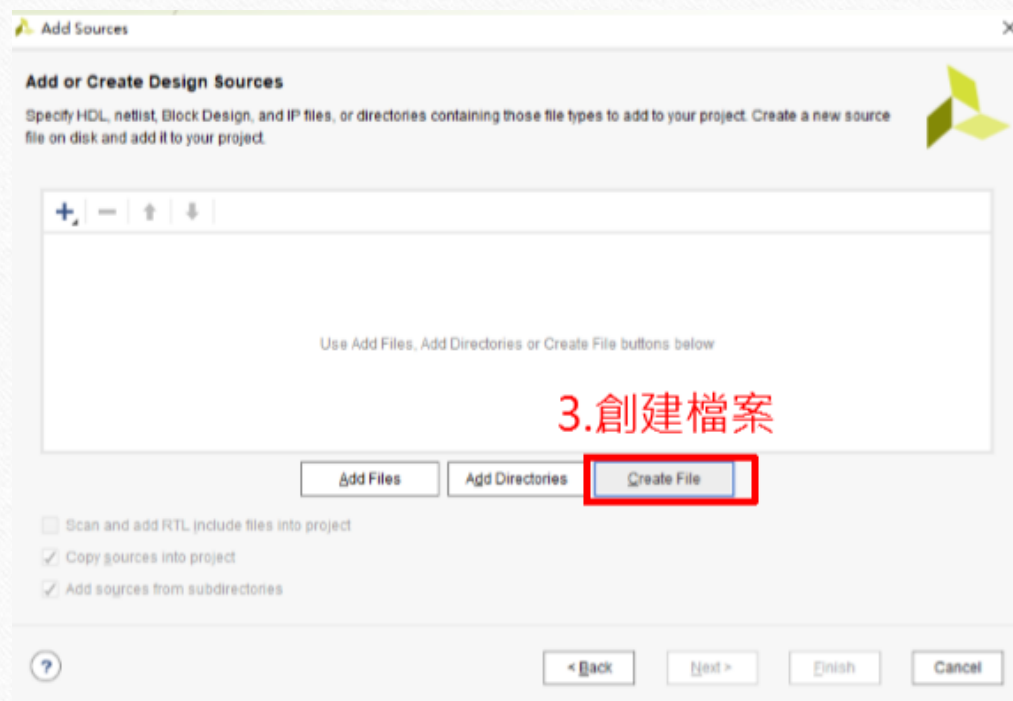


Vivado教學-創建專案原始檔

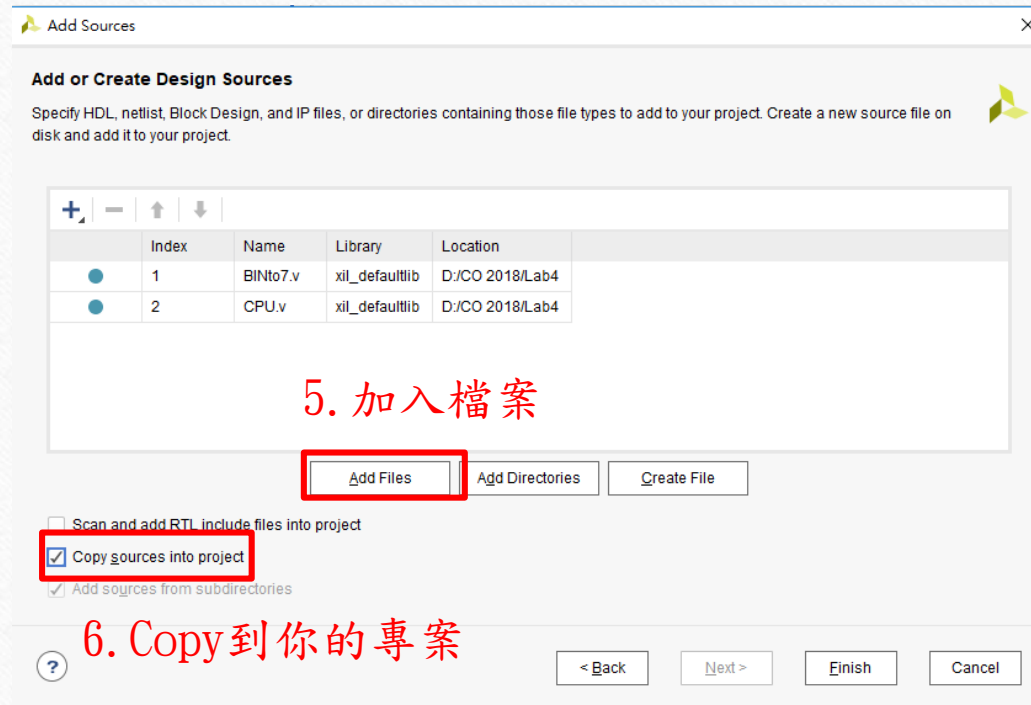
- 按右鍵新增檔案
- 選擇檔案類型：
 - constraints 可以新增.xdc檔
 - design sources 可以新增.v檔
- .xdc用來描述.
- v與實體線路的連接關係
- .v用來描述硬體行為
- 也可以從現有檔案匯



Vivado教學-創建專案原始檔



Vivado教學-加入專案原始檔



Vivado教學-將程式寫入FPGA板

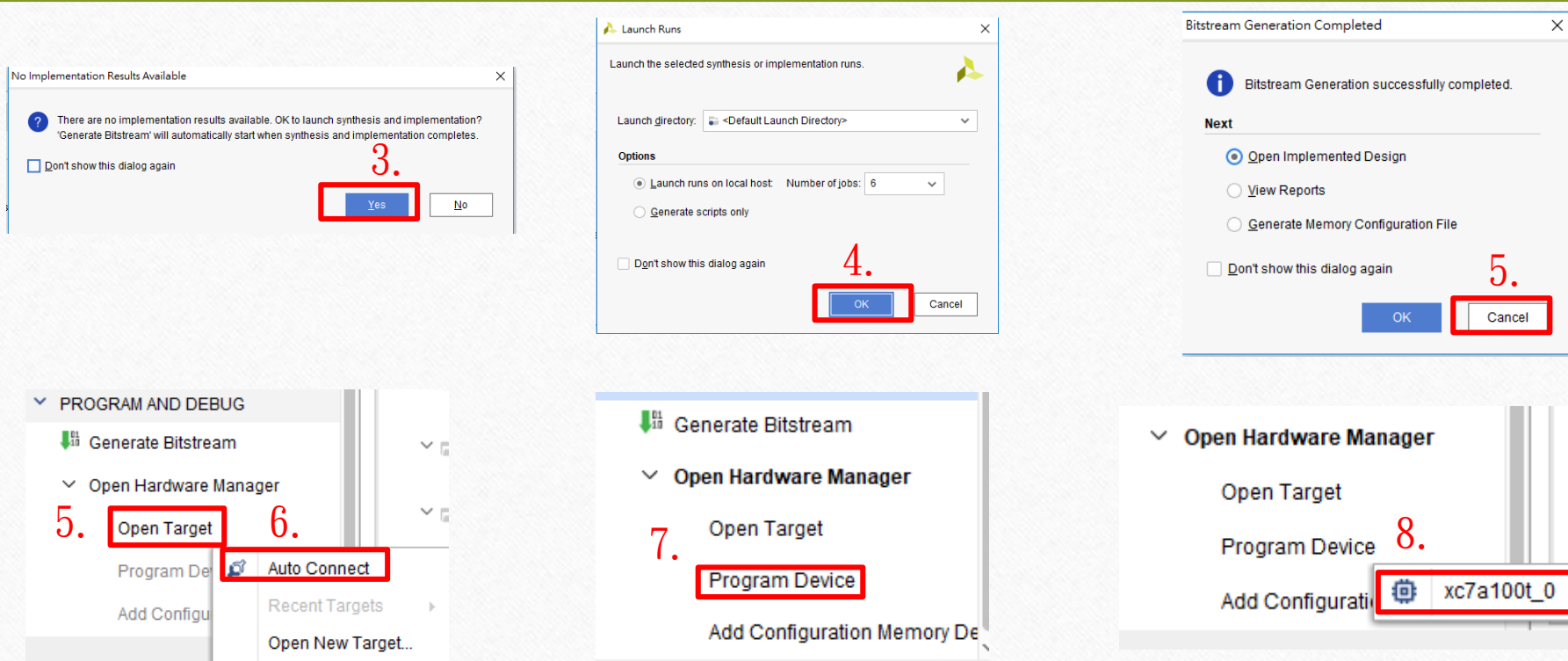
The screenshot displays the Vivado IDE interface with the following components:

- PROJECT MANAGER:** A sidebar on the left with a tree view containing:
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
 - SIMULATION
 - Run Simulation
 - RTL ANALYSIS
 - Open Elaborated Design
 - SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
 - IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - PROGRAM AND DEBUG
 - Generate Bitstream** (highlighted with a red box)
 - Open Hardware Manager
- Sources:** A central panel showing the project's source files:
 - Design Sources (2): CPU (CPU.v) (5), INSTRUCTION_FETCH (INSTRUCTION_FETCH.v)
 - Constraints (1): constrs_1 (1) (containing Nexys4.xdc)
 - Simulation Sources (2): sim_1 (2)
- Source File Properties:** A panel for CPU.v showing:
 - Enabled: ☒
 - Location: D:/CO 2018/Lab4/LAB4/LAB4.srcs/sources_1/in
 - Type: Verilog
 - Library: xil_defaultlib
- Project Summary:** A panel on the right showing the project's summary and the source file CPU.v.
- Design Runs:** A table at the bottom showing the status of various design runs.


Red handwritten annotations are present:


- 1. 寫完程式存檔** (1. Save program after writing) is written in red over the CPU.v source file.
- 2. 合成產生燒錄檔** (2. Synthesize to generate bitstream) is written in red over the 'Generate Bitstream' button in the Project Manager.

Vivado教學-將程式寫入FPGA板



Vivado教學-將程式寫入FPGA板

 Program Device ×

Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file. 

Bitstream file: × ...

Debug probes file: ...

☒ Enable end of startup check

? 9. Program Cancel

課堂練習

- 將實驗壓縮包裡面的CO_lab4example其中的專案寫入到 Nexys4 中，並了解其運作
- 修改 “top.v” 及 “Nexy4.xdc”，新增2個指撥按鈕使其能運算加法、乘法以及減法
- 向助教Demo結果
- 估Lab4成績30

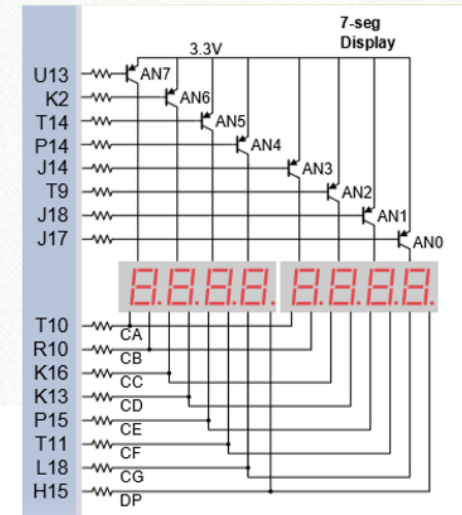
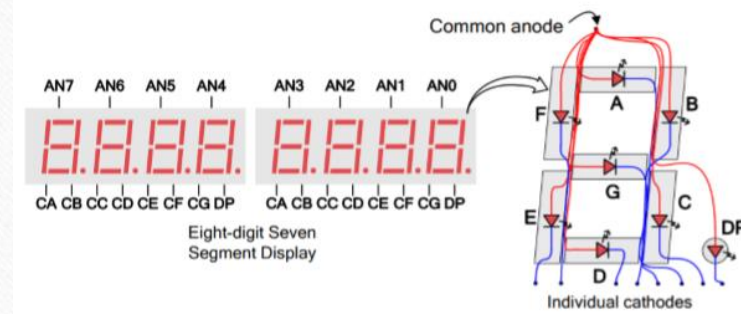
作業驗收說明

- 把作業三完成的CPU及求最相近的兩個質數寫入Nexys4 需要包含：
 - 13個指撥作為輸入值(sw0~sw12)
 - 運算結果分別以前、後4個七段顯示器顯示
 - 使用reset重新計算新值
 - 說明文件(PDF)、CPU及求最相近兩個質數的專案

※說明文件需包含：程式說明、如何控制顯示器
- 正確運算(50%)
- 能正確運算且.bit檔檔案大小排序最小的二十個人(20%)
- 作業驗收時間為12/12(三) 以前上傳

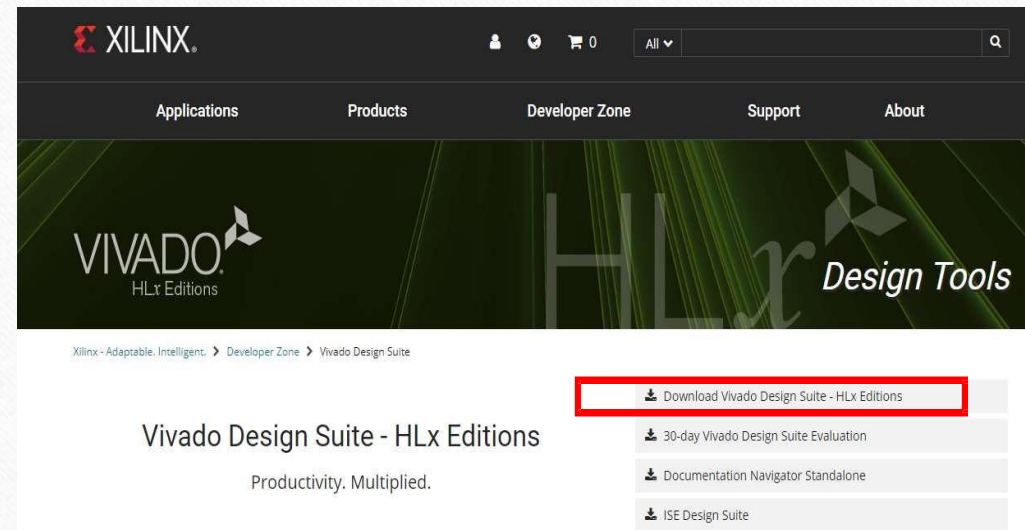
Nexys4的七段顯示器

- 不能同時讓八個七段顯示器顯示出不同的數字
- 利用視覺暫留，讓七段顯示器顯示數值
- 課堂練習裡面的Code能提供想法
- 接線部分可以參考.xdc檔



Install Vivado (1/9)

- 點選 Download Vivado Design Suite



Install Vivado (2/9)

- 點選 Vivado HLx 2018.2:WebPACK and Editions

Vivado Design Suite - HLx Editions - 2018.2 Full Product Installation

Important

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Note: Download verification is only supported with Google Chrome and Microsoft Internet Explorer web browsers.

Download includes

Download Type
Last Updated
Answers
Documentation

Vivado Design Suite HLx Editions (All Editions)
Full Product Installation
Jun 18, 2018
2018.x - Vivado Known Issues
[Release Notes](#)

Vivado HLx 2018.2: WebPACK and Editions - Windows Self Extracting Web Installer (EXE - 50.56 MB)

MD5 SUM Value : 1b00a58303ddb3bca5e84fa1b26685b0

Vivado HLx 2018.2: WebPACK and Editions - Linux Self Extracting Web Installer (BIN - 99.45 MB)

MD5 SUM Value : 982490570f0c379bfcdeb32a31a5d0af

Download Verification

Digests Signature Public Key

Vivado HLx 2018.2: All OS Installer Single-File Download (TAR/GZIP - 17.11 GB)

MD5 SUM Value : e878f870bb9d1dfc882b005550cfdbe

Download Verification

Digests Signature Public Key

Install Vivado (3/9)

- 完善個人資料後下載(此範例不需要修改)

Download Center - Name and Address Verification

U.S. Government Export Approval

- U.S. export regulations require that your First Name, Last Name, Company Name and Shipping Address be verified before Xilinx can fulfill your download request. **Please provide accurate and complete information.**
- Addresses with Post Office Boxes and names/addresses with Non-Roman Characters with accents such as grave, tilde or colon **are not supported** by US export compliance systems.

First Name *

CQ

Last Name *

Lin

Email *

10211250@gm.ntnu.edu.tw

Company Name *

CC University

Address 1 *

Sec. 1, University Road, Minxiong Township, Chiayi County 621, Taiwan

Address 2

City *

Chiayi Minxiong

State *

TW

Country *

Taiwan, Province Of China

Zip Code *

168

Phone

Job Function *

Student

Primary Market *

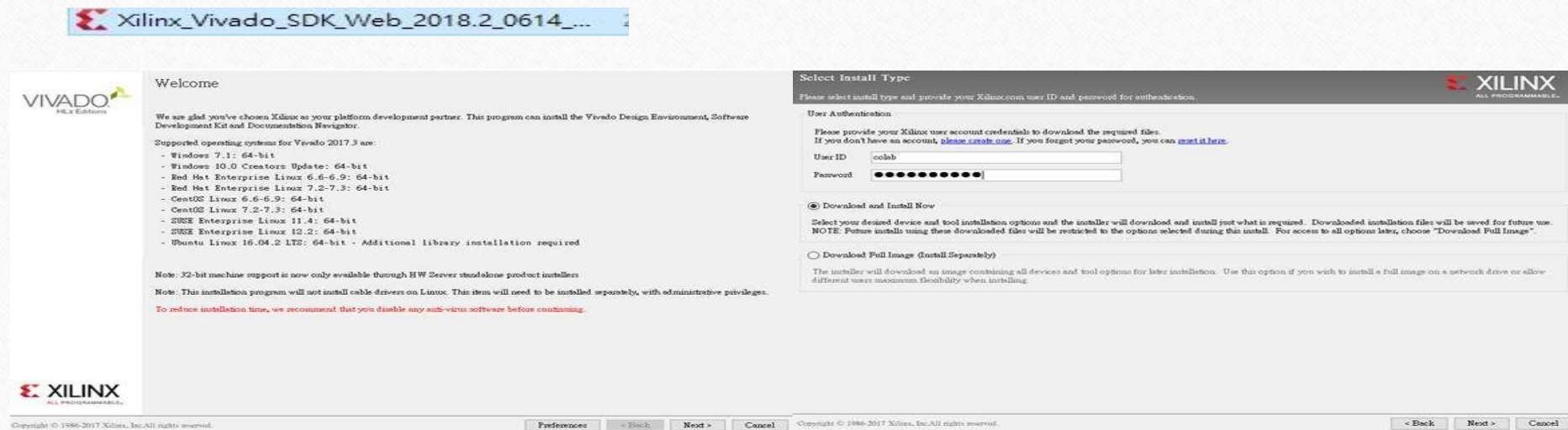
Test and Measurement

Next

19

Install Vivado (4/9)

- 點擊EXE檔開始安裝



Install Vivado (5/9)

- 開始安裝

The screenshot displays the Xilinx Vivado installation wizard. The left pane shows the 'Accept License Agreements' screen, and the right pane shows the 'Select Edition to Install' screen.

Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

Xilinx Inc. End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ I Agree

WebTalk Terms And Conditions

By checking "I AGREE" below, I also confirm that I have read [Section 12 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).

☒ I Agree

Third Party Software End User License Agreement

By checking "I AGREE" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, YOU AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).

☒ I Agree

Select Edition to Install

Select an edition to continue installation. You will be able to customize the content in the next page.

☐ Vivado HL WebPACK

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition.

☒ Vivado HL Design Edition

The full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

☐ Vivado HL System Edition

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

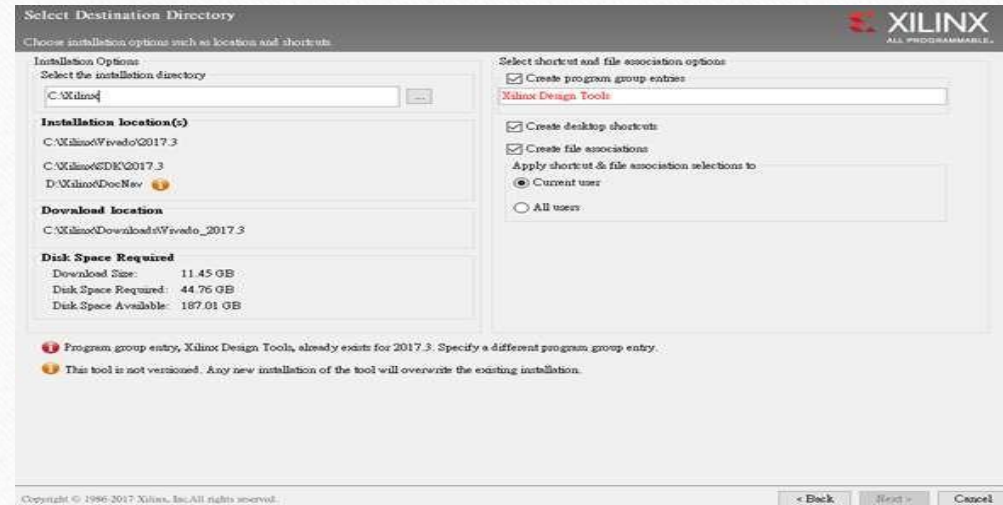
☐ Documentation Navigator (Standalone)

Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

Copyright © 1986-2017 Xilinx, Inc. All rights reserved. < Back Next > Cancel

Install Vivado (6/9)

- 開始安裝



Install Vivado (7/9)

- 等待安裝



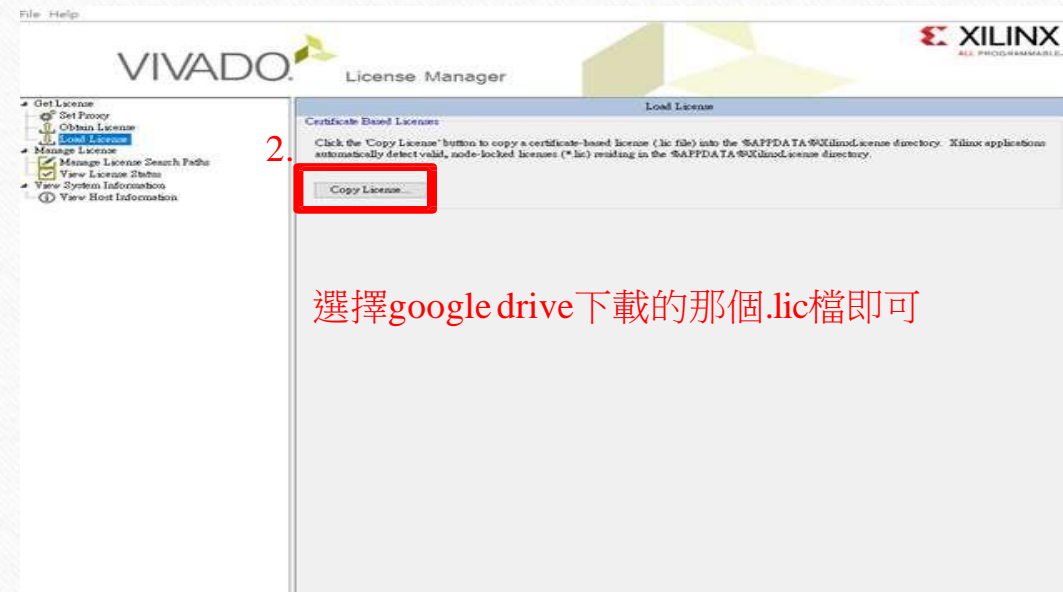
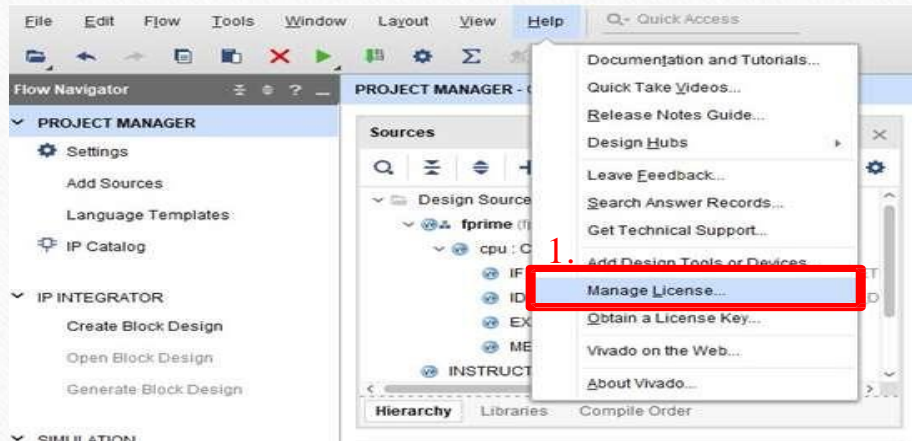
Install Vivado (8/9)

- USERNAME: colab
- password : cocococo4*
- LICENSE:
- https://drive.google.com/file/d/1ddZw3QlqKx_4s5ate7_dDbikZX7GN5h-/view?usp=sharing

備註：請大家不要修改帳號相關資料

Install Vivado (9/9)

- 加入LICENSE



選擇google drive下載的那個.lic檔即可