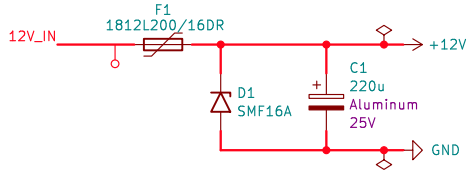
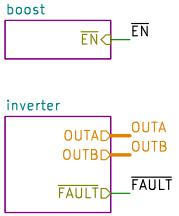
POWER INPUT

Input must be 10 to 16 V
Circuit protection
– Internal: 2 A polyfuse and TVS
– External: 3 A fuse recommended

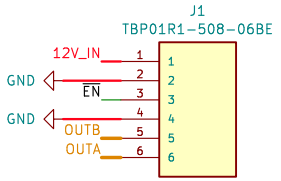


COMPONENTS



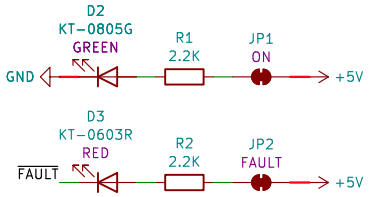
CONNECTORS

Pin 1/2: Power input
Pin 3/4: Enable input
Pin 5/6: PDLC output



INDICATORS

Indicate boost converter and inverter status



github.com/j9brown/pdlc
Brown Studios LLC

Sheet: /
File: pdlc.kicad_sch

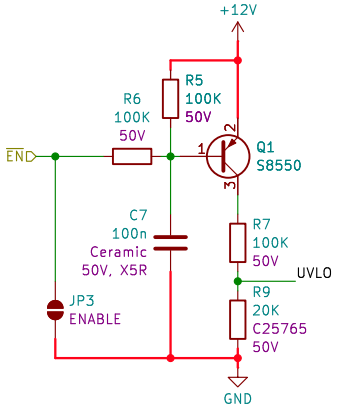
Title: PDLC Driver

Size: A4	Date: 2025-05	**Rev: v1.0**
KiCad E.D.A. 8.0.8		Id: 1/3

ENABLE AND UVLO

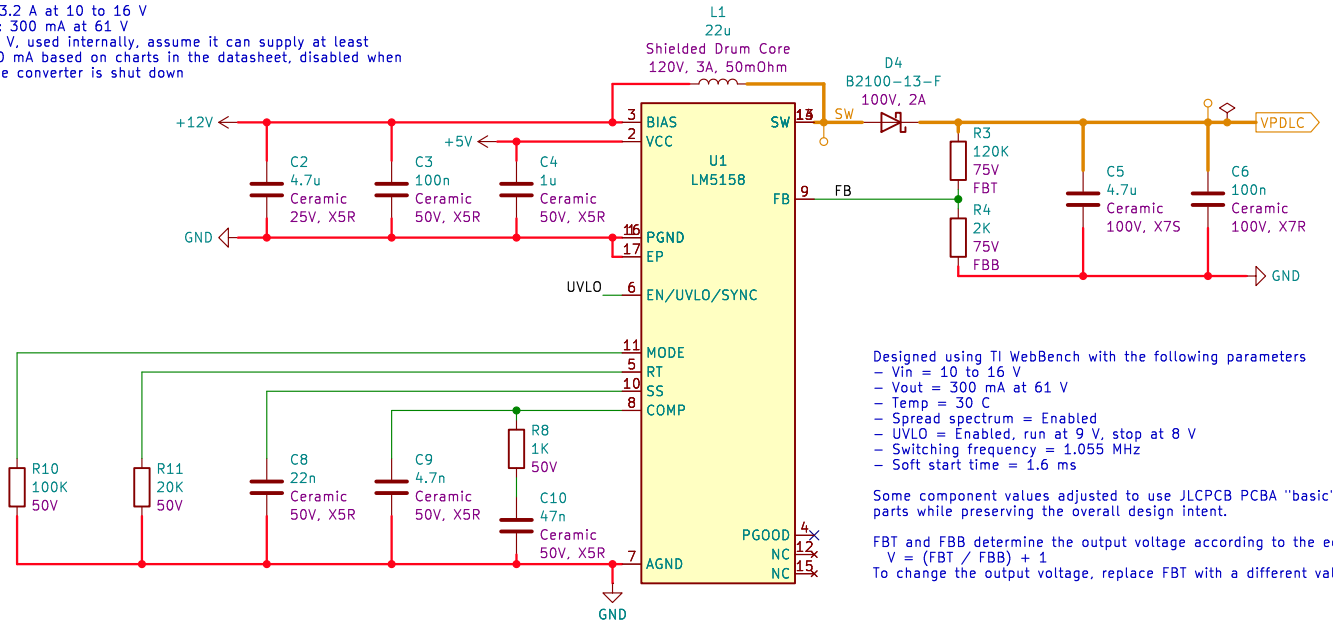
Provides a high−impedance input to enable the converter when EN is pulled low

When enabled, the converter remains in standby until BIAS rises above the UVLO threshold



60 V BOOST CONVERTER

Input: 3.2 A at 10 to 16 V
Output: 300 mA at 61 V
VCC: 5 V, used internally, assume it can supply at least 50 mA based on charts in the datasheet, disabled when the converter is shut down



Designed using TI WebBench with the following parameters
- Vin = 10 to 16 V
- Vout = 300 mA at 61 V
- Temp = 30 C
- Spread spectrum = Enabled
- UVLO = Enabled, run at 9 V, stop at 8 V
- Switching frequency = 1.055 MHz
- Soft start time = 1.6 ms

Some component values adjusted to use JLCPCB PCBA "basic" parts while preserving the overall design intent.

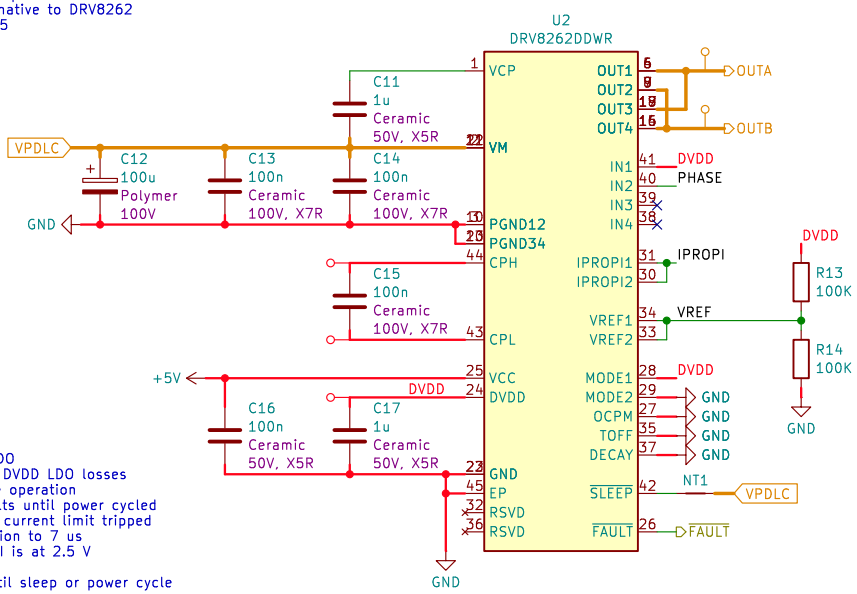
FBT and FBB determine the output voltage according to the equation
V = (FBT / FBB) + 1
To change the output voltage, replace FBT with a different value

Sheet: /boost/		
File: boost.kicad_sch		
Title: PDLC Driver Boost Converter		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 2/3

H-BRIDGE DRIVER

Drives a square wave at alternating polarity into a capacitive load
with current limiting and short circuit protection
DRV8263 will be a more economical alternative to DRV8262
but it is still in preview as of 2025/5

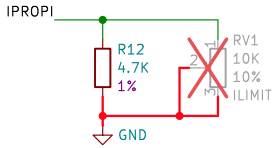
Load characteristics for PDLC film
- voltage: 60 V
- capacitance: up to 30 uF?
- inductance: negligible
- frequency: 100 Hz?
- max charge time: 2 ms?



DVDD supplies 5 V supply from internal LDO
VCC externally supplies logic to minimize DVDD LDO losses
MODE1/MODE2 set to use single H-bridge operation
OCPM set to latch-off on overcurrent faults until power cycled
DECAY set for high-side slow decay after current limit tripped
TOFF set PWM time off for current regulation to 7 us
VREF triggers current limiting when IPROPI is at 2.5 V
SLEEP set to never sleep
FAULT reports protection fault, latches until sleep or power cycle

CURRENT LIMIT

Increasing resistance of the setpoint decreases the current limit



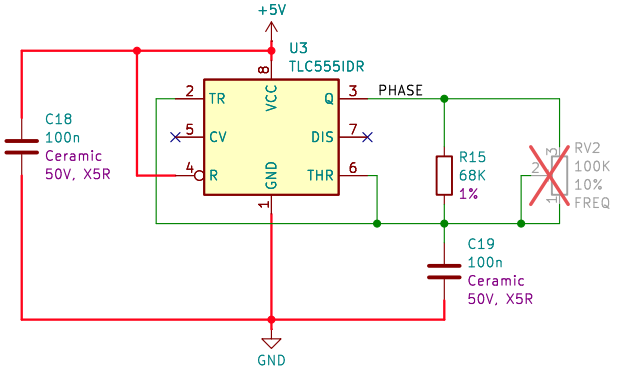
Set overcurrent protection trip current
Itrip (A) = 4717 * Vref (V) / Ripropi (Ω)
Given Vref = 2.5 V, Ripropi = 4.7 K, Itrip = 2.5 A

We can estimate an approximate lower bound for the current limit
by considering how long it would take to charge an ideal capacitor
that represents the load.

Given dt = dV * C / I, dV = 2 * 60 V = 120 V, C = 30 uF, dt < 2 ms
So I > dV / dt * C = 1.8 A

COMMUTATION SEQUENCING

Timer with 50% duty cycle
Given f = 100 Hz, C = 100n, R = 0.722 / (f * C) = 72.2K > 68 K (106 Hz actual)



Sheet: /inverter/
File: inverter.kicad_sch

Title: PDLC Driver Inverter

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8		Id: 3/3