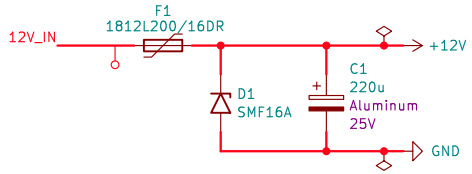
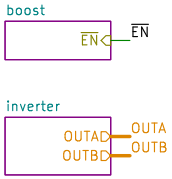
POWER INPUT

Input must be 10 to 16 V
Circuit protection
– Internal: 2 A polyfuse and TVS
– External: 3 A fuse recommended

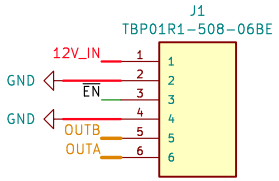


COMPONENTS



CONNECTORS

Pin 1/2: Power input
Pin 3/4: Enable input
Pin 5/6: PDLC output



INDICATORS

Indicate boost converter status

github.com/j9brown/pdlc
Brown Studios LLC

Sheet: /
File: pdlc.kicad_sch

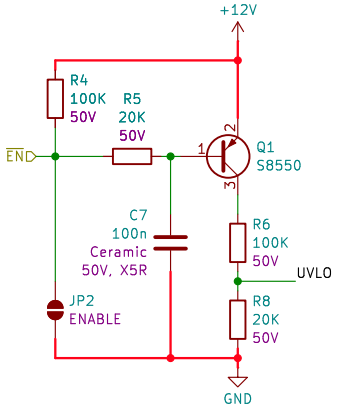
Title: PDLC Driver

Size: A4	Date: 2025-05	**Rev: v1.0**
KiCad E.D.A. 8.0.8		Id: 1/5

ENABLE AND UVLO

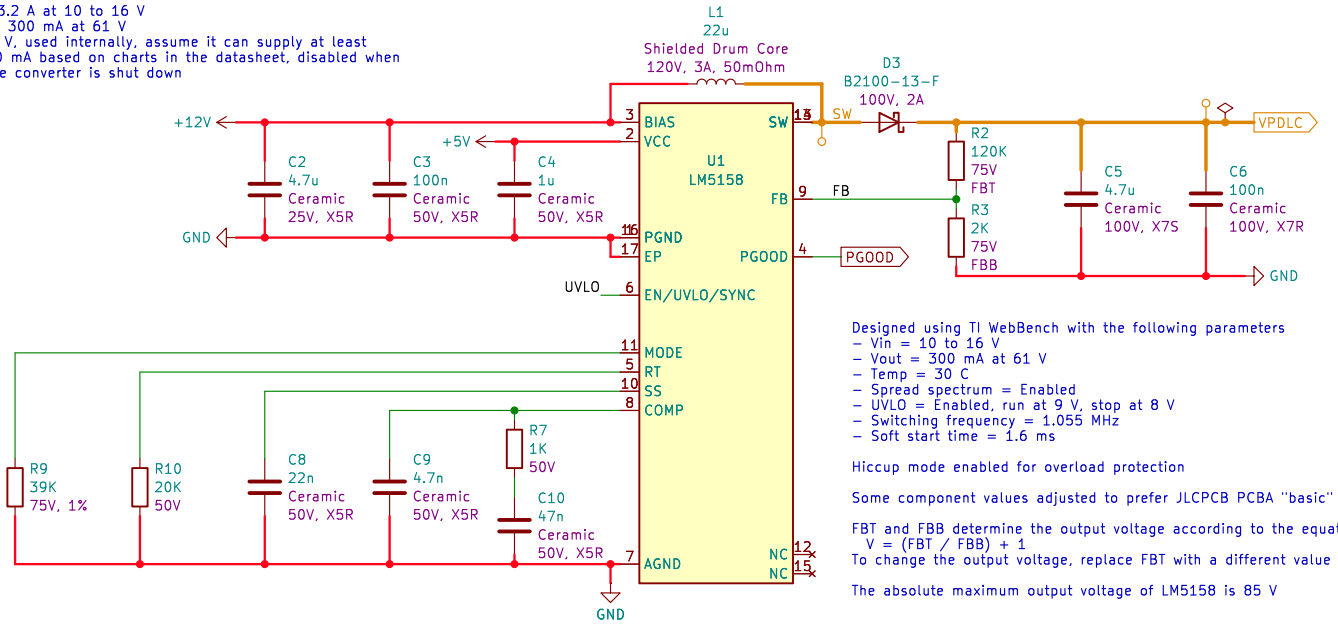
Provides a high−impedance input to enable the converter when EN is pulled low

When enabled, the converter remains in standby until BIAS rises above the UVLO threshold



60 V BOOST CONVERTER

Input: 3.2 A at 10 to 16 V
Output: 300 mA at 61 V
VCC: 5 V, used internally, assume it can supply at least 50 mA based on charts in the datasheet, disabled when the converter is shut down



Designed using TI WebBench with the following parameters
- Vin = 10 to 16 V
- Vout = 300 mA at 61 V
- Temp = 30 C
- Spread spectrum = Enabled
- UVLO = Enabled, run at 9 V, stop at 8 V
- Switching frequency = 1.055 MHz
- Soft start time = 1.6 ms

Hiccup mode enabled for overload protection

Some component values adjusted to prefer JLCPCB PCBA "basic" parts

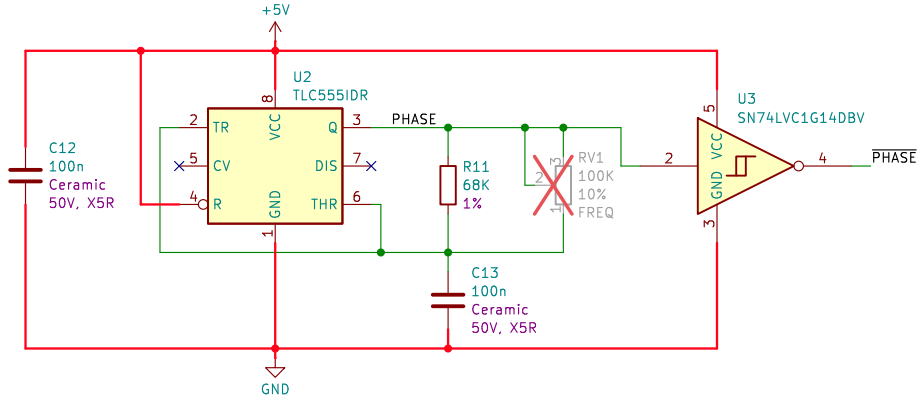
FBT and FBB determine the output voltage according to the equation
V = (FBT / FBB) + 1
To change the output voltage, replace FBT with a different value

The absolute maximum output voltage of LM5158 is 85 V

Sheet: /boost/		
File: boost.kicad_sch		
Title: PDLC Driver Boost Converter		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 2/5

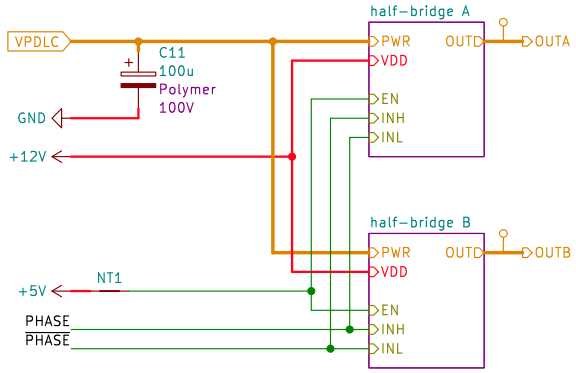
COMMUTATION SEQUENCING

Timer with 50% duty cycle
Given f = 100 Hz, C = 100n, R = 0.722 / (f * C) = 72.2K > 68 K (106 Hz actual)



H-BRIDGE

Drives a square wave with alternating polarity into a capacitive load
The half-bridges have built-in cross-conduction protection so no dead-time is needed
The boost converter provides overload protection of the output



Sheet: /inverter/
File: inverter.kicad_sch

Title: PDLC Driver Inverter

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8		Id: 3/5

HALF-BRIDGE

Design parameters

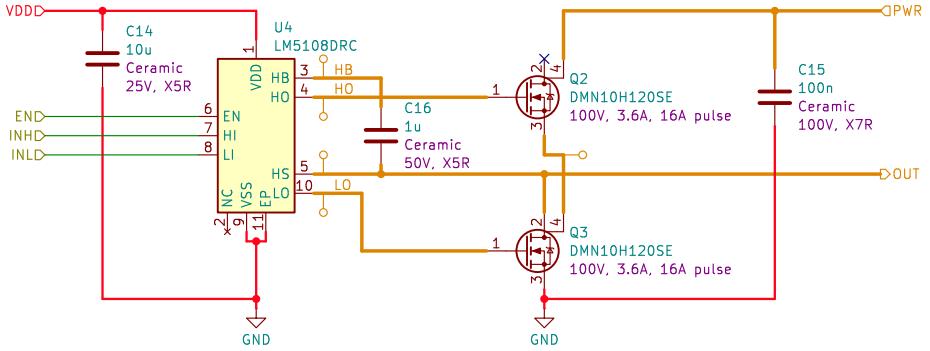
- Low frequency switching: ~100 Hz
- Low average current: up to 300 mA
- High pulsed current: could be several amps for a few milliseconds while switching a predominantly capacitive load
- High voltage: 60 V nominal, 85 V maximum
- VDD: 12 V nominal, 16 V maximum

At low frequencies, the bootstrap capacitor must be relatively large to maintain charge for the entire cycle due to internal leakage of the bootstrap circuitry which greatly exceeds the actual MOSFET gate charge. Refer to data sheet section 8.2.2.1 and assume 100% duty cycle. Rough calculation yields 200 nF so we use 1 uF to ensure a margin.

The VDD capacitor should be 10 times the bootstrap capacitor value, so 10 uF

No gate resistor is needed due to the low switching frequency and gate charge

The output MOSFET must tolerate high pulse currents when switching the capacitive load so it is sized accordingly



Sheet: /inverter/half-bridge A/
File: half-bridge.kicad_sch

Title: PDLC Driver Half Bridge

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8		Id: 4/5

HALF-BRIDGE

Design parameters

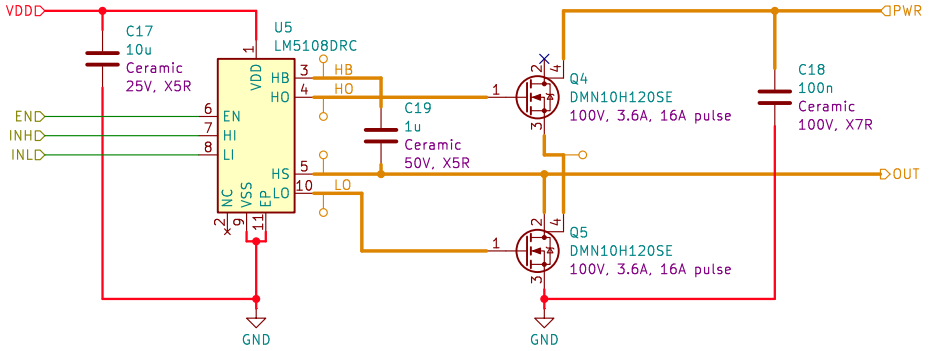
- Low frequency switching: ~100 Hz
- Low average current: up to 300 mA
- High pulsed current: could be several amps for a few milliseconds while switching a predominantly capacitive load
- High voltage: 60 V nominal, 85 V maximum
- VDD: 12 V nominal, 16 V maximum

At low frequencies, the bootstrap capacitor must be relatively large to maintain charge for the entire cycle due to internal leakage of the bootstrap circuitry which greatly exceeds the actual MOSFET gate charge. Refer to data sheet section 8.2.2.1 and assume 100% duty cycle. Rough calculation yields 200 nF so we use 1 uF to ensure a margin.

The VDD capacitor should be 10 times the bootstrap capacitor value, so 10 uF

No gate resistor is needed due to the low switching frequency and gate charge

The output MOSFET must tolerate high pulse currents when switching the capacitive load so it is sized accordingly



Sheet: /inverter/half-bridge B/
File: half-bridge.kicad_sch

Title: PDLC Driver Half Bridge

Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.8		Id: 5/5