TOPICAL REVIEW

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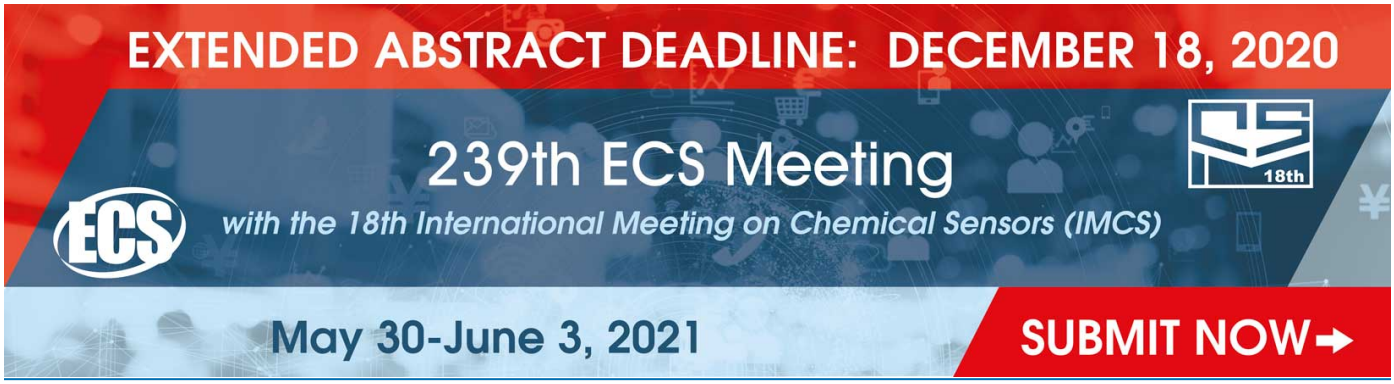

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TOPICAL REVIEW

Synaptic electronics: materials, devices and applications

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Abstract
In this paper, the recent progress of synaptic electronics is reviewed. The basics of biological synaptic plasticity and learning are described. The material properties and electrical switching characteristics of a variety of synaptic devices are discussed, with a focus on the use of synaptic devices for neuromorphic or brain-inspired computing. Performance metrics desirable for large-scale implementations of synaptic devices are illustrated. A review of recent work on targeted computing applications with synaptic devices is presented.

(Some figures may appear in colour only in the online journal)

1. Introduction

Synaptic electronics is a re-emerging field of research aiming to build artificial synaptic devices to emulate the computation performed by biological synapses. The idea of building bio-inspired cognitive adaptive solid-state devices has been around for decades [1–3]. The recent revival of interest in building electronic systems that mimic the ability of the brain in performing energy-efficient and fault-tolerant computation in a compact space coincides with the Darpa Synapse program [4] in 2008. Since then, research activities in this field have been growing rapidly (figure 1). The research effort on brain-inspired computing and synaptic electronics can be understood considering the inefficiency of conventional computational systems in solving complex problems. The conventional computing paradigm based on CMOS logic and the von Neumann architecture [5] has been ideal for solving structured problems, such as well-defined mathematical problems or processing precisely defined data sets. However, it cannot compete with biological brains where the problems involve interaction with the real world and where both the inputs and outputs are often imprecisely specified. While computation based on statistical methods [6–9] using conventional Si CMOS technologies are possible solutions, it is expected that brain-inspired computing may offer a better energy and space tradeoff. For tasks involving real-time processing of unstructured sensory data, such as image, video or voice recognition, navigation, etc, the biological brain outperforms conventional computers with a superior performance. The biological brain has a radically different architecture and function compared to conventional computers: (1) it is massively parallel, three-dimensionally organized, and extremely compact, (2) it is power efficient, (3) it combines storage and computation, (4) it is fault and variation tolerant and robust, (5) it is self-learning and adaptive to changing environments. A recent performance comparison [10] between human brains and a supercomputer (IBM Watson [11]) was carried out for computational tasks involving mainly voice recognition, natural language processing, information retrieval, and machine learning. The supercomputer won the contest (Jeopardy) with the advantage of almost 40-fold difference in reaction time to activate the buzzer. But the main points, which were missing in such comparison, were the energy consumption and physical sizes of the computational systems. Watson has 2880 computing cores (10 refrigerators worth in size and space) and requires about 80 kW of power and 20 tonnes of air-conditioned cooling

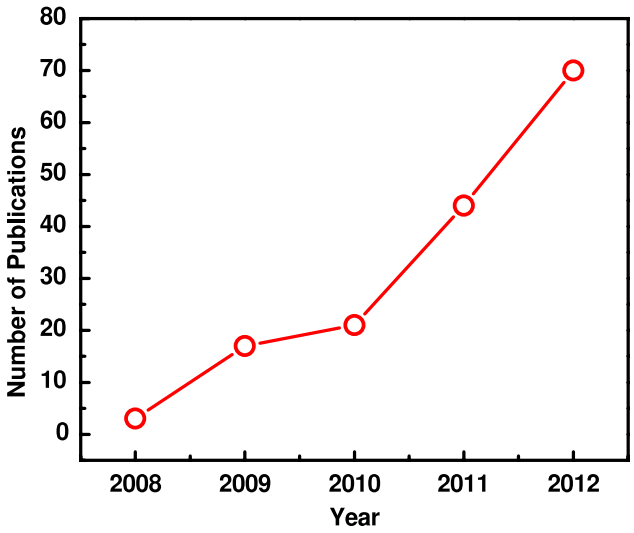

Figure 1. Data obtained by searching the Web of Knowledge using the expression: Topic = (neuromorphic and memristor) OR Topic = (neuromorphic and RRAM) OR Topic = (brain-inspired and RRAM) OR Topic = (brain-inspired and PCM) OR Topic = (neuromorphic and PCM) OR Topic = (brain-inspired and memristor) OR Topic = (memristive synapse) OR Topic = (neuromorphic and phase change) OR Topic = (neuromorphic and resistive change).

capacity [12] while human brain occupies less space than 2 l (a large soda bottle) and consumes of the order of 10 W.

The computational performance of the biological brain has long attracted significant interest and resulted in inspirations in operating principles, algorithms and architectures. While brain-inspired or neuromorphic computation aims to mimic the parallelism and integration of memory and computation at the architectural level, building such massively parallel, three-dimensional, compact systems in hardware remains a substantial challenge due to the lack of a compact electronic device which mimics the biological synapse. Advances in neuroscience in the past 50 years have significantly improved our understanding of how neurons and synapses function and has revealed clues about how crucial synapses are to biological computations that underlie perception and learning. Synapses are 20–40 nm gap junctions permitting neurons to pass an electrical or chemical signal to another cell and they are the most abundant computation element in the brain. The ability to mimic the biological computation at the synaptic level will be a big step forward toward building massively parallel computational systems. Research on synaptic devices can readily capitalize on the advances in neuromorphic circuits field (initiated by Carver Mead [13], focusing on emulating the electrophysiological behavior of real neurons with analog/digital circuits) for realizing the integration of synaptic devices with neuron circuits.

In this paper, we focus on synaptic devices and summarize the important findings and applications published in recent years. We start with a brief description of synaptic plasticity and learning (section 2). The different synaptic device implementations are reviewed in section 3 with an emphasis on materials and switching mechanisms, which is followed by an analysis of the performance metrics in section 4. Finally we review targeted computing applications with synaptic devices (section 5). We limit this review to solid-state devices for the emulation of the synaptic functionalities and do not cover the literature on neuromorphic circuits [14].

2. Synaptic plasticity and learning

The human brain consists of $\sim 10^{11}$ neurons and an extremely large number of synapses, $\sim 10^{15}$, which act as a highly complex interconnection network among the neurons [15]. Neurons consist of a soma (cell body), dendrites (thin structures that arise from the cell body) and an axon (a long cellular extension that arises from the cell body). Neurons generate action potentials (spikes), with amplitudes of approximately 100 mV and durations in the range of 0.1–1 ms in their soma. The spikes propagate through the axon and are transmitted to the next neuron through the synapses. The synapses, which are 20–40 nm wide gaps between the axon end and the dendrites, transmit the signal either chemically by releasing neurotransmitters or electrically depending on the type of the synapse. Each neuron is connected through 1000–10 000 synapses with other neurons. Synaptic transmission is a complex process which starts with the opening of voltage-gated calcium ion channels as the action potential arrives. Ca^{+2} ions diffuse inside the neuron and cause synaptic vesicles to release neurotransmitters to the synaptic gap. Neurotransmitters diffuse through the synaptic gap and bind to the receptor sites of Na^{+} gated ion channels at the post-synaptic neuron, which causes them to open and allow the Na^{+} ions to diffuse inside the cell. The membrane potential of the post-synaptic neuron becomes more positive and if it reaches a threshold, the neuron fires an action potential. This spiking activity generated by neurons and transmitted through synapses is responsible for information flow and processing behind the complex computations performed by the brain.

Neurons and synapses are the two basic computational units in the brain. Neuron computation is performed by integrating the inputs coming from other neurons and generating spikes as a result. The synapses contribute to the computation by changing their connection strength as a result of neuronal activity, which is known as synaptic plasticity. Synaptic plasticity is the mechanism that is believed to underlie learning and memory of the biological brain [16]. The concept of synaptic plasticity has been heavily influenced by Hebb's postulate stating that the connection strength between neurons is modified based on neural activities in pre-synaptic and post-synaptic cells [17, 18] (figure 2(a)). In the late 1990s, a form of Hebbian learning, spike-timing-dependent plasticity (STDP), which focuses on the temporal order of spikes, emerged as a novel concept in cellular learning [19–21]. It attracted tremendous interest in both experimental and computational fields of neuroscience [22–25]. According to an asymmetric form of STDP, initially discovered by Bi and Poo in hippocampal cultures, plasticity or so-called synaptic weight depends on the relative timing of pre- and post-synaptic spikes.

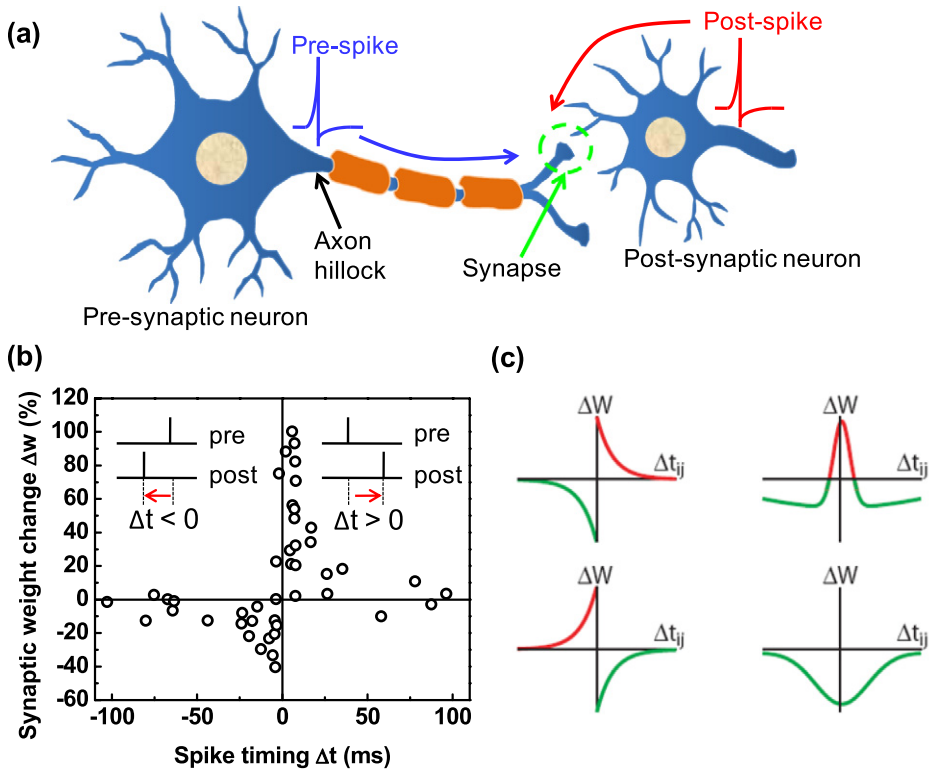

Figure 2. (a) Relative timings of neuronal spikes from the pre-synaptic neuron and the post-synaptic neuron determine the weight change in synapse. (b) Synaptic weight change is plotted as a function of relative timing of pre- and post-spikes. The data are adapted from STDP measurements in hippocampal glutamatergic synapses by Bi and Poo [19] (Reprinted with permission, copyright 1998 Journal of Neuroscience). (c) Diverse forms of STDP. Reprinted with permission from [30]. Copyright 2010 Frontiers.

The synapse potentiates (increases in synaptic weight or conductance) if a pre-synaptic spike precedes a post-synaptic spike repeatedly, and the synapse depresses (decreases in synaptic weight or conductance) if a post-synaptic spike precedes a pre-synaptic spike repeatedly. The original data from Bi and Poo's 1998 paper in figure 2(b) describes asymmetric STDP. If a pre-neuron spikes before a post-neuron ($\Delta t > 0$), the synaptic weight increases—in other words the synapse gets stronger (potentiation). The percentage increase in the synaptic weight is determined according to the value of timing difference between pre- and post-neurons's spiking times. A smaller spike timing difference results in a larger increase in synaptic weight. If post-neuron spikes before pre-neuron ($\Delta t < 0$), the synaptic weight decreases, which means that the synapse get weaker (depression). The precise pre/post-spike timing window, which controls the sign and magnitude of synaptic weight modification, is around 100 ms for biological synapses [19–21]. Different forms of STDP, which exhibit different temporal dependency on spike timing and order, have been measured by several groups [26–30] (figure 2(c)). STDP can be generalized as a mechanism which regulates the connection strength of neurons depending on their coactivity and spike timing. However, STDP is not the only form of synaptic plasticity and definitely not the only mechanism responsible for all the cellular-level computation in the brain [30]. Firing rate, spiking orders and dendritic location are some of the factors that greatly affect plasticity as well as specific cell and synapse type [31]. STDP has been measured *in vitro* and *in vivo* [18]. *In vivo* demonstrations have spanned a broad range of animals including insects, frogs, fish, rodents, cats and even humans. Preservation of timing sensitivity across many different species suggests that timing dependent plasticity plays a crucial role in synaptic computation. STDP is a temporally sensitive form of plasticity and certainly a novel paradigm that holds great promise for neuroscience and computational fields. Owing to its simplicity, biological plausibility and computational power, STDP has been widely used in computational neuroscience for pattern recognition, temporal sequence learning, coincidence detection, navigation, and direction selectivity. The important role of STDP in system-level biological computations remain as an exciting research field of neuroscience.

3. Synaptic device implementations

The interest in developing synapse-like electronic devices directed attention to material systems that have been investigated for nonvolatile memory technologies. A broad spectrum of device systems with programmable conductance inspired from already existing device technologies, such as phase change memory (PCM), resistive change memory (RRAM), conductive bridge type memory (CBRAM), ferroelectric switches, carbon nanotube devices, and three-terminal devices or FET (field effect transistor) based devices, have been explored. Different material systems or devices have strengths in various characteristics. What are the required

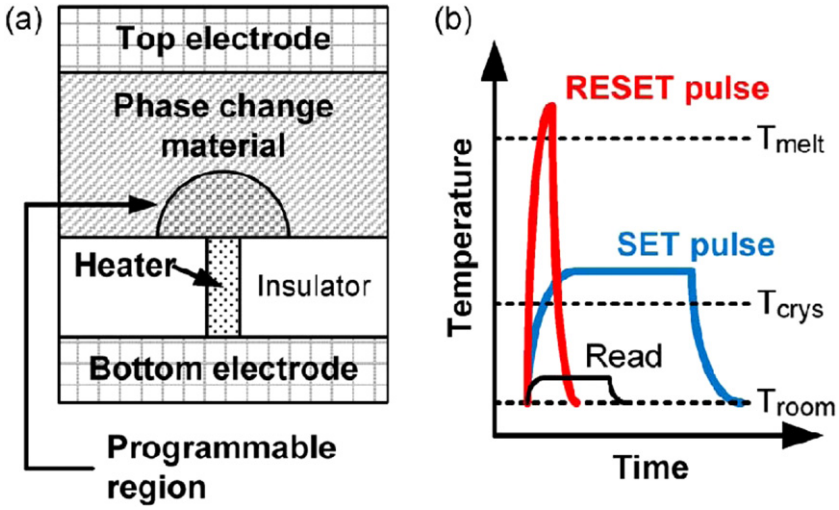

Figure 3. Cross-schematic of the conventional PCM cell. This is typically referred to as the mushroom cell. Current confined at the heater electrode and phase change material contact results in a mushroom-shaped programmed region. (b) PCM cells are programmed and read by applying electrical pulses which change temperature accordingly. Adapted with permission from [37]. Copyright 2010 IEEE.

characteristics for a synaptic device which will enable the development of brain-inspired systems technology that scales to biological levels of device density, parallelism and functionality? The synaptic device should be a simple two-terminal nanoscale device in order to reach brain-level parallelism and compactness. The main characteristics are the ones which are directly related to the parallelism, energy efficiency and fault tolerance. The synaptic device should emulate plasticity by implementing an analog-like transition between different conductance states with very low energy consumption per synaptic event. The exact performance metrics depend on the target application and the scale of the system design. In the following sections we will review the research efforts on synaptic devices, categorizing them according to their operation or dominant switching mechanism. Sections 3.1–3.4 will focus on passive synaptic devices, while section 3.5 will cover advances in FET-based active synaptic devices.

3.1. Phase change synaptic devices

Phase change materials have been intensively investigated for nonvolatile memory applications. Phase change materials offer several advantages such as scalability, reliability, endurance, multiple programming resistance levels and low device-to-device variation [32–36]. These properties enable the fabrication of industrial-scale arrays of the order of Gbits for nonvolatile memory applications. Phase change materials exhibit unique switching behavior between amorphous (high resistivity) and polycrystalline (low resistivity) states with the application of electric pulses that are large enough to generate the heat required for phase transformation. A commonly used device structure is shown in figure 3(a) [37]. Set and reset state of PCM refers to low and high resistance state, respectively. To reset the PCM cell into the amorphous phase, the programming region is first melted and then quenched rapidly by applying a large electrical current pulse for a short time period (figure 3(b)). To set the PCM cell into the polycrystalline phase, a medium electrical current pulse is applied to anneal the programming region at a temperature between the crystallization temperature and the melting temperature for a time period long enough to crystallize. Different from nonvolatile memory applications, fine control of resistance is required to emulate the analog-like behavior of biological synapses. Gradual programming of phase change synaptic devices has been demonstrated [38–41]. An order of magnitude change in the phase change cell resistance is achieved through 100 steps for both the set and reset transitions. Cross-sectional TEM analysis and simulations have revealed that modulation of the volume of the amorphous region leads to the formation of numerous intermediate resistance states [42]. Gradual set of the device resistance can also be implemented cumulatively by applying the same amplitude pulses. But gradual reset requires an increase in the amplitude to be able to continuously increase the cell resistance.

Several different spike schemes have been proposed to implement STDP with phase change synaptic devices (figure 4). The spike scheme translates the arrival timing relationship of the pre- and the post-spikes into programming pulses (amplitude, duration, and number of pulses) for the phase change synaptic device. The initial scheme proposed in [38] was a multi-pulse scheme, in which the pre-spike consists of set and reset pulses with changing amplitudes and the post-spike is a single pulse acting as gating function. The key idea of this scheme is to translate timing difference into pulse amplitude difference using the neuron circuitry. A single-pulse scheme described in [41, 43] addresses the weaknesses of a multi-pulse scheme, such as undesired programming and disturbance due to additional pulses and excess energy consumption associated with the charging of interconnect wires of a large-scale synapse array. The single-pulse scheme makes use of a communication signal between the pre-synaptic neuron and post-synaptic neuron and the timing of the spike is tracked by the neuron circuitry. Both

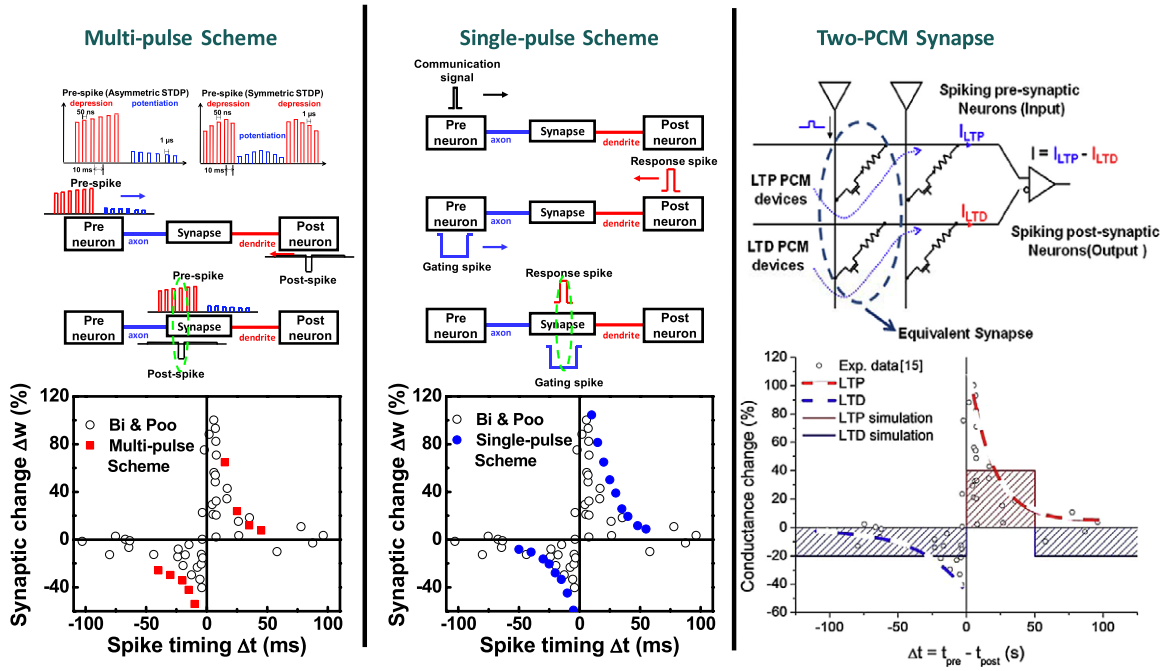

Figure 4. Multi-pulse scheme: the pre-spike consists of set and reset pulses with changing amplitudes and the post-spike is a single pulse acting as gating function. At the top, pre-spikes for asymmetric and symmetric STDP are shown. This scheme translates timing difference into the pulse amplitude and order difference. Depending on the timing difference, one of the set or reset pulses in the pre-spike overlaps with the post-spike, resulting in a change in synaptic weight. Single-pulse scheme: the single-pulse scheme makes use of a communication signal between the pre-synaptic neuron and post-synaptic neuron and the timing of the spike is tracked by the neuron circuitry. Whenever a neuron spikes, it sends a communication signal through its axon. A neuron which receives a communication signal, samples its internal potential and generates a response spike. The overlap of gating spike and response spike across the synapse results in synaptic weight change. Two-PCM synapse scheme: one PCM device (LTP) has a positive current contribution, while the other PCM device (LTD) contributes negatively toward the output CMOS neuron current. In the '2-PCM synapse', crystallizing the LTP PCM device produces a synaptic LTP-like effect, while crystallizing the LTD PCM device produces a synaptic LTD-like effect. The two-PCM synapse figures are reprinted with permission from [39]. Copyright 2011 IEEE.

types of scheme allow implementation of different forms of STDP by modulating the amplitude or the order of the pulses. A third scheme focuses on reducing energy consumption by using two PCM devices and trying to minimize the number of reset operations performed on the PCM [39]. The energy consumption in PCM is dominated by the high reset current required to melt-quench the phase change material to its amorphous phase. In this scheme, one of the PCM device implements synaptic long-term potentiation (LTP), while the other implements synaptic long-term depression (LTD). The contribution of the currents through the LTP device to the post-synaptic neuron is positive, while that of the LTD device is negative. Because the majority of the synaptic events are achieved by crystallization, this scheme promises lower power consumption for synaptic activity, although it occupies more area compared to a synaptic device based on a single PCM device. In order to choose the best STDP scheme, the tradeoff between the area and the energy consumption should be carefully examined for the specific target application and interconnect network. Arithmetic processes such as addition, multiplication, division and subtraction have been demonstrated by programming PCM devices optically [40]. The nonvolatility and the capability to program PCM cumulatively enables arithmetic computing as well as possible uses of PCM as integrate-and-fire neurons and synapses.

Different from the phase transformation from amorphous to polycrystalline state, a purely electronic form of transition from insulating to metallic state—Mott transition—can also be utilized to perform synaptic computation or neuron-like spiking activity. A research group from HP Labs has recently demonstrated biomimetic properties of neuristors using Mott memristors [44]. The neuristor is an electronic device inspired by the attenuationless signal propagation in the axon [45]. The memristor fabricated using NbO_2 exhibits a reversible insulator-to-metal phase transition when current is driven through the device to generate sufficient heat. The mechanism of the phase transition for a Mott memristor is different from the threshold switching and phase transition observed in phase change materials. A neuristor circuit consisting of Mott memristors, capacitors and resistors has been built to demonstrate neuron-like spiking behavior, which can be used as a basic building block for cellular neural networks [44].

3.2. Resistive change synaptic devices

Several resistive change materials have been employed as synaptic devices. The advantages that resistive change memory (RRAM) devices offer include great scalability, fast switching speed, satisfactory endurance and low energy consumption. A schematic of a simple metal–insulator–metal

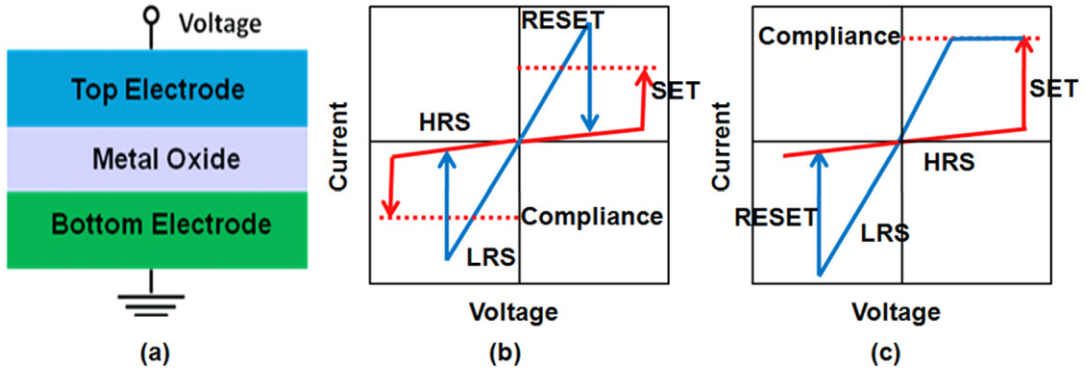

Figure 5. (a) Schematic of simple metal–insulator–metal structure used as RRAM or resistive change synaptic device. (b) Schematic of RRAM *I*–*V* curves, showing (b) unipolar and (c) bipolar modes of operation. Adapted with permission from [51]. Copyright 2012 IEEE.

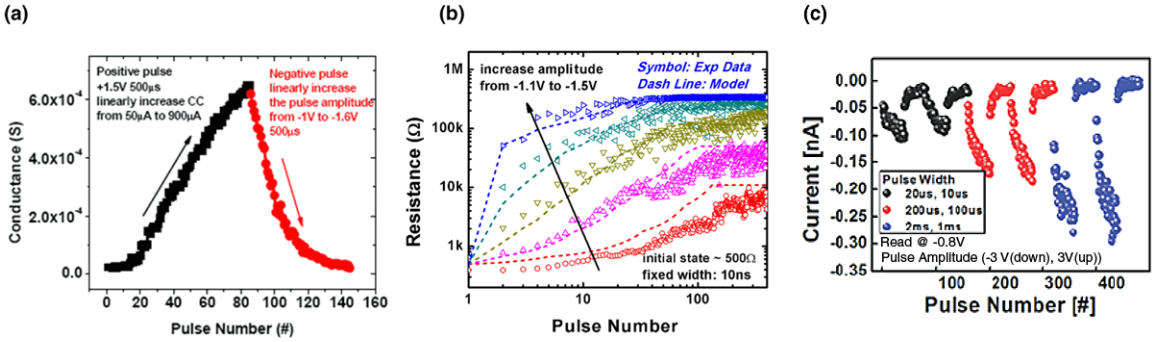

Figure 6. (a) AlO_x synaptic device. Gradual set of the device resistance is implemented by using pulses with increasing compliance current while gradual reset is implemented by increasing the negative pulse amplitude. Adapted with permission from [58]. Copyright 2012 IEEE. (b) TiO_x/HfO_x multi-layer synaptic device. Gradual reset starting from ∼500 Ω by varying pulse amplitudes. The dashed lines show the model. Adapted with permission from [59]. Copyright 2012 IEEE. (c) PCMO synaptic device. The continuous potentiating and depressing characteristics of the PCMO-based synaptic device for different pulse widths. Reprinted with permission from [60]. Copyright 2012 IEEE.

structure for metal oxide RRAM is shown in figure 5. RRAM devices can have two modes of operation: (a) unipolar and (b) bipolar. The switching mechanism of RRAM strongly depends on the oxide materials, the choice of metal electrodes and their interfacial properties. Hence, RRAM devices exhibit a variety of different switching mechanisms, which have been discussed in the literature [46–52] thoroughly. Here we will briefly discuss metal oxide RRAM, also known as anion-based resistive switching devices in some publications. Conductive bridge memory, also known as cation-based resistive switching devices in some publications, will be covered separately in section 3.3. An oft-cited switching mechanism in RRAM is filamentary switching. The set process from high resistance state to low resistance state is attributed to the dielectric soft breakdown and creation of conductive filaments, usually consisting of oxygen vacancies. The reset process from low resistance state to high resistance state is attributed to the rupture of the conductive filament, usually by recombination of oxygen vacancies with oxygen ions migrated from the electrode/oxide interfacial reservoir. The migration of oxygen ions is mainly electric field assisted. The gap distance between the conductive filament and the electrode determines the device resistance. Gradual set and reset are achieved by growth and dissolution of the conductive filament. Synaptic devices based on GdO_x/Cu:MoO_x [53], TiO_x [54], WO_x [55, 56], HfO_x [57], AlO_x [58], TiO_x/HfO_x multi-layers [59] and PCMO [60] have been reported. Gradual set/reset, programming time scale, gradual programming technique, switching mechanisms and relative STDP weight change characteristics of those synaptic devices are summarized in table 1. Due to the stochastic nature of filamentary switching, abrupt set or reset transitions are observed in most of the devices. Figure 6 shows several examples of gradual programming of resistive synaptic devices. While AlO_x synaptic devices perform very gradual and smooth transition between intermediate resistance states (figure 6(a)), the use of compliance current to control gradual programming can be difficult to implement in crossbar synaptic arrays. Use of $TiO_x/HfO_x/TiO_x/HfO_x$ multi-layer RRAM stacks enables more gradual and smooth reset switching (figure 6(b)) for synaptic devices as reported in [59]. For the resistive materials, which switch through the formation of conductive filaments, abrupt set or reset transitions are observed depending on the applied pulse width. Alibart *et al* has shown that program-verify algorithms can be used to tune device resistance at a specific bias point to within 1% relative accuracy of the dynamic range [61]. STDP has been implemented in HfO_x [57], AlO_x [58] and PCMO [60] synaptic devices using different pulse schemes (figure 7).

In addition to timing-based plasticity, two groups have utilized the short retention of the devices to illustrate short-term memory (STM) in synaptic devices, inspired

Table 1. Synaptic devices built with various resistive change materials. Size, gradual set/reset, programming time scale, gradual programming technique, switching mechanisms and relative STDP weight change characteristics of the synaptic devices are summarized along with references to the publications.

Material	Size	Gradual set	Gradual reset	Programming time scale	Gradual programming method	Switching mechanism	Relative STDP weight change
GdO_x/Cu:MoO_x [52]	100 nm	✓	×	N/A	DC sweep	Non-filamentary	N/A
TiO_x [53]	250 nm	✓	✓	10 ms	Identical pulses or varying pulse width	Non-filamentary	∼−8% to +16%
WO_x [54, 55]	130 nm [54]	✓	×	0.3–1 ms	Identical pulses [54]	Filamentary [54]	N/A
	25 μm [55]	✓	✓	0.1 ms	Varying amplitude [55]	Filamentary [55]	N/A
HfO_x/AlO_x [56]	0.5 μm	✓	✓	50 ns	Varying amplitude	Filamentary	∼−100% to +400%
AlO_x [57]	0.48 μm	✓	✓	500 μs	Varying amplitude and compliance current	Filamentary	∼−100% to +350%
TiO_x/HfO_x multi-layers [58]	5 μm	×	✓	10 ns	Identical pulses	Filamentary	N/A
PCMO [59]	150 nm–1 μm	✓	✓	10 μs–1 ms	Identical pulses or varying pulse amplitude and width	Filamentary [43]	∼−120% to +120%

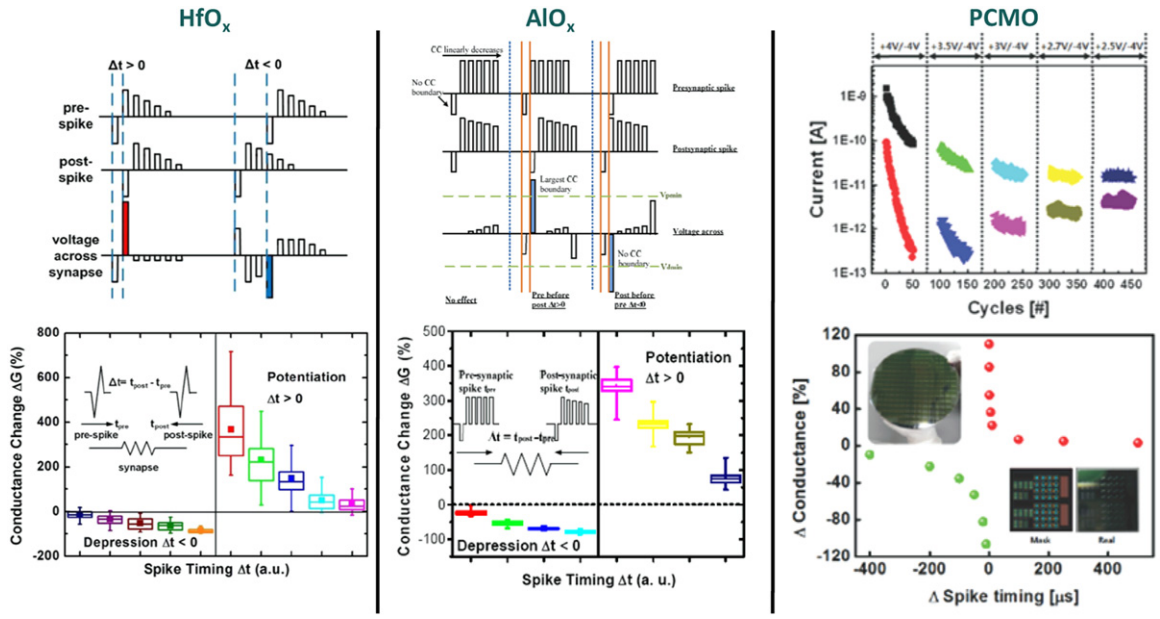

Figure 7. HfO_x/AlO_x: STDP realization schemes developed with time-division multiplexing and pulse amplitude modulation. The pulse amplitudes for the pre-spike are −1.4, 1, 0.9, 0.8, 0.7, and 0.6 V, consecutively, and for the post-spike, they are −1, 1.4, 1.3, 1.2, 1.1, and 1 V, consecutively. An STDP-like curve is constructed using the data from [57] and by employing the signal schemes explained above. Adapted with permission from [57]. Copyright 2011 IEEE. AlO_x: in STDP realization scheme schematic, V_{pmin} and V_{dmin} are the minimum voltage amplitudes which induce potentiation and depression, respectively. Only the blue-shaded pulses beyond V_{pmin} or V_{dmin} could actually change the resistance of memory device. STDP-like curve constructed using with the resistance modulation data in [58] employing the above signal scheme. Potentiation is based on data using compliance current levels to control resistance and depression is based on data using RESET stop voltages modulate conductance. Adapted with permission from [58]. Copyright 2012 IEEE. PCMO: modulation of the resistance difference between high resistance state and low resistance state by simply changing VSET_max and VRESET_max. ($V_{read} = -1$ V). The lower figure shows the STDP characteristics of the 1 k-bit RRAM array. Inset shows the 8 in wafer (left, top) and photoimages of mask and real 1 k-bit RRAM array. Reprinted with permission from [60]. Copyright 2012 IEEE.

from the biological forgetting process. Chang *et al* studied the short-term to long-term memory (LTM) transition in a $W/WO_x/Pd$ synaptic device [55]. Memory retention exhibits two regimes; one is a few seconds long while the other lasts only minutes, which is considerably shorter than required to be accounted as nonvolatile LTM. They also observed a clear dependence on the stimulation rate. Yang *et al* [56] studied the mechanisms behind LTM and STM in $Pt/WO_{3-x}/Pt$ synaptic devices and reported that volatile and nonvolatile rectifications and bipolar resistance switching can be achieved by controlling the local migration of oxygen vacancies in the same device. However, to date, back and forth switching between LTM and STM does not seem feasible due to the need for the irreversible formation process to operate in nonvolatile bipolar resistive switching mode. Operation time scales of both nonvolatile and volatile states and retention characteristics need to be in accordance with the time scales of biological LTM and STM. Retention requirements for LTM will be further discussed in section 4.

Among many different candidates for synaptic electronics, resistive change synaptic devices are attractive mainly due to their relatively lower energy consumption. Sub-pJ level energy consumption per synaptic event has been recently demonstrated [59]. Extremely scaled crossbar RRAM with an area of less than 10×10 nm^2 and with a switching energy per bit of <0.1 pJ [62] shows promise for future large-scale RRAM synaptic arrays.

3.3. Conductive bridge synaptic devices

Conductive bridge memory is another type of resistance change memory which relies on fast ion diffusion. Fast diffusive ions such as Ag^+ and Cu^{2+} migrate into the insulating medium materials to form a conductive bridge [63]. The insulating medium can be chalcogenide [64, 65], oxide [66, 67], amorphous silicon [68], or amorphous carbon [69]. Conductive bridge memory shares many of the attributes of metal oxide RRAM, and it has been utilized to act as synaptic devices. Jo *et al* reported a Ag/a–Si/W-based synaptic device [70]. It shows a gradual increase and decrease of conductance by applying identical pulses (figure 8(a)), which mimics the biological potentiation and depression of the synaptic strength. The capability to gradually increase and decrease of the device conductance is maintained after 1.5×10^8 pulse cycles (figure 8(b)), although there is a slight degradation in terms of the shift of the mean conductance and the reduced number of intermediate resistance states. Furthermore, a pulse-width modulation scheme was designed to implement the STDP learning rule on this type of synaptic device. The same group later integrated their synaptic devices in a crossbar fashion with the CMOS circuitry to function as a hybrid system [71]. Ohno *et al* reported a Ag/Ag_2S/nanogap/Pt synaptic device [72], which shows a transition from STM to LTM depending on the stimulus pulse intervals. If the intervals are large enough, the device

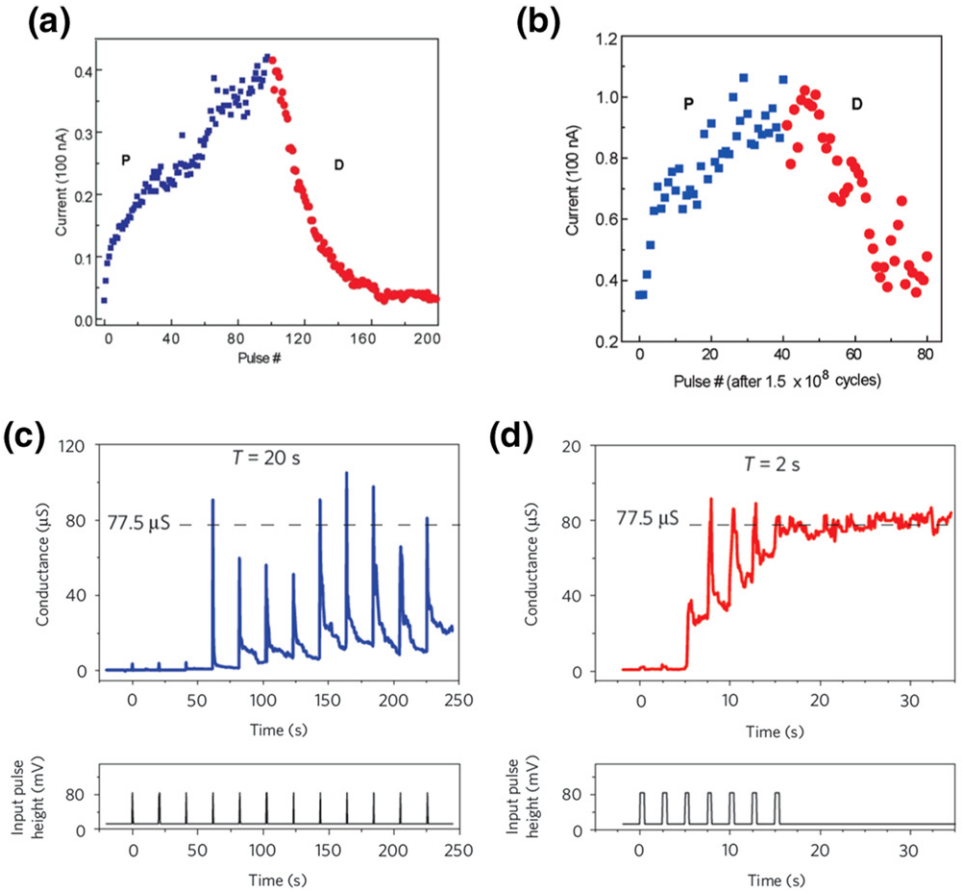

Figure 8. (a) Ag/a–Si/W synaptic device. The device conductance is incrementally increased or decreased by consecutive potentiating or depressing pulses. The conductance was measured at 1 V after each pulse and the read current is plotted. Potentiation pulses: 3.2 V, 300 μs, depression pulses: −2.8 V, 300 μs. Reprinted with permission from [70]. Copyright 2010 American Chemical Society. (b) After 1.5×10^8 potentiation/depression pulses. Potentiation pulses: 3.1 V, 800 μs, depression pulses: −2.9 V, 800 μs. Reprinted with permission from [70]. Copyright 2010 American Chemical Society. (c) Ag/Ag_2S/nanogap/Pt synaptic device. Change in the conductance of the nanogap synaptic device when the input pulses ($V = 80$ mV, $W = 0.5$ s) were applied with intervals of (c) 20 s and (d) 2 s. Reprinted with permission from [72]. Copyright 2011 Nature Publishing Group.

conductance decays (figure 8(c)); if the intervals are small enough, the device conductance remains at a high level (figure 8(d)). The same group later reported similar synaptic behavior in a Cu/Cu_2S/nanogap/Pt synaptic device [73]. Suri *et al* reported a $Ag/GeS_2/W$ synaptic device [74] that has a abrupt set transition—which is essentially a binary synapse. However, it was found that the set transition becomes probabilistic under a weak programming condition. With such probabilistic learning rule, this device is suitable for auditory and visual cognitive processing applications as demonstrated by a large-scale simulation. Generally, the conductive bridge synaptic devices can naturally mimic many features of the biological synapses since they have very similar operation principle: by release of ions into the junctions.

3.4. Ferroelectric synaptic devices

Ferroelectric materials are one of the earliest materials investigated for synaptic applications [75]. In 1999, Yoon *et al* demonstrated a modifiable synapse array with metal–ferroelectric–semiconductor FETs using $SrBi_2Ta_2O_9$ (SBT) films in the gate [76]. A three-FET configuration which shows hysteretic characteristics due to the ferroelectricity of the SBT gate is used to perform a weighted sum operation. Polarization of the ferroelectric film can be gradually changed either by applying multiple pulses with the same amplitude or by changing the write pulse amplitude. Although three-terminal FET devices have been intensively investigated for logic and memory applications, two-terminal device configurations are preferred for synaptic electronics because they offer higher device density. Recent work has investigated voltage-controlled domain configurations in ferroelectric tunnel barriers [77]. A two-terminal ferroelectric device composed of $BaTiO_3/La_{0.67}Sr_{0.33}MnO_3$ was used to implement synaptic devices. In tunnel junctions with a ferroelectric barrier, switching of the ferroelectric polarization modulates the tunnel resistance. Chanthbouala *et al* reported that the domain configuration of a ferroelectric tunnel barrier can be controlled to produce gradual switching between ON and OFF states [77]. Amplitude, duration or pulse number modulation can be used to implement a gradual resistance change. In figure 9, the resistance level of the ferroelectric tunnel junction is set by applying different

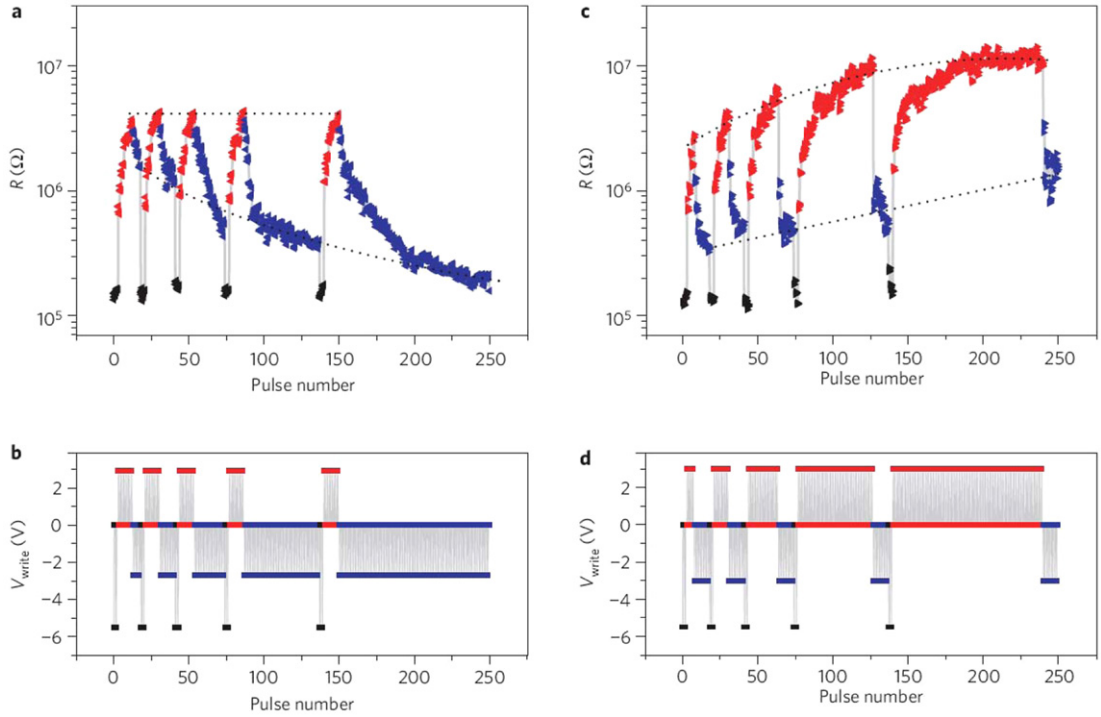

Figure 9. Ferroelectric synaptic device resistance is gradually programmed by consecutive identical pulses. Different voltage pulse sequences are shown in (b) and (d). Junction resistance modulation is shown in (a) and (c) as a function of different voltage pulse sequences in (b) and (d). In (b), write pulse amplitudes are +2.9 V and −2.7 V, and in (d), +3 V and −3 V, respectively. In (a) and (b), the number of consecutive positive pulses is fixed to 10. As seen in (a), the number of negative pulses applied subsequently determines the final resistance. In (c) and (d), the number of negative pulses is fixed. The gradual resistance increase with the number of positive pulses confirms the cumulative effects. Reprinted with permission from [77]. Copyright 2012 Nature Publishing Group.

voltage pulse sequences, which allows synaptic weight modification through STDP using a suitable pulse scheme that translates the spike timing differences into programming pulse sequences. Further investigations on domain size scaling and switching dynamics will help to better understand the scalability of the ferroelectric synaptic devices.

3.5. FET-based synaptic devices

As CMOS scaling has started to face significant barriers in achieving further performance gains, an alternative approach using FET-based devices in neuromorphic architectures has been pursued. One of the first FET-based synapses was proposed by Carver Mead, developer of the neuromorphic computing concept, in 1996 [78]. A floating gate silicon MOS transistor, programmed through hot-electron injection and electron tunneling, is used for analog learning applications. Mead and co-workers demonstrated a learning system with a 2 × 2 synaptic array, in which individual array nodes can be addressed with good selectivity. They have characterized a synapse learning rule, targeted for an autonomous learning system, combining single-transistor analog computation with memory updates computed both locally and in parallel with these synapses.

FET-based synapse and neuron circuits using single or multiple carbon nanotubes have been proposed by several groups with different architectures and target applications [79–81]. A carbon nanotube synapse circuit mainly focusing on generating post-synaptic potentials in response to applied action potentials has been demonstrated [79]. Accumulation and trapping of photogenerated carriers at the nanotube/dielectric interface has been utilized to achieve nonvolatile memory effect which is controlled by applying voltage pulses to source terminals [80]. A global optical write, which sets all the devices resistances to a minimum resistance value, is followed by programming of individual devices by electrical programming in order to implement a weighted sum operation in a four synaptic device circuit. Chen *et al* presented a spiking neuron circuit in a crossbar architecture, which integrates post-synaptic currents to trigger output spikes, similar to the integrate-and-fire mechanism in biological neurons [81]. While all these demonstrations with CNT-based FETs seem very interesting, the issues related to large-scale integration and controlled fabrication remain to be addressed for future large-scale computing applications.

Another material system studied for synaptic plasticity in the FET context is nanoparticle–organic molecule composites. Alibart *et al* demonstrated potentiation and depression type synaptic behaviors in nanoparticle–organic field effect transistors (NOMFETs) [82]. Gold nanoparticles embedded in pentacene are used as the channel of the transistor resulting in a leaky memory behavior with retention times in the range of seconds to a few thousand seconds. The charge storage capacity of the nanoparticles and the amplification factor of the organic transistor are exploited to mimic short-term plasticity due to short retention times. STDP has

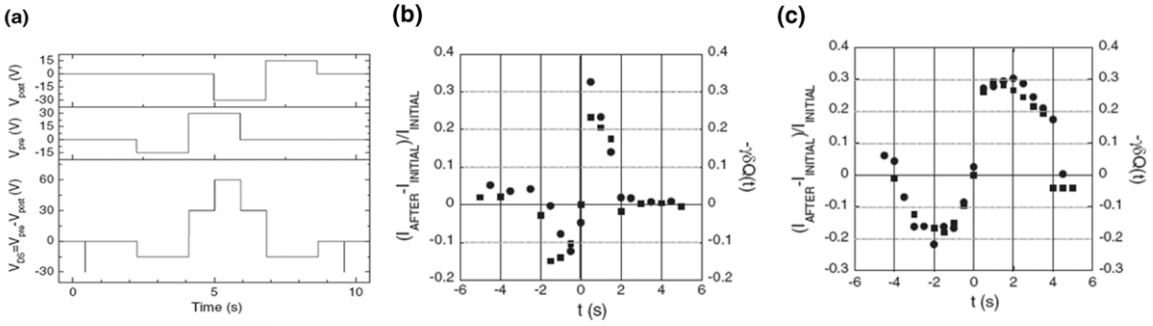

Figure 10. (a) Pre- and post-spikes' superposition and effective potential across synapse. (b) STDP obtained with triangle-shaped pulses. (c) STDP obtained with square-shaped pulses. Reprinted with permission from [83]. Copyright 2012 John Wiley and Sons.

also been demonstrated by Alibart *et al* using the NOMFET structure [83], implementing the pre- and post-spike schemes proposed in [84] (figure 10(a)). In addition to asymmetric STDP, the most common form studied in the literature, they have modulated the shape of the STDP learning window by changing the shape of the pulses in pre-spike and post-spike (figures 10(b) and (c)). Lai *et al* integrated an $RbAg_4I_5$ ionic conductor layer and ion-doped MEH-PPV conjugated polymer layer onto the gate of a Si-based MOSFET to emulate the dynamic modulation of synaptic weights [85]. Temporally correlated pre- and post-spikes are shown to modify the ionic charges in the polymer, leading to STDP implementation. Furthermore, synaptic plasticity has been demonstrated using synapses consisting of silicon TFTs and memristors [86].

4. Performance metrics

The interest in building large-scale neuromorphic systems using synaptic devices has guided the device community to make significant progress in developing synaptic devices mimicking the key characteristics of biological synapses. However, a clear understanding of the operating conditions and performance metrics remains lacking, mainly due to the diversity of the targeted application space. In this section, we cover some general characteristics for synaptic devices which are desirable for most of the applications. It is important to emphasize the difficulty in defining generalized metrics for synaptic devices because the application space for synaptic devices is very broad, as will be explained in section 5. In order to evaluate different synaptic device characteristics, a rule of thumb can be scalability to biological levels. An ideal synaptic device should have characteristics such as size, energy consumption, operation frequency, which are scalable to biological levels. The analysis below is presented with that perspective in mind.

(1) *Synaptic device dimensions*: Two-terminal structures which will enable 3D integration and potential scalability to the nanometer regime are one of the key guiding principles of synaptic devices research. The density of synapses in human cortex is $> \sim 10^9$ mm^{-3} and the physical size of the synaptic cleft is $< \sim 20$ nm [16]. Among different synaptic candidates, PCM and RRAM have shown sub-10 nm devices functioning as a memory device [62, 87], which makes them advantageous for massively parallel architectures. CBRAM, in principle, could be scaled down to sub-10 nm, as long as the metallic filament diameter is thinner than 10 nm. However, a sub-10 nm CBRAM device has not been experimentally demonstrated yet. Three-terminal FET-based synaptic devices are expected to follow similar scaling trends with CMOS technology. While ferroelectric materials promise high switching speeds and low power, scaling to sub-100 nm has remained as the biggest challenge for nonvolatile memory applications, mainly because the available signal decreases with the cell area. For many applications, synaptic devices need to exhibit multi-level resistance states, unless a stochastic binary switching mechanism is utilized. Maintaining multi-level states while scaling the device dimensions is one of the critical points to be considered in designing systems.

(2) *Energy consumption*: Among all performance metrics, energy consumption is the most challenging and probably the most difficult to realize considering the need for energy efficient brain-inspired computational systems in the future. An order of magnitude calculation can be done to estimate energy consumption per synaptic event in the brain. There are approximately 10^{13} neurons and 10^{15} synapses in brain [15] and only 1% of them is active at the same time [88]. Neurons produce spikes with a frequency of 10 Hz. Total power consumption of human brain is ~20 W. If we assume that the total power consumed by synapses is of the order of 10 W (with the rest of the power consumption taken up by the interconnection network and the neurons), then the power consumption per synaptic event can be estimated to be 10^{-13} W. Each synaptic event has duration of ~100 ms, leading to an energy consumption requirement per synaptic event of 10 fJ. If one targets a system consisting of 10^{12} synapses, the synapse energy consumption requirement can be stretched to 10 pJ. The synaptic energy consumption per programming can be calculated by multiplying the pulse amplitude with the current flowing across the device at each time point ($dE = V \times I_{prog} \times dt$) and taking an integral over time; alternatively a simple estimate can be made by multiplying the pulse amplitude with the current flowing across the device and the programming pulse width. In order to minimize synaptic energy consumption all three components—programming current, pulse amplitude and programming time—need to be minimized. In RRAM, an exponential voltage–time relationship is commonly observed. A small increase in programming voltage will decrease

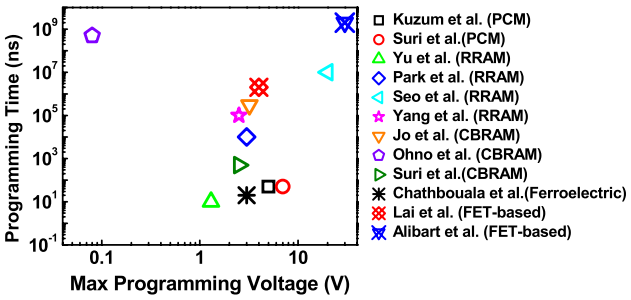

Figure 11. Programming times versus maximum programming voltage for the synaptic devices reported in the references shown in the legend.

programming time exponentially. Hence, low programming energy is obtained by minimizing the programming time (traded off by increasing the pulse amplitude slightly) for RRAM.

Some of the devices (PCM and RRAM) covered in section 3 have already shown pJ level energy consumptions. Further decrease in synaptic energy consumption to fJ levels will be challenging but important to build very large-scale systems. Minimizing the total power consumption by other components such as neurons and interconnects is as crucial as reducing the synaptic dissipation.

(3) *Operating speed/programming time*: While today's CMOS technology offers operation frequency in the range of GHz, the key advantage of brain-inspired computational systems is its computational efficiency through parallelism. By using ms long spikes and an average frequency of 10 Hz, human brain can easily process very complex tasks such as real-time visual processing, while digital computers based on devices operating at GHz cannot approach the brain's performance on such tasks. The operating speed of the brain is suitable to maintain low power consumption while exploiting parallelism in computing. As an illustration of the tradeoff between energy and operating speed (assuming that energy consumed per synaptic operation is fixed and a higher computational throughput is not required), an operation frequency of 10 MHz instead of 10 Hz would cause the brain to run on 20 MW instead of 20 W and the biological brain would have never existed in such a compact space. Therefore, the tradeoff between the operation speed and the energy consumption should always be carefully considered, especially if higher computational throughput than human brain is targeted in future. The biological operation frequency does not constitute a challenge for synaptic devices. Most of the synaptic device candidates can already operate faster than that. Programming time shorter than ms is enough to implement synaptic plasticity. Figure 11 shows programming time versus maximum operating voltage for some of the synaptic devices published in the literature. The programming time scale for the synaptic devices spans a broad range, from nanoseconds to seconds, resulting in orders of magnitude difference in the synaptic energy consumption. A fruitful area of research is the development of plasticity schemes for synaptic devices with ns or μs programming times to compensate for the timing discrepancy between the programming pulse width and the STDP window [38, 43], while keeping the synaptic energy consumption as low as possible.

(4) *Multi-level states*: Synaptic plasticity characteristics measured on biological synapses show an analog-like behavior with numerous synaptic weight states between the highest and the lowest conductances [19]. The Darpa Synapse program requirement of 1% control of synaptic conductance per synaptic activity has set the bar very high for implementing multi-level states with synaptic devices. The motivation behind this metric could be a mimicking of the cumulative nature of weight change in biological synapses. In most of the biological studies, about 60–100 pre/post-spike pairs are repeatedly applied for several minutes to induce long-term potentiation or long-term depression. The number of pairing events required to cause a certain amount of potentiation or depression shows substantial variation depending on the type and location of synapses. For instance in the optic tectum of the tadpole *in vivo*, while a moderate amount of LTP was induced after 20 pre/post-spike pairs, maximum LTP was reached after 80–200 pre/post-spike pairs [20]. On the other hand, in the cortex, 15 or fewer pre/post-spike pairs was shown to induce a high level of LTP [89]. Therefore, it is difficult to specify the required number of multi-level states by looking at biological examples, simply because of the variety in biology. Besides, because some of the proposed synaptic devices function by filamentary switching, gradual control of conductance states is extremely difficult in those cases. It has been proposed that multi-level deterministic synapses and binary probabilistic synapses would be functionally equivalent at the system level [90], which has been recently confirmed by simulations with conductive bridge synaptic devices [74]. While more multi-level states are known to bring advantages in terms of network capacity and robustness, the precise requirement for the number of conductance states remains application specific and deserves more attention by the research community.

(5) *Dynamic range*: In the synaptic device context, dynamic range can be described as the maximum resistance (conductance) ratio between the highest-resistance state and the lowest-resistance state. An electronic analog of a biological synapse, which exhibit plasticity, needs to perform a cumulative weight change with a maximum of 100% and a minimum −50% [19–21], which translates into a minimum dynamic range of 4 for the synaptic device conductance. Hence, a dynamic range of 10 is more than sufficient to implement biological plasticity. Most of the synaptic device candidates exhibit a wider programmable resistance range, which provides flexibility in choosing the operation regime. For phase change synaptic devices, operation in the low-resistance state regime has been found to be more energy efficient [43]. On the other hand, for resistive change synaptic devices the high-resistance regime is more energy efficient [59]. Additionally, high resistance is useful for minimizing the read energy, and also helps to reduce the neuron capacitor area. When I&F neuron sums the current from hundreds of synapses, the total current charges the membrane capacitor of the neuron. A high summated current will require a larger capacitor and the neuron circuitry will

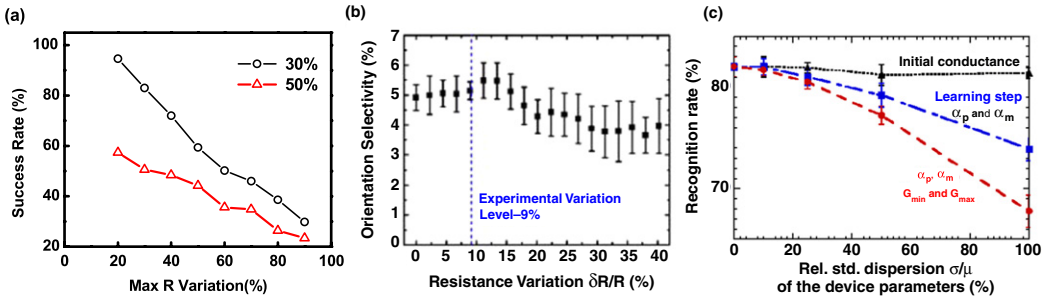

Figure 12. (a) Success rate for recalls is plotted as a function device resistance variation for 30% incomplete pattern and 50% incomplete pattern. The cell resistance is randomly chosen from a distribution with a maximum variation in the range of 20%–90%. At each variation value, the simulation is repeated 25 times. (b) Simulated orientation selectivity versus RRAM variability. At each error bar, 20 independent simulations are carried out. Experimental RRAM variability is ∼9%. Adapted with permission from [59]. Copyright 2012 IEEE. (c) Effect of variation in initial device conductances, learning step increment and decrements, and maximum and minimum conductance values. All the simulations were repeated ten times, the error bar is one standard deviation. Variation in initial conductance does not have a significant effect in recognition rate. The most variation-sensitive parameter is maximum conductance, as shown with the red dash line. Source: D. Querlioz. Reprinted with permission.

occupy a significantly large chip area. Moreover, the spikes used to program synaptic devices need to be kept low (<1 V) to minimize the energy consumption by the devices and the interconnects and reduce the circuit design complexity.

(6) *Retention for LTP and LTD and endurance*: Human memory or simpler forms of network-based memory is a system-level property which does not need to be reflected in the plasticity properties of individual devices. However, the retention of memory appears to require a certain stability of the underlying plasticity of the individual synapses in the network. Although studies have shown that long-term potentiation has the capacity to underlie memories ranging from short term to very long term [91], our understanding of synaptic plasticity and structural plasticity is at a very early stage to clarify the link. The studies on the dentate gyrus part of the hippocampus have shown that long-term potentiation can either be decremental, lasting from hours to weeks, or stable, lasting months or longer [91]. Ultimately, it can be argued that LTP and LTD need to have a retention capacity of the order of 10 years, to enable formation of life-long memories and to maintain them for long periods of time.

Determining the required endurance characteristics of biological synapses is a difficult task to experimentally perform on biological subjects since it requires extensive stimulation and recording of a single biological neuron, which needs to be alive during the course of the experiment. Alternatively, hardware implementation of synaptic networks require some level of endurance against persistent neural spiking activity in the network. It is envisioned that an endurance of 3×10^9 synaptic operations would guarantee 10 years of lifetime with 10 Hz operation frequency. Most of the work published on synaptic devices has not given enough attention to the retention and endurance characteristics for LTP and LTD. However, they will be key parameters to benchmark which synaptic device candidate is best for building large-scale brain-inspired systems.

(7) *Uniformity and variation*: Poor uniformity and variation in device characteristics is a major barrier to introducing novel nanoscale devices to CMOS or memory applications. In contrast, brain-inspired or neuromorphic architectures promise immunity against device variations. The level of variation that can be tolerated in the system level strongly depends on the network architecture and the accuracy required by the target application. Several groups have studied robustness against device variations in different neural networks through simulations [43, 59, 92]. Kuzum *et al* have shown that for pattern completion via associative recall, the success rate significantly decreases as the variation in device resistance is increased (figure 12(a)) [43]. But 30% variation in device resistance can still be tolerated with a success rate above 80%. Yu *et al* reported that there is no degradation in the system performance of a visual system constructed resistive change synapses when the measured experimental variability level (∼9%) is introduced to simulations (figure 12(b)) [59]. Querlioz *et al* studied the effect of variation in initial device conductances, learning step increment and decrements, and maximum and minimum conductance values [92, 93]. They demonstrated that an unsupervised digit recognition task can be successfully performed even in the presence of significant variation in nanodevice parameters (figure 12(c)). Because the level of variation that can be tolerated is a parameter that strongly depends on the characteristics of the neural network, we will not specify a maximum level in this review. Nevertheless, it is important to emphasize that variation levels that are not acceptable for CMOS or memory applications can easily be tolerated for neural applications with synaptic devices.

Table 2 summarizes the desirable performance metrics for synaptic devices.

5. Targeted computing applications with synaptic devices

The recent experimental demonstrations of synaptic devices have directed attention to potential computing applications and neuromorphic computational architectures. Such artificial neural-inspired systems built with synaptic devices could provide a suitable platform for a broad range of computing applications. Examples include, but are not limited to,

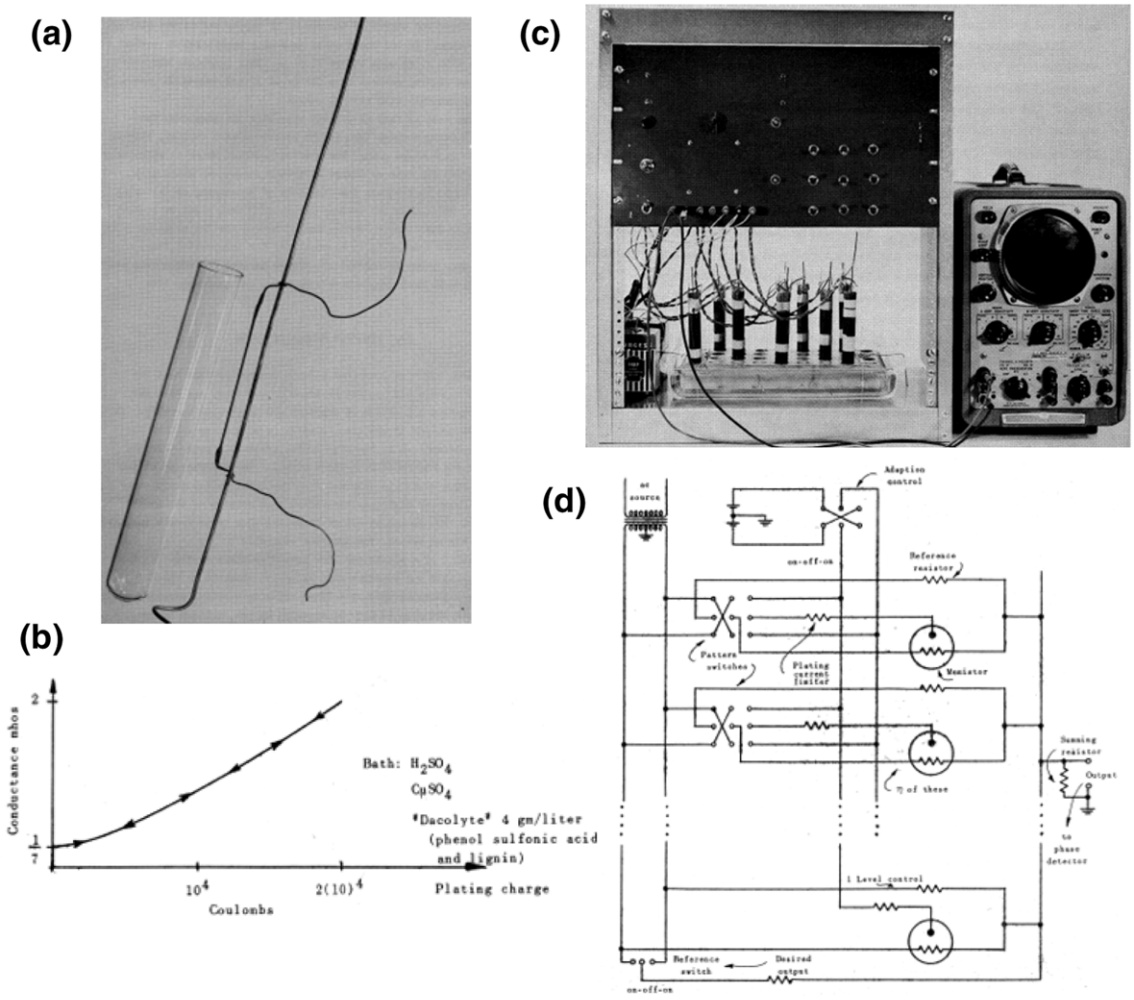

Figure 13. (a) Pencil-lead memistor element, (b) conductance modulation of memistor, (c) 3 × 3 memistor neuron built by Widrow and Hoff, (d) memistor ADALINE circuit. All figures are adapted with permission from [99].

Table 2. Desirable performance metrics for synaptic devices.

Performance metrics	Targets
Device dimensions	<20 nm × 20 nm
Energy consumption	<10 fJ
Operating speed/programming time	~10 Hz/<1 ms
Multi-level states	20–100
Dynamic range	>4
Retention/endurance (for LTP and LTD)	~10 years/3×10^9 synaptic activity

bio-inspired learning (associative and sequence) [42, 94], arithmetic computing [40, 94], pattern completion [95], real-time auditory and visual pattern extraction [84], edge detection [96], solving mazes [97], finding shortest paths, autonomous navigation, game players and even use in accelerators for heterogeneous multicores [98].

First implementations of learning in hardware were proposed in early 1960s. Bernard Widrow from Stanford University and his graduate student Ted Hoff developed the first hardware implementation of an artificial neural network, ADALINE (ADAptive LInear NEuron), consisting of 'memistors' (memory with resistors) [1, 99]. The memistor is a variable resistor which uses the electroplating phenomenon to control resistance by depositing metal on a resistive substrate (figures 13(a) and (b)). The ADALINE system with configurable memistors functions as a pattern classification machine, which learns from experiences (figures 13(c) and (d)). During the training, seven different patterns were fed into a 3 × 3 neuron circuit and the memistor resistances were modulated accordingly. The input patterns were successfully classified into one of the two associated outputs, with a better speed of convergence than the manual ADALINE system. Five years later, Karl Steinbuch constructed an associative learning memory by physically building contact points between silver and silver bromide and called it the 'Learning Matrix' [2].

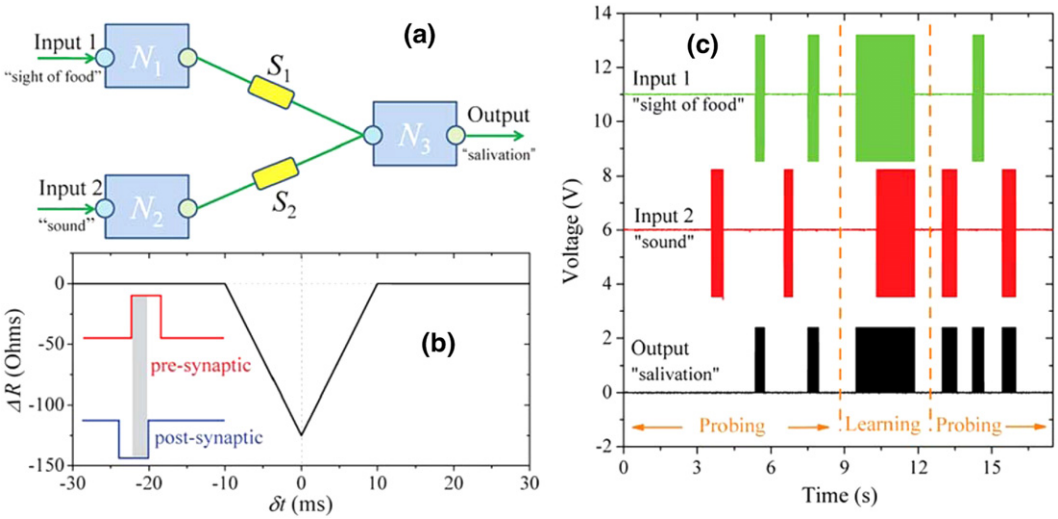

Figure 14. (a) A simple neural network containing three electronic neurons (N1, N2, and N3) connected by two memristive synapses. (b) Change in memristance induced by a pair of square pulses of opposite polarity applied to terminals of a first-order memristive system. The gray rectangle designates the time window in which the memristance change occurs. (c) Experimental demonstration of the associative memory with memristive neural networks. A simple neural network shown in (a) was realized. The first 'probing' phase demonstrates that, initially, only a signal from N1 neuron activates the output neuron. The association of the input 2 signal with the output develops in the 'learning phase' when N1 and N2 neurons are simultaneously activated. In this case, a signal at the input 1 excites the third neuron that sends back propagating pulses of a negative amplitude. These pulses, when applied simultaneously with forward propagating pulses from the input 2 to the second memristive synapse S2 cause it to learn. The final 'probing' phase demonstrates that signals from both N1 and N2 activate the output neuron. Reprinted with permission from [103]. Copyright 2010 Elsevier.

These early inspirational examples of hardware implementations of neural networks have presaged research for miniaturizing and scaling of synaptic devices using the advances in device technologies. A significant part of recent interest in applications with synaptic devices has come from the memristor community, starting with Greg Snider's paper on STDP with memristive devices in 2008 [100]. The simplicity and compactness of models developed for memristive devices has quickly led into array-level simulations of synaptic networks. Various learning algorithms that can be implemented in hardware have now been studied [101, 102].

Some of the research on computing applications with synaptic devices has focused on brain-inspired architectures and algorithms. Brain-like associative learning, sequence learning and pattern completion have been implemented with synaptic devices, demonstrating Hebbian learning, mainly in simulation environments. A simple network consisting of two synaptic devices and three neurons have been constructed to mimic Pavlov's salivation experiment [94, 103]. In figure 14, the associative learning experiment is explained. In the probing phase, non-overlapping stimuli signals are applied to the 'sight of food' and 'sound' neurons, resulting in firing of 'salivation' neuron only during 'sight of food' stimuli. In the learning phase, both 'sight of food' and 'sound' neurons are stimulated simultaneously, causing back-propagating pulses from the 'salivation' neuron to overlap with forward propagating pulses from the 'sound' neuron. A high voltage across the second synaptic device switches it into a low resistance state, which is only possible when both stimuli are correlated with each other. As a result, an association between 'sight of food' and 'sound' stimuli is developed. Following demonstration of STDP in individual synaptic devices, array-level simulations using recurrent synaptic networks inspired from hippocampus has been demonstrated [43]. The hippocampus region of the human brain is believed to play important roles in learning, episodic memory formation and spatial navigation [16, 104]. The layered and sequential anatomy of hippocampus is particularly suitable for electrophysiological investigation and it is a well-studied model system especially for studying plasticity in animals [105]. It consists of three distinct layers (dentate gyrus, CA3, CA1), which makes it easier to understand the neuronal circuitry and implement the neural circuitry using a 2D or layered 3D crossbar array-like architecture (figure 15(a)). Particularly, the CA3 region has extensive recurrent connections, which are believed to act as auto-associative memory, for storing and recalling patterns, and also are thought to enable rapid storage of large quantities of patterned input [106, 107]. Associative learning and pattern completion has been a popular subject of the study for neuromorphic circuits [108–111], probably due to their biological and psychological significance. Recently, two basic learning mechanisms, associative learning and sequence learning, have been implemented by simulations using small-scale crossbar arrays of phase change synaptic devices [42, 43]. For both learning mechanisms, a recurrent Hopfield-like network is constructed using a crossbar array composed of N neurons and $N \times N$ plastic synapses, utilizing all-to-all feedback (recurrent) connections. The connection weights of neurons are stored in synapses and the synaptic weight is adjusted according to symmetric and asymmetric STDP characteristics, measured on phase change synaptic devices (figures 15(b) and (c)). An integrate-and-fire (I&F)

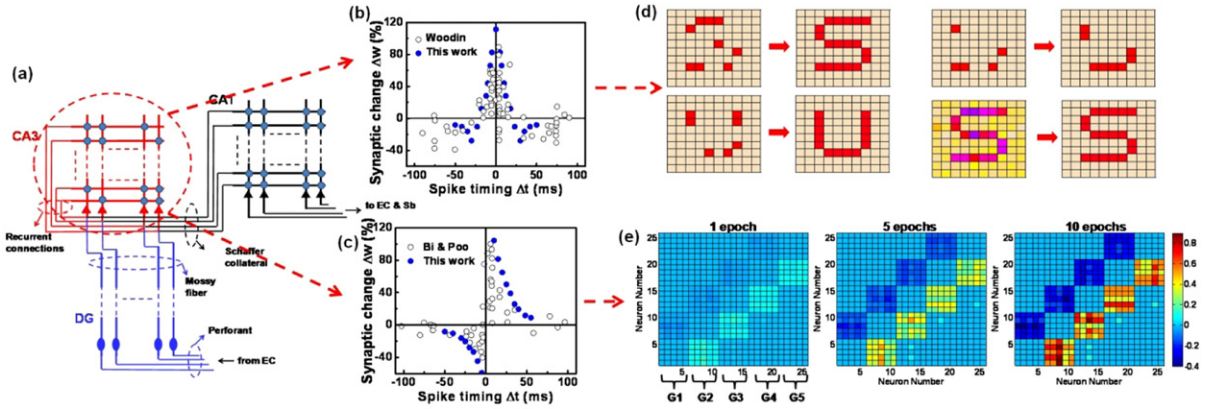

Figure 15. (a) Hippocampus model. It consists of three layers: dentate gyrus (DG) (bottom center), CA3 (top-left) and CA1 (top-right). The input to hippocampus enters from entorhinal cortex (EC) to DG via perforant pathway. The output leaves hippocampus from CA1 to EC and subiculum (Sb). (b) Symmetric STDP observed in hippocampal GABAergic synapses, biological data by Woodin [130] (reprinted with permission, copyright 2003 Elsevier). Synaptic weight change is plotted as a function of relative timing of pre- and post-spikes. The percentage change is calculated with respect to same initial value for all Δt points. (c) Asymmetric STDP observed in hippocampal glutamatergic synapses, biological data by Bi and Poo [19] (reprinted with permission, copyright 1998 Journal of Neuroscience). (d) The network can recall the original when a 50% incomplete 'S', a 50% incomplete 'U', a 70% incomplete 'U', and a noisy 'S' are presented. (e) Sequence learning with asymmetric STDP. Synaptic weight matrix is shown after 1, 5 and 10 training epochs. Synaptic efficacy is set to 0.1. The color corresponds to relative change in synaptic strengths, which are adjusted according to stimulation sequence.

model is used to update neuron potentials. The symmetric STDP acts as a coincidence detector for coactive neurons (figure 15(b)), making it appropriate to implement associative learning. In associative learning, the network learns a pattern by strengthening (potentiating) the synapses between neurons, which are coactive. If an incomplete or noisy pattern is presented, the potentiated synapses can recruit the missing neurons in order to recall original pattern. Associative learning simulations are done in a recurrent network of 100 neurons and 10 000 synapses. The simulation results have shown that the network can complete patterns with up to 50% missing elements and the recall success rate is ~85% in the presence of 30% white Gaussian noise in input data. The spike sequence dependent characteristic of asymmetric STDP (figure 15(c)) can allow neural circuits to learn temporal sequences of events and predict future events based on previous experience. Sequence learning simulations are done on a recurrent network consisting of 25 neurons and 625 synapses. 25 neurons are divided into five groups and the groups are stimulated sequentially with a probabilistic Gaussian spike train. During 10 training epochs, the weights of synapses are updated so that the network can predict what is next in the sequence. Figure 15(e) shows that synapses between consequent groups get stronger while reverse sequence synapses get weaker. The network can predict what is next in the sequence and recruit neurons to automatically compensate if the stimulation sequence shows timing variation or noise. Several other groups have simulated associative learning and pattern completion using a synaptic device or memristive device models [112–115]. Jackson *et al* demonstrated temporal sequence learning in a crossbar array using device models for phase change synaptic devices [41]. One of the strengths of neuromorphic computing is its robustness against variation and noise. Kuzum *et al* has illustrated with simulations that device-to-device and cycle-to-cycle resistance variation can be tolerated for pattern completion applications with phase change synaptic devices [43]. Associative learning forms a central part of cognition in animals and humans. Hence, synaptic networks performing associative learning will be an essential building block for high-level systems for cognitive or brain-inspired computing.

Another targeted application for synaptic electronics is auditory or visual data processing. Typically, the first step of any visual feature extraction is edge detection, and it can be done by a two-layer winner-take-all neural network with unsupervised learning. More complex image processing such as human or cat face recognition can be constructed by stacking more layers, e.g. for a deep learning algorithm [116]. Yu *et al* performed a simulation of such two-layer winner-take-all neural network as a toy model of the artificial visual system based on metal oxide RRAM synapses [117]. Figure 16(a) shows the network architecture implemented by integrate-and-fire neurons and synaptic devices: the first-layer neurons represent those in the retina, and the second-layer neurons represent those in the primary visual cortex. Every neuron in the second layer connects with all the neurons in the first layer through excitatory synapses. Every neuron in the second layer also connects to one another through inhibitory synapses. The second-layer neurons sum and integrate the input currents on the membrane capacitor independently, and the one with the largest input current fires first (becomes the 'winner'), then it discharges the membrane capacitor of all the other second-layer neurons and prevent them from firing ('takes all') through the inhibitory synapses. The unsupervised learning allows that the synapse conductance map between the first layer and the second layer gets modified slightly toward the depression direction to mimic the input pattern light intensity. Initially, the conductance of all the synaptic devices was randomized. During the training phase, 1000 gray-scale images of a 2D Gaussian bar with random center position and random orientation at all possible angles between 0° and 180° were fed into the first-layer neurons.

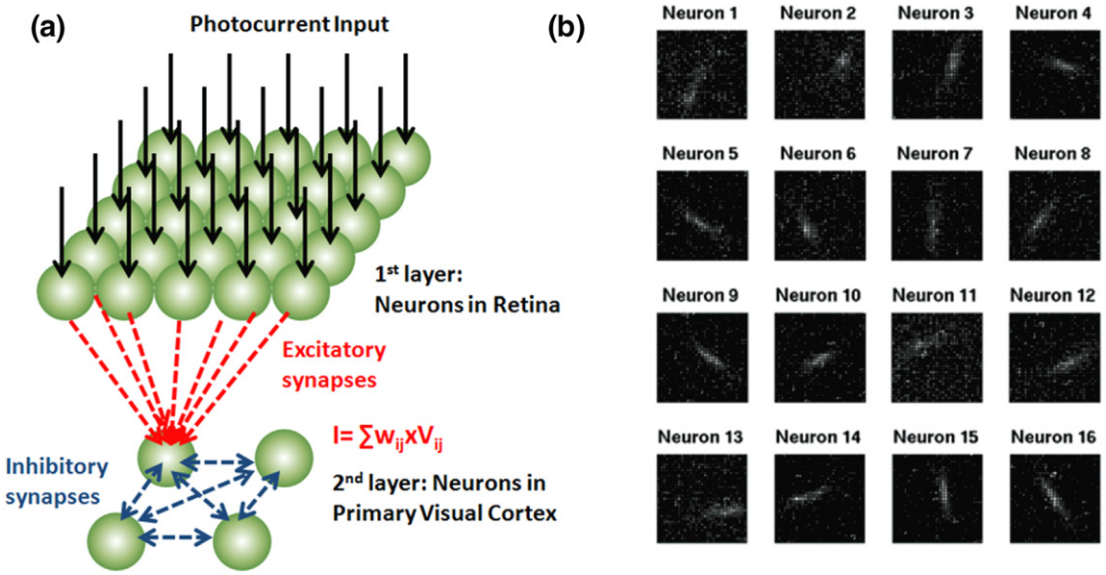

Figure 16. (a) Neuromorphic visual system based on winner-take-all architecture. The first layer and the second layer are connected with 16 348 RRAM synaptic devices. (b) Simulated final normalized synapse conductance map after training it with 1000 images. The noisy pixels are due to RRAM variation. Adapted with permission from [59]. Copyright 2012 IEEE.

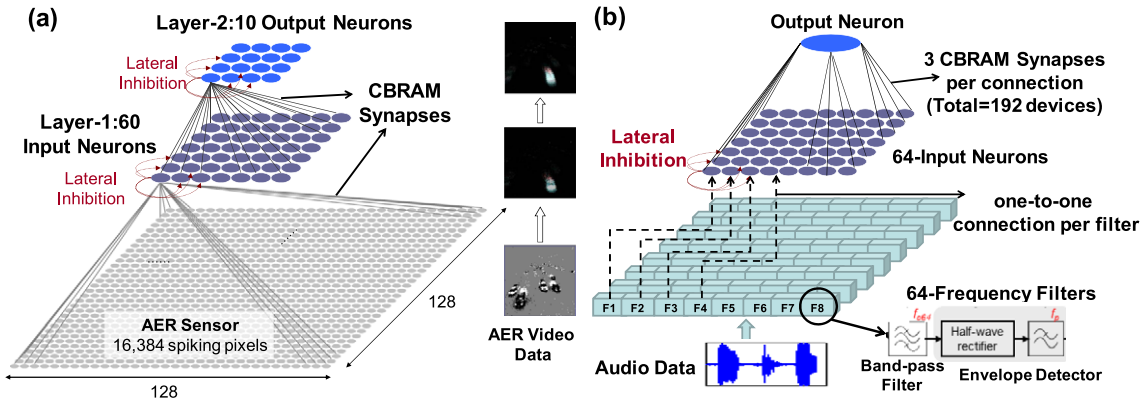

Figure 17. (a) Two-layer spiking neural network simulated for processing video data. Reprinted with permission from [74]. Copyright 2012 IEEE. (b) Single-layer spiking neural network simulated for auditory processing.

As the training progresses, the conductance begins to diverge: the conductance of synapses connecting the winner neuron in the second layer with the first-layer neurons that have a higher firing rate was least suppressed. After the training, the normalized conductance map becomes orientation selective (figure 16(b)). Furthermore, the system performance metrics such as orientation selectivity and the network storage capacity were investigated as a function of the synaptic device variability and the number of intermediate resistance states. The simulation suggests that the system performance is robust against the device variability up to the experimental measured level. However, the system performance degrades as the number of the intermediate resistance states decreases, suggesting the importance of obtaining multiple resistance levels in the synaptic device. Snider [118] and Zamarreno-Ramos *et al* [84] performed similar edge detection simulation on such winner-take-all network with memristive synaptic devices. In [84], the address-event-representation (AER) video data of driving in a car recorded from a silicon retina was used for the training. Bichler *et al* [119] performed a similar task of tracking car trajectories on a freeway using 2-PCM synapses with a simplified STDP rule where long-term potentiation and long-term depression are both produced with a single invariant crystallizing pulse. To detect cars passing in different lanes on a freeway in an unsupervised way, a two-layer feed-forward spiking neural network (figure 17(a)) has been simulated. AER data recorded with 128 × 128 pixel silicon retina is used as the input for the PCM neural network. Complex visual pattern extraction with an average detection rate of 92% has been achieved [39]. Figure 17(b) shows the network designed to learn, extract, and recognize hidden patterns in auditory data [74]. Temporally encoded auditory data are filtered and processed using a 64-channel silicon cochlea emulator and the processed data are fed to a single-layer feed-forward spiking neural network with 192 CBRAM synapses. Pure noise and an arbitrarily created pattern are

Table 3. A representative list of synaptic device characteristics following the metrics explained in section 4. The last column lists the retention/endurance that can be achieved using the same class of devices. These numbers were not measured by the reference cited in column 2. Dimensions are given as diameter (D) or width × length ($W \times L$).

	Synaptic device	Dimensions D or $W \times L$	Energy consumption	Programming time	Multi-level states	Max dynamic range	Achievable retention/endurance
Phase change	$Ge_2Sb_2Te_5$ (Kuzum *et al*)	$D = 75$ nm	2–50 pJ	∼50 ns	100	∼1000	Years/10^{12}
	$Ge_2Sb_2Te_5$ (Suri *et al*)	$D = 300$ nm	121–1552 pJ	∼50 ns	30	∼100	
Resistive change	TiO_x/HfO_x (Yu *et al*)	5 μm × 5 μm	0.85–24 pJ	∼10 ns	100	∼100	Years/10^{13}
	PCMO (Park *et al*)	$D = 150$ nm–1 μm	6–600 pJ	10 μs–1 ms	∼100	∼1000	
	TiO_x (Seo *et al*)	$D = 250$ nm	∼200 nJ	10 ms	100	>10, <100	
	WO_x (Yang *et al*)	25 μm × 25 μm	∼40 pJ	0.1 ms	>10	∼300	
Conductive bridge	Ag/a–Si/W (Jo *et al*)	100 nm × 100 nm	∼720 pJ	300 μs	100	∼10	Years/10^{8}
	Ag/Ag_2S/nanogap/Pt (Ohno *et al*)	Pt tip	∼250 nJ	0.5 s	10	>1000	
	Ag/GeS_2/W (Suri *et al*)	$D = 200$ nm	1800–3100 pJ	500 ns	2	∼1000	
Ferroelectric	BTO/LSMO (Chathbouala *et al*)	$D = 350$ nm	∼15 pJ	10 ns–200 ns	100	1000	N/A
FET-based	Ion-doped polymer-based FET (Lai *et al*)	1.5 μm × 20 μm	10 pJ	2 ms	∼50	>4	N/A
	NOMFET (Alibart *et al*)	5 μm × 1000 μm	∼5 μJ	2 s–10 s	∼30	∼15	N/A

used as inputs to test selectivity. The system has achieved sensitivity higher (>2) than the human ear with a very low false spike rate. These simulations have demonstrated that neuromorphic architectures with synaptic devices are attractive for visual and auditory data processing.

While simulations studies focus on a diverse range of applications with synaptic devices and give insights about the performance prospects of brain-inspired systems, research on neuromorphic architectures for synaptic devices is equally important [120]. The effort to map the structural and functional connectivity of the human brain has been accelerated by the launch of the Human Connectome Project [121], and more recently with the BRAIN Initiative [122]. Recent brain imaging studies suggest that the neural connectivity forms a 3D grid structure with no diagonals [123]. The connections are in the form of folding 2D sheets of parallel neuronal fibers that cross paths at right angles. This grid structure is found to be continuous and consistent at all scales and across humans and other primate species. The grid-like connectivity of the brain can be easily translated into a 2D or layered 3D crossbar array architecture with synaptic devices, bringing it one step closer to reach brain-level connectivity and synaptic density. Hybrid CMOS/nanoelectronic device networks or crossnets have been proposed to build neuromorphic systems [124–128]. These networks may be utilized to perform cognitive tasks which were originally implemented in software using neural network algorithms. Rough estimates show that with scaled CMOS technology and sub-10 nm synaptic devices these networks may eventually reach brain-level density and comparable connectivity [125].

6. Outlook and perspective

Research on synaptic devices has progressed rapidly in the last couple of years. Several material systems [129] including phase change, resistive change, ferroelectric materials, ion/insulator composites, polymers and carbon nanotubes have been investigated for synaptic applications, exploiting the physical mechanisms leading to multiple conductance states. Device structures that we are familiar with that share commonality with nonvolatile memory applications have seen more attention due to common characteristics and metrics desirable for both applications. The vision for the ideal synaptic device is overviewed in section 4 by detailing the performance metrics and their biological or application specific basis. The device characteristics desired are different from those targeted for digital nonvolatile memory applications. Table 3 summarizes some of the recent advances in synaptic devices reported in the literature. Device dimensions down to 75 nm have been demonstrated and sub-picojoule level energy consumptions have been reported. Most of the devices included in table 3 have promising scalability characteristics which will reduce energy consumption further upon scaling down the device size. Multi-level conductance states of up to 50–100 levels have been achieved by most of the synaptic device candidates. Beyond individual devices, crossbar arrays of more than 1000 synaptic devices have been built [60, 71], although neuromorphic computing has not been demonstrated at the chip scale. Meanwhile, further understanding of the switching mechanisms of synaptic devices has been obtained through a combination of experimental and simulation studies. Reliability characteristics of the synaptic devices remains an area which has not received much attention. However, it deserves more investigation as a practical implementation of brain-inspired systems with synaptic devices, which are being contemplated. Although most of the published work focuses on some specific applications for synaptic devices, the field has the potential to be utilized in a broad range of computing applications, especially the ones at the intersection of sensing and computation, where real-time and parallel processing of large-scale data is crucial. There is an enormous opportunity to completely rethink the design of computational systems in order to gain orders of magnitude of improvement in computational efficiency through inspiration from the biological brain. More interactions among different research disciplines (devices, circuits, architecture, and computing) can further cultivate the synaptic electronics field and help define more targeted research paths for the future.

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