

Horst Zimmermann

Silicon Optoelectronic Integrated Circuits

Second Edition



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Horst Zimmermann
EMCE
Technische Universität Wien
Vienna, Austria

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Preface to the Second Edition

Since the first edition of this book in 2004, a huge amount of very interesting integrated optoelectronic devices and circuits were investigated and introduced in numerous publications. Therefore, Springer and I decided to publish this extended edition. Hot topics were integrated avalanche photodiodes, and there even was a hype on single-photon avalanche diodes (SPADs) and on SPAD sensor and imager ICs in the last decade. It was only possible to select some, which seemed to be kind of key publications to me. Optical wireless communication was improved by integrated avalanche photodiodes in the linear mode. In addition, first SPAD optical receivers eliminating electronic noise and trying to approach the quantum limit set by photon statistics had to be included. First, OWC experiments with SPAD receivers seem also to be worth of inclusion in this extended edition.

There was also considerable progress with the so-called silicon photonics foundry. Therefore, a chapter describing several advanced electronic-photonic integrated ICs was added.

There were also innovative pin photodiode OEICs introducing new circuit architectures for transimpedance and bandwidth enhancement. Furthermore, really astonishing high-pixel-count image sensors and three-dimensionally integrated image sensors had to be included.

I would like to thank Dr. Claus Ascheron from Springer for initiating this extended edition and his team for technical support with the text processor. From my current research group at TU Wien, I have to thank especially Dr. Michael Hofbauer, Dr. Bernhard Goll, Dr. Kerstin Schneider-Hornstein, Dr. Hiwa Mahmoudi, Bernhard Steindl, Dinka Milovancev, and Nemanja Vokic for their excellent work and strong motivation. In the same amount, I have to thank the former group members Dr. Paul Brandl, Dr. Tomislav Jukic, Dr. Nicola Zecevic, Dr. Robert Swoboda, Dr. Reinhard Enne, Wolfgang Gaberl, Dr. Milos Davidovic, Dr. Michael Förtsch, Dr. Mohamed Atef, Dr. Christoph Seidl, Dr. Johannes Knorr, Dr. Stefan Schidl, Dr. Jürgen Leeb, and Dr. Andreas Polzer. The longest cooperation exists with XFAB Semiconductor Foundry, and I would like to thank Wolfgang Einbrodt, Dr. Konrad Bach, Detlev Sommer, Dr. Alexander Zimmer, and Dr. Daniel Gäbler for enabling the huge progress with silicon OEICs.

I also warmly thank the project partners from the European projects INSPIRED (Dr. Gernot Langguth and Dr. Holger Wille, Infineon Munich; Dr. Johannes Sturm, Infineon Villach), HELIOS (Dr. Jean-Marc Fedeli, CEA LETI, Grenoble; Dr. Franz Schrank, AMS AG, Premstätten), and IRIS (Francesco Testa, Ericsson, Pisa; Prof. Dr. Lorenzo Pavese, University of Trento; Dr. Claudio Oton, Scuola Superiore Sant' Anna, Pisa; Dr. Christoph Kopp, CEA LETI, Grenoble (I hope the others can excuse that I cannot include all of them here) as well as the national PHELICITI project partners from AIT (Dr. Bernhard Schrenk, Dr. Paul Müllner) and AMS AG (Dr. Jochen Kraft). Without them, many high-level results would not have been generated and could not have been included in this book.

My deepest gratitude, again, is directed to my wife, my daughters Luise and Lina, as well as to my son Frieder, who would have preferred to bike more often together, for their great patience.

Vienna, Austria

Horst Zimmermann

Preface to the First Edition

Since the book “Integrated Silicon Optoelectronics” appeared in the “Springer Series in Photonics” in 2000, a whole variety of silicon optoelectronic integrated circuits (SOEICs) have been developed and introduced in many journals and conference proceedings. Therefore, a new book on these new SOEICs collecting and selecting the most interesting ones was highly desirable especially because the main part of “Integrated Silicon Optoelectronics” concentrated on integrated photodetectors. This new book, in contrast, describes considerably more circuits implemented as SOEICs together with the photodetectors.

Many design engineers in semiconductor companies, ASIC and design houses have to design SOEICs, OPTO-ASICs, image sensors or even smart pixel sensors. I also feel that the number of Ph.D. students or diploma workers doing research and development in the field of optoelectronic circuits is constantly growing. This book, therefore, is intended as a second bridge (after “Integrated Silicon Optoelectronics”) between microelectronics and optoelectronics. Usually, optoelectronics plays a minor role in electrical engineering courses at universities. Physicists are taught optics but not very much semiconductor technology and chip design. This book covers the missing information for engineers and physicists who want to know more about integrated optoelectronic circuits (OEICs) in silicon technologies and about their rapidly emerging applications. The low-cost requirement permanently drives and pushes silicon OEICs in contrast to expensive III/V semiconductor receiver OEICs. This book reflects this trend by stressing CMOS OEICs. BiCMOS OEICs with their better performance, however, are also described in detail, since they are still much cheaper than III/V OEICs.

The importance of OEICs is due to the following advantages of monolithic optoelectronic integrated circuits: (i) good immunity against electromagnetic interference (EMI) because of very short interconnects between photodetectors and amplifiers, (ii) reduced chip area due to the elimination of bondpads, (iii) improved reliability due to the elimination of bondpads and bond wires, (iv) cheaper mass

production compared to discrete circuits, wire-bonded circuits, and hybrid integrated circuits, and (v) larger -3 dB bandwidth compared to discrete circuits, wire-bonded circuits, and some hybrid integrated circuits due to the avoidance of parasitic bondpad capacitances.

This book describes the basics and theory of photodetectors in a compact form. The three chapters on integrated photodetectors, thin-film detectors, and SiGe detectors describe the properties of photodiodes, which were implemented in the circuits discussed later in this book. The chapter on design of integrated circuits covers analytical methods for calculating bandwidth. Methods for calculating input and output resistance as well as electronic noise of transimpedance amplifiers were also added. Furthermore, a transmission line approach leading to a new π -model for integrated transimpedance amplifiers was included.

In the last and longest chapter, new concepts for DVD and CD-ROM OEICs and new results on these still economically more important key devices for optical storage systems were included. The state-of-the-art of fiber receiver OEICs was updated, and new market demands like plastic optic fiber receivers and burst-mode optical receivers are covered by the description of these receiver circuits. The key topics systems-on-chip (SoC) and camera-on-chip (CoC) are included. Within CoCs, revolutionary three-dimensional single-chip CMOS cameras are described. Various CMOS and BiCMOS optical sensor chips are introduced. Several innovative smart sensor circuits are highlighted. Furthermore, speed enhancement techniques for fiber receivers and large-area, large-capacitance photodiodes are explained. The general trend toward deep-sub-micrometer analog–digital CMOS SoCs is considered with respect to OEICs. Finally, new optical interconnect and free-space receivers based on the optoelectronic phase-locked loop principle are introduced.

Parts of the book have their origin in the lecture “Optoelectronic integrated circuits” started at Vienna University of Technology in 2001 and in the lecture “Optoelectronics” I had given from 1994 to 1999 at Kiel University. This book, however, dives much deeper into the topic. The possibilities of SOEICs are described thoroughly with respect to circuits, and some new integrated detectors like the innovative so-called spatially modulated light detector and the photonic mixer device (PMD) are added. The newest publications on silicon OEICs up to 2003 are considered.

I would like to thank Prof. Dr.-Ing. P. Segebrecht from Kiel University, Germany, where I began research and development on silicon OEICs, for the generous possibility to work independently and to acquire the title “habilitatus.” I am also indebted to Prof. Dr. H. Föll, who offered a wafer prober for the characterization of the OEICs. The work of the OEIC group members at Kiel University, A. Ghazi, T. Heide, M. Hohenbild, K. Kieschnick, and G. Volkholz, is highly appreciated. Three students, N. Madeja, F. Sievers, and U. Willecke, carefully performed simulations and measurements. M. Wieseke and F. Wölk helped with the preparation of numerous drawings. Special thanks go to R. Buchner from the Fraunhofer Institute for Solid-State Technology in Munich and H. Pless from Thesys Microelectronics (now Melexis) in Erfurt, Germany, for their engagement in

the fabrication of CMOS OEICs and BiCMOS OEICs, respectively. I gratefully acknowledge the funding of the projects by the German ministry for education, science, research, and technology (BMBF) within the leading project “Optical Storage.”

At the Institute for Electrical Measurements and Circuit Design (EMST) at Vienna University of Technology, I would like to thank my colleague and head of the institute Gottfried Magerl for his great support toward a quick start of research. I also have to thank my Ph.D. students M. Förtsch, J. Knorr, F. Schlögl, K. Schneider, and R. Swoboda for their careful design and characterization work. M. Hofer, Ch. Sünder, and J. Wissenwasser drew many new figures. I further have to thank G. Langguth and H. Wille from Infineon Technologies in Munich, Germany, J. Sturm from Infineon Technologies in Villach, Austria, as well as A. Martin from Infineon Technologies in Vienna, Austria, for their support and constructive cooperation. I further acknowledge funding from the European Commission in the project INSPIRED.

I extend my sincere thanks to Dr. Ascheron and his team at Springer for the good cooperation and their technical support with the text processor. My deepest gratitude, however, is directed to my wife and my daughters, Luise and Lina, as well as to my son Frieder, who supported this second book project with their encouragement and patience.

Vienna, Austria

Horst Zimmermann

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About the Author

Dr. Horst Zimmermann received the diploma in Physics in 1984 from the University of Bayreuth, Germany, and the Dr.-Ing. degree from the University Erlangen–Nürnberg working at the Fraunhofer Institute for Integrated Circuits (IIS-B), Erlangen, Germany, in 1991. Then, he was an Alexander-von-Humboldt Research Fellow at Duke University, Durham, N.C., working on diffusion in Si, GaAs, and InP until 1992. In 1993, he joined the Chair for Semiconductor Electronics at Kiel University, Kiel, Germany, where he lectured optoelectronics and worked on optoelectronic integration in silicon technology. Since 2000, he is Full Professor for Electronic Circuit Engineering at Vienna University of Technology, Vienna, Austria. His main interests are in design and characterization of analog and nanometer CMOS circuits as well as optoelectronic integrated CMOS and BiCMOS circuits. He is Author of the Springer books *Integrated Silicon Optoelectronics* and *Silicon Optoelectronic Integrated Circuits* as well as Co-author of *Highly Sensitive Optical Receivers*, *Optical Communication Over Plastic Optical Fibers*, *Analog Filters in Nanometer CMOS*, *Comparators in Nanometer CMOS Technology*, and *Optoelectronic Circuits in Nanometer CMOS Technology*. In addition, he is author and co-author of more than 500 publications. In 2002, he became Senior Member IEEE. He was primary Guest Editor of the November/December 2014 issue of IEEE Journal of Selected Topics in Quantum Electronics on *Optical Detectors: Technology and Applications*.

Symbols

A	Area (cm^2)
A_0	Low-frequency open-loop gain
$A(\omega)$	Frequency-dependent gain
APD	Avalanche photodiode
APP	Afterpulsing probability
c	Speed of light in a medium (cm/s)
c_0	Speed of light in vacuum (cm/s)
c_{bd}	Small-signal bulk-drain capacitance (F)
c_{bs}	Small-signal bulk-source capacitance (F)
c_{cs}	Small-signal collector-substrate capacitance (F)
c_{gb}	Small-signal gate-bulk capacitance (F)
c_{gd}	Small-signal gate–drain capacitance (F)
c_{gs}	Small-signal gate–source capacitance (F)
C_{ox}	Gate-oxide capacitance per area (F)
c_{ws}	Small-signal well-substrate capacitance (F)
c_{je}	Small-signal emitter–base capacitance (F)
c_{μ}	Small-signal base–collector capacitance (F)
C_e	Doping concentration of epitaxial layer (cm^{-3})
C_B	Capacitance of bondpad (F)
C_{BE}	Base–emitter capacitance (F)
C_C	Base–collector space charge capacitance (F)
C_D	Depletion capacitance of photodiode (F)
C_E	Total base–emitter capacitance of bipolar transistor (F)
C_F	Feedback capacitance of transimpedance amplifier (F)
C_{GS}	Gate–source capacitance (F)
C_I	Input capacitance of amplifier (F)
C_L	Load capacitor (F)
C_P	Capacitance of chip package (F)
C_{RF}	Parasitic capacitance of feedback resistor (F)
C_S	Parasitic capacitance of signal line (F)

C_{SE}	Base-emitter space charge capacitance (F)
C_T	Input node capacitance (F)
d	Distance (m)
d_e	Thickness of epitaxial layer (μm)
d_i	Thickness of intrinsic region (μm)
d_p	Thickness of P-type region (μm)
D	Diffusion coefficient (cm^2/s)
D_n	Diffusion coefficient of electrons (cm^2/s)
D_p	Diffusion coefficient of holes (cm^2/s)
D_t	Decision threshold of photocurrent (A)
DCR	Darc count rate
DR	Data rate (Mb/s)
E_C	Bottom of conduction band (eV)
E_F	Fermi energy level (eV)
E_g	Energy bandgap (eV)
E_t	Energy level of recombination center (eV)
E_V	Top of valence band (eV)
E	Photon energy (eV)
E	Electric field (V/cm)
f	Frequency (Hz)
f_g	Bandwidth, -3 dB frequency (Hz)
f_s	Sampling frequency (Hz)
f_T	Transit frequency (gain-bandwidth product) (Hz)
f_{GP}	Frequency of gain peak (Hz)
FF	Fill factor
g_{ds}	Transistor output conductance (A/V)
G	Photogeneration (e-h-p) (cm^{-3}/s)
$G(\omega)$	Frequency response function (V/A)
g_m	Transconductance (A/V)
h	Planck constant (Js)
\hbar	$h/2\pi$ (Js)
$h\nu$	Photon energy (eV)
i_L	Leakage current of photodiode (A)
I	Current (A)
I_{ph}	Photocurrent (A)
I_{th}	Threshold current (A)
I_B	Base current (A)
I_C	Collector current (A)
I_D	Drain current (A)
I_E	Emitter current (A)
I_S	Source current (A)
$I(x)$	Light intensity distribution (W/m^2)
$I_{i,j}$	Local luminance at pixel (i, j) (W/m^2)
j	Current density (A/cm^2)

k_B	Boltzmann constant (J/K)
$k_B T$	Thermal energy (eV)
L	Length (μm)
L_n	Diffusion length of electrons (μm)
L_p	Diffusion length of holes (μm)
L_B	Inductance of bond wire (H)
L_G	Gate length (μm)
L_W	Inductance of lead wire (H)
\bar{n}	Refractive index
\bar{n}_s	Refractive index of surroundings
\bar{n}_{sc}	Refractive index of semiconductor
\bar{n}_{ARC}	Refractive index of antireflection coating
n	Density of free electrons (cm^{-3})
n_i	Intrinsic carrier density (cm^{-3})
N	Impurity concentration (cm^{-3})
N_A	Acceptor concentration (cm^{-3})
N_D	Donor concentration (cm^{-3})
N_t	Concentration of recombination centers (cm^{-3})
p	Density of free holes (cm^{-3})
Q_E	Minority-carrier charge in the base (As)
Q_{pix}	Charge on pixel storage capacitor (As)
QE	Quantum efficiency (%)
P_{opt}	Incident optical power (W)
P_{opt}^{av}	Average incident optical power (W)
\bar{P}	Optical power in a semiconductor (W)
PDP	Photon detection probability
q	Magnitude of electronic charge (As)
r_b	Base series resistance (Ω)
r_o	Small-signal output resistance (Ω)
r_c	Small-signal collector series resistance (Ω)
r_{ex}	Small-signal emitter series resistance (Ω)
r_d	Small-signal drain series resistance (Ω)
r_s	Small-signal source series resistance (Ω)
R	Responsivity (A/W)
R_{bb}	Responsivity to black-body radiation (A/W)
R_{ov}	Oversampling ratio
R_D	Parallel resistance (Ω)
R_F	Feedback resistance (Ω)
R_S	Series resistance (Ω)
R_I	Input resistance of amplifier (Ω)
R_L	Load resistance (Ω)
\bar{R}	Reflectivity
S	Sensitivity of DVD OEICs (mV/ μW)
SPAD	Single-photon avalanche diode

t	Time (s)
t_d	Drift time (s)
t_{diff}	Diffusion time (s)
t_f	Fall time (s)
t_{int}	Integration time (s)
t_r	Rise time (s)
t_{gd}	Group delay (s)
T	Absolute temperature (K)
T_s	Sampling time (s)
U	Voltage (V)
U_{BE}	Base-emitter voltage (V)
U_D	Built-in voltage (V)
U_{DS}	Drain-source voltage (V)
U_{Ea}	Early voltage (V)
U_{GS}	Gate-source voltage (V)
U_T	Thermal voltage $k_B T/q$ (V)
U_{th}	Thermal generation/recombination rate ($\text{cm}^{-3}\text{s}^{-1}$)
U_{Th}	Threshold voltage (V)
V_{Th}	Threshold voltage (V)
V_{det}	Detector bias (V)
V_o	Output voltage (V)
V_{rev}	Reverse voltage (V)
v	Carrier velocity (cm/s)
v_s	Saturation velocity (cm/s)
v_{th}	Thermal velocity (cm/s)
W	Width of space charge region (μm)
W_B	Base thickness (μm)
W_G	Gate width (μm)
Z_F	Feedback impedance of transimpedance amplifier (Ω)
x	x direction (μm)
y	y direction (μm)
α	Absorption coefficient (μm^{-1})
β	Current gain of bipolar transistor
β_F	Feedback parameter of transimpedance amplifier (Ω^{-1})
η_e	External (total) quantum efficiency (%)
η_i	Internal quantum efficiency (%)
η_o	Optical quantum efficiency (%)
η_{tia}	Efficiency of transimpedance amplifier
$\eta_{\text{tia}}^{\text{bip}}$	Efficiency of bipolar transimpedance amplifier
$\eta_{\text{tia}}^{\text{MOS}}$	Efficiency of MOS transimpedance amplifier
ϵ_0	Permittivity in vacuum (F/cm)
ϵ_r	Relative permittivity
ϵ_s	Semiconductor permittivity (F/cm)
$\bar{\epsilon}$	Dielectric function

σ	Carrier capture cross section (cm^{-2})
τ	Lifetime (s)
τ_n	Electron lifetime (s)
τ_p	Hole lifetime (s)
τ_B	Base transit time (s)
$\bar{\kappa}$	Extinction coefficient
λ	Wavelength in a medium (nm)
λ_0	Wavelength in vacuum (nm)
λ_c	Wavelength corresponding to E_g (nm)
λ_{ch}	Channel length modulation parameter (V^{-1})
v	Frequency of light (Hz)
μ	Mobility (cm^2/Vs)
μ_n	Electron mobility (cm^2/Vs)
μ_p	Hole mobility (cm^2/Vs)
ω	Angular frequency (s^{-1})
ω_c	$2 \cdot \pi \cdot f_g$ (s^{-1})
ω_T	$2 \cdot \pi \cdot f_T$ (s^{-1})
ω_{GP}	$2 \cdot \pi \cdot f_{GP}$ (s^{-1})
ρ	Charge density (As/cm^3)
Φ	Photon flux density ($\text{cm}^{-2}\text{s}^{-1}$)
Ψ	Potential (V)
Θ	Angle ($^\circ$)

Chapter 1

Basics and Theory



Optical absorption is a fundamental process which is exploited when optical energy is converted into electrical energy. Optoelectronic receivers are based on this energy conversion process. Photodetectors convert optical energy into electrical energy. In this chapter, the most important factors needed for the comprehension of photodetectors will be summarized in a compact form. For a detailed description of the basics of optical absorption, the book [1] can be recommended. Here, emphasis will, of course, be placed on silicon devices. After the collection of the most important optical and optoelectronic definitions, we will summarize the fundamentals of device physics and modeling of solid-state electron devices including photodetectors in a compact form. A detailed review on modeling of solid-state electron devices can be found in [2]. Here, the semiconductor equations with implemented photogeneration and the models for carrier mobility used in device simulators will be listed first. Carrier drift and diffusion as well as their consequences for the speed and the quantum efficiency of photodetectors will be explained. Furthermore, the equivalent circuit of a photodiode will be discussed in order to show further aspects concerning the speed of photoreceivers.

First, however, we will introduce photons and the properties of light. Photogeneration will be defined. Furthermore, optical reflection and its consequences on the efficiency of photodetectors will be described.

1.1 Basics of Optical Absorption

1.1.1 Photons and Their Properties

Due to the work of Max Planck and Albert Einstein it is possible to describe light not only by a wave formalism but also by a quantum-mechanical particle formalism.

The smallest unit of light is a quantum-mechanical particle called a photon. The photon, consequently, is the smallest unit of an optical signal. Photons are used to characterize electromagnetic radiation in the optical range from the far infrared to the extreme ultraviolet spectrum. The velocity of photons c in a medium with an optical index of refraction \bar{n} is

$$c = \frac{c_0}{\bar{n}}, \quad (1.1)$$

where c_0 is the velocity of light in vacuum. Photons do not possess a quiescent mass and, unfortunately for the construction of purely optical computers, cannot be stored. Photons can be characterized by their frequency ν and by their wavelength λ :

$$\lambda = \frac{c}{\nu}. \quad (1.2)$$

The frequency of a photon is the same in vacuum and in a medium with index of refraction \bar{n} ($\bar{n} = 1$ for vacuum, $\bar{n} > 1$ in a medium). The wavelength λ in a medium, therefore, is shorter than the vacuum wavelength λ_0 ($\lambda = \lambda_0/\bar{n}$). As a consequence, the vacuum wavelength is used to characterize light sources like light-emitting diodes (LEDs) or semiconductor lasers, because it is independent of the medium in which the light propagates.

Photons can also be characterized by their energy E (h is Planck's constant):

$$E = h\nu = \frac{hc}{\lambda} = \frac{hc_0}{\lambda_0}. \quad (1.3)$$

According to fundamental absorption, this formula leads to the boundary wavelength, which can be detected with the bandgap $E_g = 1.1\text{ eV}$ of silicon:

$$\lambda_c = \frac{hc_0}{E_g} = 1110\text{ nm}. \quad (1.4)$$

Only light with shorter wavelengths than 1110 nm can be detected with silicon photodiodes.

A useful relation is given next which allows a quick calculation of the energy for a certain wavelength and vice versa:

$$E = \frac{1240}{\lambda_0} \quad (1.5)$$

where E is in eV and λ_0 in nm. Let us define the flux density Φ as the number of photons incident per time interval on an area A . The optical power P_{opt} incident on a detector with a light sensitive area A , then, is determined by the photon energy and by the flux density:

$$P_{\text{opt}} = E\Phi A = h\nu\Phi A. \quad (1.6)$$

Receivers for optical communication or data transmission are characterized by the average optical power $P_{\text{opt}}^{\text{av}}$ needed to achieve a certain bit error ratio.

1.1.2 *Optical Absorption of Important Semiconductor Materials*

The energy of a photon can be transferred to an electron in the valence band of a semiconductor, which is brought to the conduction band, when the photon energy is larger than the bandgap energy E_g . The photon is absorbed during this process and an electron–hole pair is generated. Photons with an energy smaller than E_g , however, cannot be absorbed and the semiconductor is transparent for light with wavelengths longer than $\lambda_c = hc_0/E_g$.

The optical absorption coefficient α is the most important optical constant for photodetectors. The absorption of photons in a photodetector to produce carrier pairs and thus a photocurrent, depends on the absorption coefficient α for the light in the semiconductor used to fabricate the detector. The absorption coefficient determines the penetration depth $1/\alpha$ of the light in the semiconductor material according to Lambert–Beer’s law:

$$I(\bar{y}) = I_0 \exp(-\alpha \bar{y}). \quad (1.7)$$

The optical absorption coefficients for the most important semiconductor materials are compared in Fig. 1.1. The absorption coefficients strongly depend on the wavelength of the light. For wavelengths shorter than λ_c , which corresponds to the bandgap energy ($\lambda_c = hc_0/E_g$), the absorption coefficients increase rapidly according to the so-called *fundamental absorption*. The steepness of the onset of absorption depends on the kind of band–band transition. This steepness is large for direct band–band transitions as in GaAs ($E_g^{\text{dir}} = 1.42 \text{ eV}$ at 300 K), in InP ($E_g^{\text{dir}} = 1.35 \text{ eV}$ at 300 K), in Ge ($E_g^{\text{dir}} = 0.81 \text{ eV}$ at 300 K) and in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($E_g^{\text{dir}} = 0.75 \text{ eV}$ at 300 K). For Si ($E_g^{\text{ind}} = 1.12 \text{ eV}$ at 300 K), for Ge ($E_g^{\text{ind}} = 0.67 \text{ eV}$ at 300 K) and for the wide bandgap material 6H-SiC ($E_g^{\text{ind}} = 3.03 \text{ eV}$ at 300 K) the steepness of the onset of absorption is small.

$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and Ge cover the widest wavelength range including the wavelengths 1.3 and $1.54 \mu\text{m}$ which are used for long distance optical data transmission via optical fibers. The absorption coefficients of GaAs and InP are high in the visible spectrum ($\approx 400\text{--}700 \text{ nm}$). Silicon detectors are also appropriate for the visible and near infrared spectral range. The absorption coefficient of Si, however, is one to two orders of magnitude lower than that of the direct semiconductors in this spectral range. For Si detectors, therefore, a much thicker absorption zone is needed than for the direct semiconductors. We will, however, see in this work that with silicon photodiodes GHz operation is nevertheless possible. Silicon is the economically most important semiconductor and it is worthwhile to investigate silicon

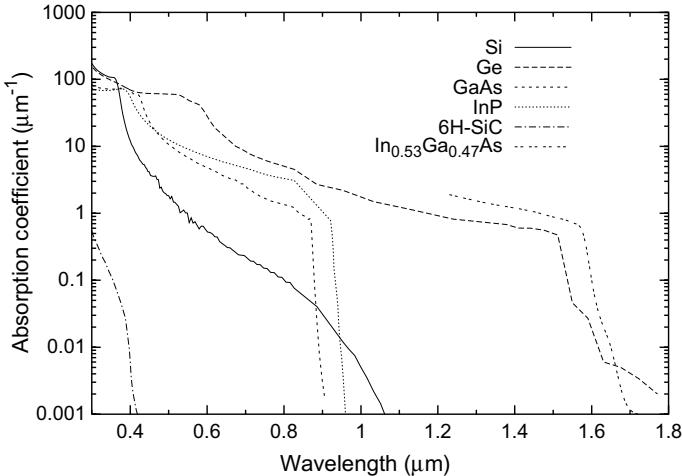


Fig. 1.1 Absorption coefficients of important semiconductor materials versus wavelength

Table 1.1 Absorption coefficients α of silicon and intensity factors I_0 (ehp/cm^3 means electron–hole pairs/ cm^3) for several important wavelengths for a constant photon flux density of $\Phi = I_0/\alpha = 1.58 \times 10^{18}$ photons/ cm^2

Wavelength (nm)	α (μm^{-1})	I_0 (ehp/cm^3)
850	0.06	9.50×10^{20}
780	0.12	1.89×10^{21}
680	0.24	3.79×10^{21}
635	0.38	6.00×10^{21}
430	5.7	9.00×10^{22}

optoelectronic devices and integrated circuits in spite of the nonoptimum optical absorption of silicon.

The absorption coefficients of silicon for wavelengths which are the most important ones in practice are listed in Table 1.1 [3, 4]. In order to compare the quantum efficiencies of photodetectors for different wavelengths, it is advantageous to use the same photon flux for the different wavelengths. The photocurrents of photodetectors are equal for the same fluxes of photons with different energy, i.e. for different light wavelengths, when the quantum efficiency of the photodetector is the same for the different photon energies or wavelengths, respectively. According to the Lambert–Beer law, different intensity factors I_0 result for a constant photon flux. As an example, intensity factors are listed for the most important wavelengths in Table 1.1 for a certain arbitrary photon flux density.

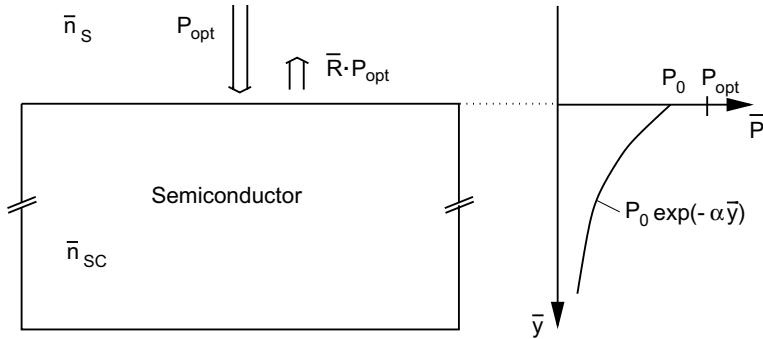
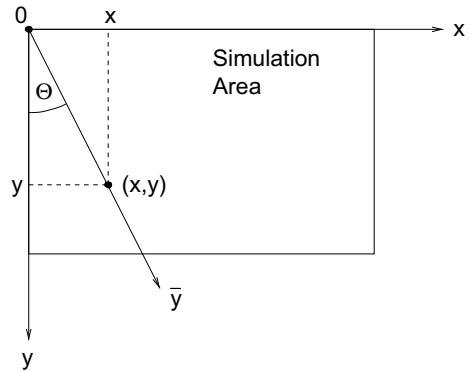


Fig. 1.2 Reflection at a semiconductor surface and decay of the optical power in the semiconductor ($P_0 = (1 - \bar{R})P_{\text{opt}}$)

Fig. 1.3 Coordinate transformation from the penetration coordinate \bar{y} to the coordinates (x, y) used in the two-dimensional device simulator for nonperpendicular light incidence



1.1.3 Photogeneration

The Lambert–Beer law can be formulated for the optical power \bar{P} analogously to (1.7):

$$\bar{P}(\bar{y}) = P_0 \exp(-\alpha \bar{y}). \quad (1.8)$$

The optical power at the surface of the semiconductor $\bar{P}(\bar{y} = 0)$ is $P_0 = (1 - \bar{R})$ (see Fig. 1.2). The optical power of the light penetrating into a medium decreases exponentially with the penetration coordinate \bar{y} in the medium (compare Fig. 1.3).

The absorbed light generates electron–hole pairs in a semiconductor due to the internal photoeffect provided that $h\nu > E_g$. Therefore, we can express the generation rate per volume $G(\bar{y})$ as:

$$G(\bar{y}) = \frac{\bar{P}(\bar{y}) - \bar{P}(\bar{y} + \Delta \bar{y})}{\Delta \bar{y}} \frac{1}{A h \nu}. \quad (1.9)$$

In this equation, A is the area of the cross section for the light incidence and $h\nu$ is the photon energy. For $\Delta\bar{y} \rightarrow 0$, we can write $(\bar{P}(\bar{y}) - \bar{P}(\bar{y} + \Delta\bar{y}))/\Delta\bar{y} = -d\bar{P}(\bar{y})/d\bar{y}$. From (1.8), $d\bar{P}(\bar{y})/d\bar{y} = -\alpha\bar{P}(\bar{y})$ then follows and the generation rate is

$$G(\bar{y}) = \frac{\alpha P_0}{A h \nu} \exp(-\alpha \bar{y}). \quad (1.10)$$

1.2 Semiconductor Equations

The physics of semiconductor devices like diodes, MOSFETs (Metal-Oxide-Silicon Field-Effect Transistors), bipolar transistors, and photodetectors is well known. The equations describing the behavior of these devices in most important cases are the semiconductor equations. These equations have already been implemented in many device simulation programs. The physical models for the parameters used in the semiconductor equations were discussed thoroughly, for instance, in [2].

Device simulation programs have been valuable tools for the development of semiconductor devices for many years. Much time and money can be saved with their help for such a purpose. They are also valuable for the development of photodetectors. We will take the two-dimensional device simulator MEDICI as an example [5]. The drift-diffusion model is implemented in this simulator. MEDICI solves the Poisson equation (1.11), the transport equations (1.13) and (1.14), and the continuity equations (1.16) and (1.17) for electrons and holes. Furthermore, photogeneration is implemented. Due to the photogeneration for the internal photoeffect, electron–hole pairs are created, i.e. the corresponding generation terms for electrons and holes are equal.

The potential Ψ in the device, for which the simulation is performed, is calculated according to the Poisson equation:

$$\Delta\Psi = -\frac{\rho}{\epsilon}. \quad (1.11)$$

The quantity ϵ is the product of the relative and absolute dielectric constants: $\epsilon = \epsilon_r \epsilon_0$. The symbol ρ represents the charge density, which can be further broken apart into the product of the elementary charge q times the sum of the hole concentration p (positively charged), of the electron concentration n (negatively charged), of the donor concentration N_D (positively charged), and of the acceptor concentration N_A (negatively charged):

$$\rho = q(p - n + N_D - N_A). \quad (1.12)$$

The current densities for electrons and holes are the sum of the drift and diffusion current densities:

$$\mathbf{j}_n = qn\mu_n \mathbf{E} + qD_n \mathbf{grad} n, \quad (1.13)$$

$$\mathbf{j}_p = qp\mu_p \mathbf{E} - qD_p \mathbf{grad} p. \quad (1.14)$$

The total current density results from the electron and hole current densities:

$$\mathbf{j} = \mathbf{j}_n + \mathbf{j}_p. \quad (1.15)$$

The continuity equations with the inclusion of photogeneration $G(x, y)$ due to the penetration of light into the semiconductor can be written as:

$$\frac{\partial n}{\partial t} = \frac{\text{div } \mathbf{j}_n}{q} + U_{\text{th}} + G(x, y), \quad (1.16)$$

$$\frac{\partial p}{\partial t} = -\frac{\text{div } \mathbf{j}_p}{q} + U_{\text{th}} + G(x, y). \quad (1.17)$$

U_{th} is the thermal generation/recombination term. The photogeneration $G(\bar{y})$ was derived above. The simulator allows us to define nonperpendicular incidence for the light. Then, $G(x, y) = G(\bar{y} = (x^2 + y^2)^{1/2})$ has to be used (compare with Fig. 1.3).

The electric field is determined by (1.11) and obeys:

$$\mathbf{E} = -\mathbf{grad} \Psi. \quad (1.18)$$

The electric field, for instance, is important for the calculation of the drift velocity \mathbf{v} of photogenerated carriers in photodetectors:

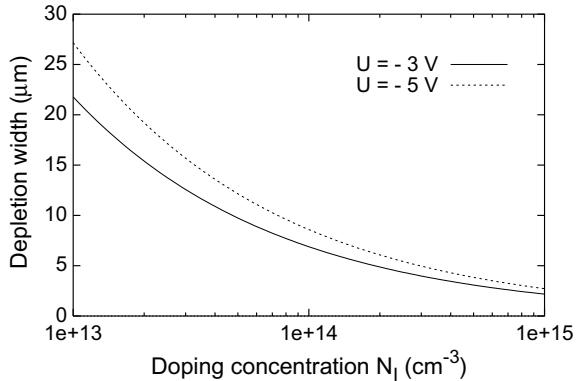
$$\mathbf{v} = \mu \mathbf{E}. \quad (1.19)$$

The mobilities of electrons and holes differ strongly and μ_n or μ_p has to be used for μ in order to calculate the electron drift velocity or the hole drift velocity, respectively. The mobilities μ_n and μ_p are only constant for a low electric field. It will be shown below that the drift velocities of electrons and holes saturate for large values of the electric field.

For the calculation of the speed of photodetectors we not only need the mobilities and the electric field but also the width of the space-charge region, where an electric field is present. In the so-called depletion approximation, i.e. with n and p approximately equal to zero in the space-charge region and $\rho = 0$ outside the space-charge region, the distribution of the electric field and the width of the space-charge region W can be calculated analytically for an abrupt PN junction:

$$W = \sqrt{\frac{2\epsilon_r \epsilon_0}{q} \frac{N_A + N_D}{N_A N_D} \left(U_D - U - \frac{2k_B T}{q} \right)}, \quad (1.20)$$

Fig. 1.4 Depletion layer width versus doping concentration of the lower doped side of a PN junction



with

$$U_D = \frac{k_B T}{q} \ln \frac{N_A N_D}{n_i^2}. \quad (1.21)$$

Let us assume that one side of the PN junction is doped to a much larger extent than the other, for instance $N_D = 10^{20} \text{ cm}^{-3} \gg N_A = 10^{16} \text{ cm}^{-3}$ or vice versa. We want to define the lower doping concentration as N_I . Equation (1.20) then can be simplified to

$$W = \sqrt{\frac{2\epsilon_r \epsilon_0}{q N_I} \left(U_D - U - \frac{2k_B T}{q} \right)}. \quad (1.22)$$

For the reverse voltage U , here, a negative value always has to be used. The space-charge region only spreads into the low doped side of the PN junction due to the simplification. This behavior, however, is a good approximation for most semiconductor diodes and for photodiodes, accordingly. The width of the space-charge region as a function of the doping concentration of the low doped side of the PN junction is shown in Fig. 1.4.

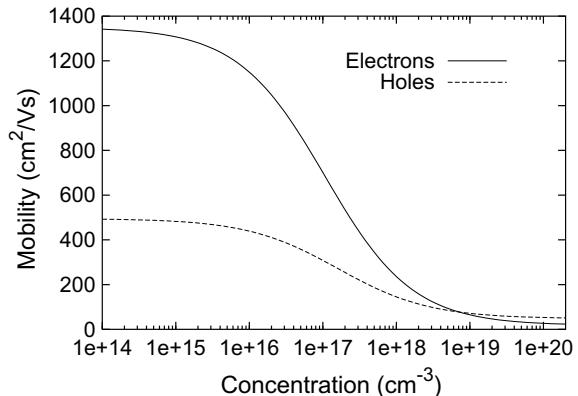
1.3 Important Models for Photodetectors

The most important processes for the characterization of photodetectors with respect to their speed are carrier drift and minority carrier diffusion. The carrier drift in conventional semiconductor materials is a much faster process than the minority carrier diffusion. For the calculation of the frequency response of photodiodes, series resistances and PN junction capacitances are also important. An even more complete equivalent circuit for photodiodes considering wiring capacitances will be discussed. Minority carrier diffusion, series resistances and capacitances reduce the speed of photodiodes.

Table 1.2 Parameter values for the approximation of the electron and hole mobilities in silicon with (1.23) and (1.24)

Parameter	Electrons	Holes
μ_{\min} (cm ² /Vs)	17.8	48.0
μ_{\max} (cm ² /Vs)	1350	495
N_{ref} (cm ⁻³)	1.072×10^{17}	1.606×10^{17}
$\nu_{n,p}$	-2.3	-2.2
$\chi_{n,p}$	-3.8	-3.7
$\alpha_{n,p}$	0.73	0.70

Fig. 1.5 Carrier mobilities in silicon versus total doping concentration [6, 7]



1.3.1 Carrier Drift

The carrier mobilities in the drift terms (see (1.13) and (1.14)) are the parameters which are responsible for the obtainable speed of photodetectors. The carrier mobilities depend on the doping concentration and on the electric field. An empirical expression is available for the dependence of the mobility on the total impurity concentration N_{total} , which also considers the influence of temperature T in K [6, 7]:

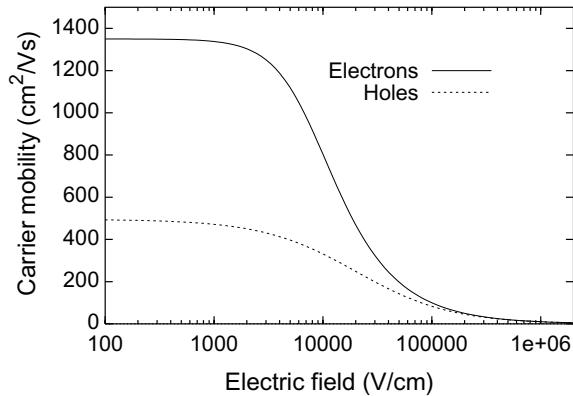
$$\mu_{0n} = \mu_{n,\min} + \frac{\mu_{n,\max}(T/300)^{\nu_n} - \mu_{n,\min}}{1 + (T/300)^{\chi_n} (N_{\text{total}}/N_{\text{ref},n})^{\alpha_n}}, \quad (1.23)$$

$$\mu_{0p} = \mu_{p,\min} + \frac{\mu_{p,\max}(T/300)^{\nu_p} - \mu_{p,\min}}{1 + (T/300)^{\chi_p} (N_{\text{total}}/N_{\text{ref},p})^{\alpha_p}}. \quad (1.24)$$

N_{total} is the sum of the concentrations of acceptors and donors. The other parameters for silicon are listed in Table 1.2.

The dependence of the carrier mobilities in silicon on the doping concentration according to (1.23) and (1.24) is shown in Fig. 1.5 for $T = 300$ K.

Fig. 1.6 Carrier mobilities versus electric field for weakly doped silicon



According to [6], the dependence of the carrier mobilities in silicon on the electric field can be approximated by

$$\mu_n = \frac{\mu_{0n}}{1 + (\mu_{0n} E / v_n^{\text{sat}})^2}, \quad (1.25)$$

$$\mu_p = \frac{\mu_{0p}}{1 + (\mu_{0p} E / v_p^{\text{sat}})^2}. \quad (1.26)$$

The values for the saturation velocities (in cm/s) can be computed from the expression [8] with T in K:

$$v_n^{\text{sat}}(T) = v_p^{\text{sat}}(T) = \frac{2.4 \times 10^7}{1 + 0.8 \exp(T/600)}. \quad (1.27)$$

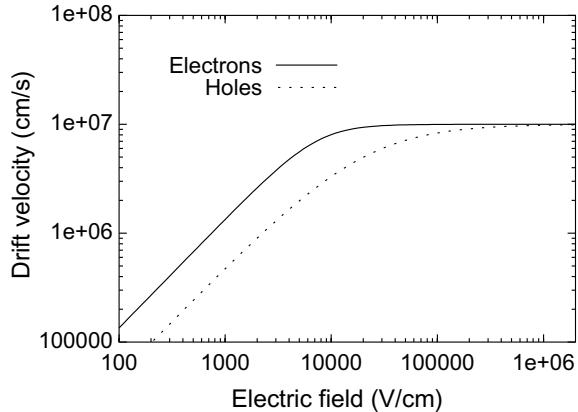
The curves calculated with (1.25) and (1.26) are shown in Fig. 1.6 for a very low doping concentration, i.e. for the ‘intrinsic’ zone of a PIN photodiode. The carrier mobilities begin to degrade for electric fields in excess of approximately 2000 V/cm.

The drift velocities, therefore, are proportional to the electric field only for smaller values of the electric field (Fig. 1.7). For values of the electric field larger than approximately 10,000 V/cm the electron drift velocity saturates. For holes, the electric field has to exceed a value of approximately 100,000 V/cm in order to obtain the hole saturation velocity.

The dependence of the carrier mobilities on the doping concentration is implemented in MEDICI with the CONMOB model [5]. The model in MEDICI for the dependence of the carrier mobilities, i.e. of the drift velocities on the electric field is called FLDMOB.

One quantity, which should be mentioned here, is the drift time, i.e. the time needed by carriers to drift through the whole width W of the space-charge region or drift zone. The drift time is determined by the drift velocity v and by the width of

Fig. 1.7 Carrier drift velocities in silicon versus electric field calculated according to (1.19), (1.25) and (1.26) for a low doping concentration



the drift zone W . The drift velocity v depends on μ and E . Furthermore, μ depends on the doping concentration. The doping concentration and the bias voltage applied to the photodiode determine the distribution of the electric field. It is, therefore, very difficult to calculate the drift time analytically, because v , μ and E in a real photodiode depend on the space coordinates. Numerical process and device simulations, in general, are necessary in order to compute the transient response of photodetectors.

When we choose the ideal PIN photodiode with a constant electric field for instance (see Fig. 1.8), it is possible to give some analytical expressions for the drift time t_d and for the rise and fall times t_r and t_f of the photocurrent (time difference between the 10 and 90% values of the stationary photocurrent) [9]:

$$t_d = t_r = t_f = \frac{d_I}{v(E_0)}. \quad (1.28)$$

Instead of W , the thickness of the intrinsic I-layer of the ideal PIN photodiode d_I is used in (1.28). For a large reverse voltage, which results in a large value of the electric field, the drift velocities may be approximated by the saturation velocity v_s and

$$t_d = t_r = t_f = \frac{d_I}{v_s} \quad (1.29)$$

results. The rise and fall times limit the maximum data rate DR of optical receivers. The maximum data rate of a photodiode (in the non-return-to-zero transmission mode) can be estimated in a conservative way to be the lower value of $DR = 1/(3t_r)$ and $DR = 1/(3t_f)$. The mean value of t_r and t_f may lead to $DR = 2/(3(t_r + t_f))$. In a more aggressive way, instead of the factor 3, the factor 2 can be used, however, in practice the bit-error rate of optical receivers determines the usable data rate. The relation between the rise time and the -3 dB bandwidth should also be mentioned [10, 11]:

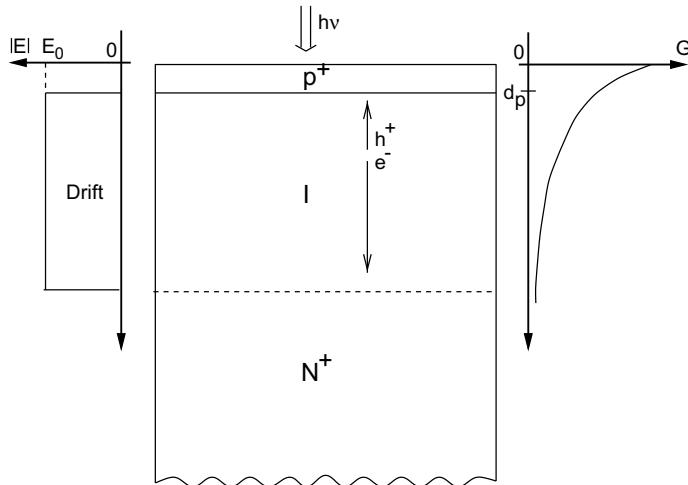


Fig. 1.8 Drift region in an ideal PIN photodiode with an undoped intrinsic I-layer

$$f_{3\text{dB}} = \frac{2.4}{2\pi t_r} \approx \frac{0.4v_s}{W}. \quad (1.30)$$

This equation was obtained for a time-dependent sinusoidal photogeneration at the surface of the PIN photodiode after integrating the conduction current density and the displacement current density over the drift zone thickness [11]. The amplitude of the short circuit photocurrent density dropped to $1/\sqrt{2}$ of its low-frequency value for $\omega t_d = 2.4$ leading to (1.30) when assuming that the transit time t_d is equal to the rise time t_r . When the thickness of the intrinsic I-layer is chosen as $W = d_I = 1/\alpha$, a simple expression is obtained for the -3 dB frequency of a PIN photodiode:

$$f_{3\text{dB}} \approx 0.4\alpha v_s. \quad (1.31)$$

Another case, for which an analytical solution may be justified, is a PN photodiode with a very large electric field. Then $v \approx v_s$ and $t_d = W/v_s$ may be used.

The electric field in most real photodiodes, however, is much lower than would be necessary in order to justify the assumption of the saturation velocities. The electric field in real PIN photodiodes also is not constant even at the low ‘intrinsic’ doping level of 10^{13} cm^{-3} [12] and, besides, a rather limited validity range of $\alpha d_I > 3$ for an analytical model, process and device simulations for the computation of the rise and fall times are necessary for real PIN photodiodes. These process and device simulations are also capable of considering the influence of carrier diffusion, which will be discussed next, on the transient behavior of photodetectors.

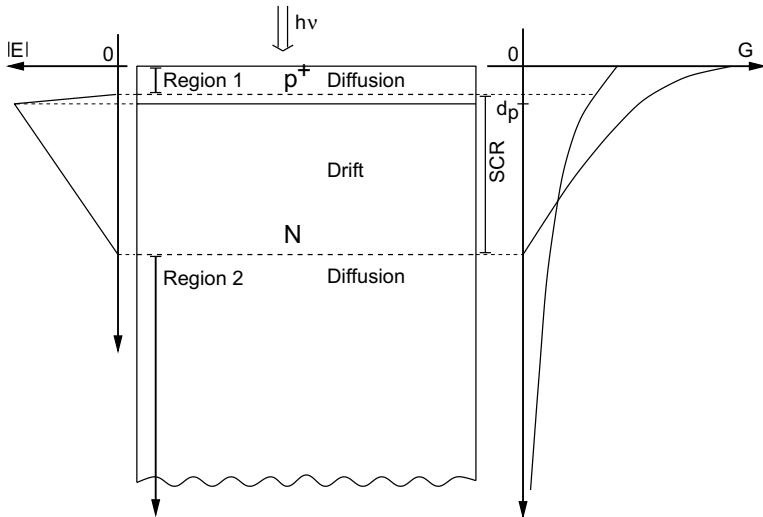


Fig. 1.9 Drift and diffusion regions in a photodiode

1.3.2 Carrier Diffusion

The diffusion of minority carriers is important for the calculation of the speed of photodetectors, when electron–hole pairs are generated in the quasineutral regions of the semiconductor where no electric field is present. There can be two such regions in a photodiode. The first region is the heavily doped surface region (P^+ in Fig. 1.9), which, however, in most cases is not very thick. The second and usually more critical region is in the depth of the semiconductor below the edge of the space-charge region SCR (see Fig. 1.9).

The carrier diffusion coefficients D_n and D_p depend on the carrier mobilities according to the Einstein relation

$$D_{n/p} = \mu_{n/p} \frac{k_B T}{q} = \mu_{n/p} U_T. \quad (1.32)$$

The value of the diffusion coefficient of electrons in Si is only approximately $35 \text{ cm}^2/\text{s}$ for low doping concentrations. The value reduces considerably for high doping concentrations. The diffusion coefficient of holes in Si is less than $12.5 \text{ cm}^2/\text{s}$ and also depends on the doping concentration.

The distance over which minority carriers diffuse is called the carrier diffusion length L_n or L_p for electrons or holes, respectively. The carrier diffusion lengths depend on the carrier diffusion coefficients and on the carrier lifetimes τ_n and τ_p :

$$L_n = \sqrt{D_n \tau_n}, \quad (1.33)$$

$$L_p = \sqrt{D_p \tau_p}. \quad (1.34)$$

The carrier lifetimes are due to dopants and unwanted impurities in the semiconductor, which are unavoidably introduced in quite small but noticeable amounts in electronic devices during the fabrication process. These impurities may act as recombination centers. Recombination centers introduce deep energy levels in the bandgap, which enhance the recombination rate of electrons and holes [13–15]. Short carrier lifetimes result in a large recombination rate. The Shockley–Read–Hall (SRH) generation/recombination rate U_{th} is implemented in MEDICI in this form [5]:

$$U_{th} = U_n = U_p = \frac{pn - n_i^2}{\tau_p[n + n_i \exp((E_t - E_i)/k_B T)] + \tau_n[p + n_i \exp((E_i - E_t)/k_B T)]}. \quad (1.35)$$

The recombination rate U_{th} depends on the densities of electrons and holes, on the intrinsic carrier density n_i , on the carrier lifetimes τ_n , τ_p , and on the difference between the energy level of the recombination center E_t and the intrinsic Fermi level E_i . The carrier lifetimes themselves depend on the total impurity density N_{total} [5]:

$$\tau_n = \frac{\tau_{0,n}}{1 + N_{total}/N_{SRH,n}}, \quad (1.36)$$

$$\tau_p = \frac{\tau_{0,p}}{1 + N_{total}/N_{SRH,p}}. \quad (1.37)$$

In N_{total} , dopants and recombination centers have to be considered. The carrier lifetimes for low doping concentrations and low densities of recombination centers are $\tau_{0,n}$ and $\tau_{0,p}$, respectively. The reference parameters $N_{SRH,n}$ and $N_{SRH,p}$ for silicon are both equal to $5 \times 10^{16} \text{ cm}^{-3}$.

Equation (1.35) can be simplified for $\tau_n = \tau_p$ and it can be seen that the recombination rate approaches a maximum for $E_t = E_i$. The carrier lifetimes are inversely proportional to the recombination rate for low injection conditions, i.e., when the densities of injected carriers $\Delta n = \Delta p$ are much smaller than the density of majority carriers.

The minority carrier lifetime (hole lifetime) in an N-type semiconductor then is

$$\tau_p = (\sigma_p v_{th} N_t)^{-1}. \quad (1.38)$$

The electron lifetime in a P-type semiconductor similarly is

$$\tau_n = (\sigma_n v_{th} N_t)^{-1}. \quad (1.39)$$

The carrier capture cross sections σ_n , σ_p , the thermal carrier velocity v_{th} and the density of unwanted impurities N_t determine the minority carrier lifetimes in low doped silicon.

The minority carrier lifetimes in as grown silicon can reach several milliseconds, whereas the fabrication process of photodetectors or integrated circuits can reduce the carrier lifetimes to the order of microseconds. Usually the minority carrier lifetimes are important only when carrier diffusion is the dominating transport mechanism. Drift times are usually of the order of nanoseconds and carrier lifetimes of the order of microseconds do not deteriorate the quantum efficiency of photodetectors when carrier drift is dominating.

Carrier diffusion is the dominant aspect in solar cells, which do not need a very quick transient response to changing light intensities [16]. The spectrum of the sun contains rather long wavelengths, which penetrate several tens of micrometers into silicon. Therefore, many electron–hole pairs are generated in region 2 (see Fig. 1.9), where carrier diffusion occurs. In order to obtain a high quantum efficiency of a solar cell, a long carrier diffusion length and, therefore, a long carrier lifetime is necessary in the semiconductor. The long carrier lifetimes in silicon with a highly developed crystal growth and process technology are the reason why silicon is the dominant material in solar cell production. The interested reader will find the state of the art in solar cell technology in [17–20], for instance.

Other optoelectronic devices, where carrier diffusion is important, are bipolar phototransistors. The diffusion of minority carriers in the base of bipolar transistors limits their switching speed and their transit frequency [21]. We will return to photodiodes here.

We want to estimate the time t_{diff} for the diffusion of electrons through a P⁺ region with thickness d_p [22, 23]

$$d_p = \sqrt{2D_n t_{diff}}. \quad (1.40)$$

This equation has been derived for a time-dependent sinusoidal electron density due to photogeneration in the P⁺ layer from the electron diffusion equation [23]. The time response of a low-pass filter with time constant $\tau_r = d_p^2/(2D_n)$ was obtained and this time constant was interpreted as the time t_{diff} that electrons need to diffuse to the space-charge region at the P⁺N junction. With (1.32), t_{diff} can be obtained:

$$t_{diff} = \frac{d_p^2 q}{2\mu_n k_B T}. \quad (1.41)$$

A much slower contribution to the photocurrent usually results from carriers being generated in the second diffusion region (see Fig. 1.9), because the holes have to diffuse a much longer distance than d_p from this region 2 to the space-charge region. The hole diffusion time through 10 μm of silicon is 40 ns whereas the electron diffusion time over the same distance is approximately 8 ns. The resulting shape of the photocurrent shown in Fig. 1.10 is characteristic of the diffusion of carriers from

Fig. 1.10 Transient behavior of the photocurrent for carrier drift and diffusion

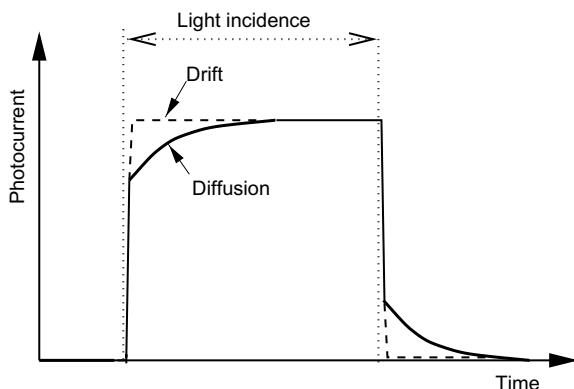
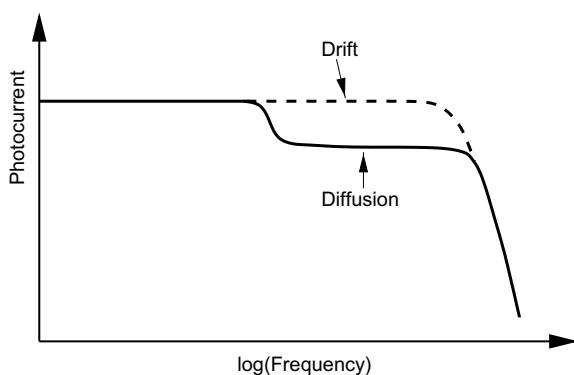


Fig. 1.11 Frequency response of the photocurrent for carrier drift and diffusion



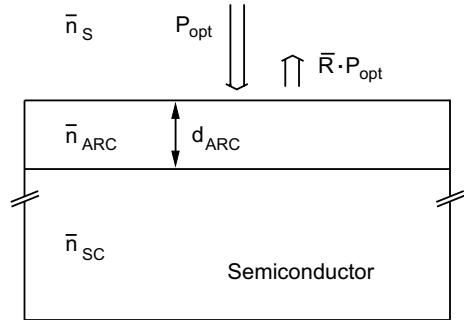
the second region into the space-charge region. The influence of carrier diffusion on the frequency response of photodetectors is shown in Fig. 1.11.

Summarizing, it can be concluded that carrier diffusion should be avoided in order to obtain fast photodetectors. One possibility is to use light with a short wavelength, i.e. with a large absorption coefficient in Si in order to avoid photogeneration in region two (see Fig. 1.9). Another possibility can be the choice of a semiconductor with larger absorption coefficients. Where neither of these measures is possible, a larger reverse voltage should be applied across the photodiode or the doping concentration in the photodiode should be reduced, in order to obtain a thicker space-charge region.

1.3.3 Quantum Efficiency and Responsivity

The total, external or overall quantum efficiency η is defined as the number of photogenerated electron–hole pairs, which contribute to the photocurrent, divided by the number of the incident photons. The external quantum efficiency can be

Fig. 1.12 Semiconductor with an antireflection coating



determined, when the photocurrent of a photodetector is measured for a known incident optical power.

A fraction of the incident optical power is reflected (see Fig. 1.2) due to the difference in the index of refraction between the surroundings \bar{n}_s (air: $\bar{n}_s = 1.00$) and the semiconductor \bar{n}_{sc} (e.g. Si, $\bar{n}_{sc} \approx 3.5$). The reflectivity \bar{R} depends on the index of refraction \bar{n}_{sc} and on the extinction coefficient $\bar{\kappa}$ of an absorbing medium, for which the dielectric function $\bar{\epsilon} = \bar{\epsilon}_1 + i \bar{\epsilon}_2 = (\bar{n}_{sc} + i \bar{\kappa})^2$ is valid ($\bar{n}_s = 1$) [3].

$$\bar{R} = \frac{(1 - \bar{n}_{sc})^2 + \bar{\kappa}^2}{(1 + \bar{n}_{sc})^2 + \bar{\kappa}^2}. \quad (1.42)$$

The extinction coefficient is sufficient for the description of the absorption. The absorption coefficient α can be expressed as:

$$\alpha = \frac{4\pi\bar{\kappa}}{\lambda_0}. \quad (1.43)$$

The optical quantum efficiency η_o can be defined in order to consider the partial reflection:

$$\eta_o = 1 - \bar{R}. \quad (1.44)$$

The reflected fraction of the optical power can be minimized by introducing an antireflection coating (ARC) with thickness d_{ARC} (see Fig. 1.12):

$$d_{ARC} = \frac{\lambda_0}{4\bar{n}_{ARC}}. \quad (1.45)$$

The index of refraction of the ARC-layer can be calculated:

$$\bar{n}_{ARC} = \sqrt{\bar{n}_s \bar{n}_{sc}}. \quad (1.46)$$

The optimum index of refraction of the ARC-layer is determined by the refractive index \bar{n}_s of the surroundings and by the refractive index \bar{n}_{sc} of the semiconductor.

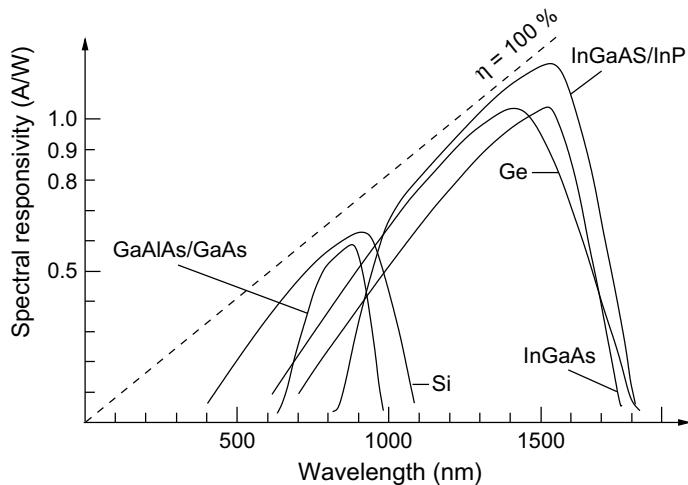


Fig. 1.13 Comparison of the responsivity of real photodetectors with an ideal photodetector with a quantum efficiency $\eta = 1$ (100%) [24]

A complete suppression of the partial reflection, however, is not possible in practice. For silicon photodetectors, SiO_2 ($\bar{n}_{\text{sc}} = 1.45$) and Si_3N_4 ($\bar{n}_{\text{sc}} = 2.0$) ARC-layers are most appropriate.

Because of the partial reflection, it is useful to define the internal quantum efficiency η_i as the number of photogenerated electron–hole pairs, which contribute to the photocurrent, divided by the number of photons which penetrate into the semiconductor.

The external quantum efficiency is the product of the optical quantum efficiency η_o and of the internal quantum efficiency η_i :

$$\eta = \eta_o \eta_i. \quad (1.47)$$

The internal quantum efficiency η_i will be discussed in Sect. 1.3.3 after carrier diffusion and drift have been introduced.

For the development of photoreceiver circuits, and especially of transimpedance amplifiers, it is interesting to know how large the photocurrent is for a specified power of the incident light with a certain wavelength. The responsivity R is a useful quantity for such a purpose:

$$R = \frac{I_{\text{ph}}}{P_{\text{opt}}} = \frac{q \lambda_0}{hc} \eta = \frac{\lambda_0 \eta}{1.243} \frac{A}{W}, \quad (1.48)$$

where λ_0 is in μm . The responsivity is defined as the photocurrent I_{ph} divided by the incident optical power. R depends on the wavelength, therefore wavelength has to be mentioned if a responsivity value is given.

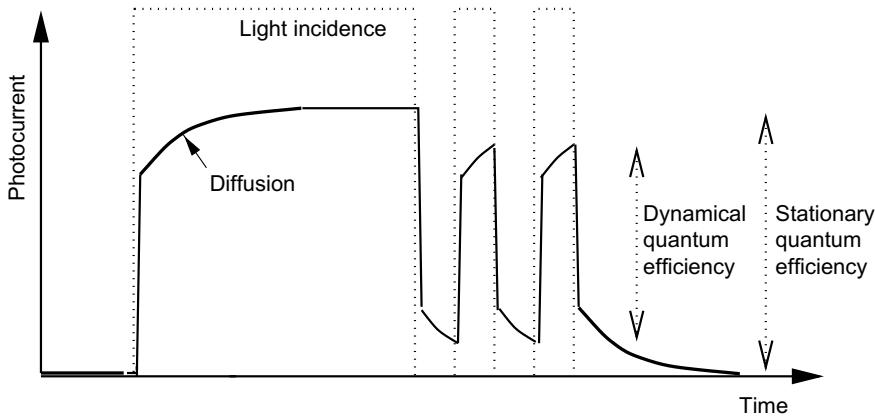


Fig. 1.14 The influence of carrier diffusion on the dynamical quantum efficiency of photodetectors at high data rates

The dashed line shown in Fig. 1.13 represents the maximum responsivity of an ideal photodetector with $\eta = 1$ or 100%. The responsivity of real detectors is always lower due to partial reflection of the light at the semiconductor surface and due to partial recombination of photogenerated carriers in the semiconductor or at its surface.

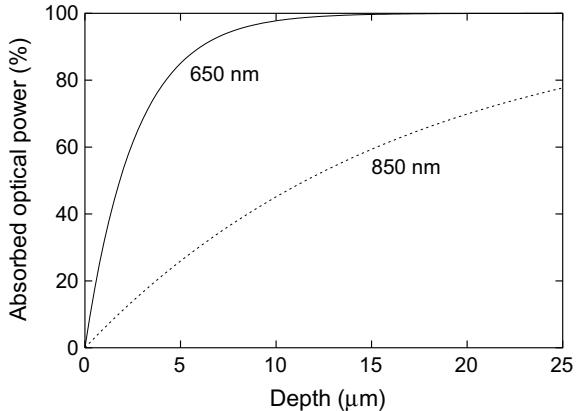
Strictly speaking we have to distinguish between the stationary and the dynamical internal quantum efficiency. In the stationary case, the light intensity and the photocurrent are constant with time. In the dynamical case both change with time. The dynamical quantum efficiency generally is lower than the stationary one.

Let us discuss the stationary case first. As explained above, practically all carriers which are photogenerated in drift regions contribute to the photocurrent. In other words, there is no negative influence of recombination on the internal quantum efficiency in the space-charge regions of photodiodes. The recombination of photogenerated carriers in region 1 and 2 (see Fig. 1.9), however, reduces the internal quantum efficiency. In the highly doped region 1, the carrier lifetime is reduced considerably according to (1.36) and (1.37). This reduces the internal quantum efficiency for short wavelengths considerably, because a large portion of the light is absorbed in region 1.

Light with long wavelengths penetrates deep into silicon and the recombination of photogenerated carriers in region 2 can reduce the internal quantum efficiency. The recombination of photogenerated carriers in region 1 is not very important for long wavelengths due to the large penetration depth and the small portion of photogenerated carriers in region 1.

In the dynamical case, carriers being photogenerated in region 1 and especially in region 2 do not have enough time to diffuse to the space-charge or drift region before the light intensity is reduced again. The diffusion tails of the photocurrent of consecutive light pulses overlap (Fig. 1.14). The photocurrent for a sine-wave

Fig. 1.15 Absorbed optical power as a function of depths in silicon



light modulation reduces similarly at high frequencies (see Fig. 1.11). It should be mentioned explicitly that the dynamical quantum efficiency depends on the frequency or data rate. The higher both these are, the smaller the dynamical quantum efficiency becomes until the minimum is reached. This minimum is set by the portion of carriers being generated in the space-charge region, when we assume that the frequency is not extremely high and all drifting carriers still reach the boundary of the space-charge region and contribute to the photocurrent. For this case, we can use the expression

$$\eta_i = (1 - \exp[-\alpha(d_p + d_l)]) \exp(-\alpha d_p) \quad (1.49)$$

to describe the dynamical internal quantum efficiency. This expression was derived for ideal PIN photodiodes (compare with Fig. 1.8) with the thickness d_l of the intrinsic region, i.e. the thickness d_l of the drift region. We can also use (1.49) for a PN photodiode shown in Fig. 1.9 to a good approximation because the space-charge region with the thickness d_l does not penetrate far into the highly doped P⁺ layer.

Figure 1.15 can be used in a good approximation for the dynamical quantum efficiency of a silicon photodiode with a shallow N⁺ or P⁺ surface region, if the depth represents the width of the space-charge region and if reflection at the Si surface is neglected, i.e. if an optimized antireflection coating is assumed. Figure 1.15 illustrates that for red light (650 nm) it is much easier to achieve a fast photodiode with a dynamical quantum efficiency close to 100% than for near infrared light (850 nm), where a much thicker absorption region, i.e. a much wider space-charge region, is required. For 650 nm, an absorption region with a thickness of about 10 μm is sufficient to achieve almost 100% dynamical quantum efficiency, whereas for 850 nm wavelength only about 45% result for this absorption region and an absorption region with a thickness of 25 μm results only in a dynamical quantum efficiency of about 80%.

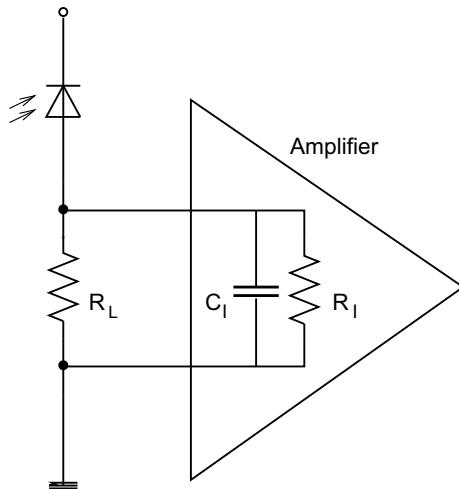


Fig. 1.16 Essential input circuit of a photoreceiver

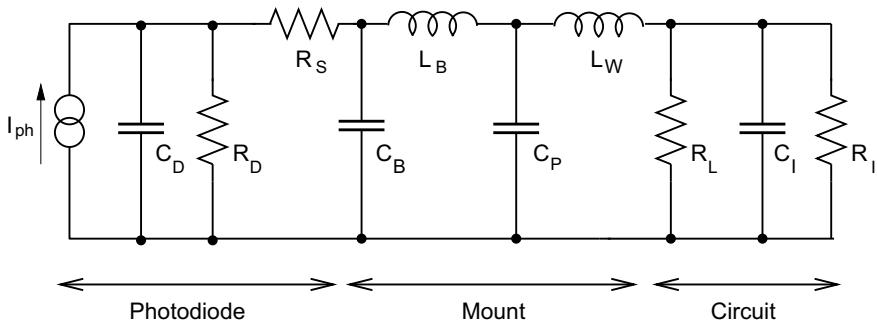


Fig. 1.17 Small-signal equivalent input circuit of a photoreceiver

1.3.4 Equivalent Circuit of a Photodiode

A photoreceiver consists at least of a photodetector, of a load resistor R_L , and of an amplifier with an input capacitance C_I and with an input resistance R_I (Fig. 1.16). The input resistance R_I can be neglected for amplifiers with a JFET or MOS input transistor. R_I , however, is important for amplifiers with a bipolar input transistor.

The complete equivalent input circuit of the photoreceiver considering parasitics due to mounting is shown in Fig. 1.17. The equivalent circuit of a photodiode is obtained without mount parasitics and without R_L , C_I , and R_I .

The current source I_{ph} represents the photocurrent in Fig. 1.17. C_D is the capacitance of the space-charge region of the photodiode. C_B is the capacitance of the bondpad of the photodiode. L_B represents the inductance of the bond wire. The stray capacitance of the detector package is considered in C_P . A typical value for

photodiode chips and integrated circuits is $C_B = 0.2\text{--}0.3 \mu\text{F}$. The stray capacitance of package pins of discrete photodiodes and of the output pins of integrated circuits is of the order of $1 \mu\text{F}$. The lead wires and the wiring on electronic boards introduce the additional inductance L_W . The inductances L_B and especially L_W become important at high frequencies.

The parallel resistor R_D , which models the reverse, leakage, or dark current of a photodiode usually is very large and can be neglected in most cases. The series resistance R_S may not be neglected when the photocurrent has to flow through low doped regions in the photodiode. R_S should be negligible for PIN photodiodes with highly doped P and N regions, when carrier drift dominates, i.e. when the ‘intrinsic’ zone is fully depleted.

The time constant t_D for a PIN photodiode with a connected amplifier is, in general, when the inductances can be neglected:

$$t_D = (R_L \| R_I)(C_D + C_B + C_P + C_I). \quad (1.50)$$

The -3 dB bandwidth $f_{3\text{dB}}$ of the input circuit of a photoreceiver is then

$$f_{3\text{dB}} = \frac{1}{2\pi(R_L \| R_I)(C_D + C_B + C_P + C_I)}. \quad (1.51)$$

Optoelectronic integrated circuits (OEICs) avoid the bondpad and package capacitances and the inductances of bond and lead wires as well as the inductance of wiring on electronic boards. Optoelectronic integrated circuits, therefore, reach a larger bandwidth $f_{3\text{dB}} = 1/(2\pi(R_L \| R_I)(C_D + C_I))$. OEICs with a MOSFET or JFET input stage of the amplifier possess a very large input resistance and the bandwidth can be written as $f_{3\text{dB}} = 1/(2\pi R_L(C_D + C_I))$.

For a reverse-biased abrupt PN junction, for which one doping type is present in a concentration several orders of magnitude larger than the other doping type, the capacitance is given by

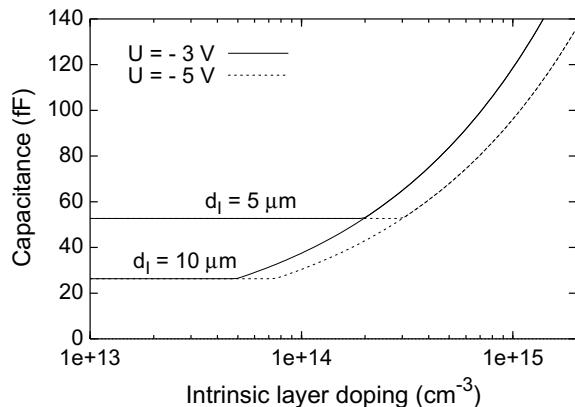
$$C_D = A \sqrt{\frac{q\epsilon_r\epsilon_0 N_{A/D}}{2}} \frac{1}{\sqrt{U_D - U - (2k_B T/q)}}, \quad (1.52)$$

with

$$U_D = \frac{k_B T}{q} \ln \frac{N_A N_D}{n_i^2}. \quad (1.53)$$

These prerequisites for the doping concentrations are usually fulfilled in photodiodes. For P^+N or N^+P photodiodes, an abrupt PN junction is a good approximation. Equation (1.52), therefore, approximates the capacitance of most photodiodes quite well. For photodiodes with deeply diffused doping regions like N-well to P-substrate photodiodes in CMOS technology, the capacitance can be calculated with the expression for linearly graded junctions [8]. However, deeply diffused doping

Fig. 1.18 Capacitance of PN and PIN diodes with an area of $2500 \mu\text{m}^2$ versus doping concentration. In the constant capacitance regime, the diode can be considered as a PIN diode. For larger doping concentrations, it is not appropriate to call the diode a PIN diode, because the ‘intrinsic’ zone is not fully depleted



regions should be avoided in silicon photodiodes at least for short wavelengths in order to keep the quantum efficiency high.

In (1.52), $N_{A/D}$ represents the doping concentration of the low doped side of the PN junction. A negative value has to be used for the reverse bias of the photodiode U .

For a so-called PIN structure, in which high doped P and N regions are at the two sides of a low doped ‘intrinsic’ zone with thickness d_I , the capacitance is approximately that of a plate capacitor (neglecting the boundary capacitance):

$$C_D^{\text{PIN}} = A \frac{\epsilon_r \epsilon_0}{d_I}, \quad (1.54)$$

where A is the area of the P^+ -doped (PIN photodiode) or N^+ -doped (NIP photodiode) region at the surface of the device.

Figure 1.18 depicts the capacitances according to (1.54) and (1.52) as a function of the doping concentration $N_{A/D}$. A diode area A of $2500 \mu\text{m}^2$, thereby, was assumed. When the doping level is reduced starting from 10^{15} cm^{-3} , the capacitance first decreases according to (1.52) until the space-charge region spreads across the whole thickness d_I of the intrinsic zone. Then C_D remains constant according to (1.54), when the doping level is reduced further. For a reverse bias of 3 V and $d_I = 5 \mu\text{m}$, the capacitance finally remains constant at a value of 53 fF, when the doping concentration drops below approximately $2 \times 10^{14} \text{ cm}^{-3}$. For $d_I = 10 \mu\text{m}$, the capacitance remains constant at a value of 26.5 fF, when the doping concentration falls below approximately $5 \times 10^{13} \text{ cm}^{-3}$. For the larger reverse bias of 5 V, constant capacitances are already reached for slightly larger doping levels (see Fig. 1.18).

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Chapter 2

Integrated Silicon Photodetectors



In this chapter the bipolar, CMOS, and BiCMOS process technologies are described. Photodetectors which are produced in these technologies without process modifications and their properties are introduced. Furthermore, the possible improvements of photodetectors resulting from small substrate and process modifications are discussed.

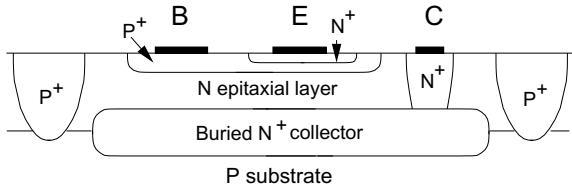
CMOS is the economically most important technology. The section on integrated photodetectors in CMOS technology, therefore, is more comprehensive than the sections on photodetectors in bipolar and BiCMOS technologies. Within the CMOS section, the sophisticated spatially-modulated-light (SML) detector suppressing slow carrier diffusion effects in standard CMOS will be described. Furthermore, the photonic mixer device (PMD) being relevant for future 3D cameras on a chip will be discussed. In addition, the innovative integration of vertical PIN photodiodes will be highlighted, since they allow a considerable improvement of the speed of CMOS OEICs. Avalanche photodiodes and single-photon avalanche diodes are explained. Triple-well processes are explained with respect of their isolation capabilities. Furthermore, image sensors using charge-coupled-devices and active pixel image sensors will be described in some detail because of their economical importance. Within the BiCMOS section, the exploitation of double photodiodes will be mentioned as another innovation for high-speed OEICs and OPTO-ASICs in standard technology. With some process modifications, a very fast vertical PIN photodiode was realized in BiCMOS technology.

2.1 Integrated Detectors in Bipolar Technology

2.1.1 Bipolar Processes

In the standard buried collector (SBC) technology [1], the N⁺ collector is implanted in the P-type substrate and an N-type epitaxial layer is grown, which serves as the N⁻ collector (Fig. 2.1).

Fig. 2.1 Schematic cross section of an NPN transistor in SBC technology [1]



The P⁺ isolation, the N⁺-collector contact, the P-type base, and the N⁺ emitter are implanted and annealed subsequently. In modern technologies, polysilicon emitters [2] and polysilicon extrinsic bases [3], oxide isolation [4, 5], or recessed oxide isolation [6, 7] are used. Alternatively, trench isolation [8–10] is also used. Here, however, a simple process flow (Fig. 2.2) will be described, in order to demonstrate more agreement with [11], where a vertical PIN photodiode has been integrated (see Fig. 2.7).

The P-type substrate with a doping concentration of $\approx 10^{15} \text{ cm}^{-3}$ is oxidized (Fig. 2.2a). Then the area for the buried collectors is defined by lithography (M1). Arsenic is diffused or, more recently, antimony is implanted (Fig. 2.2b) to form the N⁺ subcollector, which is needed to minimize the collector series resistance. Subsequently, the N[−] collector layer is grown epitaxially (Fig. 2.2c). An oxidation is performed (Fig. 2.2c) and the areas for device isolation are defined by lithography (M2). Boron is diffused and driven in under oxidizing conditions (Fig. 2.2d). The resulting P⁺ regions reach the P substrate and isolate the NPN transistor from neighboring transistors. Then lithography is applied to define the base area (M3). Boron is implanted in this area (Fig. 2.2e) and annealed partially under oxidizing conditions. The emitter area and the collector contact area are defined next (M4) and implanted with phosphorus (Fig. 2.2f) or arsenic. The annealing is again performed partially under oxidizing conditions. The contact holes are defined by lithography (M5) and aluminum is deposited (Fig. 2.2g) and structured by lithography (M6) in order to obtain interconnects (Fig. 2.2h). After oxide and nitride deposition for passivation, a seventh lithography step is needed for the opening of the bondpads. Seven steps of lithography are applied in total for this simple bipolar process with one metal layer. This simple process has often been varied and supplemented [12]. A second metal layer for instance would result in two additional lithography steps. An additional mask before M2 is required for a deep collector contact diffusion (collector plug) in order to eliminate the N[−] region and the resulting collector series resistance between N⁺ collector contact and N⁺ subcollector resulting in a single N⁺ path from the collector contact to the subcollector (see Fig. 2.1).

For our purposes, however, this simple process will be sufficient to explain the photodetectors available in bipolar processes without modifications (see Sect. 2.1). It will also be sufficient to understand the complexity of PIN photodiode integration, which will be discussed in Sect. 2.1.3.

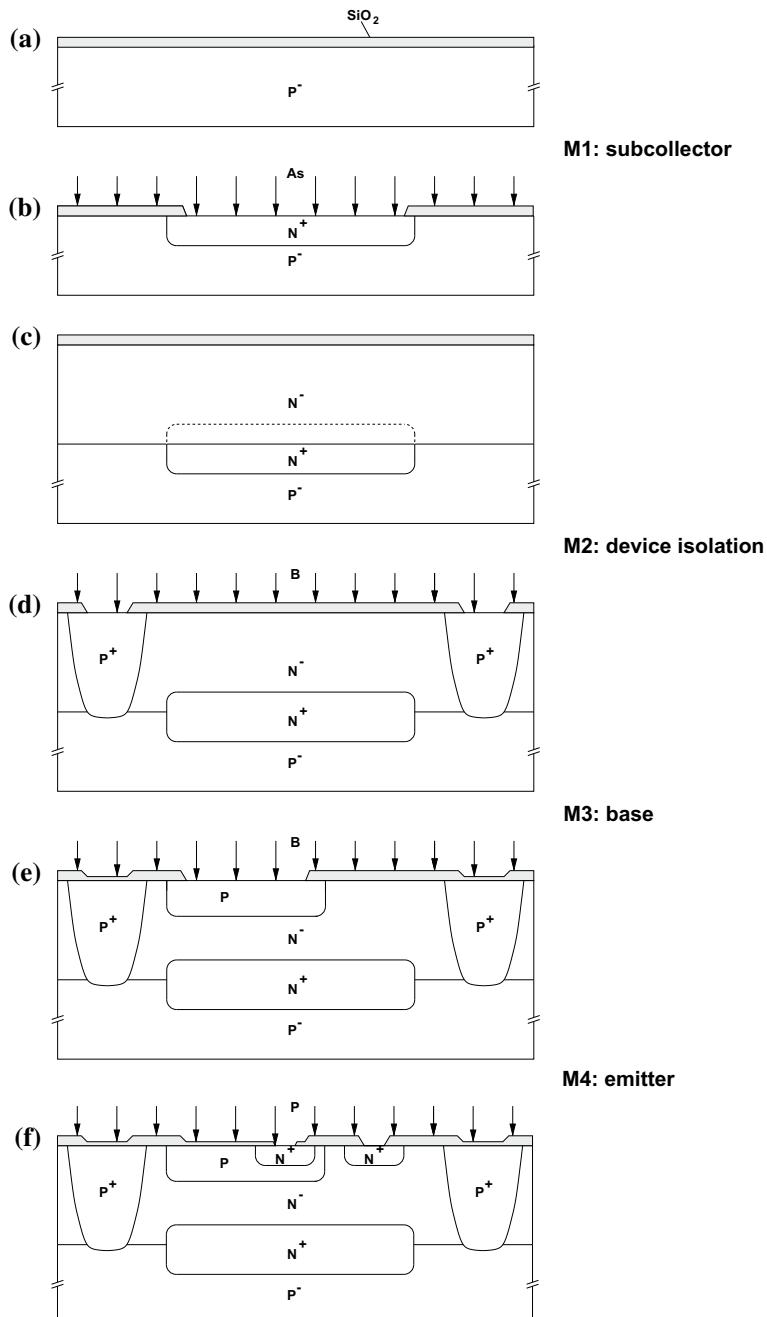


Fig. 2.2 Simplified process flow of SBC bipolar technology. **a–e** subcollector, device isolation, and base formation, **f–h** emitter, contact hole, and interconnect formation [12]

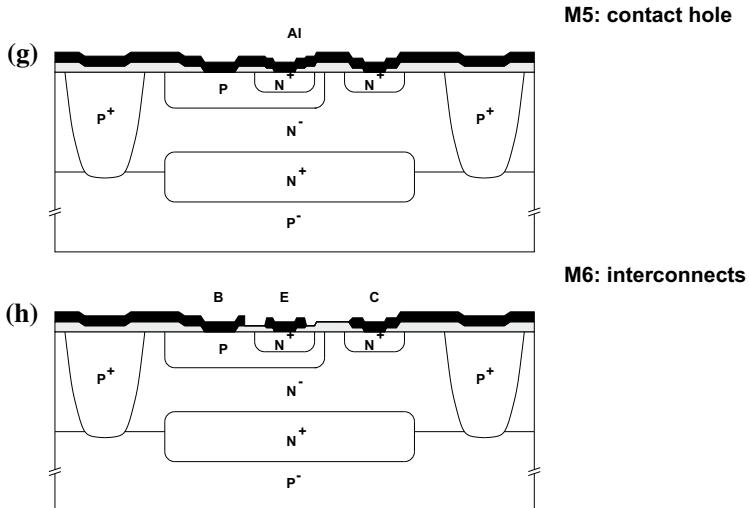


Fig. 2.2 (continued)

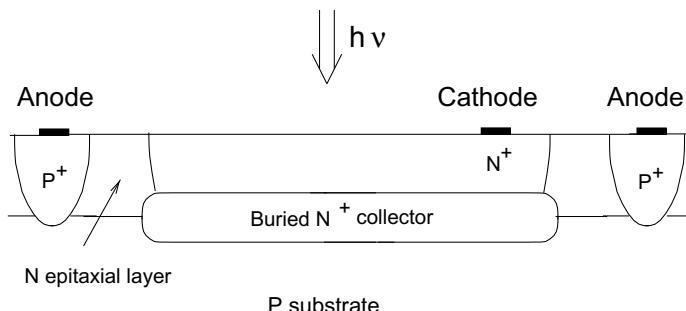


Fig. 2.3 Schematic cross section of a subcollector to substrate photodiode

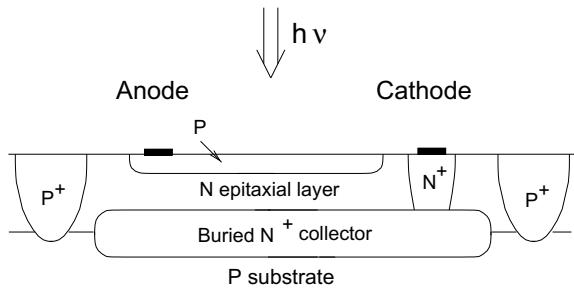
2.1.2 Integrated Detectors in Standard Bipolar Technology

Photodiodes

An N⁺/P substrate photodiode can be obtained in a bipolar OEIC, whereby the N⁺ region is formed by the N⁺ buried collector and the deep N⁺ collector plug (Fig. 2.3).

Such a photodiode was realized in [13]. For an N^+ area of $100 \times 100 \mu\text{m}^2$, a bit rate of 150 Mb/s was reported for $\lambda = 850 \text{ nm}$. The speed of the photodiode was limited by carrier diffusion in the P substrate with a doping concentration of approximately 10^{15} cm^{-3} . The transient behavior of a smaller photodiode with an N^+ area of $10 \times 10 \mu\text{m}^2$ was much better. A rise time of 0.04 ns and a fall time of 0.4 ns was reported for this smaller photodiode with $\lambda = 820 \text{ nm}$. These values would allow a data rate DR of about 850 Mb/s, when we use the conservative estimate

Fig. 2.4 Schematic cross section of a base-collector photodiode



$DR = 1/(3t_f)$. The reverse bias of the photodiode was approximately 4.2 V. The quantum efficiency of the photodiode was 30%, which was probably due to optical interferences in the isolation and passivation layers above the photodiode.

The subcollector may be omitted in Fig. 2.3. Then the photodiode is formed by the N^+ contact diffusion and the P substrate. The N^+ penetration depth, however, will be only slightly smaller. The quantum efficiency for blue and green light will be somewhat increased.

Also, without any technological modifications, the buried N^+ collector can serve as the cathode (see Fig. 2.4), the N collector epitaxial layer can serve as the ‘intrinsic’ layer of a PIN photodiode, and the base implant can serve as the anode in order to integrate PIN photodiodes with a thin ‘intrinsic’ region in bipolar technologies [14, 15]. The process of [14] was described in [16].

The small thickness of the epitaxial layer of high-speed bipolar processes in the range of about $1\ \mu m$ causes a low quantum efficiency in the yellow to the infrared spectral region (580–1100 nm). The rise and fall times of the photocurrent for light pulses are very short due to the small epitaxial layer thickness. In [14] a bit rate of 10 Gb/s for the base-collector diode and a responsivity R of merely 48 mA/W for 840 nm were reported. This low responsivity at wavelengths from 780 to 850 nm, which are widely used for optical data transmission on short fiber lengths of up to several kilometers, is a major disadvantage of standard bipolar OEICs.

The base-collector diode with a sensitive area of $100\ \mu m^2$ fabricated in a $0.8\ \mu m$ silicon bipolar technology worked up to 3 Gb/s for a wavelength of 850 nm [15]. A sensitivity of 0.045 A/W was reported. A phototransistor with a very small sensitive area of $10\ \mu m^2$ reached a data rate of 5 Gb/s. With these monolithic silicon OEICs, a higher data rate was obtained than with a III/V photodetector and a silicon amplifier [17] showing the advantage of monolithic photodetector integration.

Emitter-base photodiodes may be useful for blue and green light when the emitters are implanted. The emitter-base diode, however, does not seem to be very advantageous, when polysilicon emitters are used in the bipolar process. The polysilicon then covers the N^+ emitter and, therefore, the light sensitive area of the photodiode completely, reducing the quantum efficiency by partial light absorption in the polysilicon. In particular, the quantum efficiency for blue and UV light would be very low.

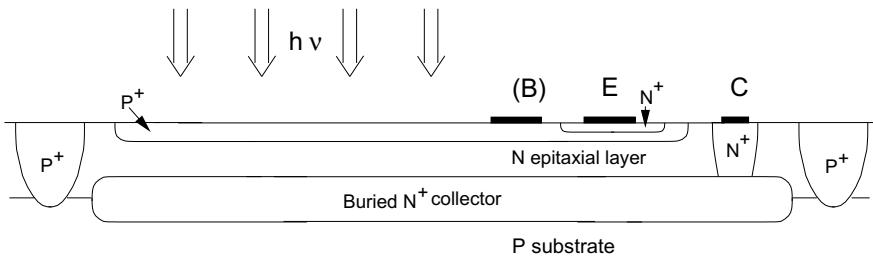


Fig. 2.5 Schematic cross section of a phototransistor in SBC technology

Phototransistors

The NPN transistor with an increased base-collector junction area can, of course, be used as a phototransistor (see Fig. 2.5). Bipolar phototransistors, simply speaking, use the base-collector diode as a photodiode and amplify the photocurrent of this diode. The P type region of this photodiode and the P-type base of the NPN transistor are one P-type region; the cathode of this photodiode and the collector of the NPN transistor consist of one N-type region. The base contact can be omitted. The electron–hole pairs generated in the base-collector space-charge region are separated by the electric field. In this space-charge region the holes are swept into the base and the electrons are swept into the collector. The holes make the base potential positive and the emitter can inject electrons into the base and towards the collector. The photocurrent of the photodiode I_{pd} is amplified by the current gain β of the NPN transistor. This amplified photocurrent is available at the collector electrode ($\beta \cdot I_{pd}$) and at the emitter ($(\beta + 1) \cdot I_{pd}$). It should be noted, however, that for long wavelengths, i.e. for large penetration depths of the light, only the fraction of the carriers photogenerated in the base-collector space-charge region will contribute to I_{pd} , which is amplified. The other fraction of the photogenerated carriers does not contribute to I_{pd} and is not amplified.

Bipolar phototransistors are known to be much slower than photodiodes. This is due to their current gain β , to the base transit time τ_B , for which carrier diffusion may be limiting, to the emitter-base space-charge capacitance C_{SE} and mainly to the rather large base-collector space-charge capacitance C_C , which results from the necessary light sensitive area. It should be mentioned that the total emitter-base capacitance C_E is the sum of the emitter-base diffusion capacitance C_{DE} and the emitter-base space-charge capacitance C_{SE} , i.e. $C_E = C_{DE} + C_{SE} = \tau_B g_m + C_{SE}$. The -3 dB frequency of a bipolar phototransistor is [18]:

$$f_{3\text{ dB}} = \frac{1}{\beta 2\pi(\tau_B + (k_B T/q I_E)(C_{SE} + C_C))} \quad (2.1)$$

This equation is the same as for a common bipolar transistor [19]. The base-collector capacitance is proportional to the size of the light-sensitive area, which is much larger in a phototransistor than the base-collector junction area of a com-

mon bipolar transistor. Therefore, the bipolar phototransistor is much slower than a combination of a PIN photodiode with a small-area common bipolar transistor. Nevertheless, a phototransistor is advantageous at low frequencies and when PIN photodiodes cannot be integrated.

For the application in optical clock distribution, a NPN transistor with a self-adjusting emitter was investigated as a phototransistor receiver for the wavelength $\lambda = 840\text{ nm}$ [14]. A double-polysilicon process [16] with a $0.5\text{ }\mu\text{m}$ thick epitaxial layer was used. The self-aligned emitter technique was used in order to realize a minimum emitter width of $0.6\text{ }\mu\text{m}$ with a $1.0\text{ }\mu\text{m}$ lithography. The current gain factor β of the transistors of 70 resulted in a relatively high sensitivity of 3.2 A/W , although the thickness of the epitaxial layer was much smaller than the penetration depth $1/\alpha = 16\text{ }\mu\text{m}$ of the light with this wavelength. A data rate of 1.25 Gb/s was reported for the NPN transistor as a phototransistor with a small size.

2.1.3 *Integrated Detectors in Modified Bipolar Technology*

UV Sensitive Photodiode

An example of a photodiode integrated in a bipolar OEIC for ultraviolet (UV) detection will also be given. An industrial application for such a sensor system is, for instance, flame detection for combustion monitoring. A spectral range has to be used in which the emitted light of the flame is more intensive than the background radiation, i.e. the black-body radiation, at the temperature of 2000 K . In the UV spectral region from 250 to 400 nm , the optical emission of the flame is much larger than the thermal background radiation from the furnace walls.

Silicon photodiodes usually have a low quantum efficiency in this UV region. The need for cheap sensor systems, however, implied the monolithic integration of the detector together with the electronic circuit in a silicon technology [20]. Additional reasons for the monolithic integration were the insensitivity of OEICs to electromagnetic interference (EMI) and a larger signal-to-noise ratio. The UV sensor was implemented in a bipolar technology [21, 22]. The cross section of the silicon UV sensor is shown in Fig. 2.6. Shallow P⁺ and N⁺ implants form the depletion region close to the crystal surface, where UV light is absorbed and carriers are generated. The depth of the implanted P⁺ and N⁺ profiles was not standard and a few additional process steps with low thermal budget and rapid thermal annealing allowed the fabrication of the UV detector and of the interface circuit on a single chip without degrading the electrical performance of the analog components.

The P⁺/N⁺ UV sensitive photodiode was fabricated in the base island of the NPN transistor, which is contacted by A_{IR} (see Fig. 2.6). The diode formed by the base and the added N⁺ region was used to reduce contributions of deeper penetrating green, red, and infrared (IR) light to the signal current. The anode current is used as the UV signal current and the photocurrent from longer wavelengths flowing to the cathode and to the A_{IR} anode is not used by the UV sensor system.

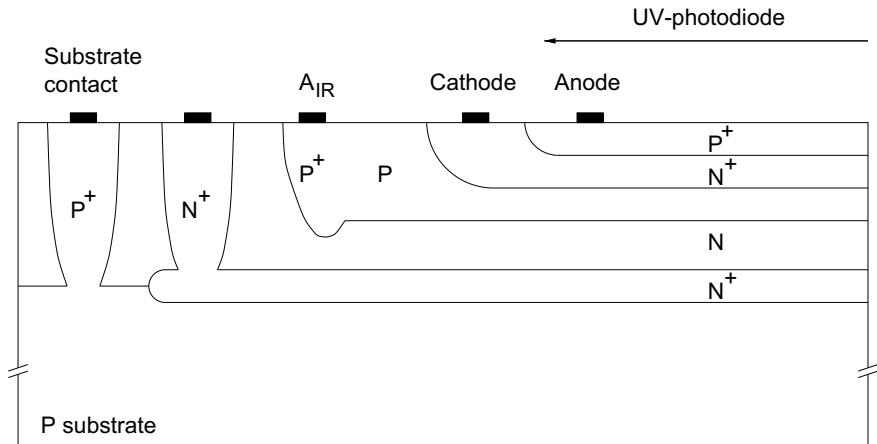


Fig. 2.6 Cross section of a bipolar-integrated UV sensitive photodiode [20]

The photocurrent of this UV detector ranged from 20 pA to 1 nA in the flame detection application. The UV-OEIC was mounted in a TO5 package with a lens focusing the UV light onto the UV sensitive photodiode with an octagonal area of 1 mm². A glass filter was used in addition to perform optical bandpass filtering. The electronic circuit of this UV sensor system will be described in Sect. 6.4.1.

PIN Photodiode

For the wavelengths 780 and 850 nm, a thickness of at least 10 µm is necessary for the so-called intrinsic layer of a PIN photodiode, due to the low optical absorption coefficient of silicon for wavelengths larger than about 700 nm. Such a large I-layer thickness requires the reduction of the epitaxial layer concentration below about 10¹⁴ cm⁻³ for a voltage of 3 V across the PIN photodiode in order to obtain a spreading of the electric field (drift region) over the whole I-zone [23]. There is, however, the so-called Kirk effect [24] or base push-out effect, which requires a large concentration for the N⁻ collector of the order of 10¹⁶ cm⁻³ for high-speed bipolar transistors with transit frequencies in the 10 GHz range or above. According to the Kirk effect, the start and the end of the base-collector space-charge region move closer to the N⁺ collector and thereby increase the width of the base drastically, when the concentration of the electrons crossing the base becomes comparable to the doping concentration N_D of the N⁻ collector. The Kirk effect is a high-injection effect, which was investigated intensively in [25–31]. We will not discuss the details. In short, the Kirk effect becomes active when the collector current density exceeds the critical value j_{critical} [32]:

$$j_{\text{critical}} = q N_D v_s. \quad (2.2)$$

To avoid the Kirk effect, the doping level in the N⁻ collector should be larger than 10¹⁶ cm⁻³. A reduction of the doping concentration N_D in the epitaxial layer

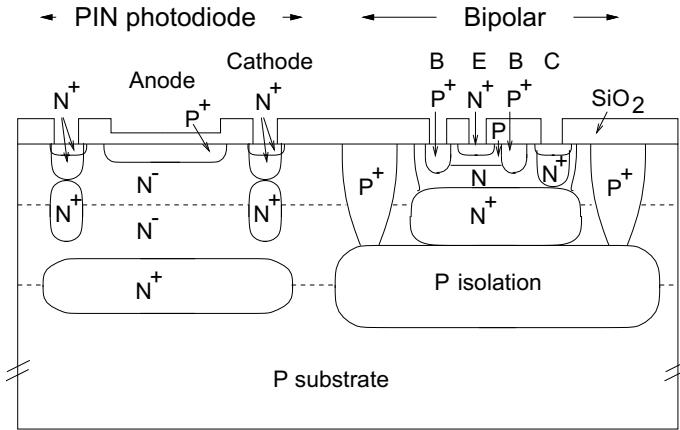


Fig. 2.7 Cross section of a PIN bipolar OEIC [11]

to below 10^{14} cm^{-3} , as would be necessary for the integration of PIN photodiodes, therefore, causes a dramatic decrease of the critical collector current density j_{critical} . In turn, the current gain and the transit frequency of the NPN transistor would drop strongly for $N_D \leq 10^{14} \text{ cm}^{-3}$.

In order to combine both of the above mentioned requirements — thick, low-doped I-layer and thin, higher doped N collector — process modifications were suggested in [11].

Figure 2.7 shows the cross section of the OEIC proposed in [11]. The PIN cathode and a P isolation were implanted into the substrate. A three-step epitaxial growth (first $2 \mu\text{m}$ as a buffer layer in order to avoid autodoping during the epitaxial process, then a $9 \mu\text{m}$ I-layer, and finally a $4 \mu\text{m}$ I-layer after the buried collector implant) was performed in order to supply the thick N-type ‘intrinsic’ layer with a reduced doping level ($< 3 \times 10^{13} \text{ cm}^{-3}$) and a thin collector [11]. Assuming that the N^+ -buried collector and the N^+ -contact implant can be used for the N^+ -cathode contact diffusions, that the P^+ -isolation implant (compare Figs. 2.1 and 2.2) of the standard process can be used for the P isolation contact, and that the base contact implant is used for the PIN anode, the process complexity is increased by three additional lithography steps compared to the original bipolar process (without steps for antireflection coating): (1) for the N^+ -buried PIN cathode; (2) for the P isolation in order to isolate the buried collectors from the N^- ‘intrinsic’ region and to restrict the cathode potential to the photodiode area; and (3) for the N collector implant in order to provide the doping level of about 10^{16} cm^{-3} . Here, the bias voltage of the photodiode is not limited by the circuit operating voltage U_{CC} or by the breakdown voltage BV_{CEO} of the NPN transistors. Larger voltages, therefore, enable high-speed operation of the PIN photodiode. This possibility, however, was not exploited in [11].

A -3 dB bandwidth of 300 MHz for $\lambda = 780 \text{ nm}$ was reported for the PIN photodiode with an area of 0.16 mm^2 at a bias of 3 V . The rise and fall times of the

photocurrent were 1.6 ns for these wavelength and bias values. Bandwidth values for higher bias values, unfortunately were not reported in [11]. The responsivity of the PIN photodiode was 0.35 A/W ($\eta = 57\%$) for $\lambda = 780\text{ nm}$. This responsivity seems to be somewhat low, although an antireflection coating is indicated in Fig. 2.7.

The potential of high-speed operation of this photodiode was demonstrated in [33]. Due to the N-buried layer and the deep N-plugs, this photodiode is isolated from the P-type substrate. The breakdown voltage of the buried cathode towards the substrate is much higher than the circuit supply voltage. Therefore, the cathode potential can be set to e.g. 17 V [33], which speeds up the photodiode considerably. A bandwidth of larger than 1.35 GHz for 660 nm was verified experimentally with a photodiode bias of 12 V for this type of vertical pin photodiode. For 850 nm, the bandwidth of the photodiode was larger than 1.05 GHz with a 12 V photodiode bias. The responsivity values of the photodiode were 0.36 A/W at 660 nm and 0.26 A/W at 850 nm.

Such a pin photodiode was integrated in a BiCMOS process. In Sect. 2.3.2 the properties of the BiCMOS-integrated pin photodiode are described.

2.2 CMOS-Integrated Photodetectors

The CMOS technology is the economically most important technology for the fabrication of microelectronic circuits. Early processes were one-well processes. Modern processes are twin-well processes. We will briefly discuss one-well processes first and then twin-well processes before a large variety of CMOS-integrated photodetectors will be described.

2.2.1 One-Well CMOS Processes

In [34] an N-well process with a minimum feature size of $1.2\text{ }\mu\text{m}$ is described, which uses epitaxial silicon wafers. The P-type substrate has a doping concentration of $2 \times 10^{18}\text{ cm}^{-3}$. On this substrate, a $12\text{ }\mu\text{m}$ thick epitaxial P⁻ layer with a doping concentration of $2 \times 10^{15}\text{ cm}^{-3}$ is deposited.

The N-channel MOSFET obtains only an anti-punchthrough implant instead of a deep P well (Fig. 2.8). The immunity against latch-up, therefore, is not very good. In order to improve the latch-up immunity of CMOS circuits and to optimize the N- and P-channel transistors independently, twin-well processes were developed.

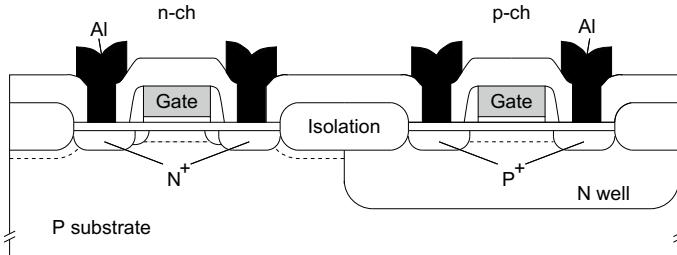


Fig. 2.8 Schematic cross section of a CMOS chip in an N-well technology

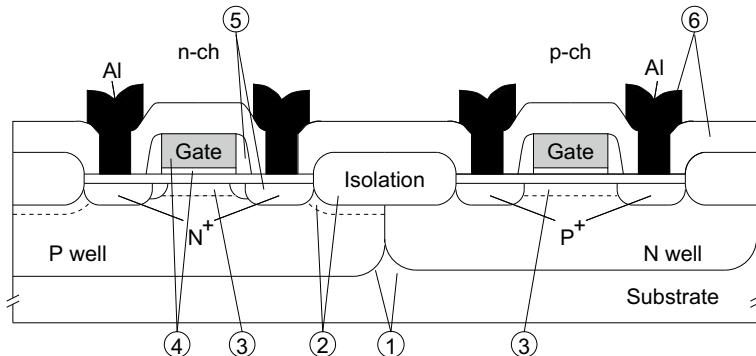


Fig. 2.9 Schematic cross section of a CMOS chip. The common CMOS process can be divided roughly into six main steps [35]

2.2.2 Twin-Well CMOS Processes

A typical submicrometer CMOS process will be described in the following. It uses twin wells [36], LOCOS (LOCal Oxidation of Silicon) isolation [5], an N⁺ polysilicon gate, and lightly doped drain (LDD) N-channel MOSFETs. As illustrated in the final device cross section (Fig. 2.9), a CMOS process consists of six main sections [35] plus passivation:

- (1) Formation of the wells by deep N- and P-type diffusions, which allow the independent tailoring of the doping profiles in each well.
- (2) LOCOS field isolation and the formation of channel-stopper regions, which isolate neighboring devices from each other electrically.
- (3) Ion implantation for the formation of surface- and buried-channel regions for N- and P-MOSFETs, respectively, in order to adjust the threshold voltages.
- (4) Gate oxidation and deposition of the N⁺ polysilicon layer with subsequent gate definition.

(5) Source/drain junction formation by ion implantation including sidewall spacers for LDD formation.

(6) Deposition of oxide, contact hole opening, and metallization.

(7) Passivation.

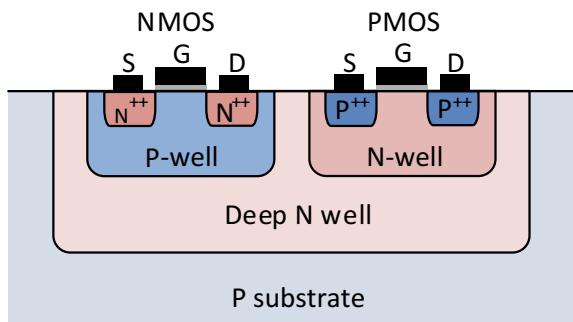
The process flow will be treated in more detail in Sect. 2.2.6. Here several other examples of modern twin-well processes will be mentioned. A $0.6\text{ }\mu\text{m}$ twin-well CMOS process of AT&T uses a $7\text{ }\mu\text{m}$ thick epitaxial layer [37]. The supply voltage is 3.3 V. The wells are drive in to a depth of about $1.8\text{ }\mu\text{m}$. Further examples of twin-well processes were reported in [38, 39]. The first of the two processes is a $0.5\text{ }\mu\text{m}$ process with a specified supply voltage of 3.3 V. The second process is a $0.25\text{ }\mu\text{m}$ process with a specified supply voltage of 2.5 V.

2.2.3 Triple-Well CMOS Processes

If in addition to the N-well and the P-well a deep N-well is processed, the process is called triple-well CMOS. Figure 2.10 shows the cross section of such a process. The deep N-well can be used to isolate the P-well of the NMOS transistor from the P-type substrate. Coupling of substrate noise via the back-gate effect into the NMOS transistor can be avoided by putting the P-well of the NMOS transistor inside a deep N-well [40].

Another motivation for a triple-well CMOS process is the immunity against latch-up [41]. Furthermore, an extremely good hardness against single-event transients was achieved without silicon on insulator (SOI). Later in this book, it will be demonstrated that triple-well (Bi)CMOS processes are very advantageous also for speed enhancement and responsivity enhancement of integrated PN photodiodes, PIN photodiodes, and PIN avalanche photodiodes. Putting the N-well inside a deep N-well increases the breakdown voltage towards P substrate, which allows very negative substrate bias to increase the bandwidth of photodiodes for which the substrate is used as anode.

Fig. 2.10 Schematic cross section of a triple-well CMOS chip



2.2.4 Integrated Detectors in Standard CMOS Processes

PN Photodiodes

The simplest way to build CMOS OEICs is to use the PN junctions available in CMOS processes: source/drain-substrate, source/drain-well, and well-substrate diodes. These PN photodiodes, however, possess regions which are free from electric fields. In these regions, the slow diffusion of photogenerated carriers determines the transient behavior of such PN photodiodes. Published PN CMOS OEICs are characterized by bandwidths of less than 15 MHz [42–44]. Another example is described in [45], where the OEIC was optimized for a dynamic range of six decades in illumination.

The source/drain-substrate and source/drain-well photodiodes are more appropriate for the detection of wavelengths shorter than about 600 nm, whereas the well-substrate photodiode is more appropriate for long wavelengths like 780 or 850 nm. Figure 2.11, for instance, shows an N⁺/P-substrate photodiode.

In addition to carrier diffusion, the series resistance of the photodiodes due to lateral anode contacts at the silicon surface together with the relatively large junction capacitance of the photodiode may limit the dynamical PN photodiode behavior. In an N-well process, the anode of the N⁺/P-substrate photodiode has to be at V_{SS} potential, which may be a restriction for circuit design.

A lateral N⁺/P-substrate/P⁺ photodiode was used as an optical detector, into which light was coupled by an integrated waveguide [42]. This detector was realized in a 0.8 μm N-well CMOS process. A maximum bandwidth of 10 MHz was achieved with a transimpedance amplifier for a photocurrent of 1 μA with $\lambda = 675$ nm. The speed of the detector was limited by carrier diffusion due to photogeneration outside the diode [43].

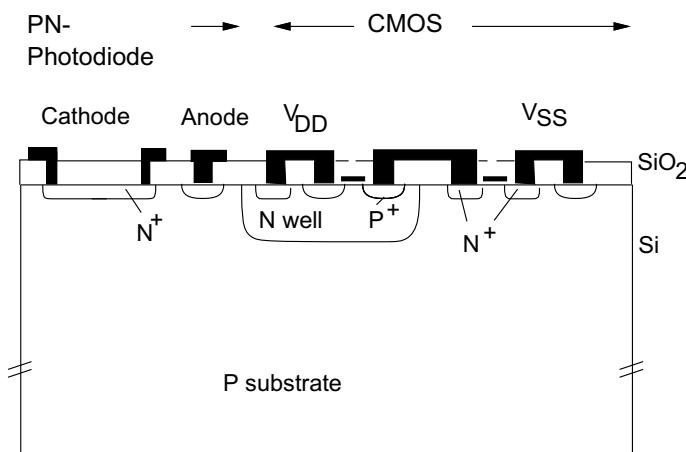
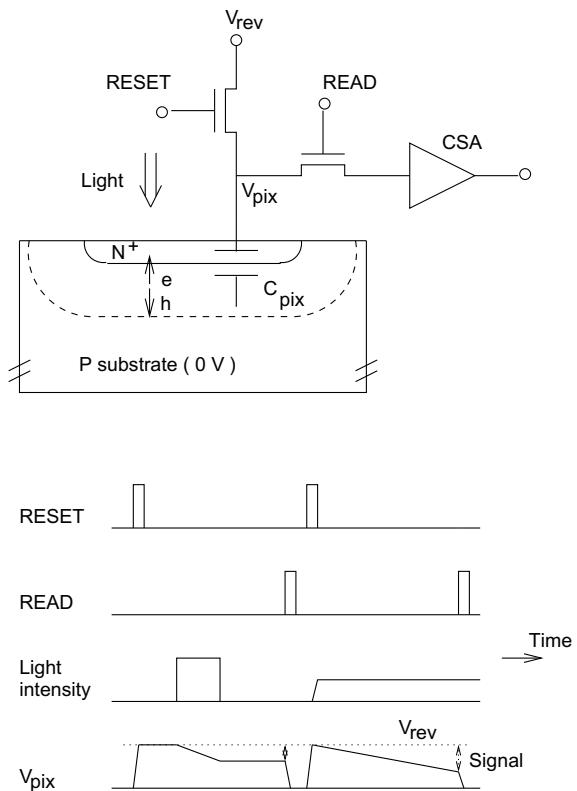


Fig. 2.11 Schematic cross section of a PN photodiode integrated in a one-well CMOS chip

Fig. 2.12 Operation of a PN photodiode in a discharging storage mode



The N-well/P-substrate diode in a $2\mu\text{m}$ N-well CMOS process was used as a photodiode in [44]. A bandwidth of 1.6 MHz with a wavelength $\lambda = 780\text{ nm}$ was reported for an unoptimized system. The leakage current density of the photodiode was 15 pA/mm^2 at 5 V . The responsivity for $\lambda = 780\text{ nm}$ was 0.5 A/W ($\eta = 70\%$). The light was coupled into the photodiode via an integrated waveguide. Therefore, the light transmission of the isolation oxide was not strongly influenced by destructive interference.

In addition to the continuous observation of the photocurrent of a PN photodiode, PN photodiodes can be operated in a storage mode. The capacitance of the photodiode can be used to integrate and store a photogenerated charge and to read it after certain periods (Fig. 2.12).

For such a purpose, the capacitance of the photodiode is initially set to the reverse voltage V_{rev} , when the reset-MOS switch is ON. Then the reset-MOS switch is opened to the OFF state and the photodiode floats for the light integration period. During this time, the capacitance is being discharged with a rate which depends on the light intensity. The remaining charge on the capacitance Q_{pix} is switched by the read-MOSFET to the input of a charge sensitive amplifier (CSA) at the end of the integration period. The smaller this charge being read, the more intensive was

the incident light. This discharging method is advantageous compared to a charging method, because the electric field due to V_{rev} in the photodiode helps to collect the photogenerated charge effectively. With a charging method, the space-charge region would be thinner and charge collection would not be as effective. N⁺/P-substrate photodiodes in a 512 one-dimensional array were, for instance, integrated in a 1.2 μm analog CMOS technology and used in the charge storage mode [46].

Double Photodiodes

The double photodiode shown in Fig. 2.13 does not need any process modifications. It consists of the N⁺/P-well diode and of the P-well/N⁻N⁺-substrate diode. The load resistor has to be connected to the common P-well anode in order to collect the photocurrents of both photodiodes.

Figure 2.14 shows the frequency response of a double photodiode (DPD) on a N⁻N⁺ substrate, which was fabricated with a 1 μm CMOS process. The doping concentration of the N epitaxial layer was approximately $1 \times 10^{15} \text{ cm}^{-3}$. The integrated 500Ω resistor was connected to the P-well anode, which was biased at +2 V. The N⁺ cathode and the N-substrate cathode were at +5 V. The reverse bias of the double photodiode accordingly was 3 V. The size of the photodiode was approximately

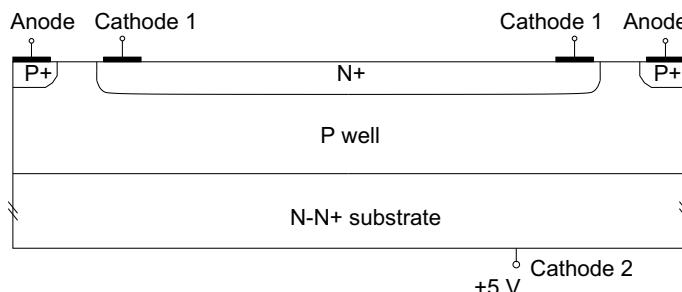
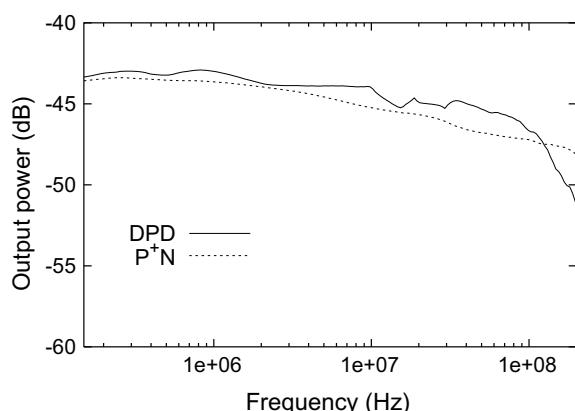


Fig. 2.13 Schematic cross section of a double photodiode

Fig. 2.14 Comparison of the frequency responses of a double photodiode (DPD) and of a P⁺N photodiode fabricated in a 1 μm CMOS process and measured with integrated 500Ω gate polysilicon resistors and a picoprobe for a wavelength of 638 nm



$50 \times 50 \mu\text{m}^2$. A -3 dB frequency of approximately 90 MHz was measured for this double photodiode with a picoprobe.

In Fig. 2.14 the frequency response of a P⁺N photodiode with the same size and fabricated on the same wafer as the double photodiode is shown for comparison. The -3 dB frequency of the P⁺N photodiode is only 32 MHz and the photocurrent already begins to decrease at a frequency of 2 MHz due to slow diffusion of photogenerated carriers from a depth of more than approximately 2 μm . In the double photodiode two space-charge regions are present. The first space-charge region is formed at the N⁺/P-well junction and the second space-charge region is present at the P-well/N-substrate junction at a depth of approximately 4 μm . Furthermore, there is an electric field between these two space-charge regions due to the doping gradient of the N well [47]. The field-free region in the substrate below the P-well/N-substrate junction where a small portion of carriers is photogenerated with red light, therefore, is thinner in the double photodiode and carrier diffusion is much less important resulting in a much larger -3 dB bandwidth.

The rise and fall times of 2.34 and 2.48 ns, respectively, for the double photodiode were determined with a picoprobe and a digital oscilloscope (Fig. 2.15). The frequency and transient responses of the double photodiode were limited by the RC time constant of its large capacitance of more than 1 pF and the 500 Ω resistor. The capacitance of the picoprobe of 0.1 pF is rather small and can be neglected.

In addition to the application of the double photodiode as a fast photodetector, it is possible to use the DPD as a color detector [48]. The diode with the shallow junction preferentially collects carriers created by shorter wavelength light, while the diode

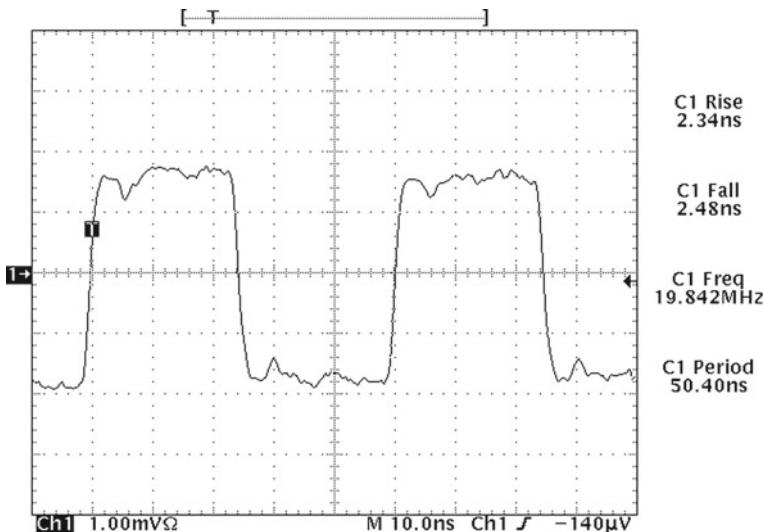


Fig. 2.15 Transient response of a CMOS-integrated double photodiode measured with an integrated 500 Ω polysilicon resistor and a picoprobe for $\lambda = 638 \text{ nm}$

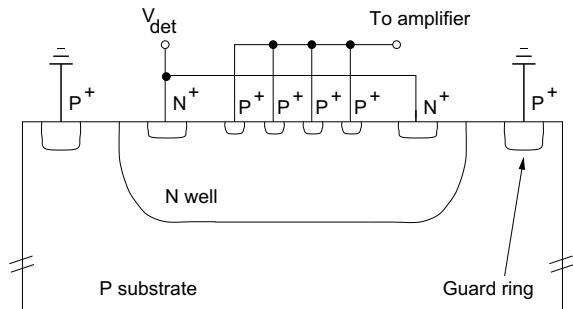
with the deeper junction collects carriers created by longer wavelength light. The shorter wavelengths predominantly generate a photocurrent in the source/drain-well diode, while the longer wavelengths predominantly generate a photocurrent in the well-substrate diode. The quantum efficiency of the source/drain-well diode peaked at about 530 nm and the quantum efficiency of the well-substrate diode showed a maximum at about 710 nm [48]. The ratio of the photocurrents of the source/drain-well diode and the well-substrate diode versus wavelength was a monotonously decreasing function in the range from 450 to 900 nm. Measuring the photocurrents of the two diodes, computing their ratio, and looking up the wavelength for this ratio value from a list stored in an EEPROM for instance allows us, therefore, to determine the wavelength in monochromatic or narrow bandwidth applications.

Interrupted-P-Finger Photodiode

Another example of a high-speed photodiode in a 0.35 μm standard CMOS technology [49] will be given in the following. The photodiode uses the P⁺ source/drain implant of the CMOS process for the anode and the N well for the cathode (Fig. 2.16).

The photoreceiver (see Fig. 6.122) uses the anode current for amplification of the optical signal (see Fig. 2.16). The slow diffusion of carriers generated by light with a wavelength of 850 nm in the P substrate, therefore, does not contribute to the photocurrent. This slow current is collected by the N well and shorted to the power supply V_{det} . To enhance the speed of the photodiode further, an interdigitated network of P⁺ fingers is employed instead of a continuous P⁺ region for maximizing the depletion regions available for carrier collection, particularly near the surface of the device. These P⁺ fingers are connected outside the light sensitive area and form the anode of the photodiode. The N well had a size of $16.5 \times 16.5 \mu\text{m}^2$. With a detector bias of 10 V, a bit rate of 1 GBit/s was reported with a bit error rate of less than 10^{-9} . The responsivity of the photodiode with the reported values of 0.01–0.04 A/W was very low due to the shallow P⁺/N-well junction. It should be mentioned that this wide range of 0.01–0.04 A/W probably is due to optical interference in the CMOS isolation and passivation stack.

Fig. 2.16 Schematic cross section of an N-well/interrupted-P-finger photodiode [49]



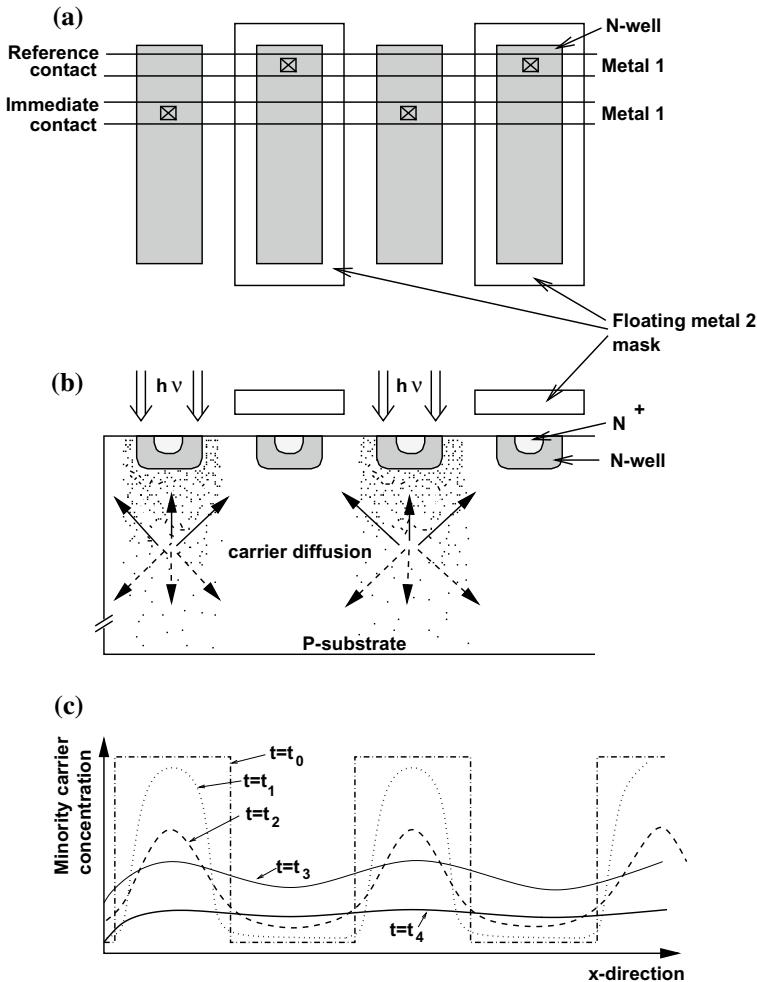


Fig. 2.17 Layout **a**, cross section **b**, and distribution of photogenerated carriers **c** of SML detector [50, 51]

2.2.5 Spatially-Modulated-Light Detector

A very sophisticated photodetector in standard CMOS technology, the spatially-modulated-light (SML) detector (Fig. 2.17), was proposed to avoid the effect of slow carrier diffusion [50].

The basic idea of this light detector is to use a reference diode (deferred detector), which measures the diffusion current caused from carriers in the substrate, and to subtract this diffusion current from the photocurrent in the immediate detector. To achieve a high speed, the immediate and deferred detectors have to be interdigitated

as shown in Fig. 2.17. A portion of the diffusing minority charge carriers (electrons) photogenerated below the immediate detectors reaches the N-well of the reference (deferred) detector and causes the reference diffusion current. The deferred detectors are covered by metal, because the incident light has to be prevented from penetrating into the deferred detector. Otherwise, the diffusion current coming from the immediate detectors could not be determined.

Figure 2.17c shows that immediately after the light incidence the photogenerated carriers are spatially modulated. After an increasing time period more and more carriers diffuse from the immediate detectors to the deferred detectors until they are almost equally distributed after the time t_3 or even better after t_4 . With this SML detector the diffusion tail present for simple PN photodiodes can be suppressed to a certain degree. The price which has to be paid, however, is a reduced responsivity due to half of the detector area being covered by metal and because carriers photogenerated below the N-well/p-substrate space-charge region do not contribute to the effective photocurrent. Responsivities of 0.1 A/W ($\eta = 15\%$) for 860-nm light and 0.132 A/W for 635-nm light were measured for an implementation in a $0.6 \mu\text{m}$ CMOS standard technology [50]. A -3 dB bit rate of 500 Mb/s was mentioned for this technology. In a $0.25 \mu\text{m}$ CMOS technology, an optical receiver with a bit rate of 700 Mb/s was realized (see Sect. 6.4.13).

2.2.6 PIN Photodiode

Lateral PIN Photodiode

A lateral PIN photodiode was fabricated together with NMOS transistors in a $1.0 \mu\text{m}$ technology using a nominally undoped substrate, which was actually P-type with $N_A = 6 \times 10^{12} \text{ cm}^{-3}$ [52, 53]. The schematic cross section of the NMOS OEIC is shown in Fig. 2.18. The PIN photodiode was fabricated directly on the high-resistivity substrate. It was stated that the thickness of the depletion layer of the PIN photodiode was approximately equal to the penetration depth of 850 nm light in silicon. The lateral PIN photodiode had a circular form with the cathode in the center surrounded by the anode. The gap between anode and cathode had a width of $10 \mu\text{m}$. A dark current of 20 nA at 5 V , a breakdown voltage in excess of 60 V , and a capacitance of 40 fF at 5 V were reported. The external quantum efficiency of the photodiode at 870 nm was 67% without an antireflection coating.

The -3 dB bandwidth of the photodiode was determined by measuring the spectral content of the photodiode response to an optical input approximating a comb of “delta” functions in the time domain. Pulses with a duration of 200 fs and a separation of 13.2 ns from a mode-locked Ti-sapphire 850 nm laser were used as the optical input for the photodiode for this measurement. The output spectrum of the photocurrent was a comb function in the frequency domain with a peak separation of 75 MHz ($1/(13.2 \text{ ns})$) and a pulse height determined by the frequency response of the photodiode. A -3 dB bandwidth of the photodiode equal to approximately 1.3 GHz

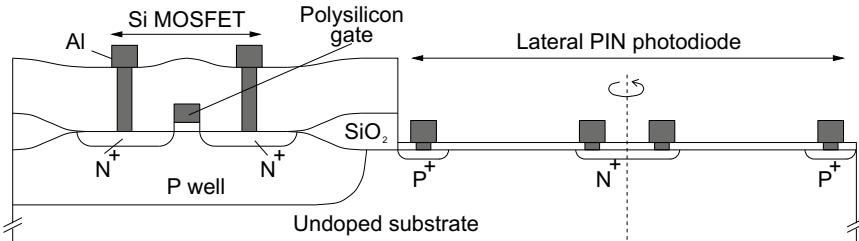


Fig. 2.18 Schematic cross section of an NMOS fiber receiver OEIC with a circular lateral PIN photodiode [52]

was indicated by this measurement technique at a photodiode bias of 5 V. This large value, however, seems questionable for central light incidence due to the low electric field beneath the wide N⁺ cathode.

Vertical PIN Photodiode

Our goal is the integration of a vertical PIN photodiode in a twin-well CMOS process. We will use Fig. 2.19 to illustrate the CMOS process sequence and the simplicity of PIN photodiode integration by means of the ‘third’ column on the right of this figure.

The starting material is usually a (100)-oriented silicon substrate — P-type in this case — with an epitaxial layer having a doping concentration of $\approx 10^{15} \text{ cm}^{-3}$. Steps (a) and (b) show the self-aligned twin-well formation with only one lithographic mask step.

(a) The structured photoresist and nitride layer on a thin oxide layer are used for doping with phosphorus by ion implantation (I²) into the N-well area selectively.

(b) After removing the photoresist, the wafers are selectively oxidized over the N-well region (LOCOS). The nitride layer is then etched off and boron is implanted to form the P well, whereby the LOCOS oxide prevents the boron from being implanted into the N-well area. The two wells are then driven in by high-temperature annealing to a depth of several micrometers and all oxides are etched off. The final impurity density of the wells at the silicon surface should be higher by at least one order of magnitude than that in the epitaxial layer to ensure independence of the device parameters of tolerances in the doping level of the epitaxial layer. The final impurity density of the wells at the silicon surface is typically of the order of 10^{16} cm^{-3} .

There are, however, also processes which do not use self-aligned twin-wells. These processes, needing two masks for the twin-well formation, are more appropriate for PIN photodiode integration, because no additional mask, i.e. no process modification is required in order to block out one of the two well implantations in the photodiode area. Although both types of processes end up with two masks for twin-well formation and PIN photodiode integration, for the process using self-aligned twin-wells the additional mask for PIN photodiode integration is a process modification. We will assume a process not using self-aligned twin-wells and start with step (c) for PIN photodiode integration.

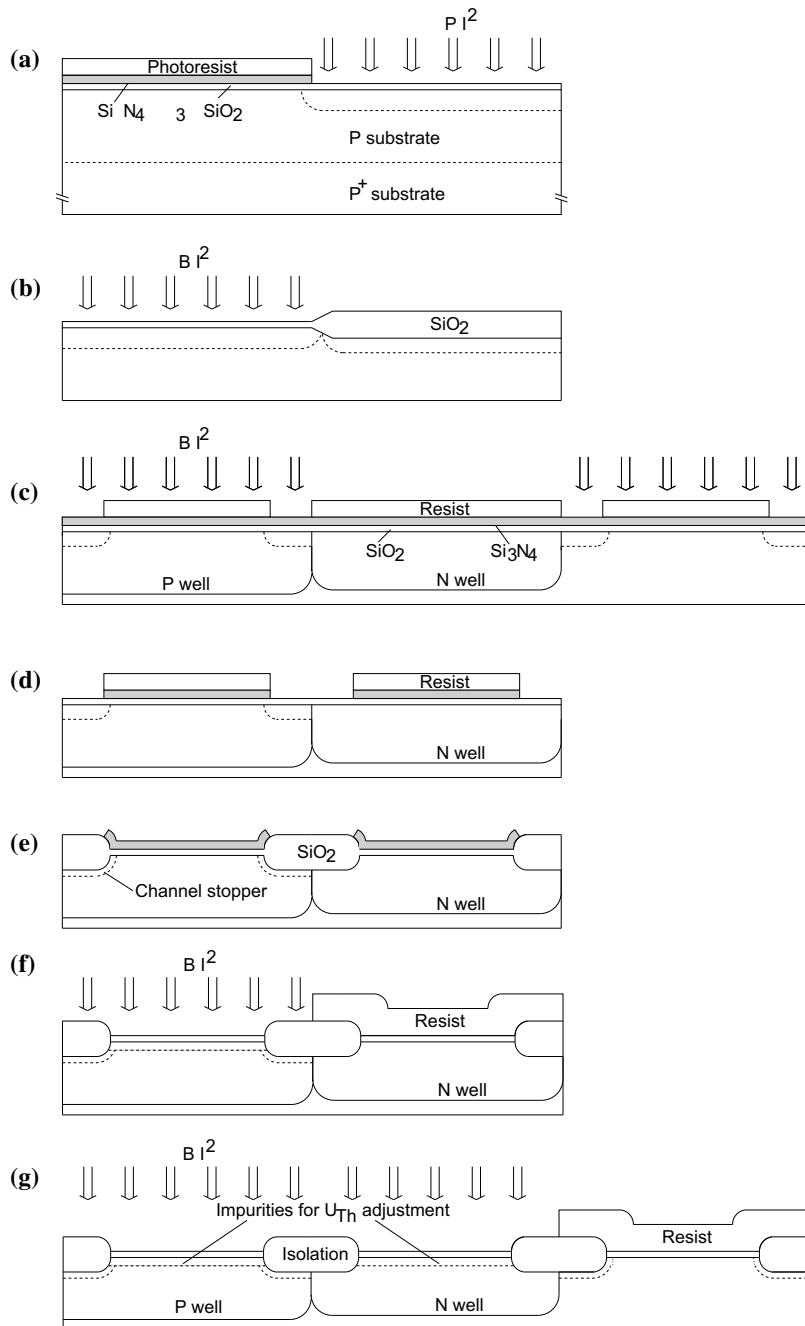
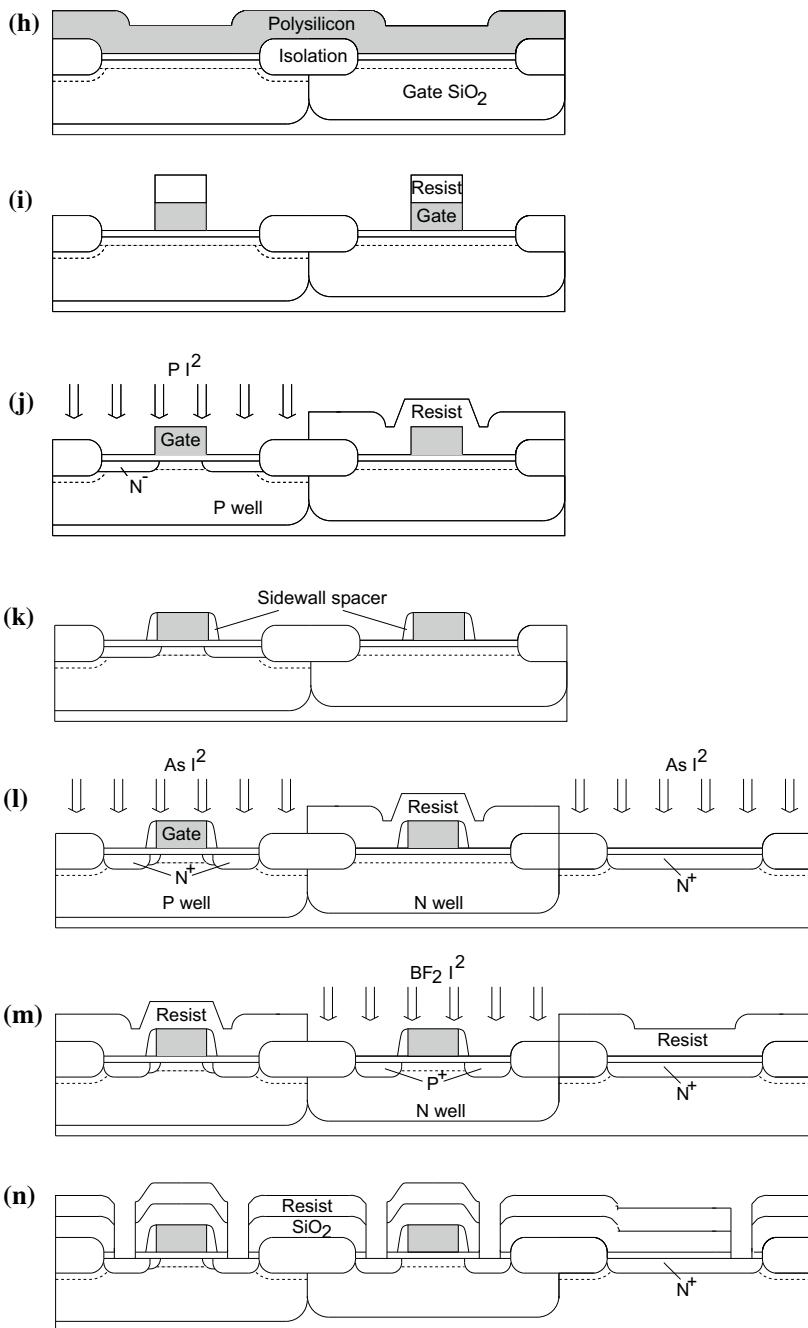


Fig. 2.19 Process flow of a modern CMOS process [35] extended by the right column for PIN photodiode integration: **a, b** well formation, **c–e** isolation formation with channel stoppers **f, g** threshold voltage adjustment, **h, i** gate-oxide and gate-electrode formation, **j** LDD implantation, **k–m** LDD sidewall and source/drain formation, **n** contact-hole formation

**Fig. 2.19** (continued)

The steps (c–e) show how LOCOS field isolation with an underlying channel-stopper region is formed.

(c) A nitride layer is deposited on a thin thermal oxide, called *pad oxide*. It is necessary for less mechanical stress concentrated at the LOCOS edge [54]. A photoresist mask is used to implant boron selectively through the oxide/nitride layer into the silicon, where the channel-stopper region is desired. The P-type channel-stopper is needed to increase the impurity density beneath the field isolation in P-well regions. Without this channel stopper, a parasitic N-channel MOSFET between two neighboring N-channel MOSFETs might be normally ON due to a large amount of positive fixed charge induced by subsequent LOCOS oxidation.

(d) The nitride layer is defined by dry etching and the pad oxide is exposed over the isolation region.

(e) The resist is removed and a thick field oxide is thermally grown to a thickness of several hundred nanometers over the isolation region. The nitride protects the remaining *active region* from being oxidized. The channel-stopper implant is driven in during this LOCOS oxidation. The nitride and thin oxide are then removed.

(f) The threshold implantation for the N-MOSFET can be done in two steps making two different threshold voltages available. The first threshold implantation is shown in Fig. 2.19f. A thin oxide is grown prior to the implantation to prevent ion channeling. The doping of the surface channel for the N-MOSFET is performed by boron or BF_2 implantation.

(g) The second threshold implantation for the N-MOSFET is shown in Fig. 2.19g. This boron or BF_2 implantation simultaneously results in the formation of a buried-channel P-MOSFET. The buried-channel P-MOSFET has the advantage of a lower $1/f$ noise compared to a surface-channel P-MOSFET. The second threshold implantation is carried out without a mask into all active regions. The photodiode region, therefore, has to be protected from being implanted by a resist mask. Let us call this mask a photodiode protection mask. The resist and all thin oxides are then removed to obtain the cross-sectional view before gate oxidation.

(h) The gate oxide is grown thermally in order to obtain a high oxide quality. Subsequently polysilicon for the gate electrode is deposited. The intrinsic polysilicon is then heavily doped with phosphorus in a gas ambient of POCl_3 at a temperature between 850 and 950 °C. In a polycide gate process, a silicide layer is then deposited on top of the polysilicon.

(i) The N^+ -polysilicon layer is defined by lithography and dry etching. The resist is removed and the gate electrode is exposed to the so-called gate reoxidation or sidewall oxidation to prevent gate-oxide integrity near the gate edges from degradation [55].

The steps (j–m) show how the N^- regions for the LDD N-MOSFET, sidewall spacers, and N^+ as well as P^+ source/drain regions are formed:

(j) Phosphorus — or more recently arsenic — is implanted as the N^- LDD dopant. The implantation energy is low so that the phosphorus or arsenic implantation is masked by the thick field oxide, the gate electrode, and the photoresist mask above the opposite type of well.

(k) After removing the resist, oxide is deposited everywhere on the wafer and anisotropically etched to form sidewall spacers.

(l) Arsenic is implanted for N^+ source/drain formation of the N-MOSFET. A resist mask protects the P-MOSFETs from being implanted. This implant is used for the cathode formation of the PIN photodiode.

(m) BF_2 is implanted selectively into the P-MOSFET source/drain regions using another resist mask.

(n) Two oxide layers are then deposited, from which the first is undoped oxide (TEOS) and the second is boron and/or phosphorus doped for improving the glass flow property, which is needed for planarization. Contact holes are then defined by lithography and opened by dry etching.

Finally, the first aluminum layer for contact and interconnect formation is deposited and defined by lithography and dry etching. Then intermetal dielectric layers and further metal depositions may follow. In industrial practice, passivating oxide, nitride, or oxynitride layers are added by plasma-assisted deposition to protect the chip from impurities and humidity coming from the surroundings. Finally, bondpad areas have to be defined and opened.

Summarizing, we can state that only one additional mask is necessary for PIN photodiode integration on P^-P^+ -substrate in order to block out an originally unmasked P-type threshold implantation, when the CMOS process does not use self-adjusting wells. Without this additional mask an N^+/P junction at the surface would result instead of the desired N^+/P^- junction. There would be a high electric field at the N^+/P junction and this would lead to a strongly reduced electric field in the ‘intrinsic’ P^- -zone of the PIN photodiode and to longer rise and fall times.

On an N^-/N^+ -substrate, the P-type PIN anode would be at the surface and the unmasked P-threshold implant increases the P^+/N^- junction depth by a small amount. In this case the electric field in the ‘intrinsic’ zone of the PIN photodiode is not reduced. The quantum efficiency for blue light may be reduced due to the larger junction depth. If this can be tolerated, no additional mask is required for PIN photodiode integration on an N^-/N^+ -substrate.

As mentioned above, the doping concentration of the epitaxial layer is usually approximately 10^{15} cm^{-3} . Considering circuits with integrated photodiodes, a reasonable reverse bias of the photodiodes is approximately 3 V, when a single-supply voltage of 5 V is used. We know from Fig. 1.4 that the width of the space-charge region for a reverse bias of 3 V is only approximately 2 μm for a doping concentration of 10^{15} cm^{-3} . Due to the larger penetration depth of red and infrared light, slow diffusion of photogenerated carriers results for the epitaxial layer doping level of 10^{15} cm^{-3} . The doping level of the epitaxial layer has to be reduced in order to avoid this slow carrier diffusion [56]. It should be mentioned that this reduction of the doping concentration in the epitaxial layer is not a process modification. The CMOS manufacturer only has to buy wafers with a lower doping concentration in the epitaxial layer.

For the optical wavelengths of 780 and 850 nm being used in optical data transmission, the thickness of the epitaxial layer of a standard twin-well CMOS process of 7 μm [37], for instance, is too small due to the small absorption coefficients of Si for these wavelengths. In addition to the reduction of the doping concentration in the epitaxial layer, therefore, its layer thickness should be increased.

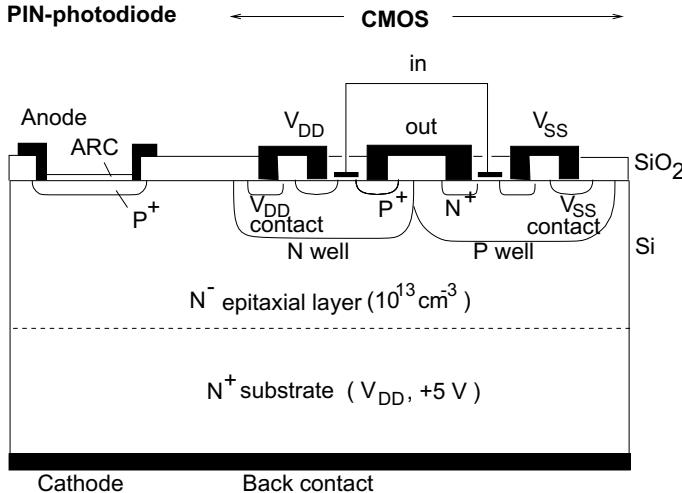


Fig. 2.20 Cross section of a N^-N^+ PIN-CMOS-OEIC [57]

There are several aspects which must be investigated when the epitaxial layer of a twin-well CMOS process is modified: (i) Latch-up immunity may be reduced. (ii) Reach-through (punch-through) between wells of the same type may occur. (iii) Electrostatic discharge hardness may suffer. Before these aspects are discussed the gain in photodiode performance by the modification of the epitaxial layer, i.e. by the reduction of its doping concentration will be shown in the following.

Results for N-type Substrate

Figure 2.20 shows the structure of a N^-N^+ CMOS-OEIC in the twin-well approach. Here the N^+ substrate serves as the cathode and the P^+ source/drain region as the anode of the integrated PIN photodiode.

PIN-CMOS photodiodes with an area of $2700 \mu\text{m}^2$, with a standard doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$ and with reduced doping concentrations in the epitaxial layer down to $2 \times 10^{13} \text{ cm}^{-3}$, and with an integrated polysilicon resistor of 500Ω , were fabricated in an industrial $1.0 \mu\text{m}$ CMOS process [58]. For the measurements, a laser with $\lambda = 638.3 \text{ nm}$ was modulated with a commercial ECL generator. The light pulses were coupled into the photodiodes on a wafer prober via a single-mode optical fiber. The rise (t_r) and fall (t_f) times of the photocurrent of the photodiodes were measured with a picoprobe (pp), which possesses a -3 dB bandwidth of 3 GHz and an input capacitance of 0.1 pF , and with a 20 GHz digital sampling oscilloscope HP54750/51.

Figure 2.21 contains the waveform of the photocurrent for the photodiode with the standard doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$ in the epitaxial layer. The values $t_r = 5.3 \text{ ns}$ and $t_f = 7.3 \text{ ns}$ were determined from the waveform for the photodiode with the standard doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$ in the epitaxial layer. These

Fig. 2.21 Measured transient response of a CMOS-integrated P⁺N photodiode with a standard epitaxial doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$ for $\lambda = 638 \text{ nm}$ and $|V_{PD}| = 3.0 \text{ V}$. The overshoot is due to direct laser modulation. The 0 and 100% lines for the determination of t_r and t_f are at 3.5 and 55.5 mV

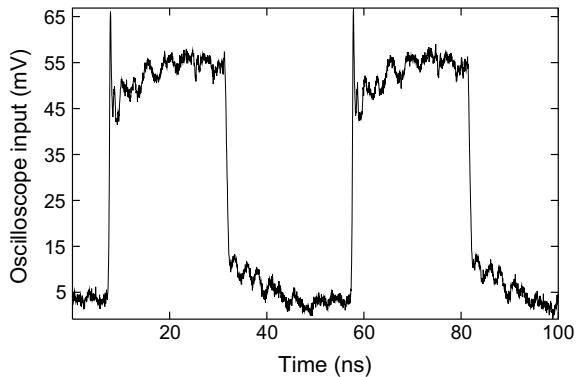
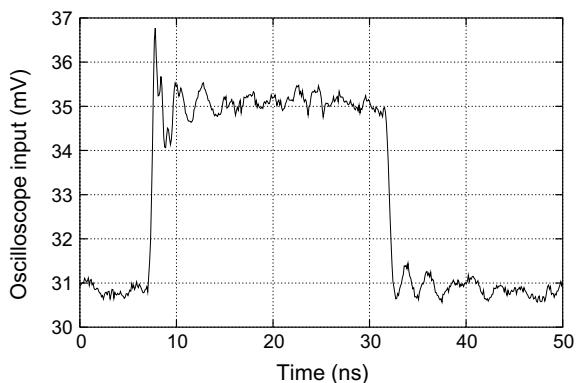


Fig. 2.22 Measured transient response of a CMOS-integrated PIN photodiode with an I-layer doping concentration of $2 \times 10^{13} \text{ cm}^{-3}$ for $\lambda = 638 \text{ nm}$ and $|V_{PD}| = 3.0 \text{ V}$. The overshoot in the signal is due to the direct modulation of the laser [59]



large values are due to the diffusion tail of the photocurrent, which is caused by the slow carrier diffusion in the standard epitaxial layer of the photodiode. Values up to $t_r = 15.5 \text{ ns}$ and $t_f = 17.6 \text{ ns}$ were also measured for the photodiode with the nominal doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$ in the epitaxial layer. The large ranges for t_r and t_f can be explained like this: The diffusion tail of the photocurrent is very sensitive to the actual doping concentration and thickness of the epitaxial layer. The rise and fall times, therefore, vary strongly with the position of the photodiode on a wafer and from wafer to wafer due to variations of doping concentration and epitaxial layer thickness.

For the PIN photodiode with a doping concentration in the epitaxial layer of $2 \times 10^{13} \text{ cm}^{-3}$, the oscilloscope extracted $t_r^{\text{osc,disp}} = 0.37 \text{ ns}$ and $t_f^{\text{osc,disp}} = 0.57 \text{ ns}$ from the waveform shown in Fig. 2.22. The evaluation according $(t_r^{\text{PIN}})^2 = (t_r^{\text{osc,disp}})^2 - (t_r^{\text{laser}})^2 - (t_r^{\text{PP}})^2 - (t_r^{\text{osc}})^2$ with $t_r^{\text{laser}} = 0.30 \text{ ns}$, $t_r^{\text{laser}} = 0.51 \text{ ns}$, $t_r^{\text{PP}} = 0.1 \text{ ns}$ and $t_r^{\text{osc}} \approx 0.02 \text{ ns}$ results in $t_r^{\text{PIN}} = 0.19 \text{ ns}$ and $t_f^{\text{PIN}} = 0.24 \text{ ns}$ [57]. With $f_{3\text{dB}} = 2.4/(\pi(t_r + t_f))$, the -3 dB bandwidth can be estimated to be 1.7 GHz for $|V_{PD}| = 3.0 \text{ V}$. With the conservative estimate $\text{BR} = 1/(1.5(t_r + t_f))$, a bit rate, BR, of 1.5 Gb/s results for $|V_{PD}| = 3.0 \text{ V}$. With an antireflection coating (ARC), the quantum efficiency η could be

Table 2.1 Measured threshold voltages U_{Th} and drain leakage currents I_{D}^{r} for different doping levels in the epitaxial layer

I-Doping (cm^{-3})	$U_{\text{Th}}^{\text{NMOS}}$ (V)	$I_{\text{D}}^{\text{r},\text{NMOS}}$ (pA)	$U_{\text{Th}}^{\text{PMOS}}$ (V)	$I_{\text{D}}^{\text{r},\text{PMOS}}$ (pA)
Standard	0.79	2.19	-0.62	63.1
1×10^{14}	0.79	0.83	-0.60	66.1
5×10^{13}	0.79	0.81	-0.60	66.1
2×10^{13}	0.78	1.02	-0.60	67.6

increased from 49 to 94%. To our knowledge this is the first time that such a high speed and such a high quantum efficiency have been achieved with an integrated silicon photodiode for a reverse voltage of only 3 V, whereby an only slightly modified standard CMOS process has been used.

Transistor Parameters

In contrast to transistors in bipolar OEICs, the electrical performance of the N- and P-channel MOSFETs is not degraded when the epitaxial layer is modified. This statement was verified by measurements (Table 2.1). The threshold voltages of the NMOS and PMOS transistors are practically independent of the doping concentration in the epitaxial layer, because these transistors are placed inside wells which possess a much higher doping level of several times 10^{16} cm^{-3} than the standard epitaxial layer with about $1 \times 10^{15} \text{ cm}^{-3}$ and because the threshold implants produce an even higher doping level ($\approx 10^{17} \text{ cm}^{-3}$) than the wells [60].

The reverse, i.e. the leakage current of the drain to well diodes is also listed in Table 2.1 for the NMOS and PMOS transistors [60]. The leakage current for the NMOS transistor in an epitaxial layer with reduced doping concentrations actually seems to be smaller than for the standard concentration.

These results confirm the superiority of the PIN-CMOS integration [56] compared to the PIN-bipolar integration [11]. In contrast to the PIN-bipolar integration, the electrical transistor parameters of the standard twin-well CMOS process are completely unaffected for the PIN-CMOS integration and can be used for circuit simulations within the design of OEICs.

Latch-up Effect

At places where N and P wells are in contact, there is the danger of latch-up. Figure 2.23 shows P- and N-type regions acting as parasitic bipolar transistors in a CMOS cross section.

The N^+ source-island of the N-channel MOSFET forms the emitter of the parasitic NPN transistor, the P well forms the base, and the epitaxial substrate forms the collector of the parasitic NPN transistor. Analogously, the emitter of the parasitic PNP transistor consists of the P^+ source island, the base consists of the N well, and the collector of the PNP transistor consists of the P well. The collector of one transistor simultaneously forms the base of the other transistor and vice versa. The NPN and PNP transistors, therefore, form a thyristor structure. The thyristor can turn

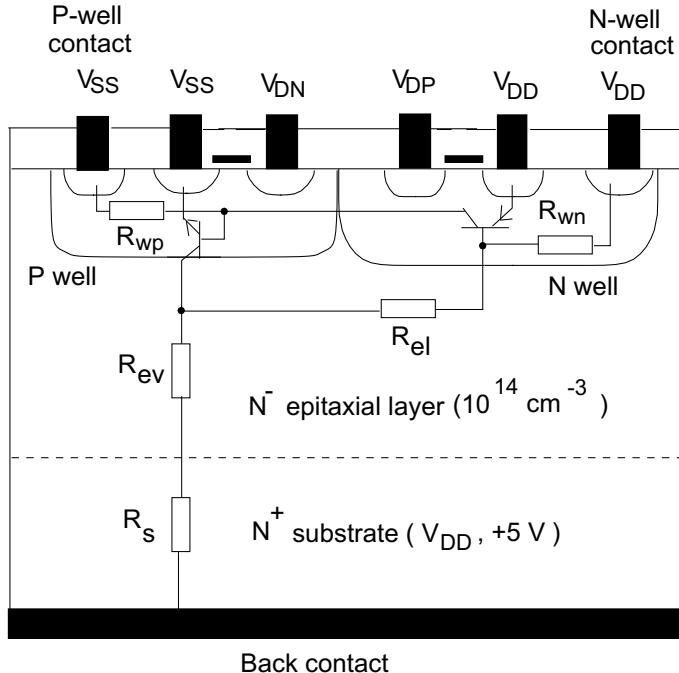


Fig. 2.23 Schematic of the parasitic bipolar transistors being responsible for latch-up in a CMOS circuit [60]

on, for instance, when the base-emitter-potential of one of the transistors exceeds a value of 0.6 V, approximately, due to a lateral current in one of the wells across R_{wp} or R_{wn} as a result of voltage spikes on the well-interconnect lines. The turn-on of the thyristor leads to a shorting of V_{DD} and V_{SS} and the transistors lose their function in the circuit at least until the next power-off and power-on. They may even be destroyed due to large currents resulting in strong heating.

A reduction of the doping concentration in the epitaxial layer for PIN photodiode integration reduces the value of the base Gummel integral of the PNP transistor and increases the PNP current gain accordingly. The value of the NPN transistor's collector series resistance R_{ev} increases when the doping concentration of the epitaxial layer is reduced. These two aspects may lead to a reduced latch-up immunity. The lateral resistor R_{el} (see Fig. 2.23), however, is also increased. This aspect increases the latch-up immunity again, because R_{el} forms a voltage divider together with R_{wn} , which is independent of the doping concentration of the epitaxial layer.

The latch-up immunity can be enhanced by appropriate design measures. When the source of the NMOS transistor is closer to the N well than the drain of the NMOS transistor, the parasitic NPN transistor may partially inject laterally into the N well as a collector instead of injecting only vertically as shown in Fig. 2.23. Therefore, the distance of neighboring N- and P-channel transistors (more accurately between N⁺

and P⁺ islands in wells of different type which are in contact with each other) must not be smaller than a minimum N⁺–P⁺ distance defined in the design rules in order to keep the so-called holding voltage above the V_{DD} voltage value. Using a larger distance increases the latch-up immunity due to a reduction of the bipolar transistor current gain with a wider base. Paying attention to this design rule results in an extinguishing current flow in the thyristor structure after the end of the firing impulse. The minimum N⁺–P⁺ distance depends on the substrate doping concentration. In order to minimize the N⁺–P⁺ distance, epitaxial wafers with highly doped substrates are used. Thus the minimum distance depends on the doping concentration of the epitaxial layer. Chapman et al. [61] from Texas Instruments reported a thickness of the epitaxial layer of 5 μm for a 0.8 μm CMOS technology. In order to keep the holding voltage above a value of 5 V, the N⁺–P⁺ distance had to be larger than 4 μm. For a constant distance of the well contacts, the holding voltage reduced to 1.5 V when the thickness of the epitaxial layer was increased to 7 μm. The holding voltage reduced to approximately 1 V for an epitaxial layer thickness of 9 μm. In order to obtain holding voltage values larger than 5 V for the thicker epitaxial layers, the distance to the well contacts had to be reduced [61].

The influence of the substrate doping concentration on the latch-up behavior of a twin-well CMOS process was investigated in [62]. The result of this work was that with a highly doped substrate (0.01–0.02 Ωcm) and with a 10 μm thick epitaxial layer (1.7–2.5 Ωcm), the emitter firing currents of the NPN and PNP transistors could be increased from 30 to 250 mA by implementing an N⁺ guard ring around the P emitter in the N well. For a low substrate doping (1.7–2.5 Ωcm), an N⁺ guard ring around the P emitter increases the emitter firing current of the NPN transistor from about 7 to 235 mA. An additional P⁺ guard ring around the N emitter increases the emitter firing current of the PNP transistor from about 9 to 60 mA. From the results of [62] we can draw the conclusion that in OEICs with reduced doping concentration in the epitaxial layer or/and increased epitaxial layer thickness, the positive influence of the highly doped substrate on the latch-up immunity is reduced. A second conclusion, however, is that the latch-up immunity can almost be regained with the implementation of guard rings.

Another very effective design measure for the suppression of latch-up is the implementation of guard rings around the wells. These design measures applied as a precaution for OEICs with a reduced doping concentration in the epitaxial layer, however, would require die area and they might result in an unacceptable increase of the die area of highly integrated digital OEICs. For analog OEICs, which contain far fewer transistors, the additional die area for latch-up precaution would be easier to accept. Because of the large economical importance of digital ICs and because of the potential high-volume market for OEICs in optical interconnects, however, the latch-up immunity of PIN-CMOS-OEICs was examined experimentally.

In order to investigate the influence of the doping concentration in the epitaxial layer on latch-up immunity a test structure (see Fig. 2.24) was fabricated together with the CMOS-integrated PIN photodiodes.

The distance of the emitters from the well boundary was 2 μm each. A V_{DD} voltage of 5.5 V was used in order to account for tolerances of power supplies. The hole

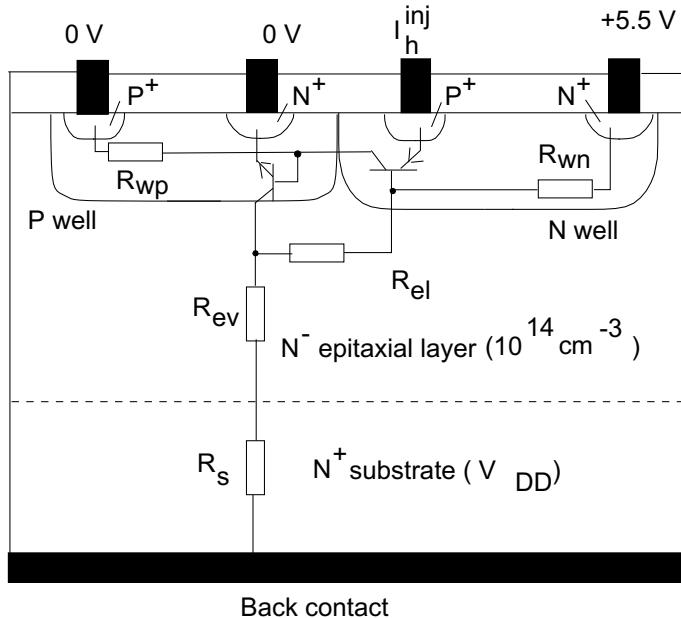
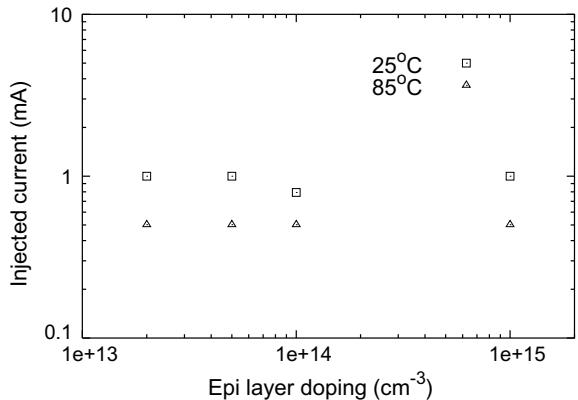


Fig. 2.24 Schematic cross section of the latch-up test structure [60]

Fig. 2.25 Injected hole current I_h^{inj} necessary for triggering latch-up versus doping concentration in the epitaxial layer [60]



current injected into the P⁺ emitter of the parasitic PNP transistor necessary for triggering the thyristor structure was measured [60]. The injected hole current necessary for triggering latch-up is shown in Fig. 2.25 for several doping concentrations in the epitaxial layer. The injected hole current necessary for triggering latch-up is constant when the doping concentration of the epitaxial layer is reduced from $1 \times 10^{15} \text{ cm}^{-3}$ to $2 \times 10^{13} \text{ cm}^{-3}$ for room temperature and for an elevated temperature of 85 °C [60]. Latch-up immunity, therefore, is not degraded when PIN photodiodes are integrated. Accordingly, the latch-up aspect does not require a modification of the design rules

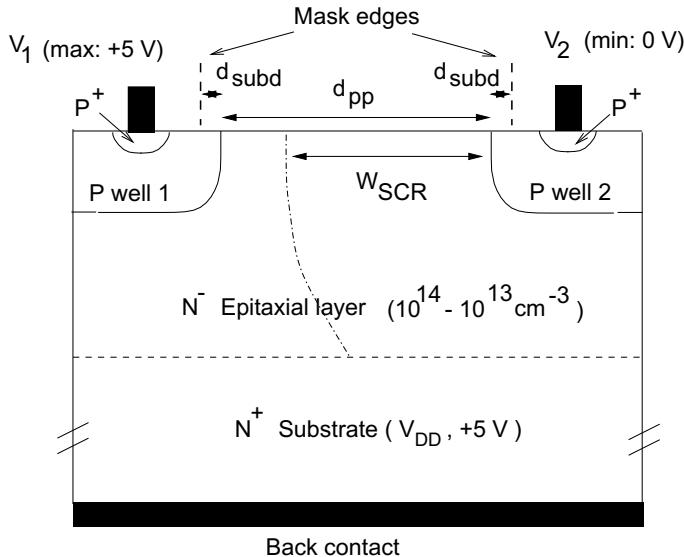


Fig. 2.26 Schematic to illustrate the reach-through effect between analog wells of the same type [63]

of the CMOS process used for PIN photodiode integration and die-area-consuming guard rings are not necessary for analog and digital CMOS OEICs.

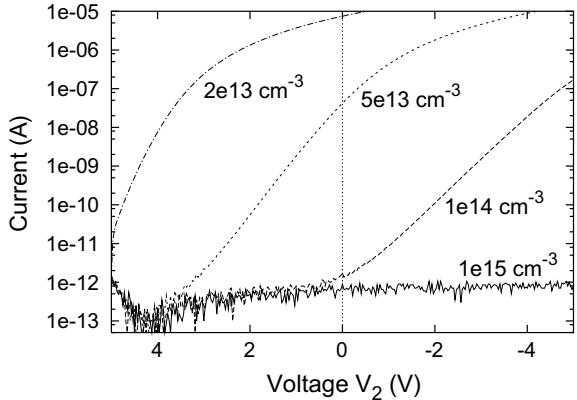
Reach-Through Effect

The reach-through or punch-through effect is important between neighboring analog wells which have a doping type different from that of the substrate. Analog wells are not at the power supply voltage rails like digital wells. Let us assume for simplicity that one of the wells is at the substrate potential (Fig. 2.26).

Then the potential difference between the two wells can be maximum. The consequence is that the space-charge region extends most widely from one well towards the other. When the space-charge region extends to the other well for a large potential difference of the two wells, a current begins to flow between the two wells (Fig. 2.27), which may change the operating point in an analog circuit. Therefore, there is a design rule which sets the minimum distance of analog wells.

When we reduce the doping concentration of the epitaxial layer, the space-charge region extends further for a constant difference voltage. The design rule for the minimum distance of analog wells, therefore, has to be modified [60]. According to (1.22) with the difference voltage of the two wells U_{12} and considering the lateral subdiffusion of the two wells d_{subd} plus a security distance d_{sec} , the new minimum distance of analog wells d_{pp}^{\min} [63] results

Fig. 2.27 Measured reach-through current for a P-island distance of 10 μm ($V_1 = +5 \text{ V}$; V_2 is varied from +5 to -5 V) [63]



$$d_{pp}^{\min} = \sqrt{\frac{2\epsilon\epsilon_0}{qN_I}(U_D + |U_{12}| - \frac{2k_B T}{q})} + 2d_{subd} + d_{sec}. \quad (2.3)$$

The difference in this equation compared to the original expression for the design rule is that N_I instead of the standard doping concentration in the epitaxial layer is used. For N_I , the low tolerance limit of the epitaxial doping concentration has to be used. $|U_{12}|$ is the maximum potential difference between two neighboring wells which have a doping type opposite to that of the substrate. This maximum potential difference depends on the actual circuit.

The worst case for the maximum potential difference would be, for instance, $V_1 = 5 \text{ V}$ and $V_2 = 0 \text{ V}$. Figure 2.27 shows reach-through currents between a P well and a P^+ island measured in a test structure actually designed for investigation of diffusion of photogenerated carriers. For $N_I = 10^{15} \text{ cm}^{-3}$, there is no reach-through current. For $N_I = 10^{14} \text{ cm}^{-3}$, there is a very low reach-through current of about $1.5 \times 10^{-12} \text{ A}$ at $V_2 = 0 \text{ V}$. For $N_I = 5 \times 10^{13} \text{ cm}^{-3}$, the reach-through current for $V_2 = 0 \text{ V}$ is about $5 \times 10^{-8} \text{ A}$, which should be tolerable for most N^-N^+ -CMOS-OEICs [64]. Actually the potential difference between P wells is less than 5 V in most circuits, and measurements confirmed that an N^-N^+ -CMOS-OEIC also works well with a doping level of $N_I = 2 \times 10^{13} \text{ cm}^{-3}$. The distance of two analog wells of 10 μm was sufficient for the circuit in [65]. For many analog circuits this value, therefore, does not increase dramatically above the original minimum analog well distance of 6.6 μm .

PIN Photodiode in 0.35 μm and 0.15 μm CMOS

A PIN photodiode was later integrated in a more modern, modular 0.35 μm process, which has also a bipolar extension to a BiCMOS process [66]. Figure 2.28 shows the cross section of this PIN photodiode. The grown thickness of the P^- epitaxial layer on the P^+ substrate was about 14 μm . The doping in the epitaxial layer was below $5 \times 10^{13} \text{ cm}^{-3}$. As an anode contact a large-area P^+/P -well substrate contact

Fig. 2.28 Cross section of PIN photodiode in 0.35 μm CMOS

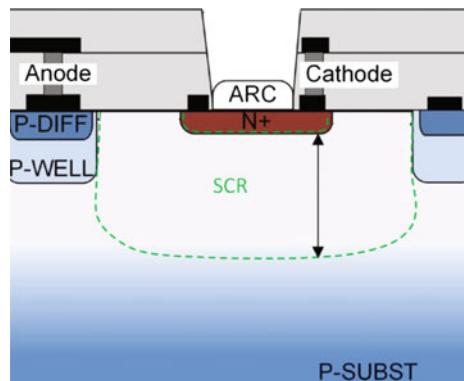
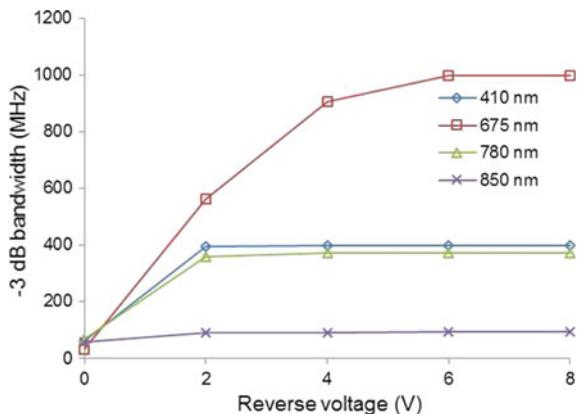


Fig. 2.29 Bandwidths of PIN photodiode in 0.35 μm CMOS in dependence on reverse voltage



was used. Due to the anti-reflection coating (ARC) optimized for red light, quantum efficiencies of 96 and 55% were achieved for 680 and 850 nm, respectively.

For a reverse voltage of -8 V , bandwidths of 398, 998, 372, and 93 MHz were measured for 410, 675, 780 and 850 nm, respectively. Figure 2.29 depicts the dependence of the -3 dB bandwidth of this pin photodiode on the reverse voltage. For 410 nm light, a considerable part of the photogenerated carriers is subject to slow carrier diffusion in the N^+ cathode. For 780 and 850 nm light, there is a strong contribution of carrier diffusion from the P^+ substrate, which limits the bandwidth especially for 850 nm due to the larger penetration depth.

A PIN photodiode was also integrated in a 0.15 μm CMOS process [67]. In this process also a deep-N-well (called N-ISO) was available to isolate the P-well of the NMOS transistor from the P-substrate. Therefore, with a reverse bias of the PIN photodiode of 8 V, bandwidths of 1.2 GHz for 650 nm and 700 MHz for 850 nm were possible. This bandwidth for 850 nm is much higher than the bandwidth of the PIN photodiode in 0.35 μm CMOS mentioned above, because the thermal budget of the 0.15 μm process is much lower and therefore its P^+ substrate diffuses much less

into the low-doped epitaxial layer. Due to this thinner transition region between the P⁺ substrate and the low-doping region in the epitaxial layer the bandwidth of the 0.15 μm PIN photodiode is much higher. The maximum responsivity of 0.46 A/W was observed for 730 nm, which corresponds to a quantum efficiency of 78.3%.

2.2.7 Charge-Coupled-Device Image Sensors

Charge-Coupled-Device (CCD) image sensors are an economically very important sub-division of integrated optical receivers. CCD image sensors were invented at Bell Labs [68]. Since then, there have been numerous publications on CCD image sensors (for instance [69–81]), because these sensors are key devices for high-volume video cameras and still-photography cameras. There is also a huge number of CCD imaging devices available on the market [82]. Record minimum pixel size was reduced from 40 μm in 1972 to 5 μm in 1995 [83]. The reported record maximum pixel number has increased from less than 2000 to 26 million in the same period [83].

Usually CCD image sensors are simply called CCDs. An advanced CCD image sensor, however, consists of photodetectors, CCDs for readout, and MOSFET source follower output drivers. For the photodetectors, PN photodiodes can be used. The CCD is a much more complicated device than the photodiode. Therefore, the CCD will be explained in some detail. The CCD is basically an array of closely spaced MOS capacitors (see Fig. 2.30). A quantity of charge can be stored below one gate when an appropriate biasing of this and the neighboring gates is chosen (see Fig. 2.30a). The electrons representing the stored charge are confined in the potential well below the electrode with the higher voltage. When the third electrode to the right of this electrode is pulsed to a higher voltage the electrons begin to transfer to its deeper potential well (see Fig. 2.30b). The voltages 5, 10, and 15 V, are chosen arbitrarily; meanwhile they have lower values (e.g. 5, 8, and 10 V [84]; 2.0 and –8.0 V [85]; 1.8 V [86]; 1.1 V [78]) in advanced CCDs.

Figure 2.31 shows the schematic cross section of a three phase N-channel CCD together with its basic input and output structures. The six (in real devices of course many more) MOS capacitors with their gates connected to the clock lines Φ_1 , Φ_2 , and Φ_3 form the main body of the CCD. The input diode (ID) and input gate (IG) inject charge packets into the main CCD body. The output gate (OG) and output diode (OD) extract the transferred charge packets from the main CCD body. Before the charge transfer, the input and output diodes are at high positive voltage in order to deeply deplete the surfaces under IG and OG. ID and IG, therefore, cannot supply electrons into the main CCD array. The potential wells under the CCD array, therefore, can be assumed to be empty. Then voltages $\Phi_1 > \Phi_2, \Phi_3$ are applied. The potential well below Φ_1 is deeper than the others. When the voltage of ID is lowered electrons flow to the potential well under the first Φ_1 electrode through IG which is at a potential higher than 5 V but lower than 10 V. At the end of the injection, the surface potentials under the IG and Φ_1 electrodes are the same as the input diode potential and the electrons are now stored under the IG and first Φ_1 electrode. Now ID can be returned

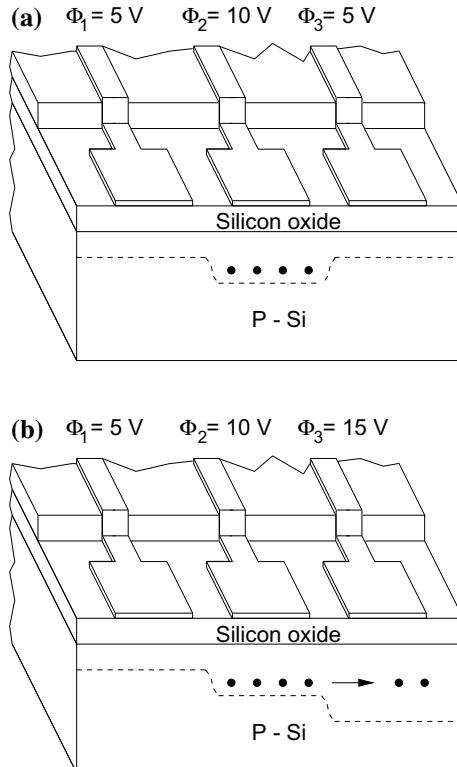


Fig. 2.30 Charge-coupled device. **a** Charge storage; **b** charge transfer [87]

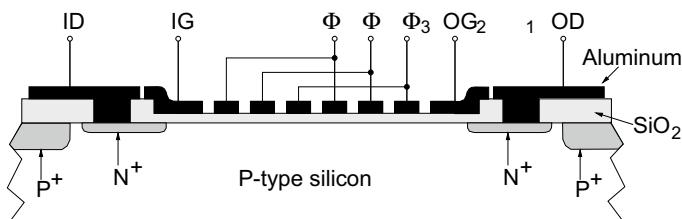


Fig. 2.31 Schematic cross section of a CCD [13]

to a higher voltage. Then, the voltage at the Φ_2 electrode is increased and the voltage at the Φ_1 electrode is reduced in order to transfer the charge to the second electrode. Now, the voltage at the Φ_3 electrode is increased and the voltage at the Φ_2 electrode is reduced in order to transfer the charge to the third electrode. This pulse sequence is repeated until the charge packet is stored under the second Φ_3 (or in a real device the last Φ_3) electrode. OG and OD are at high potentials and when the voltage at the

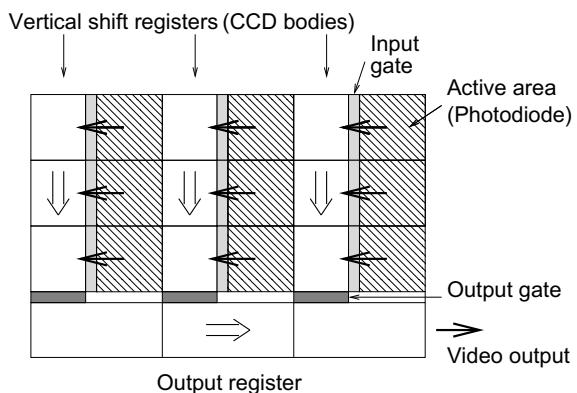
Φ_3 electrode is reduced, the charge is pushed to the output diode, thereby giving an output signal proportional to the size of the charge packet at the output terminal.

In a CCD image sensor, the input diode is the photodiode. Therefore, ID is larger in a CCD image sensor than shown in Fig. 2.31 and not covered by metal, of course. During the image integration time i.e. when the ID voltage is high, the electrons photogenerated in the space-charge region are collected and stored under the N^+ island of ID. The photogenerated holes drift to the substrate. Electrons photogenerated in the substrate below the space-charge region diffuse slowly and may recombine with holes or diffuse to neighboring pixels giving rise to cross-talk. The collected charge is proportional to the integration time and to the light intensity as long as the well is not filled. During the charge transfer in the CCD, almost no charge is lost and the output signal is proportional to the light intensity detected by the ID photodiode.

The minimum of the potential well is at the Si/SiO₂ interface, which, therefore, is a critical part of the described MOS structure. The Si/SiO₂ interface may capture electrons in localized states, preventing their proper readout. To improve the situation, buried-channel structures are used, where a thin top layer of the substrate is N-type doped [88]. The resulting potential distribution has a minimum in the silicon somewhat below the Si/SiO₂ interface, which represents a ‘cleaner’ place for storing electrons. A transfer inefficiency, defined as the relative amount of electrons left behind after transfer from one stage to the next, as low as 10^{-5} per stage is typical for buried-channel CCD structures [89].

In an advanced CCD image sensor, there are arrays of photodiodes and arrays of input gates (Fig. 2.32). The advantage of this interline transfer CCD (IT-CCD) arrangement [90–92] is that the charge transfer from the detector to the storage cells can be made very quickly since only one transfer stage is involved. In older CCD image sensors the CCD main bodies in image registers themselves were used as the photodetectors and the complete image was transferred to a storage register requiring 3N charge transfers [93]. The electrodes were made from polysilicon resulting in a low sensitivity for the blue spectral range. These two disadvantages led to the IT-CCD structure. The larger noise of the IT-CCD with photodiodes [83, 94] was less

Fig. 2.32 Schematic of a interline-transfer CCD (IT-CCD)



important. Each third MOS capacitor can have its own photodiode and input gate. One line of a picture with N pixels can be read out through the CCD output register in a serial mode to a single video output (Fig. 2.32). A complete CCD image sensor consists of a two-dimensional matrix ($N \times M$) of photodiodes and input gates as well as M CCD main bodies. The active areas are separated by channel stops consisting of narrow regions with heavy doping in order to prevent blooming, i.e. the spilling over of electrons from full wells into neighboring channels.

For the sake of completeness it should be mentioned that two-phase CCDs are also possible. These two-phase CCDs require an additional doping structure for generating an internal lateral electric field [78, 86, 93].

Single-chip color image sensors are obtained using three photodiodes in each pixel. These three photodiodes carry a red, a green, or a blue color filter, which are printed on the insulator on the CCD image sensor surface. The color filters are arranged in a mosaic pattern for achieving a better isotropy in resolution than using stripes of the three color filters [93].

A 2/3-inch 1280×1600 CCD image sensor for still photography was fabricated with a minimum feature size of $0.5 \mu\text{m}$ [80]. Its chip size was 90 mm^2 with a pixel size of $5.1 \times 5.1 \mu\text{m}^2$. Supply voltages of 3.3 and 12 V were necessary. The maximum charge storage capacity per pixel was 40,000 electrons. A sensitivity of $390 \text{ mV}/(\text{Lux s})$ was reported for green light. The output driver consisted of a triple source follower. The output sensitivity was larger than $19 \mu\text{V/electron}$ with a saturation output voltage of 0.9 V and an output noise of 10 electrons root-mean-square (RMS). This CCD image sensor was capable of taking six images per second in full resolution [80].

The fill factor of CCD imagers is considerably less than 1. Therefore microlenses were integrated in order to increase the sensitivity [95, 96]. A clock frequency of 37.125 MHz was used in a 2 million pixel CCD image sensor for a HDTV camera [97]. A similar clock frequency of 40 MHz was reported in [85]. Maximum output data rates of 250 Mb/s for CCD arrays [98] were reported. The clock rate of CCD arrays finally is limited as the transfer inefficiency increases at higher clock frequencies, depending on the actual device structure [83]. A clock rate of 325 MHz has been reached [99]. The larger the pixel number the smaller the frame rate and vice versa. A high frame rate of 10^6 frames/s was obtained for a rather small 360×360 pixel CCD imager. The readout frequency of CCDs, therefore, is rather limited. It is, however, sufficient for video applications. CCD image sensors are rather well developed and the reduction in cell size is coming to an end. The limit is set by diffraction occurring at the aperture above the photodiode in IT-CCD image sensors [100]. When the width of the aperture in the tungsten photoshield becomes smaller than about $1 \mu\text{m}$, the response of the photodiode begins to drop [100].

CCD image sensors were integrated in CMOS technology. For instance a CMOS/buried-N-channel CCD compatible process has been described [101]. Another CCD/CMOS process was suggested in [102]. The efforts to integrate CMOS with high-pixel-count CCD imagers to increase CCD functionality, however, has not been fruitful due to cost [103]. The aspect which makes it difficult to integrate CCD devices in CMOS technology is the need for closely spaced, thin polysilicon electrodes for charge transfer being incompatible with the self-adjusting gate-source/drain process-

ing scheme. Furthermore, the well doping profiles and threshold implants are not optimized for CCD devices. Silicided gates in advanced CMOS processes increase the difficulties.

A low-pixel-count 128×128 pixel CCD image sensor in a $2\text{ }\mu\text{m}$ CMOS technology with 128 charge-sensitive amplifiers and 128 analog-to-digital converters has been reported [104]. Only one 5 V power supply was necessary. The maximum picture rate was 25 pictures per second.

2.2.8 Active-Pixel Sensors

Nowadays, there is a trend towards a camera-on-a-chip (CoC), which consists of optical sensor elements and highly integrated signal-processing circuitry with a low power consumption. CCDs, therefore, have to compete with a severe rival, the active-pixel sensor (APS), for many imaging applications. It has a performance competitive with CCDs with respect to output noise, dynamic range, and sensitivity but with vastly increased functionality due to its CMOS compatibility and with the potential for lower system cost as well as for a camera-on-a-chip [103].

The APS was described first by Noble in 1968 [105]. Advanced APSs are now emerging from the most advanced image-sensor research and development laboratories in Japan [106–109]. Laboratories in the United States [110–116] and in Europe [117, 118] are trying to catch up. The charge is shifted from pixel to pixel in a CCD in order to read out the image. An APS (see Fig. 2.33), by contrast, acts similarly to a random access memory (RAM), wherein each pixel contains its own selection and readout transistors, which serve as amplifiers or buffers. The steadily decreasing feature sizes of VLSI/ULSI technologies make it possible to integrate source follower MOSFETs or amplifiers together with each photodetector for all pixels in a large two-dimensional array.

The advantages of an APS compared to a CCD sensor accordingly are:

- (i) random access
- (ii) nondestructive readout
- (iii) easy integratability with on-chip electronics.

Although CCDs can be integrated in CMOS processes, undesirable compromises in the performance of CMOS or CCD devices have to be made [103]. Important weaknesses of the CCDs are that (i) the charge-transfer efficiency (CTE) has to come very close to 100% for large pixel numbers, i.e. that the charge-transfer inefficiency has to come close to 0%, that (ii) large pixel sizes at high data rates are difficult to implement, and that (iii) readout rates are limited.

There are two types of active-pixel sensors: (i) photo-gate APS and (ii) photodiode-type APS. A photo-gate APS requires one charge transfer from the photo-gate into the storage region FD (Fig. 2.34). The photo-gate APS in its function, therefore, resembles a sample&hold circuit. The pixel is selected using transistor S in order to read out the signal. The storage region or output node is reset using transistor R. After reset, the signal charge is transferred from under the photo-gate into the

Fig. 2.33 Block diagram of an active pixel sensor imager with random access to each pixel [119, 120]

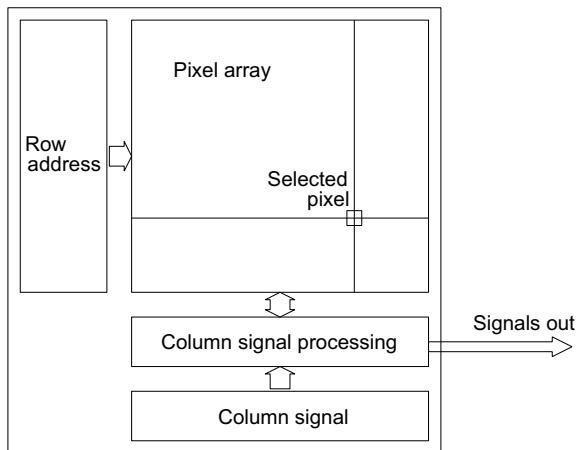
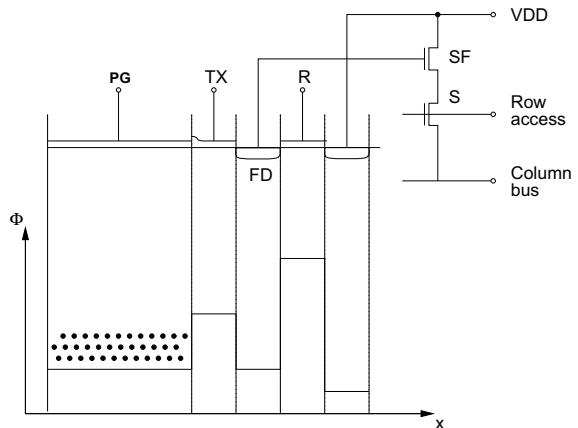
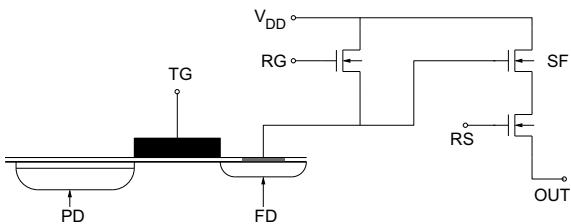


Fig. 2.34 Pixel circuit of a photo-gate active-pixel image sensor [121]



storage node FD. The change in the source-follower voltage between the reset level and the final level is the output signal from the pixel. In more detail, the operation of the sensor is as follows: The photogenerated charge is integrated under the pixel photo-gate PG, which is biased at +5 V. The transfer gate TX and the gate of the reset transistor R are biased at +2.5 V and the selection transistor S is also biased off with 0 V at its gate for charge integration. After the signal integration, all pixels or only the selected ones in the row can be read out simultaneously onto column lines. For this purpose, the pixels are first addressed by the row selection transistor S biased at +5 V, which activates the source-follower output transistor in each pixel. Now, the reset gate R can be pulsed briefly to +5 V in order to reset the floating diffusion output node FD. Then, the photo-gate PG is pulsed low to 0 V, whereby TX is held at +2.5 V, to transfer the integrated signal charge under the photo-gate to the floating diffusion output node FD. The gate potential of the source follower changes and the output voltage of the pixel changes depending on the amount of integrated

Fig. 2.35 Cross section of photodiode and transfer gate with the schematic of the remaining transistors in the 4-transistor pixel cell of a photodiode-type APS [120]



charge. It should be mentioned explicitly that without resetting the storage node FD before pixel selection, the readout is nondestructive, i.e. the pixel can be read out much more often than once.

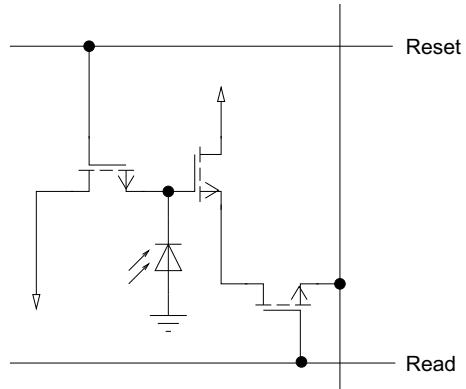
A 128×128 array with the pixel element shown in Fig. 2.34 was integrated in a $2\text{ }\mu\text{m}$ P-well CMOS process. A 100% compatibility of the image sensor with the CMOS process was reported [121]. A total area of $6.8 \times 6.8\text{ mm}^2$ was necessary for this array of pixels with the size of $40 \times 40\text{ }\mu\text{m}^2$. The larger part of this pixel size was occupied by the transistors and the active, i.e. light sensitive, area of each pixel was 26%. The output conversion factor was $4.0\text{ }\mu\text{V/electron}$. A noise floor of 42 electrons-rms and a dynamic range of 71 dB were reported [121].

An example of a photodiode-type APS pixel unit with a 4-transistor pixel cell architecture is shown in Fig. 2.35. Here the charge is integrated with the photodiode PD. For readout, this charge can be transferred by the transfer gate TG to the storage node FD. The rest of the circuit is similar to the schematic in Fig. 2.34. A larger conversion gain of $13\text{ }\mu\text{V/electron}$ was measured for a 256×256 pixel imager array with a pixel size of $7.8\text{ }\mu\text{m}$ and a fill factor of 35% in a $0.6\text{ }\mu\text{m}$ CMOS technology [120]. A dynamic range of 66 dB was obtained. The above mentioned inferiority of photodiode-type CCD imagers to MOS-detector-type CCDs with respect to noise is avoided here by providing each photodiode with its own amplifier and reset transistor [83].

A photodiode-type APS actually does not require a transfer gate. The photo-generated charge can be stored in the photodiode itself [122]. Such an APS schematic is shown in Fig. 2.36.

It is worthwhile to compare the photodiode-type APS and the photo-gate APS. The photo-gate APS has a lower quantum efficiency due to photons being absorbed in the polysilicon gate. It also needs a larger pixel size due to an additional transfer switch and it is less compatible with standard CMOS processes because it requires a thin polysilicon layer with a thickness of only about 50 nm. The advantages of the photo-gate APS are a lower noise and a higher conversion gain due to a smaller floating node capacitance [122]. A 256×256 CMOS active pixel sensor was previously combined with circuitry for motion detection [119]. The area of each pixel was $20 \times 20\text{ }\mu\text{m}^2$ with a fill factor (photo-gate area/total pixel area) of 25%. This APS was realized in a $0.9\text{ }\mu\text{m}$ CMOS process. A conversion gain of $7\text{ }\mu\text{V/electron}$ was measured. The pixel output transistor was found to be the primary APS noise source. A typical output referred noise level of 29 electrons rms and a dynamic range of 74 dB was reported.

Fig. 2.36 Active pixel with three MOSFETs [106]



Since the first edition of this book a lot of new literature on active pixel sensors came up. Unfortunately it is only possible to describe a few impressive approaches here.

A 250 Mpixel CMOS image sensor in a $0.13\text{ }\mu\text{m}$ 1P4M CMOS technology was introduced at ISSCC 2016 [123]. To overcome the problems of increased clock frequencies (e.g. 2.37 GHz in [124]) and related higher power consumption or of assuring uniformity of multi-ramp signals [125] of ADCs for enhanced pixel numbers, a dual-gain amplifier was exploited in each column single-slope ADC (SS-ADC). With this single-slope dual-gain (SSDG) ADC, the conversion period of the ADC was shortened and the dynamic range was increased without rising the power consumption. The shorter conversion time allowed readout of more pixels. A 75% shorter conversion period and a 6 dB larger dynamic range than with a conventional SS-ADC was reported [123]. The pixel size was $(1.5\text{ }\mu\text{m})^2$ and the total die size was $32.84 \times 25.85\text{ mm}^2$. The pixel sensitivity was $4,100\text{ e-/lx/s}$, the full-well capacity was $7,550\text{ e-}$, the SSDG-ADC dark random noise was $3.5\text{ e-}_{\text{rms}}$, the conversion gain was $91\text{ }\mu\text{V/e-}$, and the SSDG-ADC dynamic range was 66.7 dB . The frame rate was 5 fps at full pixel resolution. The ADC count frequency was 810 MHz . At 3.3 and 1.2 V , the power consumption amounted to 1.97 W [123].

Also in 2016 a CMOS image sensor with even 391 Mpixels in 90 nm frontend and 65 nm Cu backend technology was presented [126]. It was designed for airborne mapping applications with reduced acquisition (flight) time and costs. The array contained 26,456 times 15,072 pixels at a pitch of $3.9\text{ }\mu\text{m}$. 2D-stitching with 6 times 3 repetitions of a $4,352 \times 5,000$ pixel stitch block had to be used, because the sensor area exceeded the reticle size considerably. The diagonal of the active pixel area was 117.45 mm . A single-slope ADC was implemented in each row. A switched-capacitor circuit generated the ramp for these SS-ADCs. A linear saturation charge of 31.5 ke- and a linear dynamic range of 78 dB was reported, which compares favorably to 67 dB of a large-area CCD sensor [127]. The sensor chip measured $105.18\text{ mm} \times 65.63\text{ mm}$. Its power consumption at full resolution image capture of 14 bits and 1 fps was about 1.75 W [126].

There are developments to increase the resolution of television beyond high definition (HD). There is a new standard for ultra-high definition TV (UHDTV) with $7,680 \times 4,320$ pixels, 120 Hz frame rate and 12 bit tone resolution [128]. This standard drove the development of advanced image sensors using three-dimensional (3D) integration of sensor chip and electronics chip as well as backside illumination. 3D-integration and backside illumination allow separate optimization of sensor chip and electronics chip leading to high sensitivity of small pixels, less pixel random noise, and high operation speed. A few image sensors exploiting these techniques are described in the following.

Three-dimensional chip integration [129] was used to realize back-side illuminated (BSI) image sensors. A 33 Mpixel array (photodiode type APS with 3T pixel cells) was 3D-stacked on a 1P5M logic CMOS wafer [130]. The 3D-integration method (see also Sect. 7.1) used top-metal face-to-face bonding. With this bonding technique 2/3 of the pixel pitch possible with Through-Silicon-Via (TSV) 3D-integration was achieved. In contrast to TSV 3D-integration, the face-to-face bonding allowed connections below the pixels. A redistribution layer (RDL) was added above the top metal layers of both the pixel wafer and the electronics wafer. A much higher pixel-array-to-chip area ratio (82.5%) was obtained than with the same pixel array in a conventional 2D image sensor (30%). Four identical 8.3 Mpixel circuit blocks could be used for the 33 Mpixel 1/4-inch sensor and 16 circuit blocks can be implemented in a 1/2-inch image sensor with 133 Mpixels [130].

In [128], a 33 Mpixel 3D-stacked sensor for UHDTV with a pixel pitch of $1.1 \mu\text{m}$ and 240 fps capability was introduced. A face-to-face hybrid stacking process was applied. A $1,932 \times 4$ ADC and correlated double sampling (CDS) circuit array with analog amplifiers having a gain of up to 4 was arranged below the pixel area. The pipelined and parallel working 3-stage ADC reduced the conversion time, kept the power consumption low and enabled 12 bit precision within a horizontal scan time of $0.92 \mu\text{s}$ at 240 fps. The ADC is split into three stages: the first single-ended cyclic ADC converted the upper 3 bits, the second single-ended cyclic ADC converted the middle 6 bits, and the third successive-approximation register (SAR) ADC converted the lower 3 bits. The horizontal pitch of the interconnections was $4.4 \mu\text{m}$. To save transistor count in the pixel area, 4×4 -pixel units having four sets of 2×2 -shared pixels were implemented and repeated along the column direction. The pixel type was therefore 1.75-transistor 2×2 -shared pixel. The pixel size was $(1.1 \mu\text{m})^2$. A conversion gain of $92 \mu\text{V/e-}$ and a full-well capacity of $5,700 \text{ e-}$ were reported. The random noise was $4.5 \text{ e-}_{\text{rms}}$ for a gain of 1 and $3.5 \text{ e-}_{\text{rms}}$ for a gain of 4, both at 240 fps. The sensor consumed 3.0 W at 240 fps [128]. This image sensor exceeded the frame rate of [131] by a factor of two whereby the power consumption increased only from 2.5 to 3.0 W .

Another image sensor used 3D-integration to implement a DRAM as frame memory in order to speed up readout [132]. It was noted, that this is important since cell phone cameras cannot have mechanical shutters and use rolling exposure. Three chips were 3D-integrated: the top-layer 90 nm 1Al5Cu CMOS chip with special additional process steps for back-side illumination of the pixel array (upside down), the middle chip being a 30 nm 1W3Al DRAM chip (upside down), and the bottom 40 nm

1Al6Cu logic CMOS chip. The pixel size was $(1.22\text{ }\mu\text{m})^2$. Column single-slope 10-bit ADCs and DACs for ramp generation, and a 102 Gb/s bus were implemented. The DRAM with a capacity of 1 Gbit had four channels with 128 bit 200 MHz input and output, which allowed a high frame rate output. Electronic Image Stabilization (EIS) was achieved by using a gyro sensor. The power consumption was about 600 mW at highest resolution and 30 fps. A dynamic range of 64.8 dB was reported [132].

Since a trend in customers desires exists towards darker scenes as for instance in moon light, the dynamic range of image sensors was extended by implementing single-photon avalanche diodes [133]. This image sensor, however, showed a larger chip area and dark currents. In [134] a back-side illuminated topology with a pinned photodiode was investigated. The multiplication region was located at the N-P junction within a N-P-P⁻-P⁺ structure. The storage region was formed by the N region and a bottom P⁺ pinning layer. The electric field was vertical and its strength could be controlled by the voltage V_{APD} applied to the top P⁺ layer. With this voltage the sensitivity of the photodiode could be switched between NL-mode (linear-mode, $V_{\text{APD}} = -21.3\text{ V}$, $E = 4.0 \times 10^7\text{ V/m}$) and HS-mode (single-photon detection mode, $V_{\text{APD}} = -23.3\text{ V}$, $E = 4.4 \times 10^7\text{ V/m}$). It was possible to change this voltage within 1 ms, which was an order of magnitude below the usual exposure time. The dark counts were below 0.1 cps at $V_{\text{APD}} = -23.3\text{ V}$. In such a way the image sensor could be used for daylight (10 lux) and moonlight (10^{-4} lux) applications with a dynamic range of 100 dB [134].

2.2.9 Amorphous-Silicon Detectors

Hydrogenated amorphous silicon (a-Si:H) has been employed for a variety of imaging devices for low cost applications in large area sensor technology [135–139]. Page-sized two-dimensional a-Si:H photodetector arrays have been realized [139]. Usually, glass substrates are used for the low-temperature fabrication of a-Si:H imaging devices. A huge number of dangling bonds is present in amorphous silicon. In order to obtain stable devices, the a-Si is hydrogenated, i.e. the dangling bonds are saturated and in such a way passivated with hydrogen atoms.

The bandgap of a-Si:H is approximately 1.72–1.78 eV slightly depending on the deposition process. The bandgap of a-Si:H is much larger than that of crystalline silicon and the spectral response of a-Si:H suits the sensitivity of the human eye much better than that of crystalline silicon. The sensitivity of a-Si:H ranges from blue to red. Infrared light with $\lambda > 780\text{ nm}$ cannot be detected with a-Si:H devices. The absorption coefficient of a-Si:H depends on the hydrogen content and on the deposition process. A typical curve for the absorption coefficient is shown in Fig. 2.37 [140]. The absorption coefficient of a-Si:H is much larger than that of crystalline Si in the visible spectrum. An a-Si:H layer with a thickness of 1 μm is sufficient for completely absorbing light with $\lambda < 0.7\text{ }\mu\text{m}$ [141].

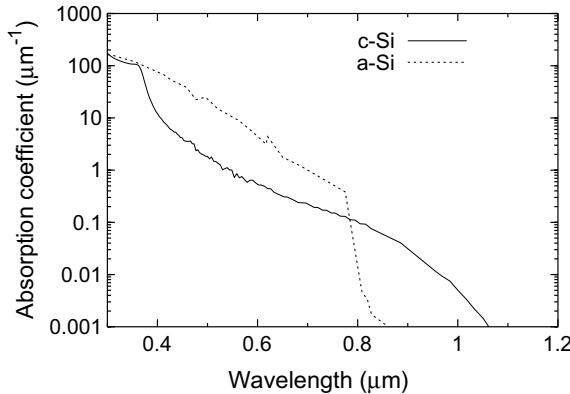


Fig. 2.37 Absorption coefficient of a-Si:H [140]

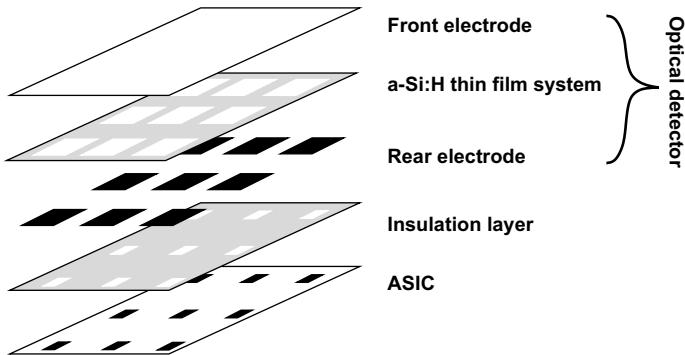


Fig. 2.38 Layer sequence of a TFA sensor [142]

Amorphous Silicon Image Sensors

Amorphous silicon image sensors can be integrated vertically on microelectronic circuits due to the low-temperature deposition of a-Si:H (below 300 °C). In contrast to the low fill factor of active-pixel sensors, vertically integrated a-Si:H image sensors provide a fill factor close to 100%. The crystalline integrated circuit typically consists of identical sub-circuits underneath each pixel detector and peripheral circuitry at the boundary of the light sensitive area. An insulating layer separates the optical detector from the crystalline chip.

Another advantage of a-Si:H image sensors is their large dynamic range of 60 dB, which can be further extended considerably by electronic measures. The concept of *Thin Film on ASIC* (TFA) [142, 143] adds much flexibility to a-Si:H image sensors. The TFA concept allows to design and optimize both the thin-film detector and the application specific integrated circuit (ASIC) independently. Figure 2.38 shows the layer sequence of a TFA sensor.

The a-Si:H thin film system of a TFA sensor does not need to be patterned and can be fabricated in a plasma-enhanced chemical vapor deposition (PECVD) cluster tool without temporarily being taken out of the vacuum for lithography. A very high yield of almost 100%, therefore, is possible for the thin film system. Furthermore, fabrication costs are very low and barely exceed those of an ordinary ASIC. Without lithography, the pixel is simply defined by the size of its rear electrode. The continuous thin-film layer permits lateral balance currents between adjacent pixel detectors, resulting in cross-talk and in a reduced local contrast. A self-structuring technology for the suppression of this effect was suggested in [144].

A pixel of the least complex a-Si:H image sensor, which provides minimum pixel sizes and maximum resolution, consists of an a-Si:H photodiode and a PMOS transfer transistor. The function principle is based on a simple charge transfer from the pixel to the readout line [145]. The photocurrent discharges the capacitance of the reverse-biased photodiode during the integration time, resulting in a signal charge proportional to the illumination intensity and to the integration time. This operation mode is called charge storage mode. The amount of storable charge can be increased by an additional MOS capacitance, which can be integrated into each pixel on the ASIC in order to achieve a higher signal-to-noise ratio. In [143] this type of image sensor was called a varactor analog image detector (VALID). VALID is addressed linewise and read out columnwise. A random access sensor is also feasible employing a modified peripheral circuitry. 128×128 pixels with an area of $16 \times 16 \mu\text{m}^2$ each were integrated in VALID using a standard $0.7 \mu\text{m}$ CMOS ASIC process. A saturation illumination of 2500 Lux after an integration time of 20 ms was achieved with an integration capacitance of 250 fF. The dynamic range amounted to 60 dB. A good linearity and no visible image lag was observed. The circuits of more complex TFA image sensors for even higher dynamic ranges, which are essential in the field of artificial vision, will be discussed in Sect. 6.4.2.

2.2.10 CMOS-Integrated Bipolar Phototransistors

Photodetectors with a built-in amplification are most desirable for weak optical signals, especially in a comparatively simple CMOS process because of the high degree of standardization, its low cost, and the widespread interest in CMOS circuits.

The simplest way to integrate a bipolar phototransistor in a CMOS process without any process modifications is to use the N well as the floating base of a PNP transistor, the P^+ source/drain diffusion as the emitter and the P^- / P^+ substrate as the collector (Fig. 2.39). This vertical bipolar phototransistor (VBPT) then can be used as an emitter follower only, because the collector is at substrate potential, i.e. at 0 V. The complementary NPN phototransistor on an N^- / N^+ substrate material is also possible, of course. The simple structure shown in Fig. 2.39, however, has the additional disadvantage of a low sensitivity for short and medium wavelengths due to the large N-well/P-substrate junction depth.

Fig. 2.39 Cross section of the simplest CMOS-integrated PNP phototransistor [146]

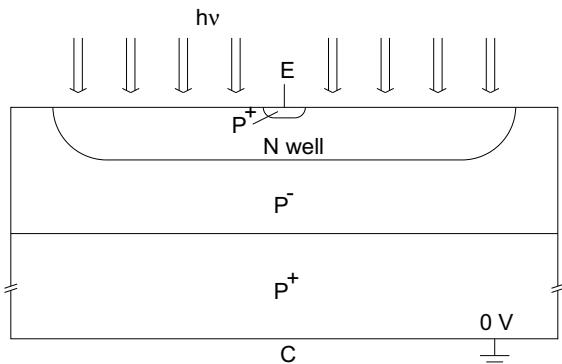
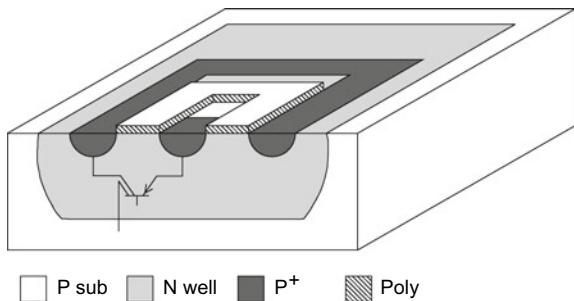


Fig. 2.40 Structure of a CMOS-integrated lateral PNP phototransistor with increased current gain [148]



The lateral bipolar transistor [147] being also available without process modification, however, can be freely connected. A typical lateral bipolar transistor usually suffers from a lower current gain and lower collector efficiency than the vertical bipolar device. In order to achieve a higher responsivity as an identically sized vertical bipolar phototransistor, modifications have been made to the typical lateral bipolar transistor [148]. The structure of this improved lateral bipolar phototransistor (LBPT) is shown in Fig. 2.40.

The lateral PNP phototransistor in a rectangular structure is formed with a P⁺ emitter surrounded by a P⁺ collector situated in an N-well base. The rectangular structure with the emitter in the center allows the optimum exploitation of the emitter efficiency. Because the base region is more lightly doped than the collector, the collector-base depletion region extends almost completely into the base. This space-charge region must not reach the emitter in order to avoid reach-through between emitter and collector. The base, therefore, has to be made wide enough. The current gain β , therefore, is rather low since β decreases when the base width W_B increases [148]:

$$\beta \approx \frac{1}{(W_B^2/2\tau_B D_N) + (D_P W_B N_A / D_N L_P N_D)}. \quad (2.4)$$

In this equation, τ_B is the minority carrier lifetime in the base, D_N and D_P are the carrier diffusion coefficients in the base, L_P is the diffusion length of holes in the emitter, and N_A and N_D are the acceptor and donor densities in the emitter and base, respectively. In [148], therefore, a trick [149] has been used in order to increase the current gain β . For this purpose, a polysilicon ring around the emitter is implemented (see Fig. 2.40) in order to set the base width. By connecting the polysilicon gate to the most positive potential in the circuit, majority carriers in the base accumulate directly under the gate, retarding the widening of the collector-base depletion region and setting the base width to that of the minimum polysilicon gate width.

It should be mentioned that the lateral phototransistor of Fig. 2.40 also contains a parasitic vertical PNP transistor. The effect is a reduction of the collector efficiency of up to 40% [147, 149], i.e. up to 40% of the collector current is lost to the substrate. In order to achieve a 100% exploitation of the amplification of the LBPT, the photodetector current, therefore, has to be drawn from the emitter.

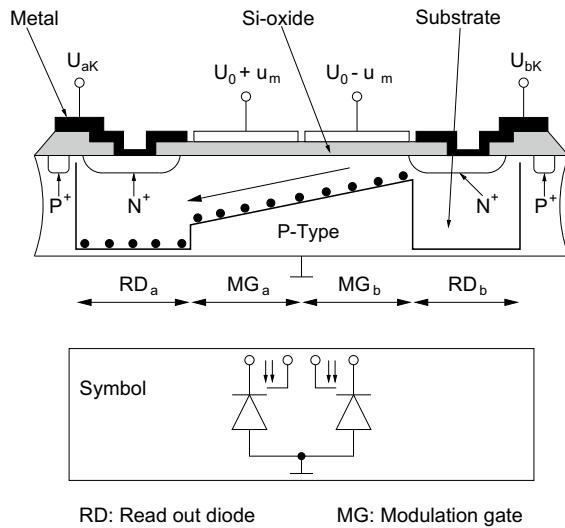
The base of the LBPT is left floating. Base bias current is provided when incident photons create electron–hole pairs. The photodetector current taken from the emitter is $(\beta + 1)$ times the base current, which would correspond to the photocurrent of a similar sized photodiode.

LBPT and VBPT devices with a size of $60 \times 60 \mu\text{m}^2$ were fabricated in a standard $2 \mu\text{m}$ digital CMOS process. An LED light source with a peak wavelength of 660 nm was used for the illumination of the devices and its illumination intensity was varied over four orders of magnitude. LBPT and VBPT output currents were approximately proportional to the light intensity. The LBPT output current was constantly about nine times greater than the VBPT output current. The output current of the LBPT was about $20 \mu\text{A}$ for an illumination intensity of 1 mW/cm^2 . For these values we can calculate a photoamplification of about 1040 compared to a photodiode of the same size. For an illumination intensity of $P' = 1 \text{ mW/cm}^2$ at 660 nm we obtain a photon flux density $\Phi = P'\lambda/(hc) = 3.33 \times 10^{15} \text{ cm}^{-2} \text{ s}^{-1}$. The photocurrent density of a photodiode $j_{\text{ph}}^{\text{PD}} = \Phi q$, therefore, is $5.33 \times 10^{-4} \text{ A/cm}^2$. For the area of $60 \times 60 \mu\text{m}^2$, $I_{\text{ph}}^{\text{PD}} = 19.2 \text{ nA}$ results. If we divide the measured LBPT photocurrent of $20 \mu\text{A}$ by this value, we obtain a photoamplification of 1040 for the LBPT.

LBPT devices also were fabricated in 1.2 and $0.8 \mu\text{m}$ CMOS processes. The active area of these devices scaled directly with the processes, i.e. the LBPT cell dimensions in the $1.2 \mu\text{m}$ process were $36 \mu\text{m}$ per side and $24 \mu\text{m}$ in the $0.8 \mu\text{m}$ process. The highest LBPT output current was observed for the CMOS process with the $1.2 \mu\text{m}$ design rules. However, no explanation was given for this finding.

The transient behavior of a photodetector determines how fast an array of photodetectors can be scanned in an image sensor. Due to charge storage, the fall time of a phototransistor is usually greater than the rise time [150]. The rise time, however, fortunately limits the scan speed of an image sensor. The fall time does not pose a problem as long as it is shorter than the time needed to scan the array. The worst-case scenario for the rise time is when a brightly illuminated cell is next to a dark cell. Step response of the LBPT with $W_B = 2 \mu\text{m}$ was measured by switching between dark and brightly illuminated cells in an array. In such a way, a rise time of $3.1 \mu\text{s}$

Fig. 2.41 Cross section and symbol of photonic mixer device [151]



RD: Read out diode MG: Modulation gate

was determined for the LBPT. In order to be complete, the dark current of the LBPT of less than 10 pA has to be mentioned.

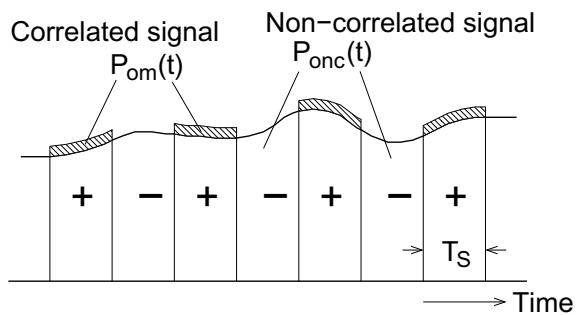
2.2.11 Photonic Mixer Device

An innovative optoelectronic device the so-called photonic mixer device (PMD) was suggested for optical distance measurement using a time-of-flight method with a pulsed laser signal [151]. This PMD is in principle a MOSFET with a split gate (Fig. 2.41). The light penetrates partially through the two polysilicon gates. The differential electrical modulation signal (u_m) derived from the laser modulation signal is applied to the gates. In dependence on the polarity of u_m , the photocurrent is directed to the readout electrode aK or bK . The PMD therefore operates like a seesaw for photocharges [151].

In the case of square-wave modulation the correlated measured light $p_{om}(t)$ (see Fig. 2.42) is usually superimposed by a much brighter background light $p_{onc}(t)$. The intensity change of the background light, however, is slow in practice and $p_{om}(t)$ is correlated with the modulation signal.

In this example (Fig. 2.41) the total modulated photocurrent drifts to the left readout electrode during the complete half period and the correlation function $\Delta U_{abm} = U_{aK} - U_{bK}$ reaches its maximum. Usually there is a phase shift (for not too large distances) between received photo signal and u_m and the magnitude of the correlation function is proportional to the distance to be determined. It has to be mentioned that the output signals of the PMD are actually currents, which have to be integrated on two capacitors to obtain the voltage signals.

Fig. 2.42 Correlated balanced sampling [152]



In a distance measurement range from 80 to 230 cm, a standard deviation of 2 mm over 1 hour of observation time was reported [152]. Newest work verified a distance error less than 1 mm corresponding to a time uncertainty (jitter) of 6.6 ps [152]. Modulation frequencies up to several 10s of MHz were applied.

The PIN photodiode technology ($0.6\text{ }\mu\text{m}$ (Bi)CMOS) was used to improve the photonic mixer device with the so-called double-cathode photodetector [153]. A fill factor of 67% was achieved. The measurement range reached up to 6.2 m. The distance standard deviation was 1 cm at a distance of 3.4 m with an optical emitter power of 1.2 mW at 650 nm. A responsivity of 0.24 A/W, a separation efficiency of 50%, and a bandwidth of 90 MHz for a wavelength of 660 nm were measured for this detector [154]. The separation efficiency was later improved to 80% for 660 nm and to 62% for 850 nm by adding a current carrying polysilicon gate [155]. Finally with buried cathode fingers the best results were achieved: a responsivity of 0.47 A/W, a separation efficiency of up to 67%, and bandwidths up to 300 MHz for 660 nm [156].

A photonic mixer device was also reported in [157] for use in the Microsoft Kinect for XBOX ONE. It was implemented in $0.13\text{ }\mu\text{m}$ CMOS and achieved a responsivity of 0.14 A/W at 860 nm and a modulation contrast of 67% at 50 MHz (56.5% at 130 MHz). Each pixel had a size of $10 \times 10\text{ }\mu\text{m}^2$ with a fill factor of 31% (without micro lens) and 60% with micro lens.

2.2.12 Avalanche Photodiodes

Thin Avalanche Photodiodes

There are many publications on integrated avalanche photodiodes (APDs) consisting of p^+ /n-well or p^+ /deep-n-well junctions with thin multiplication zone acting also as absorption zone. Carriers being photogenerated below the (deep) n-well do not contribute to the avalanche process. These thin APDs achieve high bandwidths up into the several GHz region as e.g. [158–163]. However their responsivity is rather limited at 850 nm (0.7 A/W and bandwidth 3.1 GHz [158], 1.46 A/W and 8.7 GHz [159], maximum 10 A/W and 3.2 GHz [160], 0.3 A/W and 6.3 GHz [161]) due to

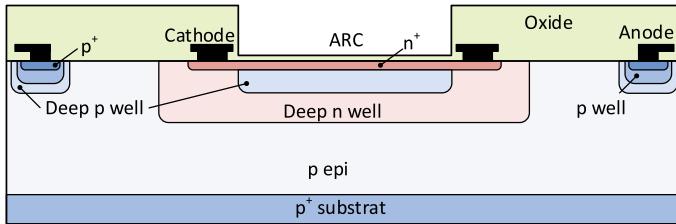


Fig. 2.43 Cross section of HV CMOS APD [165]

the thin absorption region although some high avalanche gains were reported as e.g. in [163]. In [162] responsivities of 2.04 A/W at 520 nm, 0.49 A/W at 660 nm, and 0.84 A/W at 850 nm were reported, whereby at 660 nm a bandwidth of 1.8 GHz was achieved. In [164] a lateral APD in SOI showed a responsivity of 1.42 A/W and a bandwidth of 10 GHz at 850 nm wavelength and 6.75 V reverse voltage.

Thick Avalanche Photodiodes

Avalanche photodiodes having an absorption region being much thicker than the multiplication region are described in this sub-section. A $0.35\text{ }\mu\text{m}$ high-voltage CMOS process was used to realize the avalanche photodiode shown in Fig. 2.43. The multiplication region is at the n^+ /deep-p-well junction. To avoid edge breakdown the deep-p-well is smaller than the n^+ cathode. The deep-n-well is used to compensate the deep-p-well's and the p epi doping partially to expand the space-charge region through the deep wells and the p epitaxial layer down to the p^+ substrate [165]. In such a way a thick absorption zone results and electrons photogenerated therein drift fast upwards into the multiplication zone. The breakdown voltage of this APD was 68.25 V compared to an isolation capability of this high-voltage CMOS process of 100 V.

The antireflection coating enabled a low-field (avalanche gain $M = 1$) responsivity of 0.41 A/W. The maximum responsivity for an avalanche multiplication factor $M = 6.6 \times 10^4$ was 2.7×10^4 A/W for an optical power of 5 nW at 670 nm. Both for 500 nW and 5 μ W optical power a maximum bandwidth of 850 MHz was measured for a multiplication gain of 50. The responsivity-bandwidth product was 17.4 GHz·A/W [165]. The ratio of the ionisation coefficients k of this HV CMOS APD was determined as 0.104 [166]. The excess noise factor F was 13.2 for an avalanche gain $M = 110$.

The $0.35\text{ }\mu\text{m}$ pin-photodiode CMOS technology offering also a bipolar transistor and described in [66] (see also Fig. 2.28) was used to realize an APD [167, 168]. To obtain this goal the p-well was inserted to increase the electric field strength above the critical value for impact ionisation. The cross section of this device is shown in Fig. 2.44. The breakdown voltage of this device was 35.25 V for a dark current of 10 μ A. A low-doped p^- epitaxial layer with a thickness of about $12\text{ }\mu\text{m}$ is used as thick absorption zone as in so-called discrete reach-through APDs. The p-well of this CMOS process allows full depletion of the absorption zone at rather low voltages

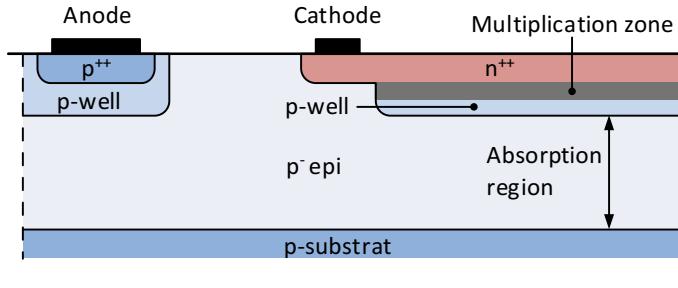
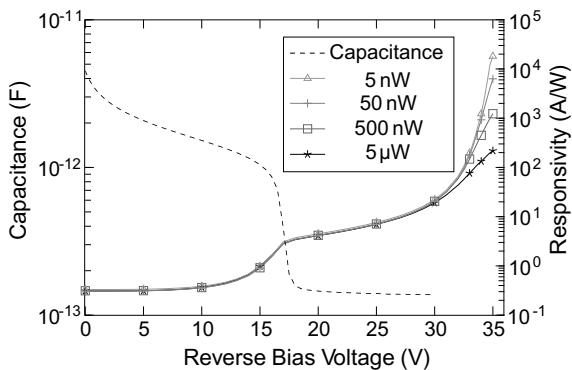


Fig. 2.44 Cross section of APD in pin-photodiode CMOS technology [168]

Fig. 2.45 Capacitance and responsivity of pin-APD



(see Fig. 2.45). At about 17 V the p-well is fully depleted and the space-charge region reaches into the low doped epitaxial layer as can be seen from the dependence of the capacitance on the reverse bias voltage. Electrons photogenerated in this thick absorption zone drift fast upwards into the multiplication zone and exploit the full thickness of this multiplication zone for impact ionisation. This thick absorption zone therefore allows a higher responsivity for red and near infrared light than that of thin (substrate isolated) APDs described above.

The responsivity of this PIN-APD is also shown in Fig. 2.45 for four different optical powers at 670 nm. Up to about 30 V reverse voltage the responsivity does not depend on the optical power. At higher reverse voltage, the photogenerated and multiplied electron-hole pairs screen the electric field, the impact ionisation decreases and the multiplication factor decreases for increasing optical power. At 35 V reverse voltage the responsivity was 18,000 A/V at 5 nW optical power [168]. At 30 V reverse voltage, the maximum bandwidth was 1.02 GHz for 5 μ W optical power and the responsivity was 19 A/W (corresponding to an avalanche gain of 61.4).

It was verified that modulation doping can increase the bandwidths of APDs in standard CMOS, where the epitaxial layer had a doping level of about 10^{15} cm^{-3} [169]. Reducing the effective p-well doping from 100 to 50% increased the bandwidth at 675 nm from 8 MHz to 386 MHz at the expense of a larger breakdown voltage.

In high-voltage CMOS the bandwidth of the APD was increased from 850 MHz to 1.02 GHz and to 1.25 GHz (M was 50 for these three cases) when the effective doping was reduced from 100 to 90% and 75%, respectively [170]. The breakdown voltage increased from 68.25 to 83.5 V and 119.25 V, respectively. Finally, the bandwidth of the pin-photodiode CMOS based APD was increased by modulation doping of 83% of the p-well to 2.3 GHz at $M = 20$ with a reverse voltage of 47.5 V [171].

A technique to measure the excess noise factor of APDs was described in [172] and these three APDs (all in 0.35 μm CMOS technologies) were compared. For an avalanche gain $M = 40$, the HV CMOS APD's excess noise factor was approximately 5, that of the pin-photodiode CMOS APD was about 4.5 to 6 depending on the incident optical power, and that of the 83%-modulation-doped pin CMOS APD was approximately 17.5. For $M = 50$, the HV CMOS APD's excess noise factor was approximately 6, that of the pin-photodiode CMOS APD was approximately 5 to 8 depending on the incident optical power, and that of the 83%-modulation-doped pin CMOS APD was approximately 23 [172]. The excess noise factors of the HV CMOS APD and of the not-modulation doped pin CMOS APD were comparable at these avalanche gains. The modulation doped pin CMOS APD's excess noise factor was clearly larger because of the low thermal budget of the 0.35 μm pin-photodiode CMOS process, which was basically a standard mixed-signal CMOS process.

Because of the precise measurement technique, the ionisation coefficients ratio k of the HV CMOS APD was determined more accurately than in [166]. The better value is 0.0849 instead of 0.104. Nevertheless, APDs integrated in CMOS chips cannot achieve the good excess noise behavior of discrete APDs fabricated in special and optimized processes.

2.2.13 Single-Photon Avalanche Diodes

Many thin, substrate isolated, single-photon avalanche diodes (SPADs) using a p⁺/n-well or p⁺/deep-n-well structure were described in the literature as e.g. in [173–176]. In these structures the multiplication zone acts also as absorption zone, which is thin due to the rather shallow n-wells or deep n-wells. Charge carriers photogenerated in the p substrate below the (deep) n-well cannot contribute to the multiplication process and their photon detection probability (PDP) for red and especially near infrared (NIR) light is rather low. A thicker multiplication zone, however still limited by the thickness of the deep n-well in 0.18 μm CMOS, led to a PDP of 43% for 600 nm with a dark count rate of 1.5 cps/ μm^2 and an afterpulsing probability (APP) of 7.2% for 300 ns dead time [177]. 3D-integration and backside-illumination of an SPAD were introduced [178] and a PDP of 29.5% at 660 nm as well as about 7% at 850 nm at 4.4 V excess bias were reported.

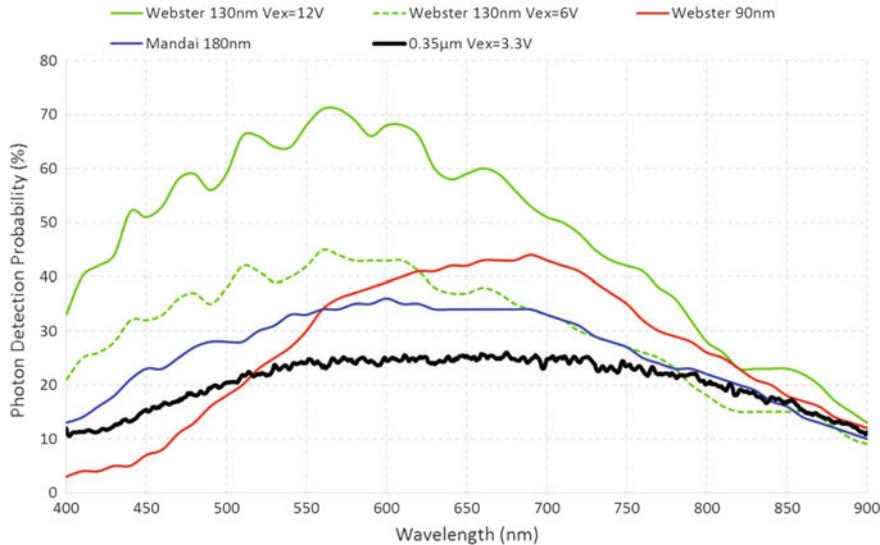


Fig. 2.46 Comparison of spectral PDP for some SPADs (Webster 130 nm: [180], Webster 90 nm: [181], Mandai 180 nm: [182]) and 0.35 μm HV-CMOS SPAD

The avalanche photodiode integrated in 0.35 μm high-voltage CMOS and shown in Fig. 2.43 was operated in the Geiger mode as a SPAD and the results were reported in [179]. The photon detection probability was 22.1% at 785 nm and at an excess voltage of 3.5 V. For the same excess bias the dark count rate was 46 kHz and the afterpulsing probability at a dead time of 35 ns was 3.4% for a diameter of 86 μm of the SPAD's active area. Figure 2.46 compares the spectral PDP of the SPAD with the structure shown in Fig. 2.43 to the spectral PDPs of some SPADs reported in literature. This HV-CMOS SPAD reaches the same PDP for 850 nm already at 3.3 V excess bias, whereas the SPAD of [180] needs an excess bias of 6 V.

A thick epitaxial SPAD with a PDE of 62.2 to 64.8% for 610 nm at an excess bias voltage of 5 V was reported [183, 184], however, the so-called n-SPAD and p-SPAD regions in a proprietary customized CMOS process were not described.

The pin-photodiode CMOS technology described in Fig. 2.28 was used to realize a SPAD having the same multiplication and absorption zones as the APD of [168]. Without an antireflection coating, a PDP of 36.7% at 635 nm was measured for an excess bias of 6.6 V [185]. Figure 2.47 shows the spectral PDP of this pin-photodiode CMOS based SPAD in comparison to that of some SPADs described in the literature. The pin-SPAD shows the same or even better PDPs for wavelengths longer than 800 nm already at an excess bias of 6.6 V compared to the SPAD of [180] at an excess bias of 12 V.

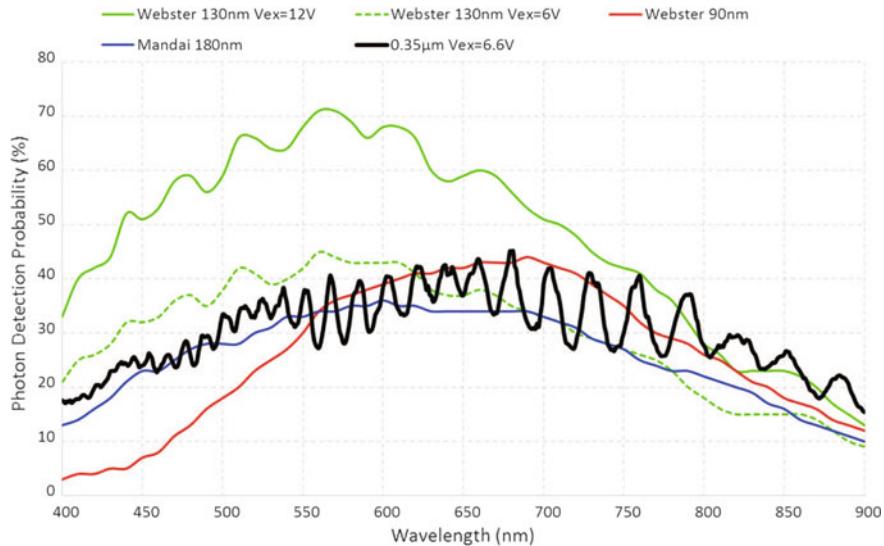


Fig. 2.47 Comparison of spectral PDP for some SPADs (Webster 130 nm: [180], Webster 90 nm: [181], Mandai 180 nm: [182]) and 0.35 μm pin-CMOS SPAD

2.3 BiCMOS-Integrated Detectors

2.3.1 BiCMOS Processes

BiCMOS stands for Bipolar&CMOS. It combines both bipolar transistors and NMOS as well as PMOS transistors in the same chip. In digital BiCMOS circuits it is possible to exploit the advantages of bipolar transistors and of MOS transistors. The capabilities of BiCMOS circuits, therefore, exceed those that are obtained when only one of the device types is used. For example, CMOS allows low-power, high-density digital ICs, which, however, are slower than bipolar ECL-based ICs due to the poor driver capability of MOS transistors, especially when large capacitive loads are encountered. Such loads occur at long interconnects on chip, at high fan-out circuits, as well as at chip outputs. The driver capability of bipolar transistors can be used to advantage in BiCMOS circuits to charge such heavy loads rapidly. Bipolar digital circuits implemented with ECL gates can also operate with small logic swings and high noise immunity. ECL gates, however, exhibit high power consumption, poor density, and limited circuit options. BiCMOS offers the benefits of both bipolar and CMOS circuits by appropriately trading off the characteristics of each technology.

BiCMOS can also offer analog and digital functions on the same chip. For instance, better device matching, lower offset voltages of operational amplifiers, and enhanced bandwidths compared to analog CMOS circuits can be obtained with analog bipolar sub-circuits in BiCMOS ICs or with BiCMOS circuits. From CMOS, the high input

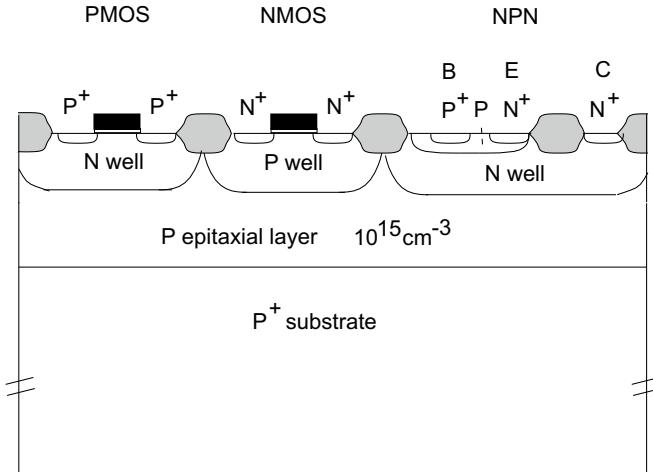


Fig. 2.48 Cross section of a triple-diffused BiCMOS structure [61, 187]

resistance, i.e. the zero input bias current, can be used advantageously in BiCMOS circuits. BiCMOS circuits, therefore, pushed mixed analog/digital (mixed signal) applications tremendously.

The interested reader is recommended to read [186] to study the advantages of BiCMOS in more detail. The benefits of BiCMOS, however, are attained at the expense of a more difficult technology development and at the expense of more complex chip-manufacturing tasks leading to longer chip-fabrication times and higher costs.

BiCMOS processes can be derived from bipolar and CMOS processes. The simplest low-cost BiCMOS process is obtained adding one mask for the P base of the NPN device to a well established CMOS process (Fig. 2.48). The added mask is used to selectively produce lightly doped P regions with a doping level of about 10^{17} cm^{-3} . The N-well fabrication step also forms the collector regions of the NPN transistors. The heavy NMOS source/drain implant is employed to produce the emitter regions and collector contacts of the bipolar transistors. The PMOS source/drain implant is used to create the base contact, since this serves to lower the base series resistance R_B . The starting substrate is either a P-type wafer or a P-type epitaxial layer on a P^+ wafer. Such simple processes are called *triple-diffused (3-D)* BiCMOS processes, because they produce triple-diffused (C, B, E) bipolar transistor structures [186, 188]. In order to optimize both the CMOS and bipolar device characteristics independently, the doping profiles in the CMOS N well and in the bipolar N well have to be made different. The base-collector breakdown voltage and therefore the collector-emitter breakdown voltage of the NPN transistor may be rather small with the CMOS N well as the collector. In order to increase these breakdown voltages the doping concentration has to be reduced making a separate collector doping, i.e. a bipolar N well, necessary. The resulting cross section is shown in Fig. 2.49.

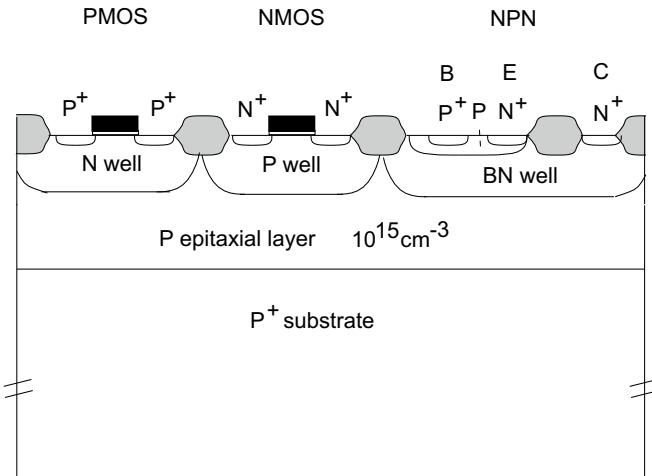


Fig. 2.49 Cross section of a 3-D BiCMOS structure with separately optimized CMOS and bipolar N wells

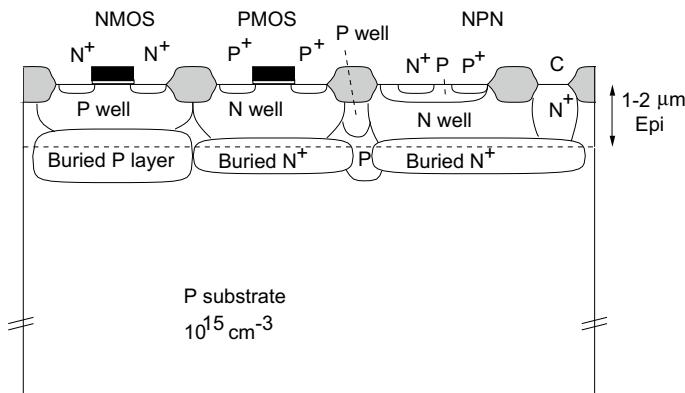


Fig. 2.50 Optimized high-performance BiCMOS structure

The main drawback of 3-D bipolar transistors is a large collector series resistance R_C . In order to improve the properties of the NPN transistors (e.g. current gain β and transit frequency f_T), polysilicon emitters allowing a thinner base were added to a 3-D BiCMOS process in [189], of course increasing the process complexity.

The most widely used high-performance BiCMOS technology is based on a twin-well CMOS process. Figure 2.50 shows the cross section of such a high-performance BiCMOS structure [187, 190]. N^+ buried layers are used to reduce the collector series resistance. These N^+ buried layers and the P buried layers also reduce the susceptibility to latch-up in the CMOS part of the BiCMOS ICs.

Four masking steps were added to an advanced $0.8\text{ }\mu\text{m}$ 12-mask CMOS process described in [61] to integrate high-performance bipolar transistors. The starting material is a lightly doped ($\approx 10\text{ }\Omega\text{cm}$) silicon wafer with a $<100>$ orientation. At the beginning of the process, a mask has to be added to pattern the N^+ buried layers (see Fig. 2.51a). Next, a selective boron implant is performed, which places an additional P-type dopant between the N^+ buried layers (see Fig. 2.51b), to reduce the minimum buried layer distance. This boron implant also creates the P-type buried layers. This self-aligned approach requiring only one mask to create both the N^+ - and P-buried layers is widely used [186]. After the removal of all oxides, a thin ($1.0\text{--}1.5\text{ }\mu\text{m}$), near-intrinsic (less than 10^{15} cm^{-3}) epitaxial layer is then deposited (see Fig. 2.51c). The steps for twin-well formation are conducted next (compare Fig. 2.19a and b). A single-mask process can be used to form both the N well and the P well. A dual-phosphorus implant (deep and shallow) is used to form the N well (Fig. 2.51d). A boron implant is used to form the P well (Fig. 2.51e). Following the implantations that introduce the well dopants, the well drive-in is performed. Then the active regions are defined (see Fig. 2.51f and compare with Fig. 2.19d). The boron channel stop is implanted next and the field oxide is grown.

At this stage, the second mask is added for the formation of the deep N^+ -collector contact (Fig. 2.51g). A deep phosphorus implant and a subsequent drive-in/anneal step are applied to form the deep-collector-contact structure. The third added mask (Fig. 2.51h) is used for the patterning of the P base, which is implanted by boron and annealed subsequently.

The fourth added mask is needed to open the areas for the polysilicon emitters (Fig. 2.51i). This process is rather complex and the interested reader will find a thorough description in [186]. The polysilicon on top of the emitters is patterned together with the polysilicon gate definition (Fig. 2.51j). From this stage on, processing (Figs. 2.51k–n) is identical to the CMOS process, from which the BiCMOS process was derived.

In order to achieve transit frequencies of the order of 10 GHz for the NPN transistors, the epitaxial N collector has a thickness of only about $1\text{--}2\text{ }\mu\text{m}$ [190–195]. In a $0.8\text{ }\mu\text{m}$ BiCMOS process, an epitaxial layer with a thickness of only $0.8\text{ }\mu\text{m}$ was used [196]. In this process, different from Fig. 2.51a, As instead of Sb was used for the buried collector and due to the thin epitaxial layer, autodoping caused by the N^+ As buried collectors during epitaxy had to be avoided. For this purpose, the pressure in the epitaxial dichlorosilane process was reduced to 25 Torr and a special temperature ramp starting at 850°C and increasing the temperature to 1150°C within 10 min resulted after 1 min at 1150°C in an intrinsic — i.e. intentionally undoped — epitaxial layer thickness of $0.15\text{ }\mu\text{m}$. The main epitaxial cycle was carried out at 860°C for approximately 18 min where the epitaxial layer was grown to a thickness of $0.8\text{ }\mu\text{m}$. The transit frequency of the NPN transistor was 11.5 GHz. A $0.5\text{ }\mu\text{m}$ BiCMOS process, for instance, is described in [197].

Fig. 2.51 Process flow of an optimized high-performance BiCMOS process [186]

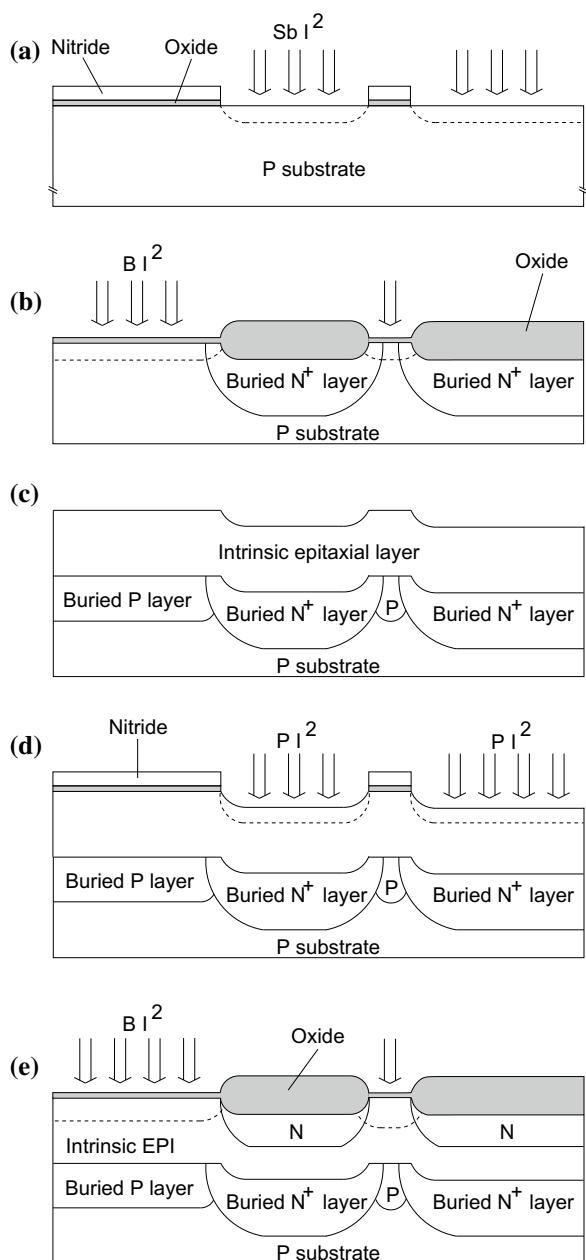


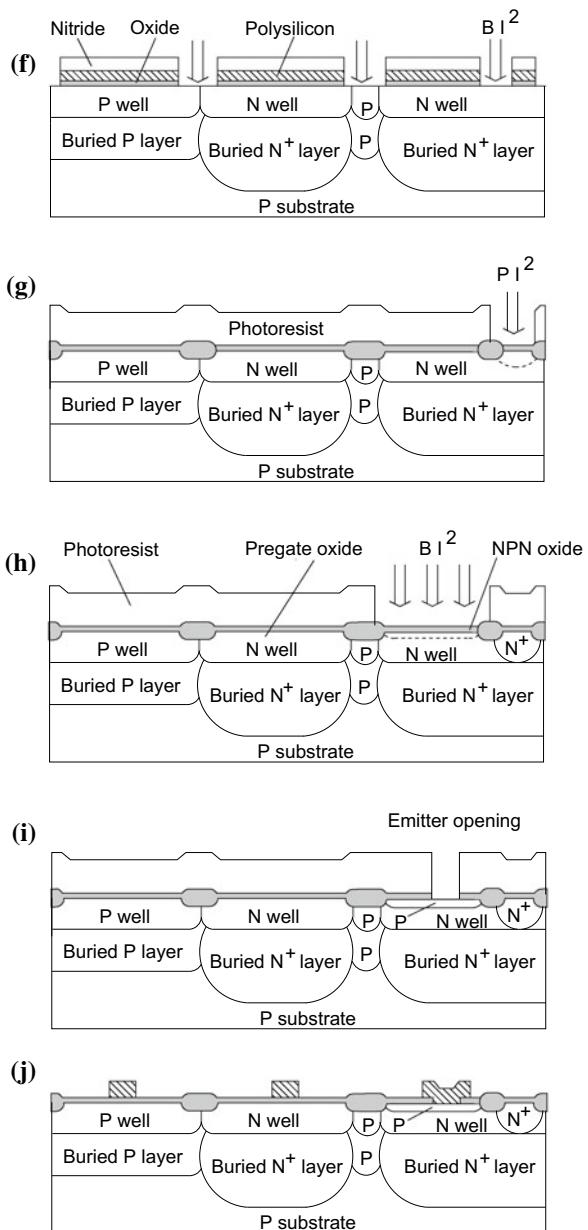
Fig. 2.51 (continued)

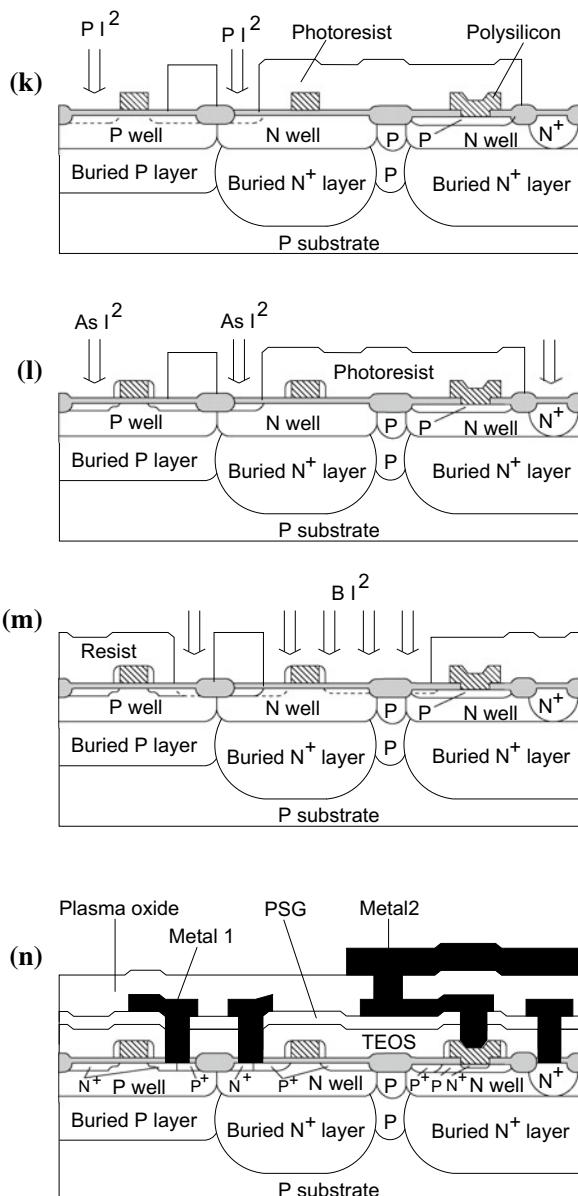
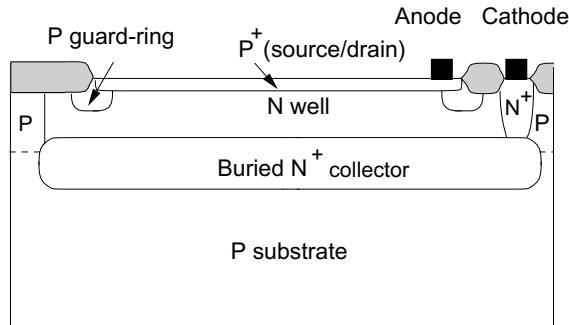
Fig. 2.51 (continued)

Fig. 2.52 PIN photodiode in a SBC-based BiCMOS technology [198]



2.3.2 BiCMOS-Integrated Photodiodes

BiCMOS circuits enable the use of photodetectors described in Sects. 2.1 and 2.2. We, therefore, have to discuss only a few photodetectors here. BiCMOS-OEICs have already been introduced [198, 199]. The OEICs in both cases consisted of a PIN photodiode and an amplifier, which exploited only MOSFETs and no bipolar transistors. The BiCMOS technology, therefore, was chosen merely for the integration of the PIN photodiode. A standard BiCMOS technology with a minimum effective channel length of $0.45\text{ }\mu\text{m}$ without any modifications was used [198, 199]. This effective channel length corresponds to a drawn or nominal channel length of about $0.6\text{ }\mu\text{m}$. The buried N^+ -collector in Fig. 2.52 was used for the cathode of the PIN photodiode. The P^+ -source/drain island served for the anode. The intrinsic zone of the PIN photodiode was formed by the N well and, therefore, had only a thickness of $0.7\text{ }\mu\text{m}$. Consequently, the responsivity of the photodiode was only 0.07 A/W for a wavelength of 850 nm [198]. For a bias of 2.5 V across the $75 \times 75\text{ }\mu\text{m}^2$ PIN photodiode with a capacitance of 1.8 pF , a -3 dB bandwidth of 700 MHz was reported. The OEIC reached a bit rate of 531 Mb/s with a bit error rate of 10^{-9} and a sensitivity of -14.8 dBm . This bit rate was limited by the capacitance of the photodiode and the feedback resistor of $1.4\text{ k}\Omega$ in the amplifier transimpedance input stage. The dark current of the photodiode was 10 nA for a reverse voltage of 2.5 V at room temperature.

In [199] a laser with a wavelength of 670 nm was used for the characterization of the same OEIC as in [198]. The data rate was increased to 622 Mb/s for this wavelength. No measured result for the responsivity was given in [199]. Instead, a three times larger responsivity value of approximately 0.2 A/W for $\lambda = 670\text{ nm}$ was estimated due to the lower penetration depth than for $\lambda = 850\text{ nm}$. This estimation, however, may be doubtful, because possible destructive interference in the isolation and passivation stack is neglected. The main drawback for the photodiode used in [198, 199] was its low responsivity due to the thin epitaxial layer in the SBC-based BiCMOS process.

In the following we will investigate an N^+/P -substrate photodiode in a CMOS-based BiCMOS technology. Figure 2.53 shows the cross section of this photodiode.

Fig. 2.53 Cross section of a N⁺/P-substrate photodiode in self-adjusting well BiCMOS technology

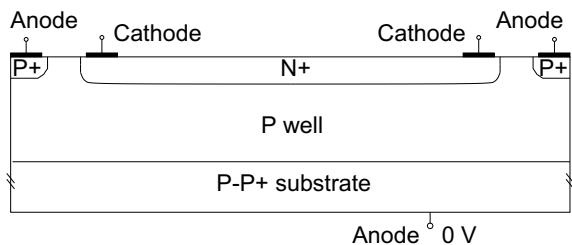
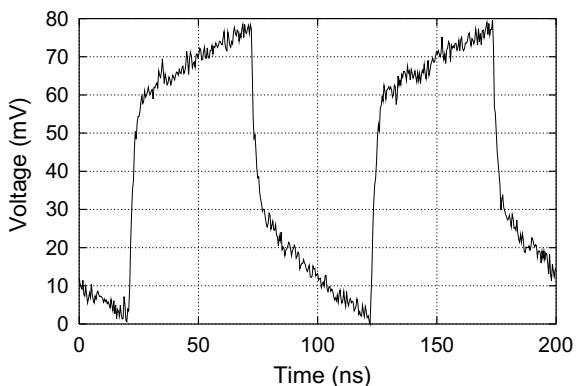


Fig. 2.54 Transient response of a N⁺/P-substrate photodiode in a self-adjusting well BiCMOS technology



The process used for the fabrication of this photodiode is optimized with respect to a minimum number of masks and implements self-aligned wells. Therefore, there is a P well incorporated in the N⁺/P-substrate photodiode. This leads to a thin N⁺/P-substrate space-charge region and the effect of slow carrier diffusion is very pronounced (see Fig. 2.54). Rise and fall times of 26 and 28 ns, respectively, are determined due to the pronounced diffusion tail. The measured -3 dB bandwidth is 6.7 MHz.

Another example for a photodetector in a standard BiCMOS technology will be added here. In a CMOS based (3-D) BiCMOS process, an N well can be used as the collector of a bipolar NPN transistor. This N well can also be used in order to form the cathode of a so-called double photodiode (DPD). Figure 2.55 shows the cross section of such a DPD. The two anodes are connected to ground. The cathode is connected to the amplifier in the OEIC (see Fig. 6.73). Two PN junctions are vertically arranged. The N-well/P-substrate junction minimizes the effect of slow diffusion of photogenerated carriers from the substrate.

In addition to the two space-charge regions at the two vertically arranged PN junctions, an electric field is also present between the two space-charge regions (see Fig. 2.56) due to the doping gradient of the N well. Therefore, there is no contribution of slow carrier diffusion from the region between the two space-charge regions.

Fig. 2.55 Cross section of a double photodiode in BiCMOS technology [200]

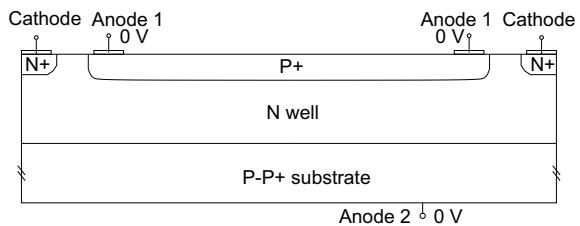


Fig. 2.56 Electric field in a double photodiode [47]

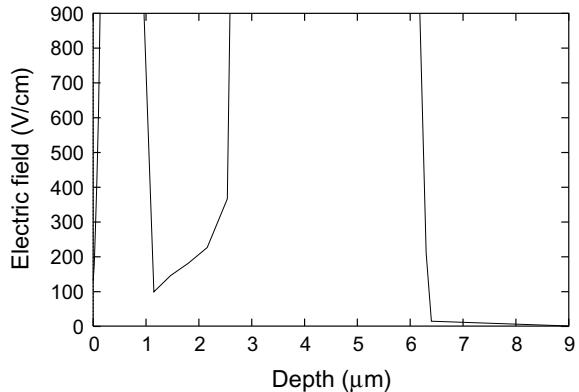
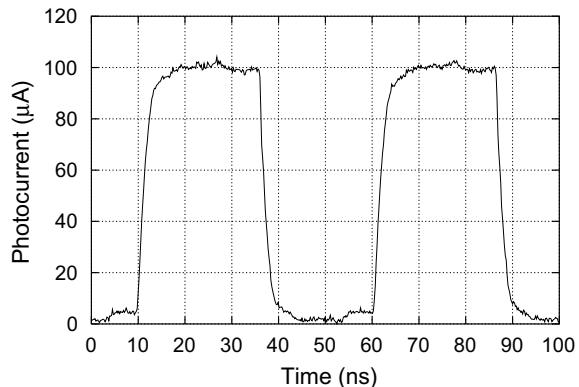


Fig. 2.57 Transient response of the double photodiode in BiCMOS technology shown in Fig. 2.55 [201]



With an integrated polysilicon resistor of $1\text{ k}\Omega$, rise and fall times of 3.2 and 2.8 ns, respectively, were measured for the DPD with $\lambda = 638\text{ nm}$ and $U_r = 2.5\text{ V}$ [201]. There is no indication of a so-called diffusion tail in the photocurrent (Fig. 2.57).

The transient response of such a DPD is compared to that of a PIN photodiode with a P⁺ anode at the surface from Sect. 2.2.6 in Fig. 2.58. The PIN photodiode possesses shorter rise and fall times. Furthermore, the behavior of a DPD with a CMOS N well is compared to that of a DPD with a bipolar N well. The DPD with the bipolar N well shows shorter rise and fall times because the doping concentration in

Fig. 2.58 Comparison of the transient response of double photodiodes with a bipolar N well and with a CMOS N well to that of a PIN-photodiode with $C_e = 5 \times 10^{13} \text{ cm}^{-3}$ ($\lambda = 638 \text{ nm}$, $U_r = 2.5 \text{ V}$)

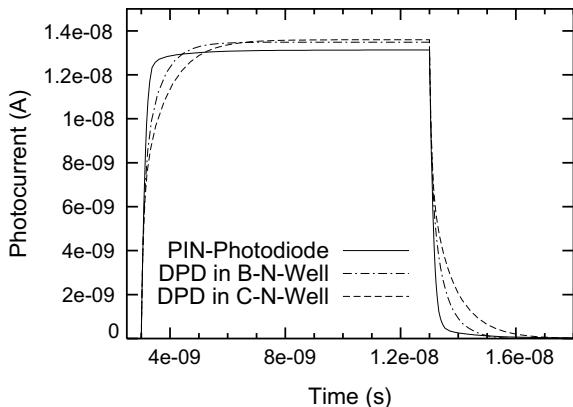
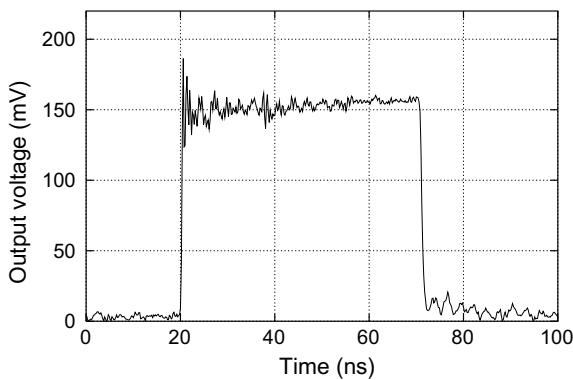


Fig. 2.59 Transient response of the double photodiode in BiCMOS technology with an area of $530 \mu\text{m}^2$ [47]

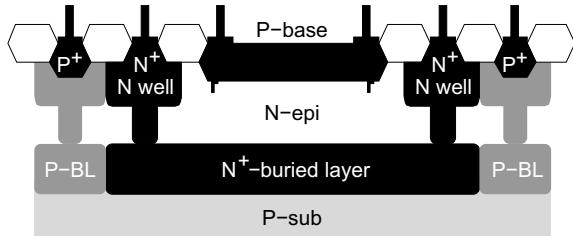


this well is lower than in the CMOS N well and the P⁺/N-well space-charge region is thicker in the DPD with the bipolar N well.

With an integrated polysilicon resistor of 500Ω , rise and fall times of 1.8 and 1.9 ns, respectively, and a -3 dB bandwidth of 156 MHz were measured for the DPD with $\lambda = 638 \text{ nm}$ and $U_r = 2.5 \text{ V}$ [200]. Later a bandwidth of 220 MHz was measured for an OEIC with a DPD of the size $50 \times 50 \mu\text{m}^2$ and with a simple transimpedance bipolar amplifier representing a low input impedance for the photocurrent of the DPD [202], leading to the conclusion that the rise and fall times of 1.8 and 1.9 ns as well as the bandwidth of 156 MHz were limited by the RC constant of load resistor and DPD capacitance.

For a DPD with the area of $23 \times 23 \mu\text{m}^2$, finally rise and fall times of less than 0.37 and 0.70 ns, respectively, and a bandwidth of 367 MHz were determined in [47], where an OEIC with this smaller DPD and with a transimpedance bipolar amplifier has been investigated. The transient response of this OEIC with the small DPD is shown in Fig. 2.59. The faster speed of the smaller DPD can be explained with a lower series resistance in the N well of the DPD and with a lower space-charge capacitance due to its smaller size in addition to the low input impedance

Fig. 2.60 Double photodiode in a SBC-based BiCMOS technology with a P-base anode [205]



of the transimpedance amplifier. The values of 0.37 and 0.70 ns for the rise and fall times of the DPD determined in [47], therefore, better characterize the intrinsic speed of the DPD. With the conservative estimate a non-return-to-zero data rate $DR = 2/(3(t_r + t_f)) \geq 620 \text{ Mb/s}$ could be derived for the DPD [47].

Fast optoelectronic integrated circuits have been successfully realized by implementing the double photodiode [203, 204] in an industrial 0.8 μm BiCMOS process without any modifications. The main benefit of this photodiode is a very high bandwidth of about 230 MHz for a light sensitive area of $2700 \mu\text{m}^2$. However, the capacitance of a DPD with an area of $2700 \mu\text{m}^2$ is 876 fF at a reverse bias of 3.3 V, which is a drawback if large photodiodes are required.

Instead of the source/drain area of the PMOS transistor in a BiCMOS technology, the P-base of the NPN transistor can be used for the anode of a PIN photodiode with a thin I-layer (see Fig. 2.60). The N-epitaxial layer and the N⁺-buried layer can be used instead of the N well. Connecting the P-base anode and the substrate contacts leads to a parallel circuit of the P-base/N-epi/N⁺-buried layer PIN photodiode (UPD) and the N⁺-buried-layer/P-substrate photodiode (LPD). The P-base layer simultaneously can be used to shield the N⁺-buried-layer/P-substrate photodiode against electric fields perpendicular to the photodiode surface. This photodiode is a double photodiode. Such a photodiode in a 0.6 μm BiCMOS technology was investigated in [205]. A responsivity of 0.4 A/W was observed for $\lambda = 780 \text{ nm}$. This rather high value was due to the N⁺/P-substrate junction in a depths of about 5 μm [205]. It should be noted that a responsivity measurement is a DC measurement. Therefore, a contribution of diffusing carriers from the substrate may have been present leading to such a high responsivity. Accordingly, the dynamic quantum efficiency may be lower than would correspond to this responsivity value.

Rise and fall times of 4–5 ns were reported for a similar double photodiode with a P⁺-source/drain anode instead of the P-base anode for $\lambda = 780 \text{ nm}$ [206]. This is a quite fast response for a photodiode in standard BiCMOS technology with a responsivity of about 0.5 A/W at this rather long wavelength [206]. Rise and fall times of 0.13 ns were observed for the upper photodiode (UPD) for $\lambda = 660 \text{ nm}$ [206]. For $\lambda = 780 \text{ nm}$ the rise and fall times of the UPD were 1.4 and 1.8 ns, respectively [206]. The responsivities of the UPD for these two wavelengths were 0.23 and 0.14 A/W, respectively. The lower photodiode (LPD) showed rise and fall times of 1.8 and 1.9 ns for $\lambda = 660 \text{ nm}$ [206]. For $\lambda = 780 \text{ nm}$ the rise and fall times

of the LPD were 7 and 10 ns, respectively. The responsivities of the LPD for these two wavelengths were 0.17 and 0.36 A/W, respectively.

Another photodiode which can be integrated in a BiCMOS process without any modifications is the N⁺/N-well/P-substrate photodiode with a capacitance of only 112 fF for the same area ($2700 \mu\text{m}^2$) as that of the DPD with a capacitance of 876 fF [207].

In Fig. 2.61 the cross section of the N⁺/N-well/P-substrate photodiode can be seen. The PN-junction is located between the N-well and the P-substrate. The depth of the pn-junction allows reliable operation at red laser light ($\lambda = 638 \text{ nm}$). The bandwidth of the N⁺/N-well/P-substrate photodiode for this wavelength is larger than 82 MHz [208]. In order to improve the quantum efficiency, the light sensitive area of the photodiode is covered by an antireflection coating (ARC) and the same quantum efficiency as for the DPD is achieved.

The bandwidth of OEICs for application in optical storage systems rapidly increased recently. Also the same OEIC should be appropriate for application in CD-ROM, DVD, and future DVD as well as DVR with different wavelengths being used (780, 650, and 400 nm) in order to save development effort and lower the prices due to higher production volumes of the same OEIC. A photodiode for such a universally applicable OEIC was introduced in [209].

The photodiode implemented in a $0.6 \mu\text{m}$ standard BiCMOS process is shown in Fig. 2.62. In order to avoid slow diffusion of photogenerated carriers from the substrate for 780 and 650 nm, the photodiode formed by the N-epitaxial layer and

Fig. 2.61 Cross section of the N⁺/N-well/P-substrate photodiode (ARC: anti-reflection coating, N⁺-cathode contact not drawn)

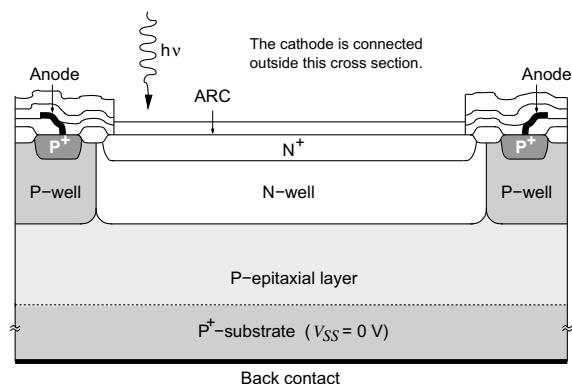
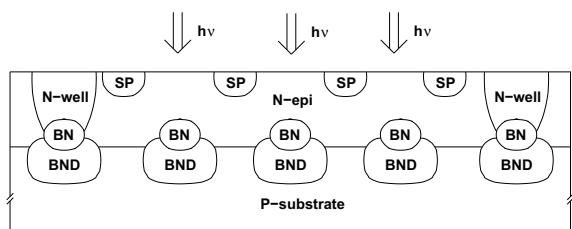


Fig. 2.62 Cross section of a shallow-P(SP)/N-epi/photodiode in standard BiCMOS technology [209]



the shallow P (SP) implant was used. The SP anode is interrupted, whereby the SP regions are connected electrically outside the light sensitive area. It is interrupted because of two reasons. First, the quantum efficiency for blue/UV light is higher than for a whole-area P-type region. Second, the junction capacitance is lower than for a whole-area P-type region in the epitaxial layer yielding an improved signal-to-noise ratio (SNR) of the OEIC for all three wavelengths. The N-epi cathode has a low-ohmic connection to the supply voltage V_{cc} via the buried-N (BN) and buried-N-deep (BND) as well as via the N-well regions. The vertical doping profile of the BN/BND doping generates an electric field that accelerates the photogenerated carriers. The BN and BND regions are interrupted (and connected outside the light sensitive area) to increase the accelerating electric field.

A capacitance of 0.25 pF and a bandwidth of 450 MHz were mentioned for the photodiodes used in channels A–D of the OEIC. The measured responsivity values of the interrupted-SP/N-epi photodiode were 0.079 A/W for 780 nm, 0.169 A/W for 653 nm, and 0.120 A/W for 402 nm [209]. The capacitance and bandwidth values are impressive results for this sophisticated photodiode. It should be mentioned, however, that the relatively low responsivity values finally limit the sensitivity of OEICs implementing this photodiode.

The integration of photodiodes in BiCMOS technology, for which process modifications are necessary, is similar to the integration of photodiodes in bipolar or CMOS technology. The integration of PIN photodiodes in optimized high-performance BiCMOS technologies (see Fig. 2.50) requires a similar additional process complexity as the integration of PIN photodiodes in bipolar technology (see Fig. 2.7). The N well can be used for the collector of the NPN transistor in the BiCMOS process. The third mask for the doping of the collector in Fig. 2.7, therefore, is not necessary for the PIN-BiCMOS integration in a process with a structure as in Fig. 2.50. Consequently, two additional masks are necessary for PIN-BiCMOS integration in such a structure.

In a 0.6 μm BiCMOS technology, the doping concentration of the N-type collector epitaxy was reduced to about 10^{14} cm^{-3} to increase the bandwidth of the pin photodiode [210]. As a starting material for the process, a p⁺ substrate with a thick low doped epitaxial layer (about 10^{13} cm^{-3}) was used. The –3 dB bandwidth of this PIN photodiode was 625 MHz for 670 nm and 238 MHz for 785 nm. The parameters of N-channel and P-channel MOSFETs as well as of the NPN transistor were not affected by the change of the substrate and the N-type collector epitaxy. The only consequence were increased reach-through currents between N-wells; which however can be handled by increased minimum N-well distances in the design rules.

A similar PIN photodiode as described in Fig. 2.7 was realized in a 0.5 μm BiCMOS process in the European project INSPIRED. A one-step epitaxial growth of the intrinsic layer having an N[–] doping of $5 \times 10^{13} \text{ cm}^{-3}$ with a thickness of 9.5 μm was done [211]. Figure 2.63 shows the cross section of an OEIC with this PIN photodiode. The cathode was implanted with arsenic, the N contacts of the PIN photodiode were implanted with phosphorus, and the P-type buried layer was implanted with boron before the epitaxial layer was grown. After epitaxial growth, a high-energy boron implantation was done to complete the re-doped P layer in order to reconstruct the P-type substrate doping concentration used originally for this BiCMOS process.

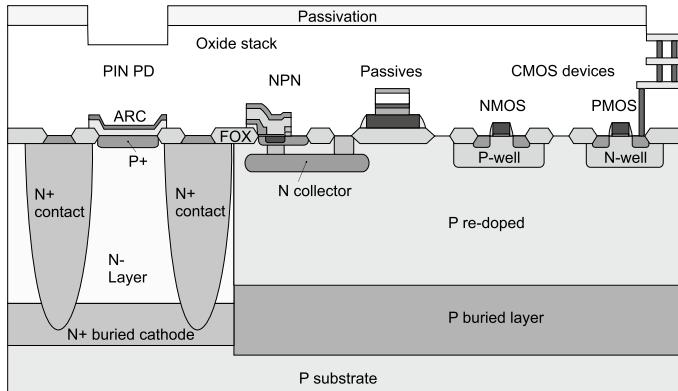


Fig. 2.63 Schematic cross section of $0.5\text{ }\mu\text{m}$ PIN BiCMOS OEIC [211]

A phosphorus implant for the contacts to the buried cathode with succeeding high-temperature diffusion basically finished the doping regions of the PIN photodiode. Due to an anti-reflection coating a quantum efficiency of 85% was reported for 660 nm wavelength.

The one-step epitaxy was possible because the buried collector of the NPN transistor was fabricated with high-energy implantation of phosphorus towards the end of the process. The NPN transistor achieved a transit frequency of 26 GHz and a current gain of 90.

According to the high breakdown voltage of the buried cathode to the substrate and to the P buried layer, the N^+ contacts of the PIN photodiode can be connected to positive voltages at least up to 17 V when the anode is connected to the input of the integrated amplifier. Such high reverse bias voltages of the PIN photodiode enhance the drift velocity. The -3 dB cut-off frequency in dependence on the reverse voltage across the PIN photodiode for two wavelengths is visible in Fig. 2.64. The -3 dB cut-off frequency increases from 1.1 GHz for 3 V reverse bias to 2.9 GHz for 17 V at 660 nm wavelength. At 850 nm light wavelength, the -3 dB cut-off frequency ranges from 300 MHz for 3 V to 2.1 GHz for 17 V thanks to the N^+ buried cathode being connected to the positive photodiode supply voltage and therefore keeping photogenerated charges diffusing from the substrate away from contributing to the photocurrent, which flows from the anode into the amplifier input.

The measured 10–90% rise and fall times in dependence on the reverse bias of the PIN photodiode can be seen in Figs. 2.65 and 2.66, respectively. At 4 V reverse voltage the rise and fall times are 400 and 600 ps, respectively, at 850 nm wavelength. At 660 nm wavelength and 4 V the rise and fall times are 149 and 210 ps, respectively. These values reduce to 200 and 400 ps as well as to 94 and 141 ps for 850 and 660 nm, respectively, at 17 V reverse voltage. These values are raw, measured data, i.e. they were not corrected concerning the rise and fall times of the laser sources used for the measurements. Therefore, the real rise and fall times of the pin photodiode are even shorter. It also should be mentioned that the electrons reached the saturation

Fig. 2.64 Cut-off frequencies of PIN photodiode in 0.5 μm BiCMOS technology [211]

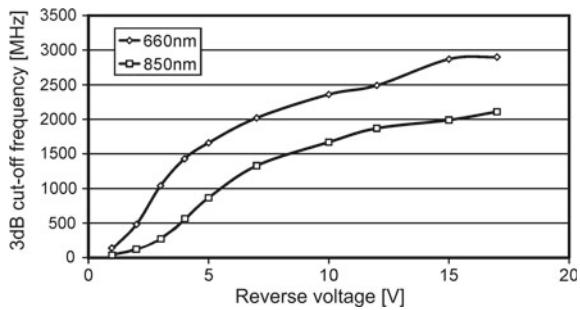


Fig. 2.65 Rise times of PIN photodiode in 0.5 μm BiCMOS technology [211]

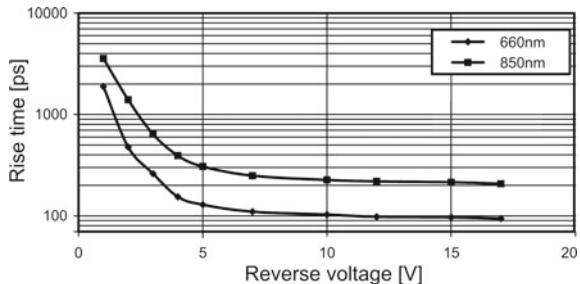
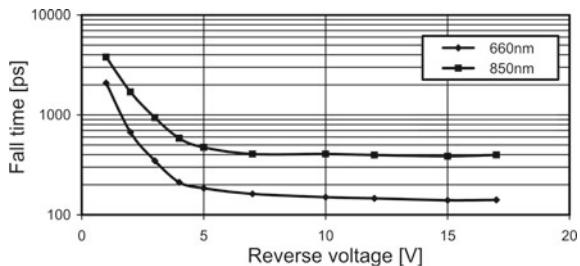


Fig. 2.66 Fall times of PIN photodiode in 0.5 μm BiCMOS technology [211]



drift velocity. The holes, however, were not yet reaching the saturation drift velocity in this pin photodiode at 17 V.

In the same 0.5 μm BiCMOS technology PIN finger photodiodes were investigated [212]. The finger structure reduced carrier recombination in the N⁺ cathode, what resulted in a responsivity of 0.25 A/W at 410 nm. These finger PIN photodiodes reached a -3 dB bandwidth of 2.0 GHz with 410 nm light and 2.2 GHz with 660 nm for a reverse voltage of 17 V.

Another PIN photodiode was integrated in a modular 0.35 μm CMOS process offering also a NPN-transistor process module [66]. Since the buried collector of the NPN transistor is formed in this process also by high-energy implantation and the P⁻/P⁺ epitaxial wafers can be bought from wafer suppliers, no epitaxy has to be done in this BiCMOS process. The cross section of this PIN photodiode is depicted

in Fig. 2.28 (The pin photodiode is the same, if the bipolar process module is added to this CMOS process.). The bandwidths for different wavelengths and reverse voltages are shown in Fig. 2.29.

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Chapter 3

Detectors in Thin Crystalline Silicon Films



Photodiodes in thin Silicon-on-Insulator (SOI) films represent a possibility to avoid slow carrier diffusion for achieving high-speed operation. CMOS circuits in Silicon-on-Sapphire (SOS) thin films allow easy hybrid integration of III/V laser diodes, since the sapphire substrate is transparent and the light can be emitted downwards through the SOS film and the sapphire substrate. Upward light emission is therefore not necessary and the III/V substrate of the VCSELs does not have to be removed. Polyimid bonding of III/V laser diodes and photodiodes on silicon as an interesting wafer-scale process also shall be described in this chapter.

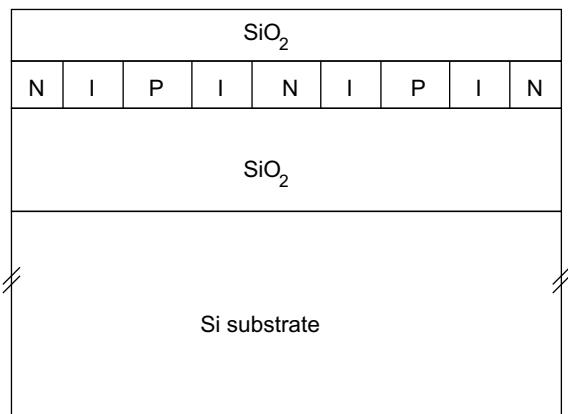
3.1 Photodiodes in Silicon-on-Insulator

Silicon-on-Insulator (SOI) has been investigated mainly as a material for CMOS technology as a substitute for bulk silicon [1]. The main advantages of thin-film SOI for CMOS are: (i) The die area consumed by device isolation can be less than for bulk material. (ii) The number of process steps can be reduced. (iii) The substrate current is suppressed. (iv) There is no latch-up effect. (v) Lower parasitic capacitances enable faster circuits and a reduction of the power consumption.

In addition to CMOS technology, SOI can be interesting for the integration of photodetectors. SOI was considered as a possibility to avoid the slow diffusion current, which is caused by carriers being generated by light with long wavelengths (in the region of 850 nm), from the substrate of integrated photodiodes. For photodetectors in a thin SOI layer, this light generates carriers in the silicon substrate wafer, which is isolated from the device SOI layer by the buried oxide. Therefore, SOI avoids the slow diffusion current known from photodiodes in bulk silicon.

A lateral PIN photodiode in a thin SOI layer was investigated first by Colinge [2]. The structure of this lateral PIN photodiode is shown in Fig. 3.1. The SOI layer was made by laser-recrystallization. The thickness of the silicon film was (440 ± 50) nm

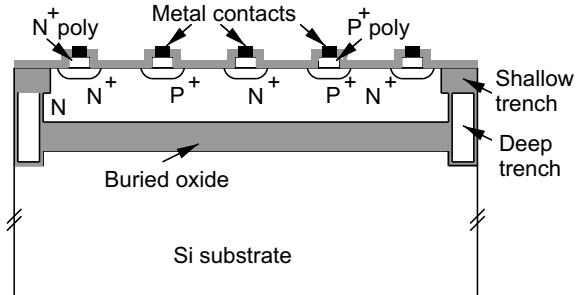
Fig. 3.1 Cross section of a lateral PIN photodetector in a thin-film SOI layer [2]



at the end of the process. The buried oxide layer had a thickness of $1\text{ }\mu\text{m}$ and the oxide on top of the silicon thin-film layer was $0.5\text{ }\mu\text{m}$ thick. The width of the intrinsic region was designed to be $7\text{ }\mu\text{m}$. The N^+ and P^+ regions were each $8\text{ }\mu\text{m}$ wide. The carrier lifetime in the laser-recrystallized SOI film was found to be approximately $8\text{ }\mu\text{s}$ and the dark current of the lateral PIN photodiode was reported to be 0.1 pA per $1\text{ }\mu\text{m}$ junction length for a reverse voltage of 5 V . This value for the dark current is large and is due to the fabrication of the SOI layer by the laser-recrystallization technique, which results in a lower thin-film quality than bonded and etched-back SOI (BESOI). Due to the low thickness of the Si film and the buried and top oxide layers, interference effects were present in the spectral photoresponse. The maximum quantum efficiency of approximately 80% was found at an interference maximum for green light. Due to the low thickness of the Si film, the quantum efficiency decreased strongly for longer wavelengths with smaller absorption coefficients. The quantum efficiency for $\lambda = 780\text{ nm}$ for instance was approximately 9% due to an interference maximum, whereas for $\lambda = 850\text{ nm}$ the quantum efficiency was reduced to only approximately 2%. No results for the transient response of the lateral PIN photodiode were reported.

Ghioni et al. [3] described a lateral PIN photodetector, which is compatible with trench isolation VLSI technology. A larger thickness of $(2.8 \pm 0.5)\text{ }\mu\text{m}$ was chosen for the SOI layer in order to obtain a larger quantum efficiency than mentioned above. The resistivity of the N-type BESOI layer was in the range of 10 to $15\text{ }\Omega\text{cm}$, which corresponds to a doping concentration in the range of $4.5 \times 10^{14}\text{ cm}^{-3}$ to $3.0 \times 10^{14}\text{ cm}^{-3}$. The thickness of the buried oxide was $1\text{ }\mu\text{m}$. Due to the thickness of the SOI layer ($2.8\text{ }\mu\text{m}$) the trench isolation technique as shown in Fig. 3.2 was used. The interdigitated PIN detector biased at 3.5 V attained -3 dB bandwidths in excess of 1 GHz with $\lambda = 840\text{ nm}$ for a finger width of $2\text{ }\mu\text{m}$ and for finger distances of less than $4\text{ }\mu\text{m}$. Photodetectors located in different positions on the wafer exhibited slightly different bandwidths ($\pm 0.2\text{ GHz}$), due to the thickness variations of the SOI layer. The dark current was less than 10 pA at a bias of 5 V for a photodetector area

Fig. 3.2 Cross section of a trench isolated lateral PIN photodetector in a SOI layer [3]



of $75 \times 75 \mu\text{m}^2$. The responsivity was 0.048 A/W ($\eta = 0.071$, quantum efficiency = 7.1%) for a finger spacing of $1.5 \mu\text{m}$ and 0.091 A/W ($\eta = 0.135$) for a finger spacing of $7.0 \mu\text{m}$. A $\pm 15\%$ fluctuation was observed for these values due to the thickness variation of the SOI film over the wafer area. For the smaller finger spacing a larger amount of the incident light is reflected by the aluminum contacts and the quantum efficiency is lower than for the larger finger spacing.

Ghioni et al. [3] reported a calculated sensitivity of -22.5 dBm for a photoreceiver comprising a MOS transimpedance preamplifier and the lateral PIN photodetector in SOI with $R = 0.09 \text{ A/W}$ at a bit-error rate of 10^{-12} .

In order to increase the responsivity, interference effects were investigated. The stack consisting of the top passivating oxide, the SOI layer, and the buried oxide layer forms a Fabry–Perot cavity, with the passivating oxide as the top reflector and the buried oxide as the bottom reflector. In such a way the lateral PIN photodetector can be considered as a resonant photodetector that can be tuned to the desired wavelength in order to maximize the responsivity. The tuning can be done by carefully adjusting the thicknesses of the cavity layers. The conditions for a maximum responsivity are for normal incidence (with l , m and n being integer numbers) [3]:

- (i) passivating oxide layer: $d_{\text{PO}} = l \cdot \lambda / (2\bar{n})$;
- (ii) SOI layer: $d_{\text{SOI}} = m \cdot \lambda / (2\bar{n})$;
- (iii) buried oxide layer: $d_{\text{BO}} = n \cdot \lambda / (4\bar{n})$.

The responsivity of such a resonant structure depends strongly on the thickness of the active layer d_{SOI} (see Fig. 3.3). In the best case, the responsivity of such a resonant structure is more than doubled, but in the worst case, the responsivity of the SOI detector is reduced below that of a nonresonant detector (where no interference effects are taken into account and only reflection at the top oxide to SOI layer interface is considered in addition to the absorption of the SOI layer). The silicon layer incremental thickness between the best case and the worst case was reported to be only 50 nm. The responsivity for $d_{\text{SOI}} = 2.74 \mu\text{m}$, for instance, is 0.125 A/W ($\eta = 0.185$), whereas it is only 0.03 A/W ($\eta = 0.044$) for $d_{\text{SOI}} = 2.79 \mu\text{m}$ in comparison to 0.055 A/W ($\eta = 0.081$) for a nonresonant detector with $d_{\text{SOI}} = 2.79 \mu\text{m}$. Therefore, an extremely good thickness control of less than $\pm 0.5\%$ is required for

Fig. 3.3 Responsivity of a trench isolated lateral SOI PIN photodetector with a light-sensitive area of 50% and with a half-wavelength top oxide layer versus SOI layer thickness. The dotted curve belongs to a nonresonant photodetector [3]

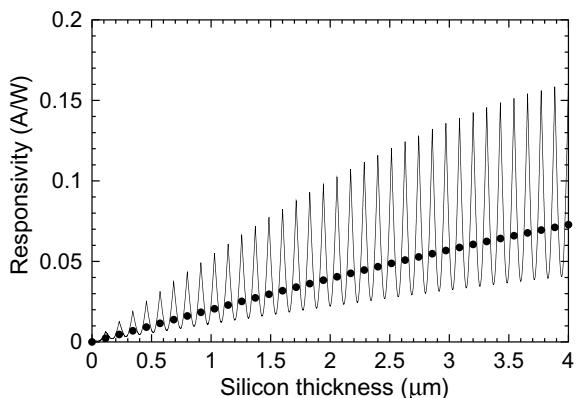
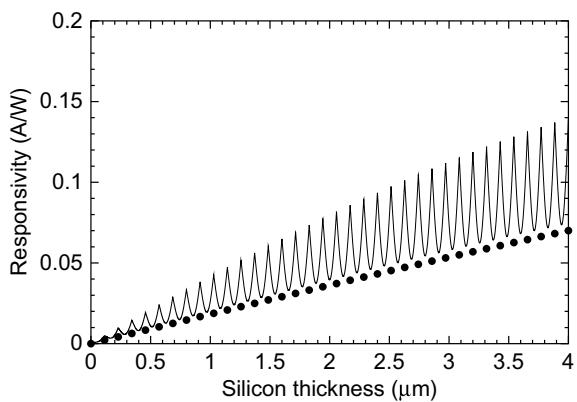


Fig. 3.4 Responsivity of a trench isolated lateral SOI PIN photodetector with a light-sensitive area of 50% and with a quarter-wavelength top oxide layer versus SOI layer thickness. The dotted curve belongs to a nonresonant photodetector [3]



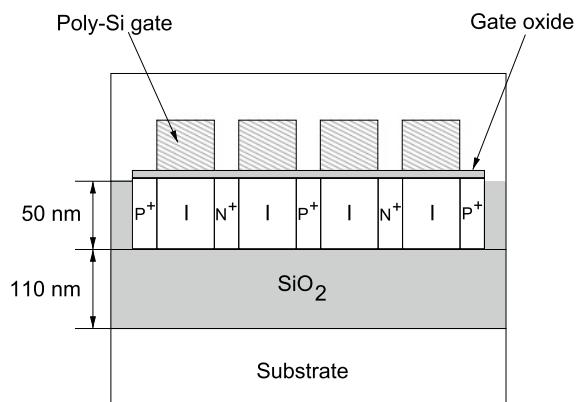
a typical active layer thickness of a few micrometers. An alternative design was suggested by Ghioni et al. [3], if such a strict control cannot be guaranteed:

- (i) passivating oxide layer: $d_{PO} = (2l + 1) \cdot \lambda / (4\bar{n})$;
- (ii) SOI layer: $d_{SOI} = m \cdot \lambda / (2\bar{n})$;
- (iii) buried oxide layer: $d_{BO} = (2n + 1) \cdot \lambda / (4\bar{n})$.

Then a maximum responsivity of 0.105 A/W ($\eta = 0.155$) for $d_{SOI} = 2.74 \mu\text{m}$ is obtained and the minimum responsivity of 0.057 A/W ($\eta = 0.084$) for $d_{SOI} = 2.79 \mu\text{m}$ (see Fig. 3.4) is a little larger than the responsivity of 0.055 A/W for the nonresonant detector. A variation by a factor of approximately two, however, for the responsivity and therefore for the quantum efficiency remains for this design, also, because a thickness tolerance of less than 50 nm for a SOI layer thickness of several micrometers can hardly be obtained by BEZOI.

Lateral PIN photodiodes in SOI films with a thickness of $3.75 \mu\text{m}$ were investigated in [4]. The quantum efficiency for 850 nm was 29% . A bandwidth of 1.1 GHz was reported for a P-N spacing of $2 \mu\text{m}$ with a SOI film resistivity of $50\text{--}100 \Omega\text{cm}$ at

Fig. 3.5 Cross section of an avalanche photodiode in a thin-film SOI layer [10]



a photodiode reverse bias of 3 V [4]. For a reverse bias of 5 V and a SOI film thickness of 2.7 μm , the bandwidth was increased to 3.4 GHz. The quantum efficiency for 840 nm of the photodiodes in the 2.7 μm thick SOI film was 24%. The reverse current of a $50 \times 50 \mu\text{m}^2$ photodiode was 25 pA at a reverse bias of 5 V [4]. At a reverse bias of 9 V, photodiodes with a 250 nm finger spacing exhibited bandwidths of 15 and 8 GHz in SOI films with thicknesses of 0.2 and 2 μm , respectively [5]. The leakage current, however, was 500 μA for this 9 V bias. The quantum efficiencies for 850 nm were 2 and 12%, respectively. Lateral PIN photodiodes in thin SOI films were implemented in OEICs, which operated up to data rates of 3.125 and even 5 Gb/s at a photodiode supply voltage of 24 V [6].

It can be concluded that despite several attempts to increase the quantum efficiency [3, 7–9], the main disadvantage of SOI photodetectors is the low quantum efficiency or responsivity. Therefore, internal amplification of the photocurrent is highly desirable.

The responsivity of a lateral PIN photodiode in a thin-film SIMOX layer was increased by the exploitation of the avalanche effect (in the opinion of the authors) for internal amplification of the photocurrent [10]. Figure 3.5 shows the structure of this photodetector for application in local area networks (LANs) such as the Gigabit Ethernet or Fibre Channel with a wavelength in the range of 780–850 nm. The N⁺ and P⁺ regions are 1 μm wide and the I-regions were 0.6 to 3.0 μm wide. The N⁺-polysilicon gates with a thickness of 200 nm make the 50 nm thick silicon layer with an N-type doping concentration of $3 \times 10^{17} \text{ cm}^{-3}$ fully depleted at a supply voltage of 2.0 V. The polysilicon gates also can be used to adjust the dark current of the photodetector. On top of the gates, several micrometers of oxide were deposited. The capacitance of a 100-square μm photodiode was only 0.2 pF due to the thin SOI layer and the 110 nm thick buried oxide.

A photodetector with a size of $60 \times 60 \mu\text{m}^2$ for the use together with an optical fiber having a 50 μm core diameter was fabricated in a 0.25 μm CMOS technology. Without an antireflection coating, a responsivity of 0.4 A/W at $\lambda = 850 \text{ nm}$ was achieved at a reverse bias of only 2.0 V. A high electric field of $1-2 \times 10^5 \text{ V/cm}$

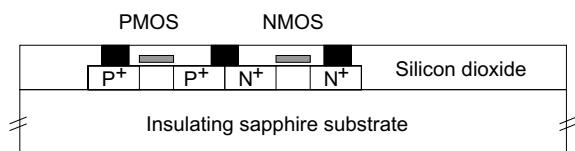
exists in the space-charge region at the P⁺ side for this voltage bringing about an avalanche effect. The photocurrent is amplified due to the rise of the ionization rate in Si under a high electric field of more than 1×10^5 V/cm [11] achieving a responsivity of the 50 nm thick photodetector similar to that of a thick vertical PIN photodiode. A dark current of $0.2 \text{ pA}/\mu\text{m}^2$ at a polysilicon gate bias of -0.8 V was reported for the photodetector. The amplifier used together with the lateral PIN avalanche photodiode in the OEIC for LAN applications will be discussed in Sect. 6.4.13 (Fig. 6.123).

3.2 Silicon on Sapphire

A hybrid integration approach representing a paradigm shift from traditional optoelectronic integration and packaging methods was described in [12, 13]. A recent breakthrough in silicon-on-sapphire (SOS) CMOS VLSI technology offers simple and elegant solutions to many system integration and packaging challenges that have to be overcome when bulk silicon CMOS technologies are used. The substrate being present for bulk CMOS ICs absorbs at 850 nm and even at 980 nm wavelengths. Complex and expensive integration procedures like VCSEL substrate removal are therefore necessary to enable optical vias through the VCSEL substrate.

The optical transparency of sapphire substrates, its high thermal conductivity and the high-speed device characteristics of SOS CMOS circuits makes SOS technology an excellent choice for cost effective optoelectronic die-as-package (DASP) systems and for implementing high-performance optical interconnects [13]. SOS CMOS technology is a close relative to the more popular silicon-on-insulator (SOI) CMOS technology that was believed to become the standard technology for deep sub-micron VLSI [14, 15]. SOS uses sapphire-aluminum oxide (Al_2O_3) instead of silicon as the substrate. Sapphire is an insulator and its thermal conductivity is higher than that of silicon dioxide. But what is more, sapphire is transparent from 200 nm to 5,500 nm. A 0.5 μm SOS CMOS process with an ultra-thin silicon layer having a thickness of only 100 nm is available from Peregrine via MOSIS foundry service [13]. The cross section of an SOS chip is shown in Fig. 3.6. The MOSFETs with low and zero threshold voltage have a lighter doping in the channel than the regular threshold voltage MOSFETs and are therefore fully depleted showing no kink effect in the $I_D - V_{DS}$ characteristics in contrast to the the regular threshold voltage MOSFETs.

Fig. 3.6 Cross section of a CMOS inverter in ultra-thin SOS [13]



VCSELs were mounted on a SOS CMOS chip. The die of the SOS chips was not optically polished on the backside. In order to avoid severe light loss due to scattering from the back surface index matching was necessary. For that purpose the die was glued on a glass cover slide using index matching wax [13]. The glass cover slide was then mounted on a blank lithography mask and placed upside down in a mask aligner. Conductive epoxy was applied to each bondpad of the VCSEL die which was subsequently placed on the wafer in the mask aligner. To fix the VCSEL die on the chip, drops of UV curable epoxy were placed at the corners of the VCSEL die. After optical alignment the blank mask with the SOS CMOS die was lowered to make contact with the VCSEL die. Then the two dies were mechanically bonded together by exposing the assembly to UV light. Finally, the assembly was placed in an oven to cure the conductive epoxy for an hour at 60 °C. The VCSELs were operated at data rates above 1 Gb/s [13]. Metal-semiconductor-metal photodiodes also were bonded to SOS CMOS receivers. These optical receivers were tested at 1 Gb/s.

3.3 Polyimide Bonding

By using polyimide bonding GaAs PIN photodiodes and vertical cavity surface emitting laser diode (VCSEL) chips were hybridized to CMOS circuits [16]. Compared to other methods, this polyimide bonding has three advantages: (i) it is a wafer-scale process; (ii) it integrates both VCSELs and photodiodes simultaneously; and (iii) it needs no accurate alignment in the bonding step. The structure of a pixel with a GaAs PIN photodiode and a VCSEL is shown in Fig. 3.7.

To apply the polyimide bonding technique to an originally uneven CMOS wafer, the CMOS wafer surface has to be planarized before wafer bonding. Special VCSEL and photodetector (PD) attaching areas besides CMOS circuit areas were prepared. Only aluminum remained in these attaching areas of the size $50 \times 50 \mu\text{m}^2$. Gold was deposited onto the VCSEL attaching areas on the CMOS wafer to act as a heat pipe for the power dissipated in the VCSELs. Then the uneven CMOS surface was planarized with polyimide (of a different type from the bonding one). Planarization

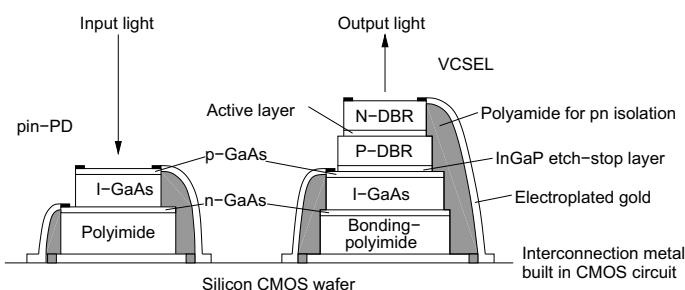


Fig. 3.7 Cross section of polyimide bonded CMOS/PD/VCSEL structure [16]

was completed by lapping and polishing the polyimide with ultra-fine aluminum oxide powder until the desired flatness was achieved. Reactive-ion etching with oxygen gas then was applied to expose the gold heat pipe areas. A surface flatness of $0.1\text{ }\mu\text{m}$ was obtained [16].

After planarization, a GaAs wafer with epitaxial layers of VCSELs and photodiodes is bonded to the CMOS wafer using polyimide as an adhesive. After removing the GaAs substrate by mechanical lapping and selective wet etching, the GaAs epitaxial structure is divided into chip-size sections, so that the prefabricated marks in the CMOS wafer are exposed. Now, the photonic devices are contacted using the marks on the CMOS wafer for photolithography. Vertical electric interconnects between the photonic devices and the CMOS circuits are formed with electroplated gold. A thermal resistance of 400 K/W was reported for a polyimide bonded VCSEL with a $15\text{ }\mu\text{m}$ upper distributed-Bragg-reflector (DBR)mesa diameter and a $40\text{ }\mu\text{m}$ square lower-DBR-mesa resulting in a temperature rise of 6 K for a VCSEL power consumption of 15 mW [16].

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Chapter 4

SiGe Photodetectors



SiGe alloys allow the integration of infrared detectors on Si. The addition of Ge to Si also increases the absorption coefficient in the spectral range from 400–1000 nm, allows a reduction of the detector thickness, and, therefore, enables faster detectors than with pure Si. To exploit the advantages of SiGe alloys for Si-based photodetectors, however, the problem associated with the lattice constant mismatch has to be understood. Subsequently, this chapter describes an example of a SiGe OEIC.

4.1 Heteroepitaxial Growth

The growth and physical properties of $\text{Si}_{1-x}\text{Ge}_x$ heteroepitaxial layers on Si have been investigated for more than 20 years [1–5] finally producing a technology which is entering high-volume and large-scale manufacturing of heterojunction bipolar transistors (HBTs) [6] and SiGe-HBT-BiCMOS circuits [7, 8]. Optoelectronic applications of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ devices also have been developed. Medium-wavelength (1.3–1.55 μm) photodetectors for optical communication [9–11], 2–12 μm infrared photodetectors for two-dimensional focal plane arrays for thermal imaging and night vision [12–14], optical waveguides [15], and infrared light emitters for chip-to-chip optical interconnects [16, 17] have been suggested.

On the way to introducing optoelectronic devices into VLSI and ULSI to obtain a silicon-based *superchip* [18, 19], however, the following significant limitations of the SiGe/Si material system have been discovered [20]:

- (i) Due to the large lattice constant of Ge, which is about 4.2% larger than that of Si, a critical thickness of $\text{Si}_{1-x}\text{Ge}_x$ layers on Si for thermal stability against misfit dislocation generation due to lattice mismatch exists [21]. This critical thickness is only about 15 nm for a Ge fraction x of 0.2 with a resulting bandgap change of approximately 150 meV [22]. Due to this low critical thickness, the

quantum efficiency of normal incidence photodetectors relying on photogeneration across the $\text{Si}_{1-x}\text{Ge}_x$ bandgap is severely limited.

- (ii) When a $\text{Si}_{1-x}\text{Ge}_x$ layer with a thickness greatly exceeding the critical thickness is grown directly onto Si, the layer relaxes but forms a dislocation density at the surface of order 10^{12} cm^{-2} [23]. This dislocation density reduces the carrier mobility and increases leakage currents significantly and is far too large to allow economic yields of devices in production [8]. Although relaxed $\text{Si}_{1-x}\text{Ge}_x$ buffer layers with the bulk lattice constant of the $\text{Si}_{1-x}\text{Ge}_x$ alloy on top of the Si substrate can be introduced and pseudomorphic heterostructures, which have a lateral lattice constant larger than that of Si, can then be grown on top of the buffer [24, 25], these relaxed buffers still reduce the threading dislocation density only to below 10^4 cm^{-2} for $\text{Si}_{0.8}\text{Ge}_{0.2}$ [23]. This density is already comparable to many III/V systems [8]. More recently, a number of annealing steps during growth have reduced the dislocation density to 10^2 cm^{-2} for $\text{Si}_{0.8}\text{Ge}_{0.2}$ and $x < 0.2$ [26]. Dislocations, however, still pose a problem for higher Ge fractions and future large-scale optoelectronic applications, therefore, remain uncertain.
- (iii) The dopant diffusion during thermal processing for device fabrication often degrades the nanometer precision in the placement of dopant atoms required for heterojunction devices, which can be achieved during the initial growth of heterostructures at temperatures below 700°C [27, 28].
- (iv) Under all combinations of strain, $\text{Si}_{1-x}\text{Ge}_x$ is an indirect-bandgap material, resulting in inefficient emission of light and inefficient detection due to a small absorption coefficient compared to pure Ge, GaAs, or InGaAs, at least for $x < 0.75$.

Let us continue with light absorption of SiGe alloys (point (iv)) in the next section.

4.2 Absorption Coefficient of SiGe Alloys

The exchange of Si atoms by Ge atoms increases the absorption coefficient. Furthermore the bandgap reduces with increasing Ge fraction and wavelengths longer than 1100 nm can be detected. Figure 4.1 shows the absorption coefficient for Ge fractions of 20, 50, and 75%.

It is advantageous to use SiGe detectors instead of Si detectors, when longer wavelengths, a thinner absorbing layer, a higher quantum efficiency and/or a higher speed of the detector are needed. In the following, an example of a SiGe receiver trying to use these advantages will be described.

Fig. 4.1 Absorption coefficient for SiGe with different compositions [29]

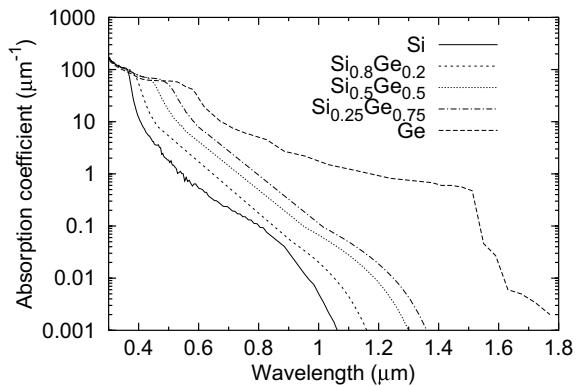
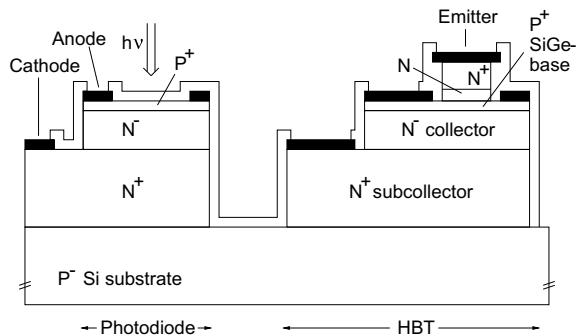


Fig. 4.2 Schematic cross section of a SiGe/Si PIN HBT photoreceiver [33]



4.3 SiGe/Si PIN Hetero-Bipolar-Transistor Integration

SiGe photodiodes were described in [30, 31], however, the amplifiers in these references employed pure Si transistor devices. SiGe/Si technology has developed rapidly in recent years and it has been demonstrated that it outperforms Si technology in terms of the speed of transistors [32]. Therefore, it is advantageous to combine SiGe/Si photodetectors with SiGe/Si transistors [33].

Figure 4.2 shows the cross section of the first monolithically integrated SiGe/Si PIN photodiode and heterojunction bipolar transistor (HBT) front-end photoreceiver. The PIN-HBT structure was grown by one-step molecular beam epitaxy (MBE). Table 4.1 contains the layer compositions and doping concentrations of the SiGe-OEIC. The emitter and collector layers consist of Sb-doped Si. The base layer of the double heterojunction NPN HBT structure is a $\text{Si}_{1-x}\text{Ge}_x$ alloy with a smaller bandgap than that of Si. The Ge mole fraction in the base layer is graded from $x = 0.1$ at the emitter side to $x = 0.4$ at the collector side to accelerate the electrons traveling through the base towards the collector by a quasi-electric field. Spacer layers on both sides of the base minimize the effect of outdiffusion during epitaxy and processing.

Table 4.1 Layer compositions and doping concentrations of a SiGe-Si PIN-HBT OEIC

Layer	Material	Type	Doping (cm^{-3})	Thickness (nm)
Emitter contact	Si	N^+	1×10^{19}	200
Emitter	Si	N	2×10^{18}	100
Spacer	$\text{Si}_{0.9}\text{Ge}_{0.1}$	I		1
Base	$\text{Si}_{1-x}\text{Ge}_x$ ($x:0.1 \rightarrow 0.4$)	P^+	5×10^{19}	30
Spacer	$\text{Si}_{0.6}\text{Ge}_{0.4}$	I		10
Collector	Si	N^-	1×10^{16}	250
Subcollector	Si	N^+	1×10^{19}	1500
Substrate	Si	P^-	2×10^{12}	$540 \mu\text{m}$

The PIN photodiode is formed by the Si N^+ -subcollector, by the Si N^- collector, and the SiGe P^+ base layers of the HBT (see Fig. 4.2). The I-absorption layer is formed by the Si N^- collector due to the one-step MBE growth, which provides advantages over regrowth such as better planarity, simpler processing, and higher yield [33]. The MBE growth temperatures for the collector and emitter layers were 415 °C. The base was grown at 550 °C. The growth rate was only 0.2 nm/s at these low temperatures.

The devices were isolated by mesa formation. The mesa size of the photodiode was $12 \times 13 \mu\text{m}^2$. After MBE, the emitter contact was defined by evaporation, followed by emitter mesa formation with SF_6 - and O_2 -based dry and KOH-based wet etching. Minimal undercut and base over-etch were obtained by the two-step etch procedure, resulting in a low base access resistance. Then the base-collector mesa was formed by dry etching. The collector and PIN cathode contacts were formed by evaporation on the exposed highly doped subcollector layer. Another etch step of the subcollector layer was applied for the separation of the devices. After this mesa isolation a PECVD SiO_2 layer was deposited and the pad contacts were opened.

The dark current of the photodiode was about 0.1 μA at $U_{\text{PIN}} = 4 \text{ V}$ and 1 μA at $U_{\text{PIN}} = 9 \text{ V}$. For the PIN photodiode with an I-layer thickness of 0.25 μm , a bandwidth of 450 MHz for $\lambda = 850 \text{ nm}$ and $U_{\text{PIN}} = 9 \text{ V}$ was measured. The PECVD SiO_2 layer with a thickness of 1.1 μm served as an antireflection coating leading to a measured responsivity of 0.3 A/W and an external quantum efficiency of 43% for $U_{\text{PIN}} = 5 \text{ V}$. Here, the SiGe anode did not increase the quantum efficiency by a significant amount compared to a Si anode. For a large enhancement of the quantum efficiency a high Ge fraction in the intrinsic zone of the PIN photodiode would have been necessary, which of course would introduce a high density of dislocations.

The bandwidth of 450 MHz was ascribed to the slow diffusion of carriers generated in the substrate and in the subcollector [33], because of the small I-layer thickness. We should not, however, accept this explanation, because the responsivity value of 0.3 A/W is too high for this explanation. It can be understood only when the cathode current, which is the sum of the subcollector/ P^- -substrate diode photocur-

rent and of the P⁺-SiGe-anode/N-collector/N⁺-subcollector diode photocurrent, was measured. The bandwidth then was not limited by carrier diffusion from the P[−] substrate but by drift in the space-charge region of the subcollector/P[−]-substrate diode. The space-charge region extended far into the low doped P[−]-substrate with $N_A = 2 \times 10^{12} \text{ cm}^{-3}$ and the measured bandwidth of 450 MHz for $U_{\text{PIN}} = 9 \text{ V}$ seems possible. The reported increase in the responsivity and in the bandwidth with increased reverse bias also supports the new explanation with drift instead of carrier diffusion.

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Chapter 5

Design of Integrated Optical Receiver Circuits



Most of the optoelectronic integrated circuits (OEICs) described in this book are analog circuits. We, therefore, will restrict ourselves to the design of analog integrated circuits. The exclusion of the design of digital integrated circuits, furthermore, seems to be justified because there are many books describing this topic (for instance [1–3]). The design of analog integrated circuits is, for instance, described in [4]. It will be, therefore, sufficient to give here an overview on the aspects being most relevant for the design of analog OEICs. Since photocurrents have to be converted to signal voltages in most applications, the transimpedance amplifier will be discussed in some detail, especially with respect to its implementation in OEICs. A new π model for such a transimpedance amplifier also will be introduced. Furthermore, the basics of electronic noise and sensitivity of optical receivers are applied to point out the possibilities of silicon OEICs. The Poisson statistics and the quantum limit are added, since they allow to eliminate the electronic noise with SPAD receivers, which will be described in Chap. 6.

5.1 Circuit Simulators and Transistor Models

Circuit simulation is useful for the development of integrated circuits in order to avoid long time periods for fabrication and high development costs. Actually, circuit simulation is absolutely necessary for the development of integrated circuits in advanced submicrometer silicon technologies, because analytical models and calculations do not cover short channel effects and, therefore, are not accurate enough. In addition, most of the circuits contain too many devices for analytical investigations.

Circuit simulators implement transistor models covering their temperature dependence as well as short-channel effects and guarantee the correct calculation of the operating point, which is the prerequisite for the simulation of frequency and transient responses, because the amplification of the circuit depends on the operating

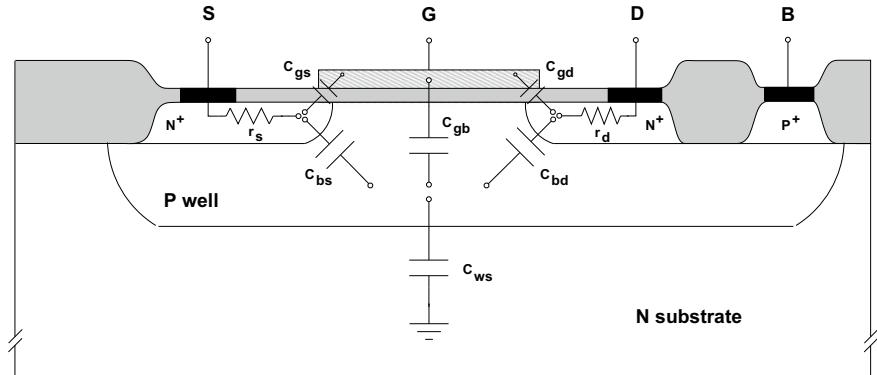


Fig. 5.1 Integrated-circuit MOS transistor structure including parasitic elements

point of the circuit, which determines the voltages across all the transistor terminals and the currents flowing in all the devices. Therefore, the transconductance g_m of each transistor, which determines the amplification, and the junction capacitances in each transistor, which determine the frequency and transient responses, depend on the operating point of the circuit.

There are several widespread circuit simulation programs: for instance HSPICE originally developed by the University of California at Berkeley and ACCUSIM as part of the MENTOR design framework as well as SPECTRE-S as part of the CADENCE design framework. ACCUSIM and SPECTRE-S are part of the professional design frameworks being used by semiconductor chip manufacturers. Foundries and manufacturers of application specific integrated circuits (ASICs) also support these frameworks. The manufacturers of ASICs make the transistor models and parameters available to customers and design houses. One of the newest and widely used transistor models covering the small signal and large signal behavior for MOSFETs is BSIM3.3 [5]. This model was used here for the development of CMOS OEICs with ACCUSIM within the MENTOR framework and for the development of BiCMOS OEICs with SPECTRE-S within the CADENCE framework.

The modeling of MOSFETs dates back to [6, 7]. The models consider parasitic capacitors and resistors within the MOS transistors shown in Fig. 5.1. The parasitic elements are included in the small-signal equivalent circuit (Fig. 5.2) underlying the transistor models implemented in modern circuit simulators. A small-signal model implicitly assumes a linear behavior. The parameters of the small-signal model are usually designated by lower case letters.

The conductances g_{bd} and g_{bs} are the conductances of the bulk-to-drain and bulk-to-source junctions. These conductances are normally very small, since these junctions are reverse-biased. The channel transconductances g_m , g_{mb} , and g_{ds} are defined as

$$g_m = \frac{\partial i_d}{\partial v_{gs}}, \quad g_{mb} = \frac{\partial i_d}{\partial v_{bs}}, \quad g_{ds} = \frac{\partial i_d}{\partial v_{ds}} \quad (5.1)$$

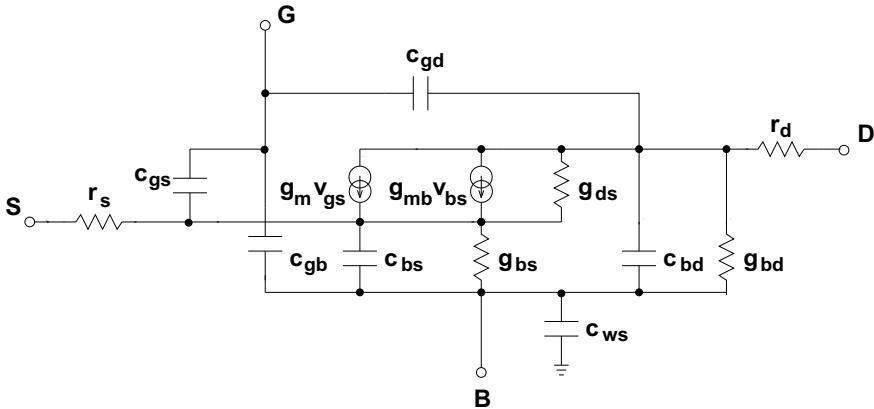


Fig. 5.2 Complete MOS transistor small-signal equivalent circuit [8]

at the quiescent point, i.e. at the operating point. The transconductance g_m gives rise to the desired amplification of a MOSFET. The so-called back-gate effect, arising from g_{mb} , however, reduces the amplification when source and bulk, i.e. well, cannot be connected as in the case when PMOS input transistors would be used in a difference amplifier on an N-type substrate, for instance. The conductance g_{ds} considers the channel length modulation effect for the transistor in saturation.

For bipolar transistors in HSPICE, level 1 can be used, for instance. SPECTRE-S, which was used in the development of BiCMOS OEICs, implements several high-current effects in addition to the large-signal model of Gummel and Poon. The simpler Ebers–Moll large-signal model is obtained, when certain parameters are left unspecified. The complete large-signal and small-signal models consider parasitic capacitors and resistors within the bipolar transistors shown in Fig. 5.3.

The complete small-signal equivalent circuit of a bipolar transistor considering the parasitic capacitors and resistors is shown in Fig. 5.4.

The parameter c_π not shown in Fig. 5.3 is the sum of the base-charging capacitance $c_b = \tau_F g_m$ and the emitter-base depletion layer capacitance c_{je} [9]. For the diffusion transistor with a constant base doping concentration, the base transit time τ_F is equal to $Q_E/I_C = W_B^2/(2D_N)$, where Q_E is the minority-carrier charge in the base, W_B is the base width, and D_N is the minority-carrier diffusion coefficient. The base-collector capacitance c_μ is the sum of $c_{\mu 1}$ and $c_{\mu 2}$ shown in Fig. 5.3. The collector-substrate capacitance c_{cs} is the sum of c_{cs1} , c_{cs2} , and c_{cs3} . The parameters r_π and r_μ are obtained easily:

$$r_\pi = \frac{\beta}{g_m}, \quad (5.2)$$

and

$$r_\mu = \frac{\Delta V_{CE}}{\Delta I_B} = \frac{\Delta V_{CE}}{\Delta I_C} \frac{\Delta I_C}{\Delta I_B} = r_o \beta, \quad (5.3)$$

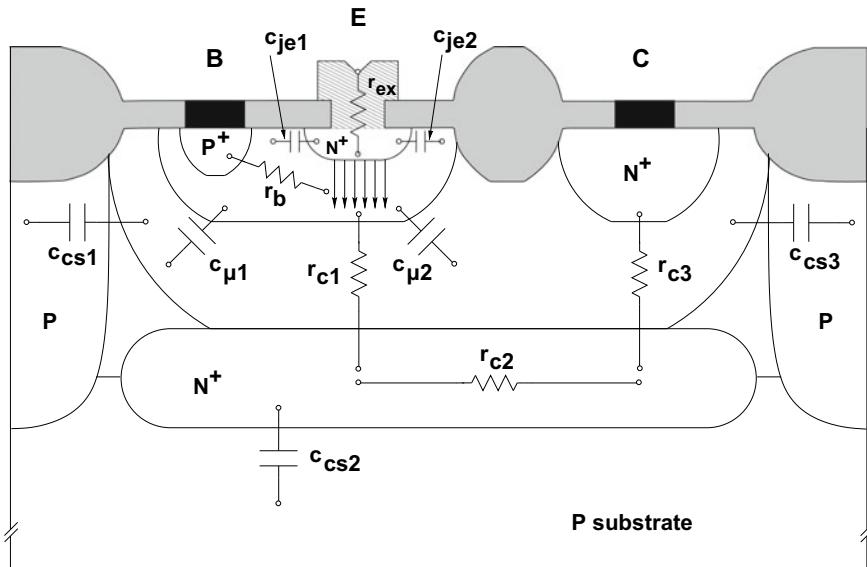


Fig. 5.3 Integrated-circuit NPN bipolar transistor structure including parasitic elements [9]

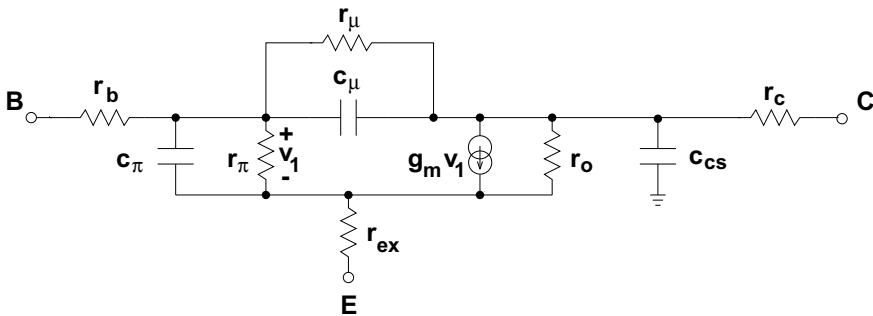


Fig. 5.4 Complete bipolar transistor small-signal equivalent circuit in a common-emitter circuit [9]

where r_o is the small-signal output resistance. The collector series resistance r_c is the sum of r_{c1} , r_{c2} , and r_{c3} (compare with Fig. 5.3). The emitter series resistance is represented by r_{ex} . The base series resistance r_b is one of the most important parameters.

The values for the parameters shown in Fig. 5.4 are available in the parameter file from the manufacturers of ASICs for several predesigned transistors.

In addition to typical parameter values, parameter values for the so-called slow and fast cases are also available. These extreme parameter values have to be considered in order to guarantee the correct function of a circuit within the complete specified range for the fabrication process. Furthermore, the influence of the tem-

perature on the performance of a circuit has to be investigated within the specified operating temperature range. For MOS circuits, the bandwidth usually reduces with increasing temperature and increases for temperatures lower than room temperature. Simulations have to be made in order to check whether the bandwidth is sufficient for the highest specified operating temperature and whether the circuit is immune against oscillations for the lowest specified operating temperature. The worst cases for MOS circuits are the combination of the highest specified operating temperature with the slow MOS transistor parameter values and the combination of the lowest specified operating temperature with the fast MOS transistor parameter values.

The current in bipolar transistors increases with temperature resulting in an increase of the circuit bandwidth with temperature. Therefore, the slow bipolar transistor parameter values have to be combined with the lowest specified operating temperature and the fast bipolar transistor parameter values have to be combined with the highest specified operating temperature in order to consider the worst cases for bipolar circuits.

In addition to the differences in the worst case behavior between MOSFETs and bipolar transistors, there are fundamental differences in the amplification and frequency behavior of MOS and bipolar transistors as well as analog MOS and bipolar circuits, which result from the fundamental difference of the output characteristics of the bipolar transistor $I_C(U_{CE}, U_{BE})$ in the forward active region and of the MOS transistor $I_D(U_{DS}, U_{GS})$ in the saturation region:

$$I_C = I_S \left(1 + \frac{U_{CE}}{U_{Ea}} \right) \exp[U_{BE}/(k_B T/q)], \quad (5.4)$$

$$I_D = \frac{1}{2} \mu_n C'_\text{ox} \frac{W}{L} (1 + \lambda_{ch} U_{DS}) (U_{GS} - U_{Th})^2. \quad (5.5)$$

These equations consider the Early effect, i.e. the increase of I_C with U_{CE} due to a decrease in the base width, by the incorporation of the Early voltage U_{Ea} and the channel length modulation effect, i.e. the increase in I_D because of the decrease in the effective channel length with an increase in the drain space-charge region width due to an increase in U_{DS} by the incorporation of λ_{ch} .

The differences between bipolar and MOS analog circuits are caused by the exponential dependence of the collector current I_C on the base voltage U_{BE} and by the quadratic dependence of the drain current I_D on the gate voltage U_{GS} . The transconductance of a bipolar transistor, therefore, is

$$g_m = \frac{\partial I_C}{\partial U_{BE}} = \frac{I_C}{k_B T/q}, \quad (5.6)$$

whereas the transconductance of a MOSFET is

$$g_m = \frac{\partial I_D}{\partial U_{GS}} = \frac{2 I_D}{U_{GS} - U_{Th}}. \quad (5.7)$$

When we assume that $I_C = I_D$ and that $U_{GS} - U_{Th} = 0.5\text{ V}$, then the transconductance of the bipolar transistor is 10 times larger than that of the MOSFET, because $k_B T/q = 25\text{ mV}$. This means that bipolar amplifiers have a much larger amplification factor than MOS amplifiers, since the amplification factor is proportional to the transconductance for most types of amplifiers. Capacitive loads can be charged more rapidly by bipolar than by MOS transistors and the bipolar transistor is said to have the better driver capability. The bandwidth of bipolar amplifiers as a consequence is larger than the bandwidth of MOS amplifiers. For many operational amplifiers, as an example, the gain-bandwidth-product is proportional to the transconductance of the input transistor [4].

The design frameworks offer schematic entry for the definition of circuit diagrams, i.e. the circuit diagram can be drawn by placing device symbols and connecting them. Within the CADENCE framework, the schematic entry program is called COMPOSER and within the MENTOR framework there is the schematic entry program DESIGN ARCHITECT. It is, therefore, not necessary for a designer to write a netlist. The circuit simulator derives the netlist from the schematic. In such a way the number of possible errors is minimized.

5.2 Layout and Verification Tools

When the required specifications are met with the circuit diagram according to circuit simulations, the next step is the layout of the integrated circuit. The frameworks contain the layout tools necessary for this task. The chip manufacturers also make the process definition and design rule files available to the customer or design house. These files are necessary for the design rule check (DRC) of the layout in order to detect violations and to be able to correct them.

When the design rule check does not report any errors, there is still the possibility of deviations from the circuit diagram. Therefore, tools are included within the frameworks for the comparison of layout and schematic. These layout-versus-schematic (LVS) tools require the design rule file. LVS is one part of the design verification. A further verification tool is included within each framework, which enables the extraction of parasitic capacitances and resistances of interconnects from the layout. These parasitics were not included in the circuit diagram for prelayout circuit simulations. They can, however, deteriorate the behavior of the circuit. Therefore, the extraction tools allow us to add these parasitics to the circuit diagram or to include them in a netlist. In such a way the so-called postlayout simulations become possible. Usually, the bandwidth of the circuit calculated by postlayout simulations will be lower than initially determined by the prelayout simulations.

Since the OEICs described here are optimized (full custom) designs, no library cells could be used for the amplifiers, i.e. all mask levels had to be designed, and the layout was done mostly manually.

5.3 Design of OEICs

Figure 5.5 shows the flowchart for the development of OEICs. Starting from the technological flowchart of a bipolar, CMOS, or BiCMOS process, the PN junction of a diode or the two PN junctions of a transistor have to be selected for a photodetector. After this selection, the topology and the doping profiles of the photodetector can be calculated using a one- or two-dimensional process simulation program considering the technological flowchart. Such programs are, for instance, SUPREM3 [10] and TSUPREM4 [11]. This topology and these doping profiles can serve as an input for a device simulator, which offers a model for photogeneration and optical transmission of isolation and passivation stacks. Such a device simulator is, for instance, MEDICI [12]. For the device simulations, the operating conditions like photodetector bias, operating temperature, and optical wavelength have to be considered. With the help of the device simulations, rise and fall times of the detector photocurrent, bandwidth, quantum efficiency, and capacitance C_D (compare Fig. 1.17) can be extracted. For the example of the integration of PIN photodiodes in a CMOS process, the results of the device simulations were used to develop process modules for the implementation of shallow junctions in order to increase the internal quantum efficiency of the PIN photodiodes and for the implementation of an antireflection coating in order to increase the optical quantum efficiency. The device simulations also showed that the series resistance of the PIN photodiodes, which would result from the use of surface substrate contacts, can be eliminated by a back contact.

The most important aspect in the design flowchart of OEICs is the combination of photodetector device simulation and circuit simulation. Experience shows that the use of C_D and of a ramp with the rise time or fall time for the photocurrent leads to good results for transient circuit simulations (Fig. 5.6). For AC simulations of the frequency response, it is also sufficient to use the photodetector capacitance C_D . It should, however, be noted that a DC offset current has to be added to the AC current source, because negative photocurrents are not possible. C_D has to be added to the schematic of the amplifier and appropriate current sources have to be defined for the circuit simulations.

For some photodetectors, C_D alone may not be sufficient and it may be necessary to include the series resistor R_S (see Figs. 1.17 and 5.6). It should be mentioned that this model may not be sufficient, when diffusion of photogenerated carriers is present in the photodetector. For this case, it may be suggested to store the photocurrent values calculated by the device simulator as a function of time in a file and to read this $I_{ph}(t)$ file by the circuit simulator in order to simulate the transient response of the OEIC. The method being most convenient concerning the combination of device and circuit simulation would be to simulate the OEIC, i.e. the photodetector together with the amplifier, using a circuit simulator on the device level. This method, however, would be very CPU time intensive when all transistors in the amplifier have to be considered by device simulations like the photodetector.

Let us return to the design flowchart of OEICs (Fig. 5.5). Possibly the schematic of the amplifier has to be changed in order to meet the specifications of the OEICs.

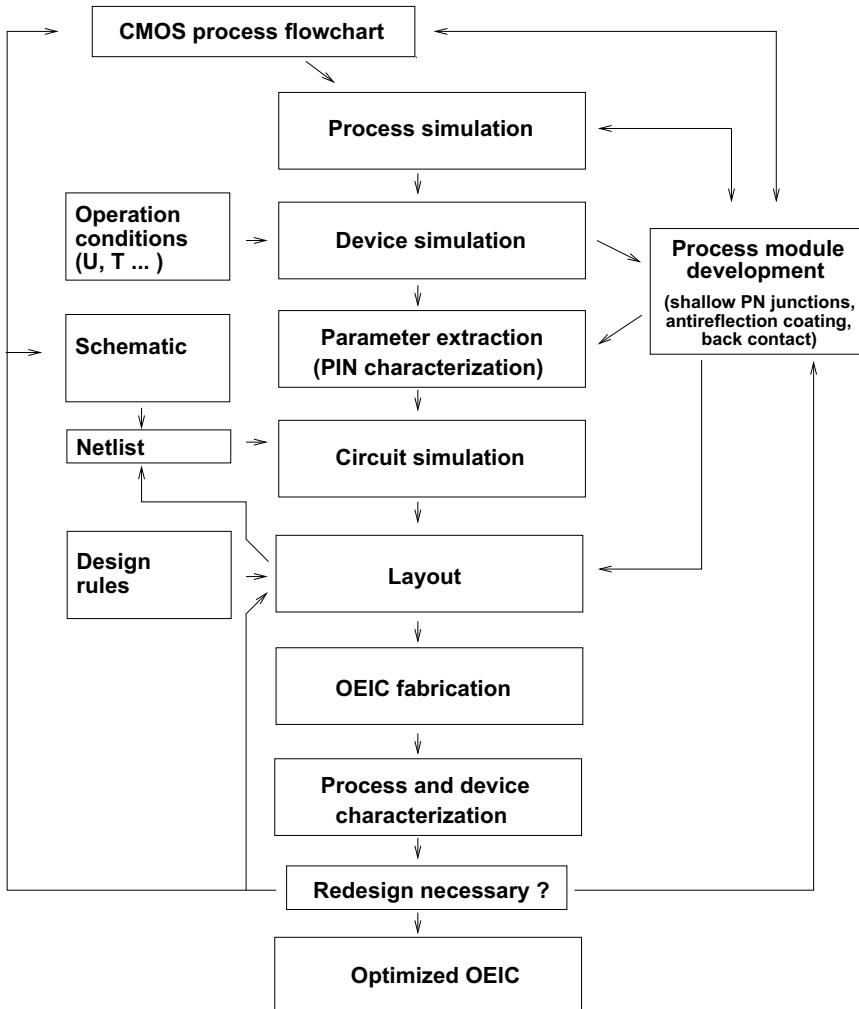
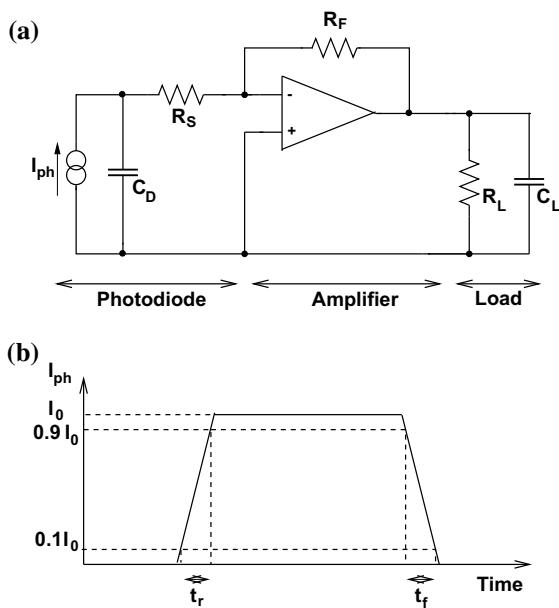


Fig. 5.5 Design flowchart for the development of OEICs. Here the integration of PIN photodiodes in CMOS OEICs is taken as an example

When these prelayout simulations predict that the specifications can be fulfilled, the layout can be drawn. For the integration of photodetectors, it is, of course, necessary to obey the design rules of the process and to add as few new design rules as possible for new process modules like the antireflection coating for instance. Due to the reduction of the doping concentration in the N^- epitaxial layer for the speed enhancement of the CMOS-integrated PIN photodiodes, the minimum distance of analog P-type wells had to be increased in order to avoid reach-through currents between P-type wells with different potentials. When the layout is finished, a design

Fig. 5.6 **a** Equivalent circuit of a photodiode for the circuit simulation of an OEIC. **b** Photocurrent versus time for the consideration of rise and fall times obtained by device simulations or by measurements



rule check is performed. After the correction of possible errors, the layout is compared with the netlist (layout versus schematic) for the detection of possible errors. Finally, when no errors are present or after they are corrected, parasitic capacitors of metal and polysilicon interconnects as well as series resistances of these interconnects are extracted and added to the netlist. For metal interconnects usually only the capacitances are extracted, because their resistances are negligible. Now, the post-layout simulation can be performed. When the specifications for the OEIC are no longer met, an iteration becomes necessary. Changes in the layout, in the netlist, or in the schematic may be necessary. Usually, it will be rather unlikely that the detector has to be modified. When all specifications are fulfilled, the so-called chip finishing is done, i.e. alignment masks and process control modules are added and arranged together with the chip layout on the reticles or on a wafer-size area. Then the masks are fabricated and the chips can be processed.

The OEICs produced have to be characterized. Information obtained by the process monitoring with the help of the process control modules will be used for the interpretation of the OEIC performance. The measured results have to be compared with the specifications for the OEIC. When all knowledge and know-how concerning the design of non-optoelectronic analog integrated circuits has been considered, the design of OEICs should be successful after the first OEIC fabrication as is most desirable and as is usually achieved in industrial chip design. When certain specifications are not met, a correction of the layout, of the schematic, of the process modules, or of the steps for photodetector integration in the technological flowchart may have to be made.

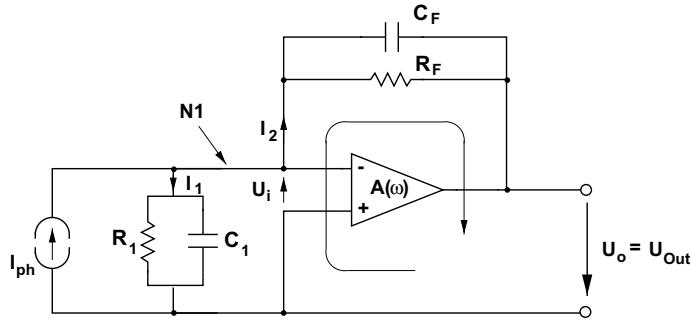


Fig. 5.7 Operational amplifier in transimpedance configuration for I/U conversion of a photocurrent

In the example of the PIN CMOS integration, the process modules, and the technological flowchart were developed perfectly at the first attempt. A redesign was only necessary to increase the sensitivity of the OEICs, i.e. of the active load resistors connected to the photodiodes, and to improve the group delay flatness in the specified frequency range [13].

5.4 Transimpedance Amplifier

A current/voltage (I/U) converter is also called a transimpedance circuit, because an output voltage being proportional to the input current is generated similarly as at an impedance. Each resistor is a current/voltage converter, with its output impedance being equal to its resistor value. In an active current/voltage converter, however, the output impedance is determined by an operational amplifier and, therefore, is independent of the proportionality factor between I and U .

A real current source can be split into an ideal current source with an impedance equal to infinity and into a parallel impedance $Z_D = R_D \parallel C_D$. Without a series resistance, i.e. $R_S = 0$, the equivalent circuit of a photodiode (Fig. 1.17) is equal to the equivalent circuit of the real current source in Fig. 5.7. In fact, the circuit in Fig. 5.7 is the most common amplifier used together with photodiodes. The compensation capacitor C_F is needed to avoid gain-peaking or to guarantee stability. The implementation of an operational transimpedance amplifier configuration is also very interesting for the optoelectronic integration especially when low offset voltages compared to a reference voltage are required. The properties of this configuration, therefore, will be discussed in detail here.

5.4.1 Frequency Response

The frequency response function $G(\omega)$ for the circuit shown in Fig. 5.7 can be derived thus:

$$U_i + I_2 Z_F + U_o = 0, \quad (5.8)$$

$$I_{ph} - I_1 - I_2 = 0 \quad (5.9)$$

with $Z_D = R_D \parallel C_D$, $Z_F = R_F \parallel C_F$, $U_i = U_o / A(\omega)$, and $I_1 = U_i / Z_D = U_o / (A(\omega) Z_D)$ where $A(\omega)$ is the frequency dependent amplification factor of the operational amplifier. Inserting U_i into (5.8), results in

$$Z_F I_2 + \left(1 + \frac{1}{A(\omega)}\right) U_o = 0. \quad (5.10)$$

Inserting I_1 into (5.9), multiplying both sides of the equation by Z_F , and adding to (5.10) leads to the transfer function, which is the *transimpedance* and possesses the dimension Ω :

$$\frac{U_o}{I_{ph}} = G(\omega) = -\frac{Z_F}{1 + (1/A(\omega))(1 + (Z_F/Z_D))}. \quad (5.11)$$

When we insert the frequency-dependent amplification of the operational amplifier $A(\omega)$ with the transit frequency ω_T

$$A(\omega) = \frac{A_0}{1 + iA_0\omega/\omega_T} \quad (5.12)$$

into (5.11), we obtain with $A_0 \gg 1$:

$$\frac{U_o}{I_{ph}} = G(\omega) = -\frac{Z_F}{1 + (Z_F/A_0 Z_D) + i(\omega/\omega_T)(1 + (Z_F/Z_D))}. \quad (5.13)$$

After the insertion of

$$Z_D = R_D \parallel C_D = \frac{R_D}{1 + i\omega R_D C_D} \quad (5.14)$$

and

$$Z_F = R_F \parallel C_F = \frac{R_F}{1 + i\omega R_F C_F}, \quad (5.15)$$

the transimpedance is:

$$G(\omega) = \frac{R_F}{1 - (\omega^2/\omega_T)R_F(C_F + C_D) + i\omega[(1/\omega_T) + R_F(1/(R_D\omega_T) + C_F + C_D/A_0)]}. \quad (5.16)$$

For an ideal operational amplifier with $A_0 = \infty$ and $\omega_T = \infty$, (5.16) can be simplified considerably:

$$G(\omega) = -\frac{R_F}{1 + i\omega R_F C_F}. \quad (5.17)$$

This ideal transfer function obviously is that of a first order low pass filter. The -3 dB frequency, therefore, is $f_{3\text{dB}} = 1/(2\pi R_F C_F)$. This is not surprising for the ideal operational amplifier, when we look at Fig. 5.7. This assumption of the ideal operational amplifier, however, is too simple an approximation of the real behavior of transimpedance amplifiers. The gain-peaking which occurs often in practice, for instance, is not included in the ideal transfer function. Especially for photodiodes with large capacitance C_D , the ω^2 term in the denominator of (5.16) must not be neglected. For a more thorough analysis, we therefore introduce the following abbreviations: $a = (1/\omega_T) + R_F[(1/R_D\omega_T) + C_F + (C_D/A_0)]$ and $b = (R_F/\omega_T)(C_F + C_D)$. The transfer function for the real operational amplifier then is:

$$\frac{U_o}{I_{ph}} = G(\omega) = -\frac{R_F}{1 - \omega^2 b + i\omega a}. \quad (5.18)$$

The magnitude of the transfer function can be determined from (5.18) to be:

$$\frac{|U_o|}{|I_{ph}|} = |G(\omega)| = \frac{R_F}{\sqrt{(1 - \omega^2 b)^2 + (\omega a)^2}}. \quad (5.19)$$

Equation (5.19) can have a maximum, i.e. a gain-peak (GP), when $(1 - \omega^2 b) = 0$, i.e. when $\omega_{GP} = \sqrt{1/b}$. The frequency for which the gain-peaking occurs then is

$$f_{GP} = \frac{\omega_{GP}}{2\pi} = \frac{1}{2\pi\sqrt{b}} = \frac{1}{2\pi}\sqrt{\frac{\omega_T}{R_F(C_F + C_D)}}. \quad (5.20)$$

If the gain-peaking is not desired, it can be eliminated for a photodiode as a current source by increasing C_F , because in this case C_F has a stronger effect on a than on b . This elimination of the gain-peaking, however, is at the expense of a reduced -3 dB bandwidth (see Fig. 5.8).

For $C_F = 50$ fF (or less) a large gain-peak occurs at about 70 MHz. With $C_F = 100$ fF, the gain-peak is already almost suppressed. Increasing C_F to 200 fF suppresses the gain-peak completely. The -3 dB bandwidths for the three cases are about 120, 90, and 50 MHz, respectively. The case with $C_F = 200$ fF can practically be considered as over-compensated.

Fig. 5.8 Frequency response of an operational amplifier in transimpedance configuration for three different values of the feedback capacitance C_F ($I_{ph} = 10 \mu A$, $R_F = 20 k\Omega$, $R_D = 10^9 \Omega$, $\omega_T = 6.28 \text{ GHz}$ ($f_T = 1 \text{ GHz}$), $C_D = 1 \text{ pF}$, and $A_0 = 100$) calculated with (5.19)

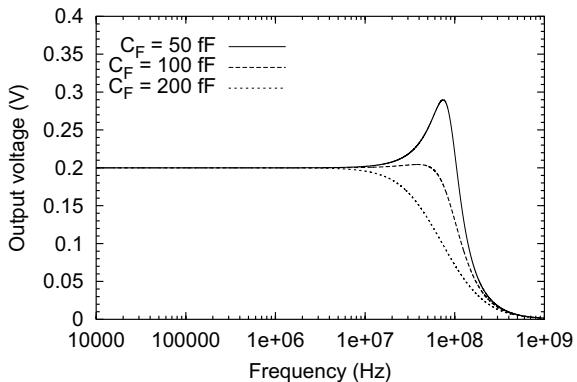
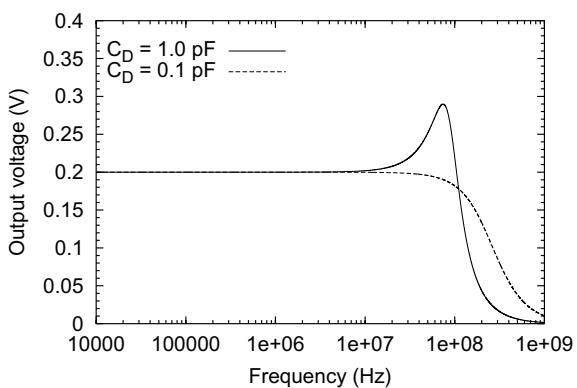
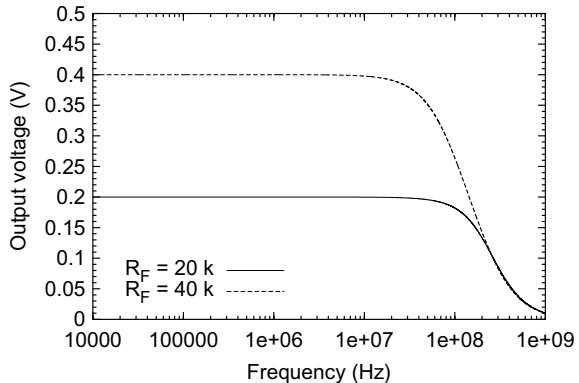


Fig. 5.9 Frequency response of an operational amplifier in transimpedance configuration for two different values of the photodiode capacitance C_D ($I_{ph} = 10 \mu A$, $R_F = 20 k\Omega$, $R_D = 10^9 \Omega$, $\omega_T = 6.28 \text{ GHz}$ ($f_T = 1 \text{ GHz}$), $C_F = 50 \text{ fF}$, and $A_0 = 100$) calculated with (5.19)



The influence of the depletion capacitance C_D of a photodiode on the frequency response is shown in Fig. 5.9. The gain-peak vanishes, when the capacitance of the photodiode is reduced from 1 to 0.1 pF . At the same time, the -3 dB bandwidth increases from about 120 to 180 MHz. We can conclude that a PIN photodiode with a capacitance of the order of 100 fF is advantageous compared to a double photodiode with a capacitance of the order of 1 pF . In order to understand the advantage of a transimpedance amplifier compared to a voltage follower configuration (compare with Fig. 1.16) with the same sensitivity, we calculate the bandwidth of the load resistor and of the photodiode capacitance $f_g = 1/(2\pi R_F C_D)$. For $R_F = 20 \text{ k}\Omega$ and $C_D = 100 \text{ fF}$, we obtain the bandwidth $f_g = 79.6 \text{ MHz}$ for the voltage follower configuration. This bandwidth of the voltage follower is much lower than the bandwidth of about 180 MHz for the transimpedance configuration with $R_F = 20 \text{ k}\Omega$ and $C_D = 100 \text{ fF}$. This example clearly demonstrates the advantage of the transimpedance amplifier. This advantage is due to the amplification factor $A(\omega)$, which reduces the effective photodiode capacitance in the transimpedance configuration with the help of the operational amplifier. Let us now return to the theory of the transimpedance amplifier.

Fig. 5.10 Frequency response of an operational amplifier in transimpedance configuration for two different values of the feedback resistor R_F ($I_{ph} = 10 \mu\text{A}$, $R_D = 10^9 \Omega$, $\omega_T = 6.28 \text{ GHz}$ ($f_T = 1 \text{ GHz}$), $C_D = 100 \text{ fF}$, $C_F = 50 \text{ fF}$, and $A_0 = 100$) calculated with (5.19)



The bandwidth can be determined from the condition

$$|G(\omega)| = G(\omega = 0)/\sqrt{2} = R_F/\sqrt{2}, \quad (5.21)$$

which leads to

$$(1 - \omega_g^2 b)^2 + (\omega_g a)^2 = 2. \quad (5.22)$$

The single positive, real solution of this equation is [14]

$$f_g = \frac{\omega_g}{2\pi} = \frac{1}{2\pi} \sqrt{\frac{1}{2b^2}(2b - a^2) + \sqrt{\frac{1}{4b^4}(2b - a^2)^2 + \frac{1}{b^2}}}. \quad (5.23)$$

The bandwidth of the transimpedance configuration is not simply proportional to $1/R_F$. Therefore, the frequency responses of the transimpedance configuration with $R_F = 20 \text{ k}\Omega$ and $R_F = 40 \text{ k}\Omega$ were calculated and compared in Fig. 5.10 in order to show the influence of R_F on the bandwidth. For $R_F = 40 \text{ k}\Omega$ the bandwidth reduces to about 100 MHz compared to 180 MHz for $R_F = 20 \text{ k}\Omega$.

5.4.2 Phase and Group Delay

The phase, in degrees, can be obtained in general from

$$\Phi(\omega) = \frac{180^\circ}{\pi} \arctan \left(\frac{\text{Im}(G(\omega))}{\text{Re}(G(\omega))} \right). \quad (5.24)$$

For the operational amplifier in transimpedance configuration, we obtain

Fig. 5.11 Phase response of an operational amplifier in transimpedance configuration for three different values of the feedback capacitance C_F ($I_{ph} = 10 \mu A$, $R_F = 20 k\Omega$, $R_D = 10^9 \Omega$, $\omega_T = 6.28 \text{ GHz}$ ($f_T = 1 \text{ GHz}$), $C_D = 1 \text{ pF}$, and $A_0 = 100$) calculated with (5.25)

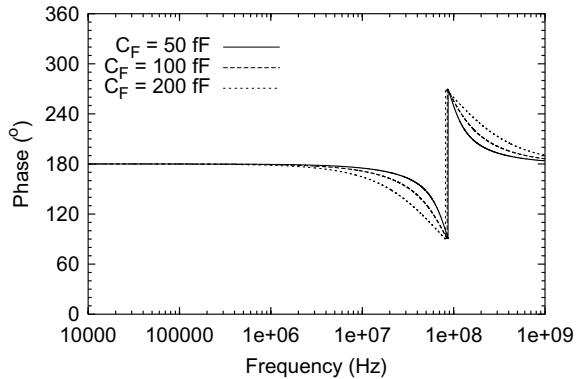
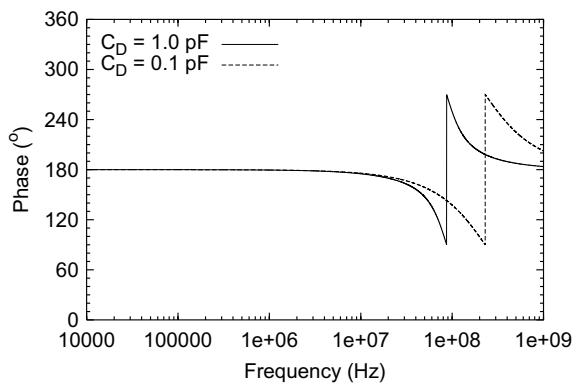


Fig. 5.12 Phase response of an operational amplifier in transimpedance configuration for two different values of the photodiode capacitance C_D ($I_{ph} = 10 \mu A$, $R_F = 20 k\Omega$, $R_D = 10^9 \Omega$, $\omega_T = 6.28 \text{ GHz}$ ($f_T = 1 \text{ GHz}$), $C_F = 50 \text{ fF}$, and $A_0 = 100$) calculated with (5.25)



$$\Phi(\omega) = -\frac{180^\circ}{\pi} \arctan \left(\frac{\omega a}{1 - \omega^2 b} \right) + 180^\circ. \quad (5.25)$$

In order to account for the inverted output signal, 180° are added for all frequencies. The pole in the argument of the arctan for $\omega = 1/\sqrt{b} = \omega_g$ causes a 180° step in the phase due to the periodicity of the arctan function. Figure 5.11 shows the phase response of the operational amplifier in transimpedance configuration for the same parameters as in Fig. 5.8.

The influence of the photodiode capacitance on the phase response can be seen in Fig. 5.12. The phase does not change as much for a lower photodiode capacitance than for a larger photodiode capacitance when the frequency increases. A PIN photodiode again is advantageous compared to a double photodiode.

For certain applications of amplifiers, the group delay has to be constant in a wide frequency range. We, therefore, will discuss the group delay t_{GD} , which we define here as $t_{GD} = -\pi/180^\circ \cdot \partial\Phi(\omega)/\partial\omega$, for the transimpedance amplifier. First we introduce the substitution $z = \omega a/(1 - \omega^2 b)$. Knowing that $\partial \arctan(z)/\partial z = 1/(1 + z^2)$, we obtain from (5.25):

Fig. 5.13 Group delay of an operational amplifier in transimpedance configuration for three different values of the feedback capacitance C_F ($I_{ph} = 10 \mu A$, $R_F = 20 k\Omega$, $R_D = 10^9 \Omega$, $\omega_T = 6.28 \text{ GHz}$ ($f_T = 1 \text{ GHz}$), $C_D = 1 \text{ pF}$, and $A_0 = 100$) calculated with (5.26)

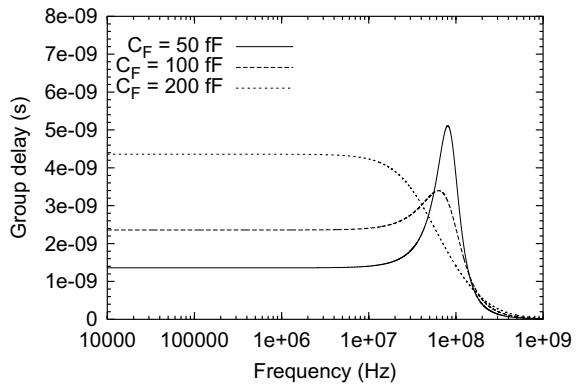
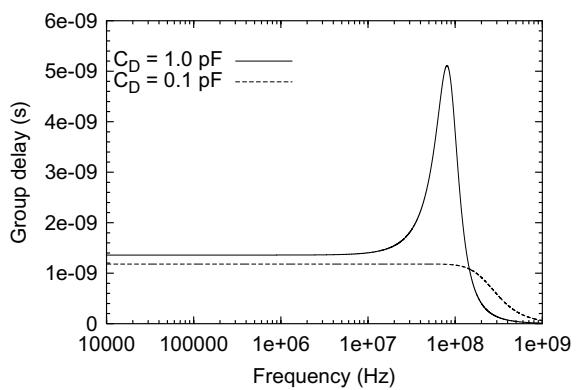


Fig. 5.14 Group delay of an operational amplifier in transimpedance configuration for two different values of the photodiode capacitance C_D ($I_{ph} = 10 \mu A$, $R_F = 20 k\Omega$, $R_1 = 10^9 \Omega$, $\omega_T = 6.28 \text{ GHz}$ ($f_T = 1 \text{ GHz}$), $C_F = 50 \text{ fF}$, and $A_0 = 100$) calculated with (5.26)



$$t_{GD} = \frac{a(1 + b\omega^2)}{(1 - b\omega^2)^2 + (a\omega)^2}. \quad (5.26)$$

Figure 5.13 shows the group delay for the three cases depicted in Fig. 5.8. There is a peak in the group delay at f_{gp} for $C_F = 50 \text{ fF}$ and $C_F = 100 \text{ fF}$. This peak is suppressed with $C_F = 200 \text{ fF}$ leading to a decrease already at rather low frequencies. The optimum C_F value for a good group delay behavior lies between 100 and 200 fF.

The influence of the photodiode capacitance on the group delay is illustrated in Fig. 5.14. For the large capacitance of a double photodiode of the order of 1 pF, a large peak results in the group delay. For the low capacitance of a PIN photodiode of the order of about 100 fF, a constant group delay is obtained for frequencies of up to 100 MHz. The PIN photodiode again is advantageous compared to the double photodiode.

5.4.3 Stability and Compensation

Above it was shown that a transfer function with two poles is obtained for the transimpedance amplifier. For such a function large values of C_D may lead to a so-called gain-peaking, an overshoot in the frequency response curve at high frequencies. Oscillations may result for a strong gain-peaking. A detailed analysis [15] leads to a value of

$$\begin{aligned} C_F &= \frac{\sqrt{2A_0 R_F C_D \omega_c} - (1 + \omega_c R_F C_D)}{R_F \omega_c A_0} \\ &\approx \sqrt{\frac{2C_D}{R_F \omega_c A_0}} - \frac{C_D}{A_0} \end{aligned} \quad (5.27)$$

for the compensation capacitor, which is necessary in order to suppress gain-peaking. The symbol ω_c is the -3 dB frequency of the amplifier; i.e. the gain of the amplifier can be expressed by $A(\omega) = A_0/(1 + i\omega/\omega_c)$. Usually (5.27) leads to unnecessarily high values of C_F [16]. If a phase margin of 45° is required, a thorough analysis of the transfer function [15] leads to

$$\begin{aligned} C_F &= \frac{\sqrt{\frac{1}{\sqrt{2}} A_0 R_F C_D \omega_c} - (1 + \omega_c R_F C_D)}{R_F \omega_c A_0} \\ &\approx \sqrt{\frac{C_D}{\sqrt{2} R_F \omega_c A_0}} - \frac{C_D}{A_0}. \end{aligned} \quad (5.28)$$

In practical transimpedance amplifier implementations, for the feedback capacitance a value between those specified by (5.27) and (5.28) should be chosen.

5.4.4 Bandwidth of Transistor Transimpedance Amplifier Circuit

As we saw above, there is a too simple expression for the bandwidth of a transimpedance amplifier taking into account only the feedback resistor and the feedback capacitor: $f_{3\text{dB}} = 1/(2\pi R_F C_F)$. The bandwidth of a transimpedance amplifier can be influenced by other quantities. Let us assume a simple transistor transimpedance amplifier to investigate additional factors being important for its bandwidth. The circuit diagram of the simple transistor transimpedance amplifier is shown in Fig. 5.15. In the following we will derive an equation for its bandwidth, which considers the operating point of this amplifier.

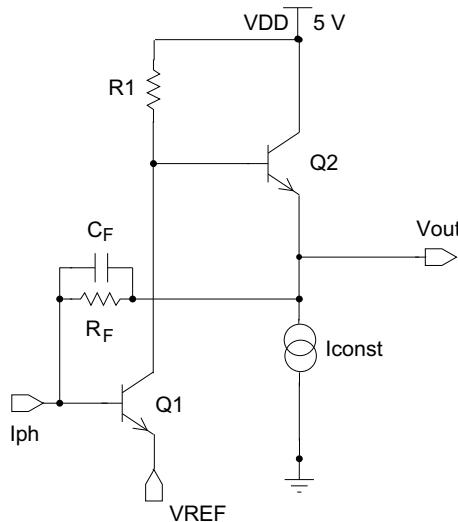


Fig. 5.15 Circuit diagram of a two-transistor transimpedance amplifier [15]

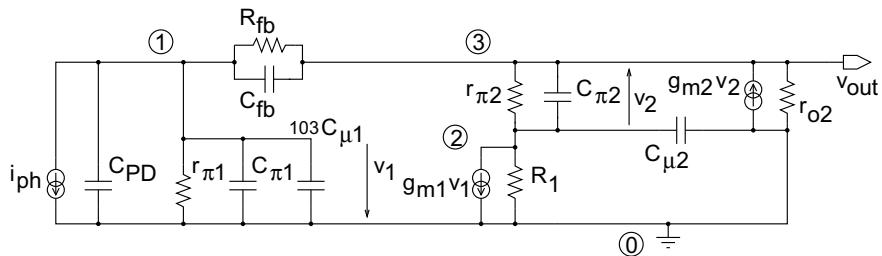


Fig. 5.16 Small-signal equivalent circuit of the first stage of the transimpedance amplifier depicted in Fig. 6.85 [15]. Node numbers are placed within circles

In Fig. 5.16 a simplified small signal equivalent circuit of the transimpedance amplifier is depicted. Compared to R_1 , the resistors r_{o1} , r_{c1} as well as the collector-substrate-capacitance C_{CS1} are negligible. Applying the Miller-theorem, $C_{\mu 1}$ can be converted to $C_M = C_{\mu 1} (1 + g_{m1} R_1) \approx 103 C_{\mu 1}$ ($g_{m1} = 1.92 \text{ mS}$, $R_1 = 54.2 \text{ k}\Omega$ for the amplifier shown in Fig. 6.85 [15]) parallel to C_{B1} . Also r_{b2} , C_{CS2} , r_{b1} and r_{c2} need not be taken into consideration for the calculations.

For the derivation of the bandwidth, the matrix equation

$$\underbrace{\begin{pmatrix} -i_{ph} \\ -g_{m1} v_{n1} \\ g_{m2} v_{n2} \end{pmatrix}}_{\mathcal{I}} = \mathcal{M} \cdot \underbrace{\begin{pmatrix} v_{n1} \\ v_{n2} \\ v_{out} \end{pmatrix}}_{\mathcal{V}} \quad (5.29)$$

is set up according to the node potential method, where v_{out} is identical with v_{n3} . Here the resistors r_{B1} , r_{B2} and r_{o2} are neglected due to their large values. $C_{\mu 2}$ is in the FF range and is also neglected.

In this circuit the matrix \mathcal{M} can be written as

$$\mathcal{M} = \begin{pmatrix} \mathcal{M}_{11} & 0 & -\frac{1+i\omega R_F C_F}{R_F} \\ 0 & i\omega C_{B2} + G_1 & -i\omega C_{B2} \\ -\frac{1+i\omega R_F C_F}{R_F} & -i\omega C_{B2} & \mathcal{M}_{33} \end{pmatrix}, \quad (5.30)$$

with $\mathcal{M}_{11} = i\omega (C_D + C_{\pi 1} + (1 + g_{m1} R_1) C_{\mu 1}) + (1 + i\omega R_F C_F)/R_F$, $\mathcal{M}_{33} = i\omega C_{B2} + \frac{1+i\omega R_F C_F}{R_F}$ and $G_1 = 1/R_1$. The voltages v_{n1} , v_{n2} , and v_{out} point from nodes 1 to 3 to the ground node 0 (see Fig. 5.16).

Using matrix

$$\mathcal{D} = \begin{pmatrix} 0 & 0 & 0 \\ -g_{m1} & 0 & 0 \\ 0 & g_{m2} & 0 \end{pmatrix}$$

the relationship

$$\mathcal{V} = (\mathcal{M} - \mathcal{D})^{-1} \cdot (-i_{\text{ph}} \ 0 \ 0 \ 0)^T \quad (5.31)$$

can be obtained.

Even now the complete transfer function $v_{\text{out}}/i_{\text{ph}}$ is too complicated for a complete analytical analysis. Therefore, the poles and zeros are calculated numerically. From the pole/zero diagram in Fig. 5.17 it can be seen that the zeros are located at $-56.6 \cdot 10^9 \frac{1}{\text{s}}$ and at $144.8 \cdot 10^9 \frac{1}{\text{s}}$. The poles can be found at $-0.47 \cdot 10^9 \frac{1}{\text{s}}$, $-(0.91 + i19.9) \cdot 10^9 \frac{1}{\text{s}}$ and at $-(0.91 - i19.9) \cdot 10^9 \frac{1}{\text{s}}$ [15]. Since the pole at $-0.47 \cdot 10^9 \frac{1}{\text{s}}$ is below the frequency of the other pole by a factor of about two and since the values for the zeros are comparatively high, it is safe to assume that this pole is dominant. Circuit simulations with a lowpass having the bandwidth f_1 and a second lowpass with the bandwidth $f_2 = 2 \times f_1$ in series resulted in a total bandwidth of $0.8 \times f_1$. The error caused by neglecting the second pole here, therefore, is about 20%.

This means that in the denominator of the transfer function which can be obtained by solving (5.31), all terms containing higher order of the frequency ω can be eliminated. The remaining terms lead to the expression

$$f_{-3 \text{ dB}} = \frac{1}{2\pi \left(R_F C_F + \frac{C_{B2}}{g_{m2}} + \frac{1+g_{m2} R_F}{(1+g_{m1} R_1)g_{m2}} C_f \right)} \quad (5.32)$$

with $C_f = (C_D + (1 + g_{m1} R_1) C_{\mu 1} + C_{B1})$. It can be seen that the bandwidth depends on the values for the feedback capacitance C_F , on the resistor R_F as well as on the transistor parameters g_{m1} , g_{m2} , $C_{\mu 1}$, C_{B1} , and C_{B2} . In the same way the value of the photodiode capacitance C_D has to be taken into consideration in the equation. This means that when the photodiode area becomes lower, the bandwidth increases. The

Fig. 5.17 Pole/zero diagram of the transimpedance amplifier

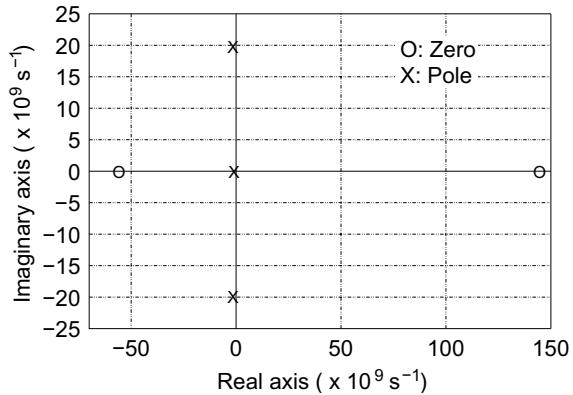
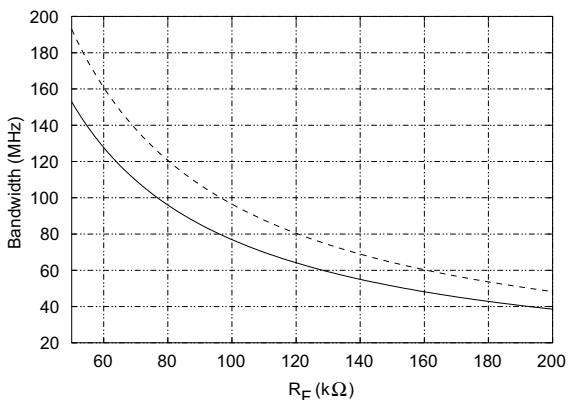


Fig. 5.18 Possible bandwidths of the transistor transimpedance amplifier as a function of R_F according to (5.32) [solid line] and the simple expression $f_{3\text{dB}} = 1/(2\pi R_F C_F)$ [dashed line] for $C_F = 15 \text{ fF}$ and $C_D = 210 \text{ fF}$ [15]



most important parameters are photodiode capacitance C_D , R_F , and C_F for a fixed operating point of the transistor amplifier. Figure 5.18 shows the actual bandwidth according to (5.32) in comparison with that calculated from the simple expression. Equation (5.32) considering the operating point of the TIA in Fig. 6.85 leads to about 25% lower values than expected from the simple expression.

Inserting the transistor parameters for the nominal case taken from a circuit simulation at the operating point into (5.32), a bandwidth of 76 MHz can be calculated for the circuit in Fig. 6.85 in high sensitivity, i.e. switch S_1 open. A numerical postlayout simulation at a temperature of 25 °C and nominal model parameters revealed a 3 dB frequency of 68 MHz [15].

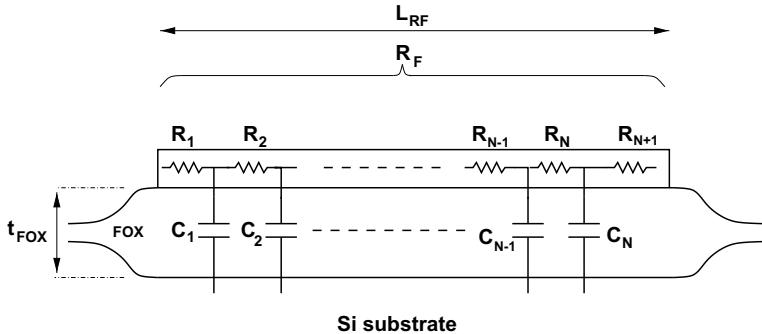


Fig. 5.19 R-C chain of an integrated polysilicon resistor

5.4.5 Bandwidth Limit of Integrated Transimpedance Amplifiers

In the following, we will derive an estimate for the maximum bandwidth of an integrated transimpedance amplifier resulting from \$R_F\$ and its parasitic capacitance. An ideal operational amplifier is implicitly assumed. Furthermore it is presumed that \$C_F\$ is not needed for compensation, i.e. that the parasitic capacitance of \$R_F\$ is sufficient for compensation.

In analog integrated circuits, polysilicon resistors are used. These polysilicon resistors are fabricated on top of an oxide layer (field oxide, FOX) on the silicon substrate. It is therefore necessary to consider the polysilicon resistor like a chain of RC elements (see Fig. 5.19). The feedback resistor \$R_F\$, therefore, has to be split in \$R_1 = 0.5R_F/N\$, \$R_i = R_F/N\$ (\$i = 2 \dots N\$), \$R_{N+1} = 0.5R_F/N\$ and the total parasitic capacitance of \$R_F\$ has to be split in \$C_i = C_{R_F}/N\$, where \$C_{R_F} = A_{R_F}/(\epsilon_{SiO_2}\epsilon_0 t_{FOX})\$ with the area \$A_{R_F} = L_{R_F} \cdot W_{R_F}\$ of \$R_F\$. The value of \$R_F\$ can be calculated from the sheet resistance \$R_{\square}^{Poly}\$ and the length \$L_{R_F}\$ and the width \$W_{R_F}\$ of \$R_F\$: \$R_F = R_{\square}^{Poly} \cdot L_{R_F} / W_{R_F}\$ assuming a linear polysilicon resistor. When \$R_F\$ is meandered, for the corner squares, \$R_{\square}^{Poly} \cdot 0.56\$ has to be considered and \$A_{R_F}\$ has to be determined in a more complicated way. For simplicity, we, however, will assume a linear polysilicon resistor.

For the integrated resistor, the parasitic capacitance increases when the resistor value has to be increased (for \$W_{R_F} = \text{constant}\$, \$L_{R_F} \propto R_F\$ and \$A_{R_F} \propto R_F\$) in order to achieve a larger sensitivity \$S\$ of the transimpedance amplifier. Let us, for simplicity, assume the time constant \$\tau_{R_F} = R_F \cdot C_{R_F}\$ for the polysilicon resistor. Then, when \$R_F \propto S\$ is increased, \$C_{R_F}\$ increases proportional to \$R_F\$ and to \$S\$, resulting in \$\tau_{R_F} \propto S^2\$. This leads to the conclusion that the bandwidth is proportional to \$1/S^2\$ for an integrated polysilicon resistor in a bipolar, CMOS, or BiCMOS transimpedance amplifier.

In order to illustrate this derived dependence of the bandwidth on \$S\$, circuit simulations have been performed with an R-C chain including \$N = 10\$ elements for

Table 5.1 Simulated bandwidths of R-C chain for an integrated polysilicon resistor

R_{\square} (Ω_{\square})	$f_{3\text{dB}}(R_F = 10\text{k}\Omega)$ (MHz)	$f_{3\text{dB}}(R_F = 20\text{k}\Omega)$ (MHz)	$f_{3\text{dB}}(R_F = 40\text{k}\Omega)$ (MHz)
100	980	245	61
1000	9800	2450	610

$R_{\square}^{\text{Poly}} = 100$ and $1000\Omega_{\square}$ with $R_F = 10$, 20, and $40\text{k}\Omega$ for a polysilicon width $W_{R_F} = 2\mu\text{m}$ and $C_{R_F}/A_{R_F} = 0.1\text{fF}/\mu\text{m}^2$. The fringe capacitance of the polysilicon resistor has been neglected in this example. The -3 dB bandwidths obtained are listed in Table 5.1.

These results show that for $R_{\square}^{\text{Poly}} = 100\Omega_{\square}$, polysilicon resistors with values of 10 and $20\text{k}\Omega$ will not limit the bandwidths of integrated transimpedance amplifiers. For a value of $40\text{k}\Omega$, however, the polysilicon resistor reduces the bandwidth to 61 MHz i.e. below the value of 90 MHz, which was obtained for a BiCMOS OEIC for optical storage systems [17]. For $R_{\square}^{\text{Poly}} = 1000\Omega_{\square}$, finally, polysilicon resistors with values of up to $40\text{k}\Omega$ possess larger -3 dB bandwidths than common integrated high-speed operational amplifiers and will, therefore, not limit the bandwidths of integrated transimpedance amplifiers.

5.4.6 New π -Model for Integrated Transimpedance Amplifier

A transmission-line approach was presented to derive a new π -model for integrated transimpedance amplifiers [18]. Due to their strong capacitive coupling to substrate ground, polysilicon resistors used in the feedback circuit contribute to the frequency response of the overall amplifier. Limitations in bandwidth, signal distortion and even instability may result. A novel, exact model of the resistor based on the transmission-line theory was suggested to describe the behavior of the overall transimpedance amplifier. A simple and descriptive approximation model, derived from the exact one, was used to find design formulas to optimize the overall amplifier performance. Though possible in general, this was demonstrated in case of an idealized amplifier with high gain, both using the exact and the simplified model to show its usefulness. The model was also verified for a real amplifier by comparison of simulated results for the approximation model and for the exact grounded uniformly distributed RC-line (URC) model.

OEICs are increasingly needed for optical storage (OS) systems like CD-ROM, Digital-Versatile-Disk (DVD) and Digital-Video-Recording (DVR) as well as for opto-electrical front-ends in fiber receivers. In both cases, the gain-bandwidth product, i.e. the transimpedance-bandwidth product is an important design parameter. In practice, the feedback resistors used in TransImpedance Amplifiers (TIAs) have values in the order of $100\text{k}\Omega$ for OS-OEICs down to the order of $1\text{k}\Omega$ for fiber receivers,

while the bandwidth reaches from below 100 MHz to several GHz. Made of polysilicon, these integrated resistors have considerable stray capacitances to ground, i.e. they depend strongly on frequency. The parasitic stray capacitance of 100 k Ω feedback resistors in OS-OEICs has to be considered, if signal frequencies reach 100 MHz or more even when the sheet resistance of the (high-resistivity) polysilicon is on the order of 1 k Ω (see last section). Fiber receivers often have to be realized for system-on-chip applications in digital deep-sub- μm CMOS or in low-cost digital CMOS technologies where only gate polysilicon with a sheet resistance of much less than 100 Ω_{\square} is available. Therefore, the parasitic capacitance of feedback resistors in the order of several k Ω also has to be considered in fiber receivers for Gb/s-application. Capacitive coupling has to be taken into account, and its negative effects on stability are generally reduced using a feedback capacitor in parallel with the feedback resistor.

Transmission-line approaches up to now only were performed for metallic interconnects in chips. In [19], a so-called single grounded uniformly distributed RC line was described for integrator applications using a two-port formulation. An improved T-model and an improved II-model consisting of one resistor and two capacitors was suggested for the modeling of on-chip interconnects [20]. A π model also consisting of one resistor and two capacitors was suggested to model the effective capacitance for the RC interconnect of CMOS gates [21]. An admittance parameter formulation was used to describe a capacitive double layers uniformly distributed RC line [22].

The goal of this section is to analyze the overall TIA taking the frequency-dependent feedback resistor into account. Using the transmission-line model, a simple approximation for the integrated feedback resistor, a novel π equivalent circuit will be derived. A very simple approximation from this model implying only a resistor and an inductor makes it possible to understand the basic behavior of the feedback circuit. A comparison with the exact model is also made. The new π equivalent circuit model as well as its simple approximation allow the optimization of an integrated transimpedance amplifier independent of and before using a circuit simulator.

Modeling Amplifier and Feedback Network

To study the amplifier with feedback network in general, it is necessary to introduce at first the major terms and parameters describing the nature of amplifier and feedback network. Figure 5.20a shows a simple transimpedance amplifier consisting of the photodiode's current source $I(s)$ in parallel with the photodiode's capacitance C_D , the amplifier (with finite complex gain $A(s)$, with the input impedance $Z_{in}(s)$, and with the output impedance $Z_{out}(s)$), and the feedback resistor R_F described by its y-parameters $Y(s)$ in parallel with the feedback capacitor C_F . $V_{in}(s)$ and $V_{out}(s)$ are the input and output voltages, respectively, both depending on the complex frequency s . The behavior of the whole amplifier can now be described using an ideal amplifier shown in Fig. 5.20b and the transimpedance $Z(s)$

$$Z(s) = \frac{1}{\frac{y_{11m}(s)}{A(s)} - y_{12m}(s)} , \quad (5.33)$$

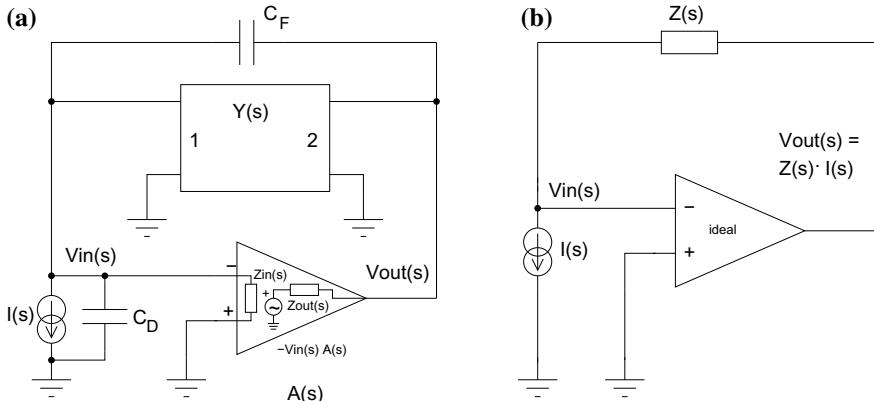


Fig. 5.20 Transimpedance amplifier consisting of real amplifier and modelled, non-ideal resistor (a). Equivalent representation with ideal amplifier and the transimpedance $Z(s)$ (b)

with the modified y-parameters $Y_m(s)$, consisting of the feedback resistor's y-parameters $y(s)$, the feedback capacitor C_F , the photodiode capacitance C_D and the amplifier input impedance $Z_{in}(s)$.

The amplifier's output impedance $Z_{out}(s)$ is assumed to be small compared to the feedback input impedance (which acts as a load). This means that

$$|Z_{out}(s)| \ll \frac{1}{|y_{22m}(s) - \frac{y_{21m}(s)}{A(s)}|} \quad (5.34)$$

Equivalent Circuit Representation for Polysilicon Resistor

The polysilicon resistor has typically a width of a few micrometers and a thickness of a few hundred nanometers. The field oxide is about $0.4\text{--}0.5 \mu\text{m}$ thick. The resistor is covered by several micrometer thick oxide and passivation layers. The length l of the polysilicon resistor is of the order $10\text{--}100$ times longer than its widths w . Therefore, the polysilicon resistor behaves like a lossy micro-strip line in a nearly homogeneous medium. With the energy concentrated in the field oxide and its distribution being independent from frequency up to several GHz (due to the small dimensions compared to wavelength), the capacitance of the field oxide is constant. The large (intended) series resistance is the major reason for strong dispersion and frequency dependency. Because $l \gg w$, the resistor can be considered as a one-dimensional lossy transmission line lying between its connections with an accuracy similar to that of micro-strip lines of a few percent [23]. From transmission-line theory, the general form for line impedance Z_w and the propagation constant γ are known as [23, 24]

$$Z_w(s) = \sqrt{\frac{R' + sL'}{G' + sC'}} \quad \text{and} \quad (5.35)$$

$$\gamma(s) = \sqrt{(R' + sL') \cdot (G' + sC')} , \quad (5.36)$$

with R' and L' representing the resistance and inductance per length unit, respectively, and G' and C' denoting the conductance and capacitance to ground per length unit, respectively. Taking into account that for a polysilicon resistor realized in a technology with smallest structure sizes of about $1\text{ }\mu\text{m}$, $R' \approx 1\text{ k}\Omega/\mu\text{m}$, $L' \approx 300\text{ fH}/\mu\text{m}$, $C' \approx 0.2\text{ fF}/\mu\text{m}$, and $G' < 1\text{ nS}/\mu\text{m}$, it follows that $|sL'| \ll |R'|$ and $|G'| \ll |sC'|$ up to several GHz. A series resistance between C' and ground caused by the finite substrate conductivity can be neglected for frequencies below 10 GHz, typically [18]. Therefore, it is possible to consider the polysilicon resistor as a grounded uniformly distributed RC-line (URC-line). Introducing the time constant τ

$$\tau = R' \cdot C' \cdot l^2 , \quad (5.37)$$

the normalized frequency Ω

$$\Omega = \omega \cdot \tau , \quad (5.38)$$

as well as the normalized complex frequency S

$$S = s \cdot \tau , \quad (5.39)$$

the Y-parameters of the polysilicon resistor are [24]

$$Y(S) = \frac{1}{R' \cdot l} \cdot \begin{pmatrix} \frac{\sqrt{S}}{\tanh(\sqrt{S})} & -\frac{\sqrt{S}}{\sinh(\sqrt{S})} \\ -\frac{\sqrt{S}}{\sinh(\sqrt{S})} & \frac{\sqrt{S}}{\tanh(\sqrt{S})} \end{pmatrix} . \quad (5.40)$$

This is the exact frequency representation of a polysilicon resistor with Y-parameters. The matrix is symmetric. It is easily shown that the absolute value of all four elements in brackets y_{11} , y_{12} , y_{21} and y_{22} converge to $1/(R' \cdot l)$ if S comes close to zero. The element's poles lie on the negative real axis, their zeros in infinity.

π Equivalent Circuit — Exact Form and Approximation

The new π equivalent circuit (see Fig. 5.21b) was chosen for two reasons: (i) it is easily created from the Y-matrix, and (ii) further components can simply be added in parallel (e.g. the feedback capacitor, see below). Figure 5.21a shows the exact π equivalent circuit using frequency dependent impedances. The frequency-dependence of these impedances $Z_1(S)$ and $Z_2(S)$ is rather complicated, because both are irrational functions of S . Therefore, an exact, but simple network representation with only a few components being valid for all frequencies is not existing [18].

In Fig. 5.21b a simple network with lumped elements and constant (i.e. frequency independent) component values is used. The simple network is equivalent to the exact one for DC and at low frequencies. The component values are determined in the following:

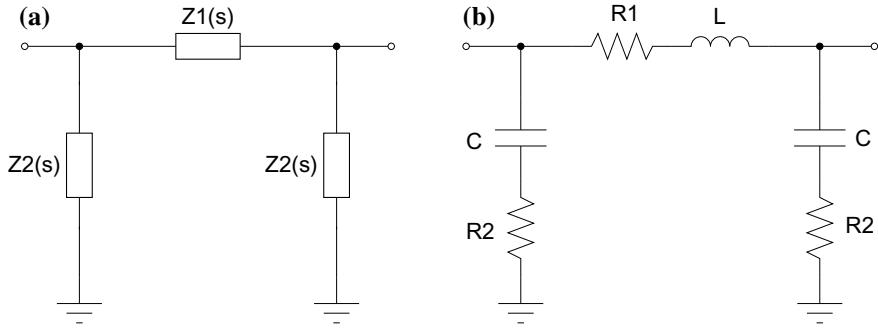


Fig. 5.21 Polysilicon resistor in exact π equivalent circuit representation (a) and in approximated π equivalent circuit representation (b)

Using (5.40), it follows that

$$Z1(S) = R' \cdot l \cdot \frac{\sinh(\sqrt{S})}{\sqrt{S}} \text{ and} \quad (5.41)$$

$$Z2(S) = R' \cdot l \cdot \frac{\sinh(\sqrt{S})}{\sqrt{S} \cdot (\cosh(\sqrt{S}) - 1)} . \quad (5.42)$$

Now the expressions for $Z1(S)$ and $Z2(S)$ have to be simplified using the truncated taylor series expansion for hyperbolic sine and hyperbolic cosine. From (5.41), $Z1(S)$ can be written as

$$Z1(S) = R' \cdot l \cdot \frac{\sum_{k=0}^{\infty} \frac{(\sqrt{S})^{2k+1}}{(2k+1)!}}{\sqrt{S}} \text{ or} \quad (5.43)$$

$$Z1(S) = R' \cdot l \cdot \left(1 + \frac{S}{3!} + \frac{S^2}{5!} + \dots \right) . \quad (5.44)$$

Truncating (5.44) after the linear term of S and using (5.37) and (5.39), one finds $Z1(S)$ consisting of a resistor $R1$ in series with an inductor L with their values

$$R1 = R' \cdot l \text{ and} \quad (5.45)$$

$$L = \frac{R' \cdot l}{6} \cdot \frac{S}{s} = \frac{R'^2 \cdot C' \cdot l^3}{6} . \quad (5.46)$$

Similarly, $Z2(S)$ can be expressed from (5.42) as

$$Z2(S) = R' \cdot l \cdot \frac{\sum_{k=0}^{\infty} \frac{(\sqrt{S})^{2k+1}}{(2k+1)!}}{\sqrt{S} \cdot \left(\sum_{m=0}^{\infty} \frac{(\sqrt{S})^{2k}}{(2k)!} - 1 \right)} \quad (5.47)$$

or

$$Z2(S) = R' \cdot l \cdot \frac{1 + \frac{S}{3!} + \frac{S^2}{5!} + \dots}{\frac{S}{2!} + \frac{S^2}{4!} + \dots} \quad (5.48)$$

Truncating (5.48) after the linear terms and dividing by S finally leads to

$$Z2(S) \cong 2 \cdot R' \cdot l \cdot \left(\frac{1}{S} + \frac{1}{6} \right) . \quad (5.49)$$

$Z2(S)$ consists of a capacitor C in series with a resistor $R2$ according to

$$C = \frac{1}{2 \cdot R' \cdot l} \cdot \frac{S}{s} = \frac{C' \cdot l}{2} \text{ and} \quad (5.50)$$

$$R2 = \frac{R' \cdot l}{3} . \quad (5.51)$$

Figure 5.21b shows the final circuit. A slightly better agreement between approximation and exact solution, however, was obtained with the following modified expression, found with the help of MATHCAD simulations [18]:

$$R2 = \frac{R' \cdot l}{6} . \quad (5.52)$$

The approximation for both impedances is better than 10%, if the normalized frequency Ω does not exceed a value of 4. Keeping in mind that Ω increases with the time constant τ according to (5.38), the latter turns out to be a central design parameter, which has to be kept small. Consequences for the physical design parameters of the polysilicon resistor will be discussed below.

Stability

In general, returning to (5.33), the whole amplifier is stable, if the transimpedance $Z(s)$ has no poles in the right half-plane of s . This is equivalent to the denominator of (5.33) having its zeros only in the left half-plane of s .

To give an imagination, a very simple case is studied. It is assumed that there are no photodiode capacitance C_D , no feedback capacitance C_F , and that the amplifier has finite, but frequency independent gain A_0 (i.e. no phase change). Amplifier input impedance $Z_{in}(s)$ should be infinite, while output impedance $Z_{out}(s)$ is zero. Then, using the normalized frequency S from (5.39), (5.33) may be written as

$$Z(S) = \frac{1}{\frac{y_{11}(S)}{A_0} - y_{12}(S)} . \quad (5.53)$$

Setting the denominator of (5.53) equal to zero to find the poles of (5.53) and using (5.40) leads to

$$\frac{\sqrt{S}}{\tanh(\sqrt{S}) \cdot A_0} + \frac{\sqrt{S}}{\sinh(\sqrt{S})} = 0 \quad (5.54)$$

or

$$\cosh(\sqrt{S}) + A_0 = 0 . \quad (5.55)$$

Solving (5.55) for A_0 leads to the following: The stability limit with two zeros of (5.55) lying on the imaginary axis is reached if the gain is

$$A_{0,\max} = \cosh(\pi) = 11.6 \quad (5.56)$$

at a frequency of

$$S_{\max} = \pm j \cdot 2\pi^2 . \quad (5.57)$$

Critical damping leading to a step response without ringing (see also below) is accomplished if (index “c” for critical)

$$A_{0,c} = 1 \quad (5.58)$$

at a frequency of

$$S_c = -\pi^2 . \quad (5.59)$$

Further poles of (5.53) lie on the negative real axis with the next one $4 \cdot \pi^2$ apart from the dominant one and thus being neglected. Therefore the gain has to lie between the limits given by (5.56) and (5.58) corresponding to a LRC resonant circuit reaching from critical damping to undamped oscillations. Because of the small gain necessary for damped oscillations, the result is rather unsatisfying. If the amplifier’s gain $A(s)$ is frequency dependent, higher gains are also possible. Better results are found using a feedback capacitor described in the next section.

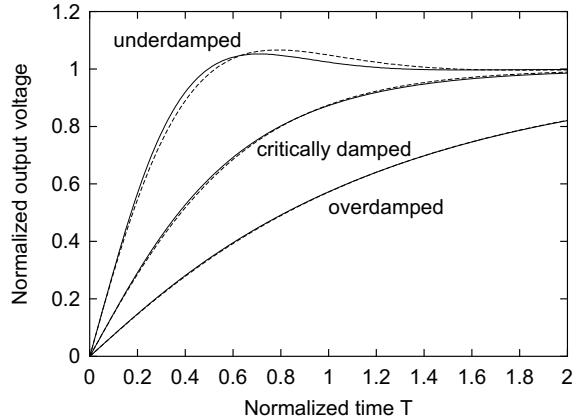
Optimum Feedback Capacitor

From Fig. 5.21b, it can be seen that the transfer impedance $Z1(\Omega)$ shows an inductive behavior. This leads to phase differences between photodiode current $I(s)$ and output voltage $V_{out}(s)$ of an OEIC amplifier. To compensate this and to maintain stability, the effect of a feedback capacitor will be investigated. To obtain an upper performance limit, the optimum feedback capacitor in terms of output voltage rise time and overshoot will be determined for an idealized large-gain large-bandwidth amplifier. Because of the large gain $A(s)$, the transimpedance $Z(s)$ only consists of $Z1(s)$ representing the polysilicon resistor in parallel with C_F , and C_D has no effect.

Using the approximation for $Z1(s)$, the feedback circuit becomes a simple LRC-resonant circuit having no ringing at critical damping (index “c”) for

$$C_c = \frac{4 \cdot L}{R^2} \quad (5.60)$$

Fig. 5.22 Step response of an ideal (large gain) transimpedance amplifier with three different dampings depending on the feedback capacitor C_F : underdamped ($C_F = 0.5 \cdot C_{F,c}$), critically damped ($C_F = C_{F,c}$) and overdamped ($C_F = 2 \cdot C_{F,c}$). Both the exact solution (solid line) and the approximation (dashed line) are shown [18]



Applied to our case and taking the actual expressions for the components from (5.45) and (5.46), the result from (5.60) is

$$C_{F,c} = \frac{2}{3} \cdot C' \cdot l . \quad (5.61)$$

C_F is necessary even in case of infinite gain (see Fig. 5.22).

PSPICE simulations show that the rise time t_r (measured from 10 to 90% of the final value) of a series resonant circuit depending on the capacitance C around critical damping is approximately

$$t_r = \tau \cdot \left(\frac{C_F}{C_{F,c}} \right)^{1.5} . \quad (5.62)$$

The 3 dB-bandwidth B can be estimated from the well-known equation

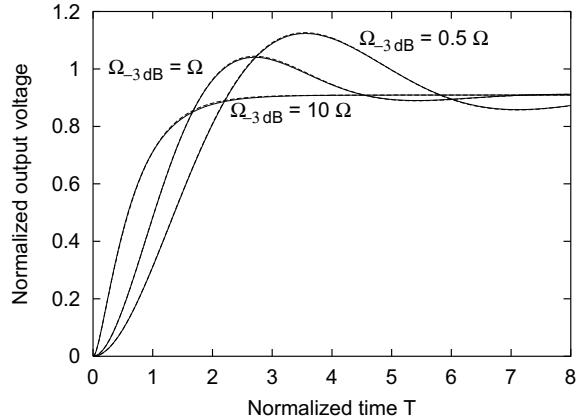
$$B \cong \frac{0.35}{t_r} = \frac{0.35}{\tau} \cdot \left(\frac{C_{F,c}}{C_F} \right)^{1.5} . \quad (5.63)$$

The accuracy of (5.62) and (5.63) is better than 10% for $C_F = 0.5 \cdot C_{F,c}$ to $C_F = 1.5 \cdot C_{F,c}$ and better than 5% for $C_F = C_{F,c}$. Improvements in bandwidth are only possible if (little) overshoot is allowed. Therefore, the simplified model is useful within the normal range of applications with no or a small amount of ringing.

In practice, using finite gain amplifiers with finite bandwidth, a lower or higher value for C_F may be necessary and C_D plays a role. Figure 5.23 shows an example in such a more real context with finite amplifier gain and bandwidth (Ω_{-3dB} is the normalized -3dB -bandwidth) in presence of the photodiode capacitance C_D .

Because of finite gain, now the complete model of Fig. 5.21b is used. The step responses shown in this figure were created using PSPICE, whereby the “exact” solution was calculated using an RC-chain of 20 elements. The example is for demon-

Fig. 5.23 Step response of a transimpedance amplifier with finite gain $A_0 = 10$, a photodiode capacitance $C_D = 5 \cdot C'l$ and a feedback capacitor $C_F = 0.5 \cdot C_{F,c}$ shown for three different amplifier bandwidths. Differences between exact solution (solid line) and the approximation (dashed line) are not visible [18]



stration of the accuracy of the new π -model and is not optimized in terms of speed or ringing.

Design Requirements for Polysilicon Resistor

The resistor made of polysilicon with the DC-value $R = R'l$, the length l and the width w is characterized by the so-called “resistance per square unit”, sheet resistance, R_\square or R_{SQ} , which has the dimension of Ohms per square. The resistor is insulated from the conducting substrate ground via a field oxide of thickness d having the relative dielectric constant ϵ_r .

Remembering the key design parameter, the time constant τ (5.37),

$$\tau = R' \cdot C' \cdot l^2 = R' \cdot l \cdot C' \cdot l , \quad (5.64)$$

the product $C' \cdot l$ has to be minimized. The DC-resistance is

$$R = R' \cdot l = R_{SQ} \cdot \frac{l}{w} , \quad (5.65)$$

while the capacitance C is

$$C = C' \cdot l = \epsilon_0 \cdot \epsilon_r \cdot \frac{(w + \Delta w) \cdot l}{d} , \quad (5.66)$$

with Δw taking the edge capacitance of the polysilicon resistor into account and ϵ_0 denoting the dielectric constant of vacuum. To obtain a required resistor R with a minimum width w , given in the design rules, and a R_{SQ} , specified for the chosen process, the resistor's length l is to be made equal to $R \cdot w / R_{SQ}$. Then, (5.37) can be written as

$$\tau = \epsilon_0 \cdot \epsilon_r \cdot \frac{(w + \Delta w) \cdot w}{d} \cdot \frac{R^2}{R_{SQ}} . \quad (5.67)$$

Table 5.2 Practical example

Parameters of polysilicon resistor	
Resistor R (DC value)	60 kΩ
Length l	180 μm
Capacitive loading C'	0.26 fF/μm
Calculated important parameters	
Feedback capacitor (critical damping)	31 fF
Time constant τ (= rise time at critical damping)	2.8 ns
Bandwidth B (critical damping)	125 MHz

As we know already from the last section, (5.67) shows that the width w should be kept as small as possible and that the sheet resistance of the resistor polysilicon, a parameter in semiconductor manufacturing, should be chosen as high as possible, i.e. analog process with high-resistive polysilicon are clearly preferable to digital processes with low-resistive polysilicon only. The dielectric constant ϵ_r as well as the thickness d often cannot be changed in the process. Of course, a low overall DC-resistance R also keeps the time constant τ small.

Finally, using (5.63) and (5.67), the expression

$$B \cdot R \propto \frac{1}{R} , \quad (5.68)$$

follows for the resistor-bandwidth product, which means that low resistor values are preferable. In fact, assuming the same resistor-bandwidth product, a DVD-amplifier with its large feedback resistor suffers more from the negative effects described herein than most fiber receivers.

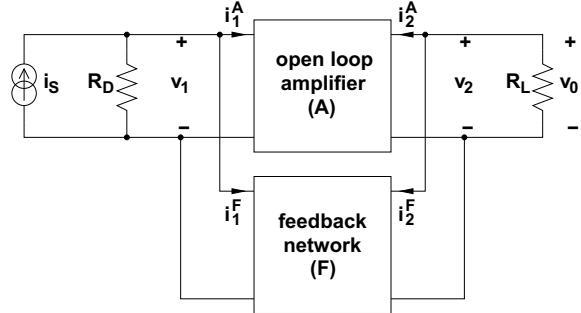
To give some impression, Table 5.2 shows a numerical example of a 60 kΩ polysilicon resistor with a sheet resistance of 1 kΩ \square , and a width of 3 μm for instance. Such a resistor is useable in OEIC-applications for optical storage systems like DVD.

This example belongs to the curves for critical damping of a high-gain amplifier shown in Fig. 5.22. The accuracy of these results is better than 5%. A bandwidth of the OEIC with a 60 kΩ feedback resistor, having the mentioned width and length, of 125 MHz is possible. It should be mentioned that this is the maximum achievable bandwidth. Real amplifiers will reduce it at least slightly.

5.4.7 Shunt-Shunt Feedback

When the feedback in a transimpedance amplifier only consists of an ohmic resistor, the name transresistance amplifier can be used instead of transimpedance amplifier. Such a transresistance amplifier is formed by a shunt-shunt feedback configuration

Fig. 5.24 Shunt-shunt feedback amplifier [25]



(Fig. 5.24). The parameters i_S and R_D are the photocurrent and the parallel resistance of a photodiode. The input port voltages are the same and the output port voltages are the same for the amplifier and feedback two-ports. The y-parameters, therefore, are appropriate for analyzing this shunt-shunt feedback configuration [25].

The amplifier and the feedback network are represented by their individual y-parameters:

$$\begin{aligned} i_1^A &= y_{11}^A v_1 + y_{12}^A v_2 \\ i_2^A &= y_{21}^A v_1 + y_{22}^A v_2 \end{aligned} \quad (5.69)$$

and

$$\begin{aligned} i_1^F &= y_{11}^F v_1 + y_{12}^F v_2 \\ i_2^F &= y_{21}^F v_1 + y_{22}^F v_2 \end{aligned} \quad (5.70)$$

where the superscript A indicates the amplifier and the superscript F indicates the feedback network.

The total input current i_1 and the total output current i_2 can be written as

$$\begin{aligned} i_1 &= i_1^A + i_1^F \text{ and} \\ i_2 &= i_2^A + i_2^F, \end{aligned} \quad (5.71)$$

Substituting (5.69) and (5.70) into (5.71) yields the two-port description for the shunt-shunt feedback amplifier:

$$\begin{aligned} i_1 &= (y_{11}^A + y_{11}^F)v_1 + (y_{12}^A + y_{12}^F)v_2 \\ i_2 &= (y_{21}^A + y_{21}^F)v_1 + (y_{22}^A + y_{22}^F)v_2 \end{aligned} \quad (5.72)$$

A more compact notation can be achieved by defining

$$y_{ij}^T = y_{ij}^A + y_{ij}^F$$

and

$$\begin{aligned} i_1 &= y_{11}^T v_1 + y_{12}^T v_2 \\ i_2 &= y_{21}^T v_1 + y_{22}^T v_2 \end{aligned} \quad (5.73)$$

because the corresponding parameters of both networks again appear together in (5.72). Since the input current is determined stronger by the feedback network than by the amplifier output and since the amplifier (and not the feedback network) drives the load, it is allowed to assume

$$\begin{aligned} y_{12}^F &\gg y_{12}^A \text{ and} \\ y_{21}^A &\gg y_{21}^F \end{aligned} \quad (5.74)$$

and (5.73) can be simplified to

$$\begin{aligned} i_1 &= y_{11}^T v_1 + y_{12}^F v_2 \\ i_2 &= y_{21}^A v_1 + y_{22}^T v_2 . \end{aligned} \quad (5.75)$$

The closed-loop gain of the shunt-shunt feedback amplifier considering the effects of R_D and R_L can now be found with the help of (5.75). At the input port and output port in Fig. 5.24, v_1 and i_1 plus v_2 and i_2 are related by

$$\begin{aligned} i_1 &= i_S - v_1 G_D \text{ and} \\ i_2 &= -G_L v_2 . \end{aligned} \quad (5.76)$$

Substituting (5.76) into (5.75) yields

$$\begin{aligned} i_S &= (G_D + y_{11}^T)v_1 + y_{12}^F v_2 \\ 0 &= y_{21}^A v_1 + (y_{22}^T + G_L)v_2 . \end{aligned} \quad (5.77)$$

The closed-loop transresistance can be obtained from (5.77) by solving for v_2 in terms of i_S :

$$A_{TR} = \frac{v_2}{i_S} = \frac{y_{21}^A}{y_{21}^A y_{12}^F - (G_D + y_{11}^T)(y_{22}^T + G_L)} . \quad (5.78)$$

Rearranging (5.78) into the standard form for a feedback amplifier gives

$$A_{TR} = \frac{v_2}{i_S} = \frac{\frac{-y_{21}^A}{(G_D + y_{11}^T)(y_{22}^T + G_L)}}{1 + \frac{-y_{21}^A}{(G_D + y_{11}^T)(y_{22}^T + G_L)} y_{12}^F} = \frac{A}{1 + A\beta_F} \quad (5.79)$$

where

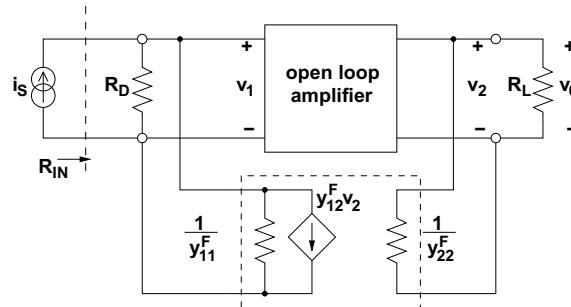


Fig. 5.25 Illustration of the amplifier described by (5.79) and (5.80)

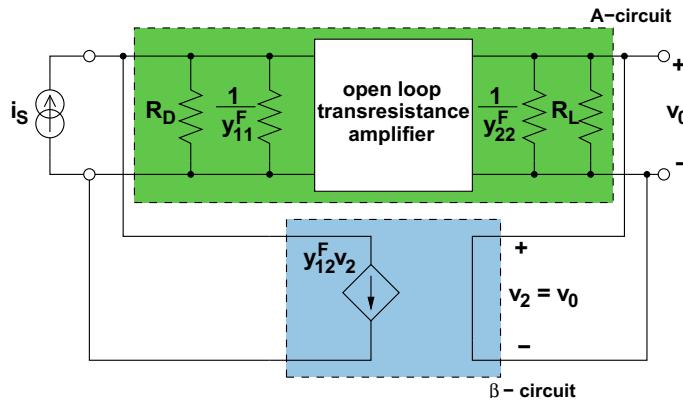


Fig. 5.26 Illustration of the feedback circuit described by (5.79) and (5.80) [25]

$$A = \frac{v_0}{i_s} = -\frac{y_{21}^A}{(G_D + y_{11}^T)(y_{22}^T + G_L)} \quad \text{and} \quad \beta_F = y_{12}^F, \quad (5.80)$$

where the feedback parameter β_F has the dimension Ω^{-1} [25]. These two equations are interpreted in Figs. 5.25 and 5.26 for the case of shunt-shunt feedback. Figure 5.25 shows the feedback amplifier with an explicit representation of the two-port parameters of the feedback network with $y_{21}^F = 0$. According to (5.79) and (5.80) the gain of the amplifier A has to be calculated including the effects of y_{11}^F , y_{22}^F , R_D ($R_D = 1/G_D$), and R_L ($R_L = 1/G_L$).

A schematic representation of these equations is given by redrawing the amplifier as in the circuit in Fig. 5.26. The position of the feedback circuit elements y_{11}^F and y_{22}^F has been changed, but the overall circuit is once again the same. The amplifier A-circuit now includes y_{11}^F , y_{22}^F , R_D , and R_L , whereas the feedback network consists only of y_{12}^F .

Fig. 5.27 First feedback circuit

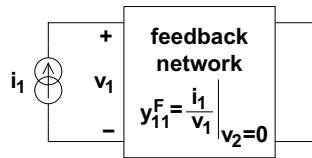


Fig. 5.28 Second feedback circuit

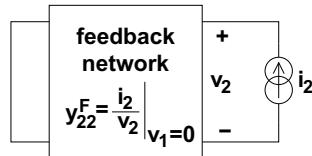


Fig. 5.29 Third feedback circuit

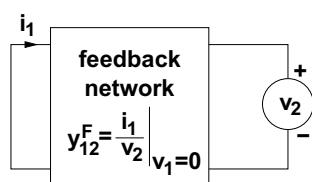
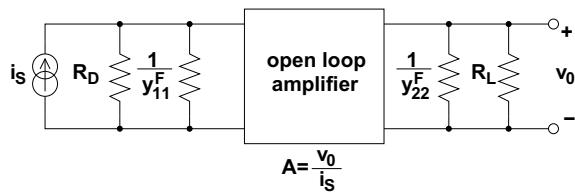


Fig. 5.30 A-circuit for the shunt-shunt feedback amplifier



Figures 5.27, 5.28, 5.29, and 5.30 illustrate the analysis technique in more detail. The three required y-parameters of the feedback network are found based on their individual definitions [25].

The determination of the y-parameter y_{11}^F with a shorted output is illustrated with Fig. 5.27. Figure 5.28 depicts the definition of the y-parameter y_{22}^F , where the input is shorted. Figure 5.29 shows the definition of the y-parameter y_{12}^F .

Then the transresistance of the open-loop amplifier A is calculated from the circuit shown in Fig. 5.30, which includes the loading effects of y_{11}^F , y_{22}^F , R_D , and R_L .

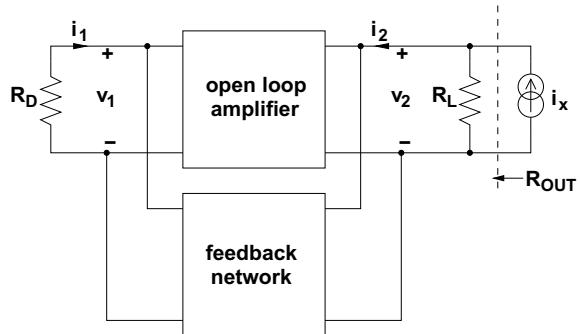
The gain finally is calculated directly from the A-circuit (Fig. 5.30).

5.4.8 Input and Output Resistance

Input Resistance

The input resistance R_{IN} of the closed loop shunt-shunt feedback amplifier (Fig. 5.25) can be calculated using the two-port description in (5.77) [25]. The input resistance

Fig. 5.31 Output resistance of the shunt-shunt feedback amplifier [25]



is

$$R_{IN} = \frac{v_1}{i_S}. \quad (5.81)$$

Solution of (5.77) for i_S in terms of v_1 gives

$$i_S = (G_D + y_{11}^T)v_1 + y_{12}^F \frac{-y_{21}^A}{(y_{22}^T + G_L)} v_1 \quad (5.82)$$

which can be rearranged as

$$R_{IN} = \frac{1}{(G_D + y_{11}^T) \left[1 + \frac{-y_{21}^A}{(G_D + y_{11}^T)(y_{22}^T + G_L)} y_{12}^F \right]} = \frac{\left(\frac{1}{G_D + y_{11}^T} \right)}{1 + A\beta_F} = \frac{R_{IN}^A}{1 + A\beta_F}. \quad (5.83)$$

Shunt feedback reduces the resistance at the port by the factor $(1 + A\beta_F)$. As the loop gain approaches infinity — for an ideal operational amplifier, for example — the input resistance of the closed-loop transresistance amplifier approaches zero. For gigabit optical receivers, however, infinity is by far not reached.

Output Resistance

The output resistance of the closed-loop amplifier can be obtained in a similar manner using the circuit shown in Fig. 5.31 [25].

Here we start with (5.75) and apply a test source i_x to the output of the amplifier:

$$\begin{aligned} i_1 &= y_{11}^T v_1 + y_{12}^F v_2 \\ i_2 &= y_{21}^A v_1 + y_{22}^T v_2. \end{aligned} \quad (5.84)$$

The voltage and current at the input port and at the output port are related by

$$\begin{aligned} i_1 &= -G_D v_1 \\ i_2 &= i_x - G_L v_x . \end{aligned} \quad (5.85)$$

Substituting (5.85) into (5.84) results in

$$\begin{aligned} 0 &= (G_D + y_{11}^T) v_1 + y_{12}^F v_x \\ i_x &= y_{21}^A v_1 + (y_{22}^T + G_L) v_x . \end{aligned} \quad (5.86)$$

When we solve for i_x in terms of v_x , we obtain

$$i_x = y_{21}^A \frac{-y_{12}^F}{(G_D + y_{11}^T)} v_x + (y_{22}^T + G_L) v_x . \quad (5.87)$$

Rearranging (5.87) yields the result for the output resistance of the overall amplifier:

$$\begin{aligned} R_{\text{OUT}} &= \frac{v_x}{i_x} = \frac{1}{(y_{22}^T + G_L) \left[1 + \frac{-y_{21}^A}{(G_D + y_{11}^T)(y_{22}^T + G_L)} y_{12}^F \right]} \\ &= \frac{\left(\frac{1}{y_{22}^T + G_L} \right)}{1 + A\beta_F} = \frac{R_{\text{OUT}}^A}{1 + A\beta_F} . \end{aligned} \quad (5.88)$$

The output resistance of the closed-loop amplifier is equal to the output resistance of the A-circuit decreased by the amount of feedback $(1 + A\beta_F)$. In the ideal case — approximately reached by operational amplifiers — the output resistance of the transresistance amplifier approaches zero when the loop gain approaches infinity.

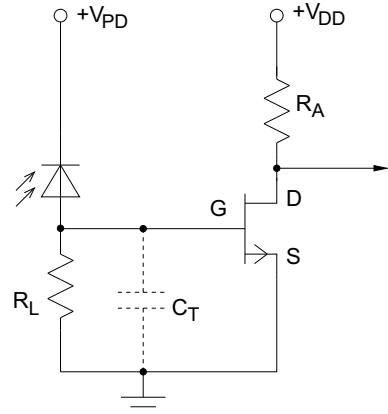
5.4.9 Noise and Sensitivity

Electronic noise has to be considered in the design of optical receivers. The received signal has to be stronger than noise in order to avoid transmission errors. In the following, the basics of electronic noise will be described. The noise of a FET photoreceiver preamplifier will be explained in some detail because it will also be shown that its noise can be used also for noise analysis of receivers with transimpedance amplifiers. Finally the sensitivity of optical receivers will be introduced.

Noise of a Photodiode with FET Preamplifier

Figure 5.32 shows the circuit of a FET photoreceiver preamplifier [26]. The resistor R_L biases the depletion-type junction field-effect transistor and sinks the leakage

Fig. 5.32 Photodiode with FET amplifier



current of the photodiode. And most important, the photocurrent is converted to a voltage signal at R_L .

The capacitance C_T

$$C_T = C_D + C_{GS} + C_S \quad (5.89)$$

is the sum of the photodiode capacitance C_D , the gate capacitance C_{GS} , and the capacitance C_S of the metal line between photodiode and gate of the FET. The gate-drain and therefore the Miller capacitance is neglected in this simple consideration.

The main sources of electronic noise in the circuit of Fig. 5.32 are the thermal noise of resistor R_L and the thermal noise of the FET's channel resistance. We neglect the shot noise due to the gate leakage current. The thermal resistor noise is described by

$$\langle \delta i_{th}^2(f) \rangle \Delta f = \frac{4k_B T}{R_L} \Delta f \quad (5.90)$$

and the thermal noise of the FET's channel resistance is expressed by using the FET's transconductance g_m

$$\langle \delta i_{Ko}^2(f) \rangle \Delta f = 4k_B T \Gamma_F g_m \Delta f . \quad (5.91)$$

The factor Γ_F is about 2/3 for silicon MOSFETs operating in the saturation region. We have to relate the channel noise of the transistor to the input of the amplifier, where we obtain an equivalent voltage fluctuation of

$$\langle \delta V_{Ki}^2(f) \rangle \Delta f = (4k_B T \Gamma_F / g_m) \Delta f , \quad (5.92)$$

which is present across the resistor R_L and the capacitance C_T . The corresponding equivalent current fluctuation is obtained by multiplication with the squared magnitude of the complex conductance

$$\langle \delta i_{\text{Ki}}^2(f) \rangle \Delta f = \langle \delta V_{\text{Ki}}^2(f) \rangle \left[\frac{1}{R_L^2} + (2\pi f C_T)^2 \right] \Delta f . \quad (5.93)$$

The total squared spectral fluctuation of the equivalent input noise current is the sum of the contributions

$$\begin{aligned} \langle \delta i^2(f) \rangle \Delta f &= \langle \delta i_{\text{th}}^2 + \delta i_{\text{Ki}}^2 \rangle \Delta f \\ &= \left[\frac{4k_B T}{R_L} \left(1 + \frac{\Gamma_F}{g_m} R_L \right) + 16\pi^2 k_B T \Gamma_F f^2 \frac{C_T^2}{g_m} \Delta f \right] . \end{aligned} \quad (5.94)$$

The circuit usually will be designed that $g_m R_L \gg 1$ is valid and it is obtained:

$$\langle \delta i^2(f) \rangle \Delta f = \left[4k_B T \left(\frac{1}{R_L} + 4\pi^2 f^2 \Gamma_F \frac{C_T^2}{g_m} \right) \right] \Delta f . \quad (5.95)$$

This relation shows that the input noise is determined by the factor C_T^2/g_m especially at high frequencies. Low capacitances in the input circuit are necessary for low-noise operation. Here OEICs have clear advantages since they avoid the bondpad capacitances.

Noise of a Photodiode with Transimpedance Amplifier

The advantage of a transimpedance amplifier over the PIN FET preamplifier shown in Fig. 5.32, is that the input resistance is lower and to obtain the same bandwidth the feedback resistor R_F respective the input-node capacitance can be larger. We will see in the following, that the transimpedance amplifier has also advantages concerning noise. The first advantage is of course that the noise current of a larger resistor ($R_F > R_L$) is lower. To see the second advantage, we investigate the transimpedance amplifier in Fig. 5.33.

According to [27] the equivalent input noise current generator i_i can be calculated using

$$\bar{i}_i^2 = \bar{i}_{ia}^2 + 4k_B T \frac{1}{R_F + R_2} \Delta f , \quad (5.96)$$

where i_{ia} is the input noise current of the amplifier, i.e. of the input transistor. That the sum of R_F and R_2 determines the noise current can be understood easily from the series circuit of the two resistors (see Fig. 5.33). Equation (5.96) illustrates the second advantage of the transimpedance amplifier concerning noise: the total equivalent input noise current is even lower than that of R_F due to R_2 . This difference, however, may not be very large in practice since R_2 often is much lower than R_F . Therefore, it is a good approximation to use the noise analysis of the PIN FET preamplifier for the transimpedance amplifier with R_F instead of R_L [28].

Sensitivity for Digital Signals

Usually binary optical signals are used in optical data transmission leading to two discrete photocurrents $\langle i_0 \rangle$ and $\langle i_1 \rangle$ (Fig. 5.34). The expected value $\langle i_0 \rangle$

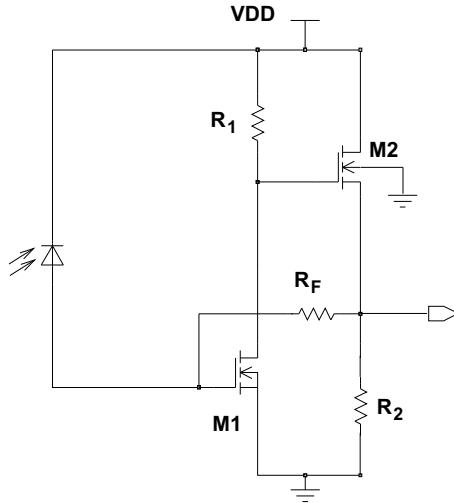


Fig. 5.33 Photodiode with MOS transimpedance amplifier

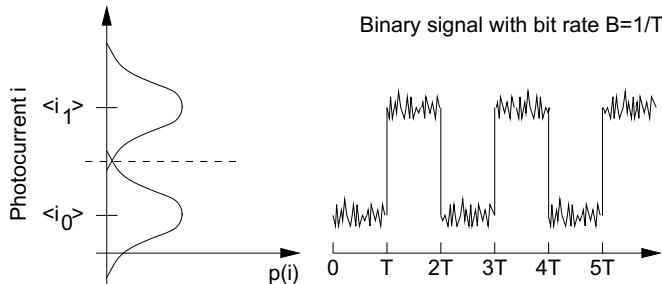


Fig. 5.34 Noisy photocurrent signal with the bit rate B and the distribution $p(i)$ of the instant i values around the logic levels $\langle i_0 \rangle$ and $\langle i_1 \rangle$ [26]

represents the logical zero and $\langle i_1 \rangle$ belongs to the logical one. It is allowed to assume that $\langle i_1 \rangle$ is larger than $\langle i_0 \rangle$. The photocurrent has a certain distribution around the expected or mean values due to the current noise introduced above. The time slot T defines the bit rate B . For simplicity, an amplifier with ideal low-pass characteristics shall be assumed. The bandwidth of this amplifier will be assumed as $B/2$ [26]. The following derivation, however, can easily be done also for a bandwidth of $2B/3$ or $3B/4$ often used in practice.

The variance of the input noise current δi_{ges} is obtained by integration of the spectral noise density (5.94) and considering also shot noise due to the leakage current i_L of the photodiode [26]:

$$\langle \delta i_{\text{ges}}^2 \rangle = \int_0^{B/2} \langle \delta i^2(f) \rangle df = \frac{2k_B T B}{R_L} + q i_L B + \frac{2k_B T \Gamma_F \pi^2 C_T^2 B^3}{3g_m} , \quad (5.97)$$

where $g_m R_L \gg 1$ has been used. We assume that the instant current values have a gaussian distribution around the expected values $\langle i_0 \rangle$ and $\langle i_1 \rangle$. The probability density for a logical zero, therefore, is

$$p_0(i) = \frac{1}{\sqrt{2\pi \langle \delta i_{\text{ges}}^2 \rangle}} \exp \left(-\frac{(i - \langle i_0 \rangle)^2}{2 \langle \delta i_{\text{ges}}^2 \rangle} \right) . \quad (5.98)$$

For a logical one

$$p_1(i) = \frac{1}{\sqrt{2\pi \langle \delta i_{\text{ges}}^2 \rangle}} \exp \left(-\frac{(i - \langle i_1 \rangle)^2}{2 \langle \delta i_{\text{ges}}^2 \rangle} \right) \quad (5.99)$$

is obtained correspondingly. For equally distributed logical zeros and ones, the mean value of the current in respect to time is:

$$D_t = (\langle i_1 \rangle + \langle i_0 \rangle)/2 . \quad (5.100)$$

This value is defined as the decision threshold. For a current $i \leq D_t$, the detected signal is considered as logical zero. The probability of a wrong decision is given by the bit error rate BER for the logical zero

$$\text{BER}_0 = \int_{D_t}^{\infty} p_0(i) di = \frac{1}{\sqrt{2\pi}} \int_Q^{\infty} \exp \left(-u^2/2 \right) du , \quad (5.101)$$

with $u = (i - \langle i_0 \rangle) / \sqrt{\langle \delta i_{\text{ges}}^2 \rangle}$ and where the noise distance

$$Q = \frac{\langle i_1 \rangle - \langle i_0 \rangle}{2\sqrt{\langle \delta i_{\text{ges}}^2 \rangle}} \quad (5.102)$$

also has been introduced. For the applied assumptions it can be shown that the bit error rate for the logical one is equal to that for the logical zero

$$\text{BER}_1 = \int_{-\infty}^{D_{\text{rem}}} p_1(i) di = \text{BER}_0 = \text{BER} . \quad (5.103)$$

Therefore the bit error rate in general obeys to

$$\text{BER} = \frac{1}{\sqrt{2\pi}} \int_Q^{\infty} \exp \left(-u^2/2 \right) \approx \frac{1}{\sqrt{2\pi}} \exp \left(-\frac{Q^2}{2} \right) \left(1 - \frac{1}{Q^2} \right) . \quad (5.104)$$

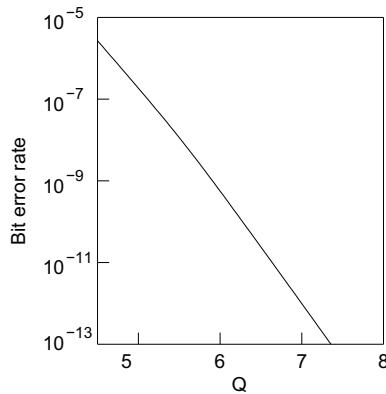


Fig. 5.35 Bit error rate in dependence of the noise distance Q [26]

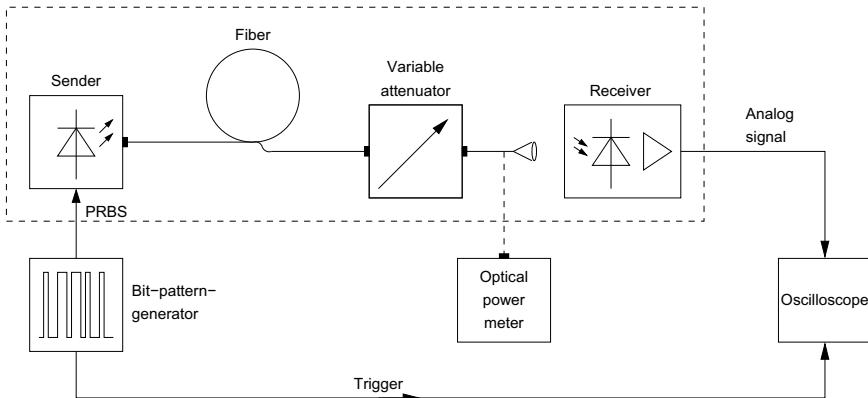


Fig. 5.36 Measurement set-up for eye diagram measurements

The error made by the approximation is less than 1% for $Q \geq 2$. The relation between bit error rate (BER) and the noise distance Q is shown in Fig. 5.35. For instance, $\text{BER} = 10^{-9}$ holds at $Q = 6$ and $\text{BER} = 1.3 \times 10^{12}$ for $Q = 7$.

Modern so-called communication analyzers or digital sampling oscilloscopes can be used to determine the noise distance Q . For this purpose, eye diagrams are taken with a set-up shown in Fig. 5.36.

The receiver under test in Fig. 5.36 has an analog output capable of driving the 50Ω input of the digital sampling oscilloscope. The digital sampling oscilloscope or communication analyzer determines the histograms shown in Fig. 5.37. The mean values $\langle i_0 \rangle$ and $\langle i_1 \rangle$ as well as their variances can be read from the display of the communication analyzer. From the variances, $\langle \delta i_{\text{ges}}^2 \rangle$ and finally the noise distance Q is calculated by the communication analyzer.

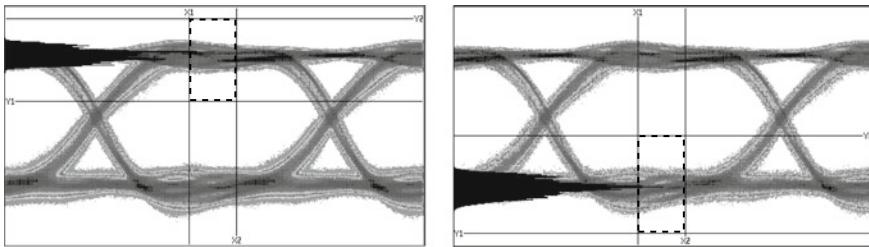


Fig. 5.37 Eye diagrams with histograms for the “1” (left) and “0” (right)

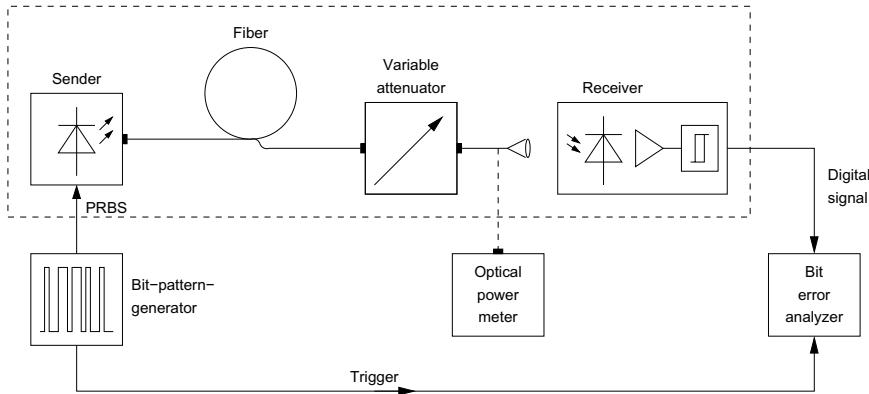


Fig. 5.38 Measurement set-up for digital bit error analysis

When the receiver under test has a digital output the set-up shown in Fig. 5.38 can be used for a bit error analysis. A bit error analyzer also can be used when the analog output of an optical receiver has a larger output voltage than the sensitivity of the bit error analyzer. The bit error analyzer digitally compares the received bits with the sent bits and counts errors. A bit error analyzer results in a more accurate characterization of optical receivers than the determination of Q with the set-up of Fig. 5.36.

The decision threshold D_t is in the middle between the “1”- and “0”-photocurrents. For bit sequences with equally distributed “1”s and “0”s it, therefore, can be expressed by the mean optical power $\eta < P >$, which is converted into photocurrent:

$$D_t = \frac{< i_1 > + < i_0 >}{2} = \eta \frac{q}{\hbar\omega} < P > . \quad (5.105)$$

The ratio r of the two photocurrent levels can be defined:

$$r = < i_0 > / < i_1 > . \quad (5.106)$$

With this definition, the optical power of a binary signal necessary to achieve a certain required bit error rate (i.e. the corresponding Q -factor) results:

$$\langle P \rangle = \frac{1+r}{1-r} \frac{\hbar\omega}{\eta q} Q \sqrt{\langle \delta i_{\text{ges}}^2 \rangle} . \quad (5.107)$$

This quantity is called sensitivity of the optical receiver and it is usually expressed in dBm ($10 \times \log(\langle P \rangle / 1 \text{ mW})$). It becomes lowest for $r = 0$, i.e. $\langle i_0 \rangle = 0$ or a vanishing “0” optical power. In this case it is

$$\langle P \rangle = \frac{\hbar\omega}{\eta q} Q \sqrt{\langle \delta i_{\text{ges}}^2 \rangle} . \quad (5.108)$$

When we insert (5.97) into (5.108), we obtain the lowest possible average optical power for a PIN-FET input stage

$$\langle P \rangle = \frac{\hbar\omega}{\eta q} Q \sqrt{\frac{2k_B T B}{R_L} + q i_L B + \frac{2k_B T \Gamma_F \pi^2 C_T^2 B^3}{3g_m}} . \quad (5.109)$$

In reality, laser diodes have to be biased above the threshold to allow fast data rates. The extinction ratio ($=1/r$) is therefore less than infinity in practice and a somewhat larger $\langle P \rangle$ is necessary than the minimum value for $r = 0$.

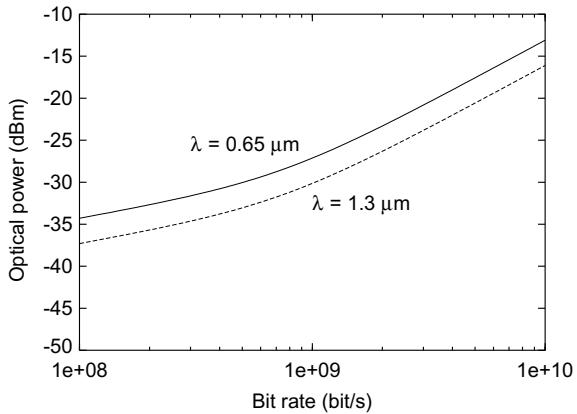
When we consider that $\omega = 2\pi c_0/\lambda$, the sensitivity depends on the wavelength. For instance

$$10 \log\left(\frac{P^{650}}{P^{1300}}\right) = 10 \log\left(\frac{1300}{650}\right) = 10 \log(2) = 3 \text{ dB} \quad (5.110)$$

shows that at an optical wavelength of 650 nm, a twice as large average optical power is needed than at 1300 nm for the same BER. For a silicon OEIC detecting a 650 nm signal this means, that the sensitivity value (e.g. -20 dBm) looks 3 dB worse than for a III/V-photodiode in combination with an amplifier possessing the same equivalent input noise current and operating with 1300 nm (e.g. -23 dBm). In comparison to $\lambda = 1540 \text{ nm}$, which is the most frequently used wavelength for long-haul optical fiber communication, the sensitivity for $\lambda = 650 \text{ nm}$ is 3.75 dB worse.

Figure 5.39 shows this 3 dB penalty for a wavelength $\lambda = 650 \text{ nm}$ compared to $\lambda = 1300 \text{ nm}$. This figure also illustrates that the noise contribution of the resistor R_L (or R_F) dominates up to about 500 Mb/s for the parameters given in the figure caption. At higher bit rates, the slope of the curves increases indicating that the FET noise dominates there for the parameters listed in the caption of Fig. 5.39. According to Fig. 5.39, a silicon OEIC can achieve a sensitivity of about -27 dBm for $\lambda = 650 \text{ nm}$ at a bit rate of 1.0 Gb/s in the NRZ transmission mode.

Fig. 5.39 Sensitivity of an optical receiver for two different wavelengths ($\eta = 0.5$, $Q = 6$ i.e. $\text{BER} = 10^{-9}$, $R_L = 3.2\text{k}\Omega$, $i_L = 10\text{ pA}$, $\Gamma_F = 2/3$, $C_T = 0.5\text{ pF}$, and $g_m = 1\text{ mS}$) calculated with (5.109)



5.4.10 Poisson Statistics and Quantum Limit

If electronic noise would not exist at all, the physical limit for the sensitivity of optical receivers would be set by the Poisson statistics for incident photons. The quantum limit results from the variation of the number of photons, which hit the detector and generate electron-hole pairs (or photoelectrons) in a bit time slot $T = 1/B$ (B = bit rate per second). The probability $p_m(k)$ that k events happen in the time interval T , when m events occur in average in T , is given by the Poisson distribution [29]

$$p_m(k) = \frac{m^k}{k!} e^{-m}. \quad (5.111)$$

When we assume a detection efficiency of 100%, 21 photons in average are needed in a “1”-bit that the BER is smaller than 10^{-9} , since the probability that a “0” ($k=0$) is detected has to be smaller than 10^{-9} , which requires $m = 21$ or larger. It also has to be mentioned that an extinction ratio of infinity is required for the light source, if the Poisson statistics is to be made use of.¹ When error correction is an option, the BER can be up to 2×10^{-3} [30, 31] and only 7 photons are needed in average.

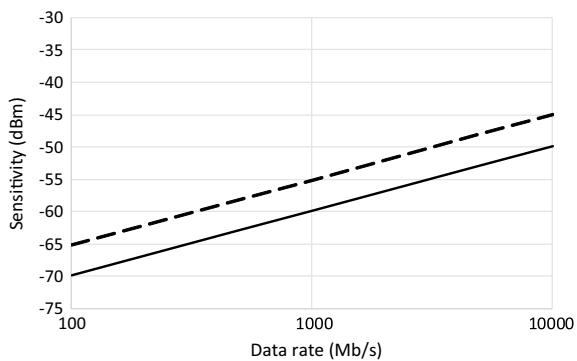
The average optical power $\langle P \rangle$ corresponds to the average number of photons m like this:

$$\langle P \rangle = \frac{mh\nu B}{2}. \quad (5.112)$$

The photon energy is $h\nu$ and B is the data rate in s^{-1} . The average optical power necessary to reach a certain BER is called sensitivity. The sensitivity is often expressed in dBm ($10 \log(\langle P \rangle / 1\text{ mW})$). The sensitivity for the quantum limit and BERs of 10^{-9} and 2×10^{-3} is shown in Fig. 5.40. It should be mentioned that the

¹This will cause some limitations for optical free-space communication in presence of background light.

Fig. 5.40 Quantum limit for a wavelength of 670 nm (dashed line: BER = 10^{-9} ; solid line: BER = 2×10^{-3})



quantum limit depends on the wavelength. In the next chapter, SPAD receivers will be introduced, which tried to approach to the quantum limit.

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Chapter 6

Examples of Optoelectronic Integrated Circuits



In this chapter the full variety of silicon receiver OEICs in digital and analog techniques will be introduced. Examples of optical receivers range from low-power synchronous digital circuits for massively parallel optical interconnects and three-dimensional optical storage to asynchronous Gb/s fiber receivers. Hybrid integrated laser drivers are included as examples of optical emitters. Low-offset analog OEICs for two-dimensional optical storage systems like digital-versatile-disk (DVD) and digital-video-recording (DVR) will be described as well as image sensors. Among various optical sensors for industrial and medical applications, smart pixel sensors as well as distance measurement circuits leading to 3D cameras and paving the way to innovative cameras-on-a-chip (CoC) will be presented. Furthermore, very interesting 3D sensors with pin and single-photon avalanche diodes are described. Techniques like integrated voltage-up-converters and the four-quarter POF receiver approach for speed enhancement of OEICs as well as newer POF receivers will also be introduced. Innovative solutions to overcome the bandwidth limitations of integrated resistors in transimpedance amplifiers are described. Developments of burst-mode and deep-sub- μm receivers are additionally addressed. Newest integrated receivers for optical wireless communication with pin and avalanche photodiodes are included. Two highly parallel optical receivers with total data rates of up to 140 Gb/s are described. Furthermore, highly innovative SPAD receivers eliminating electronic noise and reducing the gap to the quantum limit are introduced. A comparison of fiber and optical interconnect receivers plus an innovative optoelectronical PLL circuit as well as a summary are finally included.

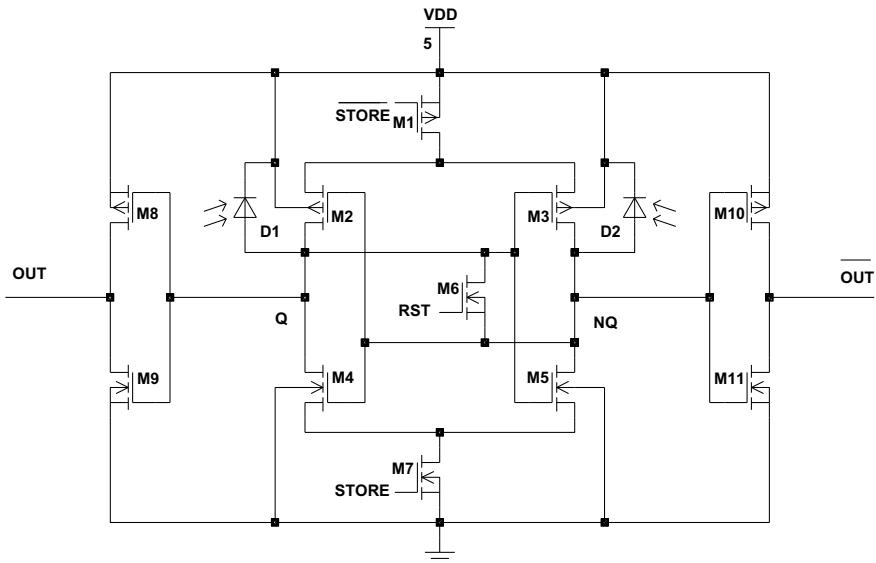


Fig. 6.1 CMOS synchronous photoreceiver circuit [1]

6.1 Digital CMOS Circuits

In this section, the properties of digital CMOS OEICs are described because of their potential application in massively parallel optical interconnects and volume holographic optical memories. Synchronous circuits and among them one implementing a spatially-modulated-light detector are appropriate for such purposes. Furthermore, asynchronous photoreceivers for application in the testing of digital CMOS circuits on the wafer level deserve to be described here.

6.1.1 Synchronous Circuits

For the application in massively parallel optical interconnects between VLSI chips a novel monolithic optoelectronic receiver system was presented in a standard $0.7\text{ }\mu\text{m}$ N-well CMOS technology [1]. The circuit, which requires two clock signals, reset (RST) and store (STORE), and therefore is a synchronous circuit, is shown in Fig. 6.1.

The heart of the synchronous receiver is a CMOS bistable flip-flop, which acts as a sense-amplifier. The flip-flop is formed by two CMOS inverters, M2/M4 and M3/M5. The input of each inverter is connected to the output of the other inverter. In such a way a dual state can be stored. In order to use the flip-flop as a light receiver, two photodiodes were added to the drains of the P-channel transistors M2 and M3. In fact the diodes were not separated from the transistors. The diodes were obtained

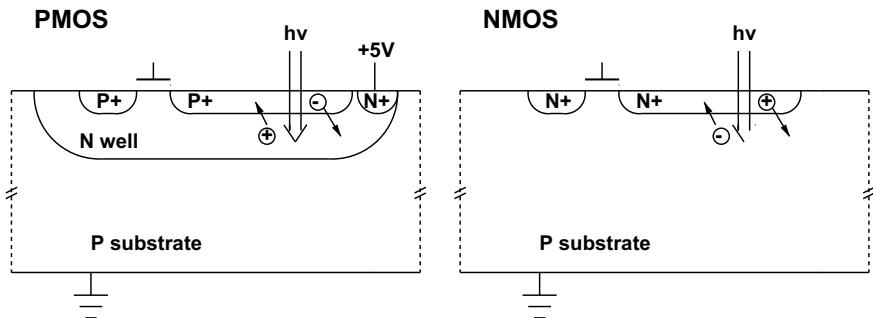


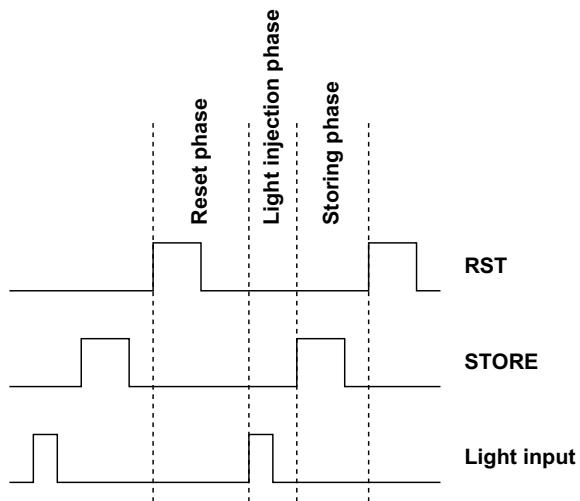
Fig. 6.2 Cross section of MOS transistors with enlarged drain areas as photodiodes [1]

by extending the drains to an area of $15 \times 15 \mu\text{m}^2$. The P⁺ drain island and the N well, therefore, form the photodiode (Fig. 6.2).

The timing of the synchronous receiver is shown in Fig. 6.3. Before the flip-flop can receive, i.e. store, a new bit, a reset signal has to be applied to M6. During this reset signal, the flip-flop is deactivated by a low voltage level at the gate of M7 and by a high voltage level at the gate of M1. M6 is conducting during reset and forces the nodes Q and NQ to the same potential. After the reset phase, M6 is switched off and light can fall into one of the diodes, let us say into D1. Electron–hole pairs are generated at the P⁺N junction between the drain of M2 and the N well. The N well is biased at VDD = 5 V. The potential of the drain can be assumed to be at a floating level of approximately VDD/2. The P⁺N photodiode is biased in the reverse direction and the photogenerated carriers are separated in the electric field region of the PN junction effectively. The photogenerated electrons drift into the N well and the photogenerated holes drift into the P⁺ region. There is also a slower contribution of diffusing minority carriers to the photocurrent, because the light penetrates also in deeper field-free regions of the N well. As a consequence of the photocurrents, the potential of node Q becomes more positive than that of node NQ. When the supply voltages are applied to the flip-flop via M1 and M7, the sense-amplifier flip-flop begins to work. A more positive input signal of the inverter M3/M5 results in a more negative output signal at node NQ, which causes a higher output signal of the inverter M2/M4 at node Q. This amplifying ring process continues until digital levels, i.e. VDD and ground levels are obtained at the two output nodes Q and NQ of the flip-flop, respectively. It was reported that this final stable state was reached after approximately 3 ns from the beginning of the light incidence [1].

A minimum light input energy of 176 fJ, which corresponds to an optical power of $59 \mu\text{W}$ within a time interval of 3 ns, was needed for an optical wavelength of 830 nm in order to obtain a correct decision of the sense-amplifier flip-flop. This minimum light energy causes a voltage change of 264 mV at node Q [1]. This voltage change is amplified by the flip-flop to a digital level. With the PMOS version described above a bit rate of 120 Mb/s was obtained. In the NMOS version, i.e. using the N⁺-drain to P-substrate diodes of the transistors M4 and M5 as photodiodes (see Figs. 6.1 and 6.2), a maximum bit rate of 180 Mb/s was reported. This higher speed of the

Fig. 6.3 Timing diagram of a synchronous CMOS photoreceiver [1]



NMOS version of the synchronous receiver can be explained by the faster diffusion of electrons in the P substrate. The PMOS version is slower because holes are the minority carriers in the N well and holes are diffusing slower than electrons due to the lower hole mobility.

For massively parallel optical interconnects it is necessary to minimize the die area of the receivers. The receiver circuit shown in Fig. 6.1 occupied an area of $55 \times 24 \mu\text{m}^2$ without the output buffers. The synchronous receiver with the sense-amplifier flip-flop is especially interesting for application in massively parallel optical interconnects due to its very small area consumption.

The function of this receiver is called synchronous because the clock signals reset and store are needed. These signals have to be transmitted in additional optical fibers, for which asynchronous receivers are needed, or have to be supplied electrically.

In the following, another application of sense-amplifier flip-flops, where the reset and store signals are readily available, will be described. Sense-amplifier flip-flops can readily be used for the read process of page-oriented optical memories (POMs), like volume holographic storage systems [2]. Such optical memories need highly parallel read circuits. A small size of each detector and each amplifier is therefore essential. The clock signals for reset and store (or latch) of the sense-amplifier flip-flop are readily available in optical memories and these signals do not have to be extracted for this application. The POMs offer the potential for high capacity, random access times from 10 to $100 \mu\text{s}$, and page sizes up to 1 Mb, yielding data transfer rates of 10–100 Gb/s. Maximum output data rates of 250 Mb/s for CCD arrays [3] are insufficient for POM systems. Pixel circuits, like that in Fig. 6.4 with sense-amplifier flip-flops, combine a large speed, a high gain, and a small size. They can be embedded in each pixel yielding active receivers in a highly parallel arrangement. The circuit of a pixel in a photodetector array for a page-oriented optical memory (Fig. 6.4) combines two flip-flops (latches) in order to achieve a high gain.

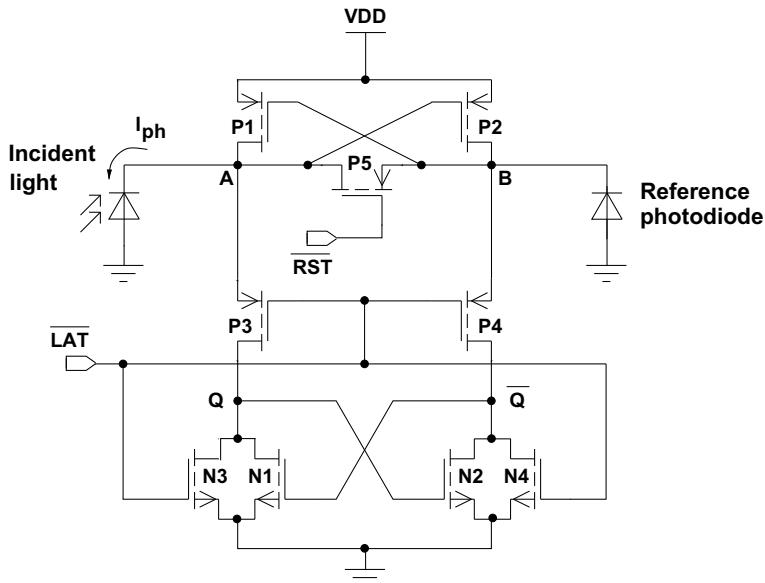


Fig. 6.4 Photoreceiver circuit for smart photodetector array [4]

The operation of the circuit is controlled by reset \overline{RST} and latch \overline{LAT} . The P latch with transistors P1 and P2 is isolated from the N latch with N1 and N2 via P3 and P4 for $\overline{LAT} = 1$. The pull-down devices N3 and N4 are conducting and the N latch is reset for $\overline{LAT} = 1$. Next \overline{RST} is set to 0. During this reset, the photosensitive inputs A and B are shorted through P5 and $V_A = V_B = V_{RST} \approx VDD + V_{Th,PMOS}$. When \overline{RST} is taken high again, parasitic capacitances hold nodes A and B at V_{RST} putting the P latch in a metastable state. A photocurrent I_{ph} at one of the differential inputs causes the corresponding input voltage to drop. Positive feedback in the P latch increases the differential voltage. When \overline{LAT} is changed to 0, this differential voltage is amplified by the N latch and the signal is acquired at Q and \overline{Q} . P1 and P2 should be small in size for a high sensitivity to small photocurrents. The static power consumption of the circuit in Fig. 6.4 is determined by leakage currents. The dynamic power consumption mainly depends on the capacitance of the photodiode. In [4], the N-well to P-substrate photodiode in a $0.35\text{ }\mu\text{m}$ CMOS process was used with a photosensitive N-well area of $50 \times 50\text{ }\mu\text{m}^2$. The capacitance of this photodiode was approximately 1 pF. The size of the photoreceiver circuit in Fig. 6.4 without the photodiodes was $20 \times 22\text{ }\mu\text{m}^2$. An optical power of $2.5\text{ }\mu\text{W}$ for $\lambda = 839\text{ nm}$ was necessary to toggle the receiver. With an assumed photodiode responsivity of 0.3 A/W , a switching energy of 150 fJ was estimated [4]. A single-pixel data rate of 245 Mb/s was determined for the circuit in Fig. 6.4. With the circuitry necessary for error correction, a maximum pixel number of approximately 26 700 per $0.35\text{ }\mu\text{m}$ CMOS chip was projected in [4]. The bit rate per chip for corrected data was estimated to be 102 Gb/s stemming from the high parallelism.

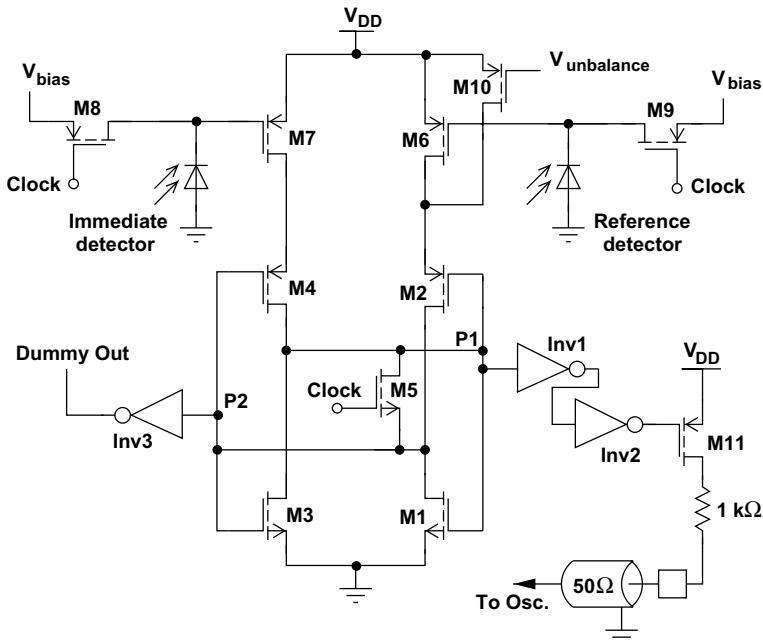


Fig. 6.5 Circuit of a CMOS synchronous receiver with SML detector and sense amplifier [5]

A sense-amplifier receiver for optical data link applications and parallel optical interconnects also was used together with the SML detector (see Sect. 2.2.5). The circuit diagram of this sense-amplifier receiver [5] is shown in Fig. 6.5.

The receiver is reset during the negative phase of the clock when M8 and M9 are on and connect the immediate as well as the reference detector (both represented by diodes in Fig. 6.5) to V_{Bias} . When the clock turns high, both detector parts are left floating. Now the receiver is sensitive to light incidence. Both detector parts integrate carriers that reach the detector junctions. The potentials at both cathodes drop proportional to the integrated charges. The charge in the immediate detector, however, is larger (drifting and a part of diffusing carriers are integrated) than that in the reference detector (only a part of diffusing carriers is collected). Consequently, M7 has a larger $|V_{GS}|$ than M6. The drain current of M7 is larger than that of M6, which brings the sense-amplifier out of equilibrium. This equilibrium was established during the positive phase of the clock, when M5 was on. When light was received, the cross-coupled inverters M3, M4 and M1, M2 deliver a digital HIGH and a digital LOW at their outputs. When, there was no light incidence, both potentials at the gates of M6 and M7 are the same and noise determines the direction into which the inverter pair flips. To avoid this problem, an unbalance is built in by M10. An appropriate gate potential ($V_{unbalance}$) of M10 determines the direction into which the inverter pair flips, when there was no light incidence. With light incidence, it flips into the other

direction. This unbalance measure implements a threshold. The incident light has to overcome this threshold to bring the receiver into the state “received light”.

The inverters Inv1 and Inv3 are buffers to extract the received state. Actually for extraction only one inverter would be sufficient, however, for a better performance of the receiver a symmetric load on nodes P1 and P2 is required. Via Inv2, PMOS transistor M11 drives a voltage divider 21:1 to use an oscilloscope with a 50Ω input impedance for characterization purposes.

With a $0.8\mu\text{m}$ CMOS technology, a bit rate of 155 Mb/s with an optical pulse power of $5.6\mu\text{W}$ for $\lambda=860\text{nm}$ was possible. The size of the SML detector was $70\times70\mu\text{m}^2$ and the sense amplifier (without output driver) fitted into the same area. The power consumption of the sense-amplifier receiver for a bit rate of 180 Mb/s was 0.5 mW [5].

6.1.2 Asynchronous Circuits

Compact and fast photoreceivers with on-chip photodiodes in standard CMOS technology have been developed as optical inputs for testing of digital circuits [6]. Novel CMOS circuits work at increased speed and they cannot be tested on the wafer level at their working speed with conventional electric needle contacts. In order to overcome this limitation, optical inputs can be used. The light is coupled into photodiodes on the chips via optical fibers being adjusted on a wafer prober (Fig. 6.6). The outputs of the chip having lower frequency were contacted with electric needles or capacitively with a special probe sensor. The output signals are checked for correctness by the comparator in a test equipment (Fig. 6.6).

In a $1.5\mu\text{m}$ CMOS technology an input frequency of 250 MHz was obtained for an optical wavelength of 635 nm with an optical receiver requiring a die area of only $70\times70\mu\text{m}^2$. Maximum input frequencies of 243 and 187 MHz were reported for the wavelengths of 685 and 787 nm, respectively. The N⁺-source/drain to P-substrate diode in the N-well CMOS process was used for the photodiodes with an area of $20\times20\mu\text{m}^2$. The speed of the circuit test on the wafer was increased several times compared to the conventional electrical input technique using this optical input technique. This performance could be obtained with a current comparator circuit with a statically supplied reference photodiode. The circuit diagram of this photoreceiver is shown in Fig. 6.7.

The transistors M1, M2 and M3, M4, respectively, form current mirrors, which amplify the photocurrents of the signal and reference photodiodes. The transient response has its optimum for a width ratio W2/W1 of 2–2.5 [6]. The amplified photocurrents are compared to each other by the transistors M2 and M4. The advantage of this configuration is its good sensitivity to small differences in the photocurrents due to the high impedance node N3. Due to the high drain resistances a small difference in the currents results in a large voltage change. The advantage of this photoreceiver clearly is that the photocurrent of the N⁺P signal photodiode does not have to drop much to obtain a logical zero at the output node N3 of the current comparator, when

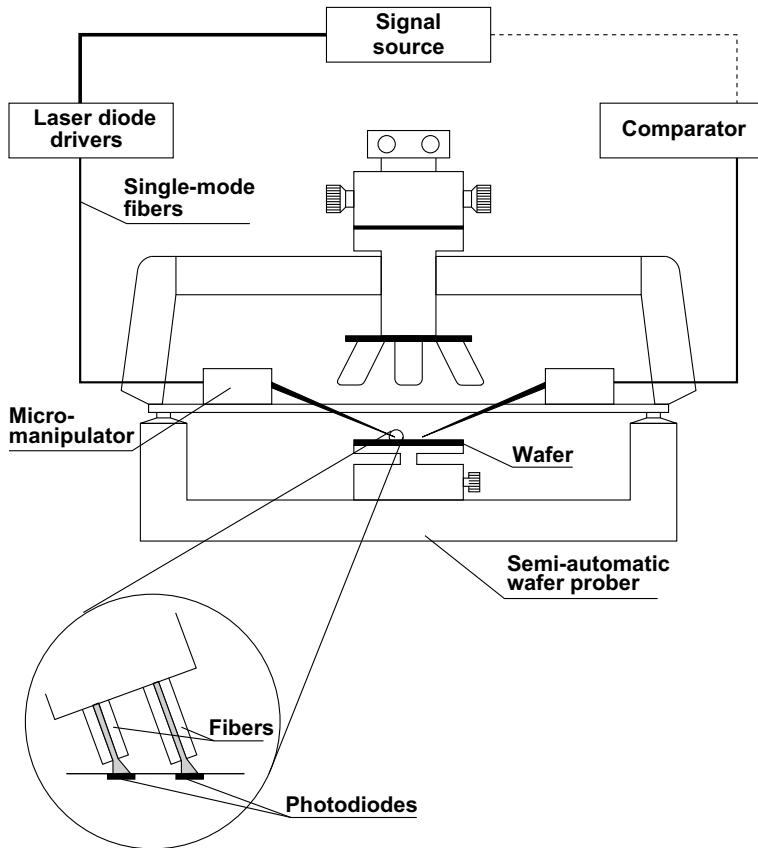


Fig. 6.6 Test equipment using optical inputs on a wafer level [7]

the light is switched off for a short period, i.e. a large contribution of the slow diffusion current to the photocurrent is possible. It has to be mentioned, however, that large photocurrents and large optical powers are necessary to obtain fast current mirror amplifiers. The optical power used for chip testing was of the order of 1 mW [6]. Another advantage of this current comparator circuit is its robustness for the application in automatic chip testers. Compared to the synchronous receiver shown in Fig. 6.1, the current comparator circuit shown in Fig. 6.7 works asynchronously and, therefore, does not need overhead circuitry for timing. The speed of the current comparator circuit in a $1.5\text{ }\mu\text{m}$ CMOS technology is comparable to the speed of the synchronous receiver in a $0.7\text{ }\mu\text{m}$ CMOS technology for the optical wavelength of 787 nm. The speed of the current comparator circuit, therefore, can be improved considerably by using a technology with a smaller gate length. The signal photodiode feeding an N-channel current mirror and the reference photodiode feeding

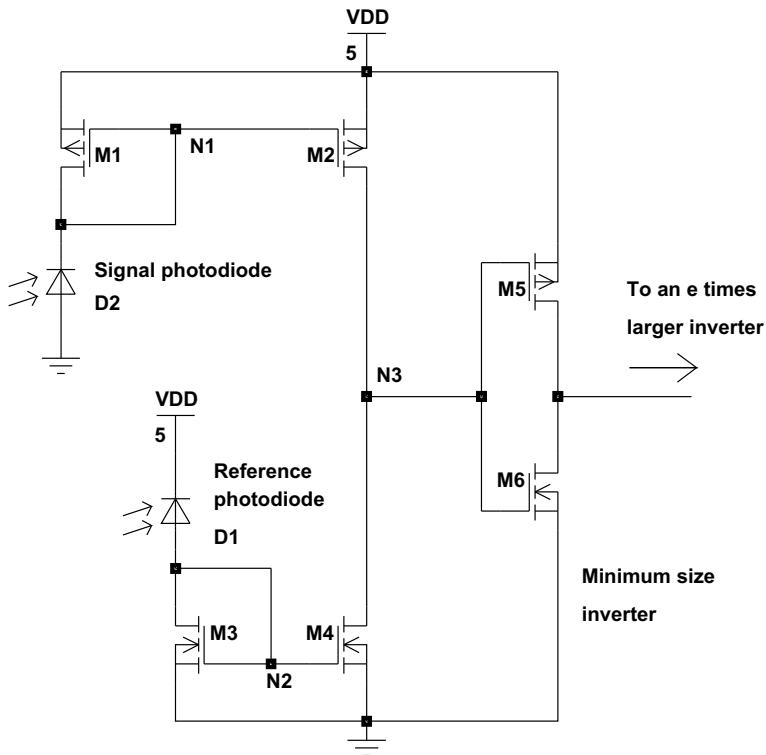


Fig. 6.7 CMOS current comparator photoreceiver circuit [6]

the P-channel current mirror probably would allow a further increase in the input frequency.

6.2 Digital BiCMOS Circuits

The principle of a current comparator circuit shown in Fig. 6.7 for a CMOS photoreceiver was also applied to a BiCMOS photoreceiver for the high speed testing of frequency dividers on the wafer level [7]. Figure 6.8 shows the BiCMOS version of a current comparator. In the 1.2 μm BiCMOS process fast NPN transistors were available, which preferably were used in the signal current mirror. The slower P-channel current mirrors are kept for the reference path.

The circuit shown in Fig. 6.8 was used for a high speed test of a BiCMOS frequency divider on the wafer level. N^+ to P-substrate and P^+ to N-well photodiodes with areas of $20 \times 20 \mu\text{m}^2$ were used. A frequency of 800 MHz was successfully fed into the BiCMOS frequency divider optically with a wavelength of 635 nm via a single-mode

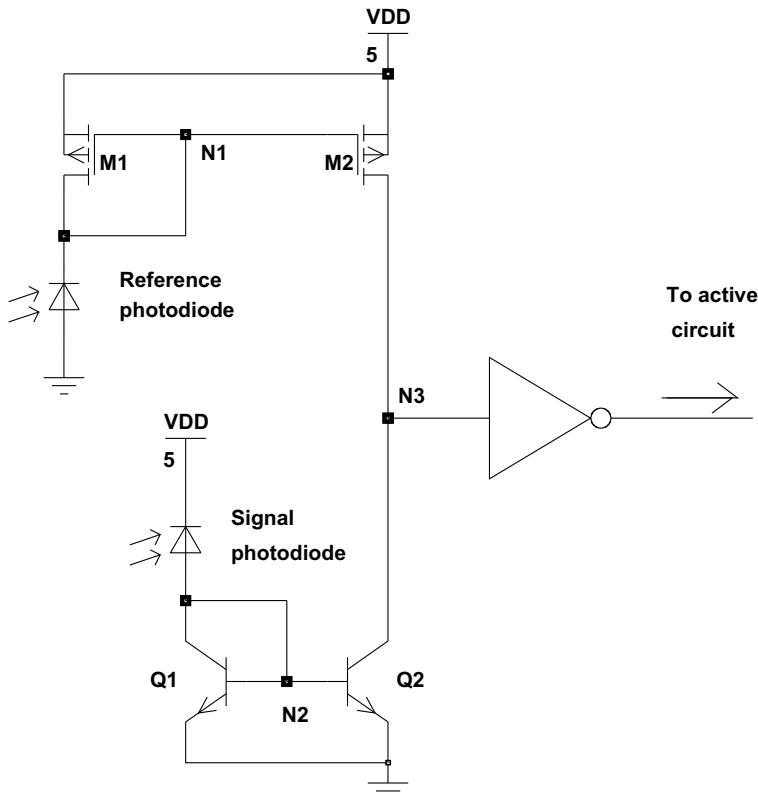


Fig. 6.8 BiCMOS current comparator photoreceiver circuit [7]

fiber. The optical output power of the commercially available semiconductor laser used in [7] was of the order of 1 mW. The area consumption of an optical input was reported to be less than $70 \times 70 \mu\text{m}^2$.

6.3 Laser Driver Circuits

A simple two-transistor CMOS driver (Fig. 6.9) based on a current-shunting principle, which provides a low-area, tunable power circuit with a measured small-signal bandwidth of 2 GHz in 0.5 μm CMOS technology, has been implemented in a flip-chip bonded CMOS VCSEL chip [8].

The PMOS transistor is used to supply an adjustable current through the laser, and the NMOS transistor is used to quickly shunt the current into and out of the VCSEL for digital operation. The multimode VCSELs could be operated at 1.25 Gb/s from below the laser threshold in this digital operation. In this case, the eye pattern

Fig. 6.9 CMOS shunt laser driver circuit [8]

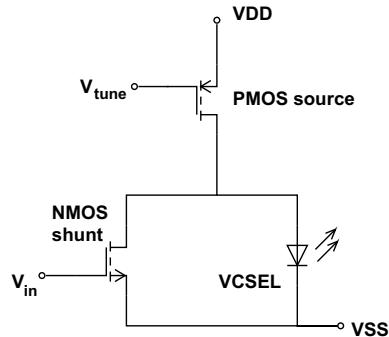
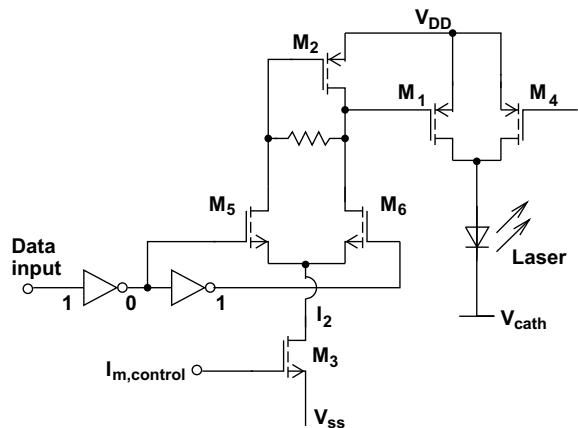


Fig. 6.10 CMOS laser driver circuit [9]

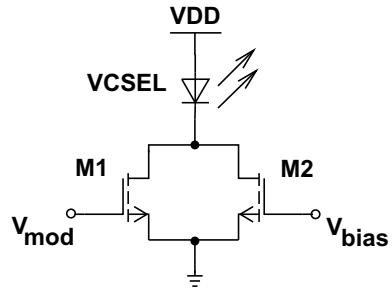


indicated a turn-on delay of the lasers of about 180 ps. For a bit error rate of less than 10^{-11} at 1.25 Gb/s, the total power consumption of one driver and laser was about 17.5 mW at an optical power of -6.9 dBm. The NMOS transistor used as a small signal modulator, reducing the laser current only by a small amount and especially not below the threshold current, allowed to verify a bandwidth of the order of 2 GHz. This low-power high-speed operation demonstrates the utility and potential of the flip-chip bonding technique for optical interconnect technology.

Another hybrid CMOS-VCSEL transmitter has been introduced [9]. An array of 8 GaAs-AlAs lasers with an InGaAs triple-quantum-well active region was wire-bonded to driver circuits in a $1.0\text{ }\mu\text{m}$ CMOS technology. The threshold current I_{th} of the lasers was 2.7 mA and the peak optical output power exceeded 1 mW without heat sinking. Typical turn-on voltages $V_{\text{ld}}(I_{\text{th}})$ were (3 ± 0.5) V. The driver circuit is shown in Fig. 6.10.

Since the laser array had one common cathode, only the lasers' anode terminals are independent and the modulation current I_{m} is controlled by the PMOS transistor M_1 . The PMOS transistor M_4 regulates the laser bias current, which has to be somewhat larger than I_{th} in order to allow fast laser modulation. By minimizing stored charge

Fig. 6.11 Laser driver circuit with two NMOS transistors [10]



in the current steering transistors, fast rise and fall times with low jitter and skew can be achieved. The choice of the width of M_1 , however, is a trade-off between low parasitic capacitance for small device width and a reduced output impedance for a large width. A device width of $500\mu\text{m}$ has been chosen as a good compromise for $I_m = 15\text{--}25\text{ mA}$ in [9].

The NMOS devices M_5 and M_6 together with the inverter between their gates perform a single-ended to differential conversion. The NMOS device M_3 controls the modulation current I_m . The PMOS transistor M_2 serves as a current mirror reference in the ‘1’ state and is a self-biased inverter in the ‘0’ state. In such a way U_{gs} of M_1 is not zero but approximately equal to the threshold voltage in the ‘0’ state, when the laser is off, and a high modulation speed can be obtained. In the ‘1’ state, I_2 is mirrored (amplified by a certain factor) through M_2 to M_1 and into the laser. With a 50Ω resistor load instead of the laser and with $I_m = 25\text{ mA}$ the rise and fall times were about 0.5 ns and the eye pattern was wide open at 622 Mb/s . When a chip with 8 CMOS drivers was incorporated into one package with a VCSEL array flip-chip mounted onto a BeO substrate, the bond-wire inductances somewhat degenerated the slew rate [9]. A data rate of 622 Mb/s with a bit error rate of less than 10^{-9} , however, still has been obtained.

The cell size of one driver circuit with output pads was $175 \times 300\mu\text{m}^2$. The average power dissipation of one channel was 137 mW for an optical output power of 1 mW with $I_m = 20\text{ mA}$, where the laser consumed 75 mW (55%), M_1 dissipated 45 mW (33%), and its driver used 17 mW (12%). For an array with many CMOS-VCSEL channels, this large power dissipation generates too much heat and better designs are necessary.

A laser driver circuit consisting of two N-channel MOS transistors (see Fig. 6.11) is advantageous compared to the shunt driver circuit in Fig. 6.9 with respect to power consumption. Here, M_2 is used to bias the laser above threshold (‘0’) and M_1 increases the laser current in order to obtain a high optical output power (‘1’). Here, the current flowing continuously is lower than in the shunt driver circuit shown in Fig. 6.9. The circuit in Fig. 6.11 was implemented in [10] to modulate flip-chip bonded InGaAs quantum well VCSELs with an I_{th} of 6.4 mA .

The N-channel MOSFETs had a gate length of $0.8\text{ }\mu\text{m}$ and a gate width of $30\text{ }\mu\text{m}$. With V_{mod} between 3.2 and 5 V the optical output power could be controlled between 0.05 and 1.3 mW, when $\text{VDD}=8.5\text{ V}$ had been chosen. A possible modulation rate of 2 Gb/s for the circuit in Fig. 6.11 has been estimated [10].

6.4 Analog Circuits

In this section, a bipolar amplifier circuit for an optical flame detection system with a very high transimpedance of $1.1 \times 10^9\text{ V/A}$ will be described. Another bipolar amplifier for audio CD systems is also described because of a so-called T-type feedback circuitry.

Two pixel circuits of a-Si:H CMOS image sensors with reduced cross-talk and a very high dynamic sensitivity range, respectively, an image sensor being adaptive to motion and light intensity, a self-calibrating logarithmic camera-on-a-chip (CoC), and an imager allowing read-out of regions-of-interest will follow. Furthermore, a fingerprint detector using lateral bipolar phototransistors is discussed. Innovative circuits for optical distance measurement and 3D sensors are described next. After these, smart pixel sensors are discussed. Then different optical CMOS and BiCMOS sensor circuits, single-photon sensors and sensors for optical storage systems are described.

Subsequently, continuous-mode fiber receivers are explained. New speed-enhancement techniques, plastic-optical-fiber (POF) receivers, as well as burst-mode, deep-sub-micron receivers, and receivers aiming to the quantum limit then follow. A comparison of the performance of OEIC receivers compactly represents the state of the art. Finally an optoelectronic PLL will be discussed.

6.4.1 Bipolar Circuits

The detector of a UV-sensitive OEIC [11] was already described in Sect. 2.1.3. The electronic circuit of the UV sensor system for flame detection where the photocurrent was only $20\text{ pA}-1\text{ nA}$ will be explained here.

Due to the small photocurrents a large amplification with a large transimpedance of 10^9 V/A was necessary in order to obtain signal voltages of up to 1 V. Fortunately, the system did not require accurate control of the gain and, therefore, the current amplification factors of the NPN and PNP transistors of the complementary bipolar process could be fully exploited without a feedback circuitry. The circuit diagram of the bipolar amplifier is shown in Fig. 6.12.

The transistors Q_{13} and Q_{15} both in common base configuration together with their current sources Q_{12} and Q_{14} , respectively, provide a low-impedance input for the photocurrent ($R_{\text{in}} = 1/g_{\text{m},13}$). The UV photodiode is biased at zero volts. The anodic UV photocurrent I_{UV} (compare Fig. 2.6) flows into the emitter of Q_{13} and

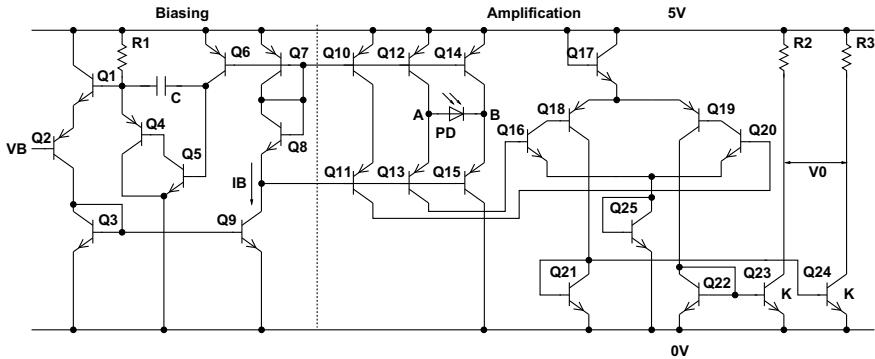


Fig. 6.12 Circuit diagram of a UV sensitive OEIC [11]

is injected into the base of Q_{16} . Transistor Q_{16} amplifies the photocurrent by its current gain factor β_{16} . This amplified current forms the base current of Q_{18} . At the collector of Q_{18} , the photocurrent is amplified by the value of the product $\beta_{16} \times \beta_{18}$. The collector current of Q_{18} is mirrored into Q_{24} by Q_{21} and finally transformed into a voltage by R_3 .

The infrared-dependent cathodic current $I_{UV} + I_{IR}$ (see Sect. 2.1.3) is shunted to V_{CC} by Q_{14} . The transistors Q_{10} and Q_{11} supply a reference bias current I_B to Q_{20} , which is the input of the second branch of the differential amplifier with Q_{16} , Q_{18} , Q_{19} , and Q_{20} . A reference current amplified by β_{19} and β_{20} is mirrored via Q_{22} and Q_{23} to R_2 . The voltage V_o across the output terminals of the circuit is, therefore, given by

$$V_0 = \beta_{16}\beta_{18}KR_3(I_{UV} + I_B) - \beta_{19}\beta_{20}KR_2I_B. \quad (6.1)$$

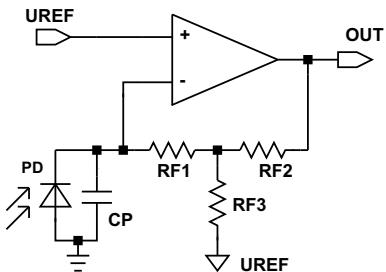
When perfect device matching ($Q_{16} = Q_{20}$, $Q_{18} = Q_{19}$, and $R_2 = R_3$) can be assumed, the output voltage V_o does not depend on the bias current I_B :

$$V_9 = \beta_{16}\beta_{18}KR_3I_{\text{UV}}. \quad (6.2)$$

For the complementary bipolar process, β is approximately 140. R_3 was designed to be $28\text{ k}\Omega$, and the mirror factor K was 2. This resulted in a transimpedance of $1.1 \times 10^9 \text{ V/A}$.

Although the output voltage is independent of I_B , I_B has to be very well controlled for correct operation and it has to be very small, because of the large transimpedance value. The bias section Q_1-Q_9 replicates the gain stage (Q_4 corresponds to Q_{18} , Q_5 corresponds to Q_{16} , and $R_1 = R_3$) and feeds back the proper bias current via Q_6 , Q_{10} , and Q_{12} . I_B can be adjusted accurately in the nA range with the reference voltage V_B . For V_B ranging from 0 to 3.5 V, I_B is adjustable between 15 and 0 nA. The compensation capacitor $C = 12 \text{ pF}$ is needed for the stability of the feedback loop.

Fig. 6.13 T-type closed-loop configuration for high transimpedance gain [12]



The response time of the sensor of less than 100 ms was determined by the capacitance of the UV photodiode and the small photocurrents. The input-equivalent noise was smaller than $3.7 \text{ pA}/\sqrt{\text{Hz}}$ at 1 Hz. The power consumption of the UV-OEIC was 4 mW at 5 V. The total chip area was 4 mm^2 of which the UV photodiode occupied 1 mm^2 .

After this example of an open loop very-high-gain amplifier, an amplifier with a T-type feedback network will be explained. Such a bipolar preamplifier OEIC for compact disk (CD) systems was described in [13]. The amplifier provides a high transimpedance gain, i.e. a low photocurrent is converted to a large voltage, and a relatively large bandwidth. In order to achieve these properties, the feedback via the T-type network shown in Fig. 6.13 is applied. The T-type network consists of the resistors R_{F1} , R_{F2} , and R_{F3} , whereby the values of R_{F1} and R_{F2} were chosen to be equal in [13]. The T-type network is an appropriate measure to simulate a high resistance R_F with low resistor values. The effective value R_F is

$$R_F = (R_{F1} R_{F2} + R_{F1} R_{F3} + R_{F2} R_{F3}) / R_{F3} \quad (6.3)$$

and the output voltage V_o is obtained

$$V_o = -I_{ph} R_F. \quad (6.4)$$

In such a way it is possible to construct high-gain amplifiers without a high-resistivity polysilicon process module. Emitter polysilicon or gate polysilicon in a (Bi)CMOS process is sufficient. The T-type feedback can also be considered as a means to avoid large RC time constants of large resistance values, requiring a large polysilicon area with a large parasitic capacitance. Effective resistance values of $82 \text{ k}\Omega$ for a maximum photocurrent of $1.2 \mu\text{A}$ and of $328 \text{ k}\Omega$ for a photocurrent of $0.3 \mu\text{A}$ were realized in [13], whereby the true resistors had much lower values and the die area could be kept low at $400 \times 350 \mu\text{m}^2$. It should be mentioned, however, that the input offset voltage of the operational amplifier is also amplified [12].

The circuit is shown in Fig. 6.14. Only NPN transistors are used in the OEIC for a compact disk (CD) system in order to achieve a large bandwidth. The transit frequency of the NPN transistors was 1.5 GHz. The operational amplifier has the voltage followers Q3 and Q4 in front of the common-emitter difference amplifier

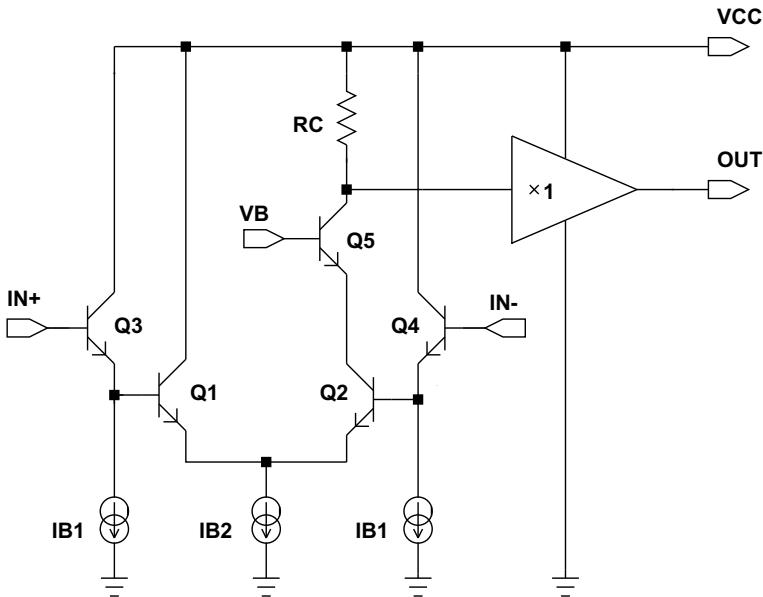


Fig. 6.14 Simplified circuit diagram of a bipolar OEIC for CD systems [13]

stage Q1/Q2 to obtain a low input current, whereby a large offset voltage due to the voltage drop across the T-type network caused by the base current of Q2 can be avoided.

The transistors Q2 and Q5 form a cascode stage to avoid a large Miller capacitance of Q2. High performance PNP transistors were not available and instead of a PNP current mirror load, the resistor R_C is used. Another voltage follower is used in order to obtain a low output impedance and to isolate the collector of Q5 from the load capacitance. The low-frequency open-loop gain was estimated to be $A_0 = 0.5g_m R_C = 40$. A compensation network was reported to be necessary, however, it was not described in [13]. The photodiodes used in the CD-OEIC also were not described.

The complete CD-OEIC contained fast channels with a bandwidth of 16 MHz for a maximum photocurrent of $1.2 \mu\text{A}$ and slower channels for a photocurrent of $0.3 \mu\text{A}$. For the fast channels, rise and fall times of 22 ns with a settling time to 0.1% of 200 ns were reported. The systematic offset voltage due to the base current of Q4 was smaller than 4 mV. The power consumption for one fast channel was 9.8 mW at 5 V.

6.4.2 Two-Dimensional CMOS Imagers

In Sect. 2.2.9, the concept of Thin Film on ASIC (TFA) was described. As an alternative to a self-structuring technology for the a-Si photodetectors in image sensors, an

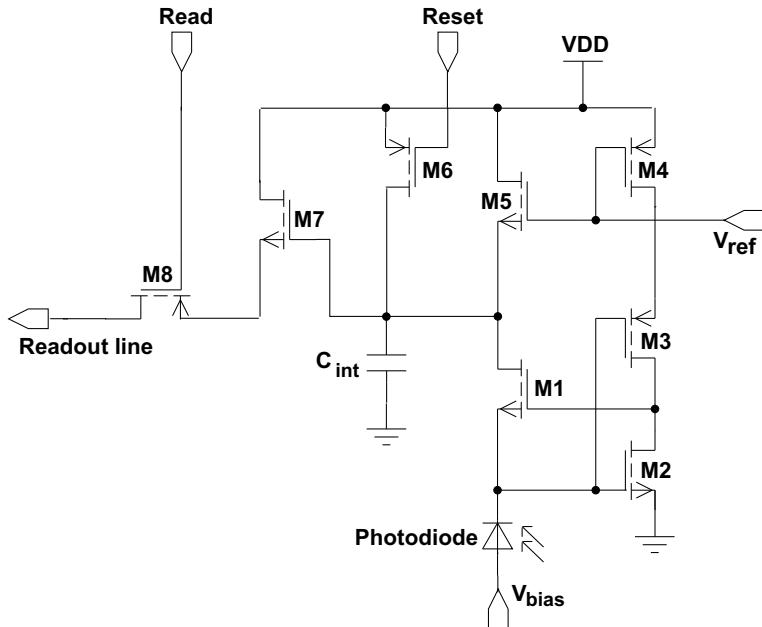


Fig. 6.15 Circuit diagram of a pixel in AIDA for operating the photodiode in a constant voltage mode [14]

electronic circuit within each pixel was presented which reduces cross-talk between neighboring pixels [14]. The TFA sensor overcoming the coupling effect of neighboring photodetectors in an unstructured a-Si:H film by electronic means was called AIDA (Analog Image Detector Array). A circuit inside each pixel (in c-Si) provides here a constant rear electrode potential for the photodetectors, thereby eliminating lateral currents between neighboring photodetectors in the a-Si:H film. The photodetectors are used in a constant voltage mode. The circuit diagram of a pixel is given in Fig. 6.15. Each pixel consists of an a-Si:H photodetector, eight MOSFETs and one integration capacitance C_{int} . C_{int} is discharged by the photocurrent. The inverter M2, M3 and the source follower feedback M1 keep the cathode voltage of the detector constant. M4 limits the power consumption of the inverter. M5 restricts the minimum voltage across the integration capacitance to 1.2 V in order to always keep the constant voltage circuit working. The integrated voltage on C_{int} is read out via M7 in source follower configuration and via the switch M8. The reset operation is performed as M6 recharges C_{int} after readout. The effective integration time of the pixel is the time period between two reset pulses, because readout is nondestructive and is performed at the end of the integration period.

The integration time may be varied according to the brightness of the scene. By this means, the sensitivity is controlled for all pixels globally. The AIDA sensor consists of 128×128 pixels with a size of $25 \times 25 \mu\text{m}^2$ each. The dynamic range of

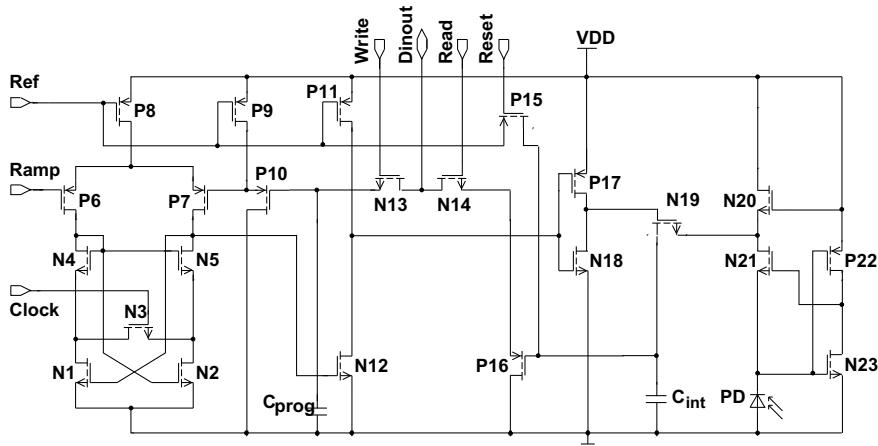


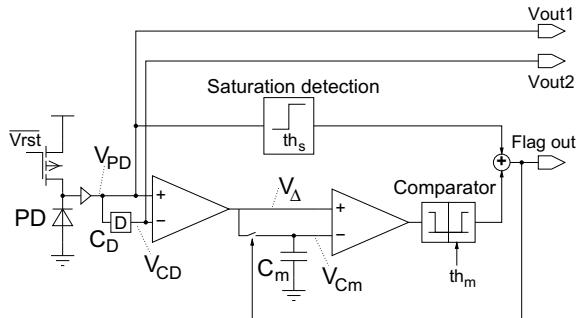
Fig. 6.16 Pixel circuit diagram of a locally adaptive image sensor [14]

the sensor amounts to 60 dB for an integration time of 20 ms. The dynamic range can be extended significantly by means of the sensitivity control. The sensor was tested for illumination levels as high as 80,000 Lux. No blooming effects or image lag were observed [14].

For applications of an image sensor in a vehicle guidance system, for instance, which requires a very high degree of safety, the global sensitivity control is not appropriate. A number of pixels with excessive illumination may be saturated, whereas only slightly illuminated pixels may generate signal voltages below the noise and dark current levels. As pixels with logarithmic output characteristics exhibited a seriously increased sensitivity to temperature changes and fixed pattern noise, a Locally Adaptive Sensor in TFA-technology (TFA-LAS) was suggested [14]. The TFA-LAS allows to control the integration time and, therefore, the sensitivity of each pixel individually [15]. Figure 6.16 gives the complete pixel circuitry realized in the c-Si below each a-Si:H pixel photodetector.

The photocurrent is integrated into the MOS capacitance C_{int} while the rear electrode of the photodiode (cathode) is kept at a constant potential (compare Fig. 6.15). The integration time value is calculated externally for each illumination period and programmed into the pixel as an analog voltage V_{prog} , which is stored on the capacitor C_{prog} . V_{prog} standing at $Dinout$, is switched via N13 to C_{prog} for this purpose. This voltage on C_{prog} is compared to a linear voltage ramp generated by the peripheral electronics during the integration phase. The comparator consisting of the transistors N1–N5 and P6–P8 starts the integration as soon as the voltage ramp rises above V_{prog} and stops it at the falling edge of the ramp. A standard 0.7 μ m CMOS ASIC technology implementing the TFA-LAS pixel schematic of Fig. 6.16 enabled a dynamic illumination range of more than 100 dB throughout the complete pixel array at any time. This corresponds to the outstanding dynamic range of c-Si PIN detectors, which is over 100 dB at an illumination intensity of 1000 Lux. For the TFA-LAS, the voltage

Fig. 6.17 Processing scheme for adaptive integration time in each pixel [16]



range for the pixel signal amounts to 54 dB. The remaining dynamic range of 46 dB is included in the integration time and, therefore, in the programming voltage. The combination of both signal and programming voltage thus gives the information on the illumination level of a specific pixel. The TFA-LAS consisted of 64×64 pixels with a size of $40 \times 50 \mu\text{m}^2$ each.

An image sensor in which each pixel adapts its integration time to motion and light intensity was proposed in [16]. The integration time is shortened when motion is detected in the pixel or when pixel intensity becomes saturated. The adaptivity to motion and light significantly enhances temporal resolution and dynamic range of the image sensor. A scene containing both bright and dark regions can be captured by the pixels with shorter and longer integration times, respectively. Because of the adaptivity to motion, a higher temporal resolution is obtained in a moving area and a higher signal-to-noise ratio is achieved in a static area. The proposed sensor can be utilized for either high-speed imaging or wide dynamic range imaging, which is, for instance, beneficial to imaging systems for vehicles.

In order to control the integration time pixel by pixel, signal processing circuits are combined with the image sensor. The processing scheme of each pixel based on motion detection and saturation detection is shown in Fig. 6.17. Each pixel holds the integrated charge on the photodiode capacitance until motion or saturation is detected. Motion and saturation detection is processed every t_Δ seconds, which is the shortest integration interval. t_Δ was set very small because the proposed sensor was intended to operate at a high frame rate [16].

The motion detection works as follows. First, V_Δ corresponding to the signal integrated during the shortest interval t_Δ is calculated by the difference between V_{PD} and V_{CD} (see Fig. 6.17). V_{PD} corresponds to the integration on the photodiode from the last reset to the present. V_{CD} is the voltage on the memory capacitance C_D which is delayed by t_Δ and stems from the previous integration. V_Δ , therefore, can be considered as the change in pixel intensity during a t_Δ integration time. C_m is another memory capacitor that keeps the V_Δ of the last output. When the difference between V_Δ and V_{Cm} exceeds a certain threshold th_m , the pixel intensity is judged to have significantly changed and the pixel is considered to have observed motion. When this occurs a flag signal is set and the pixel outputs V_{PD} and V_{CD} . Furthermore,

the new V_{Δ} is stored on C_m and the photodiode is reset and integration is restarted, then.

The saturation is detected when V_{PD} exceeds the threshold th_s (Fig. 6.17). The flag signal is also activated and V_{PD} and V_{CD} are output, when this occurs. V_{Cm} is also over-written by the corresponding V_{Δ} , and the photodiode is reset and restarts integration. If the pixel detects no motion or saturation, the photodiode is not reset and keeps integrating without outputting V_{PD} and V_{CD} .

A prototype with 32×32 pixels of the adaptive image sensor was fabricated in a 1-poly 2-metal $1\text{ }\mu\text{m}$ CMOS technology [16]. The pixel size was $85 \times 85\text{ }\mu\text{m}^2$. Together with memory and processing blocks, the total die size was $4.0 \times 6.1\text{ mm}^2$. Each pixel contained 17 transistors for processing and 10 transistors for memory. Processing required 64 transistors per column in addition. A fill factor of 14% was given. Power dissipation was 150 mW at 5 V. The minimum integration interval was $680\text{ }\mu\text{s}$ and the maximum integration interval was 16 ms in order to be able to display the output image on a monitor. A dynamic range of 56 dB, a readout noise of 3.1 mV RMS, a saturation charge level of 1,860,000 electrons, and a conversion gain of $1.1\text{ }\mu\text{V}$ per electron were achieved [16]. A good scalability for larger pixel arrays and low power consumption was claimed. In the case of 512×512 pixels, a power consumption of 2.4 W was estimated [16].

An interesting solution for a single-chip CMOS camera with logarithmic response was suggested [17]. The high-dynamic-range CMOS image sensor implements non-integrating, continuously working photoreceptors with logarithmic response. The uniformity problem caused by device-to-device variations is greatly reduced by implementation of an analog self-calibration resulting in a fixed pattern noise (FPN) of 3.8% (RMS) of an intensity decade at a uniform illumination of 1 W/m^2 . The sensor provides a resolution of 384×288 pixels and a dynamic range of six decades in the intensity region from 3 to 3 kW/m^2 spanning the range from moon light to sun and bright studio light. The image sensor contains all components required for operating as a camera-on-a-chip.

The method of correlated double sampling (CDS) is usually implemented in integrating image sensors [18]. The individual pixel offsets are corrected by taking the difference between the output signals before integration (reset state) and after integration. This concept, however, fails for continuously working photoreceptors, since there is no reset state. Off-chip methods with digital calibration using a frame memory for storing the individual pixel offsets have been established [19, 20]. Compared to another single-chip approach [21], the new solution achieves better correction due to a higher number of transistors and an additional capacitor.

Calibration is performed by a reference current instead of a photocurrent. All photoreceptors are stimulated by the same reference current during the calibration cycle. Without FPN, all pixel outputs would show an identical signal. In reality, however, there are device-to-device variations and these signals differ from each other. The self-calibration concept is shown in Fig. 6.18. An operational amplifier compares the individual output voltage to a reference voltage and adjusts each pixel until both voltages are equal. Then, the calibrated pixel state is stored on an analog memory (capacitor C) in every photoreceptor. Because the calibration amplifier is

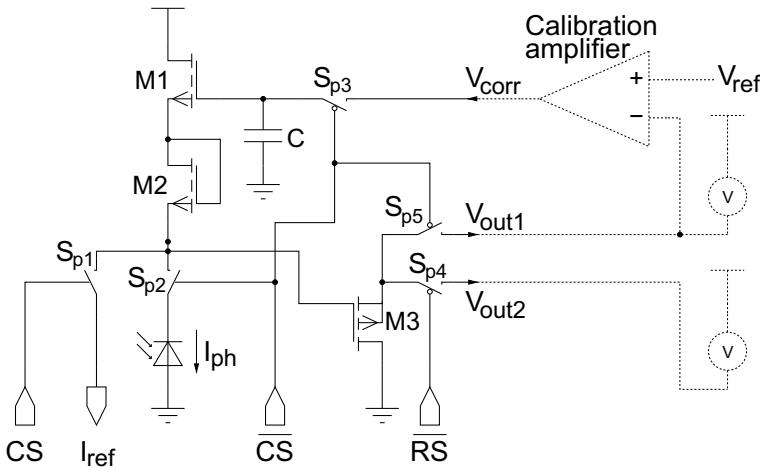


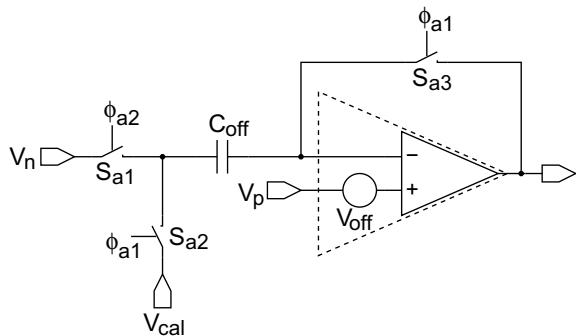
Fig. 6.18 Circuit diagram of self-calibrating logarithmic pixel [17]

very area consuming, it is not included in the pixel itself, but is located at the border of the sensor array. One amplifier belongs to all pixels of one array column and calibrates them sequentially.

The pixel switches S_{p1} to S_{p5} are realized as single MOS transistors. PMOS switches in contrast to NMOS switches are drawn with a circle. The control signals CS , \bar{CS} , and \bar{RS} are connected to all pixels of the same row, the lines I_{ref} , V_{out1} , V_{out2} , and V_{corr} belong to all pixels of the same column. During image acquisition the control line CS (calibration select) is set to LOW and the inverted line \bar{CS} to HIGH. The switch S_{p2} consequently is closed whereas the switches S_{p1} , S_{p3} , and S_{p5} are open. The transistors $M1$ and $M2$ working in subthreshold region for weak photocurrents convert the photocurrent I_{ph} into the logarithmic voltage V_{log} . The two transistors in series result in a doubled signal slope compared to a single transistor. The sensor signal V_{log} is buffered by the PMOS source follower $M3$. The current required for the operation of this buffer is provided by a current source located outside the pixel and shared with all pixels in a column. To select one pixel for readout, the control signal RS is made LOW switching on S_{p4} and connecting the buffer $M3$ to the V_{out2} line.

When CS is made HIGH and \bar{CS} therefore becomes LOW, the switches S_{p1} , S_{p3} , and S_{p5} are closed and S_{p2} is opened. The image sensor changes to the calibration mode. The receptor circuits are no longer stimulated by the photocurrents but by the reference current I_{ref} . The sensor signal in calibration mode $V_{log,cal}$ is connected to the V_{out1} line guiding the sensor signal to the calibration amplifier. This operational amplifier compares V_{out1} to the reference voltage V_{ref} and delivers the correction voltage $V_{corr} = A(V_{ref} - V_{out1})$ where A is the gain of the calibration amplifier. A change of V_{corr} is transferred to $V_{log,cal}$ via $M1$ and $M2$. The receptor circuit in

Fig. 6.19 Circuit diagram of autozeroing calibration amplifier [17]



calibration mode, therefore, forms a feedback loop composed of the logarithmic photosensor and the operational amplifier.

When the pixel returns to the image acquisition mode for CS made LOW and \overline{CS} made HIGH, S_{p3} is opened and V_{corr} is stored on the pixel capacitor C. Now, the photocurrent I_{ph} flows through M1 and M2. Due to the previous calibration, V_{out2} does not depend on the transistors M1, M2, and M3 and their actual properties. The effect of mismatch of these transistors in different pixels is removed by the calibration. Since mismatch of the photodiode responsivity or of charge injection of the switch S_{p3} is much lower, the originally dominating sources of mismatch, i.e. of FPN, are eliminated by the calibration. After calibration, however, mismatch of the photodiode responsivity and of charge injection of the switch S_{p3} are responsible for the remaining FPN.

To avoid variations between individual columns, the reference current sources and the calibration amplifier have to match precisely. The reference current sources are implemented as single MOS transistors biased with an adjustable gate voltage to adapt the reference current to the actual requirements. To achieve a good matching, each transistor was divided into five parts and spread over four adjacent columns. The drain current matching was found to be better than 3% (RMS) for a reference current of 50 pA [17]. The input offset voltage of the calibration amplifier is reduced by implementing the autozeroing concept [22] depicted in Fig. 6.19. The feedback path through S_{a3} with Φ_{a1} HIGH allows to store the intrinsic amplifier offset V_{off} on the capacitor C_{off} . During normal operation Φ_{a1} is LOW and both inputs V_n and V_p are now shifted by the offset stored on C_{off} leading to a differential input offset of zero. In order to reduce the FPN strongly by the self-calibration mechanism, the amplifier has to provide a high gain [17].

The architecture of the complete image sensor implementing the described self-calibration mechanism is shown in Fig. 6.20. The sensor array contains 386×290 pixels, of which 384×288 can be selected for readout. The additional outer rows and columns are dummy structures to avoid variations in the outer visible pixels due to border effects. The autozeroing calibration operational amplifiers and the reference current mirrors are located above the sensor array. A clock circuit provides nonoverlapping clocks to control the calibration amplifiers. The reference current

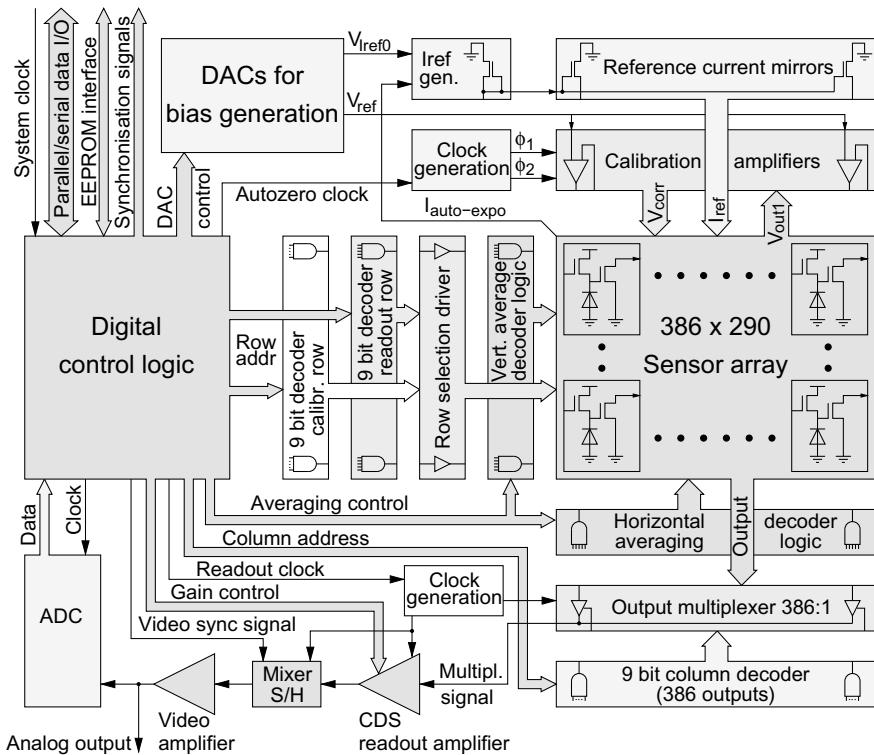
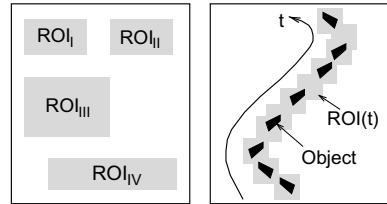


Fig. 6.20 Architecture of the complete self-calibrating logarithmic image sensor [17]

can be adapted with the help of a mirror circuit with adjustable gain. The bias generation block contains 19 digital-to-analog converters (DACs) each providing a voltage programmable in the range from 0 to 5 V. These voltages were required to bias and control the analog sensor circuits.

9-bit decoders and row drivers for selecting the calibration and readout row are placed to the left of the photosensor array. During readout the pixel signals are guided to the analog output multiplexer controlled by the 9-bit column decoder located below. CDS is applied in the readout amplifier to eliminate column FPN. Subsequently, a mixer with a sample-and-hold stage combines the sensor output with the video synchronization signal which is amplified by the video amplifier. An integrated analog-to-digital converter (ADC) generates a 10-bit digital value which can be read out via a parallel interface or a high-speed serial link. The digital logic block on the left side is responsible for the overall control of the image sensor chip. It enables operations like zooming or averaging and it selects all timing parameters. An EEPROM interface offers the possibility to save the chip parameter values in an external EEPROM. They can be automatically recovered after a system or power-on reset.

Fig. 6.21 Region-of-interest configurations (left: multiple regions of different size; right: target tracking) [23]

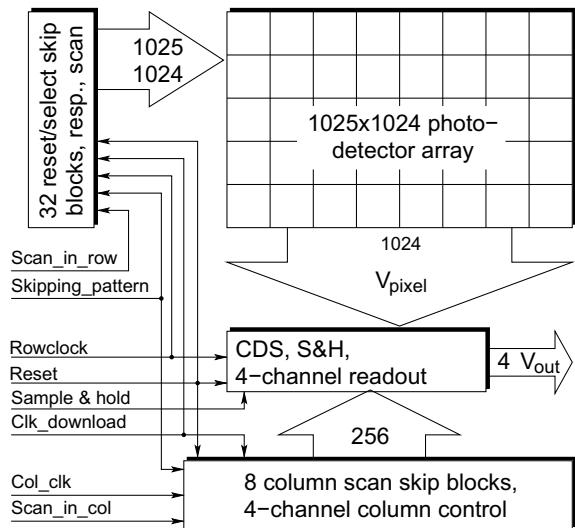


The self-calibrating logarithmic single-chip camera has been designed and fabricated in a $0.6\text{ }\mu\text{m}$ CMOS process [17]. Only one polysilicon layer was provided by this process. Therefore, all capacitors were implemented as metal-metal-poly sandwich structures or as MOS capacitors. The third metal layer has been used to protect all devices besides the photodiodes from the incident light. The photodiodes were N^+/P -substrate diodes with a quantum efficiency of approximately 50% at 625 nm and a capacitance of 100 fF . The fill factor was about 30%. The pixel pitch was quite large and amounted to $24\text{ }\mu\text{m}$ due to the high number of 10 transistors per pixel and due to the pixel capacitor with 150 fF realized as a MOS capacitor. The active die area was $11.5 \times 7.7\text{ mm}^2$. The photosensor array itself covered $9.2 \times 6.9\text{ mm}^2$ corresponding to somewhat more than the size of a 2/3-inch CCD sensor [17]. The slope of the logarithmic sensor could be adjusted between 130 and 720 mV per decade by changing the feedback capacitors in the switched-capacitor readout amplifier. With the help of reference structures it was found that the calibration mechanism improved the pixel nonuniformities by a factor of 10 or more. The power consumption of the image sensor was 150 mW at 5 V . The maximum pixel rate was 8 MHz [17].

Sometimes it is interesting to read out image areas called “regions of interest” (ROI). Figure 6.21 shows different ROI configurations of a $1\text{k} \times 1\text{k}$ CMOS image sensor [23]. One possible readout operation mode allows to read out several ROIs ($\text{ROI}_I \dots \text{ROI}_{IV}$) with different sizes and positions. Another possible application is target tracking where the ROI can follow the moving object. Both the start position and the size of each ROI are quantized at 32 pixels. The advantage of dividing the sensor into subgroups of 32×32 pixels is that a lot of chip area can be saved compared to a complete on-chip decoder for fully random access. It was stated that about 95% of the area for such a decoder were saved by the ROI block technique [23].

The architecture of the ROI imager is shown in Fig. 6.22. The CMOS image sensor in $0.5\text{ }\mu\text{m}$ technology contains a 1025×1024 pixel array with each pixel implementing the same pixel circuit as shown in Fig. 2.36. The row with number 1025 is used as dark row with light-independent pixels. These are used to compensate for dark current and channel mismatch. The digital circuitry at the left side of the pixel array contains shift registers for reset and select operation (exposure control) of the image sensor and the logic for ROI readout. Correlated double sampling (CDS) located at the bottom of each column is implemented to significantly reduce $1/f$ -noise and fixed pattern noise (FPN). A column parallel sample&hold stage and an analog four-channel multiplexer are implemented to provide a video frame rate at 512×512 pixel image resolution.

Fig. 6.22 Architecture of region-of-interest imager [23]



The chip area of the ROI imager realized with a standard N-well 0.5 μm CMOS process was 164 mm^2 . The pixel pitch was 10 $\mu\text{m} \times 10 \mu\text{m}$ with a fill factor of 41%. With a full frame resolution 15 frames per second were possible. With one integration time a dynamic range of 61 dB was reported. Using a multi-exposure technique the dynamic range could be extended to 92 dB [23]. The power dissipation was 300 mW at 3.3 V.

Another interesting CMOS image sensor in bulk silicon should be mentioned here. It combines a lateral bipolar phototransistor array and a current comparator for digitizing the image [24]. The lateral bipolar phototransistor described in Sect. 2.2.10, Fig. 2.40, was used as a photodetector in a fingerprint detection chip fabricated in standard CMOS technology. The fingerprint detection chip contained an 64×64 array of the lateral phototransistors.

The phototransistors in the array were scanned by connecting one at a time to a current comparator using MOS transistors as selection switches. The circuit of the current comparator is shown in Fig. 6.23.

A threshold must be established so that pixel current values may be compared in order to give a black/white image. The most convenient point to place the threshold is the average of all pixel currents in order to obtain a global average. It also may be advantageous to select only m pixels from the entire array to give a local average from a sub-array. The average of the pixel currents is then obtained by dividing the measured current by m . In the fingerprint detection system, for instance, four rows of the 64×64 array were used and a 256:1 current mirror was used to give the average pixel current. The current mirror gate voltage is stored on a 10 pF capacitor. From this capacitor the reference voltage V_{ref} is derived setting the reference current for the current comparator. During the following 4096 clock cycles, all pixels are selected one at a time and their photocurrents are digitized to '1' or '0' by the current

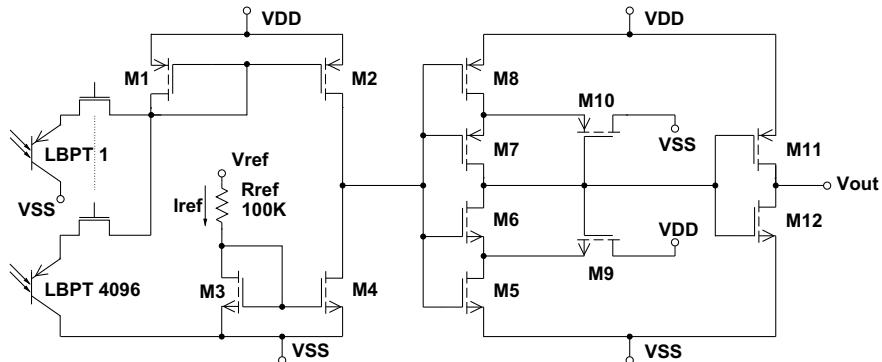
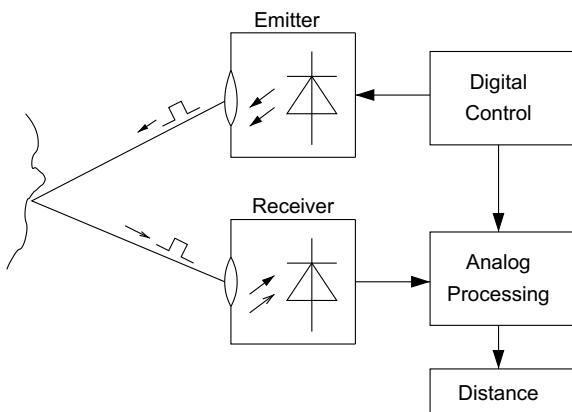


Fig. 6.23 Current comparator circuit of a fingerprint detector [24]

Fig. 6.24 Principle for optical distance measurement [25]



comparator. During each clock cycle, one selection MOS switch is activated and the pixel current is pulled through the PMOS current mirror M1 and M2 (Fig. 6.23). If this pixel current is greater than the average current, which was set up through M3 and M4, V_{out} goes high; otherwise V_{out} goes low. The transistors M5–M12 compose a noninverting Schmitt trigger, which imposes a hysteresis and, in turn, stable digitization.

The field of application of such an image detection system is not limited to a fingerprint detection system, of course. Other types of pictures can also be digitized.

6.4.3 Optical Distance Measurement Circuits

The so-called time-of-flight (TOF) method is often used for optical distance measurement. The principle of TOF is shown in Fig. 6.24.

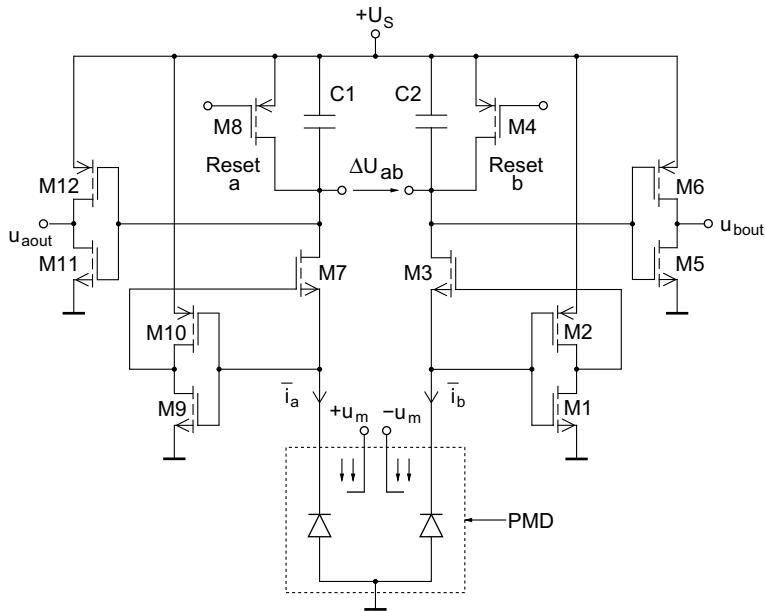


Fig. 6.25 Circuit for optical distance measurement with PMD [27]

A light-emitting diode (LED) or a laser diode is used to send a light pulse. The light reflected at the object to which the distance has to be determined is detected by a receiver. The time difference t_{of} between emission of the light pulse and its reception at the receiver is directly proportional to the distance:

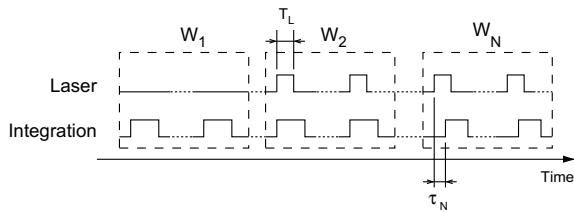
$$d_{\text{obj}} = \frac{c_0 t_{\text{of}}}{2} \quad (6.5)$$

where c_0 is the velocity of light in vacuum or air. For short distances, where t_{of} is shorter than the light pulse, the phase shift from emitted pulse to detected signal can be used to determine the distance.

A time-of-flight optical distance measurement circuit can be advantageously based on the CMOS photonic mixer device (CMOS PMD) described in Sect. 2.2.11. The PMD combines the detection of the light and the correlation of this optical signal with the electrical signal used for modulation of the LED or laser diode [26, 27]. For short distances, the CMOS PMD, therefore, can be used as a detector for the phase difference between this light detected after reflection and this electrical signal. Figure 6.25 shows a circuit appropriate for optical distance measurement with a PMD.

The electrical signal that modulates the light source is applied to the two gates of the PMD in a differential form ($+u_m$ and $-u_m$). The photocurrents of the PMD i_a and i_b flow through the NMOS transistors M7 and M3, respectively. The inverters M9

Fig. 6.26 Successive integration with N windows for each distance measurement [25]



and M10 with the source follower M7 as well as M1 and M2 with the source follower M3 keep the potential at the PMD source and drain largely independent from the size of the photocurrents by decoupling the PMD from the load capacitors C1 and C2. The PMD source/drain potential is kept at the inverter threshold which is at about $U_s/2 = 2.5$ V. The photocurrents of the PMD i_a and i_b charge the capacitors C1 and C2. With a delay of the received light pulse compared to the electrical modulation signal due to the time-of-flight, a different charge is accumulated on the two capacitors resulting in a voltage difference. Simply speaking, the voltage difference ΔU_{ab} is proportional to the optical distance between the measurement unit and the target. Actually the sum of both charges also has to be determined to eliminate the influence of the target reflectance, since the distance is proportional to $\Delta U_{ab}/(\Delta U_a + \Delta U_b)$. The inverters M5 and M6 as well as M11 and M12 amplify the voltage difference ΔU_{ab} to $U_{aout} - U_{bout}$. A good matching between these inverters is essential. Background light is integrated on both capacitors in the same way. Without precautions like compensation of background light it can drive the inverters into saturation. In practice, measurements with at least three different phase differences between electrical laser modulation signal and u_m are performed to obtain an unequivocal distance result [27].

When no such a PMD shall be used, conventional photodiodes can be used as a light detector. Background light can be measured without any laser pulses in the cycle W_1 (Fig. 6.26). The following cycles are used to determine the time-of-flight of the laser echo. A number of $N - 1$ consecutive integration windows is used to reduce the influence of noise on the distance measurement. The basic idea of these consecutive integration windows is to accumulate the small signal caused by each pulse, adding at each pulse the voltage signal of the last packet to the previous ones for a suitable number of pulses. A better signal-to-noise ratio is obtained by averaging the noise contributions on many samples.

Figure 6.27 shows the block diagram of an implemented pixel architecture. The photodiode read-out stage is a voltage amplifier. A self-biasing cascode amplifier resulting in a good gain, low input-referred noise, immunity to transistor mismatch, and good pixel-to-pixel uniformity was chosen [25].

The operation of the first stage is characterized by three major steps [25]: (i) the photodiode capacitance is reset to V_{pol} by switching on transistor S_{res} . (ii) The cascode amplifier is properly biased by switching S_{bias} on; the two transistors Mn1 and Mp2 are forced into their saturation region, biasing the amplifier at its highest gain operating point regardless of transistor mismatch. (iii) The switch S_{bias} is finally

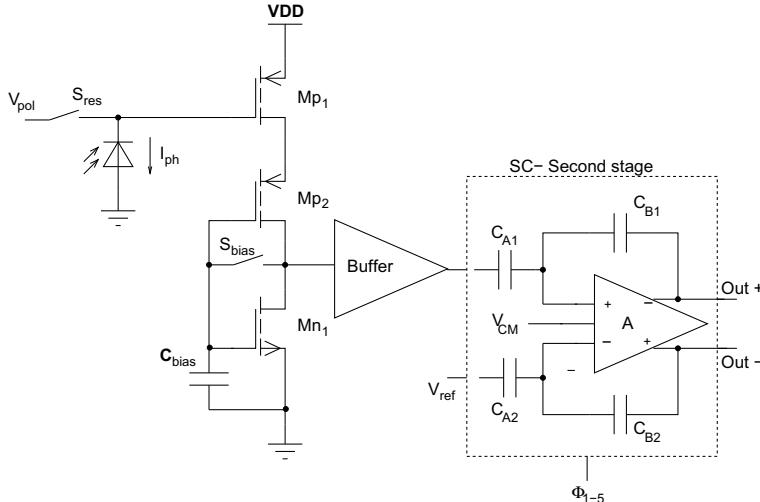


Fig. 6.27 Block diagram of circuit for optical distance measurement [25]

opened. A voltage value suitable to keep the amplifier in the high-gain region is sampled on C_{bias} and the amplifier works as a standard cascode amplifier. The gain of the amplifier implementation was 45 with an input-referred noise of $13 \mu V_{rms}$.

The second stage (Fig. 6.27) performs the correlated double sampling (CDS) filtering and the charge accumulation. The greatest parts of kT/C and flicker noise contributions are removed. A fully differential topology was chosen to reduce switch charge injection effects and “environmental” noise because of its good common-mode signal rejection ratio. Switched-capacitor (SC) circuits with their digital noisy power supply lines, therefore, become possible. A folded cascode architecture was employed in the SC-amplifier resulting in high gain, small area occupation, low noise, and low power consumption.

The operation of the second stage is like this [25]: The accumulation capacitances $C_{B1,2}$ are reset first while the OTA is kept in a voltage follower configuration and its input offset is sampled onto the feedback capacitances. Then the first stage reset value (including low-frequency noise contribution) is sampled onto C_{A1} , while the reference value V_{ref} is sampled onto C_{A2} . Then the charge stored onto $C_{A1,2}$ is discharged onto the feedback capacitors $C_{B1,2}$ and the amplifier outputs change to the reset value $\Delta V_{Out_1} = Out^+ - Out^- = V_{res}$. The signal value V_{sig} is subsequently sampled onto C_{A2} (while V_{ref} is sampled onto C_{A1}) and the stored charge is then fed to $C_{B1,2}$. After the five cycle procedure, the amplifier output gives $\Delta V_{Out_1} = V_{res} - V_{sig}$. The five-cycle procedure is repeated at each pulse, thereby accumulating the charge purged by the reset and noise equivalent charge. The output signal after the i -th packet is $\Delta V_{Out_i} = \Delta V_{Out_{i-1}} + (V_{res} - V_{sig})_i$.

A test chip fabricated in a $0.6 \mu m$ 3M-2P CMOS technology had a good accuracy for distances from 7.5 to 10m at pulse numbers $N = 64$ and $N = 128$. At shorter

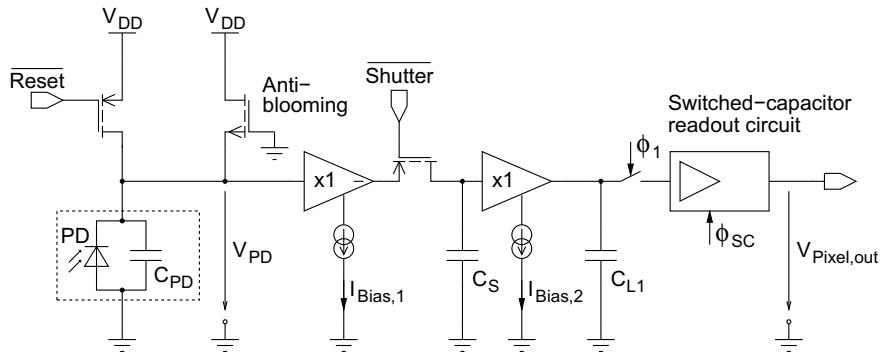


Fig. 6.28 Pixel circuit of 3D-imager [28]

distances the distance error of the test chip was up to about 20% [25]. The test chip allowed a variation of the pulse number N between 4 and 1024. The area of a pixel was $180 \times 160 \mu\text{m}^2$ with a fill factor of 14%. The circuitry was screened by metal 3 against light incidence.

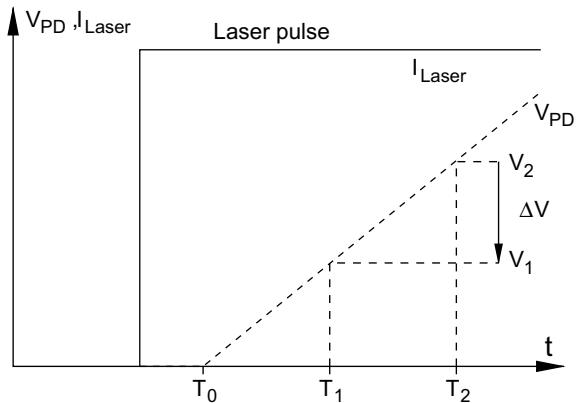
6.4.4 3D Sensors with Photodiodes in Standard CMOS

A CMOS imager chip for three-dimensional (3D) imaging applications containing a 32×2 photodiode array, fast synchronous electronic shutter, analog switched-capacitor (SC) readout, multiple double short time integration (MDSI), clocking, pulse synchronization, and control was presented [28]. These features allow optical time-of-flight (TOF) measurements of laser pulses reflected from a target. The circuit diagram of each pixel in this 3D imager is shown in Fig. 6.28.

To achieve a high speed the photodiode voltage V_{PD} is buffered by a source follower. The voltage stored on C_S is then transferred using a second buffer to a switched-capacitor readout circuit. This SC readout circuit performs several tasks: sample&hold, correlated double sampling (CDS), and analog accumulation if laser pulse bursts are used [28]. The electronic shutter is activated by switching the reset transistor off and the shutter transistor on.

The measurement principle of the 3D TOF imager is illustrated in Fig. 6.29. A light pulse of a few ns duration generated by an IR laser diode illuminates the field of view by using a simple optical diffuser to widespread the laser beam. Simultaneously or after a fixed delay time, the electronic shutter is activated. The photocurrent of the reflected light including background illumination of the scene in the field of view is integrated at the photodiode array PD. The amount of the generated charge depends on synchronous timing of the laser diode and electronic shutter as well as on the propagation delay of the reflected pulse, i.e. on the distance. After a few ns (T_1), the electronic shutter is switched off and the corresponding voltage $V_1(\text{ill})$ of each

Fig. 6.29 Principle of measurement used in the 3D-imager [28]



pixel is stored on the pixel storage capacitor C_S . This measurement is repeated with the same shutter time and without active illumination (laser is off). The resulting voltage $V_1(\text{dark})$ is then subtracted from the previous measurement resulting in $V_1 = V_1(\text{ill}) - V_1(\text{dark})$ at the SC readout circuit. A second measurement cycle with a different integration time, i.e. the shutter is closed at T_2 (see Fig. 6.29), results in a second voltage V_2 . With these two cycles the time-of-flight T_0 can be extrapolated and the distance d can be obtained as [28]:

$$d = \frac{1}{2} c_0 \frac{V_2 T_1 - V_1 T_2}{\Delta V}, \quad (6.6)$$

where c_0 is the velocity of light. With this approach the influence of the background light and the reflectivity of the object are cancelled.

Optionally to increase the accuracy or the distance range, each of the two measurement cycles may be repeated m times applying laser pulse bursts thus yielding MDSI [28]. The resulting voltage differences are accumulated in the SC readout circuit. An improvement of the signal-to-noise ratio (SNR) by a factor \sqrt{m} results extending the range of the distance sensor.

Several important aspects have to be mentioned. The CDS operation reduces not only offsets and low frequency noise of the buffers but also of the SC readout circuit. Shutter clocking is very important since shutter phase noise, i.e. a jitter or time offset between the different shutters in the array, results in a distance inaccuracy. A shutter phase noise of 1 ps, for instance, corresponds to a 0.15 mm distance error [28]. To obtain best synchronous shutter clocking, synchronization circuits ensure minimum skew (see Fig. 6.30).

The 3D CMOS imager was fabricated in a $0.5 \mu\text{m}$ three-metal-layer, one-polysilicon (3M1P) CMOS process. Two linear photodiode arrays with 32 pixels each were integrated on the 3D imager chip. N-well/P-substrate photodiodes with an area of $260 \mu\text{m}^2$ were implemented. The die had an area of 42 mm^2 including all circuitry and bondpads. By employing subtraction of readings with laser ON and OFF

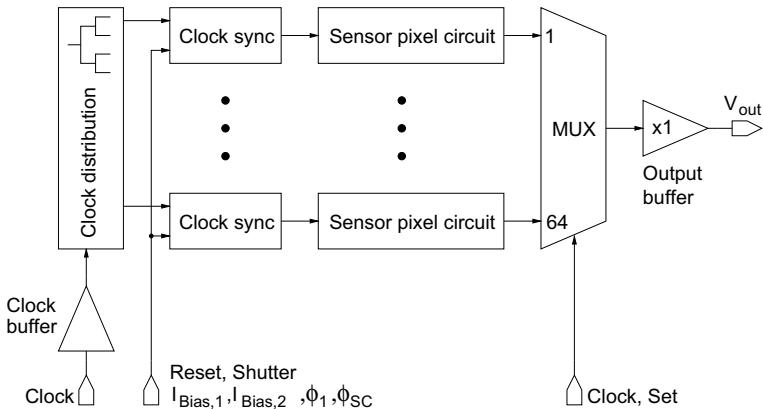


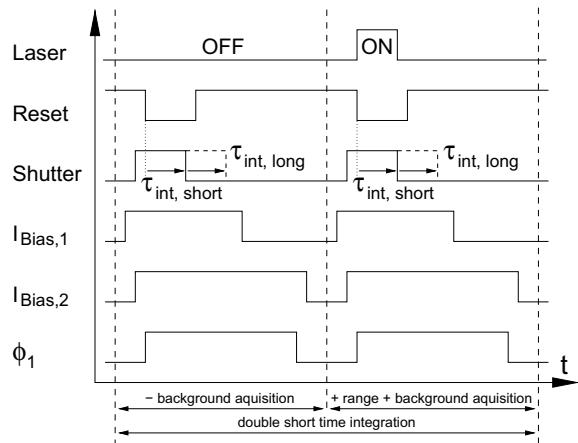
Fig. 6.30 Block diagram of 3D-imager chip [28]

and by using short pulses and shutter times, insensitivity to background illumination even with direct sun light was achieved [28]. The light falling on the chip circuitry was blocked by a metal3 shielding. Another trick was necessary to combine low-noise and high-speed in analog CMOS circuits. High bias currents are required during operation. To avoid thermal problems dynamic power management using switched bias currents I_{Bias} (see Figs. 6.28 and 6.31) was employed. The power dissipation was 330 mW at a single 3.3 V supply. The minimum shutter period was 30 ns. Measurements verified an insensitivity to background light up to 10 kLux [28]. Due to noise optimization the measured noise-equivalent-power (NEP) was 5.2 W/mm² at 30 ns shutter time. Calibrated distance measurement showed a linearity error of less than 5% for different pulse counts. For a 3D image an accuracy of ± 1 cm was reported [28]. The range resolution of less than 5 cm for one pulse and for a measurement range of more than 5 m was given. The range resolution became less than 1 cm for burst operation with 100 pulses. A maximum frame rate of 20,000 frames/s reducing to 4,000 frames/s in 100-pulses burst operation for 3D images at a 66 MHz clock was reported. Because the sensor array implemented only two pixel points in one lateral dimension, a linear mechanical scan was required for 3D image recording. The measurement range was up to 10 m depending on the number of pulses [28].

6.4.5 3D Sensors with PIN Photodiodes

The PIN photodiode reported in [29] and depicted in Fig. 2.63 was used together with a bridge circuit for correlation and background light suppression in a distance measurement sensor [30]. The parasitic capacitances of the poly-poly capacitors used in the correlation pixel circuit were reduced by placing them into the N⁻ environment of the PIN photodiode. Unfortunately this PIN photodiode BiCMOS technology was

Fig. 6.31 Pixel timing diagram of 3D-imager chip [28]



not available any longer and work on 3D sensors was continued with the technology mentioned in the following.

The PIN photodiode described in Sect. 2.3.2 and [31] was exploited in a 2×32 pixel range finding sensor [32]. It was realized in the CMOS part of a $0.6 \mu\text{m}$ BiCMOS technology. An operational amplifier was employed in each pixel to keep the voltage across the photodiode constant during integration. The area of each pixel was $158 \mu\text{m} \times 109 \mu\text{m}$. Background light suppression of this pixel worked well up to 120 klx. Due to the operational amplifier, the power consumption of each pixel was 0.1 mA at 5 V. Therefore, a more power saving approach will be described in the following.

The chip photo of a 16×16 pixel 3D sensor IC in $0.6 \mu\text{m}$ CMOS is shown in Fig. 6.32 [33]. The chip has dimensions of $3.3 \text{ mm} \times 3.0 \text{ mm}$. This sensor uses the integrated PIN photodiode described in Sect. 2.3.2 and [31]. The sensor principle is so-called indirect time-of-flight by evaluating the phase of the reflected signal. 16 phase steps were used with this 3D sensor. A correlator in each pixel allowed reconstruction of the correlation triangle from 16 measurement points. From the maximum of the correlation triangle (ϕ_{TOF}) the distance d can be determined:

$$d = \frac{c_0 t_{TOF}}{2} = \frac{c_0 \phi_{TOF}}{4\pi f_{mod}} . \quad (6.7)$$

c_0 is the velocity of light and f_{mod} is the modulation frequency of the emitted light (10 MHz square wave in [33]). The sensor determined simultaneously in each pixel the distance (i.e. ϕ_{TOF}) belonging to the corresponding image point of the scene. The pixel size was $125 \mu\text{m}$ in square with an optical fill factor of 66%. The circuit depicted in Fig. 6.33 contained only NMOS transistors with $0.6 \mu\text{m}$ gate length and $1.6 \mu\text{m}$ gate width. PMOS transistors were not used (except in logic cells) in order to avoid an N-well in the pixels and to achieve this fill factor. The two integration capacitors had a value of 0.5 pF each.

Fig. 6.32 Micro photograph of 16×16 pixel 3D sensor IC

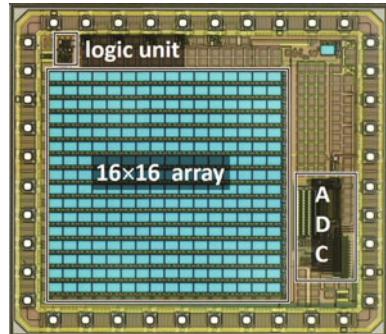
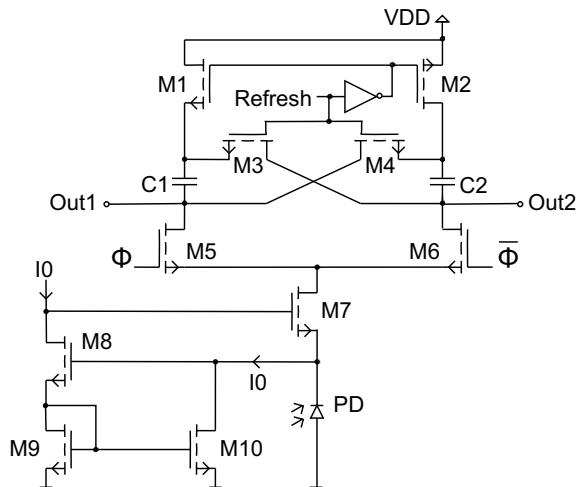


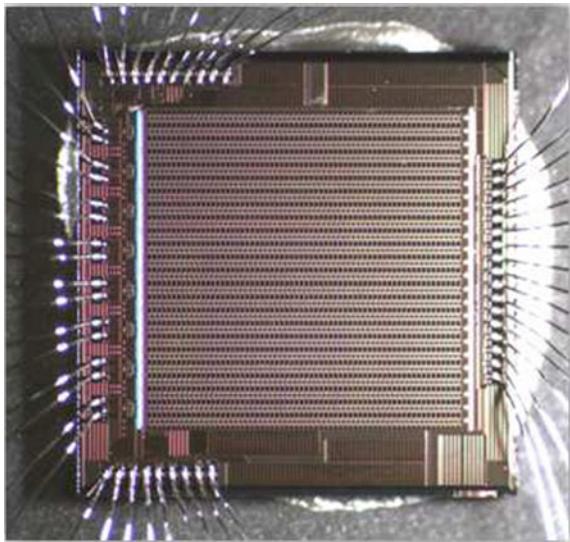
Fig. 6.33 Pixel circuit of 16×16 pixel 3D sensor IC



Since the photodiode's capacitance leads to losses, when the cathode potential changes, M7 was used to keep the voltage across the pin photodiode constant. M7 was biased with a current of $1 \mu\text{A}$ to obtain a regulation bandwidth of 100 MHz being sufficient for a square-wave modulation with 10 MHz . M8 which controls M7 needs another $1 \mu\text{A}$. The in-pixel current source I_0 generates this current, which is also mirrored via M9 and M10 to M7.

Transistors M1 to M6 represent the main part of the pixel correlation circuit. M5 and M6 switch the photocurrent either to the integration capacitor C1 or C2 steered by the modulation clock Φ and $\bar{\Phi}$. After some integration cycles, a refresh is applied, during which M1 and M2 isolate the capacitors C1 and C2 from VDD and M3 and M4 connect C1 and C2 in an anti-parallel way. In such a way the integrated common-mode charge from I_0 and from background light is extinguished, but the differential correlation signal is kept. During this refresh, Φ and $\bar{\Phi}$ are set to ground switching off M5 and M6 (I_0 and the photocurrent are bypassed to VDD by a transistor not shown in Fig. 6.33) [34]. After the refresh, integration can go on. For readout, Φ

Fig. 6.34 Micro photograph of 64×48 pixel 3D sensor IC



and $\overline{\Phi}$ are also set to ground and the output voltages can be selected to the row line. The difference of the two output voltages represents one point of the correlation function. After this cycle, the phase of the modulation clock is stepped by 1/16 of the clock period. Figure 6.32 shows the chip photo of this 3D sensor. A 12-bit analog-to-digital converter (ADC) [35] for pixel readout with 1 MS/s was implemented. A SAR topology was chosen. At 5 V supply voltage, the ADC consumed 6 mW. Its active area was 0.3 mm^2 . At an object distance of 1 m, a standard deviation of 1 cm was reported with a light source consisting of four power LEDs at 850 nm with together 0.9 W. Background light of up to 150 klx could be suppressed without any optical filter. The measured distance changed by 5 cm for 100 klx background light [36].

The PIN photodiode described in [37] was implemented in a 64×48 pixel 3D sensor IC in $0.35 \mu\text{m}$ CMOS [38]. The low capacitance of the pin photodiode of $0.014 \text{ fF}/\mu\text{m}^2$ improved the signal-to-noise ratio (SNR). One correlator of the pixel circuit described in [39] was used in each pixel with a cut-off frequency of 18 MHz instead of 35 MHz and the maximum integration time was extended to 2 ms to optimize the SNR. The ambient-light suppression block introduced in [40] was exploited in this 3D sensor IC. The sensor IC is shown in Fig. 6.34. The area of this sensor IC is $4 \times 4 \text{ mm}^2$, whereby the pixel array occupies $2.8 \times 2.8 \text{ mm}^2$. Each pixel has an area of $60 \times 45 \mu\text{m}^2$ with a fill factor of 50%.

The standard deviation of the measured distance was below 3.7 mm in the optimum operating range [38]. The pixel could extract the phase of the modulated signal with an optical power of 1 nW successfully for an ambient light power in excess of 600 nW. With a power-LED based 850 nm light source of 12 W for the modulated signal, a background light of 180 klx did not show any influence on the measured distances.

A 512×424 pixel 3D sensor exploited the photonic mixer device consisting of polysilicon fingers and readout cathodes in modified $0.13\text{ }\mu\text{m}$ CMOS technology [41]. It was declared as being suitable for application in the Microsoft Kinect for XBOX ONE. The starting epitaxial wafer was optimized in thickness and doping concentration, however, no details were reported. Each pixel containing 10 N-channel MOSFETs and two MIM capacitors had a size of $10 \times 10\text{ }\mu\text{m}^2$ with a fill factor of 31% (without micro lens) and 60% with micro lens. A responsivity of 0.14 A/W at 860 nm and a modulation contrast of 67% at 50 MHz (56.5% at 130 MHz) were reported. The pixel circuit was fully differential and implemented the integration and background light compensation circuit visible in Fig. 6.33, however, without a circuitry for keeping the bias voltage of the readout electrodes constant. 256 10-bit ADCs with a conversion rate of 8 MS/s each and a frequency clock generator having 312.5 ps phase step resolution were integrated on the sensor IC. Thanks to two 4-lane MIPI D-PHY interfaces an input/output data rate of 8 Gb/s was obtained. The distance range was from 0.8 to 4.2 m with a depth uncertainty of 0.5% [41]. An optical narrow-band filter was integrated in a 5-plastic-element F1.0 optics achieving a field of view of $70^\circ \times 60^\circ$. The 3D-sensor chip's area was $8.2\text{ mm} \times 14.2\text{ mm}$. The frame rate was 60 fps at maximum and 30 fps typically [41].

6.4.6 3D Sensors with SPADs

Single-photon avalanche diodes are very interesting for range sensors because of the weak reflected signals and limited emitter power due to eye safety reasons. A 128×128 -pixel image sensor with time-to-digital converter (TDC) was introduced in [42]. A high-voltage $0.35\text{ }\mu\text{m}$ CMOS process was used for the fabrication of this sensor chip. The SPAD was described in [43]. Passive quenching and active recharge was implemented. The photon detection probability was 35% for 460 nm at an excess bias of 3.3 V . For the 3D sensor a wavelength of 635 nm with a peak power of 250 mW was used. 32 10-bit TDCs were integrated. A typical time resolution of 97 ps within a range of 100 ns was reported. The readout system was capable of handling 7.68 Gb/s . In a distance range from 20 to 375 cm the maximum mean error was 9 mm [42].

A 340×96 -pixel SPAD sensor in combination with a scanner achieved an image range up to 100 m [44]. This sensor was realized in high-voltage $0.18\text{ }\mu\text{m}$ CMOS. A P+/deep N-well SPAD was implemented. The pitch of the SPADs was $25\text{ }\mu\text{m}$ and an optical fill factor of 70% in macro pixels with 12 SPADs each was reported. This ToF Sensor was operated with 870 nm light and 40 mW illumination power. 32 macro pixels with a 12-bit TDC each with a resolution of 208 ps were implemented. With 80 klux background light, the repeatability error was below 10 cm over the full 100 m range. The nonlinearity error was 0.37%.

In [45] a 202×96 -pixel SPAD sensor also in high-voltage $0.18\text{ }\mu\text{m}$ CMOS using passive quenching and active recharge was introduced. The optical fill factor was reported also as 70%. An illumination repetition rate of 0.133 MHz was used. The illumination power was 21 mW at 870 nm and a frame rate of 10 fps was used. The

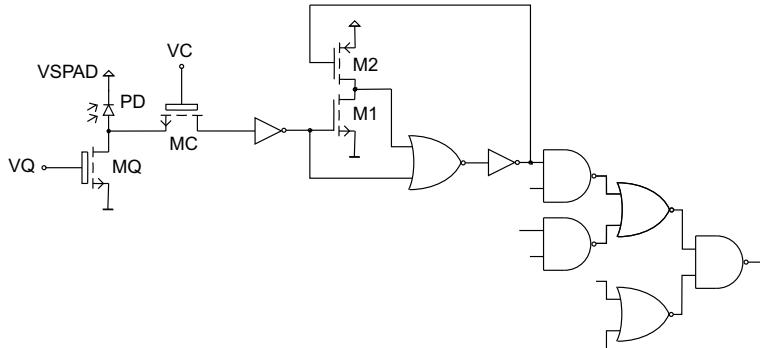


Fig. 6.35 Pixel circuit of a digital-SiPM-based TOF sensor

target reflectivity was 9%. With 70 klux background light, the repeatability error (1σ) was below 14.2 cm for the 100 m range. A relative precision of 0.14% was reported [45].

A very impressive 64×64 -pixel direct TOF sensor with SPADs in a so-called digital silicon photomultiplier (dSiPM) configuration was introduced in [46]. It was developed for operation together with a kW-range 532 nm laser. A $0.15 \mu\text{m}$ 6-metal layer CMOS process was used leading to a chip area of $4.4 \times 4.4 \text{ mm}^2$. A similar SPAD as described in [47, 48] was implemented. The breakdown voltage of the SPADs was 21.8 V and they were operated at 3.3 V excess bias voltage. Each pixel contained eight SPADs, of which each was connected to a monostable and a following OR-tree (see Fig. 6.35) to combine the pulses from different SPADs on a single line and to compress the SPAD pulse duration from 10 to 100 ns to below 1 ns.

The quenching transistor MQ (passive quenching) and the clamping transistor MC were thick-oxide transistors in order to allow the excess bias voltage of 3.3 V for the SPAD. The clamping transistor limited safely the pulse to 1.8 V at the input of the connected inverter. VC had to be at least one threshold voltage larger than the inverter's threshold to avoid operation of MC in the triode region. The monostable generated short pulses with a duration of two gate delays and an additional safety margin designed by tuning M2's aspect ratio. The implemented pulse width was 260 ps with a Monte-Carlo simulated standard deviation of 17 ps. The OR tree used a cascade of NAND-NOR gates to save area. Eight SPADs were combined in each pixel. In such a way a high pixel count rate could be handled.

Smart triggering, a 4-bit photon counter and a 16-bit time-to-digital converter were implemented in each pixel. The pixel pitch was $60 \mu\text{m}$ with a pixel fill factor of 26.5%. For readout, each pixel delivered a 20-bit word. For characterization a 70-ps 470 nm laser was applied and a total FWHM jitter of 780 ps was found including the contributions of SPAD, of the quenching circuit, of the OR tree and of the TDC.

In the imaging mode the large array was used to take a 64×64 3D image for distances up to 300 m (maximum time-of-flight 2 μs) with an accuracy better than 1.5 m ($\sigma < 0.2 \text{ m}$). In the altitude mode the array was applied for a single-point

measurement of a distance of up to 6 km with an accuracy better than 35 m [46]. A background photon flux of 100 Mph/s/pix was possible. The maximum frame rate in the imaging mode was 17.9 kfps. The power consumption was 47.7 mW for the digital part (1.8 and 3.3 V) and 45.8 mW for the SPADs (21.8 V) [46].

6.4.7 Smart Pixel Sensors

State-of-the-art CMOS technology allows to integrate photodetectors, analog, and digital electronic functionality on the same “smart image sensor” chip or even in so-called “smart pixels”. In such a way pixels with a very high functionality can be realized with properties which are difficult to achieve or which are not possible to achieve with conventional photosensors. Some examples out of the whole variety of smart pixel sensors like linear transforming smart pixels, optically addressable gate arrays, smart pixel sensors for real-time optical tomography for medical and technical applications as well as sensors for basic machine vision tasks with the ultimate goal of creating “seeing chips” will be addressed in the following.

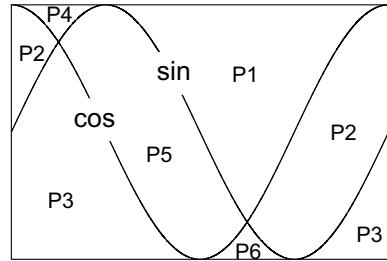
Let us consider linear transforming smart pixels first. The fact that the shape of photodiodes can be chosen almost arbitrarily allows an easily realizable way to a huge amount of photosignal processing capability. We want to assume an one-dimensional light intensity distribution $I(x)$ that falls onto a photodiode whose photosensitive width $w(x)$ is varying with the distance x . Because the responsivity of photodiodes can be linear over more than 10 orders of magnitude [49], the output signal s_{pd}

$$s_{pd} = \int_a^b I(x)w(x)dx \quad (6.8)$$

of the photodiode results. Therefore, parametrized linear transforms of incident light distributions can be determined without additional processing elements, when the photodiode shape is chosen properly. A triangular shape, for instance, allows to determine the centroid of an one-dimensional light distribution [50]. An amplitude-modulated sine shape comprises a Fourier-transform pixel which calculates the weighted sine and cosine part of a signal, with which the magnitude and phase of an incident light pattern could be obtained accurately [50]. This principle was implemented in several optical metrology and encoder products with an accuracy of below 0.1 μm for linear and rotational distance measurements [51].

An improved Segmented Fourier Phase Detector (SFPD) was presented in [51]. The construction principle of this SFPD is shown in Fig. 6.36. A sine and cosine function are superimposed within one period. In a CMOS chip 12 periods of 80 μm each were implemented. Six photosensitive segments, P1–P6, were present. The photocurrents of these segments can be converted to six proportional voltages by transimpedance amplifiers. By the proper addition of these voltages $U_{P1}–U_{P6}$, purely sinusoidally modulated signal voltages, $U_{PD1}–U_{PD4}$, are obtained [51]:

Fig. 6.36 Construction principle of SFPD [51]



$$\begin{aligned} U_{PD1} &\propto U_{P1} + U_{P4} + U_{P5}, & U_{PD2} &\propto U_{P2} + U_{P3} + U_{P6}, \\ U_{PD3} &\propto U_{P1} + U_{P4} + U_{P2}, & U_{PD4} &\propto U_{P5} + U_{P3} + U_{P6}. \end{aligned} \quad (6.9)$$

The desired quadrature signals U_{\sin} and U_{\cos} result as differences in both signal pairs:

$$U_{\sin} = U_{PD1} - U_{PD2}, \quad U_{\cos} = U_{PD3} - U_{PD4}. \quad (6.10)$$

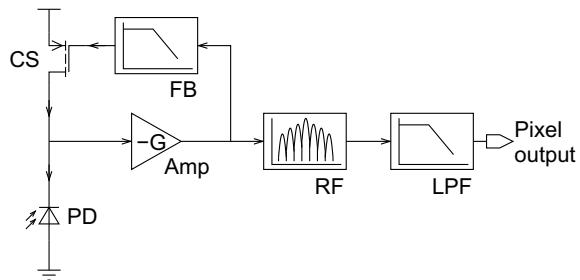
The phase angle Φ can be obtained from

$$\Phi = \arctan \frac{U_{\sin}}{U_{\cos}}. \quad (6.11)$$

The relative position x_ϕ within a grating period p is proportional to the phase angle Φ : $x_\phi = p\Phi/2\pi$. The detector design and signal processing can be simplified, since both small photodetectors P4 and P6 appear only in combination with the large photodetectors P1 and P3, respectively. Therefore, P4 and P1 as well as P6 and P3 can be connected to form the new photodetectors P1' and P3': P1' = P1 + P4 and P3' = P3 + P6. In such a way only four transimpedance amplifiers are necessary and the photocurrents of the small detectors P4 and P6 do not have to be amplified separately [51].

Another very interesting form of smart pixels are optically programmable gate arrays. Field programmable gate arrays (FPGAs) are today widely used to develop electronic systems cost and time efficiently. FPGAs contain a large number of digital configurable logic blocks (CLBs) with which many logical functions can be realized. Furthermore programmable signal routing components between CLBs and input-output blocks are implemented in FPGAs. The FPGA's configuration data is often stored in a program memory which is read in from an external storage device at power-up or when a new configuration has to be programmed. Since despite of clock periods in the nanosecond range the configuration times of FPGAs can be in the millisecond range, optically programmable gate arrays (OPGAs) [52] may further increase the computational speed of advanced microelectronic systems. The central element of an OPGA is a combination of a smart pixel and a CLB, resulting in a so-called optically configurable block (OCB). A few hundred photons are sufficient to

Fig. 6.37 Principle of pixel for optical low-coherence tomography [50]



change the logic function of an OCB. Therefore, smart pixels can contribute to a much closer connection between photonics and electronics especially since computation seems to be carried out electronically and data seem to be transferred optically and to be stored optically for a long period in the future.

Optical low-coherence tomography (OCT) [53] is a rather new and sophisticated technique for acquiring three-dimensional images with micrometer resolution of many biological and technical objects which are diffusely reflecting making it difficult to distinguish details in their bulk by conventional methods. In the beginning of OCT, the image acquisition had to be done by mechanical scanning with a single-channel (point) OCT detector, due to the complexity and necessary performance of the signal processing circuitry. Figure 6.37 shows the block diagram of such a circuitry. A smart pixel for OCT applications has to implement photodetector, offset cancellation (done with the block FB by changing the current in the PMOS current source CS, because the modulation signal is typically -60 dB or far below the DC signal), low-noise preamplifier, rectification, programmable low-pass filtering and random access readout.

All these functions were realized in one smart OCT pixel with 20 MOSFETs [54]. An OCT chip in $2\text{ }\mu\text{m}$ CMOS technology with a bipolar transistor option implementing 58×58 smart OCT pixels for simultaneous imaging of parallel OCT channels was demonstrated. The total die area of the OCT chip was $7.2 \times 7.2\text{ mm}^2$ with a pixel pitch of $110\text{ }\mu\text{m}$. The photodiodes had a size of $35 \times 35\text{ }\mu\text{m}^2$. A sensitivity of -58 dB, i.e. a minimum detectable optical power of 6.3 fW was observed compared to the shot-noise limit of 1.2 fW . The detection limit thus was 7.2 dB above the shot-noise limit probably due to electronic noise in the signal processing circuitry [54]. This OCT chip represents an interesting step towards a new type of inexpensive real-time imaging without ionizing radiation with many possible applications in medicine, biology, and technical surface topography [50].

Sensors for basic machine vision are a large field of current investigations. The increasing demand for fast and efficient low-power and low-cost vision systems is also being led by the needs of surveillance, automotive and mobile systems market. This market asks for the capabilities of segmentation, recognition as well as classification of characters, faces, and postures, for instance. The traditional way to fulfil these tasks is: (i) acquisition of the image on a low-cost CCD camera and (ii) software processing of the raw image information on a digital platform (personal computer,

digital signal processor (DSP), or application specific integrated circuit (ASIC)). Although the computational capabilities of digital platforms improve every year, they are far from low-cost and portability, as needed for the visual applications targeting the grand public [55]. A possible solution is to shift part of the computation into the sensor itself, where in each pixel analog preprocessing can be performed [56–61]. In this way the camera becomes a more sophisticated device, i.e. a so-called retina. In many cases the pictures taken are preprocessed electronically, involving algorithms that perform preprocessing in parallel for or at all pixels. Each pixel has to be equipped with its own analog or digital pre-processor which processes its own photosignal and these of its neighbors independently of each other at the same time. Here only one recent example for such a massively parallel approach can be included [55]. In this example, each pixel exploits the local image surroundings to calculate local gradients. Similar to biological vision systems which can focus attention on the most conspicuous portion of a scene, the smart pixels described in [55] implement a most interesting concept to read out the gradient signals: the gradient information is temporally ordered from the largest to the smallest gradient's magnitude, resulting in address-event coded output.

The main idea for computation of the spatial gradients is based on the definition of the derivative of a 2-dimensional function performed in the vector direction \mathbf{r}

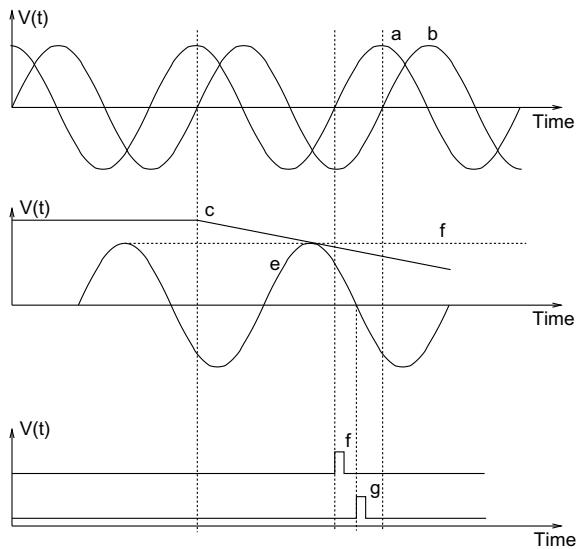
$$\frac{\partial I(x, y)}{\partial \mathbf{r}} = \frac{\partial I(x, y)}{\partial x} \cos\alpha + \frac{\partial I(x, y)}{\partial y} \sin\alpha \quad (6.12)$$

where α is the vector's angle. This angle can be swept in time using steering functions and the computation of the gradient on a discrete lattice square at the pixel level can be performed by

$$\frac{\partial I_{i,j}}{\partial \mathbf{r}(t)} = \frac{I_{i+1,j} - I_{i-1,j}}{2} \cos\omega t + \frac{I_{i,j+1} - I_{i,j-1}}{2} \sin\omega t \quad (6.13)$$

where $I_{i,j}$ represents the local luminance at pixel (i, j) as detected by the photodiode and ω is the angular frequency of the steering functions. In such a way, the local derivative in the direction of vector \mathbf{r} , i.e. the angle ωt , is continuously determined as a linear combination of two basis functions (the derivatives in x and y directions). This is the principle of steerable filters [62]. A function is called steerable under a transformation (translation, rotation, scaling, etc.) when all transformed versions of this function can be expressed using linear combinations of a fixed, finite set of basis functions. Here the sine and cosine functions are interpolating functions. The first nearest neighbor pixels in x and y directions are involved here in the computation of the gradient. Due to the interpolating functions, sub-pixel precision is possible, i.e. derivatives in directions between discrete pixel locations can be calculated. The spatial gradient is by definition the vector $\mathbf{r}(t)$ for which (6.13) reaches its maximum. If the image, i.e. its luminance fluctuates substantially slower in time than $1/\omega$, (6.13) represents a sine wave in time, which is called *local steering function* in the following,

Fig. 6.38 Signal activity during frame acquisition. After completion of the first period of the interpolation functions a and b , the dynamic threshold c starts decreasing. When the threshold equals the stored maximum d of the local steering function, a gradient's magnitude pulse f is generated. A zero-crossing pulse g is emitted during the first descending flank of e following the magnitude pulse f [55]

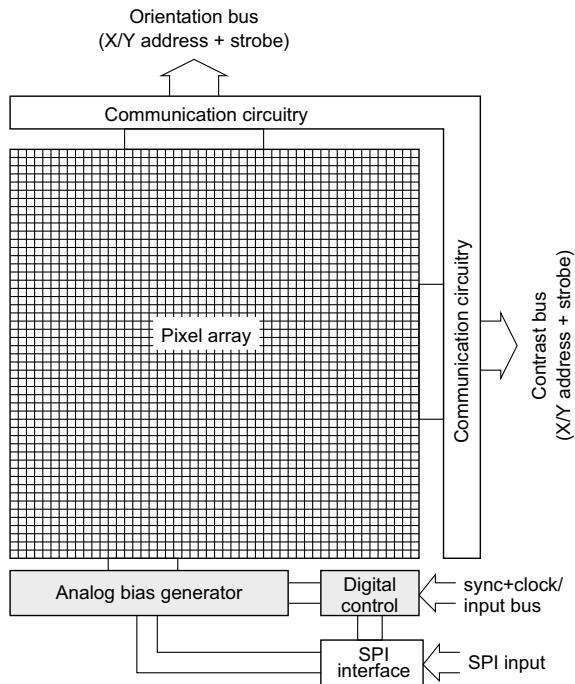


for which amplitude and phase are related to the magnitude and direction of the gradient, respectively.

As a consequence, the coding of information is straight forward. After the first revolution of the interpolating functions, each local steering function went through a maximum, which can be captured by a simple peak-detection mechanism and stored locally on small (parasitic) capacitors. Then, at the next period of the interpolating functions, a monotonic decreasing threshold function (at best with a constant slope) is triggered (see Fig. 6.38). When the decreasing threshold equals the stored maximum value, address-event pulses, encoding the location of the corresponding pixel, are generated and transmitted on an asynchronous bus [63]. In this scheme, the time of appearance of an event on the bus is directly related to the gradient's magnitude, and the sending of gradient information off-chip is ordered from high to low values. The gradient's direction similarly contained in the phase of the local steering functions, is also pulse-encoded in time by detecting the zero-crossing.

Because all communications are completely asynchronous, i.e. each pixel can access the bus independently from the others, collisions have to be avoided. Therefore, each pixel is allowed to access the bus only once during a frame acquisition resulting in a slightly complicated logical structure of the pixel. Another powerful measure to avoid collisions is to dynamically control the decreasing threshold function. The threshold can be decremented faster in the first part of the acquisition, when information is typically sparse, and slower in the latter part of the acquisition. Still another collision avoidance mechanism is used: a pixel momentarily raises the global threshold when emitting a pulse to prevent other pixels with similar maximum values from firing.

Fig. 6.39 Architecture of gradient extraction chip [55]



The chip architecture is characterized by five main blocks (Fig. 6.39): a serial peripheral interface (SPI) block, a digital control block, an analog bias block, communication circuitry (one for each bus), and the pixel array with photodiodes and analog computation circuitry in each pixel. Let us now have a look on these blocks in more detail.

Two low-level computations, global normalization and low-pass spatial filtering, are performed on the image before extraction of the spatial gradients. The normalization is done by regulating the total current. It is needed to guarantee proper operation under different illumination. Low-pass filtering was necessary to reduce high-frequency noise introduced by the derivative operation and for obtaining subpixel accuracy [55]. For proper gradient extraction and minimization of events generated onto the two buses for magnitude and direction information, a state machine was implemented in the pulse generator block of each pixel. This state machine starts acquisition of a frame after receiving a sync signal provided by the user. Prior to an acquisition, the old stored maximum values are cleared. The local steering function then starts to be calculated. During its first period, the maximum values are detected and stored locally. The decreasing threshold is launched and the pixels wait for it to match their locally stored maximum value. A communication pulse is generated on the “magnitude” bus when matching eventually occurs. Then, the pixel switches to the second state where it waits for the zero crossing on the descending flank of the local steering function. When this happens, a second pulse is emitted; this time onto

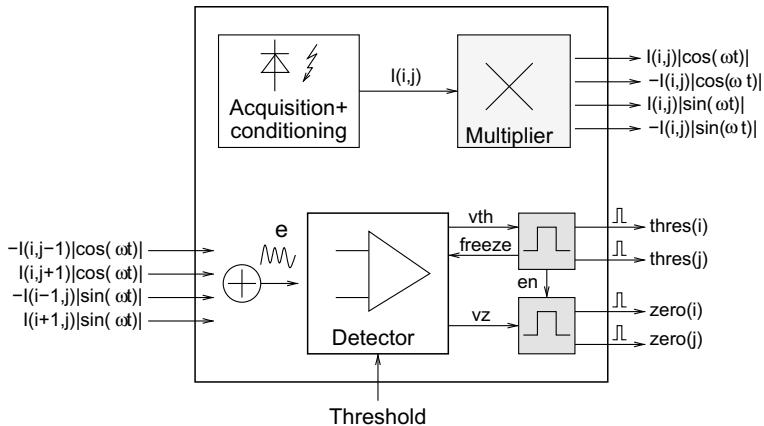


Fig. 6.40 Pixel block diagram of gradient extraction chip [55]

the “direction” bus. Now, the pixel enters the third state where it is in stand-by and cannot generate any pulses until a new sync signal is received and the whole scheme starts again.

The serial peripheral interface (SPI in Fig. 6.39) serves for programming of the chip. With its help, the normalization current, the width of the spatial low-pass filter, the analog biases, the gain of the photo-receptors, and the frame rate can be changed. The digital control block generates the threshold function as a monotonic decreasing ramp as well as the sine and cosine interpolating functions. Discrete values are computed at fixed time intervals and then converted into analog reference currents by the analog bias block. This block supplies fixed global bias voltages or currents, which are needed by the pixels as references. The communication circuitry consists of two 14-bit buses. Each bus contains 7 bits for the pixel x - and y -address each. When a pulse is generated in a pixel, the communication circuitry encodes its (x, y) address in a digital word. To indicate whether the code is valid or not, a strobe signal is also provided.

In the following, the circuits will be described in more detail. Figure 6.40 shows the overall pixel structure. The photodiode measures the local luminance. The pixel is connected to its closest neighbors to perform low-pass filtering and to compute the local spatial gradient. A multiplier (see below) performs the multiplication of basis function and interpolating functions in current mode. The result of current summation from the nearest neighbors at the summation node represents the local steering function (e in Figs. 6.38 and 6.40). A detection block samples its maximum value, compares it with the dynamic threshold, and determines its zero crossing. The two remaining blocks in the pixel structure (Fig. 6.40) encode the gradient’s information onto the buses and guarantee the correct sequencing of the state machine. The multiplier and detection block covered about 60% of the pixel area [55]. The pulse generators took about 20% and the photodiode about 15% of the total pixel

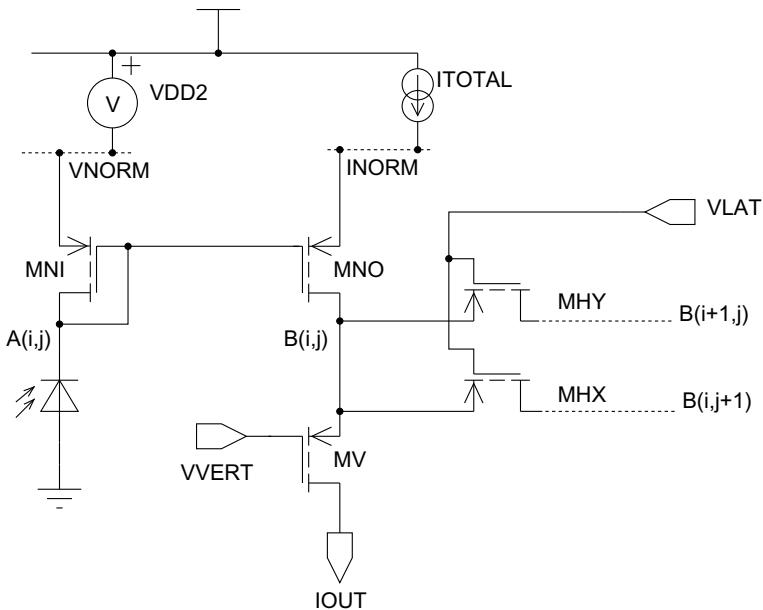


Fig. 6.41 Circuit for light-to-current conversion and signal conditioning [55]

area. The connections and the signal conditioning circuitry occupied the rest of the pixel area.

Figure 6.41 shows the current mode circuit for light-to-current conversion and signal conditioning. An N-well/P-substrate photodiode was used. For normal illumination conditions, the photocurrent ranged between a few pA for dark current and about 10 nA for full light incidence. The current normalization is done by a weighted current mirror. The weights self-adjust in order to keep the total output current fixed to a certain programmable value. Another advantage of the current mode is that the photocurrents are directly available without integration. The low-pass filtering is done in a diffusion network formed by pseudo-conductances laterally connecting the south ($B(i + 1, j)$) and east ($B(i, j + 1)$) nearest neighbor pixels. This network of pseudo-conductances is achieved by MOS transistors operating in weak inversion [64]. The lateral and vertical pseudo-conductances in the diffusion network can be controlled by VLAT and VVERT.

The multiplier depicted in Fig. 6.42 calculates the local steering functions. One-quadrant multipliers were chosen to simplify the pixel circuit. This was possible because the sine and cosine interpolating functions change sign at well defined instants. Therefore, it was possible to generate a positive and a negative replica of the desired product with an error of less than 1% [55]. These replicas were switched at appropriate times to distribute the right signal to the proper neighbor. In such a way the silicon area could be kept smaller than for a four-quadrant multiplier.

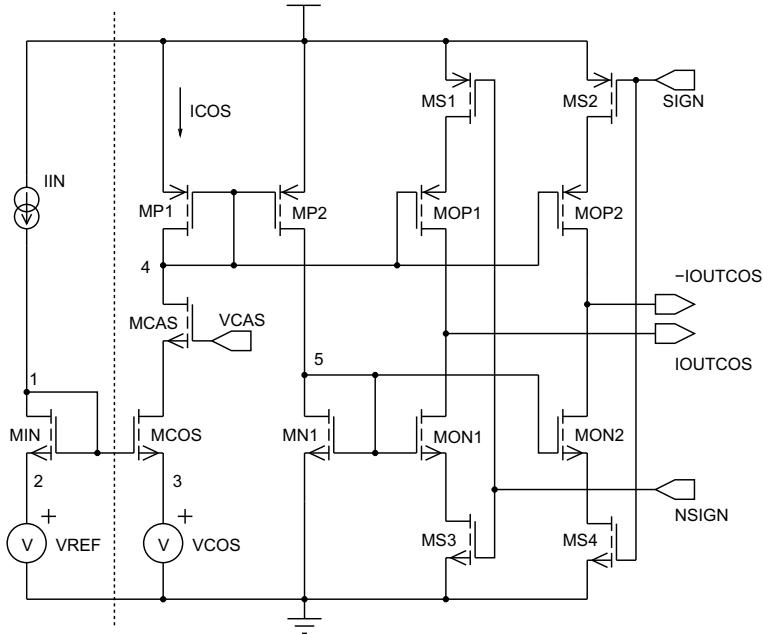


Fig. 6.42 Circuit of the multiplier for the cosine product. The right part is replicated to obtain the sine product, while the left part is common to the two half circuits [55]

The core of the multiplier consists of matched transistors MIN and MCOS biased in weak inversion. The output current, therefore, is given by

$$I_{\text{COS}} = I_{\text{IN}} \exp \frac{V_{\text{REF}} - V_{\text{COS}}(t)}{U_T} \quad (6.14)$$

where I_{IN} is the low-pass filtered normalized photodiode output current IOUT of Fig. 6.41. The voltages V_{REF} and V_{COS} have to be set so that

$$\exp \frac{V_{\text{REF}} - V_{\text{COS}}(t)}{U_T} = |\cos \omega t| \quad (6.15)$$

in order to obtain the desired product. Since the output is a current, the most accurate way to generate voltages is with reference currents. Two reference transistors in the bias block being identical to MIN and MCOS supply voltages V_{REF} and $V_{\text{COS}}(t)$ on the basis of currents so that

$$I_{\text{COS}}(t) = I_{\text{COS}}^*(t) \frac{I_{\text{IN}}}{I_{\text{REF}}} \quad (6.16)$$

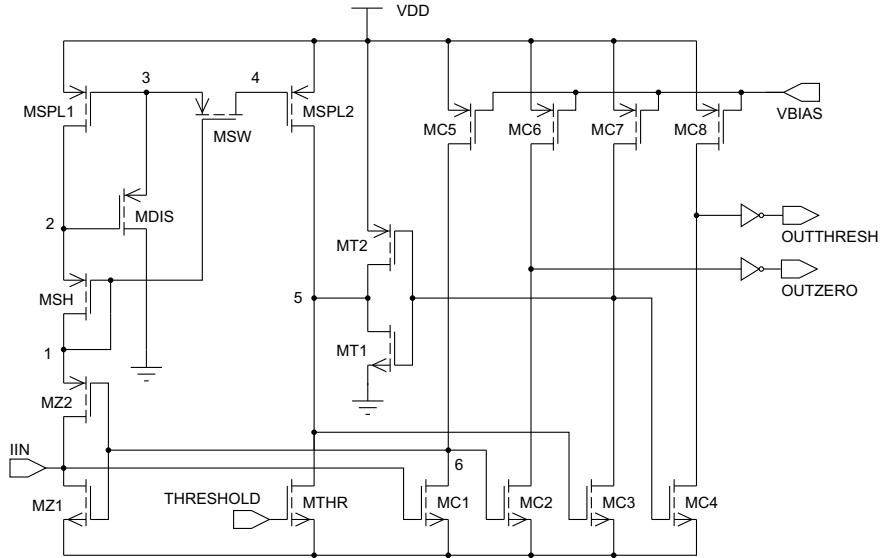


Fig. 6.43 Circuit of the detection block [55]

where $I_{\text{COS}}^*(t)$ is a rectified sinusoidal reference current delivered from the bias block. In such a way the multiplications do not depend on physical process parameters. MIN in MCOS have to match to each other of course. The parameter I_{REF} allows multiplier amplification.

Four-quadrant multiplication is achieved in the following way: transistors MP1, MP2, and MN1 replica the cosine current, while transistors MOP1, MOP2, MON1, and MON2 form the current mirrors output, which are connected to the neighbor pixels. Transistor switches MS1/MS3 and MS2/MS4 select the right branch according to the input levels SIGN and NSIGN. For a high SIGN (NSIGN is then low), a positive current flows from IOUTCOS and a negative one from $-IOUTCOS$. The sign of these currents changes for a low SIGN (NSIGN = high). The silicon area of the multiplier block was $1920 \mu\text{m}^2$ [55].

The detection block extracts the magnitude and direction of the local gradients. This unit detects the zero crossing of the local steering function, samples and stores its maximum value, and determines the time when the threshold function matches the stored maximum value. The circuit diagram of the detection module is shown in Fig. 6.43. At first, the detection block determines the sign of the local steering function denoted IIN in Fig. 6.43. This task is performed by the comparator consisting of transistors MZ1, MZ2, MC1, MC2, MC6, and MC7. The output signal OUTZERO of this comparator is fully digital. When input current flows into the circuit (through MZ1 to ground), OUTZERO is low. When IIN flows out from the input (sourced by MZ2 from VDD), OUTZERO is high. The logical level of OUTZERO, therefore, indicates the sign of IIN.

For a negative input current I_{IN} , it is drawn from the maximum detection circuit formed by transistors MSH, MSPL1, MSPL2, MDIS, and MSW. The maximum detection works only when I_{IN} is negative, i.e. when MZ2 is conducting. In this case, transistor MSW is also conducting and MDIS acts on the gate of MSPL1 to make its drain current equal to the input current. The transistor MDIS, however, is only active as long as the magnitude of I_{IN} increases. MDIS is cut off when the magnitude of the input current starts to decrease. When this occurs, the potentials at nodes 1 and 2 (see Fig. 6.43) rise and turn off MSW. Therefore, the output transistor MSPL2 is isolated and it now holds the maximum current reached by the input. The parasitic capacitance of node 4 including the gate-source capacitance of MSPL2 is exploited to hold the maximum value. The isolation device MSW is necessary to avoid coupling to the hold node 4 via the gate-drain capacitance of MSPL1. This capacitance desaturates quickly when the input current starts to decrease. Without the isolation transistor MSW, the fast variation of the drain-gate voltage of MSPL1 would induce a charge on node 4, which in turn would change the stored maximum value too quickly. The isolation transistor MSW reduces this effect but cannot eliminate it completely [55]. The relative error is larger for low currents. Therefore, the current from the photodiode is amplified in the multiplier block to obtain a local steering current largely unaffected by this coupling.

When the maximum value is available on transistor MSPL2, the comparison with the dynamic threshold can start. The current difference $I_D(\text{MSPL2}) - I_D(\text{MTHR})$ is compared to zero by the comparator formed by the transistors MT1, MT2, MC3, MC4, MC7, and MC8. This comparator is identical to the one described above. The digital value of the output voltage OUTTHRESH indicates whether the stored maximum is larger or lower than the threshold. The transition of this digital value constitutes an event. Reset transistors are required to clear the stored maximum values before a new frame acquisition starts. The reset transistors are not included in Fig. 6.43 [55]. The output signals OUTTHRESH and OUTZERO were buffered with an inverter each before they are connected to the next stage. Behind these inverters, threshold crossings are represented by high-to-low transitions and zero crossings are represented by low-to-high transitions [55].

The next stage is the pulse generator block. The two circuits shown in Figs. 6.44 and 6.45 were derived to generate and communicate the threshold-crossing and zero-crossing events, for which a current pulse has to be generated only once for each pixel during one frame acquisition. For this purpose, the pixel communication circuitry has to keep track of the latest history of the pixel in two one-bit registers included in each pulse generator (MEMTH in Fig. 6.44 and MEMZ in Fig. 6.45). These registers also exploit parasitic stray capacitances to save chip area.

A sync signal starts each frame acquisition and brings all pixels into state 1. A reset is applied to the zero-crossing pulse generator making its inputs RESET and NRESET (Fig. 6.45) high and low, respectively. To realize that any zero crossing in state 1 has to be disregarded before a threshold crossing has been communicated, the memory nodes MEMTH and MEMZ of the pulse generators are set to VSS each time when a sync signal is applied. In this state threshold pulses are possible because MSX and MSY (Fig. 6.44) are on and zero-crossing pulses are disabled, because switch

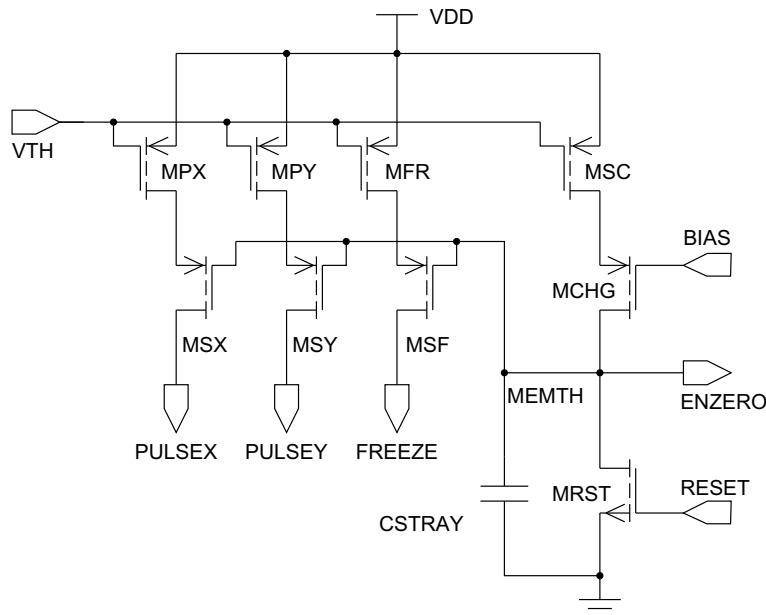


Fig. 6.44 Circuit of the threshold pulse generator [55]

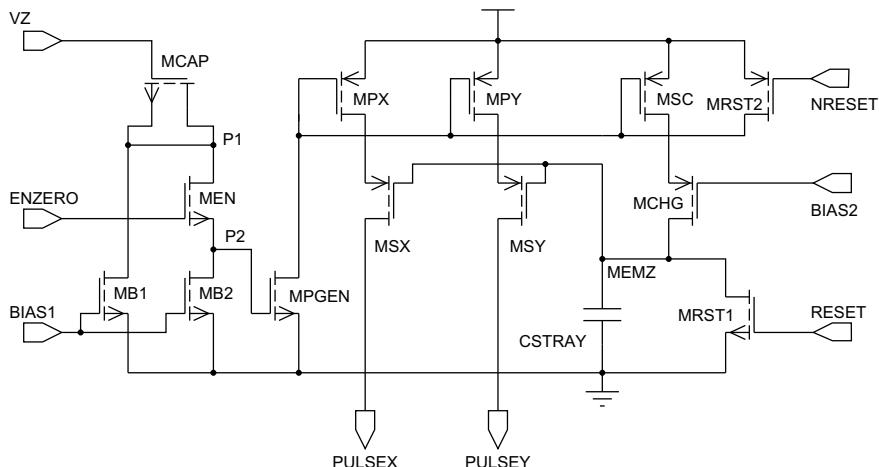


Fig. 6.45 Circuit of the zero-crossing pulse generator [55]

MEN in Fig. 6.45 is off. For a threshold matching, a high-to-low transition happens on input signal VTH and transistors MPX, MPY, and MFR are made conducting. At the same time transistor MSC is turned on and the charge current of MCHG increases the potential of the memory node, bringing MEMTH into the high logical state. This

new state causes that switches MSX and MSY are turned off. In such a way two current pulses out of the nodes PULSEX and PULSEY result. The length of these pulses is set by a bias current via a programmable BIAS signal.

The zero-crossing generator is enabled when transistor MEN is switched on by a logical high value at MEMTH. $\text{MEMTH} = 1$ and $\text{MEMZ} = 0$ correspond to state 2 of the state machine, in which the threshold generator is disabled. When a zero crossing is detected on the descending flank the local steering current produces a low-to-high transition of signal VZ and node P2 is brought high through the coupling capacitor MCAP and switch transistor MEN. This potential change at node P2 causes MPGGEN to turn on transistors MPX and MPY resulting in X and Y current pulses from PULSEX and PULSEY of Fig. 6.45. Transistor MSC is also on and delivers charging current through MCHG to the memory node MEMZ, which is therefore pulled high. With a time delay determined by BIAS2, the transistors MSX and MSY and the pulses are turned off. Now $\text{MEMTH} = 1$ and $\text{MEMZ} = 1$ hold, the state machine is in state 3, and both generators are disabled.

The transistors MB1 and MB2 in Fig. 6.45 are necessary to bring down nodes P1 and P2 after a zero-crossing event, when the pulse generators are in the initial state, i.e. before a threshold event. When the input signal goes high in this state (corresponding to detection of a zero crossing), node P1 is also drawn high, but no pulse is generated due to node P2 being isolated from node P1 by MEN, which is off. The potential on P1 would remain high without MB1 and as soon as MEN would be switched on by the threshold pulse generator. P2 would follow P1 to the high state and a pulse would be generated belonging to a threshold detection instead to a zero-crossing detection.

The column (x-axis) and row (y-axis) address is encoded by two pulses from PULSEX and PULSEY. A third FREEZE pulse (see Fig. 6.44) is needed to avoid collisions. A freeze pulse being present momentarily increases the threshold current by slightly charging the stray capacitance of node THRESHOLD in the detection block (see Fig. 6.43). In such a way, other pixels with maximum values close to the threshold are prevented from emitting pulses during the time needed by the currently emitting pixel to send its information onto the bus.

The communication circuitry generates the address code for firing pixels. It also produces a STROBE signal, which can be used off-chip to latch the actual value of the x- and y-axes addresses. These addresses determine the location of the active pixel. The time of address appearance on the bus characterizes either the magnitude or direction of the spatial gradient depending on which pulse generator has been active [55].

The chip with an array size of 100×100 was implemented in a $0.5 \mu\text{m}$ analog CMOS technology with a total silicon area of 86 mm^2 [55]. The size of each pixel was $80 \times 80 \mu\text{m}^2$ with a fill factor of 15%. The total number of transistors in the chip was 850,000, whereby the number of transistors per pixel was 84. The static power consumption was 50 mW. A frame rate of 1000 Hz was possible and the sensitivity of the retina spanned from 0.3 to 10 W/m^2 . The key to such fast processing is the application of the theory of steerable filters in an analog VLSI implementation to compute the magnitude and direction of the gradients. An irradiance of 2 mW/m^2 was

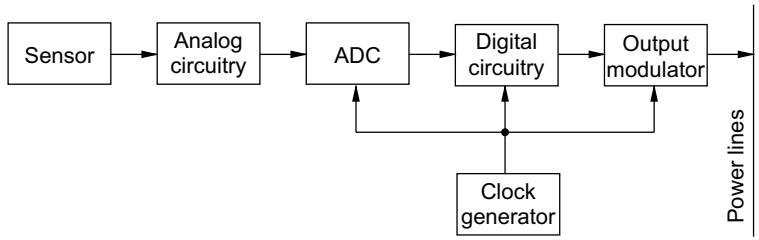


Fig. 6.46 Smart sensor system for medical applications [65]

necessary to enable reliable edge detection. The standard deviation of the frequency distribution of the errors on the direction of the gradients was 7.7° [55].

Let us summarize. The very sophisticated signal processing circuitry in each pixel truly justifies to classify the silicon retina chip described in [55] as a smart pixel chip. While this “silicon retina” delivers only preprocessed data, the interpretation of the actual image content still has to be done off chip. The required interpretation logic, however, presumably can be integrated one day on the same chip which will then be a single-chip machine vision system, a so-called “seeing chip”.

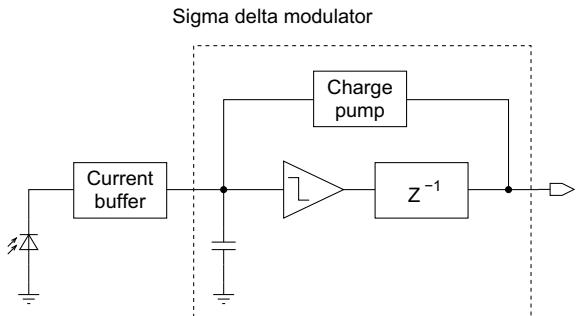
6.4.8 CMOS Optical Sensors

Here a low-level light sensor and preprocessor OEIC for a disposable medical probe for chemoluminant diagnostic applications shall be introduced. A 10-Hz $5\text{--}10\mu\text{W}/\text{cm}^2$ (corresponding to a maximum photocurrent of $4\mu\text{A}/\text{cm}^2$) input optical signal in the visible spectrum has to be analyzed by this OEIC, which contains the sensor, analog circuits, an analog-to-digital converter (ADC), digital circuits and an output modulator (see Fig. 6.46).

One of the advantages for integrating the optical sensor in a disposable probe is the elimination of cleaning the probe between measurements. The disposable light sensor must be cheap and the number of I/O pins must be small to allow reliable contacting of the detachable parts. Usually a serial bus interface is used leading to a number of three pins for the two power lines and the data pin. The number of pins, however, can be reduced down to only two, since the output data can be modulated on the power lines as shown in Fig. 6.46.

Usually current-to-frequency conversion [66, 67] thanks to its simplicity and high precision is a good candidate for analog-to-digital conversion, when no fast measurements are required. Operation of those current-to-frequency converters is based on counting the number of pulses produced by a current-controlled oscillator (CCO) over a constant period of time to obtain a digital presentation of the incident light intensity. A simple first-order sigma-delta modulator for analog-to-digital conversion was successfully used in an area image sensor [68]. The signal-to-noise ratio (SNR) of a sigma-delta modulator theoretically improves by 9dB for each doubling of the

Fig. 6.47 Architecture of sensor for medical applications [65]



oversampling ratio. Doubling the measurement time in the CCO scheme, which corresponds to doubling the oversampling ratio, in contrast, improves the SNR only by 3 dB [65]. A first-order sigma-delta ADC, therefore, can achieve potentially a higher SNR than a CCO, whereby the first-order sigma-delta ADC is only slightly more complicated. A single-bit first-order sigma-delta modulator ADC was chosen due to its inherent linearity, robustness against process deviations, and simplicity. The sensor architecture is shown in Fig. 6.47.

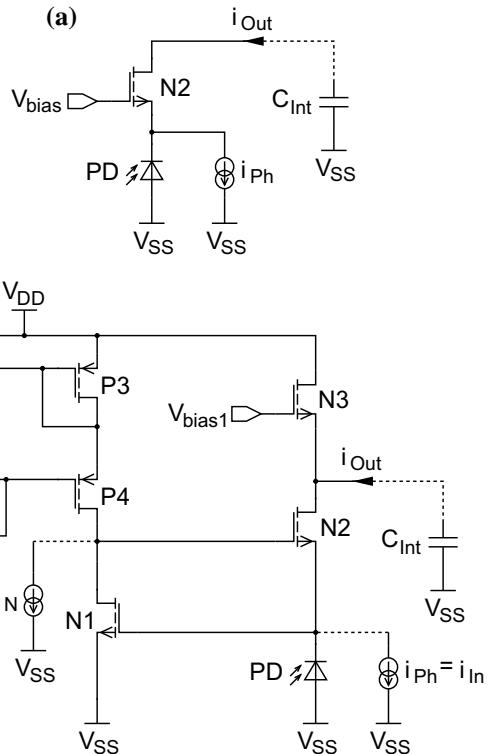
The sensor reported in [65] consists of an integrated photodiode with an area of $500 \times 500 \mu\text{m}^2$, a current buffer, and the sigma-delta modulator. The photocurrent from the photodiode is buffered by the current buffer into an integrating capacitor. The photocurrent is integrated on an external integrating capacitor rather than on the diode junction capacitance itself to improve the photocurrent-to-voltage conversion efficiency [65]. This is advantageous because the integrating capacitor is much smaller than the diode junction capacitance achieving a larger output voltage for the same charge. The integrator voltage is compared to the threshold level by sampling the comparator. As soon as the integrator voltage drops below the threshold, a constant amount of charge is pumped into the integrator. In such a way a first-order sigma-delta modulation loop is formed. The output is a one-bit digital signal, modulated by the input photocurrent.

Let us examine the circuit of the current buffer before the first-order sigma-delta modulator. Due to the small area of the integrated photodiodes compared to a cm^2 , the current buffer has to provide a sufficient bandwidth for input currents as low as tens of picoamps. For such a purpose, the usual common gate circuit shown in Fig. 6.48a does not perform satisfactory. The input pole of this circuit is determined by the transistor transconductance and the photodiode junction capacitance [65]:

$$\frac{i_{\text{out}}}{i_{\text{ph}}} \|_{C.G.} = \frac{g_{m,N2}}{sC_D + g_{m,N2}} \quad (6.17)$$

The maximum photocurrent for the photodiode area of 0.25 mm^2 is $4 \mu\text{A}/\text{cm}^2 \times 0.25 \text{ mm}^2 = 10 \text{nA}$. At this very low current, transistor N2 is in subthreshold with

Fig. 6.48 Common gate (a) and boosted current buffers (b) [65]



$$g_{m,N2} = \frac{q I_{ph}}{k_B T} \quad (6.18)$$

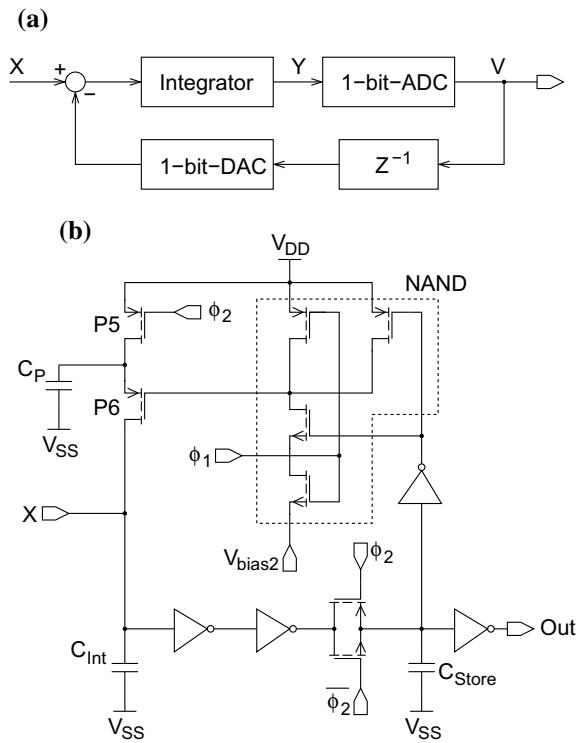
For a photocurrent of 10 pA , the bandwidth can be calculated to be only about 0.6 Hz , which is much too low for the diagnostic application. The transconductance does not depend on the transistor dimensions in subthreshold operation, thus this property cannot be improved by transistor sizing. Another circuit has to be chosen. The circuit illustrated in Fig. 6.48b possesses a better performance.

The boosted configuration [69] with feedback effectively decreases the input impedance by the loop transfer and increases the output impedance by the same factor. There is a feedback loop via $c_{gs,N2} + c_{gd,N1}$. The loop transfer function is [65]:

$$LT(s) = \frac{c_f^2}{C_D(c_f + c_{gs,N2})} \times \frac{(s + \frac{g_{m,N2}}{c_f})(s - \frac{g_{m,N1}}{c_f})}{(s + \frac{g_{m,N2}}{C_D})(s + \frac{g_{ds,N1}}{c_f + c_{gs,N2}})} \quad (6.19)$$

where $c_f = c_{gs,N2} + c_{gd,N1} \approx c_{gs,N2}$. For $z_1 < p_2$, i.e. the frequency of the first zero is smaller than that of the second pole, the possibility of complex poles is elimi-

Fig. 6.49 Single-bit first-order sigma-delta modulator (a) and its implementation (b) [65]



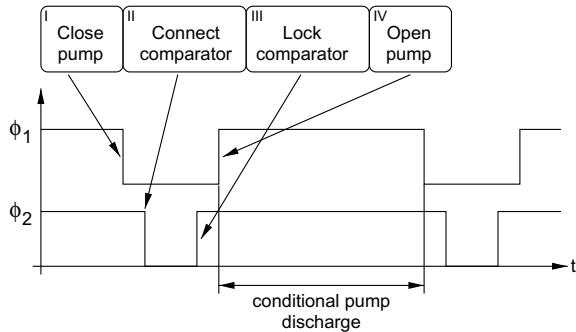
nated. Increasing the bias current enlarges g_{ds1} , and z_1 becomes smaller than p_1 for sufficiently large bias currents around $1 \mu\text{A}$ [65].

The block diagram of the first-order single-bit sigma-delta modulator and its implementation are shown in Fig. 6.49a and b, respectively. The comparator is an one-bit quantizer formed by two inverters in series. The comparator threshold does not affect the modulator performance [70], thus the circuit is not sensitive to transistor threshold voltage variations. The transmission gate is the sampling delay element. The comparator activates the charge pump (P5, P6, and C_p), which is a single-bit digital-to-analog converter, via the NAND gate. The operation is synchronized by two-phase 1-kHz clocks Φ_1 and Φ_2 (see Fig. 6.50).

At a low transition of Φ_1 (event I), P6 is cut off. At a low transition of Φ_2 (event II), the comparator transmission gate opens and the result propagates to the NAND gate. P5 turns on simultaneously and charges C_p to the supply voltage. At event III (high transition of Φ_2), the result is latched on C_{Store} and P5 is turned off. Subsequently, on event IV (high transition of Φ_1), if $V_{C_{\text{Int}}} < V_{\text{Th}}$, the $V_{\text{bias}2}$ voltage is set on the P6 gate, pumping a constant amount of charge Q_p into C_{Int} , and the cycle repeats.

The amount of charge pumped into the integrator is $Q_p = C_p(V_{\text{DD}} - V_{\text{bias}2} - V_{\text{Th}})$. The exact amount of Q_p is, of course, subject to V_{Th} variations, but there is no need to control it precisely. The gain and offset of the modulator response are affected by

Fig. 6.50 Clock diagram [65]



charge level variations, but the response stays linear [70]. As a result, the circuit can be calibrated for fixed gain and offset variations by a single calibration measurement [65].

The maximum pulse rate is the 1-kHz sampling rate of the modulator. The input current, i.e. the photocurrent, can be obtained from the modulator pulse rate as follows. The integration capacitor C_{Int} receives the same amount of charge at each modulator pulse, resulting in $\Delta V = 0.5 \text{ V}$ on the capacitor. The input current charging, assuming that the modulator does not saturate, is

$$I_{\text{in}} = \frac{N_{\text{pulses}}}{T_{\text{measurement}}} \times \Delta V \times C_{\text{Int}} \quad (6.20)$$

where $N_{\text{pulses}}/T_{\text{measurement}}$ is the output pulse rate. The output pulse rate is proportional to I_{in} .

The OEIC chip for diagnostic applications was realized in a $0.5 \mu\text{m}$ 1P3M CMOS technology. The circuit consisted of 31 transistors and occupied an area of $160 \times 110 \mu\text{m}^2$. The power supply was a single 3.3 V source. The signal bandwidth of 10 Hz was verified [65]. The leakage current of the photodiode of 80 pA/cm^2 limited the dynamic range (ratio between the maximum photocurrent and the leakage current) to 10^4 or 80 dB . In order to avoid rather rare metastability problems, the authors suggested to introduce a positive feedback (flip-flop) into the modulator loop instead of the transmission gate [65].

Let us have a look onto the SNR of this medical sensor OEIC finally. The noise is determined by three major contributors: photodiode shot noise, current buffer noise, and the reset noise of the charge pump. Transistor N1 is the dominant noise source in the current buffer. The current buffer noise can be represented as an equivalent current noise source i_n at the drain of N1 (see Fig. 6.48). The noise transfer function was computed as [65]:

$$A_{\text{noise}}(s) = -\frac{(sc_{\text{gd},N2} - g_{\text{m},N2}) \cdot (sC_D - g_{\text{ds},N2})}{(s - p_1) \cdot (s - p_2)} \quad (6.21)$$

This equation possesses a low-frequency zero $g_{ds,N2}/C_D$ in the noise transfer, which effectively suppresses the 1/f-noise of the feedback amplifier that would have dominated otherwise.

Simulations showed that the dominant noise source is the photodiode shot noise for frequencies below 100 Hz [65]. The output current of the current buffer is integrated on C_{Int} for one sampling period. C_{Int} accumulates some noise charge in addition to the signal charge. The charge pump reset noise ($k_B T C$ noise) is added to the integrator charge noise and the total charge noise power is [65]:

$$\overline{q_n^2} = \int_0^\infty S_{i,\text{in}}(f) \left(\frac{\sin(\pi f T_s)}{\pi f} \right)^2 df + k_B T C_P \quad (6.22)$$

where $S_{i,\text{in}}(f)$ is the noise spectral density of the current buffer output signal and T_s is the sampling time. In the digital frequency domain, the entire noise power spectrum is folded into the range from 0 to π , whereas the signal occupies only a fraction of this range due to oversampling. For a 10-Hz input bandwidth and a sampling frequency of 1 kHz, the signal occupies the range from 0 to $\pi/50$. The out-of-band components are cut off by the decimation low-pass filter. The true noise power after decimation, therefore, is 50 times lower than after (6.22). Referring the output noise to the input gave $i_{n,\text{in,rms}} = 0.82 \text{ pA}$, while the rms photodiode shot noise alone was about 0.81 pA [65].

A first-order sigma-delta modulator implies quantization noise [70]:

$$\overline{n^2} = \frac{\pi^2 \Delta^2}{36} R_{\text{ov}}^{-3} \quad (6.23)$$

where Δ is the distance between the quantization levels. In [65] Δ is the maximum effective current pumped by the charge pump: $\Delta = Q_p/T_s$. R_{ov} is the oversampling ratio defined as the ratio of the sampling frequency f_s and the input signal Nyquist frequency $2f_0$:

$$R_{\text{ov}} = \frac{f_s}{2f_0}. \quad (6.24)$$

From (6.23) a 9-dB noise decrease follows for each doubling of the sampling frequency. With the power of a sine wave with amplitude $\Delta/2$ as a reference level, the signal-to-noise ratio (SNR) is [65]:

$$SNR = \frac{\left(\frac{\Delta}{2}\right)^2}{2} \frac{36}{\pi^2 \Delta^2} R_{\text{ov}}^3 = \frac{9}{2\pi^2} R_{\text{ov}}^3. \quad (6.25)$$

According to this equation the SNR is about 51 dB for an oversampling ratio R_{ov} of 64 and about 60 dB for $R_{\text{ov}} = 128$ [65]. It is necessary to reduce the quantization noise to the noise floor of photodiode shot noise and current buffer noise. This can be achieved for a high enough sampling rate. The noise floor was reached for a sampling

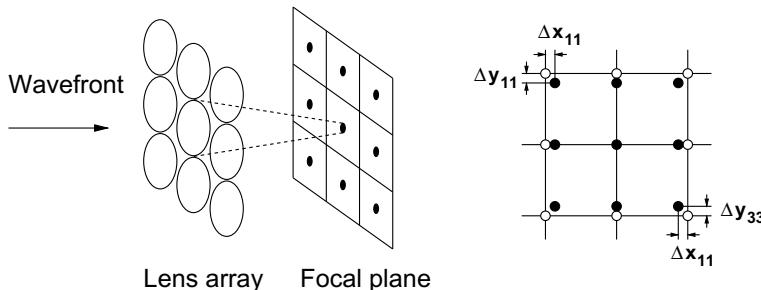


Fig. 6.51 (Left) Principle of Hartmann–Shack wavefront detection. (Right) Focal point pattern of a reference wavefront (open circles) and of a distorted wavefront (filled circles) [71]

time of approximately $200\ \mu\text{s}$ corresponding to an oversampling ratio R_{ov} of about 256 [65]. The SNR for this oversampling ratio is 69 dB.

An analog ASIC facilitating the focal point position detection in a Hartmann–Shack wavefront sensor for optical wavefront measurements was described [71]. The phase information of the light beam can be obtained by detecting the lateral deviation of each focal point of the Hartmann–Shack sensor’s lens array caused by the partial distortion of the aberrated wavefront within the according lens. As a future aim, measuring optical distortions of the human eye was mentioned in [71]. Therefore, the ASIC was optimized to process an optical incident power of $1\ \text{nW}$ per focal point, because the incident power is below $0.01\ \text{W/m}^2$ due to security limitations when directly penetrating the eye’s retina by the measuring beam. To prevent eye movements from disturbing the measurements, a frame repetition rate of several hundred hertz was necessary.

A single-path measurement scheme often applied in an optical wavefront detection system is referred to as the Hartmann–Shack wavefront detection scheme [71]. A Hartmann–Shack sensor (HSS) consists of an array of optical lenses arranged within the optical path to divide the incident light beam into a matrix of subapertures (Fig. 6.51a).

Each lens focuses into a focal point located within the lens array’s focal plane. When a local tilt is present in the wavefront within the aperture of the lens, the focal point is deviated perpendicular to the optical axis (Fig. 6.51b). The magnitude of the deviation is in a first order proportional to the magnitude of the local tilt in the wavefront. The tilt can therefore be quantified. The light beams’s total wavefront can be reconstructed by means of a least-square-fit of the measured data of all focal point deviations. The mathematical description of the optical path difference (OPD) between the calculated wavefront and an arbitrary reference wavefront thereby is commonly based on high-order two-dimensional Zernike polynomials [72, 73].

A lens array is mounted in parallel to the photodetector matrix in a distance of the focal length. When the partial wavefront’s average is tilted within the aperture of a lens, the corresponding focal point is deflected (Fig. 6.52a).

Fig. 6.52 (Left) Deviation of the focal point due to a tilt in the wavefront within the lens. (Right) Intensity distribution of a focal point [71]

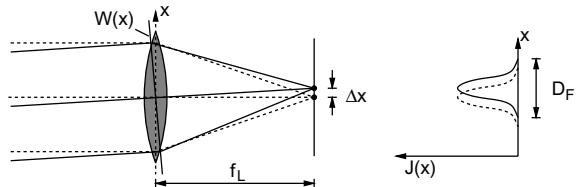
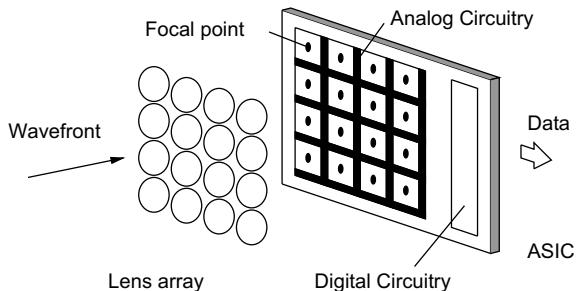


Fig. 6.53 Architecture of the HSS system [71]



Assuming paraxial optics, i.e. $\sin(x) = x$, the deflection Δx can be calculated from [71]

$$\frac{dW}{dx} = \frac{\Delta x}{f_L}, \quad (6.26)$$

where dW/dx is the wavefront's tilt in x -direction and f_L is the focal length of the lenses in the lens array. For $f_L = 53\text{ mm}$ as an example, a wavefront tilt of $dW/dx = 200\text{ nm}/400\text{ }\mu\text{m}$ causes a focal point deflection of $\Delta x = 26.5\text{ }\mu\text{m}$.

The lateral intensity distribution of a focal point can be approximated by a gaussian distribution (Fig. 6.52b). According to Fourier optics, the intensity distribution is circular with minima and maxima of decreasing intensity. The diameter D_F of the first minimum-intensity circle (often referred to as the diameter of the *Airy disc*) is [71]

$$D_F = \frac{1.22\lambda f_L}{D_L} \quad (6.27)$$

with the lens diameter D_L . For $\lambda = 780\text{ nm}$ and $D_L = 400\text{ }\mu\text{m}$, $D_F = 126\text{ }\mu\text{m}$ is obtained which is much larger than $\Delta x = 26.5\text{ }\mu\text{m}$. Thus the signal processing circuitry has to determine the location of the maximum intensity by distinguishing only slightly differing values.

The Hartmann–Shack sensor (HSS) ASIC described in [71] combines photo-sensitive devices for image detection and electrical circuits for focal point position detection (Fig. 6.53). For easy readability, only 4×4 lenses and focal point detectors are drawn whereas the ASIC actually included 16×16 focal point detectors.

Analog circuitry is implemented to evaluate focal point intensity distributions for the maximum by use of the winner-take-all (WTA) algorithm. Parallelism is inherent in this approach as originally presented by Lazzaro [74]. Each focal point detector

Fig. 6.54 (Left) Zoomed illustration of the photodetectors within one cluster. (Right) Global architecture of one cluster [71]

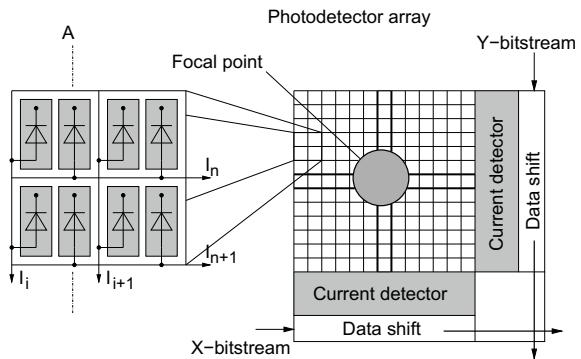
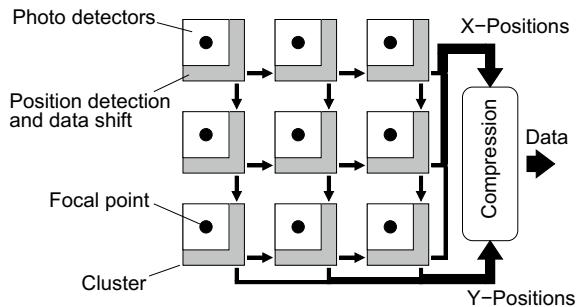


Fig. 6.55 Data flow in the HSS [71]



(called cluster in Fig. 6.54) contains an array of photodiodes and surrounding analog signal processing circuitry to find the location of the focal point's intensity maximum. After detection, the position data is transferred to digital circuitry, where reformatting and compression is performed. The position detection clusters are linked together via shift registers to push the position data to the compression unit (Fig. 6.55). Finally data are sent to the output for a least-square-fit calculation of the Zernike polynomial coefficients.

The lateral dimensions of a cluster were $400 \times 400 \mu\text{m}^2$ to fit the lens diameter. The chip area of the signal processing circuitry had to be kept as small as possible to enlarge the photosensitive area. The photodiodes are placed in a special pattern within the photodetector array of one cluster. The array contains a number of 19×19 photodetector pixels, each consisting of two adjacent photodiodes covering an area of $p^2 = 17.6 \times 17.6 \mu\text{m}^2$ [71]. The left diode is connected to its column neighbors and the right diode is connected to its row neighbors (Fig. 6.54b). In such a way, a number of 19 stripes in each direction is realized, allowing to read out the stripe currents of the x- and y-direction simultaneously. Figure 6.56 shows a cut through the chip along line A in Fig. 6.54 with the intensity distribution of a focal point. Each photodiode stripe is illuminated by a fraction of the incident power within the length p and the row currents I_n are generated.

Fig. 6.56 Intensity distribution of a focal point (not to scale) [71]

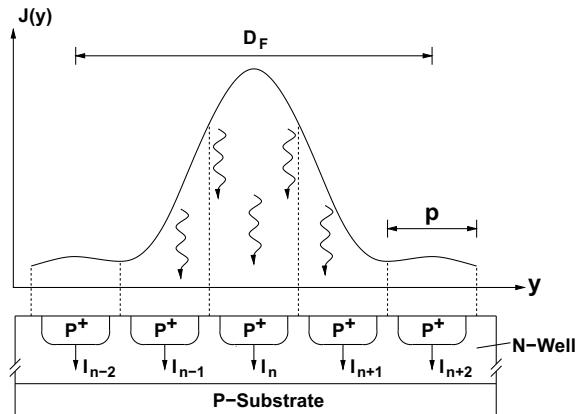
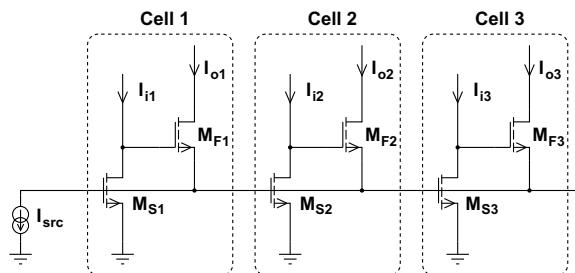


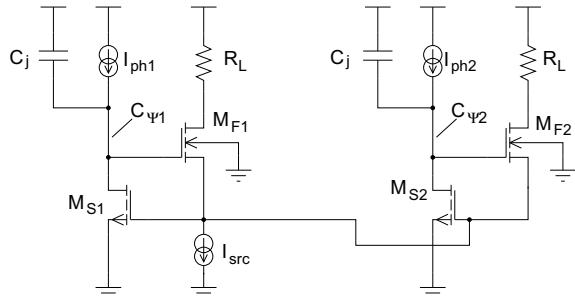
Fig. 6.57 WTA topology illustrated with three cells implementing n-channel MOSFETs [71]



Let us now have a look onto the signal processing circuitry in the HSS. The most important part of the ASIC's signal processing circuit is the current detector for determining the maximum current among the 19 generated photocurrents. MOSFETs are used for that purpose. The winner-take-all (WTA) algorithm proposed in [74] fits best to the task to detect locally a maximum of several photocurrents. The basic circuitry of the WTA topology for position detection as presented in [74] is shown in Fig. 6.57. Three cells are drawn for the detection of three currents. Each cell contains the two MOSFETs M_S and M_F . M_S senses the input current I_i and generates a V_{DS} , which is connected to the gate of M_F . The gates of all transistors M_S are connected, and owing to the same transfer characteristics ($I_D(V_{DS})$), one of them generates the highest drain potential due to its highest $I_D(I_i)$ and V_{GS} of the according M_F is the highest of all transistors M_F . Most of the current of the current source I_{src} is sunk by this M_F and guided to I_o , inhibiting current flow in the other transistors M_F . Since speed properties of this algorithm are essential to the HSS, the transient response has to be investigated in detail.

The transient response of a cell is mainly limited by the capacitance at the drain node C_Ψ of M_{S_n} (Fig. 6.58). When the input current I_{ph2} becomes larger than a constant I_{ph1} , three time steps occur until the output currents change significantly [71]. In the first step, the photocurrent I_{ph2} changes to a higher magnitude, but the gate potential of M_{S_2} keeps the same since it is still defined by M_{S_1} and M_{F_1} . The

Fig. 6.58 Photodiode junction capacitance and parasitic capacitors $C_{\Psi 1}$ and $C_{\Psi 2}$ [71]



parasitic capacitor $C_{\Psi 2}$ is charged by $\Delta I 2 = I_{ph2} - I_{D,S2}$ to raise V_{DS} of M_{S2} . In the second step, $V_{DS}(M_{S2})$ is high enough to significantly affect the current through M_{F2} . Now, M_{F2} inhibits the current flow through M_{F1} by increasing its drain current to almost I_{src} , and the gate potential of M_{S1} and M_{S2} changes to a slightly higher value. In the third step, the capacitor $C_{\Psi 1}$ is discharged, reducing the drain potential of M_{S1} to its equilibrium value. The first time step of recharging the parasitic capacitor $C_{\Psi 2}$ clearly dominates the response time, because of the small amount of ΔI for charging.

The junction capacitance of the photodiode stripe with 19 P⁺/N-well diodes is about 2.3 pF at a reverse voltage of 2 V. According to circuit simulations for a change of the photocurrent I_{ph2} from 46 to 54 pA at a constant I_{ph1} of 50 pA, it takes about 0.6 s to raise V_{DS} of M_{S2} by a value of 1 V from the initial value to change the output current conditions of the two cells significantly [71]. To reduce this unacceptable high value of response time, therefore, different extensions to the basic WTA topology have been introduced.

The largest influence to the response time of a WTA cell stems from the photodiode capacitance C_j . A regulated cascode configuration with transistors M_C and M_R as illustrated in Fig. 6.59 can be applied to reduce the capacitance value appearing at the drain node of the transistors M_{Sn} . The resulting parasitic capacitor at the drain nodes of the transistors M_{Sn} is then dominated by the drain junction capacitor of M_S and the gate capacitor of M_F . It was stated that it takes about 13 ms with the cascode configuration to change the output current conditions significantly [71].

A further improvement of response speed can be achieved by setting the node potential of the drains of transistors M_{Sn} to a defined value, which bypasses the first time step. For that purpose, the transistors M_{In} are introduced at the nodes Ψ_n (Fig. 6.60). With them a start-up value of for instance $V_{init} = 0.9$ V can be set. Since all M_{Fn} conduct the same drain current I_D with ($\sum I_D(M_{Fn}) = I_{src}$), the gate-source voltages V_{GS} of transistors M_{Sn} are forced to a low value almost shutting off transistors M_{Sn} . When the nodes Ψ_n are released for an integration time t_{int} , the capacitors $C_{\Psi n}$ are recharged by the complete photocurrents, as long as $V_{GS}(M_{Sn})$ still prevents significant current flow in transistors M_{Sn} . For the highest photocurrent I_{phi} , M_{Fi} sinks most of I_{src} , inhibiting current flow in the other transistors M_{Fn} , and the cell wins. Due to recharging the capacitors $C_{\Psi n}$ with the complete photocurrent

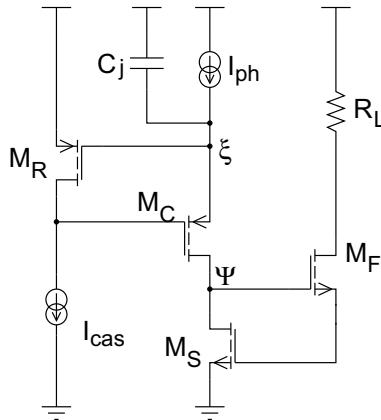


Fig. 6.59 Regulated cascode configuration for enhancing the response speed [71]

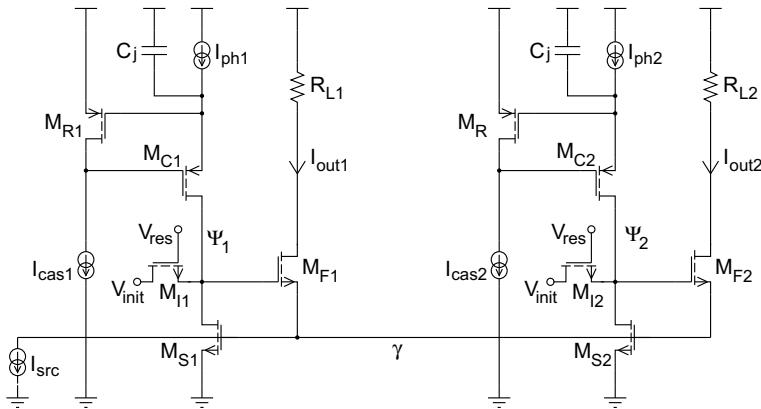


Fig. 6.60 Introduction of an initial condition for the drain potentials of M_S [71]

instead of the difference of photocurrents, the response speed is accelerated by about an order of magnitude [71].

In addition to these two measures, local excitatory feedback is applied as suggested by Starzyk [75], which feeds back a portion of the output current to the input current of each cell, thereby boosting the effect of charging the capacitors C_{Ψ_n} . To adapt the large output current in the range of nanoamperes to the small input photocurrent in the range of picoamperes, a new feedback topology has been implemented. A PMOS current mirror is added, where the feedback attenuation is controlled with the body effect of the output MOSFETs (Fig. 6.61). The amount of current, which is fed back to the input node, is determined by considering the subthreshold drain current characteristics proposed by Vittoz [76] for the body effect, resulting from applying different potentials to the source and bulk terminals of M_{FB} . The ratio I_{out}/I_{fb} is given by

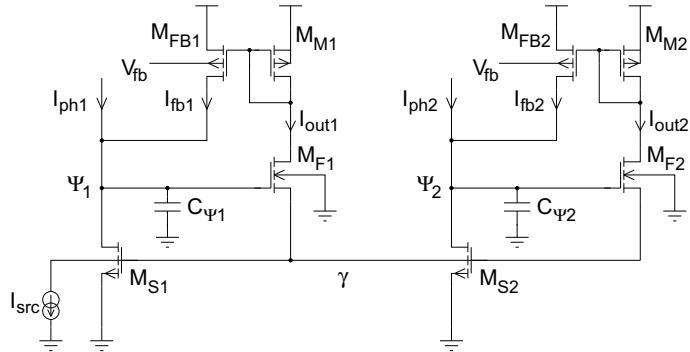


Fig. 6.61 Feedback configuration of a portion of the output currents to the input nodes with the current mirrors M_{Mn}/M_{FBn} [71]

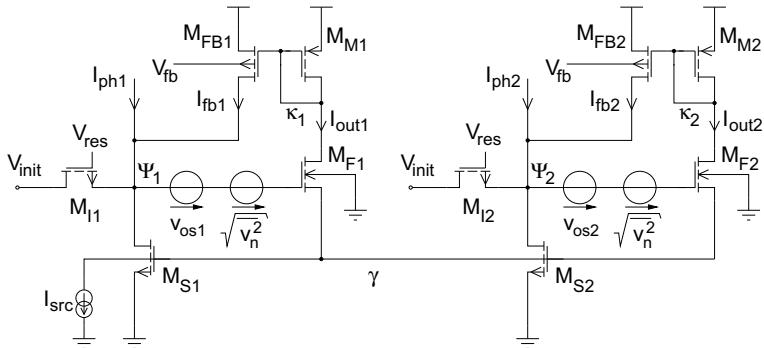


Fig. 6.62 Noise and mismatch considerations of a WTA cell [71]

$$\frac{I_{out}}{I_{fb}} = e^{V_{SB}(n-1)/nV_T}, \quad (6.28)$$

where $n \approx 1.5$ and $V_T = k_B T/q$. According to simulations, a further increase of response speed can be achieved, when the feedback current is well adapted [71].

Implementing all three described topologies in the WTA configuration, the transient response time could be reduced from 0.6 s to below 1 ms [71]. Noise and mismatch, however, increase due to these measures. These issues will be discussed next.

In the picoampere range, noise generally is important and has to be considered. The gate potential of transistors M_{Fn} is very sensitive to noise and mismatch. Two voltage sources therefore are placed at their gates (Fig. 6.62). The first one is taken to model the noise voltage $\overline{v_n^2}$, the second one to consider the effect of mismatch with an offset voltage v_{os} .

Different noise sources contribute to $\overline{v_n^2}$. Poisson's distribution of uncertainty in counting single events has to be applied. The uncertainty n_n of the number of electrons being accumulated at the capacitor C_Ψ , thus, can be calculated from the charge Q

on the capacitor [71]:

$$n_n = \sqrt{N} = \sqrt{\frac{Q}{q}}. \quad (6.29)$$

The first noise contribution to $\overline{v_{n1}^2}$ is caused by the photocurrent I_{ph} , the leakage current of the photodiode I_L , and the feedback current I_{fb} [71]:

$$\overline{v_{n1}^2} = \left(q n_n \frac{1}{C_\Psi} \right)^2 = q \frac{Q}{C_\Psi^2} = \frac{q}{C_\Psi^2} \int_0^t I_{ph} + I_L + I_{fb} d\tau. \quad (6.30)$$

The second noise contribution stems from reset noise by setting the capacitor C_Ψ to a defined value before the integration period. During this period, the capacitor is charged to a voltage with an uncertainty resulting from thermal resistor noise. This noise can be obtained by considering the spectral density of current noise and impedance at the node Ψ [71]:

$$\overline{v_{n2}^2} = \int_0^\infty \frac{2q(I_{ph} + I_L + I_{fb})}{|i2\pi f C_\Psi + g_{ds}(MI) + g_{ds}(MS)|^2} df. \quad (6.31)$$

The third noise contribution is caused when transistor M_I is shut off. Several electrons are pushed to the node Ψ due to charge feedthrough from the gate of M_I . The number of these electrons is [71]

$$n_{i,ft} = \frac{1}{q} C_\Psi \Delta V. \quad (6.32)$$

With Poisson's statistics, the third noise contribution is obtained [71]:

$$\overline{v_{n3}^2} = \frac{1}{C_\Psi^2} (\sqrt{n_{i,ft}} q)^2 = \frac{1}{C_\Psi} q \Delta V. \quad (6.33)$$

Flicker noise (1/f-noise) causes the fourth contribution to noise [71]:

$$\overline{v_{n4}^2} = \int_0^{f_0} \frac{K F}{2 f C_{ox} W L K'} df. \quad (6.34)$$

Thermal noise of the channel resistance of M_F transforms to its gate and forms the fifth contribution to noise [71]:

$$\overline{v_{n5}^2} = \int_0^{f_0} \frac{8k_B T}{3g_m} df. \quad (6.35)$$

The bandwidth of the transfer function of transistor M_F can be calculated with a small-signal analysis of I_{src} , M_F , M_M , and the parasitic capacitors C_κ of the node κ

[71]:

$$f_0 = 1.57 f_1 = 1.57 \frac{1}{2\pi} \frac{g_m(M_M) + g_{ds}(M_F)}{C_\kappa} df, \quad (6.36)$$

where the relation $f_0 = 1.57 f_1$ considers a transfer function with a single pole at the frequency f_1 .

The different noise contributions are independent and the equivalent noise of the circuit shown in Fig. 6.62 is therefore obtained as [71]

$$\overline{v_n^2} = \sum_{i=1}^5 \overline{v_{ni}^2} = \overline{v_{np}^2}(I_{ph}) + \overline{v_{nc}^2}, \quad (6.37)$$

where $\overline{v_{np}^2}$ represents the noise depending on the amount of charge on the capacitor C_Ψ accumulated by the photocurrent I_{ph} and where $\overline{v_{nc}^2}$ represents the noise floor.

When a photocurrent of 10 pA is accumulated on C_Ψ during an integration period t_{int} of 1 ms, the uncertainty of the voltage across the capacitor C_Ψ was calculated in [71] from (6.37):

$$\frac{\sqrt{\overline{v_n^2}}}{\Delta V_\Psi} = \frac{2.7 \text{ mV}_{\text{rms}}}{200 \text{ mV}} \approx 1.3\%. \quad (6.38)$$

When a significant current I_{fb} is flowing, the noise properties of the circuit depend strongly on the ratio of I_{ph}/I_{fb} , which is a nonlinear function of $\overline{v_n^2}$ [71]. For that case, a simple analytical expression could not be derived [71]. Measurement of focal point positions revealed an error due to noise. In feedback mode with an incident optical power of 1 nW ($\lambda = 680 \text{ nm}$) per focal point and with an integration time of 1 ms, the detection of the focal point position suffered from an average noise level of 1.89 pixels for the x -direction and 1.81 pixels for the y -direction, with a pixel size of $17.6 \mu\text{m}$ [71].

Mismatch between the WTA cells is also critical for the functionality of the WTA scheme. The accuracy of distinguishing input currents for differences is based on comparing node potentials of several identically built circuit blocks. To estimate consequences of fixed pattern noise (FPN), the voltage source v_{os} has been added in the WTA cell (Fig. 6.62). Neglecting mismatch of the photodiode stripes, the most important mismatch results from V_{GS} deviations of transistors M_S , M_F , and M_{FB} , from different charge injection values of M_I , and from differing values of the capacitors C_Ψ [71].

Noise and mismatch contribute to the total uncertainty of $V_{GS}(M_F)$ [71]:

$$\sigma(V_{GS}(M_F)) = \sqrt{\overline{v_n^2} + v_{os}^2}. \quad (6.39)$$

The accuracy of the WTA function can be estimated by forming the ratio of this uncertainty to the capacitor voltage difference ΔV_Ψ due to the accumulated photocurrent during the integration period. The difference of the photocurrent of two neighboring photodiode stripes is determined by the light spot diameter and the

stripe width and is therefore at most 8% [71]. Thus, a wrong decision of the WTA circuit happens when $\sigma(V_{GS})/\Delta V_\Psi > 8\%$.

Optical glasses of spectacles were measured, to demonstrate the main issue of the HSS ASIC to quantify wavefront aberrations. For that purpose the optical glasses were placed between the laser source and the lens array. The focal point positions captured by the ASIC were fed into a personal computer to perform a least-square-fit for calculating the Zernike polynomial coefficients, from which spherical and cylindrical aberrations can be derived [72]. For integration times of 1, 2, and 4 ms and frame repetition rates of 500, 333, and 200 Hz, respectively, the observed relative errors for the spherical and cylindrical aberrations of the optical glasses were 7.5, 6, and 4.5%, i.e. 0.15, 0.12, and 0.09 diopters [71].

In order to prevent illumination and photogeneration in the sensitive analog circuitry, the ASIC was shielded completely by a metal layer, except for the photosensitive areas. The ASIC was fabricated in a $0.6 \mu\text{m}$ N-well CMOS process with single poly and triple metal. The chip dimensions were $7.7 \times 8.2 \text{ mm}^2$ [71].

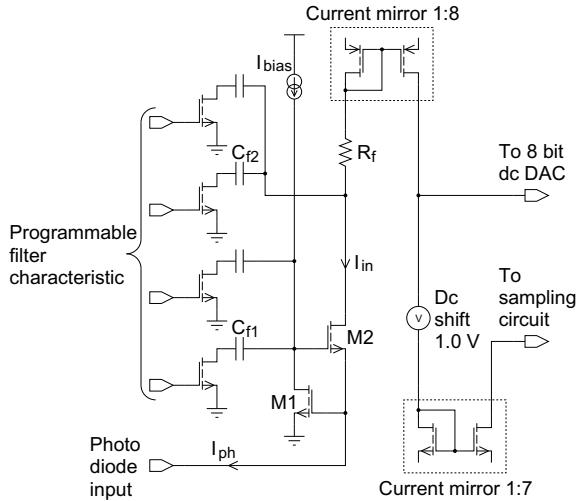
6.4.9 BiCMOS Optical Sensors

There is a huge variety of optical sensors. It is not possible to describe all of them here. In the following a movement detection system working with infrared light consisting of a low-noise input amplifier, a low-pass filter, and a 10-bit tracking analog-to-digital converter as well as a laser driver with a low current noise is discussed [77]. This system was integrated on a chip in $0.5 \mu\text{m}$ standard BiCMOS technology. The photodiode is shown in Fig. 2.60.

The low-noise input amplifier will be introduced next. The system works with a high level of dc background light and a very weak level of ac signal light in the frequency range 10 Hz–50 kHz. Since the spectral density of the shot noise of a photodiode is proportional to the total photocurrent (high dc part and weak ac part), whereas the ac-signal-to-noise-ratio is important in the system, the only way to reduce the total integrated shot noise is to limit the noise bandwidth. This has to be done properly, because signals in the operating bandwidth have to stay undamped. The circuit principle of the input stage implemented in the system is illustrated in Fig. 6.63.

The frequency characteristics is programmable for minimizing the noise bandwidth and for avoiding peaks in the noise transfer characteristics. The photodiode is biased reversely with a constant voltage due to NMOS transistor M2 with its transconductance g_{m2} . The PIN photodiode in standard BiCMOS technology shown in Fig. 2.60 was integrated together with the low-noise input amplifier depicted in Fig. 6.63. The photocurrent is filtered by the programmable low-pass filter of second order. The transfer function of the input stage is [77]

Fig. 6.63 Principle of low-noise input amplifier [77]



$$\frac{I_{in}(s)}{I_{ph}} = \frac{1 + s \frac{C_{f1}}{g_{m1}}}{s^2 \frac{C_{f1} C_D}{g_{m1} g_{m2}} + s \frac{C_{f1}}{g_{m1}} + 1} \quad (6.40)$$

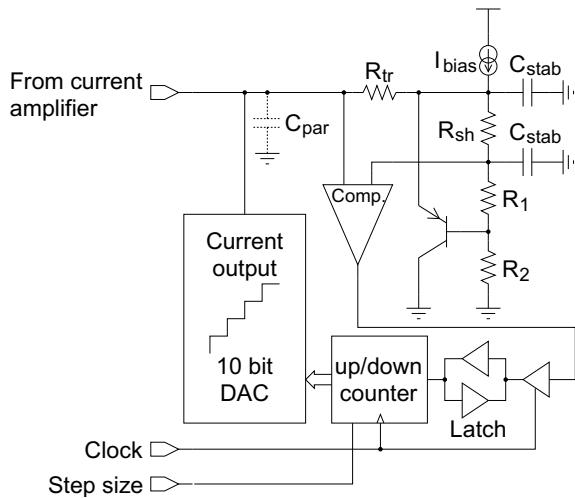
with the photodiodes capacitance C_D , the sum of the programmable filter capacitors C_{f1} , and the transconductances g_{m1} and g_{m2} of the input transistors. R_f and C_{f2} form an additional low-pass filter for I_{in} and complete the filter of second order. Current mirrors realize the required amplification for the photocurrent. The compensation of the dc part of the photocurrent is done between the two current mirrors. For a reliable operation of the 8-bit DAC for the dc compensation an additional dc voltage shift is necessary as included in Fig. 6.63 [77].

As typical values for the ac part of the photocurrent 0.5 nA and 0.5 μ A for its dc part were mentioned in [77]. The dc part multiplied by the amplification of the first current mirror is compensated by the dc DAC being controlled by a digital algorithm.

The application of the system required a 10-bit word for the ac part every 10 μ s. A clock frequency of 1 MHz was used to transmit the 10-bit word via a serial interface. A tracking ADC (Fig. 6.64) to save chip area could be implemented for the 10-bit ADC assuming a more or less continuous input signal.

In the tracking ADC, the current difference between the input current and the current of the 10-bit DAC produces a voltage drop across the transimpedance resistor R_{tr} . This voltage drop is limited by the least-significant-bit (LSB) current of the 10-bit DAC. The comparator decides every clock cycle, whether the counter should count up or down. To synchronize the comparator output it has to be latched before the counter changes its output. The sampling speed of the system was limited by the maximum allowed current consumption. The design of the comparator in the tracking ADC, therefore, had to be done carefully by optimizing the speed and limiting the current consumption of this circuit module. The parasitic input capacitance C_{par} of the

Fig. 6.64 Tracking analog-to-digital converter as sampling system [77]



tracking ADC had to be minimized by a carefully performed chip layout, because the charge/discharge current of the parasitic capacitance at the input node is represented by the LSB DAC current of 50 nA and therefore puts a speed limit for the tracking ADC [77].

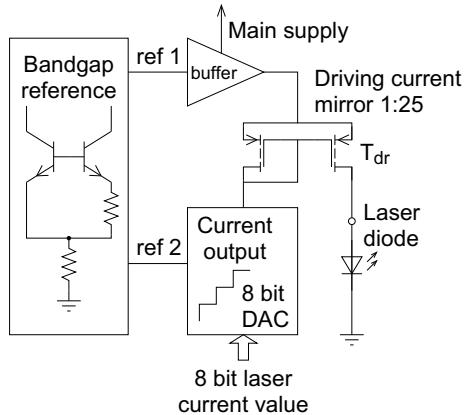
The voltage divider formed by R_{sh} , R_1 , and R_2 serves as a bias structure for the comparator input. Adaptive count steps are used in the 10-bit up/down counter in order to follow faster changing signals with a higher slew rate [77].

The system discussed here is a light transmitting and receiving system. A laser diode with a wavelength of 780 nm has to be driven in this system. In order to achieve a photocurrent of 1 μ A in the photodiodes integrated in the movement detection chip, the laser diode needs a maximum current of about 11 mA [77]. Figure 6.65 depicts the low-noise laser driver circuit also implemented in the BiCMOS optical sensor chip.

Special measures are necessary to ensure that the current through T_{dr} is free of any disturbances from the power supply. For that purpose the bandgap reference supplied voltage ref1 in Fig. 6.65 is amplified in the buffer in such a way that the minimum voltage across the driver transistor T_{dr} is at least 300 mV for the highest laser diode current of 11 mA. The reference current ref2 (Fig. 6.65) in addition has to be provided by a buffered bandgap reference voltage and a temperature compensated resistor network in order to become independent from the main supply [77].

It was very important for the application that the emitted light was free of any noise, because noise in the emitted light would reduce the signal-to-noise ratio of the receiving part in the system. Since above the laser threshold current the emitted light is approximately proportional to the laser diode current, the driver output current had to be free of current noise. With the configuration shown in Fig. 6.65 an integrated RMS noise current of only $0.5 \mu\text{A}$ up to 300 kHz at a driving current of 11 mA was achieved [77].

Fig. 6.65 Block diagram of low-noise laser driver circuit [77]



Due to the various tricks described, the innovative light detection chip achieved low-noise amplification, high sampling speed, and a low over-all current consumption of 4 mA in a voltage operating range from 3.0 to 5.5 V whereby the laser diode current was not included. The proposed system consisting of six receiving channels, the laser driver unit, voltage regulation, and a digital interface was realized within a chip area of about 18 mm². The integration of such an analog-digital system also including the optical detectors on the mixed-signal chip posed a challenge. The coupling of clock signals from the digital part of the system to the sensors consuming a large area and generating only a very weak signal, however, could be avoided by placing the digital part near the chip corner and locating digital signal lines as well as digital pads as far away as possible from the sensor array and the input amplifiers [77].

6.4.10 Sensors Using Single-Photon Detection

An ambient light sensor in 0.13 μm CMOS using an SPAD array being appropriate as proximity sensor in smart phones was introduced [78]. The chip area and power consumption were reduced by implementing simple digital circuits for detection and counting of photons. A metal filter structure enabled operation within 100 to 25,000 lux. The chip area was 0.046 mm² and the power consumption was 125 μW at 1.0 V. The bias voltage for the SPADs was 10.5 V.

A 32 × 32 SPAD imager in 0.18 μm CMOS being able of photon counting and determining the photon arrival time simultaneously for taking 2D and 3D images was reported [79]. Each pixel contained four SPADs with independent time gating and quenching, a common 50 ps resolution time-to-digital converter, and 4 independent photon counters enabling several operation modes. The SPAD array pitch was 100 μm with a fill factor of 9.6%. The chip dimensions were 4.2 × 4.6 mm².

A 160×120 SPAD imager in $0.35\text{ }\mu\text{m}$ technology for fluorescence lifetime imaging was presented [80]. The SPAD median dark count rate was 580 Hz at 3 V excess bias. The chip size was $3.42 \times 3.55\text{ mm}^2$. The analog counter had a sensitivity of 16.5 mV per SPAD event. With a compact pixel circuit needing only seven MOS transistors and a MOS capacitor a pitch of $15\text{ }\mu\text{m}$ and a fill factor of 21% were possible. This image sensor acquired information on photon position, number of photons, and time distribution resulting in a cost-effective sensor for scientific imaging applications. The self-referenced ADC was capable of cancelling out pixel-to-pixel non-uniformities and of speeding up the frame rate to 486 frames/s. The analog output needed a power of 20.6 mW and in the digital mode the sensor chip consumed 156.7 mW [80].

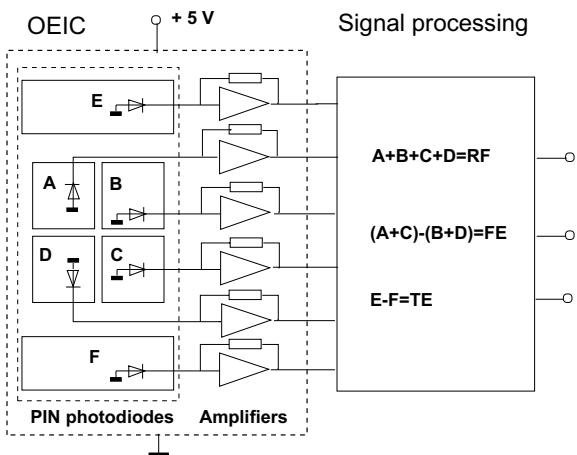
A quarter video graphics array (QVGA) image sensor with a 320×240 SPAD pixel array using a $8\text{-}\mu\text{m}$ pitch and realizing a fill factor of 26.8% was described in [81]. A shared well SPAD devices topology was essential to obtain this pitch and fill factor. The dark count rate of the SPADs was 47 counts/s with an excess bias voltage of 1.5 V . The photon detection probability (PDP) of the SPAD was 39.5% at 480 nm . A minimum dead time of 1.1 ns was reported. Analog photon counting was exploited with a sensitivity of 14.2 mV per SPAD event. The minimum equivalent read noise was 0.06 e^- . Used as a binary quanta image sensor (QIS), a 16-kframes/s real-time oversampling was demonstrated and the single-photon QIS theory was verified with 4.6-fold overexposure latitude and a read noise of 0.168 e^- . The chip size was $3.4 \times 3.1\text{ mm}^2$. It was stated that the approach is scalable to megapixel arrays [81].

A 256×256 3D-integrated SPAD imager for direct time-of-flight (DTOF) applications consisting of a back-illuminated SPAD wafer in 45 nm CMOS CIS technology and a 65 nm low-power CMOS wafer was introduced [82]. The DTOF sensor system working at 532 nm used a dual axis scanner and a laser signature identification technique. This technique exploited digital polar modulation with phase-shift keying (PSK) on the emitted light leading to a suppression of an interference laser at 637 nm with 32-PSK by 18.6 dB . The sensor worked in a 150 m range with 7 cm accuracy in the high-resolution mode. In the low-resolution mode, the range was 430 m at 80 cm accuracy. The chip size was $0.25 \times 0.8\text{ mm}^2$ [82].

6.4.11 CMOS Circuits for Optical Storage Systems

Compact disk (CD), CD-ROM, and Digital-Video-Disk/Digital-Versatile-Disk (DVD) are optical storage (OS) systems with a storage capacity of the order of $1\text{--}10\text{ GByte}$ [83]. The stored information is read with a focused laser beam. Depending on the stored state of 0 or 1, more or less light intensity is reflected into the read circuit, which we will call OS-OEIC. Special arrangements of 6 to 8 photodiodes are implemented in OS-OEICs in order to obtain the signals for tracking and for focusing in addition to the RF signal, which contains the stored information (see Fig. 6.66). Digital-video-recording (DVR) systems allow also writing of information by the focused

Fig. 6.66 OEIC for compact disc, CD-ROM and DVD applications



laser beam. In contrast to the name *digital-video-disc-system*, the DVD-OEIC is a purely *analog* front-end circuit, which is a key-device for the whole DVD-system. OS-OEICs for CD and CD-ROM are also analog circuits. The data rate and therefore the speed of the optical storage system are determined by the OS-OEIC.

In OS systems, accordingly, the demand for fast OEICs is steadily increasing, especially in the red spectral range ($\lambda \approx 635\text{--}650\text{ nm}$). The integration of both the optical devices and the electronic circuits on the same chip leads to a smaller die area, to lower manufacturing costs and to faster systems. Furthermore, the reliability and the immunity against electromagnetic interference of OEICs are enhanced compared to a two-package solution with a photodiode package and an amplifier package. In comparison to a two-chip solution with a photodetector chip being wire-bonded to an amplifier chip in one package, the die area consumption of a monolithic OS-OEIC is smaller, because the area of a photodiode in an OS system is smaller than the area of a bondpad.

For fast OS systems, integrated PN photodiodes are not sufficient, because only a bandwidth of 10–15 MHz is achievable [84, 85]. Although a -3 dB bandwidth of 32 MHz can be derived from the frequency response of a P⁺ to N-substrate photodiode shown in Fig. 2.14, the photocurrent already begins to decrease at a frequency of 2 MHz due to slow diffusion of photogenerated carriers. Hence, PIN photodiodes are required. It was shown that for the integration of a PIN photodiode in a standard twin-well CMOS process (1 μm), which uses epitaxial wafers, little modification is necessary. Compared to the published approaches in [86, 87] with standard-buried-collector (SBC) based bipolar OEICs, less additional process complexity is required [88] as was already pointed out in Sects. 2.1.3 and 2.2.6. The cross section of a CMOS-OEIC was already shown in Fig. 2.20.

In order to obtain fast integrated PIN photodiodes, the standard doping concentration of the epitaxial layer of $1 \times 10^{15}\text{ cm}^{-3}$ has to be reduced to approximately $5 \times 10^{13}\text{ cm}^{-3}$ [88]. This reduction of the doping level does not influence the elec-

trical parameters of the CMOS devices, since the MOSFETs are placed in wells and, therefore, the model parameters for circuit simulation did not have to be modified for the design of the OEICs [89]. ESD (electrostatic discharge) and latch-up immunity could be obtained by appropriate layouts.

OS-OEICs have to fulfill a stringent requirement concerning the output offset voltage. A fast and low-area CMOS optoelectronic integrated circuit (OEIC) for optical storage (OS) systems containing photodiodes and transimpedance amplifiers with a low offset voltage was presented [90]. The photodiodes and the amplifiers were monolithically integrated in a $0.6\text{ }\mu\text{m}$ CMOS process. A replica transimpedance amplifier and a low-offset operational amplifier were implemented for offset reduction. An expression for the standard deviation of the output offset voltage was derived analytically [90]. A -3 dB frequency of 147 MHz and a sensitivity of $24\text{ mV}/\mu\text{W}$ at 670 nm were measured, as well as an offset voltage deviation of 4 mV . With this performance, an innovative low-cost CMOS OEIC was suggested being a true alternative to BiCMOS OEICs developed and used in the years 2002 and 2003.

Optical storage systems such as Audio CD, CD-ROM (compact disk read only memory), DVD (digital video disk or digital versatile disk), or DVR (digital video recording) require OEICs with a high bandwidth, a high sensitivity, and a low output offset voltage compared to an external reference voltage V_{Ref} . To achieve high bandwidths and low offset voltages bipolar or BiCMOS processes are preferred [91, 92]. In [93] an OS OEIC exploiting complementary bipolar current mirrors with a bandwidth of 250 MHz in BiCMOS technology was described. Apart from the absent description of the essential idea, fast PNP transistors were needed, which are only available in costly BiCMOS processes. The OEIC proposed in [90], however, was implemented in a low-cost $0.6\text{ }\mu\text{m}$ CMOS process.

Usually operational amplifiers in transimpedance configuration perform the photocurrent to voltage conversion [91, 94, 95]. But low-offset CMOS operational amplifiers need large-area input transistors. Therefore it is difficult to achieve high-speed CMOS OS OEICs [94, 95]. Fiber receivers often use inverters in transimpedance amplifiers as for instance in a 155 Mb/s -receiver [96] or in a 1 Gb/s -receiver [97]. To obtain a high bandwidth in the CMOS OS OEIC, the transimpedance amplifier of the OEIC proposed in [90] consists of a one-stage inverter with a polysilicon feedback resistor and two source followers, which reaches a bandwidth of 147 MHz and a sensitivity of $24\text{ mV}/\mu\text{W}$. In the operating temperature range and due to process variations, the dark-level output voltage of the CMOS OS OEIC would vary from 2.43 to 2.64 V . To reduce this output offset voltage, a replica offset cancellation (ROC) circuit suggested for BiCMOS OS OEICs in [92] was used. Alternatively, this could be done by subtracting the output voltage of the replica amplifier from the output voltage of the transimpedance amplifier [98, 99], but this method requires a fast subtracting circuit. This disadvantage can be avoided, if a rather slow low-offset operational amplifier is used to adjust the output bias voltage of both the inverter-transimpedance and the replica inverter-amplifier to be equal to the reference voltage V_{Ref} . With this method we can achieve an output offset voltage of much less than 15 mV .

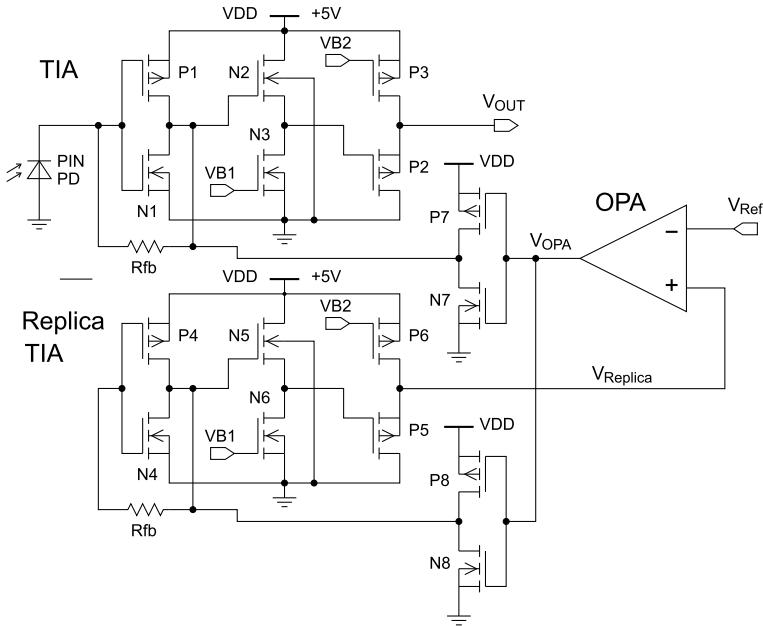


Fig. 6.67 Simplified schematic of low-offset CMOS DVD OEIC [90]

To be able to judge the over-all performance of an OS OEIC a figure of merit FOM, which combines the bandwidth $f_{3\text{dB}}$, the sensitivity S and the maximum output offset voltage V_{offset} of an OS OEIC, can be defined [90]:

$$FOM = \frac{f_{3\text{dB}} \cdot S}{V_{\text{offset}}} \quad (6.41)$$

Combining the results mentioned above, this CMOS OS OEIC described here featured an outstanding figure of merit of $287\text{MHz}/\mu\text{W}$.

Besides the use of a low-cost CMOS process, a complete OS OEIC, using the proposed circuit, would only occupy a chip area of about 1mm^2 [90]. Common comparable OEICs need chip areas of 2mm^2 [94] to 3.25mm^2 [91, 92].

The simplified schematic of the OEIC is shown in Fig. 6.67. The transimpedance amplifier consists of a single-stage inverter N1/P1 and a feedback resistor Rfb. Two source-followers N2/N3 and P2/P3 are appended to drive a load capacitance of up to 10pF . VB1 and VB2 are bias voltages. The replica transimpedance amplifier has the same structure and exactly the same layout as the transimpedance amplifier. A very simple method to vary the DC level of the output voltage was implemented by the inverters N7/P7 respectively N8/P8. Because of the use of long-channel transistors, their output resistance is rather high (approximately $500\text{k}\Omega$). So they act as bipolar current sources pulling the output voltages of the inverters N1/P1 and N4/P4 up or down by $\pm 0.34\text{V}$. A low-offset operational amplifier is used to regulate the output

Table 6.1 Variances and their weights needed in (6.57) [90]

Parameter	a_j	σ_j^2 (mV ²)
VTN1	0.4866	21.45
VTP1	-0.5134	12.89
VTN2	-1	5.005
VTP2	1	0.669
VTN4	-0.4866	21.45
VTP4	0.5134	12.89
VTN5	1	5.005
VTP5	-1	0.669
VTN7	0.1301	20.02
VTP7	-0.1032	12.03
VTN8	-0.1301	20.02
VTP8	0.1032	12.03
$V_{\text{offset,OPA}}$	-1	0.858

voltage of the replica transimpedance amplifier V_{Replica} to the same level as the reference voltage V_{Ref} . The operational amplifier uses a standard differential input stage with a complementary output stage. A similar structure is described in [100]. Because the used CMOS operational amplifier has no systematic offset and a gain being sufficiently large, the output voltage should be equal to the reference voltage V_{Ref} if no light is coupled into the photodiode. But as a result of non ideal matching of the transistor pairs N1/N4, P1/P4, N2/N5, P2/P5, N7/N8, P7/P8 and of the input transistors of the operational amplifier, an output offset voltage occurs. We assume that the values of the threshold voltages V_T of the MOS transistors are distributed normally with the variances $\sigma_{V_T}^2$. The variance $\sigma_{V_T}^2$ can be derived by [90]

$$\sigma_{V_{Ti}}^2 = \frac{\text{AVTOL}^2}{W_i L_i}, \quad (6.42)$$

where L_i is the length and W_i is the width of the transistor i. AVTOL is a process dependent matching parameter. Table 6.1 lists the $\sigma_{V_T}^2$.

To determine the standard deviation of the output offset voltage, an equation describing the dependence of the output voltage on the transistor threshold voltages V_{Ti} and the input offset voltage V_{IO} of the CMOS operational amplifier is derived [90]. At first we determine the output voltage of the inverter N1/P1, which is also the output voltage of the inverter N7/P7. Equation (6.43) shows the relation of their drain currents.

$$I_{DS,N1} + I_{DS,N7} = I_{DS,P1} + I_{DS,P7}. \quad (6.43)$$

Using a simple large-signal MOSFET model, (6.44) follows, where V_{OPA} is the output voltage of the operational amplifier.

$$\begin{aligned} & \frac{\text{KPN}}{2} \frac{W_{\text{N1}}}{L_{\text{N1}}} (V_{\text{DS,N1}} - V_{\text{TN1}})^2 + \\ & \frac{\text{KPN}}{2} \frac{W_{\text{N7}}}{L_{\text{N7}}} (V_{\text{OPA}} - V_{\text{TN7}})^2 = \\ & = \frac{\text{KPP}}{2} \frac{W_{\text{P1}}}{L_{\text{P1}}} (V_{\text{DD}} - V_{\text{DS,N1}} - V_{\text{TP1}})^2 + \\ & \quad \frac{\text{KPP}}{2} \frac{W_{\text{P7}}}{L_{\text{P7}}} (V_{\text{DD}} - V_{\text{OPA}} - V_{\text{TP7}})^2 . \end{aligned} \quad (6.44)$$

The gain factor of the NMOS transistors KPN is higher than the gain factor of the PMOS transistors KPP. To compensate this imbalance, the width of the PMOS transistors W_{Pi} of all inverters are chosen by the relation (6.45):

$$\frac{W_{\text{Pi}}}{W_{\text{Ni}}} = \frac{\text{KPN}}{\text{KPP}} . \quad (6.45)$$

To minimize the length of the following equations the definitions (6.46)–(6.48) are established:

$$k = \frac{W_{\text{N1}} L_{\text{N7}}}{W_{\text{N7}} L_{\text{N1}}} = \frac{W_{\text{N4}} L_{\text{N8}}}{W_{\text{N8}} L_{\text{N4}}} \quad (6.46)$$

$$V_{\text{iA}} = V_{\text{DD}} - (V_{\text{TPi}} + V_{\text{TNi}}) \quad (6.47)$$

$$V_{\text{iS}} = V_{\text{DD}} - (V_{\text{TPi}} - V_{\text{TNi}}) . \quad (6.48)$$

Now (6.44) is solved for the drain-source voltage $V_{\text{DS,N1}}$, which is equal to the output voltage of the inverter N1/P1

$$V_{\text{DS,N1}} = \frac{V_{\text{iS}}}{2} + \frac{V_{\text{7A}} V_{\text{7S}} - 2 V_{\text{OPA}} V_{\text{7A}}}{2k V_{\text{1A}}} . \quad (6.49)$$

The output voltage V_{OUT} of the transimpedance amplifier can be derived by (6.50)

$$V_{\text{OUT}} = V_{\text{DS,N1}} + V_{\text{GS,P2}} - V_{\text{GS,N2}} . \quad (6.50)$$

Inserting (6.49) into (6.50), (6.51) follows:

$$\begin{aligned} V_{\text{OUT}} = & V_{\text{GS,P2}} - V_{\text{GS,N2}} + \frac{V_{\text{iS}}}{2} + \\ & + \frac{V_{\text{7A}}}{2k V_{\text{1A}}} (V_{\text{7S}} - 2 V_{\text{OPA}}) . \end{aligned} \quad (6.51)$$

In an equivalent way (6.52), which describes the output voltage of the replica transimpedance amplifier V_{Replica} , can be obtained:

$$\begin{aligned} V_{\text{Replica}} = & V_{\text{GS,P5}} - V_{\text{GS,N5}} + \frac{V_{4S}}{2} + \\ & + \frac{V_{8A}}{2kV_{4A}} (V_{8S} - 2V_{\text{OPA}}) . \end{aligned} \quad (6.52)$$

Equation (6.53) applies, if the voltage gain of the operational amplifier is adequately large. V_{IO} is the input offset voltage of the CMOS operational amplifier:

$$V_{\text{Replica}} = V_{\text{Ref}} - V_{\text{IO}} . \quad (6.53)$$

If (6.52) and (6.53) are combined, the output voltage of the operational amplifier V_{OPA} can be derived:

$$\begin{aligned} V_{\text{OPA}} = & \frac{kV_{4A} (V_{\text{IO}} - V_{\text{Ref}} + V_{\text{GS,P5}} - V_{\text{GS,N5}})}{V_{8A}} + \\ & + \frac{kV_{4A} V_{4S} + V_{8A} V_{8S}}{2V_{8A}} . \end{aligned} \quad (6.54)$$

If this result is inserted into (6.51), (6.55) follows:

$$\begin{aligned} V_{\text{OUT}} = & V_{\text{GS,P2}} - V_{\text{GS,N2}} + \frac{V_{1S}}{2} + \frac{V_{7A}}{2kV_{1A}V_{8A}} \bullet \\ & \bullet \left[2kV_{4A} (V_{\text{Ref}} - V_{\text{IO}} + V_{\text{GS,N5}} - V_{\text{GS,P5}}) + \right. \\ & \left. + V_{7S}V_{8A} - V_{8A}V_{8S} - kV_{4A}V_{4S} \right] . \end{aligned} \quad (6.55)$$

In (6.56), the output offset voltage V_{offset} is defined:

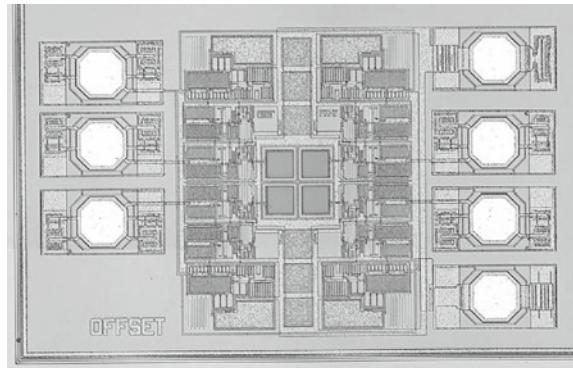
$$V_{\text{offset}} = V_{\text{OUT}} - V_{\text{Ref}} . \quad (6.56)$$

The expected value of V_{OUT} is equal to V_{Ref} , so the expected value of V_{offset} is zero. The variance of the output voltage σ_{OUT}^2 , which is equal to the variance of the offset voltage, can be obtained by:

$$\sigma_{\text{OUT}}^2 = \sum_j a_j^2 \sigma_j^2 \quad (6.57)$$

$$\text{with } a_j = \frac{\partial V_{\text{OUT}}}{\partial V_j} . \quad (6.58)$$

Fig. 6.68 Chipfoto of low-offset CMOS DVD OEIC [90]



V_j stands for the threshold voltages of the transistors N1-8 and P1-8 as well as the input offset voltage V_{IO} of the operational amplifier. In the calculation of the derivations of V_{OUT} , it is possible to assume that the variances of the gate-source voltages are equal to the variances of the threshold voltages. Because of their rather large area it is not necessary to consider the threshold voltage variances of the transistors N3, P3, N5, and P5. The values of a_j are derived from (6.58) and (6.55). The variances σ_j^2 are derived from (6.42). The values of a_j and σ_j^2 are listed in Table 6.1. In consideration of (6.57) from these values the standard deviation of the output voltage $\sigma_{OUT} = 5.486 \text{ mV}$ follows. This means that 99.4% of the produced OEICs have a dark-level output voltage of $V_{Ref} \pm 15 \text{ mV}$ [90].

A PIN photodiode, similar to that described in [101], was applied on a P^+ substrate. The anode of the photodiode was formed by the P^+ substrate and was connected to ground. The cathode of the PIN photodiode was formed by an N^+ source/drain region. An antireflection coating (ARC) was used to achieve a high photodiode quantum efficiency $\eta = 96.5\%$ at $\lambda = 670 \text{ nm}$. Rise times of 660 ps and fall times of 620 ps were measured at the photodiode.

To exploit the available chip area, four identical OS receivers were implemented on one chip. The chip was fabricated using a $0.6 \mu\text{m}$ CMOS process. Figure 6.68 shows a microphotograph of the four receivers each with an associated photodiode. The whole chip including the bondpads occupies an area of $930 \mu\text{m} \times 555 \mu\text{m}$. Figure 6.69 shows one of the four receivers in detail, consisting of the PIN photodiode (PD), the transimpedance amplifier (TIA), the replica transimpedance amplifier (Replica), and the operational amplifier (OPA).

The OS OEIC was measured on wafer level. The results of one receiver typical for all four receivers are shown in Table 6.2.

For all measurements the supply voltage V_{DD} was 5 V and the reference voltage V_{Ref} was 2.5 V. The light was coupled into the photodiode via a single-mode optical fiber adjusted on a wafer prober. The light source was a laser diode with an optical wavelength of $\lambda = 670 \text{ nm}$ modulated via a bias-tee. The output voltage was measured with a picoprobe (input capacitance 0.1 pF, bandwidth 3 GHz). The transient response was measured with a digital storage oscilloscope Tektronix CSA8000. Rise times of

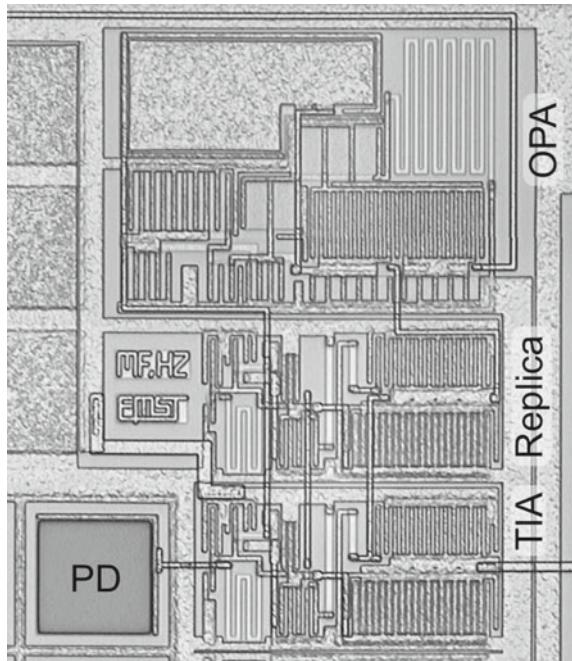


Fig. 6.69 Chipfoto of one channel in low-offset CMOS DVD OEIC

Table 6.2 Summary of results for the low-offset CMOS OEIC [90]

	SpectreS simulation	Measured results
Supply current	13.6 mA	10.6 mA
Sensitivity	29.2 mV/ μ W	23.9 mV/ μ W
Transimpedance	58.3 k Ω	46.0 k Ω
Bandwidth	191 MHz	147 MHz
Rise time	1.85 ns	2.40 ns
Fall time	1.87 ns	2.45 ns
Noise voltage density (at 100 MHz)	36 nV/ $\sqrt{\text{Hz}}$	–

2.4 ns and fall times of 2.45 ns were measured. The frequency response was measured with a network analyzer Hewlett Packard 8753E. The frequency response of the OS receiver, displayed in Fig. 6.70, shows a flat response with a bandwidth of 147 MHz. The bandwidth as well as the supply current are lower than the simulated values (see Table 6.2), which is caused by process tolerances. The lower sensitivity could be explained by tolerances of the feedback resistor or of the antireflection coating of the photodiode [90].

Fig. 6.70 Frequency response of low-offset CMOS DVD OEIC [90]

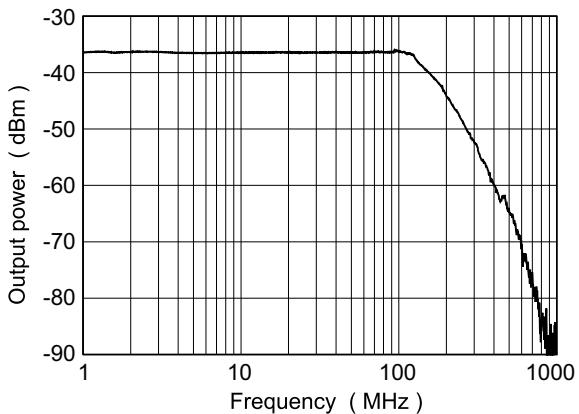
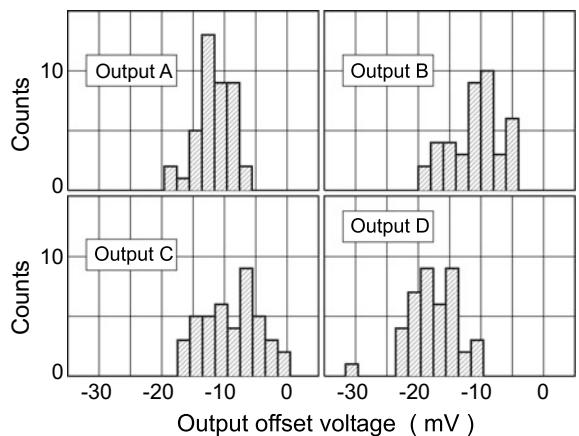


Fig. 6.71 Distribution of output offset voltage in low-offset CMOS DVD OEIC [90]



The results of the DC output offset voltage measurements are shown in Fig. 6.71. A number of 42 chips was measured along 2 rows across a whole wafer. The mean values of the output offset voltages of the outputs 1 to 4 are: -11.47 , -11.02 , -9.07 and -17.41 mV [90]. The associated standard deviations are: 3.19 , 4.12 , 4.51 , and 3.55 mV. The mean value of the offset voltages of all 168 channels shown in Fig. 6.71 is -12.24 mV, the standard deviation is 4.04 mV [90]. Though the standard deviation is less than the calculated value of 5.486 mV, the mean values are definitely deviating from 0 V for the output offset voltage. The source of these aberrations could be traced back. Because of the rather high supply currents (Table 6.2), voltage drops along the ground conductors appear, which cause voltage differences between the transimpedance amplifiers and their associated replica TIAs [90]. In a redesign this drawback can be avoided by a proper designed layout.

The OEIC presented in [90], nevertheless, featured an outstanding figure of merit $FOM = 287 \text{ MHz}/\mu\text{W}$. Other OS OEICs achieved figure of merits from $32.9 \text{ MHz}/\mu\text{W}$ [94] to $83.5 \text{ MHz}/\mu\text{W}$ [91].

Three suggestions for improvement could be made [90]: First, the single-stage inverters (N1/P1, N4/P4) could be replaced by 3-stage inverters. The higher gain of this topology results in a higher bandwidth of the transimpedance amplifiers. Secondly, the simple method of shifting the DC level by the inverters N7/P7 and N8/P8 has an influence on the value of the transimpedance and therefore on the sensitivity of the OEIC. This effect can be minimized by level-shifting within the proposed 3-state inverter. Finally, it has to be mentioned, that an improved layout can minimize the output offset voltage.

An optical receiver for optical storage systems implemented in a low-cost $0.6\text{ }\mu\text{m}$ CMOS process was described. In a first attempt, a bandwidth of 147 MHz and a sensitivity of $23.9\text{ mV}/\mu\text{W}$ could be achieved. The output voltage offset deviation of 4.04 mV was smaller than the calculated value. This OS OEIC achieved an outstanding figure of merit of $287\text{ MHz}/\mu\text{W}$ with a potential of improvement. It was shown that four independent receivers including the photodiodes and bondpads can be placed within a chip area of 0.51 mm^2 . A complete 8-channel DVD OEIC should therefore only occupy a total chip area of approximately 1 mm^2 [90].

6.4.12 BiCMOS Circuits for Optical Storage Systems

OEICs for optical storage (OS) systems with an enhanced data rate contain four fast channels (A–D) for data extraction and focus control plus four slower channels (E–H) for tracking control with a ten times larger sensitivity (Fig. 6.72).

No process modifications were necessary in the BiCMOS process implementing a double photodiode shown in Fig. 2.55 [102]. The schematic of one fast channel of an eight-channel OS-BiCMOS-OEIC is shown in Fig. 6.73 [102]. Polysilicon-polysilicon capacitors are available in the $0.8\text{ }\mu\text{m}$ BiCMOS process and a transimpedance amplifier is realized here. The gain is switchable between high (H), medium (M), and low (L). Only NPN transistors are used in the signal path and the resistor loads R1 and R2 are implemented in the difference amplifier in order to achieve a high -3 dB bandwidth. The value of 44 MHz was confirmed by measurements for the high gain [103]. The emitter follower Q5 reduces the output impedance of the operational amplifier.

The base currents of Q1 and Q2 in the input stage of the operational amplifier are approximately $5\text{ }\mu\text{A}$. Such a large input current of the operational amplifier, flowing through the transimpedance resistor R3, leads to a systematic output offset voltage of approximately 0.1 V , when no special measures are taken. These special measures are: The transistors Q3 and Q4 are used to sense the base currents of Q1 and Q2, respectively. The current mirrors M1/M2 and M3/M4 mirror the base currents of Q3 and Q4 into the bases of Q1 and Q2, respectively [104]. With this bias current cancellation, the output offset voltage could be reduced to less than 9 mV [102].

The frequency responses for the three different gain factors of the OS-BiCMOS-OEIC are shown in Fig. 6.74. The -3 dB bandwidth for the high gain is 44 MHz , for the medium gain it is 59 MHz , and for the low gain it is 64 MHz . The slightly

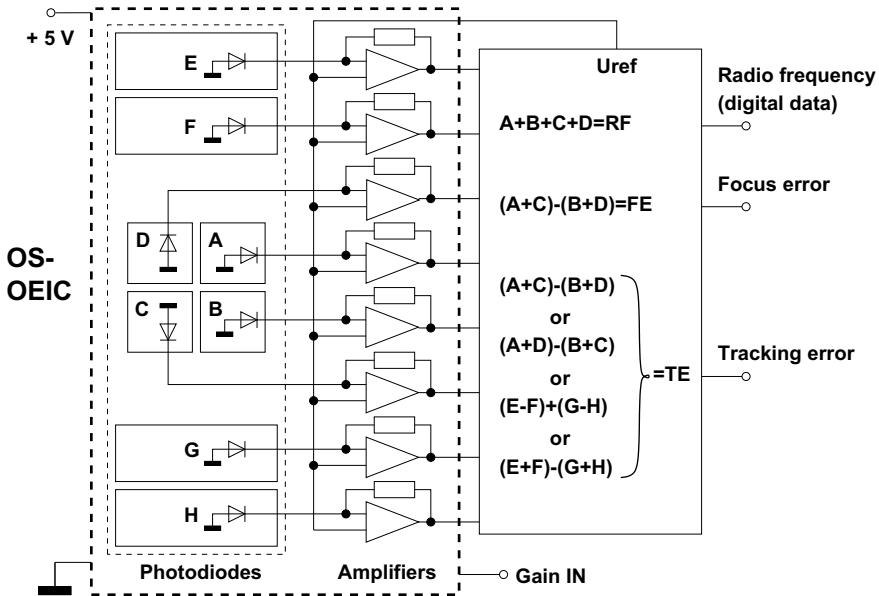


Fig. 6.72 Block diagram of an OS-BiCMOS-OEIC

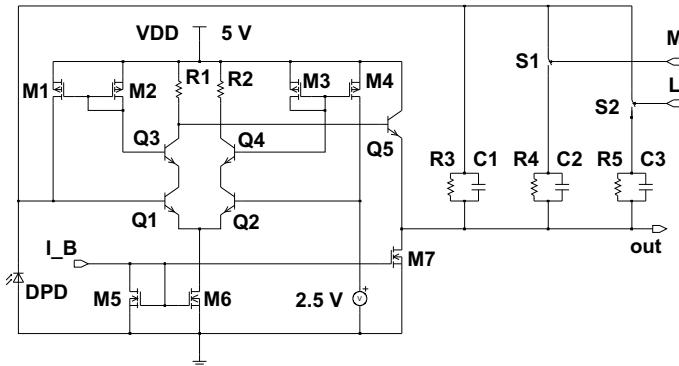


Fig. 6.73 Schematic of the fast channels A–D in an OS-BiCMOS-OEIC [102]

decreasing frequency responses between 1 and 40 MHz are due to parasitic capacitors in the amplifier and not due to slow carrier diffusion of photogenerated carriers in the double photodiode (DPD). The power consumption of the circuit in Fig. 6.73 is 7 mW at 5.0 V and with an antireflection coating a sensitivity of 10.5 mV/ μ W is achieved with the highest gain factor. The active die area of this circuit is 0.054 mm². An 8-channel OEIC with four of the above described fast amplifiers and four ten times more sensitive MOS amplifiers consumed a power of approximately 40 mW.

Fig. 6.74 Frequency response of an BiCMOS OEIC for optical storage systems for three different optical input powers, i.e. three different gain factors [102]

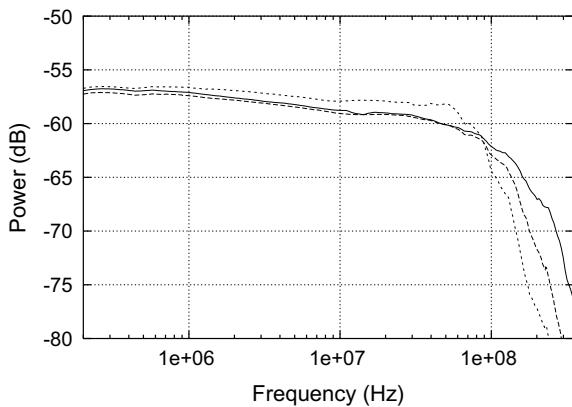
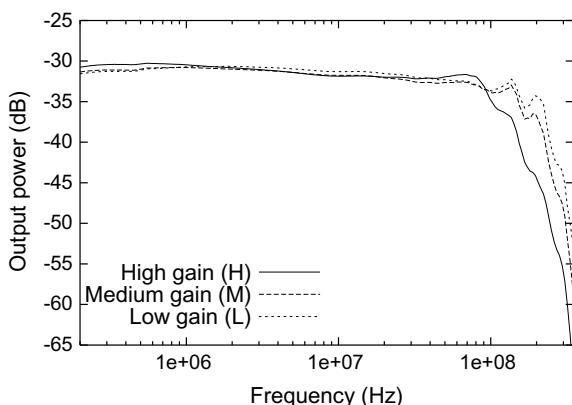


Fig. 6.75 Frequency responses of the fast channels A–D of a high-bandwidth BiCMOS OEIC for optical storage systems measured with three different optical input powers, i.e. three different gain factors [91]



At the expense of a higher power consumption, an even higher speed of OEICs for optical storage systems is possible [91]. A high-bandwidth BiCMOS OEIC has been demonstrated, which implemented fast amplifiers with the same schematic shown in Fig. 6.73 but with larger bias currents than in [102]. These fast amplifiers exhibit -3 dB bandwidths in excess of 90 MHz (Fig. 6.75).

An integrated double photodiode (Fig. 6.73) is connected to a transimpedance amplifier using an operational amplifier in order to obtain a low output offset voltage compared to a reference voltage of 2.5 V as is required for applications in optical storage systems. For a universal applicability, the gain is switchable by MOS elements between high (H, R3), medium (M, $R4 \parallel R3$) and low (L, $R5 \parallel R4 \parallel R3$) with a ratio of approximately 1/3 each. Polysilicon-polysilicon capacitors are used for frequency compensation with C1, C2, and C3. Here, the bias current cancellation of the input transistors Q1 and Q2 reduces the systematic output offset of approximately 110 mV, which would result from the base current of Q1 across the resistor $R3 \approx 20 \text{ k}\Omega$, to below 11 mV. According to simulations, the low-frequency open-loop gain of the operational amplifier is 27 dB and its transit frequency is 870 MHz in the case of a

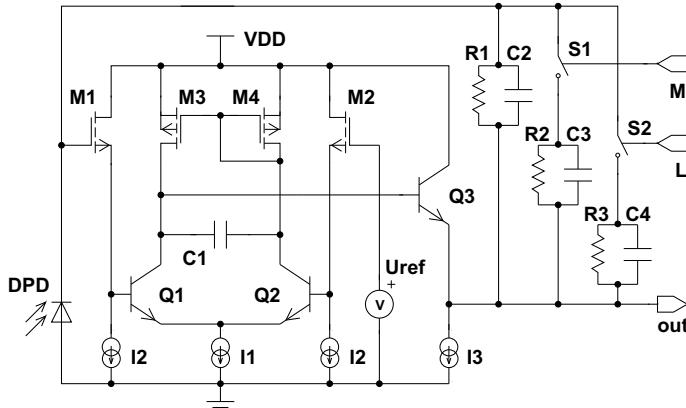


Fig. 6.76 Schematic of the sensitive channels E–H in a high-bandwidth OS-BiCMOS-OEIC [91]

load of $1\text{ k}\Omega$ and 10 pF . An OEIC was packaged, mounted together with these load elements on a printed circuit board, and the frequency responses were measured with a probe head having an input capacitance of 1.7 pF . The slight decrease in the frequency responses (Fig. 6.75) between about 5 and 80 MHz is due to parasitic capacitors in the amplifier and is not due to slow diffusion of photogenerated carriers in the DPD. The measured bandwidths exceed a value of 92 MHz. This value is much larger than the bandwidth of 7.3 MHz of the circuit for $8\times$ speed CD-ROMs fabricated in $0.8\text{ }\mu\text{m}$ CMOS technology with off-chip photodiodes [95].

Figure 6.76 shows the schematic of the four sensitive channels E–H with a ten times larger sensitivity for tracking control in the optical storage system. A double photodiode with approximately twice the size of the DPDs in the channels A–D is implemented in the channels E–H. The N-channel MOSFET source followers M1 and M2 are added in front of the bipolar difference amplifier Q1 and Q2 in order to avoid input currents and the resulting output offset voltages across the feedback resistors of about $200\text{ k}\Omega$. A high sensitivity of $100\text{ mV}/\mu\text{W}$ in combination with a low offset voltage can be realized in such a way. The PMOS load elements M3 and M4 are implemented for Q1 and Q2 in the difference amplifier in order to achieve a larger open-loop gain than with resistor load elements. The compensation is split between C1 and C2, C1 and C3, as well as C1 and C4. According to circuit simulations, the low-frequency open-loop gain of the circuit shown in Fig. 6.76 is 36 dB with a transit frequency of 130 MHz.

The frequency responses of the channels E–H are shown in Fig. 6.77. The values for the -3 dB bandwidths are listed in Table 6.3 together with other results.

Each amplifier in the channels A–H covers an active die area of about 0.079 mm^2 , and the total die area of the high-bandwidth BiCMOS OEIC amounts to 3.25 mm^2 . The power consumption of the high-bandwidth OS-BiCMOS-OEIC is less than 75 mW at 5.0 V. Table 6.3 summarizes further technical data of the fast and the sensitive channels of the high-bandwidth OS-BiCMOS-OEIC.

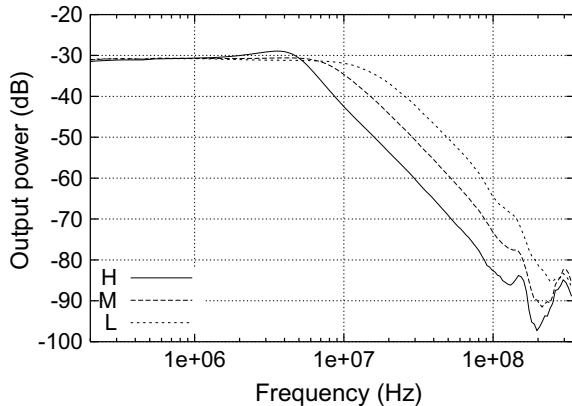


Fig. 6.77 Frequency responses of the sensitive channels E–H of a high-bandwidth BiCMOS OEIC for optical storage systems measured with three different optical input powers, i.e. three different gain factors

Table 6.3 Measured results of the high-bandwidth OS-BiCMOS-OEIC

	H	M	L
$f_{-3 \text{ dB}}$ (MHz) A–D	92.0	94.9	95.1
$f_{-3 \text{ dB}}$ (MHz) E–H	5.2	8.5	14.6
Sensitivity (mV/mW) A–D	8.8	2.9	0.9
Sensitivity (mV/mW) E–H	88.1	29.3	9.1
U_{Offset} (mV) A–D	<10.8	<9.5	<9.0
U_{Offset} (mV) E–H	<7.4	<6.4	<6.4
Noise (dBm) @ 10 MHz with 30 kHz RBW A–D	-81.5	-85.0	-85.2
Noise (dBm) E–H	-66.0	-67.5	-73.5

Figure 6.78 shows the microphotograph of the OS-BiCMOS-OEIC with bandwidths in excess of 90 MHz, which was realized in full custom design. The results demonstrate that it is possible to avoid the slow carrier diffusion problem by exploiting double photodiodes in standard BiCMOS technology.

A BiCMOS optoelectronic integrated circuit (OEIC) for optical storage systems containing photodiodes and transimpedance amplifiers with a reduced offset voltage is introduced next. A reference transimpedance amplifier and a low-offset operational amplifier are implemented for offset reduction. This technique can be called replica offset compensation.

Bipolar or BiCMOS operational amplifiers are necessary in order to obtain a high -3 dB frequency. Bipolar transistors in the input stage of such an amplifier, however, result in an input current in contrast to CMOS amplifiers. This input current flows across the feedback resistor and causes an output offset voltage in an operational transimpedance amplifier. A bias current cancellation technique has been applied

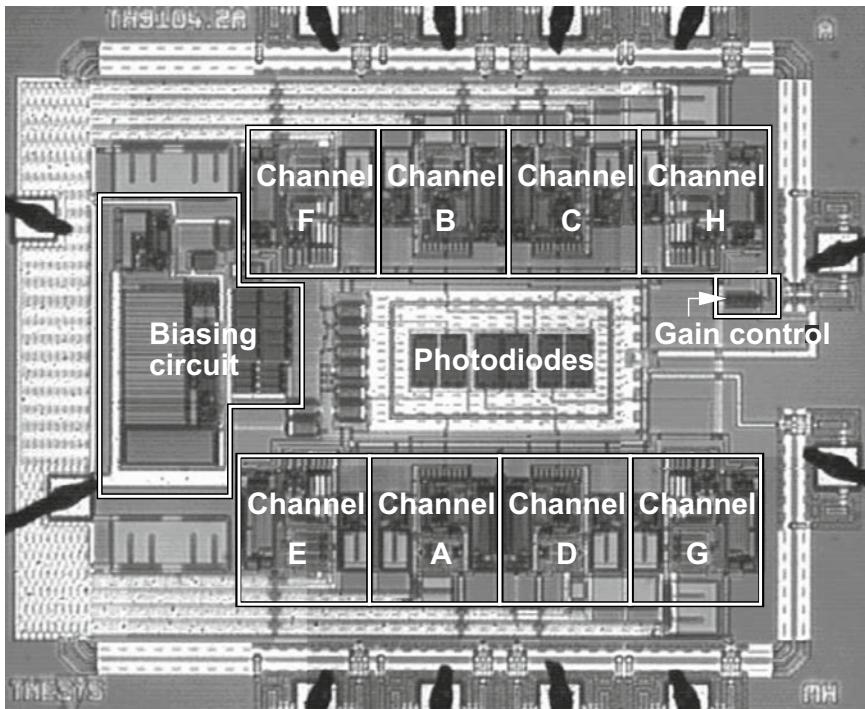
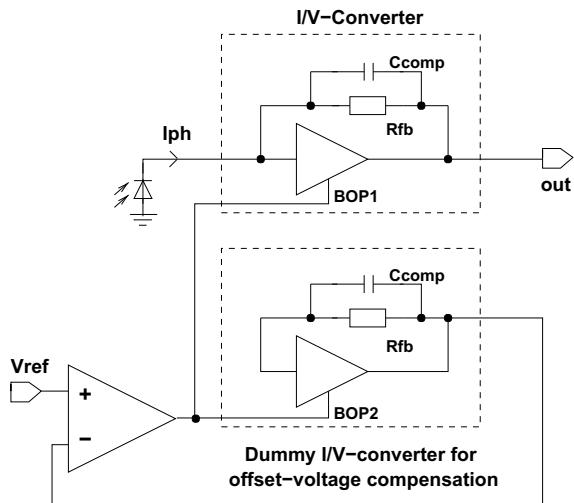


Fig. 6.78 Micrograph of a high-bandwidth BiCMOS DVD OEIC [91]

to reduce the output offset voltage from 100 to 9 mV in an OEIC with a sensitivity of $10.5 \text{ mV}/\mu\text{W}$ at 638 nm [102] and to below 11 mV as shown in the last example above. For a sensitivity of $25 \text{ mV}/\mu\text{W}$ the feedback resistor, however, has to be increased from about $24\text{--}60 \text{ k}\Omega$ leading to an increased output offset voltage when assuming the same input current of the operational amplifier. A circuit topology with a better performance implementing transistor transimpedance amplifiers instead of operational transimpedance amplifiers has, therefore, been investigated and will be shown here.

The innovative topology of an OEIC with an enhanced sensitivity for optical storage systems is shown in Fig. 6.79. This topology is called replica offset compensation. A current-to-voltage converter is connected to the integrated photodiode. The BOP1 (bias operating point) input allows to correct the operating point of this transimpedance amplifier in order to cancel the output offset voltage. For this purpose an identical dummy current-to-voltage converter with an open input and a low-offset operational amplifier are integrated together with the transimpedance amplifier connected to the photodiode. The operational amplifier measures the output offset voltage of the dummy I/V converter compared to $V_{\text{ref}} = 2.1 \text{ V}$ and changes its operating point via the BOP2 input in order to minimize the output offset voltage. The BOP1 input of

Fig. 6.79 Basic topology for output offset voltage reduction [92]



the actual transimpedance amplifier is also connected to the output of the operational amplifier. In such a way, the output offset voltage of the transimpedance amplifier can be reduced provided that a good matching between the two I/V converters and a low offset voltage of the operational amplifier can be guaranteed. The first requirement can be dealt with a careful layout reducing the distance between corresponding devices in the two I/V converters. The second requirement can be fulfilled, because the operational amplifier can be designed for a very slow response, i.e. transistors with a large emitter area or large gate lengths and widths for a good matching can be used. The replica offset compensation technique guarantees that the output voltage of the OEIC channels becomes independent of process tolerances — especially fast and slow cases — as well as independent of operating temperature.

An OEIC containing four fast channels (for data extraction) and four sensitive channels (for tracking control in the optical storage system) with larger R_{fb} values was fabricated in a $0.8 \mu\text{m}$ BiCMOS technology. The N-well/P-substrate photodiode (Fig. 2.61) with a light sensitive area of 2500 mm^2 was implemented in the fast channels. The same photodiodes with an area of 9100 mm^2 were used in the sensitive channels. The schematic diagram of the fast and sensitive channels of the BiCMOS OEIC is shown in Fig. 6.80. The transistor transimpedance amplifier is formed by the NPN transistor Q1 in common emitter configuration, the PMOS load element M1, the emitter follower Q3, and the feedback resistor R_{fb1} . The NPN transistor Q3 provides a low output impedance of this input stage. The capacitor C_{fb1} is used for compensation. The emitter follower Q11 decouples the feedback path from the output and provides a low overall output impedance. Q11 also leads to an output voltage close to the reference voltage. The dummy I/V converter is formed by Q2, M2, Q4, R_{fb2} , C_{fb2} , and Q12. Q5–Q10, R5–R10 and M3/M4 are used for biasing. The circuit

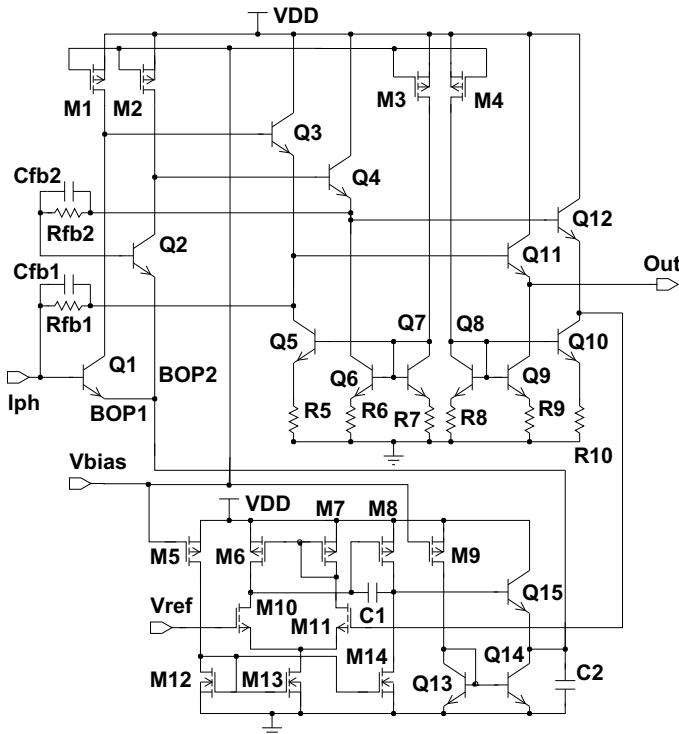


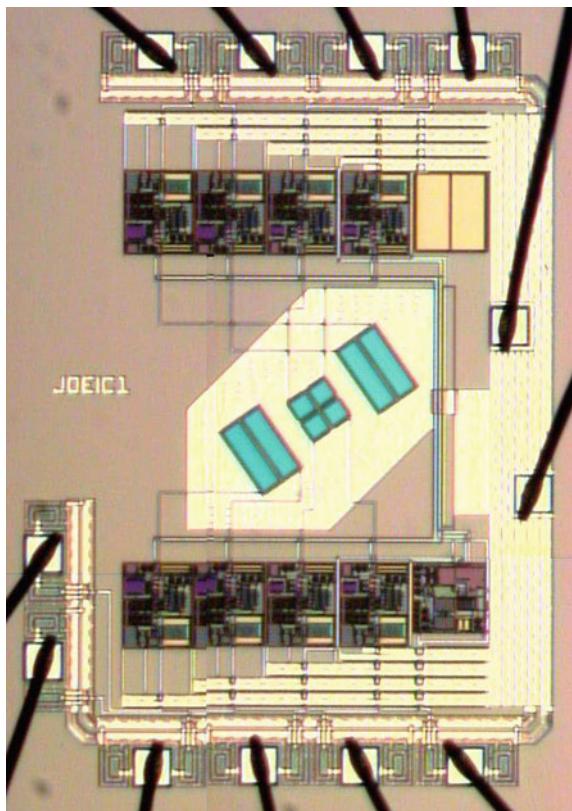
Fig. 6.80 Schematic diagram of one channel of the BiCMOS OEIC [92]

diagram in Fig. 6.80 corresponds to the interlaced layout for good matching of the two I/V converters.

The BiCMOS operational amplifier is based on a CMOS Miller type topology with the NPN emitter follower Q15 at the output in order to supply a voltage source with a low output resistance for the emitter inputs BOP of the two I/V converters. The simulated low-frequency differential gain of the operational amplifier is 77 dB and its transit frequency is 7.3 MHz. The chipfoto of an eight-channel DVD OEIC implementing the replica offset compensation is shown in Fig. 6.81.

For characterization, laser light with a wavelength $\lambda = 638$ nm was coupled into the photodiodes via a single-mode optical fiber adjusted on a wafer prober. A sensitivity for the fast channels of 25 and of $51\text{ mV}/\mu\text{W}$ for the sensitive channels at 638 nm was found [92] by determining the incident light power with a calibrated photodiode. A network analyzer HP8751A was used for laser modulation and for frequency response measurements. A -3 dB frequency of 58.5 MHz was measured for a fast channel A-D with a load of $10\text{ k}\Omega$ and 10 pF (Fig. 6.82). The sensitive channels E-H showed a -3 dB frequency of 26.7 MHz with the same load [92]. All measured output offset voltages for photodiodes and OEICs in the dark were lower than 7.5 mV [92]. This value is considerably lower than the maximum simulated off-

Fig. 6.81 Microphotograph of the BiCMOS OEIC implementing the replica offset compensation

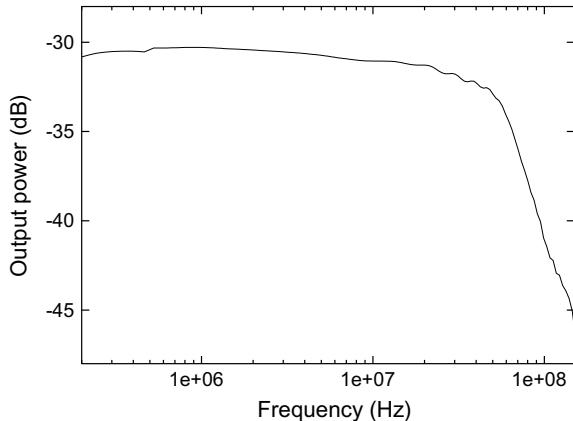


set voltage of a reference amplifier without offset compensation of more than 72 mV for worst case transistor parameters at room temperature [92].

It should be mentioned that the BiCMOS operational amplifier and the emitter BOP inputs reduce the bandwidth of the I/V converters. This is due to the output resistance of this operational amplifier. The output resistance of the BiCMOS operational amplifier, however, is obviously rather low, since the bandwidth of 58 MHz is not considerably lower than that of a reference I/V converter of 82 MHz where the emitter of Q1 was connected to V_{ref} directly [92].

The bandwidth of the N-well/P-substrate photodiode may seem to be rather high compared to [84] where a bandwidth of 1.6 MHz was reported for a similar photodiode for $\lambda = 780$ nm. The high bandwidth determined here, however, can be explained by the shorter wavelength and by an electric field, i.e. by a drift zone for photogenerated carriers, due to the doping gradient of the N-well similarly to that in the N-well of a double photodiode [105]. The external quantum efficiency of the N-well/P-substrate photodiode in the standard process for $\lambda = 638$ nm and a reverse bias of 2.5 V was 78% corresponding to a responsivity $R = 0.40 \text{ A/W}$. This value could be increased to 95% ($R = 0.49 \text{ A/W}$) by an antireflection coating layer.

Fig. 6.82 Frequency response of a fast channel of the BiCMOS OEIC implementing replica offset compensation [92]



Noise measurements at 10 MHz with a resolution bandwidth of 30 kHz revealed values of -76 and -65 dBm for the fast and sensitive channels, respectively. The power consumption determined by simulation was 36 mW for a fast channel at a supply voltage of 5.0 V. The active die area of each channel is approximately 0.042 mm^2 and the total chip area is 3.1 mm^2 .

The bandwidth-sensitivity product has been increased by factors of 1.8 and 3.2 compared to the circuits described in [91, 102], respectively. Additionally, the new offset compensation technique allowed a reduction of the output offset voltage from 11 mV [91] to below 7.5 mV.

A newer BiCMOS OEIC with enhanced sensitivity for advanced optical storage systems was presented [106]. The OEIC in an industrial $0.8\text{ }\mu\text{m}$ BiCMOS process showed a sensitivity of $43\text{ mV}/\mu\text{W}$ in combination with a -3 dB-bandwidth of 60 MHz.

A schematic overview of the high-sensitivity DVD-OEIC is shown in Fig. 6.83. It contains six channels, each consisting of an $\text{N}^+/\text{N-well}/\text{P-substrate}$ photodiode (Fig. 2.61) and a transimpedance amplifier.

The four photodiodes A–D for the fast channels cover an area of $75 \times 75\text{ }\mu\text{m}^2$ each, and the two larger photodiodes for the sensitive channels have an area of $190 \times 250\text{ }\mu\text{m}^2$. To reduce the chip area and the power consumption, two channels are combined with a dummy amplifier for output voltage regulation, each.

Figure 6.84 shows the circuit diagram of the amplifier. The circuit mainly consists of two transimpedance preamplifiers for current/voltage conversion, a free running transimpedance amplifier without a photodiode and an operational amplifier for output voltage compensation. Two current sources provide the currents needed to adjust the operating points of the transimpedance amplifiers and the operational amplifier. The upper and the lower transimpedance preamplifiers convert the photocurrents of the $\text{N}^+/\text{N-well}/\text{P-substrate}$ photodiodes A and B to corresponding voltages whereas the preamplifier in the middle is needed in order to refer the output voltage of the transimpedance amplifiers to the reference voltage U_{ref} . Without the dummy amplifier in

Fig. 6.83 Structure of the 6-channel OEIC for DVD [106]

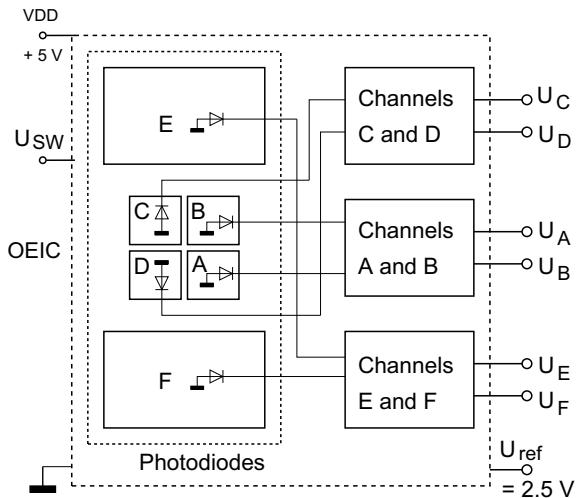
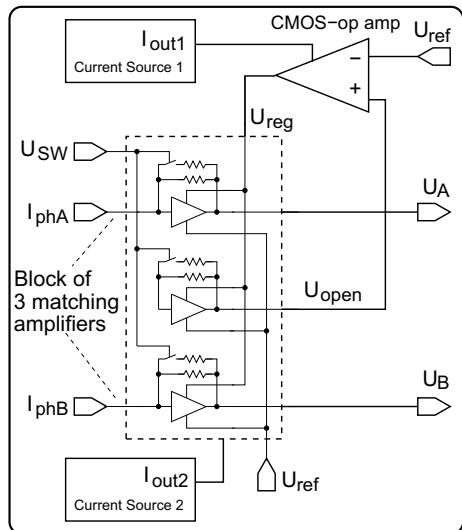


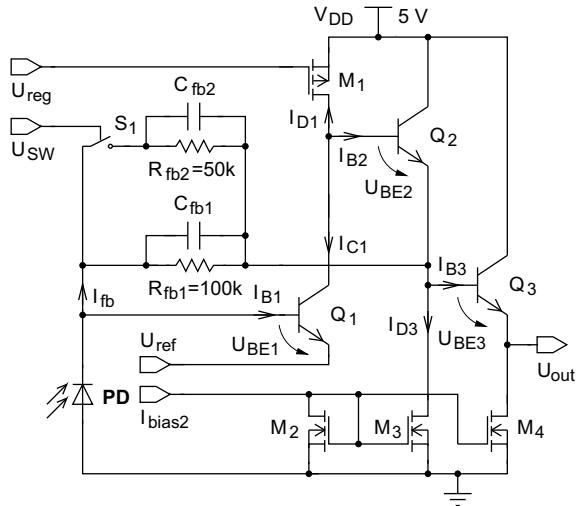
Fig. 6.84 Block diagram of two channels of the high-sensitivity DVD-OEIC [106]



the middle, the base current of the NPN transistor Q_1 would cause an output offset voltage of about 0.3 V referred to U_{ref} when no light incidents into the photodiodes.

This offset voltage is reduced as follows: When the output voltage of the dummy amplifier, which is applied to the non-inverting input of the operational amplifier, is lower than the reference voltage U_{ref} , the output voltage U_{reg} has a low value. Since M_1 is a P-channel-MOSFET (Fig. 6.85), its gate-source voltage increases, and at the same time the voltage at the base of Q_2 increases. The consequence is that the output voltage of the transimpedance amplifiers becomes higher. Steady state is achieved when the voltages at the inverting and at the non-inverting inputs of the operational

Fig. 6.85 Detailed circuit diagram of the transimpedance amplifier [106]



amplifier are equal. If good matching between the dummy amplifier and the other transimpedance amplifiers can be obtained and the operational amplifier has a low offset voltage, the offset voltage of the active channels can be minimised.

A detailed circuit diagram of the transimpedance amplifier for the fast channels can be seen in Fig. 6.85. The gain is switchable between high and low in order to detect two different photocurrents for read and write access. Again only NPN transistors are used in the signal path in order to obtain a high bandwidth. For the input stage the active load M_1 is applied.

A relation between the photocurrent and the output voltage can easily be found if the base currents are neglected. The voltage at the base of Q_1 is $U_{\text{ref}} + U_{\text{BE}1}$. A voltage of $I_{\text{ph}} \times R_{\text{fb}}$ is added, and the voltage $U_{\text{BE}3}$ at the output emitter follower is subtracted. If we assume that the base-emitter voltages of Q_1 and Q_3 are equal, we obtain the relation

$$U_{\text{out}} = U_{\text{ref}} + I_{\text{ph}} R_{\text{fb}}. \quad (6.59)$$

In a more detailed analysis, the base currents of the bipolar transistors have to be taken into account. This reveals a more complex DC transfer function which depends on numerous parameters of the transistors. Many of these parameters are subject to tolerances in the BiCMOS process making it difficult to design low-offset amplifiers without any control measures. Temperature changes within the operating temperature range also change the output voltage for constant or zero light levels.

Varying the drain current of PMOS load transistor M_1 has an impact on the DC transfer function and thus on the output voltage. Therefore the replica offset compensation scheme is applied to compensate the output voltage of the transimpedance amplifier with respect to the output voltage at dark photo current.

The main difference between the fast and the sensitive transimpedance amplifiers is the value of the resistors in the feedback path. In the fast channels feedback resistors of $R_{fb1} = 100 \text{ k}\Omega$ and $R_{fb2} = 50 \text{ k}\Omega$ are implemented. At high gain the sensitivity S^{high} of the amplifier can be calculated as

$$S^{\text{high}} = \frac{I_{\text{ph}} R_{fb1}}{P_{\text{opt}}} \eta_{\text{tia}} = \frac{R_{fb1} q \eta \lambda}{h c_0} \eta_{\text{tia}} \approx 48 \frac{\text{mV}}{\text{mW}}, \quad (6.60)$$

and at low gain a value of

$$S^{\text{low}} = \frac{R_{fb1} || R_{fb2} q \eta \lambda}{h c_0} \eta_{\text{tia}} \approx 15.9 \frac{\text{mV}}{\text{mW}} \quad (6.61)$$

is obtained, where $\eta_{\text{tia}} = r_{DS,M1}\beta / (r_{DS,M1}\beta + R_{fb})$ [107] is the conversion efficiency of the transimpedance amplifier with a value of 98% for $R_{fb1} = 100 \text{ k}\Omega$. In the case of the sensitive channels R_{fb1} is $150 \text{ k}\Omega$ and R_{fb2} is $70 \text{ k}\Omega$. This leads to sensitivities of $S^{\text{high}} = 72 \text{ mV/mW}$ and $S^{\text{low}} = 22.9 \text{ mV/mW}$.

Using (5.27) and (5.28) comparatively low values for the feedback capacitances of $C_{fb1} = 15 \text{ fF}$ and $C_{fb2} = 10 \text{ fF}$ were determined. A numerical circuit simulation considering the parasitic capacitances of the feedback resistors revealed that without these compensation capacitors a gain peaking in the frequency response curve would be visible [106]. For the sensitive channels lower values of the feedback capacitances could have been implemented according to (5.27) and (5.28). Instead, for additional compensation i.e. a larger phase margin even higher values of $C_{fb1} = C_{fb2} = 25 \text{ fF}$ were chosen. The bandwidth is with 20 MHz still much higher than required for these channels.

The performance of the circuit was characterized on wafer level by the following experimental setup: red laser light with a wavelength of 638.3 nm was coupled into the photodiode via a single-mode optical fiber adjusted on a wafer prober. To measure the bandwidth, a network analyser was chosen, which modulated the laser driver and evaluated the electrical output signal of the OEIC picked up by a picoprobe. The picoprobe was characterised by an input impedance of $10 \text{ M}\Omega$, an input capacitance of 100 fF and a -3 dB -bandwidth of 3 GHz.

For the fast channels of the OEIC a bandwidth of $f_{-3 \text{ dB}}^{\text{high}} = 60 \text{ MHz}$ at high gain and $f_{-3 \text{ dB}}^{\text{low}} = 61.6 \text{ MHz}$ at low gain were measured (Fig. 6.86), which were in good agreement with the simulated bandwidths [106].

The measured sensitivity of the fast and the sensitive channels at high gain was 43 and 60 mV/mW , respectively. This means that the fast channels are by a factor of 1.7 more sensitive than the OEIC described in [92] whereby the bandwidth is the same. The circuits can thus be applied in DVD systems with a lower laser power. The measured values for the sensitivity are lower than the calculated values which was lead back to process deviations for the polysilicon resistors. The measured results are summarised in Table 6.4.

Figure 6.87 shows a microphotograph of the six-channel OEIC with outside dimensions of $1333 \times 1595 \text{ mm}^2$. In the upper row the pads for the supply and

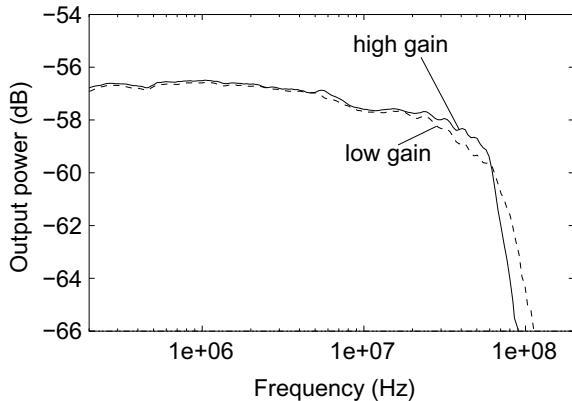


Fig. 6.86 Frequency response of fast channel [106]

Table 6.4 Measured results of high-sensitivity OEIC for $\lambda = 638.3$ nm. The noise values refer to a frequency of 10 MHz and a resolution bandwidth of 30 kHz [106]

	Offset (mV)	Sensitivity (mV/mW)	Noise (dBm)
A, Low Gain	17.8	15.3	-84.6
A, High Gain	8.4	43.3	-84.3
F, Low Gain	-12.7	20.7	-82.6
F, High Gain	8.2	60.4	-80.5

the reference voltage can be seen. The three pads T1, T2 and M on the left side are used for switching off selective channels for test purposes before packaging. The SW-pad in the lower row is needed for gain switching. All other pads are used for the output signals of the six transimpedance amplifiers, which are located in groups of two each on the chip. The photodiodes are surrounded by a metal shield which prevents penetration of laser light into the silicon substrate outside the light sensitive areas of the photodiodes.

Summarizing and concluding, a high-sensitivity BiCMOS OEIC with bandwidths of more than 60 MHz has been realized. The bandwidth-sensitivity product has been increased by a factor of 1.7 compared to [92]. With a dummy channel for two read channels in the replica offset compensation scheme, the chip area was reduced from 3.1 to 2.1 mm^2 by a factor of almost 1.5. The $\text{N}^+/\text{N-well}/\text{P-substrate}$ photodiode in conjunction with a BiCMOS amplifier is a good choice for high-speed, high-sensitivity and low-cost applications such as CD-ROM or DVD.

When a higher speed and a high sensitivity are required in addition to a low output offset voltage for the OS-OEICs, a two-stage optical receiver may be necessary. The circuit principle of such a two-stage amplifier [98] is shown in Fig. 6.88. The

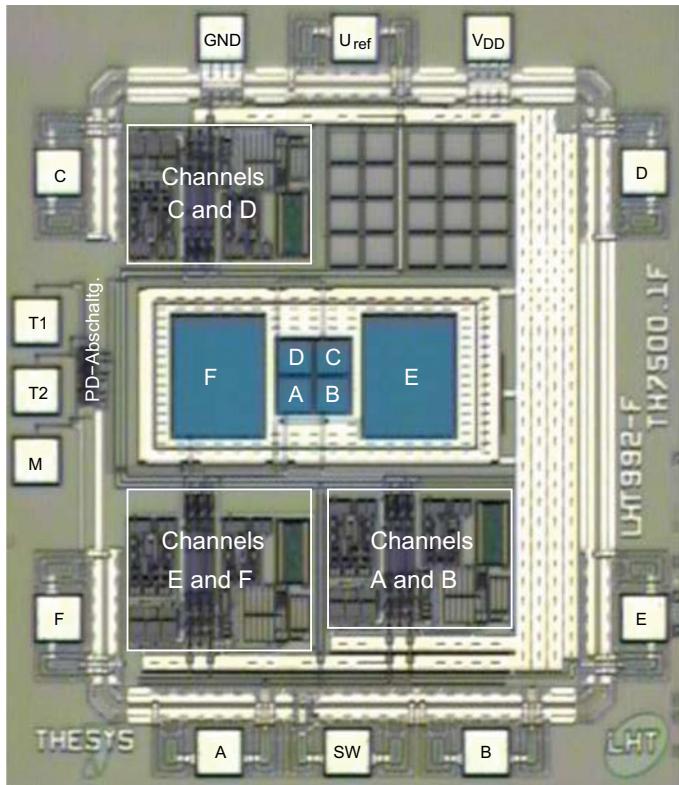


Fig. 6.87 Microphotograph of the high-sensitivity OEIC

circuit consists of a transimpedance amplifier for the photocurrent and a reference I/U converter for offset compensation plus an operational amplifier in subtractor configuration. The subtractor can be used simultaneously as a voltage amplifier with the amplification factor RS_2/RS_1 enabling a high overall sensitivity of the OEIC. It must be mentioned, however, that offset voltages due to mismatch of the two transimpedance input amplifiers and due to mismatch in the operational amplifier are also amplified.

The circuit diagram of the complete circuit is shown in Fig. 6.89. In order to achieve a high bandwidth, only NPN transistors are used in the signal paths of the preamplifiers. Q1 is used in common-emitter configuration, Q3 is used as emitter follower, and the feedback resistor R_{fb1} together with Q1 and Q3 represent a low input impedance for the photocurrent of the double photodiode (DPD). Thereby, the effect of the DPD capacitance is minimized. The reference voltage V_{ref} is chosen as the emitter potential of Q1 in order to increase the reverse voltage of the DPD to $V_{BE,Q1} + V_{ref}$. The values for R_1 , R_{fb1} , and C_{fb1} were $3\text{k}\Omega$, $27\text{k}\Omega$, and 25fF , respectively. A second emitter follower (Q11) is implemented for level shifting and decoupling of

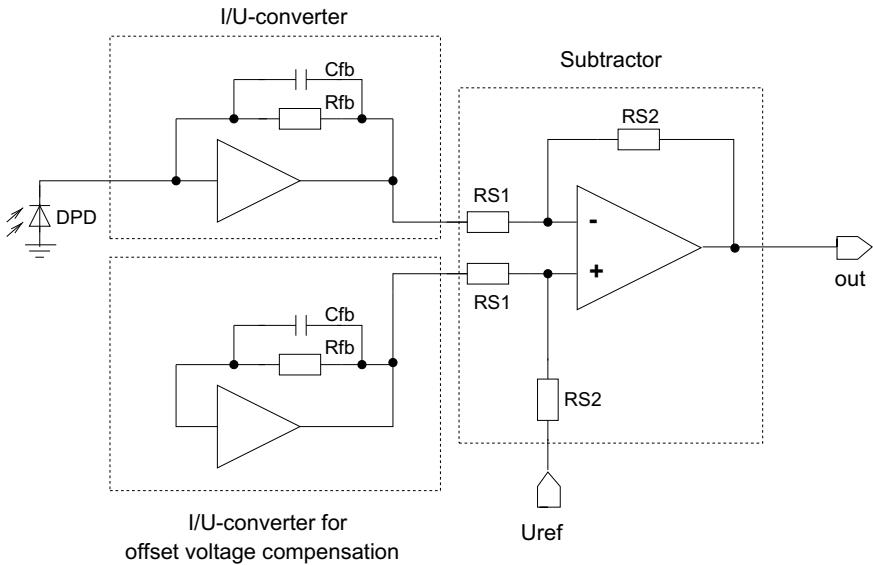


Fig. 6.88 Block diagram of a two-stage optical receiver for one fast channel of a high-speed OS-BiCMOS-OEIC

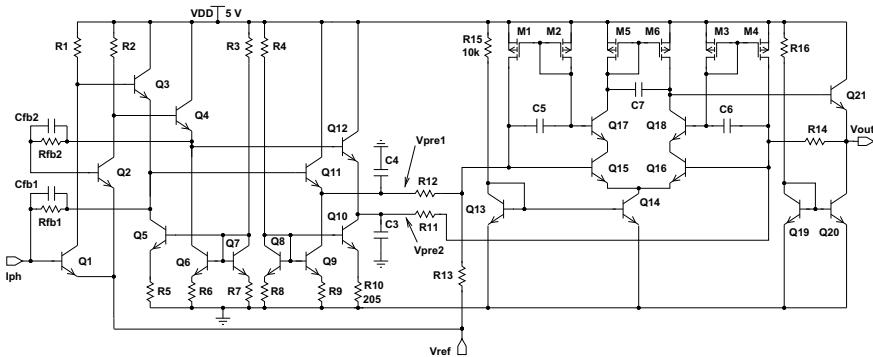


Fig. 6.89 Schematic of high-speed BiCMOS-OEIC for the fast channels A–D in an OS-BiCMOS-OEIC [99]

output and feedback path. The second preamplifier consists of transistors Q2, Q4, and Q12 as well as the current mirror with Q6 and Q7 and the feedback resistor R_{fb1} plus the compensation capacitor C_{fb2} . At the outputs of the preamplifiers, C3 and C4 are added as further compensation capacitors.

The large signal DC transfer functions of the preamplifiers are given by

$$V_{pre1} = V_{ref} + \eta_{tia} I_{ph} R_{fb1} + I_{B,Q1} R_{fb1}, \quad (6.62)$$

and

$$V_{\text{pre}2} = V_{\text{ref}} + I_{B,Q2}R_{\text{fb}2}, \quad (6.63)$$

when we assume $U_{\text{BE},Q1} = U_{\text{BE},Q11}$ and $U_{\text{BE},Q2} = U_{\text{BE},Q12}$. The efficiency factor η_{tia} of the preamplifier is given by $\eta_{\text{tia}} = R_1\beta/(R_{\text{fb}1} + R_1\beta)$. For $\beta = 100$ and for the resistor values given above the efficiency factor η_{tia} of the transimpedance preamplifier is equal to 0.917. The base current of Q1 (and Q2) causes a voltage of about 0.1 V across $R_{\text{fb}1}$ (and $R_{\text{fb}2}$). In order to achieve a low output offset voltage compared to V_{ref} , therefore, the second preamplifier without a photodiode and the subtractor operational amplifier are necessary. Perfect matching of the two preamplifiers ($I_{B,Q1} = I_{B,Q2}$, $R_{\text{fb}1} = R_{\text{fb}2}$, $R_1 = R_2$, $\beta_1 = \beta_2$, $U_{\text{BE},Q3} = U_{\text{BE},Q4}$, $U_{\text{BE},Q11} = U_{\text{BE},Q12}$) is, however, necessary in order to obtain $V_{\text{pre}1} = V_{\text{pre}2}$ for a dark photodiode. This perfect matching of the two preamplifiers requires a careful layout to achieve a low output offset voltage.

The preamplifiers are connected to the subtractor operational amplifier via R5 and R6. The bias current cancellation introduced in Fig. 6.73 is applied to reduce the input currents of the operational amplifier necessary for a low output offset voltage. A PMOS current mirror load with M5 and M6 is used here in order to obtain a higher open loop gain of the operational amplifier. For $R_{11} = R_{12}$ and $R_{13} = R_{14}$, an analysis of the subtractor amplifier yields the transfer function

$$V_{\text{out}} = V_{\text{ref}} + \frac{R_{13}A_{\text{d}}(s)}{(R_{12} + R_{13}) + R_{12}A_{\text{d}}(s)}(V_{\text{pre}1} - V_{\text{pre}2}) \quad (6.64)$$

and

$$V_{\text{out}} \approx V_{\text{ref}} + \frac{R_{13}}{R_{12}}\eta_{\text{tia}}I_{\text{ph}}R_{\text{fb}1}, \quad (6.65)$$

when we assume a large open loop voltage gain $A_{\text{d}}(s)$ of the operational amplifier. A -3 dB frequency of 189 MHz was determined by numerical prelayout simulation for the complete amplifier with a load of $R_L = 1\text{k}\Omega$ and $C_L = 10\text{ pF}$. The complete two-stage amplifier was designed for a sensitivity of $10\text{ mV}/\mu\text{W}$ and an offset voltage of less than 10 mV for $R_{11} = R_{12} = R_{13} = R_{14}$.

The OEIC with the DPD and the two-stage amplifier was fabricated in a $0.8\text{ }\mu\text{m}$ BiCMOS technology. The measured frequency response of this two-stage optical receiver is shown in Fig. 6.90. A -3 dB frequency of 147.7 MHz is determined from this frequency response. The power consumption of the two-stage optical receiver is 35 mW at a supply voltage of 5 V. The active die area of the two-stage optical receiver is $340 \times 140\text{ }\mu\text{m}^2$.

An even faster OEIC for optical storage systems has been presented recently. A bandwidth of 250 MHz has been achieved with a four-stage current amplifier in a standard $0.6\text{ }\mu\text{m}$ BiCMOS technology with fast vertical PNP transistors [93]. This OEIC can be used for channel data rates up to 600 Mb/s corresponding to 22X DVD with 12,000 RPM. The photodiode shown in Fig. 2.62 was optimized to a low capacitance of 0.25 pF . Nevertheless, the high bandwidth is an astonishing result

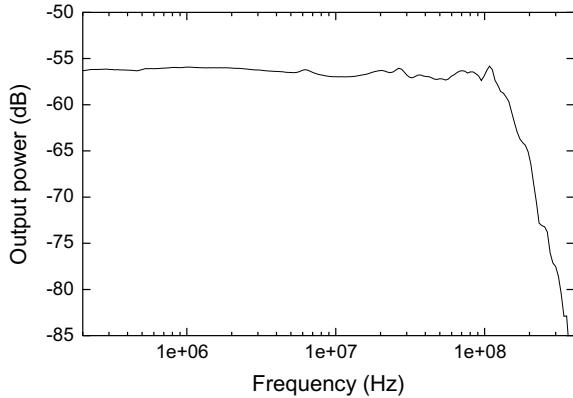


Fig. 6.90 Frequency response of a two-stage optical BiCMOS receiver for the fast channels A–D of a high-speed BiCMOS OEIC for optical storage systems [99]

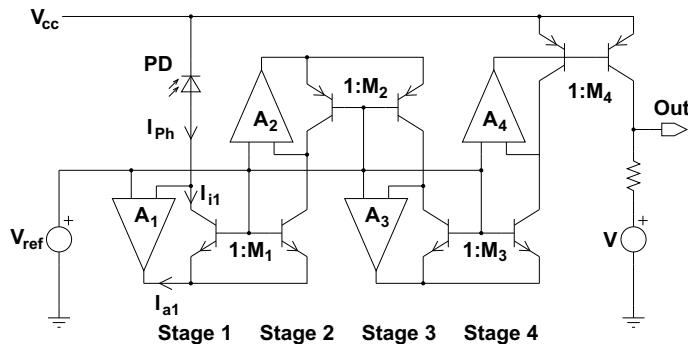


Fig. 6.91 Circuit topology of one segment in the fast OEIC for optical storage systems [93]

when we consider that no bias currents were superimposed to the photocurrents to reduce the offset of the amplifiers. Lowest power consumption, therefore, also could be achieved.

Figure 6.91 shows the topology of the current preamplifier used in the 8-channel OEIC. Since the gain-bandwidth product of the BiCMOS process is 400 GHz and a gain over 1,000 was needed, a four-stage amplifier with a bandwidth of at least 400 MHz for each stage was necessary [93]. The current amplifiers are no typical current mirrors. Instead the base-emitter voltage is the same of both transistors in each amplifier stage of which the second transistor actually is a parallel circuit of up to four transistors and the emitter currents are supplied by V/I amplifiers A1–A4. With MOS switches between and in the stages, the gain was switchable between 2 and 2048 for different laser powers during read and write as well as for different media according to the scheme illustrated in Fig. 6.92.

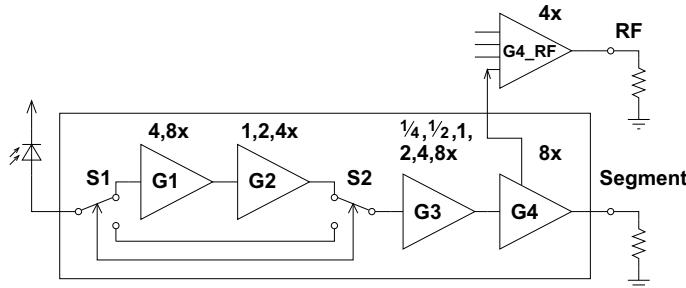


Fig. 6.92 Gain partitioning of one segment in the fast OEIC for optical storage systems [93]

A sum amplifier (RF amplifier) for the channels A–D was also implemented [93]. The bandwidth of this RF amplifier only weakly depended on the gain. The gain of the satellite amplifiers in channels E–H was always four times higher than shown in Fig. 6.92.

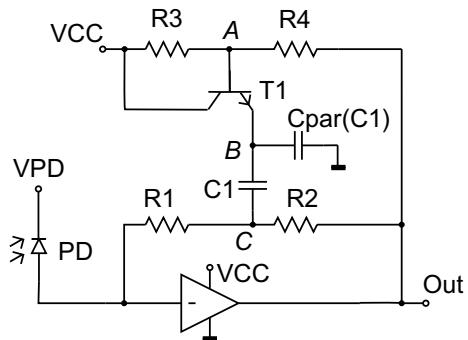
It has to be mentioned that a trick was necessary to achieve the high bandwidth for low photocurrents, since photocurrents of 100nA to $1\mu\text{A}$ cause the transit frequencies of the NPN transistors T1 and T2 to drop to tens of kHz to 1 MHz [93]. The large attenuation resulting at 400 MHz had to be eliminated. This was done by bypass capacitors which were not included in the circuit diagram shown in [93], however. The V/I amplifiers A1 to A4 used NMOS input transistors to avoid base input currents, their DC-current offset, and their base-current shot-noise.

Gain peaking around 200 MHz was caused by crosstalk between the output drivers and the first two stages [93]. It was stated that this problem can be solved in a redesign by separated front-end and back-end supplies. The output stage delivered a current of 8mA into a 150Ω load with a one-sigma offset value of $117\mu\text{V}$ [93].

A further improvement of OEICs for optical storage systems was introduced at ISSCC 2004. The so-called capacitive coupled voltage divider (CCVD) feedback allows to increase the feedback resistor value of TIAs considerably and thereby to avoid further amplifier stages, to reduce the offset voltage and the power consumption [108]. The integrated polysilicon resistor with an intended value of $200\text{k}\Omega$ caused a bandwidth limitation to 67.5 MHz (see also Sect. 11.4 in [109]) due to the parasitic capacitance of the polysilicon resistor towards substrate. If we assume a resistor having one third of this resistor value, i. e. $66.6\text{k}\Omega$, the bandwidth increases by a factor of nine. This behavior is taken advantage of by the CCVD approach. Figure 6.93 shows a single-stage TIA with CCVD feedback.

In a first version the transistor T1 was not present, i.e. nodes A and C were connected directly by the capacitor C1. First, the operation of this circuit without T1 shall be explained. The feedback path is split into low- and high-frequency path. The voltage divider R1-R2 ($R_1 = 66.6\text{k}\Omega$, $R_2 = 133.3\text{k}\Omega$, low-frequency path) and the voltage divider R3-R4 ($R_3 = 1.33\text{k}\Omega$, $R_4 = 2.66\text{k}\Omega$, high-frequency path) are connected by the capacitor C1 ($C_1 = 0.55\text{pF}$, T1 shall not be present). At low frequencies the impedance of C1 is large and the TIA's total transimpedance is $R_1 + R_2$. The

Fig. 6.93 TIA with CCVD feedback network [108]



ac signal at node A is one third of the TIA's output signal. At high frequencies, C1 has a low impedance and node C is forced to the same ac signal as being present at node A. The TIA's transimpedance is therefore three times R1, i.e. $200\text{ k}\Omega$. This first version showed a bandwidth of 265 MHz [110] due to the parasitic capacitance of C1 towards substrate (Cpar(C1)). With the improved version (transistor T1 included to drive the parasitic capacitance of C1) as shown in Fig. 6.93 the bandwidth was extended to 378 MHz, whereby due to process tolerances the transimpedance was $178\text{ k}\Omega$ [108] with $\text{VPD} = 5\text{ V}$. The observed bandwidth enhancement is smaller than the theoretical factor of nine due to the limited bandwidth of the amplifier. The corresponding transimpedance-bandwidth product was $67.3\text{ THz}\Omega$ for $\text{VPD} = 5\text{ V}$. For $\text{VPD} = 12\text{ V}$, the transimpedance-bandwidth product was $73.9\text{ THz}\Omega$ with a bandwidth of 415 MHz.

An even further improvement of single-stage TIAs was possible with the capacitive coupled distributed resistors (CCDR) feedback [111]. The same $0.5\text{ }\mu\text{m}$ BiCMOS process as in [108] was used. The pin photodiode of [112] shown in Fig. 2.63 was implemented. Compared to the CCVD approach, the two voltage dividers are arranged vertically, one on top of the other, and they couple capacitively without needing an extra coupling capacitor. The resistors and the coupling capacitor are distributed. The parasitic capacitance of the coupling capacitor is eliminated. Figure 6.94 shows the arrangement of the two resistors used in the feedback path of the TIA. The bottom resistor is realized by an n-well and the top resistor is realized as polysilicon resistor on field oxide above. Figure 6.95 shows the circuit diagram of the TIA with the CCDR feedback path.

If we can assume an ideal amplifier with infinite gain and bandwidth, the input node of the TIA represents a virtual ground. Then the polysilicon resistor and the resistor in the n-well are both connected from the output of the TIA to an ac ground. Consequently the electric field between the two resistors is constant and the capacitance between the two resistors does not have any effect. The resistance of the n-well should be small to observe a large improvement of the bandwidth of the CCDR over that of a simple polysilicon resistor. Therefore, the two n^+ regions at the boundaries of the n-well (see left part of Fig. 6.94) are implemented and the n-well was kept as narrow as possible to keep the n-well to substrate capacitance small.

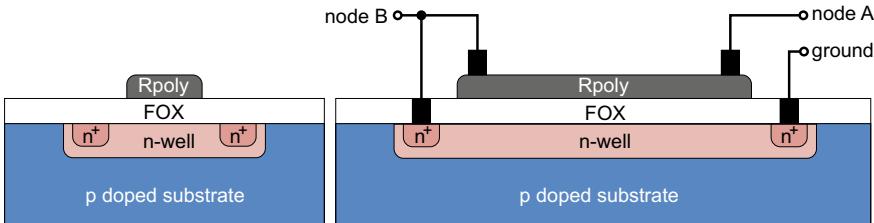
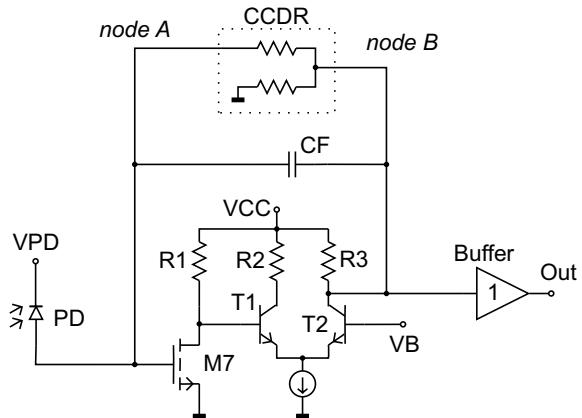


Fig. 6.94 Cross section (left) and longitudinal section (right) of CCDR [111]

Fig. 6.95 TIA circuit with CCDR [111]



An n-channel MOSFET in common-source configuration is used to obtain a high input resistance and a bipolar differential amplifier is exploited because of its high transconductance (see Fig. 6.95). The output buffer is only needed to drive the $50\ \Omega$ measurement equipment. For an ideal feedback resistor of $200\text{ k}\Omega$ a bandwidth of 716 MHz was calculated [111]. At 5 V, the power consumption of the CCDR TIA was 70.5 mW, of which 50 mW were dissipated by the output buffer. For 660 nm and 405 nm, -3 dB bandwidths of 615 MHz and 603 MHz, respectively, were measured. The transimpedance was $201\text{ k}\Omega$, leading to transimpedance-bandwidth products of $123\text{ THz}\Omega$ and $121\text{ THz}\Omega$, respectively. As an optical receiver, sensitivities for BER = 10^{-9} were -29.4 and -27.0 dBm at 1 and 1.25 Gbit/s, respectively.

6.4.13 Continuous-Mode Fiber Receivers

Optical multimode fibers for optical data transmission usually possess a core diameter of 50 or $62.5\ \mu\text{m}$. The core diameter of single-mode fibers for wavelengths shorter than $1.1\ \mu\text{m}$ actually is less than $10\ \mu\text{m}$. Small-area photodiodes therefore can be used in order to realize a low capacitance at the input of the receiver circuits. The bondpad capacitances of wire-bonded receivers are much larger than the

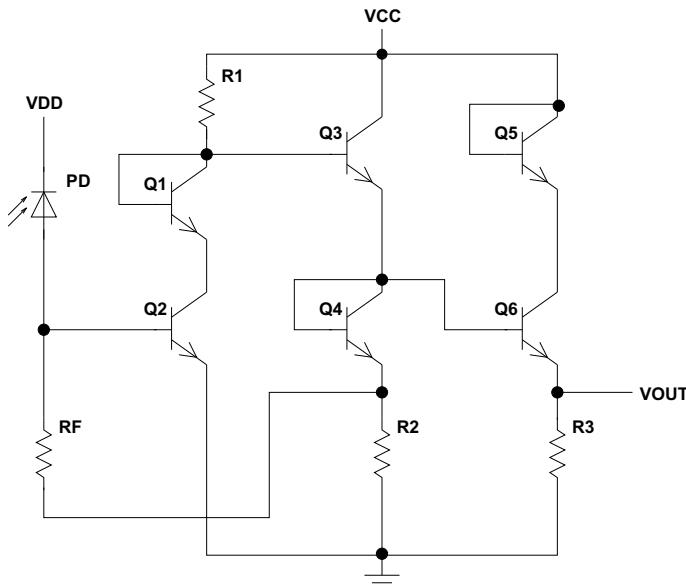


Fig. 6.96 Circuit diagram of a bipolar photoreceiver [113]

capacitance of PIN photodiodes. Monolithically integrated optical fiber receivers should be the first choice as a consequence. In the following, a bipolar OEIC as well as several NMOS OEICs, BiCMOS OEICs, and many CMOS OEICs for application as continuous-mode fiber receivers will be described.

Bipolar SiGe Receiver

The superior speed of SiGe HBTs compared to Si bipolar transistors has already been mentioned and the structure of a monolithic SiGe-Si PIN-HBT receiver was described in Chap. 4. Here, the bipolar transimpedance amplifier circuit of this receiver (see Fig. 6.96) will be discussed.

The receiver consists of a PIN photodiode, a common emitter gain stage, two emitter follower buffers, and a resistive feedback loop. NiCr thin-film resistors were used in the monolithic SiGe HBT receiver [113]. The transistors Q1, Q4, and Q5 are used as level shifting diodes. Q1 and Q5 reduce U_{CE} of Q2 and Q6, respectively, because the breakdown voltages of high-speed transistors are quite low.

The two voltage sources VDD and VCC were necessary to optimize the PIN transient behavior and the operating point of the amplifier. The value of the feedback resistor R_F determines the bandwidth, gain, and noise characteristics of the photoreceiver. The value of R_F is usually chosen based on a trade-off between these three parameters. In [113], a value of $640\ \Omega$ was chosen for R_F resulting in a transimpedance gain of $52.2\ \text{dB}\Omega$. The bandwidth of $1.6\ \text{GHz}$ was obtained for the transimpedance amplifier with a f_T of $25\ \text{GHz}$ for the HBTs with an emitter area of

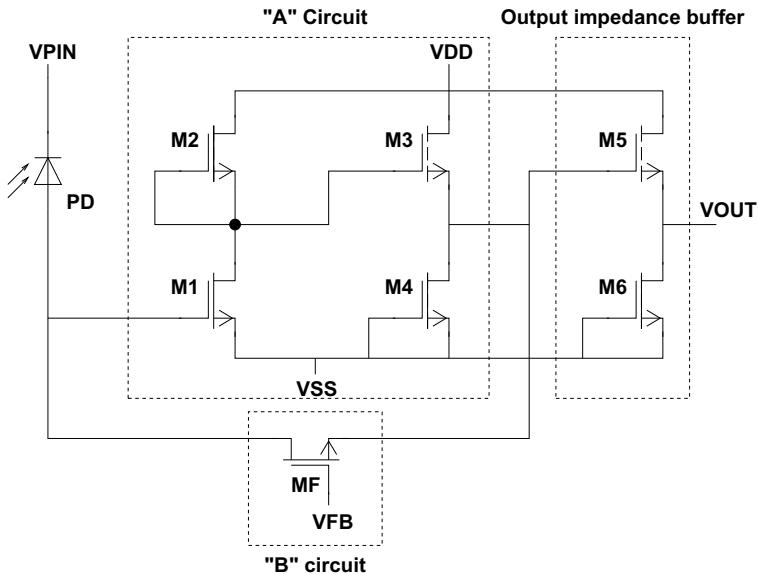


Fig. 6.97 Schematic of an NMOS fiber receiver OEIC [114]

$5 \times 5 \mu\text{m}$. The optical bandwidth of 460 MHz of the PIN-HBT receiver was measured for $\text{VDD} = 9 \text{ V}$ and $\text{VCC} = 6 \text{ V}$. The bandwidth of the receiver was limited by the photodiode and the trade-off mentioned above might be improved with respect to an increased gain, i.e. a larger sensitivity. An input noise spectral density of $8.2 \text{ pA}/\sqrt{\text{Hz}}$ up to 1 GHz caused by shot noise from the base current and thermal noise from the feedback resistor was given. With these values, the photoreceiver sensitivities of -24.3 and -22.8 dBm were estimated for 0.5 and 1 Gb/s, respectively, for a bit error rate (BER) of 10^{-9} and $\lambda = 850 \text{ nm}$.

NMOS Receivers

The next example is an NMOS OEIC. A lateral PIN photodiode was integrated in a $1.0 \mu\text{m}$ NMOS technology using a nominally undoped substrate, which was actually P-type with $N_A = 6 \times 10^{12} \text{ cm}^{-3}$ [114, 115]. This lateral PIN photodiode is described in Sect. 2.2.6.

An NMOS transimpedance preamplifier (Fig. 6.97) implementing a depletion transistor at the input was integrated together with a lateral PIN photodiode (see Fig. 2.18). The second and third stages were formed by source followers. The source follower stage M3/M4 with M4 as a constant current source is used to establish the correct operating point across the feedback loop with MF as an active resistor. The source follower stage M5/M6 at the output was sized to match a 50Ω load impedance. Open-eye operation for bit-rates of up to 40 Mb/s with a photocurrent of $3 \mu\text{A}$ for $\lambda = 870 \text{ nm}$ and for a transimpedance of $3 \text{ k}\Omega$ was reported [114].

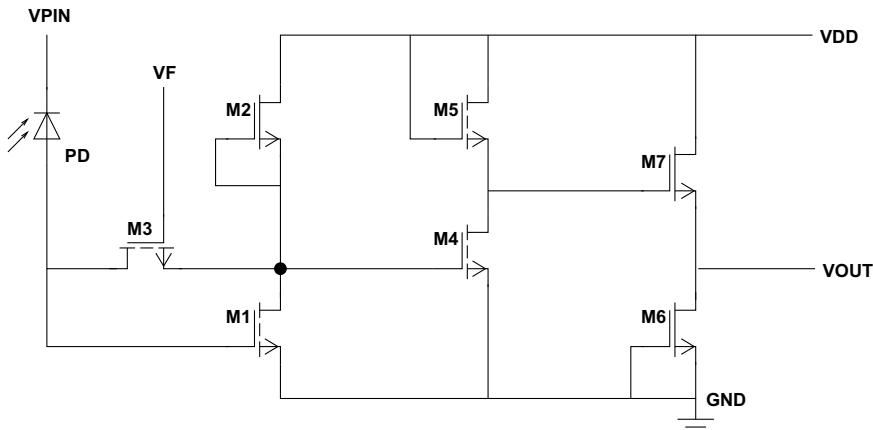


Fig. 6.98 Circuit diagram of an improved NMOS fiber receiver OEIC [116]

The authors of [114] later improved their photoreceiver [116]. An N-type Si substrate with a resistivity of 1000–3000 Ωcm was taken and an interdigitated lateral PIN structure with a finger width of $2\ \mu\text{m}$ and a finger spacing of $10\ \mu\text{m}$ instead of the ring structure (see Fig. 2.18) was implemented. The total area of the photodiode was $50 \times 50\ \mu\text{m}^2$. A dark current of $1.3\ \text{pA}$ at $5\ \text{V}$ and of $63\ \text{nA}$ at $30\ \text{V}$ was found. The quantum efficiency was increased to 84 and 74% at 800 and 870 nm, respectively, due to a SiO_2 antireflection coating with a thickness of 150 nm. A bit-rate of $500\ \text{Mb/s}$ was achieved from the interdigitated PIN photodiode at $30\ \text{V}$, however, its frequency response showed a diffusion tail below $100\ \text{MHz}$ [116].

The preamplifier has also been modified. Figure 6.98 shows the improved three-stage preamplifier. The feedback via M3 is only across the first stage with the common-source amplifier M1 and the depletion load M2. The second stage with the enhancement mode MOSFETs M4 and M5 further amplifies the signal and is used as a buffer to drive the depletion source follower M7 with an output impedance of $50\ \Omega$. At the optimum feedback, $V_F = 1.25\ \text{V}$, the transimpedance was $6.5\ \text{k}\Omega$ and a $45\ \mu\text{A}$ dynamic range of the photocurrent was obtained. The bandwidth of the photoreceiver was $130\ \text{MHz}$ for $870\ \text{nm}$ light, when biased with $V_{DD} = 8\ \text{V}$, $V_F = 1.25\ \text{V}$, and $V_{PIN} = 30\ \text{V}$. Open-eye operation under these conditions was demonstrated up to $300\ \text{Mb/s}$. The sensitivity of the photoreceiver was $-33\ \text{dBm}$ at $155\ \text{Mb/s}$ and $-25.5\ \text{dBm}$ at $300\ \text{Mb/s}$ at a bit error rate (BER) of 10^{-9} for a pseudo-random bit sequence (PRBS) of $2^{23} - 1$ under the same conditions. At a bias of $V_{DD} = 8\ \text{V}$, the power dissipation was $44\ \text{mW}$, with $2\ \text{mW}$ from the first two stages. A redesigned circuit [117] achieved sensitivities of -22.8 , -15 , and $-9.3\ \text{dBm}$ at bit rates of 622 , 900 , and $1000\ \text{Mb/s}$, respectively. This redesigned preamplifier had a bandwidth of $500\ \text{MHz}$ and dissipated only $10.8\ \text{mW}$ at a power supply voltage of $1.8\ \text{V}$. $V_{PIN} = 30\ \text{V}$, however, was still necessary for a $-3\ \text{dB}$ frequency of $150\ \text{MHz}$ and a $-6\ \text{dB}$ frequency of about $750\ \text{MHz}$ for the lateral PIN photodiode.

Newer results were presented for photoreceivers with the same circuit topology as in Fig. 6.98 on high resistivity and on SOI substrates [118]. With the lateral PIN photodiode on high-resistivity silicon a sensitivity of -23.2 dBm at a data rate of 1 Gb/s and a BER of 10^{-9} was achieved with a reverse bias of 30 V at the photodiode and a VDD of 3.5 V . The same sensitivity at a data rate of 622 Mb/s was reported with a photodiode reverse bias of 10 V .

With a lateral PIN photodiode in a $3.0 \mu\text{m}$ thick SOI layer of N-type and orientation (100) with a resistivity of $50\text{--}80 \Omega\text{cm}$ on a buried oxide with a thickness of $3 \mu\text{m}$ and an NMOS transimpedance amplifier with the circuit topology of Fig. 6.98 a sensitivity of -15.3 dBm at 622 Mb/s and at a BER of 10^{-9} was obtained for $\text{VDD} = 3 \text{ V}$ and $V_{\text{PIN}} = 3 \text{ V}$ with $\lambda = 850 \text{ nm}$ [118]. With higher supply voltages of $\text{VDD} = 5 \text{ V}$ and $V_{\text{PIN}} = 5 \text{ V}$ a sensitivity of -12.0 dBm at a data rate of 1.5 Gb/s was found. A sensitivity of -12.2 dBm finally was reported with $\text{VDD} = 5 \text{ V}$ and $V_{\text{PIN}} = 20 \text{ V}$ for a data rate of 2.0 Gb/s . These impressive results are due to the optimized SOI layer thickness allowing the suppression of the slow drift in the depth between the N^+ - and P^+ -fingers, which is present in the lateral PIN photodiode on high-resistivity bulk silicon.

It can be concluded that the approach of [116–118] results in a rather good performance of the photoreceiver at the cost, however, of a rather large supply voltage of up to 30 V for the lateral PIN photodiode. This voltage is usually not present in modern electronic systems and advanced microelectronic circuits, which operate at $5, 3.3, 2.5, 1.8 \text{ V}$ or even lower voltages.

BiCMOS Receivers

Results of BiCMOS-OEICs, consisting of a PIN photodiode and an amplifier, which exploited only MOSFETs and no bipolar transistors, have been published [119, 120]. The BiCMOS technology, therefore, was chosen merely for the integration of the PIN photodiode. A standard BiCMOS technology with a minimum effective channel length of $0.45 \mu\text{m}$ was used without any modifications [119, 120]. This effective channel length corresponds to a drawn or nominal channel length of about $0.6 \mu\text{m}$. The buried N^+ collector in Fig. 2.52 was used for the cathode of the PIN photodiode, the P^+ -source/drain island served for the anode, and the intrinsic zone of the PIN photodiode was formed by the N well (see Sect. 2.3).

The circuit diagram of the CMOS preamplifier used in the BiCMOS OEIC is shown in Fig. 6.99. The input stage of this amplifier with the NMOS transistors N1, N2, and N3 is a single-ended transimpedance amplifier featuring DC input coupling. The feedback resistor R3 had a value of $1.4 \text{ k}\Omega$. However, with the additional voltage gain of the following circuit elements, the effective transimpedance of the amplifier was about $3.0 \text{ k}\Omega$. The circuit with the transistors N5 and N6 produces a reference voltage for the gate of P5. This voltage is close to the midpoint of the voltage swing at the gate of P3 and can be considered as a kind of decision threshold. P3 and P5 are source followers, which are biased by the current sources P2 and P4, respectively. N4–N6 and P1–P5 perform a single-ended to differential conversion. N7 and N8

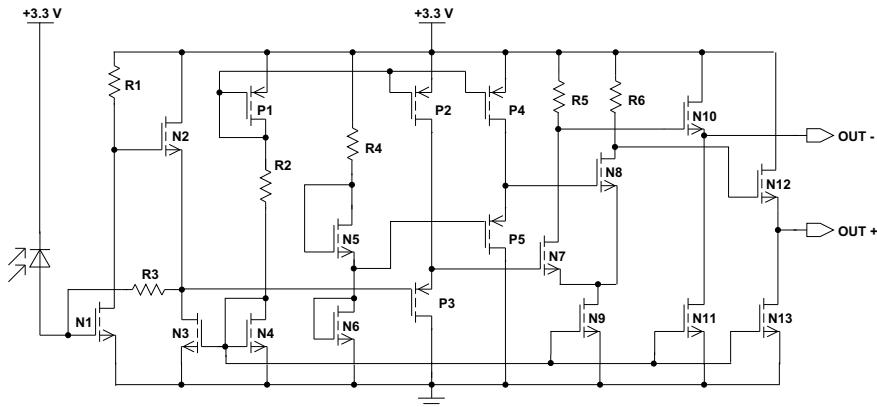


Fig. 6.99 Circuit diagram of an OEIC in BiCMOS technology with a buried N^+ collector as cathode of a PIN photodiode [119]

form a differential amplifier. N10–N13 are source-follower drivers with an output impedance of $50\ \Omega$.

The power dissipation of the core amplifier circuit was 30 mW from a 3.3 V supply, with an additional 57 mW in the output source followers. The -3 dB bandwidth of the receiver was 300 MHz . The OEIC reached a bit rate of 531 Mb/s with a bit error rate of 10^{-9} and a sensitivity of -14.8 dBm for $\lambda = 850\text{ nm}$.

In [120] a laser with a wavelength of 670 nm was used for the characterization of the same OEIC as in [119]. The data rate was increased to 622 Mb/s for this wavelength. This bit rate was limited by the capacitance of the photodiode and the feedback resistor of $1.4\text{ k}\Omega$ in the amplifier transimpedance input stage.

Another BiCMOS fiber receiver OEIC has been described containing a double photodiode (Fig. 2.55) and a bipolar preamplifier (Fig. 6.100). This OEIC has been fabricated in a $0.8\text{ }\mu\text{m}$ BiCMOS technology.

The transistor Q1 is used in common-emitter configuration. Together with the emitter follower Q2 and the feedback resistor R_{fb} , Q1 forms a transimpedance input stage. The emitter follower Q4 is used for level shifting and for decoupling the feedback loop from the output. A reference voltage V_{REF} of 2.5 V has been applied to the emitter of Q1 resulting in a reverse bias of about 3.3 V for the double photodiode lying between the input and ground.

The transient response of a double photodiode with an area of $530\text{ }\mu\text{m}^2$ shown in Fig. 2.59 has been measured with this amplifier. A bandwidth of 367 MHz has been determined for the OEIC. Wide-open eye patterns with a turn-on delay of 0.2 ns at a bit rate of 531 Mb/s for $\lambda = 638\text{ nm}$ (Fig. 6.101) were obtained with this BiCMOS OEIC containing a double photodiode with an area of $530\text{ }\mu\text{m}^2$ in a standard technology without any modifications [121].

A low-noise monolithically integrated 1.5 Gb/s optical receiver in $0.6\text{ }\mu\text{m}$ BiCMOS technology with a PIN photodiode similar to that described in [86] was pre-

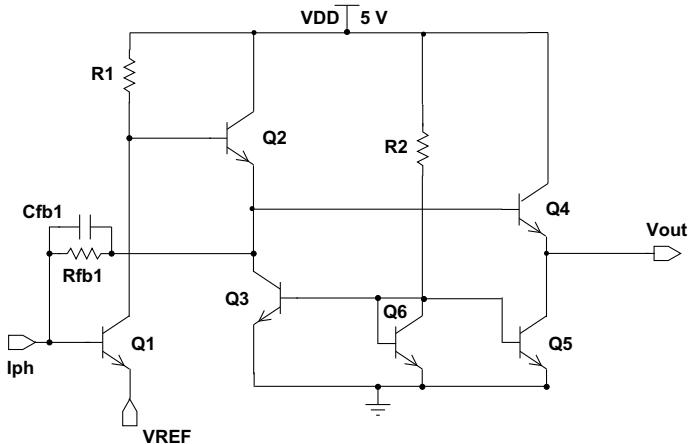
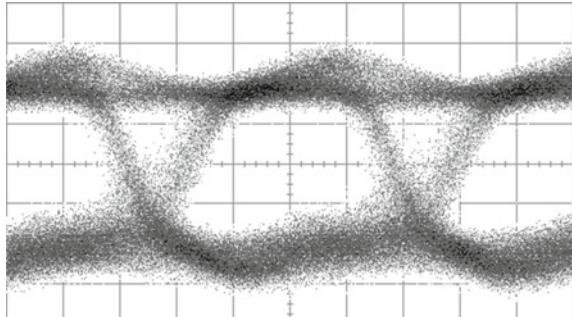


Fig. 6.100 Schematic of fiber receiver OEIC fabricated in BiCMOS technology [121]

Fig. 6.101 Eye diagram of a BiCMOS fiber receiver OEIC recorded at 531 Mb/s with a PRBS word length of $2^{23} - 1$ (time scale: 400 ps/div.; amplitude: 100 mV/div.) [121]



sented recently [122]. It can be used in optical interconnects and in short-range data transmission via optical fibers in local area networks and for fiber-in-the-home. Optical interconnects may offer a solution for the increased bandwidth demands in communication within electronic systems e.g. between electronic boards via optical backplanes or via free space. High-bandwidth and high-sensitivity optical receivers are especially necessary when many star couplers or many beam splitters are implemented in the optical transfer path. The same demands hold for free space optical interconnects when the emitted optical power is spread over a large area to reach many receivers. Optical free-space data transmission between different computers, printers, scanners and so on within larger rooms also requires sensitive receivers. Low-cost, high-reliability, and high-performance photo receivers are needed to support the growth of optical interconnects.

A possibility to speed up integrated photodiodes is to use a second higher supply voltage for the photodiode to increase the electric field, i.e. the drift velocity. A second supply voltage of 24 V was also necessary for lateral PIN photodiodes on SOI [118, 123]. Due to the thickness of the SOI layer of 2 μm the photodiode's quantum

efficiency, however, was small at 850 nm. In [124] –26.2, –20.3, and –12 dBm at data rates of 622 Mb/s, 1 Gb/s, and 2 Gb/s, respectively, for the receiver in [123] were given for a pseudo-random-bit-sequence (PRBS) of $2^7 - 1$. Below an OEIC in 0.6 μm BiCMOS technology [122] will be described, which achieves a sensitivity of –23.9 dBm at a single 5 V supply and –24.3 dBm at $\text{VCC} = 5 \text{ V}$ and $\text{VPD} = 17 \text{ V}$ both at a data rate of 1 Gb/s and a PRBS of $2^{31} - 1$.

In [122] a vertical PIN photodiode suggested in [86] with a large I-layer thickness was implemented leading to a quantum efficiency of 74% at a wavelength of 670 nm and 50% at 850 nm. This photodiode uses a P-type substrate. The cathode is formed by an N^+ region on which a low-doped N^- epitaxial layer is grown. A deep P-type region is implemented to reconstruct the P-type substrate doping concentration in the circuit regions of the OEIC [86]. This photodiode has the advantage that a reverse bias higher than the circuit supply voltage can be applied for a high drift speed.

The schematic of the amplifier implemented in the BiCMOS OEIC is shown in Fig. 6.102. The OEIC consists of a PIN photodiode followed by a transimpedance amplifier and two post amplifier stages. The PIN photodiode had a responsivity of 0.40 A/W at 670 nm and a capacitance of about 50 fF already at a reverse bias of 3 V. The diameter of this diode was 50 μm . To maintain low noise the first amplifier stage is a transimpedance amplifier with a feedback resistor of $R_1 = 3.2 \text{ k}\Omega$. Further amplification is obtained with two amplifier stages to enhance the signal amplitude and drive the bondpad and the load. This two-stage post amplifier had an overall gain of 20 dB and every stage had the same structure as the input stage to obtain low offset. In this application low offset was only necessary to ensure that the bias points of the amplifiers have the optimal values and that the output voltage range is not significantly limited by process variations.

An NMOS transistor (M1) instead of a NPN transistor was implemented at the input of the amplifier in order to achieve a larger output voltage range (about 1.3 V) compared to less than 0.8 V in case of an NPN transistor. The MOS transistors M1–M6 had the shortest possible gate length (0.6 μm) for highest bandwidth and maximum conductance. T1–T6 were bipolar transistors which have a transit frequency of about 25 GHz. Emitter followers were used instead of source followers to increase the bandwidth due to the lower output impedance. A second reason was, that gain reduction could be avoided which would have resulted due to the back-gate effect of the available NMOS transistors without a complimentary buried layer below the P well. T1, T3 and T5 were used as diodes to reduce the collector-emitter voltage of the emitter followers (T2, T4 and T6) to prevent breakdown.

The areas of the MOS- and bipolar transistors were exponentially expanded with progressive stages to obtain the same relative load for each stage and finally a low impedance output stage. This was done to have the possibility to drive low-impedance loads during measurement. This option, however, lead to a high supply current. For applications where the signal is processed internally on chip the output stage can be reduced in size and current consumption.

Figure 6.103 shows the resulting chip which occupies an area of approximately $870 \mu\text{m} \times 410 \mu\text{m}$. The photodiode together with its metal shield against light incidence outside of its light-sensitive area with a diameter of 50 μm has a size of

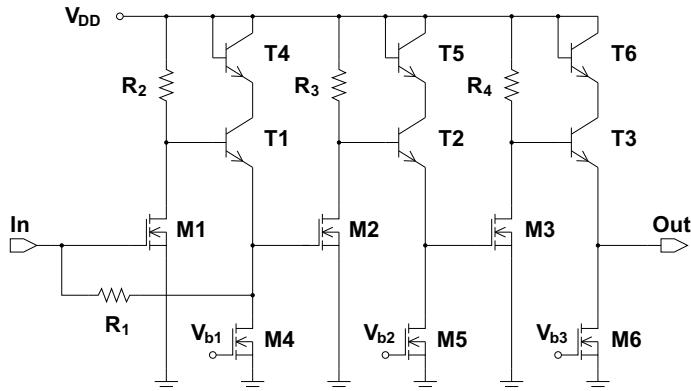
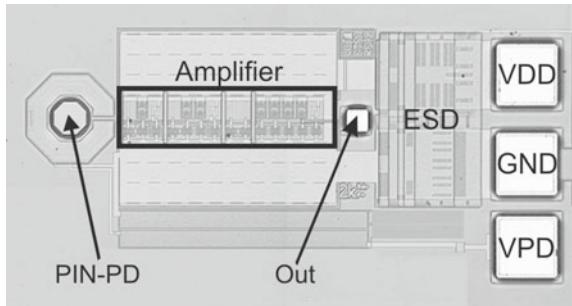


Fig. 6.102 Schematic of low-noise fiber receiver OEIC fabricated in $0.6\text{ }\mu\text{m}$ BiCMOS technology [122]

Fig. 6.103 Chipfoto of fiber low-noise receiver OEIC fabricated in $0.6\text{ }\mu\text{m}$ BiCMOS technology [122]



$140\text{ }\mu\text{m} \times 140\text{ }\mu\text{m}$. The light shield can be made smaller or omitted entirely. The active area of the amplifier, however, is only $80\text{ }\mu\text{m} \times 350\text{ }\mu\text{m}$ allowing easily a pitch of 125 or $150\text{ }\mu\text{m}$ in one dimension for massively parallel optical interconnects. The output pad is small compared to the supply pads to maintain a low capacitive load for the data signal.

For measurements, the OEIC was bonded on a printed circuit board (PCB) to minimize the stray inductance of the connection from the supply blocking capacitors to the chip [122]. The evaluation of the behavior of this OEIC was done under two load conditions. First the bandwidth and transient response were measured with a 3-GHz picoprobe on the output pad. The picoprobe loaded the OEIC output with 100 fF and $10\text{ M}\Omega$. The same measurements were done with an AC-coupled resistor divider connected directly to the $50\text{ }\Omega$ oscilloscope input. Therefore the output pad was connected with a bond wire to a PCB, where an external $220\text{ }\Omega$ resistor and a 100 nF capacitor were mounted. The output signal was lead to the oscilloscope via a $50\text{ }\Omega$ micro-strip line on the print, which resulted in a $220\text{ }\Omega - 50\text{ }\Omega$ voltage divider. This was done to overcome the problem of the noise from the picoprobe which degrades the receiver sensitivity significantly. The lower cutoff frequency of

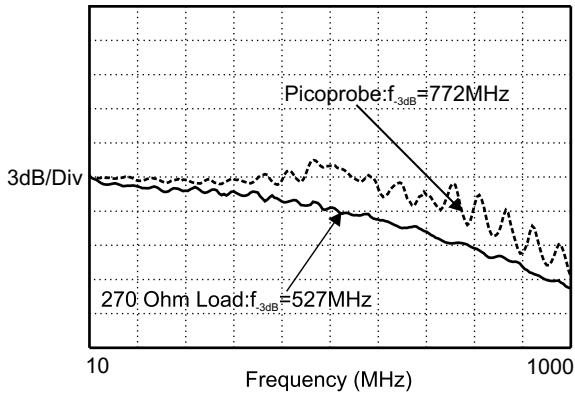


Fig. 6.104 Frequency response of low-noise fiber receiver OEIC fabricated in $0.6\text{ }\mu\text{m}$ BiCMOS technology under different load conditions with VPD = 17 V [122]

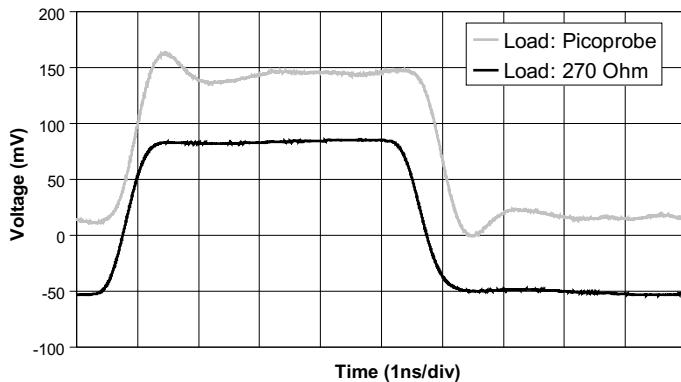


Fig. 6.105 Transient response of low-noise receiver OEIC fabricated in $0.6\text{ }\mu\text{m}$ BiCMOS technology for different loads with VPD = 17 V [122]

this capacitively coupled voltage divider was 6 kHz. The 220Ω resistor together with the characteristic impedance of our measurement system (50Ω) resulted in an overall load of 270Ω at the OEIC output. The bandwidth and rise time was slightly degraded due to this load, but the noise was only limited to thermal noise of the $220/50$ voltage divider, which was much lower than the picoprobe noise [122]. The results of the frequency responses with VPD = 17 V can be seen in Fig. 6.104. In Fig. 6.105 the transient behavior is shown for the two cases.

Table 6.5 shows the bandwidth dependence on photodiode bias voltage. With the supply voltage of the photodiode increased to 17 V, the bandwidth extends to 772 MHz. Table 6.6 lists the measured rise and fall times in dependence on the photodiode reverse voltage. With 17 V, rise and fall times of 0.46 and 0.48 ns, respectively, were achieved [122].

Table 6.5 Bandwidth of the OEIC in dependence on the photodiode bias voltage [122]

V_{PD} (V)	Load: $270\ \Omega$ (MHz)	Load: picoprobe (MHz)
5	442	658
7.5	487	723
10	489	765
12	518	769
15	519	770
17	527	772

Table 6.6 Rise and fall times of the OEIC in dependence on the photodiode bias voltage [122]

V_{PD} (V)	Load: $270\ \Omega$		Load: picoprobe	
	t_r (ps)	t_f (ps)	t_r (ps)	t_f (ps)
5	669	760	531	547
7.5	602	679	515	533
10	589	661	473	493
12	580	653	463	481
15	575	648	465	484
17	571	648	462	482

The OEIC consumed 31 mA of supply current at a supply voltage of 5 V which results in a power consumption of 155 mW. The DC-sensitivity of this OEIC was $13.7\text{mV}/\mu\text{W}$ at 670 nm which leads together with the responsivity of the photodiode to an effective transimpedance of $34.1\text{k}\Omega$. Together with a bandwidth of 772 MHz, a $26\text{THz}\Omega$ effective transimpedance-bandwidth product was obtained. This OEIC had a separate supply pad (VPD) for the cathode of the photodiode. The receiver, therefore, could be used either in a single 5 V environment at a reduced data rate of 1.25 Gb/s or the full data rate of 1.5 Gb/s could be achieved with 17 V at the cathode of the photodiode. All measurements were performed with a 670 nm laser diode modulated by a 2.5 Gb/s ECL pattern generator for the bit error measurements or via a bias-T by a HP8753E network analyzer for the frequency response measurements.

The sensitivity measurements for a BER of 10^{-9} were performed with a pseudo random bit sequence (PRBS) with a length of $2^{31}-1$. The eye diagram was observed with a Tektronix communication system analyzer CSA8000. Due to the noisy picoprobe, these measurements were taken with the $220/50\ \Omega$ resistor divider at the output. The results for different data rates and photodiode voltages are shown in Table 6.7. The result for a data rate of 1.5 Gb/s with a dual supply of 5 and 17 V was a sensitivity value of -22.1 dBm . For a single supply of 5 V and a data rate of 1.25 Gb/s at a sensitivity of -22.7 dBm was obtained. At a data rate of 1.0 Gb/s, the

Table 6.7 Summary of the sensitivity of the low-noise BiCMOS OEIC for a BER of 10^{-9} and a PRBS of $2^{31}-1$ [122]

Data rate (Mb/s)	Sensitivity at $V_{PD}=5\text{ V}$ (dBm)	Sensitivity at $V_{PD}=17\text{ V}$ [122] (dBm)
622	-24.5	-24.5
1000	-23.9	-24.3
1250	-22.7	-24.1
1500	-	-22.1

Table 6.8 Comparison of the sensitivity of the OEIC described in [123, 124] with the low-noise BiCMOS OEIC in [122] for a data rate of 1.0 Gb/s and $VDD=5\text{ V}$

	Sensitivity (dBm)	PRBS	V_{PD} (V)
1 μm NMOS on SOI [123, 124]	-20.2	2^7-1	20
1 μm NMOS on SOI [123, 124]	-18.7	$2^{23}-1$	20
1 μm NMOS on SOI [123, 124]	≈ -18	2^7-1	5
0.6 μm BiCMOS [122]	-24.3	$2^{31}-1$	17
0.6 μm BiCMOS [122]	-23.9	$2^{31}-1$	5

sensitivity at a single 5 V supply was -23.9 dBm which is slightly better than the value of -23.3 dBm reported in [118] with two supply voltages ($V_{PD}=30\text{ V}$ and $VDD=3.9\text{ V}$, see Table 6.14). Table 6.8 compares the results achieved in [122] with that reported in [123–125]. In [123] a PRBS of 2^7-1 was used and a penalty of 1.5 dB was mentioned for a PRBS of $2^{23}-1$ leading to a sensitivity of -18.7 dBm at 1 Gb/s compared to a value of -24.3 dBm for a PRBS of $2^{31}-1$ of the 0.6 μm PIN BiCMOS OEIC reported in [122]. For a photodiode bias of 5 V, a penalty of 2–4 dB was reported in [123] leading to a sensitivity of about -18 dBm , which compares to a value of -23.9 dBm of the 0.6 μm PIN BiCMOS OEIC reported in [122].

The measured incident optical powers reported in [122] were averaged values of a laser diode with an extinction ratio of 6.5. The results, therefore, can be corrected to values that are 1.3 dB lower, if a source with infinite extinction ratio is used. Further improved sensitivity at the lower bit rates can be achieved when filters limiting the bandwidth according to the desired data rate are applied between the output of the OEIC and the signal analyzer [122]. The results in Table 6.7 were measured without a filter. Figure 6.106 shows the eye diagrams at the data rates of 1.0 and 1.5 Gb/s at a bit error ratio (BER) of 10^{-9} with a photodiode bias of 17 V.

Figure 6.107 shows the dependence of the BER on the average optical input power for various data rates. Due to intersymbol interference (ISI), the sensitivity at 1.5 Gb/s is reduced by 2 dB. At 1.25 Gb/s a BER below 10^{-12} was verified. At 1.0 Gb/s a BER of 10^{-13} was achieved at an averaged incident optical power of -23.1 dBm [122].

It was shown that low noise and high data rates can be achieved with silicon PIN BiCMOS OEICs, which make them useful for application in optical interconnections.

Fig. 6.106 Eye diagrams of low-noise receiver OEIC fabricated in $0.6\text{ }\mu\text{m}$ BiCMOS technology with VPD = 17 V, $\lambda = 670\text{ nm}$, $2^{31}-1$ PRBS at a data rate of **a** 1 Gb/s with $P_{\text{in}} = -24.3\text{ dBm}$ (H: 200 ps/div, V: 20 mV/div) **b** 1.5 Gb/s with $P_{\text{in}} = -22.1\text{ dBm}$ (H: 100 ps/div, V: 20 mV/div) [122]

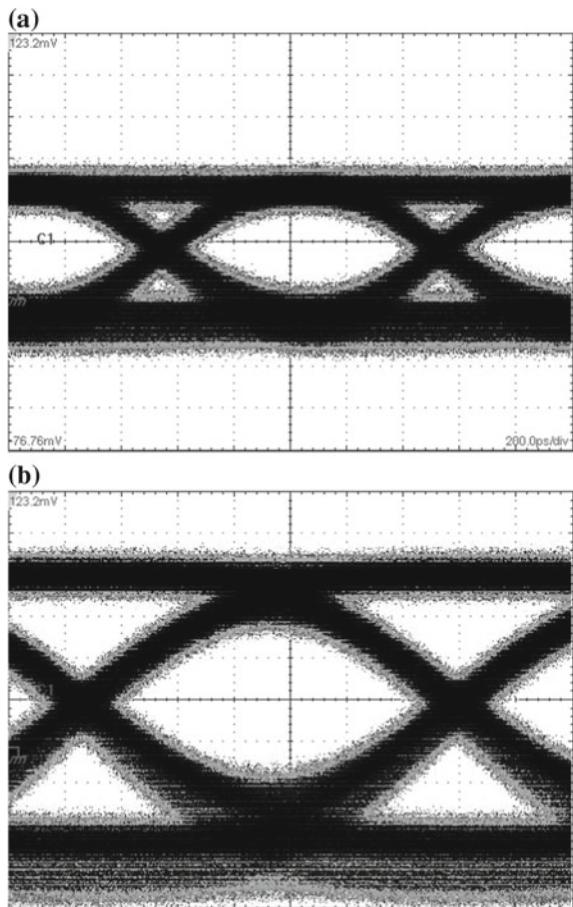
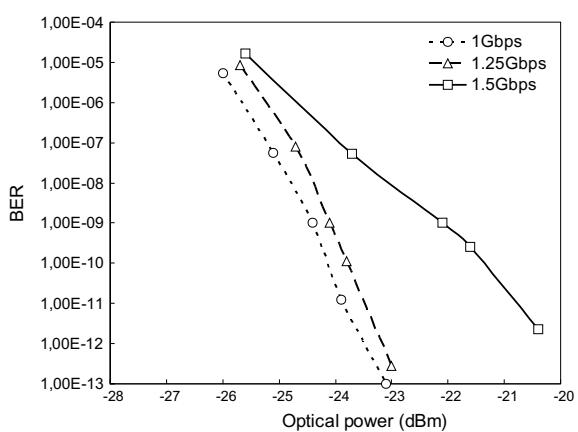


Fig. 6.107 BER of low-noise receiver OEIC fabricated in $0.6\text{ }\mu\text{m}$ BiCMOS technology with VPD = 17 V in dependence on the average optical input power at $\lambda = 670\text{ nm}$, $2^{31}-1$ PRBS, VPD = 17 V [122]



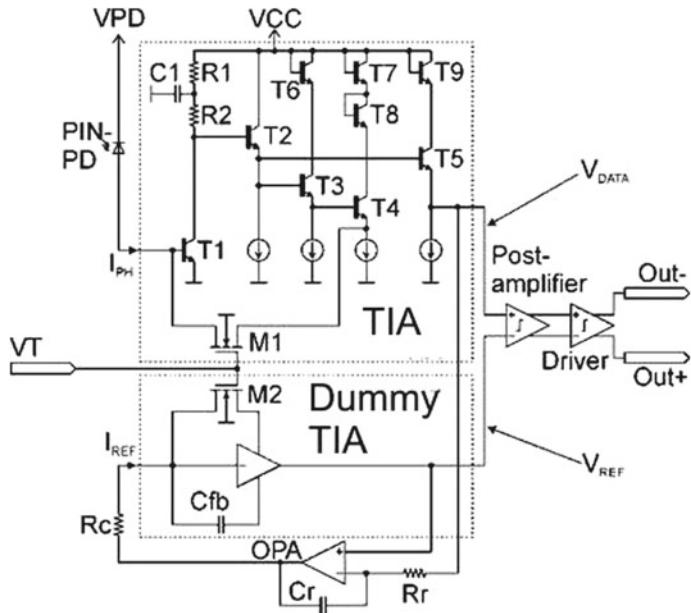


Fig. 6.108 Simplified circuit diagram of the receiver part of the OEIC with VUC fabricated in $0.5\text{ }\mu\text{m}$ BiCMOS technology

The low active area of photodiode and amplifier allow the application in massively parallel optical interconnects. The sensitivity, bandwidth and current consumption can be further optimized [122].

A 5 Gb/s receiver OEIC in modified $0.5\text{ }\mu\text{m}$ silicon BiCMOS using the pin photodiode of Fig. 2.63 [112] with a diameter of $50\text{ }\mu\text{m}$ was introduced in [126]. This OEIC used the electric-field enhancement technique (see also Sect. 6.4.17) by integrating a voltage-up-converter (VUC) to increase the bandwidth of the photodiode. The circuit of the receiver part is shown in Fig. 6.108. The TIA with T1 in common-emitter configuration and emitter followers T2 and T5 as well as active feedback resistor M1 converts the photocurrent I_{PH} to the signal voltage V_{DATA} . The dummy TIA with the proportional-integral (PI) controller (OPA, R_r , R_c , and C_r) generates the reference voltage V_{REF} , which is the averaged voltage of V_{DATA} , for the following post amplifier designed as symmetrical limiter. The diode-connected npn transistors T6–T9 reduce the collector-emitter voltages of T3–T5 to prevent breakdown [126].

The differential topology with TIA and dummy TIA suppresses power supply noise especially in the range of some megahertz, where the charge pump generates switching noise. The Miller capacitor C_{fb} of the dummy TIA limits its bandwidth and therefore its noise was negligible compared to that of the main TIA [126]. Due to the lower cut-off frequency of the PI controller of about 50 kHz ambient light was suppressed but data rates down to 155 Mb/s with PRBS31 could easily be received. The post-amplifier and 50Ω driver had a differential gain of 30 dB .

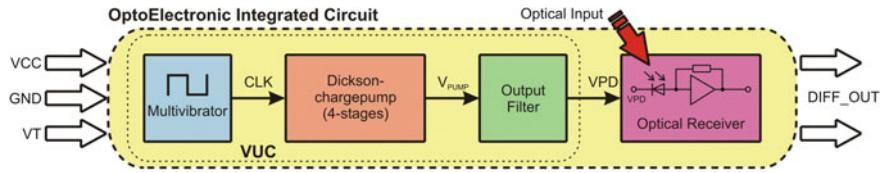


Fig. 6.109 On-chip generation for the photodiode bias VPD of the OEIC with VUC fabricated in $0.5\text{ }\mu\text{m}$ BiCMOS technology

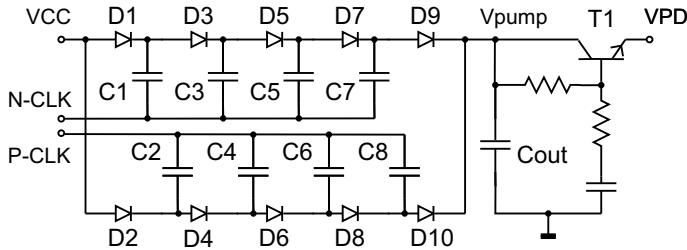


Fig. 6.110 Four-stage Dickson charge pump of the OEIC with VUC fabricated in $0.5\text{ }\mu\text{m}$ BiCMOS technology

Figure 6.109 shows the generation of the photodiode bias on the receiver chip. The multivibrator as an oscillator and the 4-stage Dickson charge pump were designed symmetrically to keep the disturbances to the integrated photodiode and TIA low. The charge-pump capacitors worked with exponentially decaying voltages reducing the injection of substrate noise via the large parasitic capacitances of the charge-pump capacitors towards substrate. The current of the multivibrator was kept constant by integrated constant current sources to minimize voltage spikes at the bond-wire inductances due to current changes. With a dark photodiode, i.e. no photocurrent, the switching frequency was about 60 MHz. For a photocurrent of $100\text{ }\mu\text{A}$, the switching frequency reduced to about 30 MHz. The totally symmetrical Dickson charge pump kept substrate and power supply noise low [126].

Figure 6.110 shows the circuit of the symmetrical four-stage Dickson charge pump. The diodes were formed by a pn junction of the npn transistor. The pump capacitors had a value of 2 pF and C_{OUT} was 5 pF . The low-pass filter was formed by T_1 as emitter follower, whose base voltage was filtered by a lead-lag filter with corner frequencies 1 and 10 MHz [126]. With a supply voltage $VCC = 5\text{ V}$, the four-stage Dickson charge pump generated an output voltage $V_{PUMP} = 11.7\text{ V}$. A $0.5\text{ }\mu\text{m}$ BiCMOS technology with $f_t = 25\text{ GHz}$ was modified to integrate a pin photodiode together with receiver and VUC (see Fig. 6.111). The chip area was $1160 \times 870\text{ }\mu\text{m}^2$. The charge pump output was on-chip connected to VPD. The VPD bondpad was only present for characterization purposes [126].

The OEIC chip consumed a power of 185 mW at 5 V , of which 160 mW belonged to the receiver and 25 mW to the VUC. The power of the receiver consisted of 100 mW for the output driver and 60 mW for TIA, dummy TIA, and post amplifier. An over-all

Fig. 6.111 Microphotograph of the OEIC with VUC fabricated in $0.5\text{ }\mu\text{m}$ BiCMOS technology

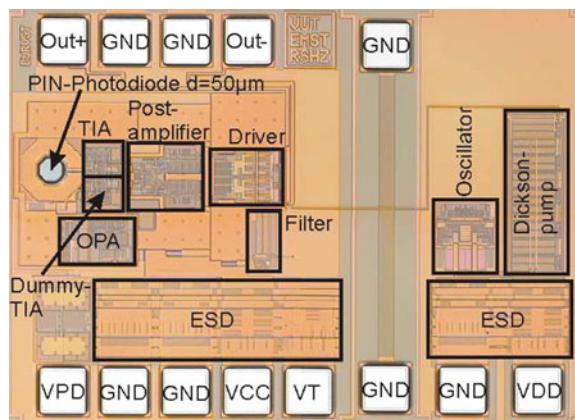
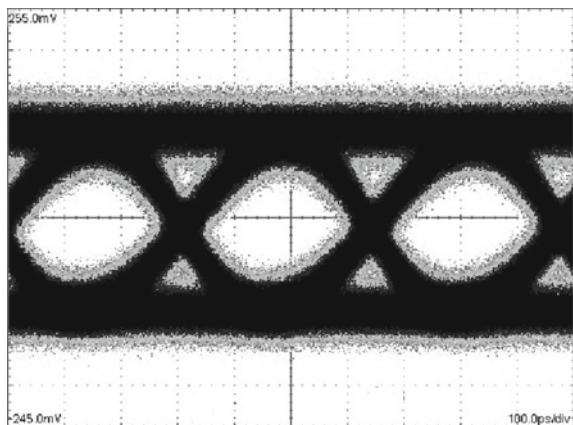


Fig. 6.112 Measured eye diagram of the OEIC with VUC fabricated in $0.5\text{ }\mu\text{m}$ BiCMOS technology at 3 Gb/s and average optical input power of -24.3 dBm ($\text{VPD} = 11\text{ V}$, 660 nm , PRBS31, $\text{BER} = 10^{-9}$)



gain-bandwidth product of $120\text{ THz}\Omega$ was achieved. At 5 V, the space-charge region extended already through the complete intrinsic zone of the pin photodiode and the -3 dB bandwidth was already 1.5 GHz . The VUC with $\text{VPD} = 11\text{ V}$ increased the bandwidth to 2.4 GHz . Rise and fall times of 186 and 208 ps, respectively, were measured with the VUC being active [126].

The measured eye diagram at 3 Gb/s (NRZ) is shown in Fig. 6.112. Sensitivities of -29.3 , -24.3 , -22.9 , and -20.5 dBm for 1 , 3 , 4 , and 5 Gb/s , respectively, all for $\text{BER} = 10^{-9}$ and for 660 nm were measured. No influence of the VUC was noticed compared to the usage of an off-chip 11 V DC supply. At 2.5 Gb/s with 850 nm a sensitivity of -22.8 dBm was reported [126]. In [127], even results at 6 Gb/s were reported: the sensitivity was -21.0 dBm for 660 nm and -18.2 dBm for 850 nm .

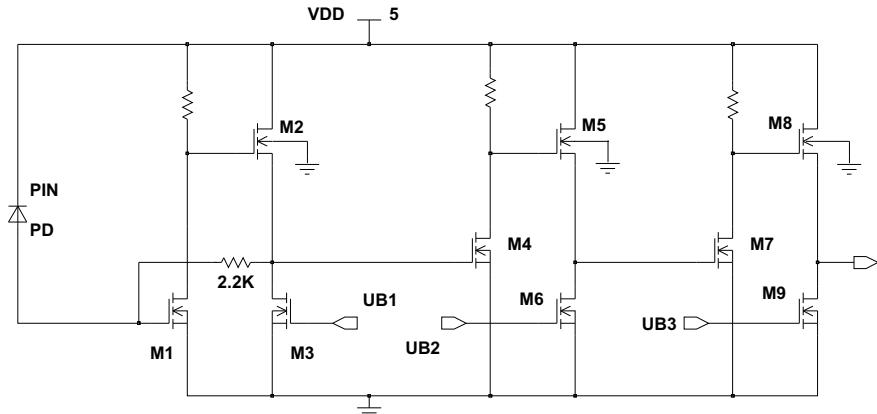


Fig. 6.113 Circuit diagram of a CMOS preamplifier OEIC [101]

CMOS Receivers

Another field of application for OEICs in addition to fiber receivers is optical interconnect technology, because electrical interconnects on a board or system level are becoming a problem due to steadily increasing clock frequencies. In particular, signal reflections on long interconnects on large boards and the cross-talk on high-density electronic boards with conductor widths of 0.1 mm and conductor spacings of 0.1 mm are critical. Optical interconnects, e.g. via waveguide-in-board or fiber-in-board and optical backplanes, avoid the problems of electrical interconnects.

For the application in optical interconnect technology, a CMOS preamplifier OEIC was developed choosing the innovative monolithic integration of vertical PIN photodiodes in a twin-well CMOS-process (Fig. 2.20) [88], which uses epitaxial wafers. The integration of PIN photodiodes in such a CMOS technology requires much less additional process complexity than the published approaches to standard-buried-collector (SBC) based bipolar OEICs [86, 87]. Three additional masks were necessary for the PIN-bipolar integration and for the avoidance of the Kirk effect [86]. Only one photodiode protection mask is added for the PIN-CMOS integration in order to block out an originally unmasked threshold implantation from the photodiode area. A reduction of the standard doping concentration C_e of approximately $1 \times 10^{15} \text{ cm}^{-3}$ in the epitaxial layer was necessary in order to obtain fast integrated PIN photodiodes. In contrast to a reduction of the current gain and of the transit frequency of bipolar transistors in bipolar OEICs due to the Kirk effect, the electrical performance of the N- and P-channel MOSFETs is not degraded when the doping level in the epitaxial layer is reduced, because these MOSFETs are placed in wells [88]. Reach-through and electrostatic discharge (ESD) aspects in the CMOS OEICs can be dealt with using appropriate design measures.

In contrast to the OEIC of [116], here, only a single power supply of 5 V is needed. The circuit of the preamplifier OEIC is shown in Fig. 6.113.

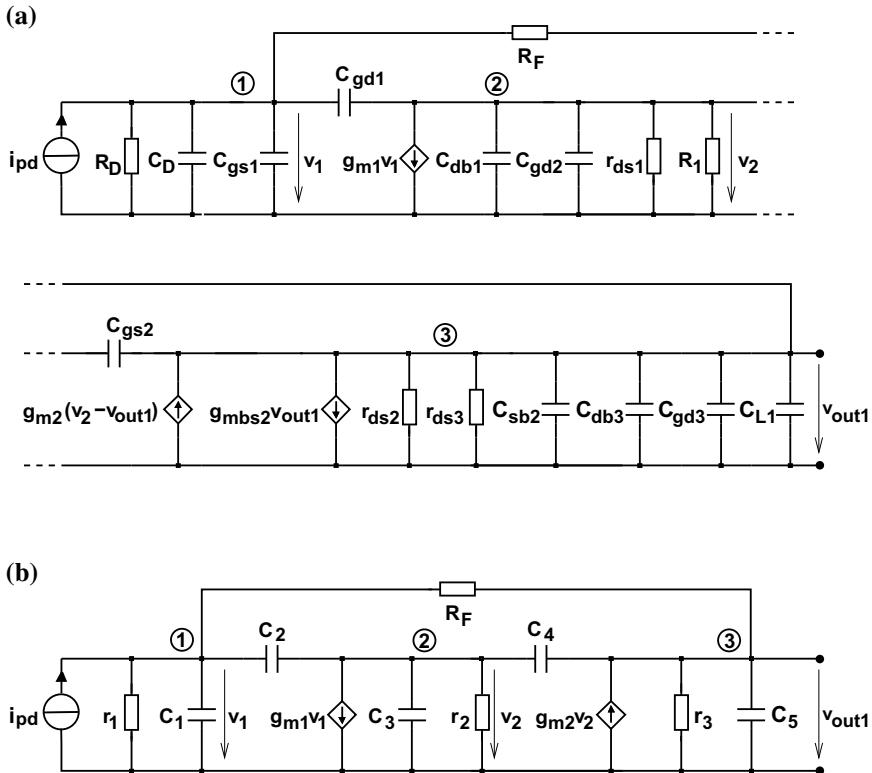


Fig. 6.114 Small-signal equivalent circuit of the first stage in the amplifier shown in Fig. 6.113 (a) and its simplified small-signal equivalent circuit (b) [128]

The amplifier consists of three stages. The input stage with M1–M3 is a transimpedance configuration. The source followers M2, M5, and M8 as well as the current sources M3, M6, and M9 are used for level shifting. Without these transistors, V_{GS} of transistor M1 would be larger and a lower voltage across the PIN photodiode would result and would increase the rise and fall times of its photocurrent. The threshold implant in Fig. 2.19g was omitted in order to reduce the threshold voltage of transistors M2, M5, and M8 intentionally to about 0.4 V by using the photodiode protection mask in order to obtain lower V_{GS} values and to realize the optimum level shifting in such a way. Due to the feedback across the 2.2 k Ω transimpedance resistor R_F and to the identical dimensions of the transistors in the different stages, a good independence from process deviations within the relatively large specified process tolerances of the used digital CMOS process is obtained [101].

The small-signal transimpedance of the input stage can be calculated from the small-signal equivalent circuit (Fig. 6.114a).

For lower frequencies the small-signal equivalent circuit simplifies because the inner transistor capacitances can be considered as open circuit (Fig. 6.114a). This

leads to the node equations [128]:

$$i_{\text{pd}} - \frac{v_1}{r_1} - \frac{v_1 - v_{\text{out}1}}{R_F} = 0 \quad (\text{Node 1}) \quad (6.66)$$

$$g_{m1}v_1 + \frac{v_2}{r_2} = 0 \quad (\text{Node 2}) \quad (6.67)$$

$$g_{m2}v_2 - \frac{v_{\text{out}1}}{r_3} + \frac{v_1 - v_{\text{out}1}}{R_F} = 0 \quad (\text{Node 3}), \quad (6.68)$$

where

$$\begin{aligned} r_1 &= R_D \\ r_2 &= \frac{1}{g_{ds1} + \frac{1}{R_1}} \\ r_3 &= \frac{1}{g_{m2} + g_{mbs2} + g_{ds2} + g_{ds3}} . \end{aligned}$$

C_1 includes the capacitances between input node 1 and ground; C_2 between node 1 and 2. C_3 are all capacitances between node 2 and ground, C_4 between node 2 and 3, and C_5 between node 3 and ground. There are the following equations:

$$\begin{aligned} C_1 &= C_D + C_{gs1} \\ C_2 &= C_{gd1} \\ C_3 &= C_{db1} + C_{gd2} \\ C_4 &= C_{gs2} \\ C_5 &= C_{sb2} + C_{db3} + C_{gd3} + C_{L1} . \end{aligned}$$

C_5 does not explicitly include C_{gs3} which is in series to C_{gd3} with a value of $\approx C_{gd3}$. These capacitances are considered in the load capacitance C_{L1} , which also considers the input capacitance C_{in2} of the second amplifier stage.

Solving the node equations leads to the transimpedance $v_{\text{out}1}/i_{\text{pd}}$ of the input stage. With the resistance R_D of the photodiode much bigger than R_F , it follows:

$$\frac{v_{\text{out}1}}{i_{\text{pd}}} = R_F \frac{\left(\frac{1}{R_F} - A\right)}{\left(\frac{1}{r_3} + A\right)} , \quad (6.69)$$

with

$$A = g_{m1}g_{m2}r_2 . \quad (6.70)$$

If $A \gg \frac{1}{R_F}$ and $A \gg \frac{1}{r_3}$, the transimpedance of the input stage is just $-R_F$.

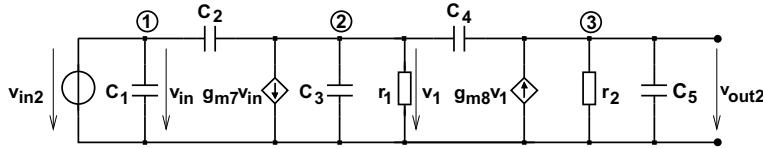


Fig. 6.115 Small-signal equivalent circuit of the second stage in the amplifier shown in Fig. 6.113 [128]

The small-signal gain of the second and third stage is identical considering an unloaded output of the third stage and can be extracted from Fig. 6.115 to

$$A_{v2} = \frac{v_{out2}}{v_{in2}} = -\frac{g_{m7}g_{m8}}{\left(g_{ds7} + \frac{1}{R_2}\right)(g_{m8} + g_{mbs8} + g_{ds8} + g_{ds10})} . \quad (6.71)$$

Assuming an ideal source follower, i.e. the well of the transistor is connected to its source: $g_{mbs8} = 0$, and assuming low output conductances g_{ds} , the expression simplifies to

$$\frac{v_{out2}}{v_{in2}} \approx -\frac{g_{m7}g_{m8}}{\frac{1}{R_2}g_{m8}} = -g_{m7}R_2 . \quad (6.72)$$

However, it is necessary to take the bulk-source voltage of the source follower M2, M5, and M8 into account, such (6.71) has to be used. With a single power supply of 5 V and parameter values from a numerical circuit simulation, the transimpedance of the input stage can be calculated with (6.69) to $-1.616 \text{ k}\Omega$, and the gain of the second and third stage with (6.71) to -3.61 [128]. Thus the overall transimpedance of the amplifier results to $-21.06 \text{ k}\Omega$.

The transfer function $v_{out1}(s)/i_{pd}(s)$ of the input stage of the amplifier shown in Fig. 6.113 can be written with the three node equations including the capacitances according to Fig. 6.114a+b [128]:

$$v_1 \left[\frac{1}{r_1} + \frac{1}{R_F} + s(C_1 + C_2) \right] - v_2(sC_2) - v_{out1} \left(\frac{1}{R_F} \right) = i_{pd} \quad (6.73)$$

$$v_1 (g_{m1} - sC_2) + v_2 \left[\frac{1}{r_2} + s(C_2 + C_3 + C_4) \right] - v_{out1}(sC_4) = 0 \quad (6.74)$$

$$v_1 \left(\frac{1}{R_F} \right) + v_2(g_{m2} + sC_4) - v_{out1} \left[s(C_4 + C_5) + \frac{1}{r_3} + \frac{1}{R_F} \right] = 0 \quad (6.75)$$

or as a matrix equation:

$$\begin{pmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \\ v_{out1} \end{pmatrix} = \begin{pmatrix} i_{pd} \\ 0 \\ 0 \end{pmatrix} . \quad (6.76)$$

The solution of this equation system with $a_{13} = a_{31}$ is

$$\frac{v_{\text{out1}}(s)}{i_{\text{pd}}(s)} = \frac{a_{21}(-a_{12}a_{13} + a_{32}a_{11}) + a_{13}(a_{12}a_{21} - a_{22}a_{11})}{(a_{13}a_{21} - a_{11}a_{23})(-a_{12}a_{13} + a_{32}a_{11}) - (a_{12}a_{21} - a_{22}a_{11})(-a_{13}^2 + a_{33}a_{11})} . \quad (6.77)$$

This can also be written in the following form

$$\frac{v_{\text{out1}}(s)}{i_{\text{pd}}(s)} = \frac{Z(s)}{N(s)} = \frac{a + bs + cs^2 + ds^3}{e + fs + gs^2 + hs^3 + is^4} . \quad (6.78)$$

Here, it can be seen, that the input stage has already four poles and three zeros. The disadvantage of algebraic solving of the node equations is the high complexity with just small circuits. In addition, the solution may be correct, but hard to “understand”. For a better understanding there are two main possibilities to estimate the cutoff frequency of the circuit. (i) If there is a dominant pole, the cutoff frequency is determined mainly by this pole. This is true when a zero in the denominator of the transfer function is much smaller than the others in absolute values. In addition the zeros of the numerator have to be at higher frequencies such that the cutoff frequency is not influenced. The dominant pole is formed by the quotient of the first two coefficients of the denominator polynomial. (ii) With no dominant pole the cutoff frequency is determined by several poles and zeros. A simple estimation of the cutoff frequency can be done with the so-called *Open-Circuit Time-Constant* method [129]. The cutoff frequency of a circuit is then

$$f_{-3 \text{ dB}} \approx \frac{1}{2\pi \sum_{i=1}^m R_{i0} C_i} . \quad (6.79)$$

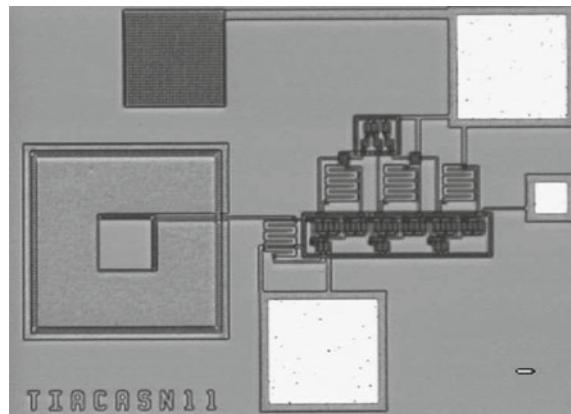
The resistances R_{i0} have to be determined at the nodes of the respective capacitances C_i while all other capacitances are removed. After determination of all terms $R_{i0} C_i$ it is obvious which node is dominant. For the input stage of the amplifier (Figs. 6.113 and 6.114) this shows that the cutoff frequency is dominated by the time constant $R_{10} C_1$. It is [128]

$$R_{10} = \frac{R_F + r_3}{1 + Ar_3} , \quad (6.80)$$

with A from (6.70). For a high cutoff frequency, R_{10} should be small, and for a high transimpedance (6.69) has to be considered. Because of the coupled parameters, a high cutoff frequency and a high transimpedance cannot be chosen freely from each other. Therefore the shown design is a compromise between these two goals.

The cutoff frequency of the first stage of the amplifier in Fig. 6.113 after (6.79) is 1034 MHz. The result obtained by numerical circuit simulation for the cutoff frequency of the first stage is 1080 MHz. Such a high cutoff frequency is possible because of the very low capacitance C_D of the integrated PIN photodiode (about

Fig. 6.116 Microphotograph of a CMOS receiver OEIC [101]



26 fF). A discrete setup of photodiode and amplifier would add more capacitances at the input node of the amplifier and therefore reduce the cutoff frequency of the circuit.

Simulated results of the complete amplifier of Fig. 6.113 with all three stages are: the cutoff frequency is 419 MHz and its overall transimpedance is $-20.7\text{ k}\Omega$ [128]. The lower cutoff frequency is caused by the capacitive load of 0.3 pF. This low capacitive load is justified with an internal postamplification of the output voltage. There is a good agreement between the simulated and analytically calculated transimpedance of -20.7 and $-21.1\text{ k}\Omega$, respectively.

The CMOS receiver OEIC was fabricated in a $1.0\text{ }\mu\text{m}$ industrial CMOS process [130]. The microphotograph of the CMOS preamplifier OEIC can be seen in Fig. 6.116.

The photodiode, having a light sensitive area of $2700\text{ }\mu\text{m}^2$, together with its metal shield around covers an area of approximately $150 \times 150\text{ }\mu\text{m}^2$. The preamplifier occupies an active area of less than $130 \times 200\text{ }\mu\text{m}^2$. The sensitivity of the PIN CMOS preamplifier OEIC was $4.7\text{ mV}/\mu\text{W}$ without ARC and its power consumption was 19 mW at 5.0 V .

The oscilloscope extracted a rise time $t_r^{\text{osc,disp}} = 15.5\text{ ns}$ and a fall time $t_f^{\text{osc,disp}} = 17.6\text{ ns}$ for the OEIC with the doping concentration of $1 \times 10^{15}\text{ cm}^{-3}$ in the epitaxial layer for a laser wavelength of 638.3 nm. These large values for t_r and t_f are due to the slow carrier diffusion in the standard epitaxial layer of the photodiode. The corresponding values for the concentration of $2 \times 10^{13}\text{ cm}^{-3}$ in the epitaxial layer, where the depletion region spreads through the whole epitaxial layer and carrier diffusion in the photodiode is eliminated, were 1.05 and 1.26 ns, respectively [101].

Figure 6.117 shows the eye diagram of the CMOS preamplifier OEIC in Figs. 6.113 and 6.116. The eye diagram was measured on the wafer level with a picoprobe (input capacitance: 0.1 pF) at the output of the OEIC, with an HP54750/51 digital sampling oscilloscope, and with an ECL bit pattern generator, which modulated a red semiconductor laser with a wavelength of 638.3 nm. A pseudo-random bit sequence (PRBS)

Fig. 6.117 Measured eye diagram of a CMOS preamplifier OEIC for the application in a fiber and interconnect receiver (time: 500 ps/div, amplitude: 0.2 V/div)

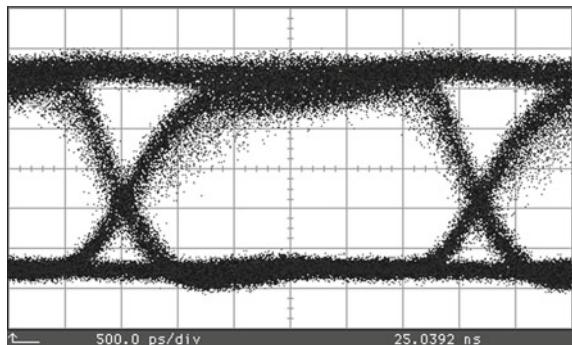
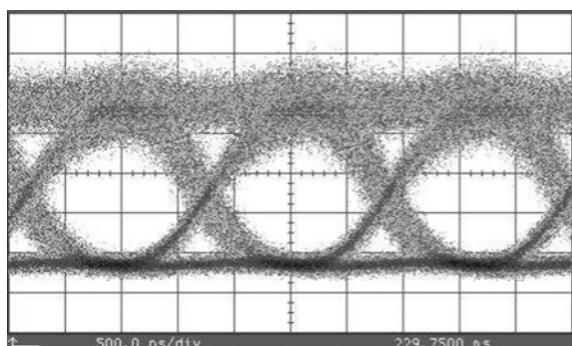


Fig. 6.118 Eye diagram of the redesigned PIN OEIC with the amplifier shown in Fig. 6.113 (622 Mbit/s, 500 ps/div, 200 mV/div, $\lambda = 638 \text{ nm}$, $C_e = 2 \times 10^{13} \text{ cm}^{-3}$) [128]



of $2^{23} - 1$ in a non-return-to-zero (NRZ) bit rate of 320 Mb/s was used. The doping concentration in the epitaxial layer of the wafer which was used for the fabrication of the OEIC was $2 \times 10^{13} \text{ cm}^{-3}$.

Simulations showed that shorter rise and fall times can be expected for an improved preamplifier and bit rates in excess of 600 Mb/s seem feasible for a wavelength of 638 nm. For wavelengths of 780 and 850 nm bit rates of 500 Mb/s were estimated by simulations [101]. Meanwhile, the OEIC has been redesigned and characterized by eye diagram measurements at a bit rate of 622 Mb/s with a wavelength of 638 nm [131]. The redesigned OEIC containing a PIN photodiode with an area of $2700 \mu\text{m}^2$ and the amplifier of Fig. 6.113 in $1.0 \mu\text{m}$ CMOS technology with an active area of $230 \times 150 \mu\text{m}^2$ showed a measured sensitivity of $5.7 \text{ mV}/\mu\text{W}$ for 638 nm and $7.1 \text{ mV}/\mu\text{W}$ for 850 nm [128]. With the responsivity of the pin photodiode without antireflection coating (ARC) of 0.24 A/W for 638 nm and 0.30 A/W for 850 nm an overall transimpedance of $23.75 \text{ k}\Omega$ results for the amplifier in Fig. 6.113 compared to a simulated transimpedance of $20.7 \text{ k}\Omega$ and a calculated transimpedance of $21.1 \text{ k}\Omega$. The higher measured value can be explained by process tolerances. For a wavelength of 638 nm, rise and fall times of 1.08 and 0.94 ns, respectively, were measured for the PIN OEIC with the amplifier in Fig. 6.113 and with $C_e \approx 2 \times 10^{13} \text{ cm}^{-3}$. The eye diagram of this OEIC for a data rate of 622 Mbit/s is shown in Fig. 6.118.

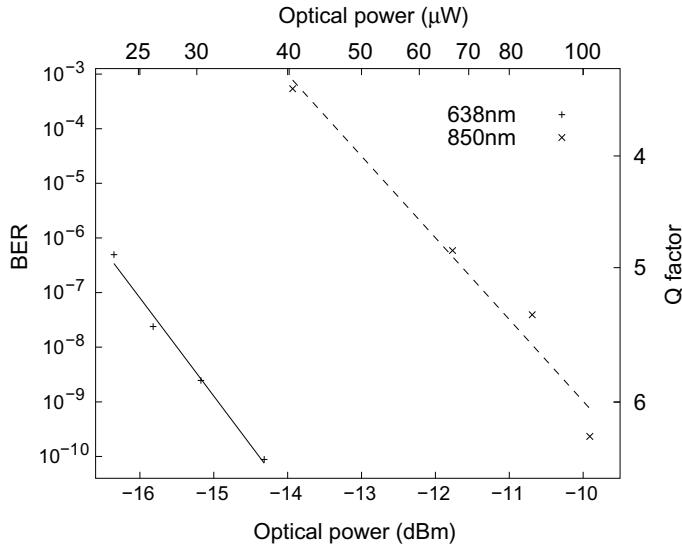


Fig. 6.119 Bit error rate of the PIN OEIC with the amplifier from Fig. 6.113 in dependence on the optical input power with $V_{DD} = 5$ V and $C_e = 2 \times 10^{13} \text{ cm}^{-3}$ at 622 Mb/s [128]

A sensitivity of -14.9 dBm was obtained for an non-return-to-zero (NRZ) data rate of 622 Mb/s by measurement of the bit error rate in dependence on the optical input power for a BER of 10^{-9} at 638 nm (Fig. 6.119).

For 850 nm, the sensitivity was -10.0 dBm for the same data rate and BER. For the redesigned PIN OEIC after Fig. 6.113, a power consumption of 23 mW was observed for a supply voltage of 5 V [128].

An sophisticated OEIC in standard CMOS technology using the SML detector described in Sect. 2.2.5 was reported [132]. Nine receiver channels for optocoupler applications were implemented. In each channel, the photocurrent of the immediate detector (I in Fig. 6.120) and the diffusion current of the deferred detector (D in Fig. 6.120) are first amplified and then an OTA (operational transconductance amplifier) is used to subtract the diffusion signal from the immediate detector signal.

A reference channel is needed since data transmitted by optocouplers are not coded, and hence not dc balanced. The average of the signal, therefore, cannot be used as a threshold level. A reference channel has to be used to determine the threshold level I_{ref} (see Fig. 6.120). The LED in this channel is always on and the reference receiver takes half of the difference between the photocurrent of the immediate detector and the diffusion current of the deferred detector. The current I_{ref} is mirrored into the active channels 1–9 as a threshold value for these channels. When the difference current of immediate and deferred detector ($I - D$) exceeds this threshold, the OTA produces a positive output signal. If no light incidents in the SML detectors of channels 1–9, the threshold is not reached and the output signal of the OTA remains negative [132].

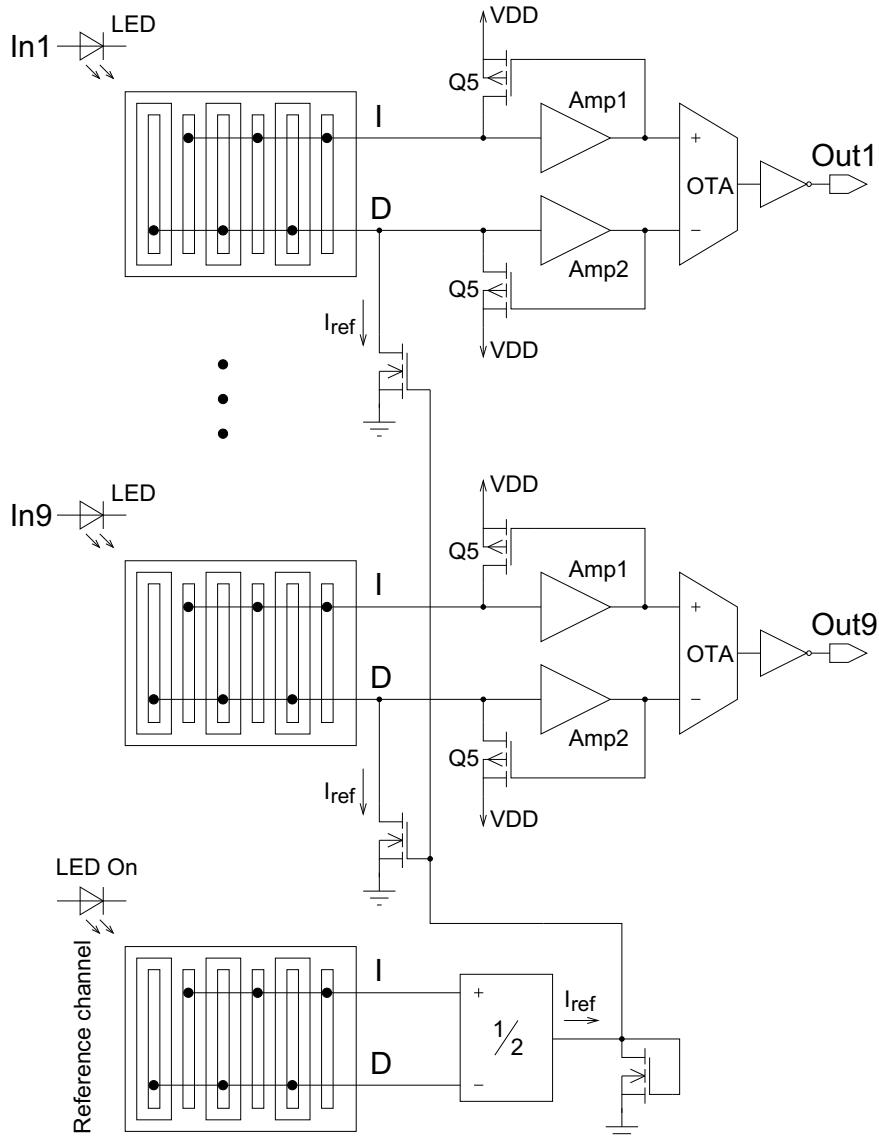


Fig. 6.120 Schematic overview of the SML detector OEIC [132]

The circuit diagram of the two identical amplifiers of each channel is shown in Fig. 6.121. This amplifier has active transistor feedback (**Q5**) and therefore acts as a transimpedance amplifier [132]. Transistor **Q5** connected as a one-stage amplifier in common-source configuration was degenerated with a channel length of $6.3\ \mu\text{m}$

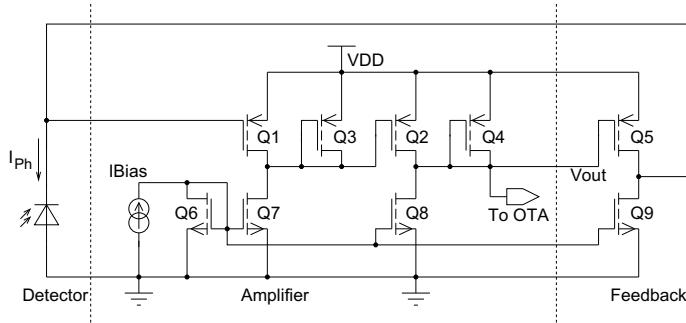


Fig. 6.121 Circuit diagram of the transimpedance amplifier used in the SML OEIC [132]

[132]. A transimpedance amplifier is obtained since Q5 (with the constant current load Q9) transforms a voltage into a current (g_{m5} corresponds to $1/R_F$).

For a large open-loop gain A_{OL} the transimpedance

$$\frac{V_{\text{out}}}{I_{\text{Ph}}} = \frac{1/(-g_{m5})}{1 - i(f/2\pi C_{\text{det}})/(A_{OL}g_{m5})} \quad (6.81)$$

is obtained [132] with V_{out} and I_{Ph} defined in Fig. 6.121. If $-g_{m5}$ is replaced by $1/R_F$, the behavior of a conventional TIA is obtained. MOS diode loads Q3 and Q4 are used to achieve stability (Fig. 6.121).

The circuit was implemented in a $0.6\text{ }\mu\text{m}$ standard CMOS technology. The SML detectors had an area of $50 \times 50\text{ }\mu\text{m}^2$. The receivers including the output driver fitted easily into an area of $50 \times 230\text{ }\mu\text{m}^2$ each [132]. At 860 nm, sensitivities of -23 dBm for 200 Mb/s and -18 dBm for 250 Mb/s , respectively, were reported for a BER of 10^{-9} . The power consumption of each channel was about 4 mW [132]. A data rate of 700 Mb/s was achieved in a $0.25\text{ }\mu\text{m}$ CMOS technology with a sensitivity of -18.7 dBm for a BER of 10^{-9} at 860 nm. The sensitivity for a BER of 10^{-12} was about -18.0 dBm . The power consumption of a channel in this chip was 2.5 mW [133], which is a remarkable low value.

A fast fully integrated single-beam optical bulk CMOS receiver (Fig. 6.122) was realized in the Lucent $0.35\text{ }\mu\text{m}$ production process [134]. This receiver contained the photodetector shown in Fig. 2.16. The amplifier of this receiver is formed by three inverter stages. The first stage with M1 and M2 is an inverter-based transimpedance stage with the P-channel MOSFET M8 as the feedback element. The gate voltage of M8 could be adjusted for optimum performance (V_{tune}) at a given optical power and bit rate. This first stage converts the photocurrent, flowing from the anode of the photodiode through the active resistor M8, into a voltage. The second stage with the inverter M3, M4 amplifies this voltage. The N-channel MOSFET load M5 reduces the gain and increases the bandwidth. With M5, the technology dependence of the amplifier gain is reduced and the switching threshold of this stage is stabilized [135]. The third stage with M6 and M7 supplies a high gain. This stage acts as

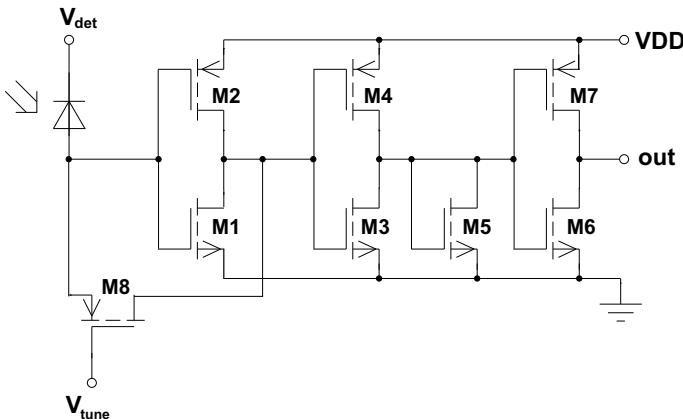


Fig. 6.122 CMOS inverter receiver OEIC [134]

an asynchronous decision circuit resulting in a fully digital logic output level. For a correct and optimum performance of this DC-coupled three-stage preamplifier circuit, the dimensions of the transistors M5 and M8 have to be chosen carefully [134].

The supply voltage of the preamplifier was varied between 1.8 and 3.3 V. The best sensitivity was obtained at a supply bias of $V_{DD} = 2.2$ V. A bit error rate of 10^{-9} for a bit rate of 1 Gb/s was obtained with an average optical input power of -6.3 dBm and with a detector bias $V_{det} = 10$ V. This low sensitivity results from the low responsivity of the photodiode of less than 0.04 A/W. Another disadvantage of this OEIC is the high detector bias of 10 V.

For an OEIC fabricated in a $0.25\text{ }\mu\text{m}$ fully-depleted CMOS SOI process technology, a single 2 V supply was sufficient [136]. The photodiode of this OEIC was a lateral PIN photodiode in a 50 nm thick SOI layer (see Fig. 3.5). The authors ascribed the high photodiode responsivity of 0.4 A/W to an avalanche effect [136]. The amplifier circuit of this OEIC is shown in Fig. 6.123.

The preamplifier circuit is based on a transimpedance amplifier with a feedback resistor R_{fb} of $5\text{ k}\Omega$. The N-channel MOSFET N1 is used in a common-source circuit. The PMOS transistor P1 forms the active load for N1. N2 is used as source follower in order to obtain a low output impedance of the transimpedance input stage. N3 is a constant-current source. N4 amplifies the output voltage of the transimpedance input stage. P6 is used as a source follower for shifting the signal level towards VDD and reducing the output impedance. This shifting towards VDD is necessary to allow the implementation of the second source follower N7 for further reducing the output impedance. P5 and N8 are constant-current sources. P3, P4, N5, and N6 supply the reference voltage V_{ref} for biasing the amplifier. The constant-current sources P1, P2, and P5 are set by P3. These four transistors form current mirrors.

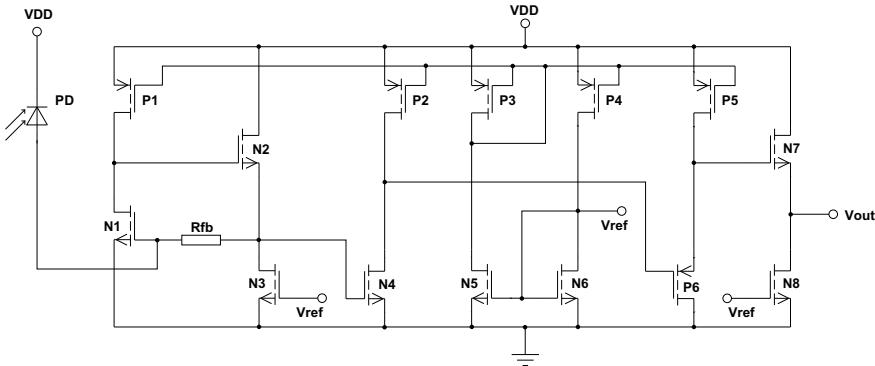


Fig. 6.123 CMOS receiver OEIC on SOI [136]

Using a 850 nm wavelength, a bandwidth of 1 GHz was measured for a supply voltage of 2 V for an average optical input power of -13 dBm ($50 \mu\text{W}$) [136]. The OEIC occupied an area of $650 \times 400 \mu\text{m}^2$.

An OEIC for inter-chip communication using silicon-on-sapphire (SOS) CMOS technology was introduced [137, 138]. Similar to SOI technology, SOS technology reduces parasitic bulk capacitances. It, therefore, increases the bandwidth. Further advantages are that SOS reduces cross-talk, power and substrate noise. Especially instabilities due to bulk substrate feedback are avoided [137]. A receiver circuit fabricated in an SOS 0.5 μ m CMOS process operating at 1 Gb/s while consuming only 5 mW of power at a 3.3 V supply with an effective transimpedance of 50 k Ω was presented [137]. This power consumption is low compared to 26 mW of a 1.5 Gb/s receiver [139] and to over 100 mW of other designs [97, 140].

The circuit diagram of the SOS receiver is shown in Fig. 6.124. The first stage has a transimpedance of $9\text{ k}\Omega$ and was designed for Gb operation with 0.5 pF input capacitance generated by a MSM or PIN photodiode. The photodiode is represented by a reverse biased diode in parallel with its capacitance C_D in Fig. 6.124. There are five high-bandwidth gain stages following the transimpedance input stage. A differential-to-single ended conversion is done in a sixth stage and a source follower output buffer (not capable of driving a $50\text{ }\Omega$ load rail-to-rail) forms the output [137]. $10\text{ }\mu\text{A}$ of photocurrent at each receiver input or $20\text{ }\mu\text{A}$ of photocurrent at one input caused a rail-to-rail output swing for a 3.3 V supply [137]. PMOS load elements are used in a MOS diode configuration to avoid biasing circuitry. The receiver, therefore, required only one bias (V_{nb}). The transimpedance amplifier had a phase margin of 45% for limited gain peaking [137].

The transistors in the gain stages had smaller widths than that in the transimpedance stage. The chain of gain stages, therefore, could be made fast while consuming little power since the input transistors of each stage comprise the load of the previous stage. Large input transistors in the transimpedance amplifier improve the gain of the input stage and the sensitivity of the receiver due to reducing electronic

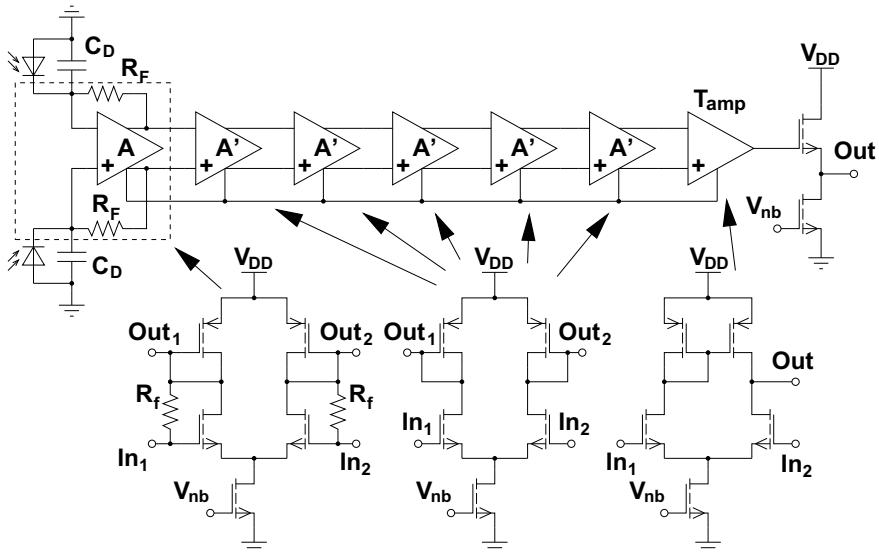


Fig. 6.124 CMOS receiver OEIC on SOS [137]

noise. The bandwidth of the transimpedance amplifier is dominated by the input node capacitance, feedback resistance, and the gain of the differential amplifier.

The Peregrine Ultra-thin SOS process provided N and P channel devices with three channel doping level, i.e. with three different threshold voltages [137]. Zero-threshold MOSFETs with no channel doping with the same output currents as doped devices with larger widths could therefore be exploited with smaller widths. Thus, gate capacitances could be minimized. The P-channel load devices were zero-threshold devices in order to limit capacitive loading on the outputs of the amplifier stages. The NMOS input transistors, however, were regular threshold devices with $V_{Th} = 0.7\text{ V}$ since they exhibit a higher transconductance at equal currents than the zero-threshold devices [137]. Higher g_m input transistors result in a higher gain-bandwidth product.

The differential topology was chosen to make it well suited to optical interconnect applications. The differential design is robust to process variations, which may vary device parameters, to power supply noise, and to ambient light conditions. Due to its low power consumption the SOS receiver is ideal for use among a large array of VCSEL inputs switched about a laser threshold.

The SOS receiver was operated at 650 Mb/s with a differential optical input and at 900 Mb/s with a single optical input [137]. The experiments were performed with a 0.5 pF MSM photodiode bonded to each input. The SOS receiver area was $45 \times 70\text{ }\mu\text{m}^2$ [137]. No sensitivity data were reported. The quality of eye diagrams for $100\text{ }\mu\text{W}$ optical input power was not very good due to jitter [137].

Based on the circuit shown in Fig. 6.113, an improved CMOS photoreceiver (Fig. 6.125), which contains a vertical PIN photodiode and which combines a data rate of 622 Mb/s with a photodiode quantum efficiency of 94%, has been developed.

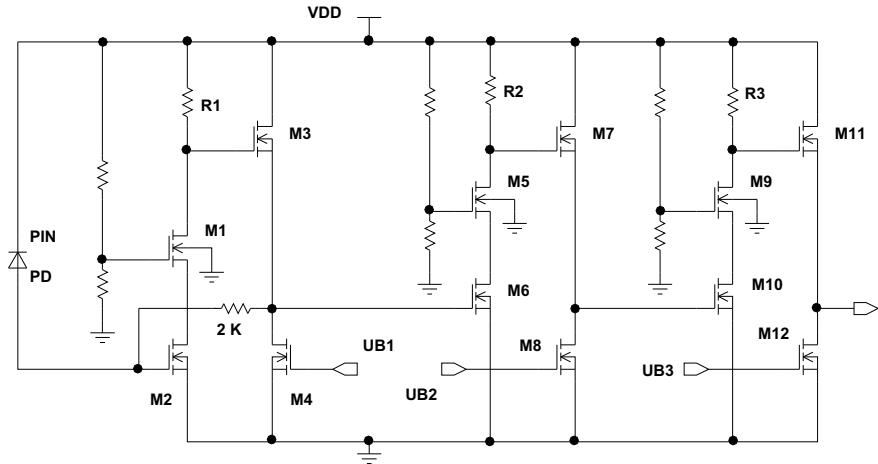


Fig. 6.125 Circuit diagram of a CMOS preamplifier OEIC with a possible data rate of 622 Mb/s for application in a fiber and interconnect receiver [101]

The innovative monolithic integration of vertical PIN photodiodes in a twin-well CMOS process (Fig. 2.20) [88] which uses epitaxial wafers, has been demonstrated to combine both high speed and large quantum efficiency of the photodiode [101]. In contrast to the OEICs of [116, 134], there, only a single power supply of 3.3 V was needed. The circuit of the high-bandwidth preamplifier with an integrated PIN photodiode is shown in Fig. 6.125. It is a typical high-frequency amplifier. Only N-channel MOSFETs are used in order to obtain a high bandwidth. The input stage with the transistors M1–M4 is a transimpedance configuration, which converts the photocurrent change in the integrated PIN photodiode to a voltage change. The cascode transistors M1, M5, and M9 reduce the Miller effect and increase the bandwidth correspondingly. The source followers M3, M7, and M11 as well as the current sources M4, M8, and M12 are used for level shifting. The threshold voltage of transistors M3, M7, and M11 has been reduced intentionally to about 0.4 V by the photodiode protection mask in order to obtain lower V_{GS} values. Polysilicon resistors were employed as load elements, since depletion transistors were not available in the digital CMOS process. Due to the feedback across the 2 k Ω resistor and to the identical dimensions of the transistors in the different stages, a good independence from process deviations within the relatively large specified process tolerances of the digital CMOS process used has been obtained. Three identical biasing circuits ($UB_1 = UB_2 = UB_3$) are used instead of one in order to minimize parasitic coupling between the stages.

The following calculations and estimations can be made for the circuit schematic of Fig. 6.125: The small-signal transimpedance of the first stage is calculated in the same way as described for the amplifier shown in Fig. 6.113. In Fig. 6.126 the complete and the simplified small-signal equivalent circuit of the first stage is shown.

Caused by the cascode transistor M1, another node is present compared to the circuit in Fig. 6.115. The small-signal output resistance r_{ds1c} between node 2 and 3

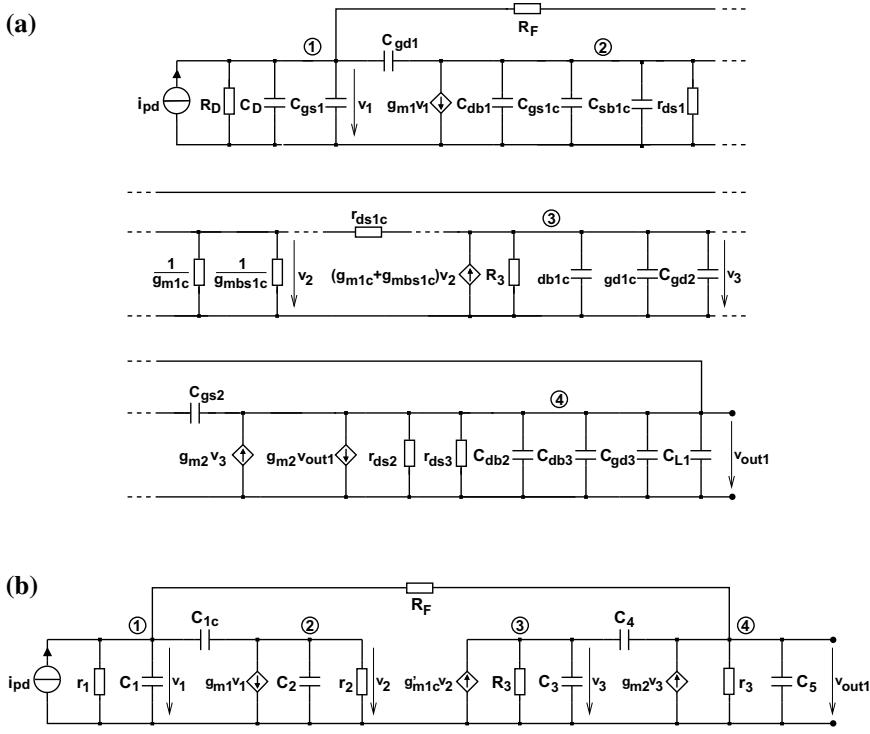


Fig. 6.126 Small-signal equivalent circuit of the first stage in the amplifier of Fig. 6.125 (a) and its simplified small-signal equivalent circuit (b) [128]

has been neglected in Fig. 6.126b. It is [128]

$$\begin{aligned} r_1 &= R_D \\ r_2 &= \frac{1}{g_{ds1} + g_{m1c} + g_{mbs1c}} \\ r_3 &= \frac{1}{g_{m2} + g_{ds2} + g_{ds3}} . \end{aligned}$$

The same expression as in (6.69) follows for the transimpedance. But now it is

$$A = g_{m1}g'_{m1c}g_{m2}r_2R_3 . \quad (6.82)$$

with $g'_{m1c} = g_{m1c} + g_{mbs1c}$. Compared to the amplifier in Fig. 6.113, the transimpedance of the first stage is now a little bit lower caused by the smaller feedback resistance R_F ($2.0\text{k}\Omega$ instead of $2.2\text{k}\Omega$). This was chosen to achieve a higher cutoff frequency. With $V_{DD} = 5\text{V}$ and the parameter values taken from a numerical circuit

simulation and used in (6.69), the transimpedance of the input stage is $-1.585\text{ k}\Omega$. The small-signal amplification of the second stage is [128]

$$A_{v2} = \frac{v_{\text{out}2}}{v_{\text{in}2}} = -\frac{g_{m4}g_{m5}(g_{m4c} + g_{mbs4c})R_3}{(g_{m5} + g_{ds5} + g_{ds6})(g_{m4c} + g_{mbs4c} + g_{ds1})} . \quad (6.83)$$

Here a value of -4.64 can be calculated. With the second and third stage designed identically, the overall transimpedance of the amplifier in Fig. 6.125 results to $-34.1\text{ k}\Omega$. The higher amplification in the second and third stage is responsible for a 50% increase of the overall transimpedance compared to the amplifier shown in Fig. 6.113.

Estimating the frequency response of the amplifier shown in Fig. 6.125, it is necessary to consider the capacitances of the amplifier. For the first stage they are (Fig. 6.126):

$$\begin{aligned} C_1 &= C_D + C_{gs1} \\ C_{1c} &= C_{gd1} \\ C_2 &= C_{db1} + C_{gs1c} + C_{sb1c} \\ C_3 &= C_{db1c} + C_{gd1c} + C_{gd2} \\ C_4 &= C_{gs2} \\ C_5 &= C_{db2} + C_{db3} + C_{gd3} + C_{L1} . \end{aligned}$$

The four node equations to calculate the transfer function are [128]:

$$v_1 \left[\frac{1}{r_1} + \frac{1}{R_F} + s(C_1 + C_{1c}) \right] - v_2(sC_{1c}) - v_{\text{out}1} \left(\frac{1}{R_F} \right) = i_{pd} \quad (6.84)$$

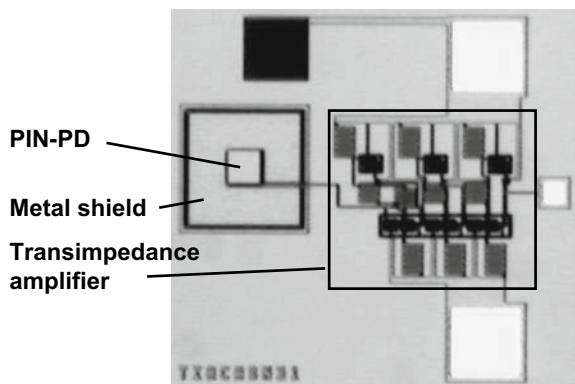
$$v_1(g_{m1} - sC_{1c}) + v_2 \left[\frac{1}{r_2} + s(C_{1c} + C_2) \right] = 0 \quad (6.85)$$

$$-v_2g'_{m1c} + v_3 \left[\frac{1}{R_3} + s(C_3 + C_4) \right] - v_{\text{out}1}(sC_4) = 0 \quad (6.86)$$

$$-v_1 \frac{1}{R_F} - v_3(g_{m2} + sC_4) + v_{\text{out}1} \left[\frac{1}{R_F} + \frac{1}{r_3} + s(C_4 + C_5) \right] = 0 . \quad (6.87)$$

The first stage of the amplifier shown in Fig. 6.125 has five poles and four zeroes. The transfer function is therefore even more complex as the one for the amplifier of Fig. 6.113. As with the amplifier of Fig. 6.113 the Open-Circuit Time-Constant method [129] was used. The time constant related with node 1 was again the one with the biggest influence on the cutoff frequency [128]. The resistance R_{10} results in the same expression as in (6.80) with A from (6.82). Now the difference to the amplifier shown in Fig. 6.113 is obvious. Although the capacitance C_1 is the same, a higher value for A could be achieved through the insertion of the cascode transistor M1.

Fig. 6.127 Microphotograph of a high-speed CMOS receiver OEIC [141]



This leads to a smaller time constant $R_{10}C_1$. Additionally the feedback resistance R_F was lowered from $2.2\text{k}\Omega$ in the amplifier of Fig. 6.113 to $2\text{k}\Omega$ in the amplifier of Fig. 6.125. This results in a cutoff frequency of 1.27GHz for the input stage of the amplifier shown in Fig. 6.125 [128]. A simulation for the complete three-stage topology of the amplifier in Fig. 6.125 showed an overall cutoff frequency of 922MHz with a capacitive load of 0.3pF .

The sensitivity of the PIN preamplifier OEIC was $4.7\text{mV}/\mu\text{W}$ for a wavelength $\lambda=638\text{nm}$ increasing to $9.0\text{mV}/\mu\text{W}$ with ARC, which corresponds to an overall transimpedance of $18.4\text{k}\Omega$. Its power consumption was 44mW at 5.0V reducing to 17mW at 3.3V [128].

The photodiode, together with its metal shield around, covers an area of approximately $150 \times 150\text{\AA m}^2$ (see Fig. 6.127). The preamplifier occupies an active area of less than $190 \times 200\text{\AA m}^2$.

For $\lambda=638\text{nm}$, values of 0.62 and 0.86 ns for the rise and fall times, respectively, at the output of the preamplifier (Fig. 6.128) were obtained for a concentration of $2 \times 10^{13}\text{ cm}^{-3}$ in the epitaxial layer, where the depletion region spreads through the whole epitaxial layer already with a supply voltage of 3.3V [101].

The correction of the $t_{r/f}$ values for the laser and picoprobe rise and fall times results in $t_r^{\text{OEIC}}=0.53\text{ns}$ and $t_f^{\text{OEIC}}=0.69\text{ns}$. These values indicate that CMOS OEICs with a reduced doping concentration in the epitaxial layer having an appropriate output buffer can be used as receivers for optical data transmission via fibers or for optical interconnects on a board level up to a bit rate BR of 622Mb/s in the non-return-to-zero (NRZ) mode, verified by a measured eye diagram with a pseudo-random bit sequence (PRBS) of $2^{23}-1$ (Fig. 6.129).

An redesigned OEIC implementing the PIN photodiode with an area of 2700\AA m^2 and the amplifier of Fig. 6.125 in 1.0\AA m CMOS technology with an active area of $190 \times 200\text{\AA m}^2$ showed a measured sensitivity of $10.4\text{mV}/\mu\text{W}$ for 638nm and $10.9\text{mV}/\mu\text{W}$ for 850nm . With the responsivity 0.24A/W of the photodiode without ARC at 638nm , we obtain an overall transimpedance of $43.2\text{k}\Omega$ for the amplifier of Fig. 6.125 compared to a calculated transimpedance of $34.1\text{k}\Omega$ [128]. The higher

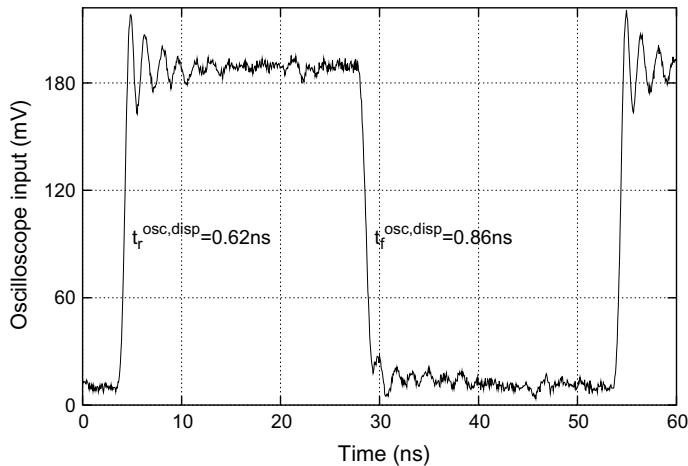
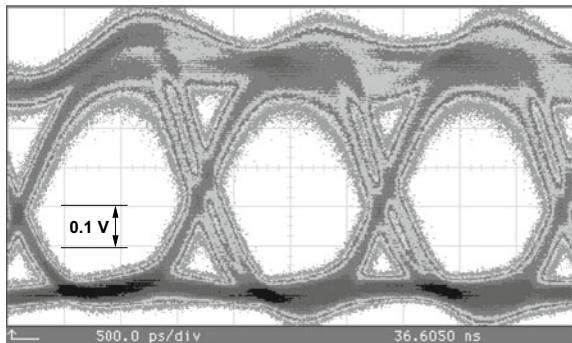


Fig. 6.128 Waveform at the output of the CMOS preamplifier OEIC with a possible data rate of 622 Mb/s for application in a fiber and interconnect receiver [107]

Fig. 6.129 Measured eye diagram of a CMOS preamplifier OEIC with a possible data rate of 622 Mb/s for application in a fiber and interconnect receiver (time: 500 ps/div, amplitude: 0.1 V/div) [101]



measured value can be explained by process tolerances of the resistors' sheet resistance and of the transistor parameters. The transient response of this PIN OEIC with $VDD = 2.5\text{ V}$ is shown in Fig. 6.130.

The measured rise and fall times of the PIN OEIC with the amplifier shown in Fig. 6.125 and with a supply voltage of 2.5 V are 0.89 and 1.14 ns, respectively.

A sensitivity of -14.0 dBm for a data rate of 622 Mb/s at a wavelength of 638 nm for a BER of 10^{-9} was determined by measurements for the PIN OEIC with the amplifier shown in Fig. 6.125 working with a supply voltage of 3.3 V (Fig. 6.131). For 850 nm, the sensitivity was -12.3 dBm for the same supply voltage, data rate, and BER. The power consumption of the redesigned amplifier (Fig. 6.125) in $1.0\text{ }\mu\text{m}$ technology was 42 mW for a supply voltage of 5 V reducing to 15 mW for 3.3 V and 8 mW for 2.5 V. The sensitivity, however, increased to -10.3 dBm for a data rate of 622 Mb/s, for 638 nm, and for the supply voltage of 2.5 V.

Fig. 6.130 Transient response of the PIN OEIC with the amplifier of Fig. 6.125 at $VDD = 2.5\text{ V}$ ($\lambda = 638\text{ nm}$, $C_e = 2 \times 10^{13}\text{ cm}^{-3}$) [128]

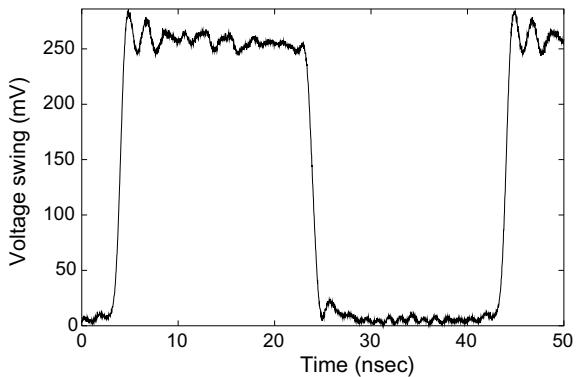
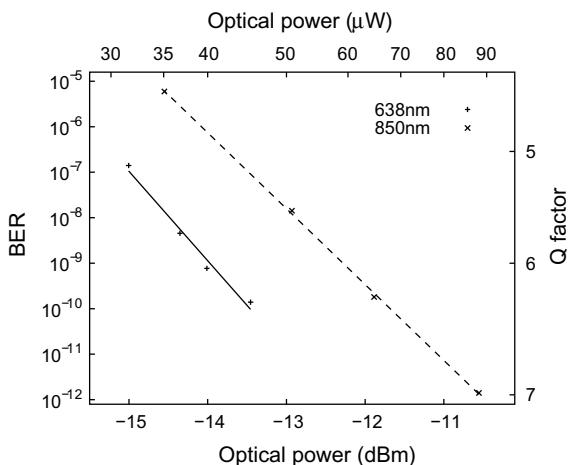


Fig. 6.131 Bit error rate of the PIN OEIC with the amplifier of Fig. 6.125 at $VDD = 3.3\text{ V}$ in dependence on the optical input power with $C_e = 2 \times 10^{13}\text{ cm}^{-3}$ at 622 Mb/s [128]



OEICs in a $1.0\text{ }\mu\text{m}$ technology implementing the amplifier according to Fig. 6.125, however, with the double photodiode, i.e. $C_e \approx 1 \times 10^{15}\text{ cm}^{-3}$, also were investigated [128]. A sensitivity of about -8.4 dBm for a BER of 10^{-9} was found for a data rate of 622 Mb/s at 638 nm with a supply voltage of 5 V [128]. For 850 nm, the time response of the DPD was too slow for data rates of 622 and 531 Mb/s. Even at 311 Mb/s, a BER of 10^{-9} could not be achieved for a maximum optical power of $180\text{ }\mu\text{W}$ at 850 nm [128].

OEICs in a $0.8\text{ }\mu\text{m}$ technology implementing the double photodiode and an amplifier according to Fig. 6.132 also were fabricated and characterized. The measured rise and fall times of these OEICs with the double photodiode and the standard doping concentration $C_e \approx 1 \times 10^{15}\text{ cm}^{-3}$ in the epitaxial layer were 1.21 and 1.14 ns, respectively, for 638 nm and for a supply voltage of 5 V. A data rate of 622 Mb/s at 638 nm was possible with this OEIC using a standard doping concentration $C_e \approx 1 \times 10^{15}\text{ cm}^{-3}$ in the epitaxial layer. With a reduced doping concentration $C_e \approx 2 \times 10^{13}\text{ cm}^{-3}$ in the epitaxial layer, i.e. with the double-pin photodiode a BER

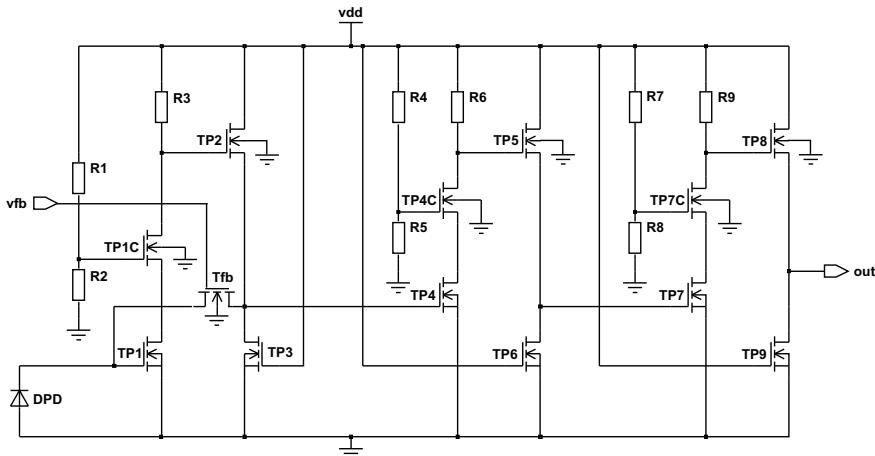


Fig. 6.132 Circuit schematic of the transimpedance amplifier with cascode and double photodiode in $0.8 \mu\text{m}$ -BiCMOS (p-substrate)

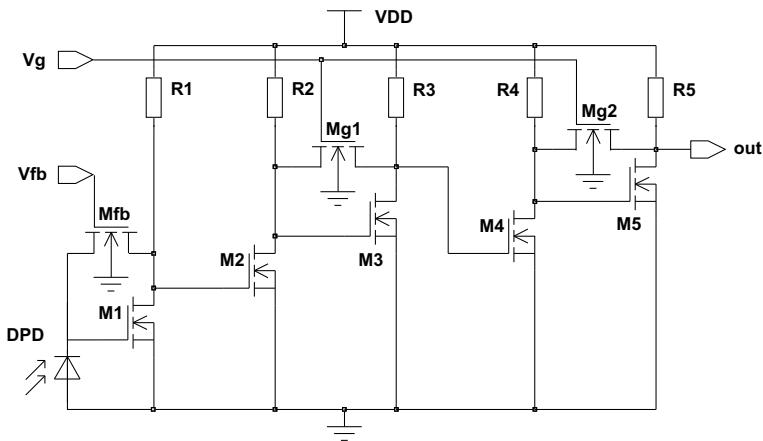
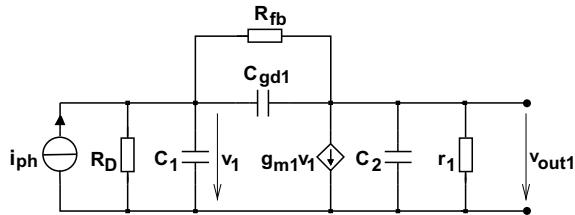


Fig. 6.133 Circuit diagram of interconnect receiver OEIC [142]

of 10^{-9} could not be achieved for 850 nm at a data rate of 622 Mb/s due to limited laser power. At a data rate of 531 Mb/s, however, a Q factor of 6.85 corresponding to a BER of 3.77×10^{-12} for an optical input power of about $180 \mu\text{W}$ was determined for 850 nm [128].

For the application in optical interconnects, OEICs implementing the double or double-pin photodiode were processed in a modular $0.8 \mu\text{m}$ BiCMOS technology, however only devices also present in the corresponding $0.8 \mu\text{m}$ CMOS technology were implemented [142]. The circuit diagram of the interconnect receiver OEICs is shown in Fig. 6.133.

Fig. 6.134 Small-signal equivalent circuit of the first amplifier stage [142]



Only N-channel MOSFETs with minimum channel lengths ($L=0.8\mu\text{m}$) were used in order to achieve a high data rate. The NMOS transistors M1–M5 operate in common source configuration (Fig. 6.133). The input stage with transistor M1 in transimpedance configuration converts changes in the photocurrent of the photodiode to voltage changes. The feedback resistor in the input stage is formed by the NMOS transistor Mfb. Two further stages with two transistors each are used as voltage amplifiers. The active feedback resistor in each of the two stages (Mg1, Mg2) limits the gain and therefore enhances the bandwidth.

In the following, expressions for the transimpedance and for the poles of the circuit will be presented. For that purpose the circuit is divided into three stages. The first stage is an inverter with NMOS transistor M1 and with resistor load R_1 . The feedback device Mfb with the value R_{fb} is connected between drain and gate of M1. The small-signal transimpedance can be calculated for the small-signal equivalent circuit shown in Fig. 6.134.

For a large value of the space-charge resistance R_D , which is justified for the integrated photodiodes with low leakage currents (for small-sized integrated silicon photodiodes: $R_D > 10^{10}\Omega$), the result for the low-frequency small-signal transimpedance of the first stage is [142, 143]:

$$\frac{v_{out1}}{i_{pd}} = \frac{1 - g_{m1} R_{fb}}{\frac{1}{r_1} + g_{m1}} , \quad (6.88)$$

with

$$r_1 = \frac{1}{g_{ds1} + \frac{1}{R_1}} .$$

For $g_{m1} R_{fb} \gg 1$ and $g_{m1} \gg \frac{1}{r_1}$, the transimpedance corresponds to the negative value of the feedback resistor R_{fb} . The value of the feedback resistor R_{fb} determines the ideal transimpedance of the input stage in a first approximation.

A calculation of the dominant pole, which can be assumed according to simulations, leads to [142, 143]:

$$\omega_{p1} = \frac{1 + g_{m1} r_1}{R_{fb} \left[C_1 \left(1 + \frac{r_1}{R_{fb}} \right) + C_{gd1} \left(1 + g_{m1} r_1 \right) + \frac{C_2 r_1}{R_{fb}} \right]} , \quad (6.89)$$

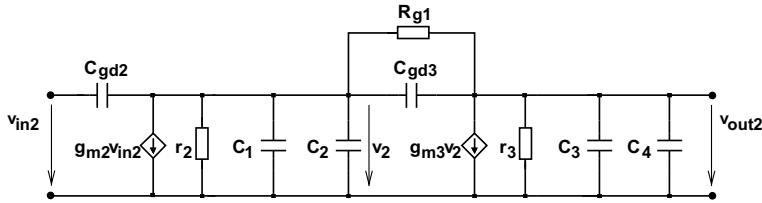


Fig. 6.135 Small-signal equivalent circuit of the second amplifier stage [142]

for the first stage with

$$C_1 = C_D + C_{gs1} + C_{sb,Mfb} + C_{gs,Mfb} \quad \text{and}$$

$$C_2 = C_{db1} + C_{L1} + C_{db,Mfb} + C_{gd,Mfb} ,$$

where C_D is the space-charge capacitance of the integrated photodiode and C_{L1} is the input capacitance of the second amplifier stage. From this expression for the dominant pole it can be seen easily that a larger value of R_{fb} for a larger transimpedance results in a lower bandwidth as one expects.

The second and third amplifier stages are constructed identically. They consist of two NMOS-resistor inverters each with a resistive feedback from the output of the second inverter to the input of the first inverter. The feedback resistors M_{g1} and M_{g2} with the values R_{g1} and R_{g2} , respectively, determine the voltage gain as well as the bandwidth of the second and third stage. Larger values of R_{g1} and R_{g2} result in a larger gain but also in a lower bandwidth. The choice of R_{g1} and R_{g2} by setting V_g , therefore, is a trade-off between a high bandwidth and a high transimpedance of the interconnect receiver OEIC. The low-frequency small-signal voltage gain A_{v2} of the second stage can be derived from the small-signal equivalent circuit shown in Fig. 6.135.

The following result is obtained [143]:

$$A_{v2} = \frac{v_{out2}}{v_{in2}} = \frac{g_{m2}(R_{g1}g_{m3} - 1)}{g_{m3} + \frac{1}{r_2} + \frac{1}{r_3} + \frac{R_{g1}}{r_2r_3}} \approx g_{m2} \left(R_{g1} - \frac{1}{g_{m3}} \right) \quad (6.90)$$

with

$$r_2 = \frac{1}{g_{ds2} + \frac{1}{R_2}} \quad \text{and} \quad r_3 = \frac{1}{g_{ds3} + \frac{1}{R_3}} . \quad (6.91)$$

Here, R_{g1} and g_{m2} are the major factors influencing the voltage gain. The transconductance g_{m3} of transistor M3, however, also should be made large in order to increase the voltage gain. The voltage gain of the third stage can be calculated correspondingly. The total or effective transimpedance of the receiver OEIC is the product of the transimpedance of the first stage and the voltage gains of the second and third stage. A value of 65 kΩ for the total transimpedance is estimated using (6.88) and

(6.90). The corresponding value obtained by numerical circuit simulation was $71\text{ k}\Omega$ [143].

The small-signal equivalent circuit of the second stage also can be used to determine its bandwidth under the assumption that a dominating pole exists [142, 143]:

$$\omega_{p2} = \frac{g_{m3} + \frac{1}{r_2} + \frac{1}{r_3} + \frac{R_{g1}}{r_2 r_3}}{\left(1 + \frac{R_{g1}}{r_3}\right) \left(C_{gd2} + C_{gd3} + C_1 + C_2\right) + \left(1 + \frac{R_{g1}}{r_2}\right) \left(C_{gd3} + C_3 + C_4\right) - 2C_{gd3}}, \quad (6.92)$$

with

$$\begin{aligned} C_1 &= C_{db2} + C_{gs3}, \\ C_2 &= C_{sb,Mg1} + C_{gs,Mg1}, \\ C_3 &= C_{db,Mg1} + C_{gd,Mg1} \quad \text{and} \\ C_4 &= C_{db3} + C_{L2}, \end{aligned}$$

where C_{L2} is the input capacitance of the third stage. The pole of the third stage can be calculated accordingly. Considering all three stages, a bandwidth of about 350 MHz can be estimated [142, 143].

An OEIC with the CN-well double photodiode having a size of $2700\text{ }\mu\text{m}^2$ and the circuit shown in Fig. 6.133 was fabricated in a $0.8\text{ }\mu\text{m}$ MOS technology. The active die area of the OEIC was $130 \times 70\text{ }\mu\text{m}^2$ and the OEIC consumed a current of 13 mA from $\text{VDD}=5\text{ V}$. The transient response of this DPD OEIC is presented in Fig. 6.136. A large voltage swing of 4 V is achieved for an optical input power of $200\text{ }\mu\text{W}$. A large-signal sensitivity of $20\text{ mV}/\mu\text{W}$ results from these values for the output voltage swing and for the optical input power. The effective large-signal transimpedance of $44.4\text{ k}\Omega$ for the amplifier can be obtained when we consider a realistic quantum efficiency of 90% for $\lambda=638\text{ nm}$ resulting in a photocurrent of the DPD of approximately $90\text{ }\mu\text{A}$ for an optical input power of $200\text{ }\mu\text{W}$. This value of $44.4\text{ k}\Omega$ is lower than the above estimated value of $65\text{ k}\Omega$ for the over-all small-signal transimpedance. This difference can be explained by a non-linear behavior for large signals. The value of $44.4\text{ k}\Omega$ for the large-signal over-all transimpedance, however, is a remarkably high value at the data rates achieved.

Let us note that the MOS amplifier topology is advantageous compared to bipolar amplifier topologies at high optical input power. High optical input powers can be handled without slowing down the maximum data rate since the MOS amplifier does not show saturation effects known from bipolar amplifiers. The MOS topology, therefore, allows a high dynamic range of the optical input power without a special limiter or automatic gain control circuit. The eye diagram of the interconnect DPD OEIC is shown in Fig. 6.137. The bit error rate of the DPD OEIC was determined for the NRZ data rates of 531 and 622 Mb/s in dependence on the optical input power. The results for the bit error rate (BER) are shown in Fig. 6.138. It can be seen from this diagram that the optical input power of -10.0 dBm is necessary for a bit error

Fig. 6.136 Transient response of a DPD OEIC with $\lambda = 638 \text{ nm}$, $C_e \approx 1 \times 10^{15} \text{ cm}^{-3}$, $V_{fb} = 4 \text{ V}$, $V_g = 4 \text{ V}$ and $P_{opt} = 200 \mu\text{W}$ [142]

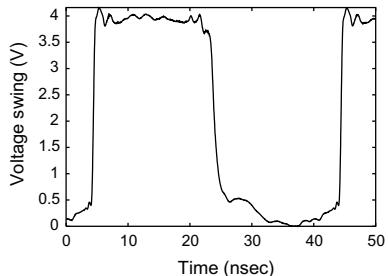


Fig. 6.137 Eye diagram of a DPD OEIC for a data rate of 622 Mbit/s with $\lambda = 638 \text{ nm}$, $C_e \approx 1 \times 10^{15} \text{ cm}^{-3}$, $V_{fb} = 4 \text{ V}$, $V_g = 4 \text{ V}$ and $P_{opt} = 200 \mu\text{W}$ (500 ps/div, 1 V/div) [128]

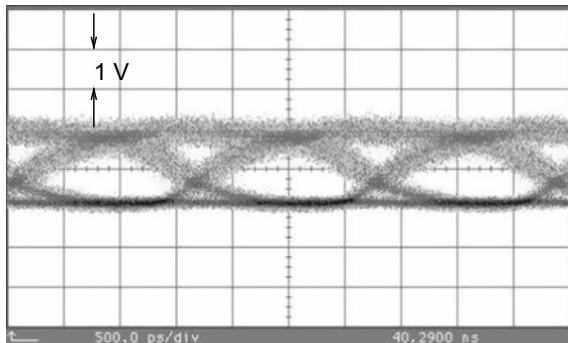
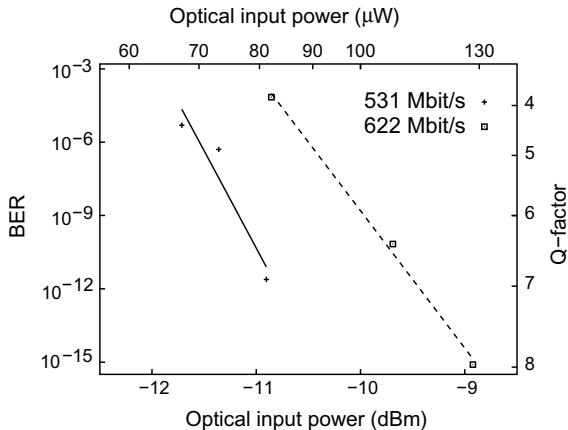


Fig. 6.138 Bit error rate (BER) of the DPD OEIC in dependence on the optical input power with $\lambda = 638 \text{ nm}$ and $C_e \approx 1 \times 10^{15} \text{ cm}^{-3}$ ($V_{fb} = 4 \text{ V}$, $V_g = 4 \text{ V}$) [128]



rate of 10^{-9} at the data rate of 622 Mb/s. At 531 Mb/s, the sensitivity of the DPD OEIC is -11.2 dBm for the same bit error rate. These values are very good results for an OEIC in a standard MOS technology with the standard doping concentration in the epitaxial layer of the order of 10^{15} cm^{-3} .

A PIN CMOS OEIC in $1.0 \mu\text{m}$ technology with improved properties has been presented [144] whereby the same PIN photodiode as in [101] has been used. For $\lambda = 850 \text{ nm}$ and for the standard epitaxial layer doping $C_e \approx 10^{15} \text{ cm}^{-3}$ with $|V_{PD}| = 3.0 \text{ V}$,

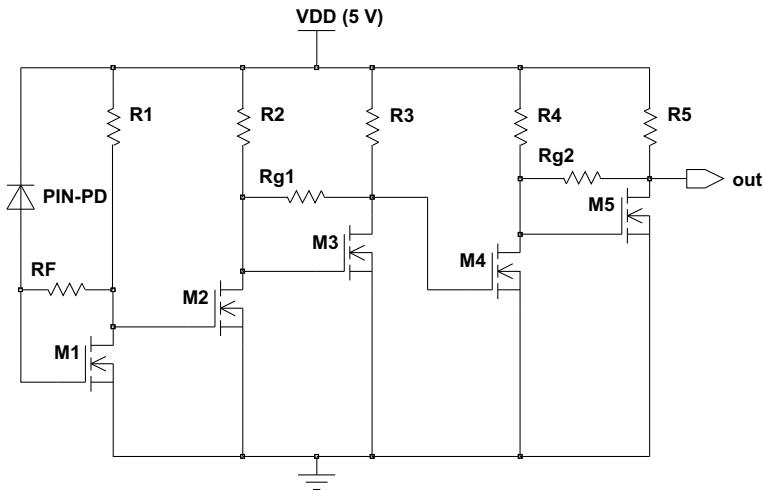


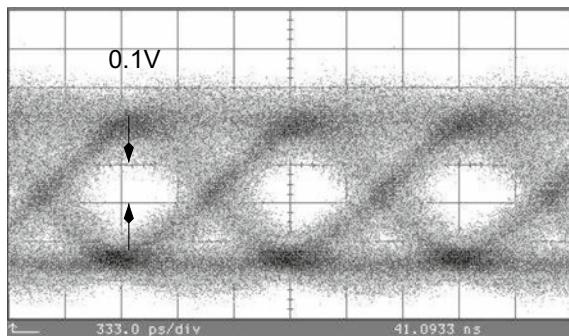
Fig. 6.139 Circuit diagram of a CMOS preamplifier OEIC with a possible data rate of 1 Gb/s for application in a fiber and interconnect receiver [144]

rise and fall times of 11.5 and 11.7 ns, respectively, were measured for the CMOS-integrated PIN photodiode. These large values for t_r and t_f are due to the slow diffusion of photogenerated carriers in the standard epitaxial layer of the photodiode. The corresponding values for $C_e = 2 \times 10^{13} \text{ cm}^{-3}$, where the depletion region spreads through the whole epitaxial layer and carrier diffusion in the photodiode is eliminated, were 0.55 and 0.67 ns, respectively, for $\lambda = 850 \text{ nm}$ [144]. These values for the rise and fall times were not corrected for the rise and fall times of the 850 nm light source and of the picoprobe.

The quantum efficiency for 638 nm was 47 and 44% for 850 nm without antireflection coating. A special antireflection coating (ARC) on the PIN photodiodes was optimized for $\lambda = 638.3 \text{ nm}$ resulting in a quantum efficiency of 94% for this wavelength [101]. The responsivity at 850 nm measured for the PIN photodiodes with this ARC is 0.49 A/W corresponding to a quantum efficiency of 71.8% [144]. A thicker antireflection coating optimized for 850 nm, however, will result in a larger quantum efficiency according to optical simulations. The quantum efficiency of the PIN photodiodes for $\lambda = 638.3 \text{ nm}$ would then be reduced of course [144].

The high-speed preamplifier circuit with an integrated PIN photodiode is shown in Fig. 6.139. Only n-channel MOSFETs with minimum channel lengths are used in order to achieve a high bandwidth. The transistors M1–M5 operate in common-source configuration. The input stage with M1 in transimpedance configuration converts changes in the photocurrent of the photodiode to voltage changes. The feedback resistor RF in the input stage is formed by gate polysilicon. Two further stages with two transistors each are used as voltage amplifiers. The polysilicon feedback resistor in each of the two stages (R_{g1}, R_{g2}) limits the gain and therefore boosts the bandwidth. A bandwidth of 480 MHz was simulated for the OEIC. Due to the

Fig. 6.140 Measured eye diagram of a $1.0\text{ }\mu\text{m}$ CMOS preamplifier OEIC for the application in a fiber and interconnect receiver (time: 333 ps/div , amplitude: 0.1 V/div) [144]



feedback resistors, a good independence from process deviations within the relatively large specified process tolerances of the used digital CMOS process is obtained. The sensitivity of the PIN preamplifier OEIC was $13.8\text{ mV}/\mu\text{W}$ without ARC, which corresponds to an overall transimpedance of $45.9\text{ k}\Omega$. Compared to [101], the sensitivity of the new OEIC has been increased by a factor of more than 2.5. Its power consumption was 22.5 mW at 5.0 V . The photodiode had an area of $2700\text{ }\mu\text{m}^2$. The preamplifier occupied an active area of $245 \times 140\text{ }\mu\text{m}^2$ due to the large area necessary for the resistors formed by low-resistivity (gate) polysilicon.

The rise and fall times measured at the OEIC output with the picoprobe were 0.78 and 0.76 ns , respectively, with a supply voltage of 5.0 V . The eye diagram measured at the OEIC output is shown in Fig. 6.140 for an NRZ data rate of 1 Gb/s with a PRBS of $2^{23}-1$. The higher data rate of this OEIC is due to less transistors in the preamplifier than in the typical high-frequency circuit with cascode transistors and source followers described in [101] and shown in Fig. 6.125. In [101], 12 NMOS transistors were used in the preamplifier, which therefore contained more parasitic capacitances. Here, the number of parasitic capacitances is considerably lower. In addition, the gain per amplifying transistor is lower here, allowing for a higher bandwidth of the new preamplifier.

The so-called Q-factor is defined as $(B_1 - B_0)/(\sigma_1 + \sigma_0)$ [145], where B_1 and B_0 are the mean values and σ_1 and σ_0 are the standard deviations of the output signal for a ‘1’ and ‘0’. B_1 , B_0 , σ_1 , and σ_0 can be determined from eye diagram measurements. The bit error rate (BER) then is available from $\text{BER} \approx \exp(-Q^2/2)/Q/\sqrt{2\pi}$ [145]. The BER of the OEIC has been determined with an HP54750/51 digital sampling oscilloscope for the NRZ data rates of 622 Mb/s and 1 Gb/s in dependence on the optical input power [144]. The results for the bit error rate are shown in Fig. 6.141. From this diagram for a $\lambda = 638\text{ nm}$ being especially interesting for data transmission over plastic optical fibers and for optical interconnects, it can be seen that the optical input power of -15.4 dBm is necessary for a BER of 10^{-9} at a data rate of 1 Gb/s . At 622 Mb/s , the sensitivity of the OEIC for the same BER is -17.2 dBm . The sensitivity for a BER of 10^{-10} at a data rate of 1 Gb/s is -14.8 dBm . The sensitivity for a BER of 10^{-11} at a data rate of 622 Mb/s is -16.5 dBm . For $\lambda = 850\text{ nm}$, a sensitivity

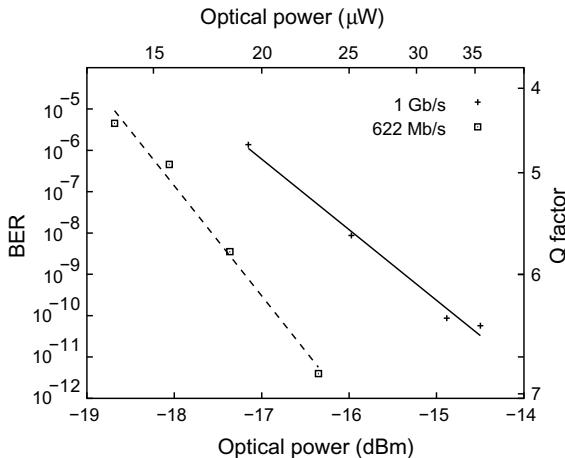


Fig. 6.141 Bit error rate in dependence on the optical input power of a $1.0\text{ }\mu\text{m}$ CMOS preamplifier OEIC for the application in a fiber and interconnect receiver [144]

Table 6.9 Comparison of the sensitivity of a PIN OEIC and of a DPD OEIC for a BER of 10^{-9}

λ (nm)	PIN OEIC without ARC (dBm @ Mb/s)	DPD OEIC with ARC (dBm @ Mb/s)
638	$-15.4 @ 1000^b$	$-10.0 @ 622^a$
638	$-17.2 @ 622^b$	$-11.2 @ 531^a$
850	$-15.3 @ 622^b$	$-7.6 @ 531^b$

^a $C_e \approx 1 \times 10^{15} \text{ cm}^{-3}$

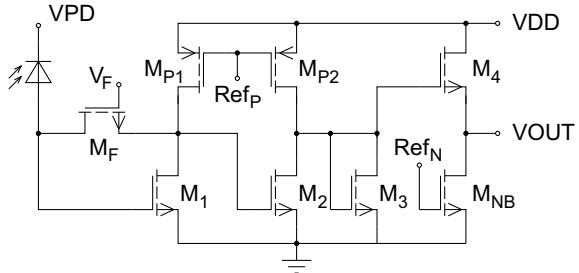
^b $C_e = 2 \times 10^{13} \text{ cm}^{-3}$

of -15.3 dBm for a BER of 10^{-9} at a data rate of 622 Mb/s has been verified. These values are very good results for an OEIC in a $1.0\text{ }\mu\text{m}$ CMOS technology.

The overall transimpedance of $46\text{k}\Omega$ and the data rate of 1Gb/s result in a $46\text{Tbit}\Omega/\text{s}$ transimpedance data rate product. With the simulated bandwidth of 480MHz a $23\text{THz}\Omega$ effective transimpedance-bandwidth product results which exceeds the value of $18\text{THz}\Omega$ reported in [96].

Table 6.9 summarizes the sensitivity results for the PIN CMOS OEIC. The results of an OEIC with a similar circuit and a double photodiode in a $0.8\text{ }\mu\text{m}$ CMOS technology [142] are included for comparison. Active feedback resistors for flexible adjustment of the sensitivity were implemented in this DPD OEIC instead of polysilicon feedback resistors (see Fig. 6.133). The DPD OEIC fabricated in a standard MOS technology achieved a data rate of 622 Mb/s at a quite good sensitivity value of -10 dBm for 638 nm [142]. A sensitivity of -7.6 dBm for 850 nm at a data rate of 531 Mb/s was verified for the DPD OEIC with a reduced epitaxial doping concentration $C_e = 2 \times 10^{13} \text{ cm}^{-3}$. It shall be mentioned that this sensitivity value for 850 nm can be improved by $2\text{-}3 \text{ dB}$ by optimizing the thickness of the antireflection coating for the wavelength of 850 nm . The sensitivity at 638 nm then would be

Fig. 6.142 Circuit diagram of a 130 nm CMOS OEIC [124]



reduced of course. It also has to be noted that the PIN CMOS OEIC was optimized whereas the DPD OEIC has not been redesigned.

The sensitivity of the PIN CMOS OEIC for a data rate of 1 Gb/s and a BER of 10^{-9} with a value of -15.4 dBm for 638 nm exceeds the sensitivity of -6.3 dBm of a $0.35 \mu\text{m}$ OEIC for 850 nm [134] by a factor of 8. Compared to an OEIC with a lateral PIN photodiode [117] the sensitivity was increased by a factor of 4. It shall be mentioned that the implementation of an antireflection coating will improve the sensitivity of the OEICs by a value of 2–3 dBm. The minimum sensitivity of -17 dBm specified in the Gigabit Ethernet networking standard, therefore, should be achievable with PIN CMOS OEICs [144].

The data rate of the PIN CMOS OEICs has been limited by the amplifier in a $1.0 \mu\text{m}$ technology. With sub-micrometer PIN-CMOS-OEICs, however, data rates in excess of 1 Gb/s are possible.

An OEIC in a 130 nm unmodified CMOS process flow on SOI wafers with a $2 \mu\text{m}$ thick Si film was reported recently [124]. The resistivity of the Si film was larger than $10 \Omega\text{cm}$. Since the thickness of the SOI film was larger than the SOI film thickness of 100 nm used for the SOI-CMOS process, the transistors essentially had the performance of bulk devices. The P⁺ and N⁺ drain/source regions were used for the anode and cathode stripes of lateral PIN photodiodes in the $2 \mu\text{m}$ thick Si film. Due to the only $2 \mu\text{m}$ thick Si film, the external quantum efficiency was about 10% for a wavelength of 850 nm [124]. The total area of the photodiodes was $2500 \mu\text{m}^2$, whereby the electrode width and spacing was varied. The electrodes of the lateral PIN photodiode were salicided to reduce their series resistance. The integration process was performed to the first copper level [124].

The NMOS transistor had a saturation transconductance of 550 mS/mm for a width/length ratio of 1/0.175 and a threshold voltage of 0.330 V . The cutoff frequency f_T of this transistor was 60 GHz . The P-channel transistor had a cutoff frequency of 40 GHz [124]. These values make them attractive for Gb/s-electronics.

The circuit diagram of the CMOS transimpedance amplifier used in the SOI OEIC is shown in Fig. 6.142. A PMOS load M_{P1} is used for the NMOS transistor M_1 in the transimpedance input stage. The output voltage of this input stage is amplified by a second stage with M_2 and M_{P2} . A diode load (M_3) is used for this stage to limit the gain and boost the bandwidth. A source follower (M_4) with its current source M_{NB} is used at the output. A 1 GHz design and a 3 GHz design was made for the circuit shown

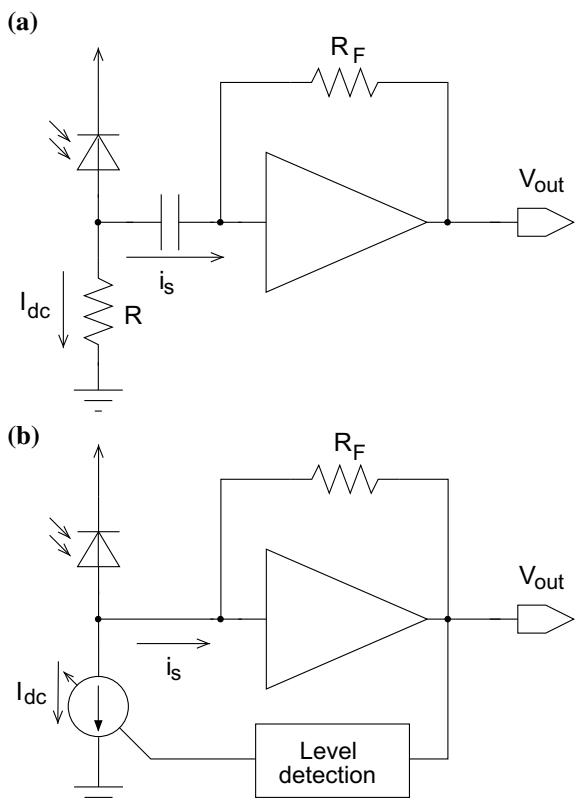
in Fig. 6.142 [124]. The 1 GHz design achieved a sensitivity of -19 dBm at 1 Gb/s for a PRBS of $2^7 - 1$. The 3 GHz design achieved maximum sensitivities of -16.6 , -15.4 , -10.9 , 0.9 , and 2 dBm at 2, 3.125, 5, 6, and 8 Gb/s, respectively, for a BER of 10^{-9} with a wavelength of 850 nm. It was stated that the receiver characteristics were measured with a circuit supply voltage VDD of 3.2 V [124]. The photodetector bias was 24 V for the mentioned performance [124]. It was reported that single supply 3 V operation was possible up to 3.125 Gb/s. A penalty of 0.5 dB was incurred for a PRBS of $2^{31} - 1$ [124]. The total dissipated power was 10 mW for the 1 GHz design and 35 mW for the 3 GHz design [124].

6.4.14 Receiver for Wireless Infrared Communication

Certain applications as for instance wireless infrared data communication require rejection of photocurrents generated by ambient light. Variable gain transimpedance amplifiers are also required for this application. In [146] a preamplifier with a 70 MHz bandwidth, a dynamic range of 77 dB, and a maximum transimpedance gain of $19 \text{ k}\Omega$ was presented, whereby the bandwidth was controlled within a factor of two over a 31-dB variation in gain. Free-space infrared (IR) wireless data links in laptop computers, computer peripherals, and digital cameras pushed new developments in optical receiver design. Such wireless communications emphasize system integration and low cost. Commercial digital CMOS consequently is preferred over higher-speed technologies such as GaAs or bipolar, especially since high speed is not required and is not possible since large-area photodiodes are required. Current Infrared Data Association (IrDA) standards support 4 Mb/s [147] and future standards for data rates of 100 Mb/s are being investigated [146]. A wide dynamic range is essential in order to accommodate variable link distances. In situations where the signal is weak, the photocurrent generated by ambient light can overwhelm the signal. IrDA standards specify a maximum ambient light level being more than 100 times larger than the minimum signal. The inherent dynamic range of fixed-transimpedance amplifiers is typically not sufficient for an IR wireless receiver.

A technique placing a variable signal attenuator before the preamplifier [148, 149] has been described. A bipolar differential pair as a current attenuator was used. Bipolar transistors are necessary in this technique because their exponential voltage-to-current characteristics ensures a well-regulated photodiode bias voltage across many orders of magnitude. Varying the preamplifier gain [150, 151] poses its own problems. Reported variable-gain transimpedance amplifiers based on traditional designs are difficult to stabilize [150, 151]. In [146] a two-stage differential transimpedance amplifier was presented whose stability depends only on the tracking of identical pairs of resistors. In contrast to the designs reported in [150, 151], the bandwidth of this amplifier is well controlled over the entire gain range. A controlled bandwidth improves the sensitivity by rejecting out-of-band noise without additional filtering.

Fig. 6.143 Ambient photocurrent rejection technique with **a** a passive RC network and with **b** an active feedback loop [146]

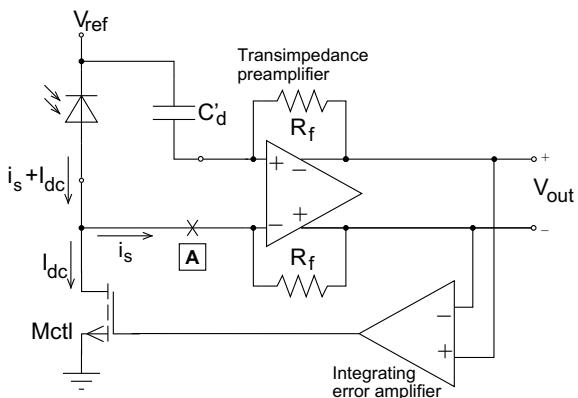


For rejecting ambient light at the preamplifier, there are two main alternatives. The first possibility is to place a high-pass resistance-capacitance (RC) network at the input of the preamplifier (see Fig. 6.143a, [149, 152, 153]). The high-frequency signal current i_s passes through while the dc part I_{dc} is blocked and shunted away by resistor R . This solution has two major drawbacks. Large on-chip resistors and capacitors are required to obtain a sufficiently low cut-off frequency and the photodiode bias varies with the ambient light intensity reducing the bandwidth for a high ambient light level.

The second possibility is to use an active feedback loop as shown in Fig. 6.143b. Peak level detection is effective [154, 155], but assumes that the average current is constant and requires a reset mechanism. Alternatively, average level detection can be applied [85]. The structure described in [146] represents another solution, where the feedback loop does not impose constraints on the design of the transimpedance amplifier. The ambient light-rejection circuit shown in Fig. 6.144 requires a low chip area and effectively regulates the photodiode bias voltage.

The transimpedance amplifier converts the current from the photodiode into a differential voltage. The rejection circuit formed by the error amplifier and transistor

Fig. 6.144 Optical preamplifier with ambient photocurrent rejection [146]



M_{ctl} operates as follows: The dc component of the photocurrent produces an offset in the average levels of the differential outputs. This offset is integrated over time by the error amplifier. Transistor M_{ctl} acts as a variable-current sink which eliminates the average photocurrent I_{dc} at steady state. The average photocurrent consists of the ambient photocurrent and the dc component of the signal. The differential signal path allows a high immunity to noise from the power supply and substrate. The photodiode, however, can only be connected to one terminal creating an unsymmetry at the input of the differential structure. Therefore, an additional capacitor C'_d is required at the other input of the transimpedance amplifier to match the photodiode capacitance and to rebalance the circuit [146]. Perfect matching ensures that noise injected at the bias voltage V_{ref} appears as a common-mode signal that is rejected effectively by the differential structure.

To study the characteristics of the ambient photocurrent rejection circuit, we can break the loop at point A in Fig. 6.144. The feedback loop is effective at low to midband frequencies where the loop gain is given by:

$$L(s) = A_{\text{tmp}} A_{\text{err}}(s) g_{\text{mctl}} \quad (6.93)$$

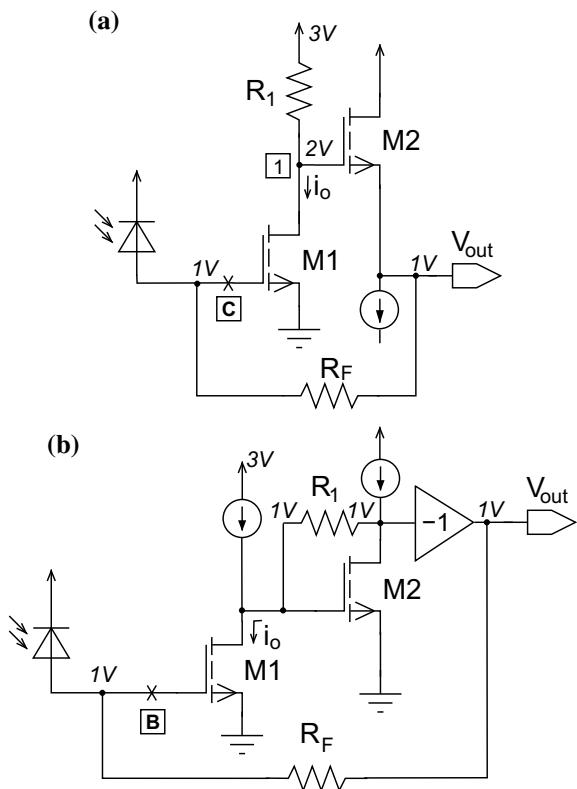
with A_{tmp} being the passband gain of the transimpedance amplifier and g_{mctl} the transconductance of M_{ctl} . The gain of the error amplifier $A_{\text{err}}(s)$ has a dominant-pole response

$$A_{\text{err}}(s) = \frac{A_{\text{dc}}}{1 + s/\omega_{\text{p1}}} \quad (6.94)$$

with A_{dc} being the dc voltage gain, and ω_{p1} the dominant pole frequency. The closed-loop response of the preamplifier with ambient light rejection is

$$\frac{v_{\text{out}}(s)}{i_s} = \frac{A_{\text{tmp}}}{1 + L(s)} \approx A_{\text{tmp}} \times \frac{s + \omega_{\text{p1}}}{s + A_{\text{tmp}} A_{\text{dc}} \omega_{\text{p1}} g_{\text{mctl}}} \quad (6.95)$$

Fig. 6.145 Traditional a and in [146] proposed b transimpedance amplifier

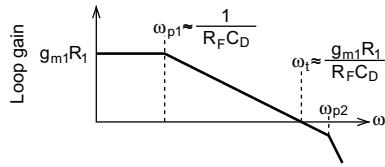


where the zero located at $\omega = \omega_{p1}$ is much lower in frequency than the pole at $\omega = A_{\text{imp}} A_{\text{dc}} \omega_{p1} g_{\text{mctl}}$. The preamplifier, therefore, exhibits a high-pass response with a cut-off frequency $\omega_{\text{HP}} = A_{\text{imp}} A_{\text{dc}} \omega_{p1} g_{\text{mctl}}$, a passband gain A_{imp} , and a dc gain $1/A_{\text{dc}} g_{\text{mctl}}$. g_{mctl} is proportional to $\sqrt{I_{\text{dc}}}$. Therefore, both the preamplifier's dc gain and high-pass cutoff frequency increases and the dc gain decreases with increasing I_{dc} [146].

An adequate phase margin is required for stability of the feedback loop. The error amplifier has to be compensated so that ω_{p1} is low enough for maximum values of A_{imp} and g_{mctl} [146] (see (6.93)). An upper limit to the transconductance g_{mctl} can be set by limiting the gate voltage of M_{ctl} . Accordingly a maximum current in M_{ctl} results, which must be larger than the current generated by the photodiode under the brightest ambient light conditions.

As mentioned above, variable-gain transimpedance amplifiers are difficult to stabilize. Figure 6.145a shows the traditional transimpedance amplifier with transistor M1 in common-source configuration and a source follower M2 to obtain a lower output impedance. Figure 6.145b shows the transimpedance amplifier proposed in [146]. The main difference is transistor M2 in common-source and in shunt-feedback configuration. This structure was proposed in [156, 157] for fixed-gain preamplifiers.

Fig. 6.146 Frequency plot of loop gain [146]



The three-stage amplifier in Fig. 6.145b consists of a transconductance first stage, a transimpedance second stage, and an output stage for small-signal inversion. The overall voltage gain of the amplifier is [146]

$$A = -\left(\frac{v_{out}}{i_0} \frac{i_0}{v_{in}} (-1)\right) \approx g_{m1}R_1 \quad . \quad (6.96)$$

The same result is obtained for the traditional design assuming unity gain for the output source follower.

The stability of these circuits can be investigated by breaking the feedback loops at points B and C. Figure 6.146 shows the behavior of the loop gain of both circuits.

The TIA unity-gain frequency is approximately

$$\omega_t \approx \frac{A}{R_F C_D} \approx \frac{g_{m1} R_1}{R_F C_D} \quad (6.97)$$

The stability of the amplifiers is determined by the relative position of ω_t to the non-dominant pole ω_{p2} . According to (6.97), ω_t increases when R_f reduces. The non-dominant pole, however, is not significantly affected by R_F . Gain-peaking at high frequency occurs when ω_t comes too close to ω_{p2} . To avoid this, ω_t should track changes of R_F . Especially when resistor R_1 could track R_F (see (6.97)), ω_t would remain constant and stability would be guaranteed. The bandwidth BW of the transimpedance amplifiers is approximately

$$BW \approx \frac{1 + A}{R_F C_D} \approx \frac{g_{m1} R_1}{R_F C_D} \approx \omega_t \quad (6.98)$$

R_1 following R_F is also the condition to maintain a constant bandwidth. This tracking is difficult in the traditional circuit [146, 150, 151]. The structure shown in Fig. 6.145b, however, allows this tracking because R_1 is used as a shunt feedback resistor similar to R_F . Both resistors have essentially the same terminal voltages, with one terminal biased at $V_{GS1,2}$ and the other terminal connected to the output. Both, R_1 and R_F , therefore, can be realized as MOSFETs of the same type. Although R_1 and R_F can be designed to track to any fixed ratio, the design in [146] was simplified by making $R_1 = R_F$.

The optimization of the bandwidth makes a small-signal analysis necessary. The small-signal model is shown in Fig. 6.147. C_f is the shunt feedback capacitance

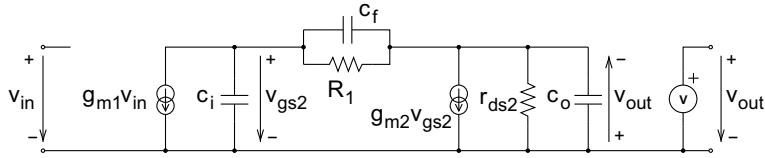
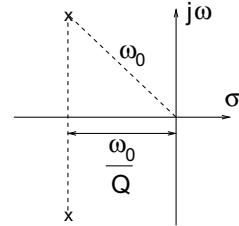


Fig. 6.147 Small-signal model of 3-stage amplifier [146]

Fig. 6.148 Illustration of complex poles [146]



across the gate and drain of transistor M2, C_i and C_o are the total capacitances at the internal node and output node, respectively.

Due to the capacitances C_i and C_o , the second stage exhibits a second order response. Assuming $g_{m2} \gg 1/r_{ds2}$ and $1/R_F$, and $C_F \ll C_o$ the frequency response is approximately [146]:

$$A(s) = \frac{v_{\text{out}}}{v_{\text{in}}}(s) \approx -\frac{g_{m1}}{C_i C_o} \frac{s C_f + (1/R_1 - g_{m2})}{s^2 + \frac{g_{m2} C_f}{C_i C_o} s + \frac{g_{m2}}{C_i C_o R_1}}. \quad (6.99)$$

By choosing C_f correctly, the poles of this transfer function can be made complex (see Fig. 6.148), leading to the following design equations:

$$\omega_0 \approx \sqrt{\frac{g_{m2}}{C_i C_o R_1}} \quad (6.100)$$

$$Q \approx \frac{1}{C_f} \sqrt{\frac{C_i C_o}{g_{m2} R_1}} \quad (6.101)$$

Commonly, a variable-gain transimpedance amplifier is optimized for a desired bandwidth at its maximum gain. At lower gain settings, only the stability of the circuit has to be confirmed. As one possible way to design the circuit in Fig. 6.145b, the start with the second stage was described in [146]. For a given bandwidth, the maximum value of R_1 can be determined from (6.100) by estimating the values of g_{m2} , C_i , and C_o , based on device geometry and power dissipation, and by choosing a nondominant pole frequency ω_0 sufficiently higher than ω_t (e.g. $\omega_0 \approx 2\omega_t$) [146]. The value of C_f corresponding to a desired Q-factor (e.g. $1/\sqrt{2} = 0.71$ for a flat response

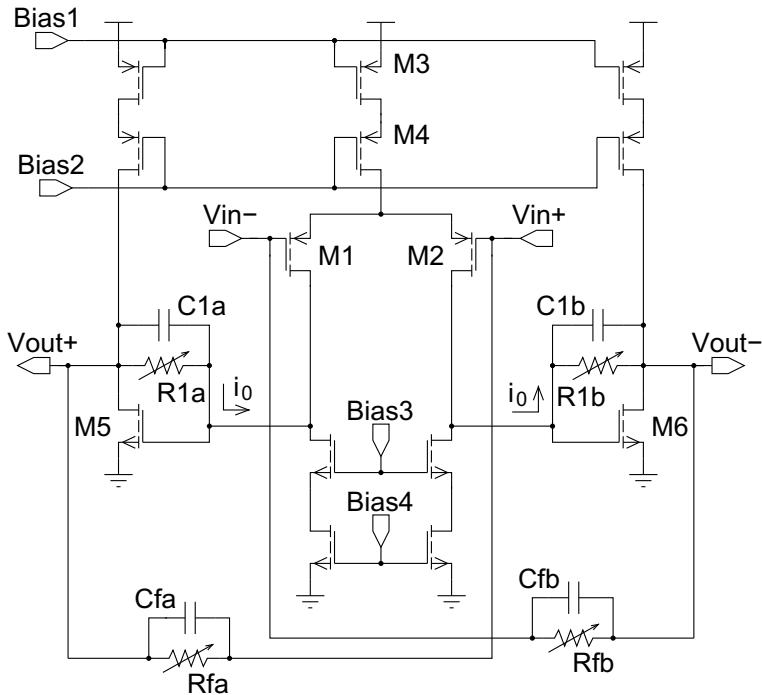


Fig. 6.149 Fully differential CMOS variable-transimpedance amplifier [146]

[158]) then can be found using (6.101). For a given photodiode capacitance C_D and estimating g_{m1} , (6.97) then determines the maximum value of R_F .

Figure 6.149 shows the differential version of the variable-gain transimpedance amplifier. The transconductance first stage is here realized by a P-channel differential pair M1/M2, allowing to place the input transistors into an isolated N well to reduce substrate noise at the expense of a slightly larger thermal noise [96]. The NMOS transistors M_5 and M_6 bias each output at about 1 V. The inverting buffer shown in Fig. 6.145b in the single-ended design is eliminated in the differential version. Small-signal inversion is here achieved by simply cross coupling the differential outputs.

The dynamic range is the ratio of the noise floor of the amplifier to its maximum input current. The maximum signal current is limited to half of the tail current of the input differential pair.

A test chip with a bandwidth of 70 MHz for demonstration of a 100 Mb/s link was implemented in a 0.35 μm CMOS technology [146]. An input capacitance of 5 pF being typical for large photodiodes used in IR wireless receivers was assumed. The maximum possible photocurrent due to ambient light was 30 μA . This value corresponds to a 10 mm² silicon photodiode in direct sunlight. The maximum high-pass cutoff frequency was 1 MHz. A value of 1 MHz is low enough for a 100 Mb/s

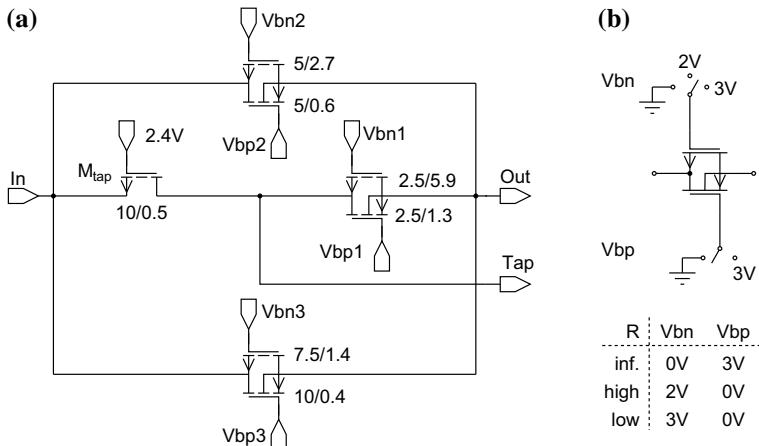


Fig. 6.150 Pass-transistor array (**a**) used to implement variable resistors and detail of pass transistor (**b**). The W/L dimensions are given in units of micrometers [146]

non-return-to-zero (NRZ) signal with a certain run-length limiting to prevent the transmission of long strings of 1's or 0's [146]. The tail current of the transimpedance amplifier's input differential pair was set to $800\,\mu\text{A}$ to keep the power dissipation below $10\,\text{mW}$. The maximum input current, therefore, was $400\,\mu\text{A}$. The gains of the variable-transimpedance amplifier ranged from $20\,\text{k}\Omega$ ($86\,\text{dB}\Omega$) down to $500\,\Omega$ ($54\,\text{dB}\Omega$) corresponding to a gain interval of $32\,\text{dB}$ [146].

The four variable resistors of the differential transimpedance amplifier were identical. To realize the mentioned gain range, each resistor consisted of three pairs of pass transistors (see Fig. 6.150). Three differently scaled pass transistors with three settings each were implemented, i.e. $3^3 = 27$ different resistance values were possible. To maximize the linearity, complementary N- and P-channel transistors were used, and the N wells of the P-channel transistors were tied to the outputs of the array to eliminate the back-gate effect. A speed penalty of about 40% was mentioned in [146] due to the N-well capacitance. The transistor M_{tap} acts as a series resistor. By connecting the error amplifier to the middle tap terminal (see Fig. 6.150a) instead of from the output, the loop gain of the ambient photocurrent rejection circuit was reduced, thereby lowering the high-pass cutoff frequency [146].

The test chip occupied an area of 1.44 mm^2 . The error amplifier was a common 2-stage CMOS OPAMP with a 5 pF internal compensation capacitor [146]. Its simulated dc gain was 94 dB and it had a dominant pole at 150 Hz . Measurements showed a maximum transimpedance gain of $19\text{ k}\Omega$ and a gain range of 31 dB . Over the gain range, the measured bandwidth varied from 85 to only 103 MHz . A total input-referred noise current of 56 nA was present at the maximum gain. With this noise floor and a maximum input current of $400\text{ }\mu\text{A}$, the preamplifier had a dynamic range of 77 dB (38.5 dB optical) [146]. The preamplifier consumed an electrical power of 8 mW at 3 V .

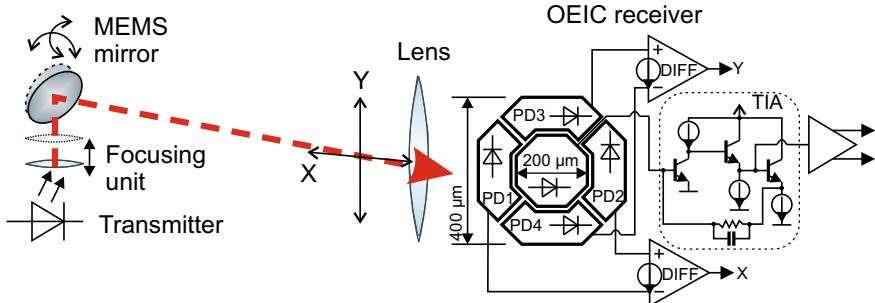


Fig. 6.151 OWC principle and block diagram of receiver OEIC with simplified TIA circuit

6.4.15 OWC Receivers and Experiments with Visible Light

OWC with PIN Photodiode Receiver

A pin photodiode receiver in a modular $0.35\text{ }\mu\text{m}$ PIN photodiode CMOS technology (see Fig. 2.28) with a npn-transistor module, i.e. in a BiCMOS technology, was developed for application in an optical wireless communication (OWC) system. The OWC principle and the receiver OEIC are depicted in Fig. 6.151 [159]. A narrow optical beam, obtained with a focusing unit, and beam steering with a MEMS mirror allow line-of-sight OWC over a wide distance with a total field of view of 21.6° each in x- and y-direction. First a wide beam can be used to find the receiver in a short time (using e.g. a Bluetooth feedback channel or a camera and image recognition [160]). Then the signals from the four satellite photodiodes can be used to focus and center the beam to the fast central detector. A receiver lens was used (limiting the total receiving angle to 9°). A transimpedance amplifier (TIA) exploiting npn transistors amplified the signal from the fast central pin photodiode. Two differential amplifiers processed the signals from the two opposite satellite photodiodes each.

The fast receiver channel with the npn-transistor TIA achieved a -3 dB bandwidth of 2.1 GHz , which is larger than the pin photodiodes bandwidth of 1.0 GHz , due to a certain peaking of the emitter followers at high frequencies. The substrate potential VSUB was at -7.5 V , leading to a reverse voltage across the pin photodiode of about 8.3 V ($\text{VSUB} + \text{base-emitter voltage}$). This negative substrate potential was possible, because the deep n-well of the triple-well (Bi)CMOS process was used to isolate the p-well of the n-channel MOSFET from the p-type substrate (and because the collector-substrate breakdown voltage of the npn transistor was much larger). For 3 Gb/s data rate the sensitivity of -23.4 dBm was obtained [159].

Each of the two differential TIAs consisted of a current comparator exploiting a PMOS current mirror with M1 and M2 (see Fig. 6.152) and a transimpedance amplifier. The difference in the photocurrents of PD1 and PD2 flows across RF ($100\text{ k}\Omega$) and generates an output voltage being proportional to the difference of the two photocurrents. The transimpedance amplifier was formed by a two-stage CMOS Miller OTA. The equivalent input noise current of these differential TIAs was 1.3 nA .

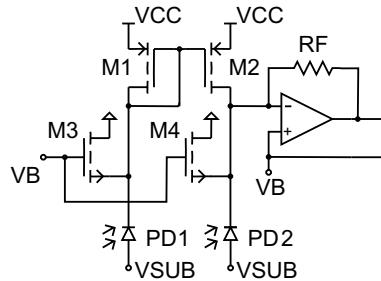


Fig. 6.152 Circuit of differential TIAs

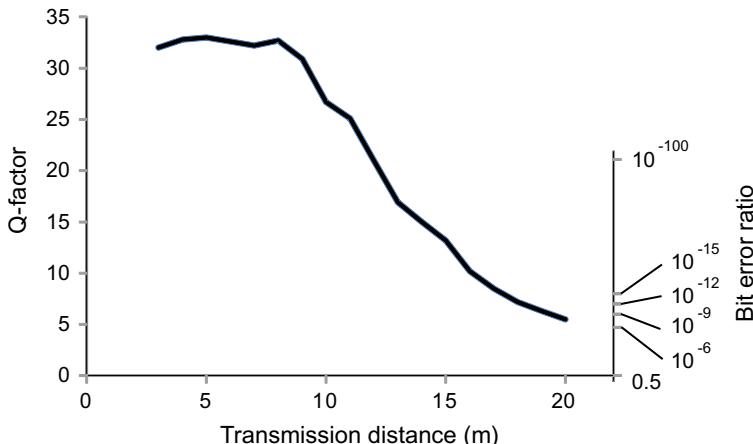


Fig. 6.153 Q-factor and BER over distance

at a bandwidth of 1.6 MHz. The differential TIA was designed for photocurrent differences up to $\pm 15 \mu\text{A}$. For higher photocurrents due to strong background light, the drain potentials of M1 and M2 would go below VB ($V_{\text{CC}} = 3.3 \text{ V}$, $V_B = 1.5 \text{ V}$), in worst case even down to negative values (i.e. to almost $V_{\text{SUB}} = -7.5 \text{ V}$). In such a way the maximum drain-source and gate-source voltages of M1 and M2 could be violated. To exclude this danger, M3 and M4 are inserted as voltage clamps, which take over the photocurrents when the drain potentials of M1 and M2 fall below $V_B - V_{\text{THn}}$, where V_{THn} is the threshold voltage of M3 and M4. In such a way M3 and M4 exclude negative potentials for the drains of M1 and M2.

Figure 6.153 shows the Q-factor and the bit error ratio versus transmission distance at 3 Gb/s. A transmission distance of 19 m was possible with a BER below 10^{-9} for a PRBS of $2^{31} - 1$ [159]. For distances of 18 m and less, the BER was better than 10^{-12} .

Another kind of application was aimed at in [161]. A very-high-data-rate receiver was necessary for a special optocoupler to be used in electron-beam lithography with

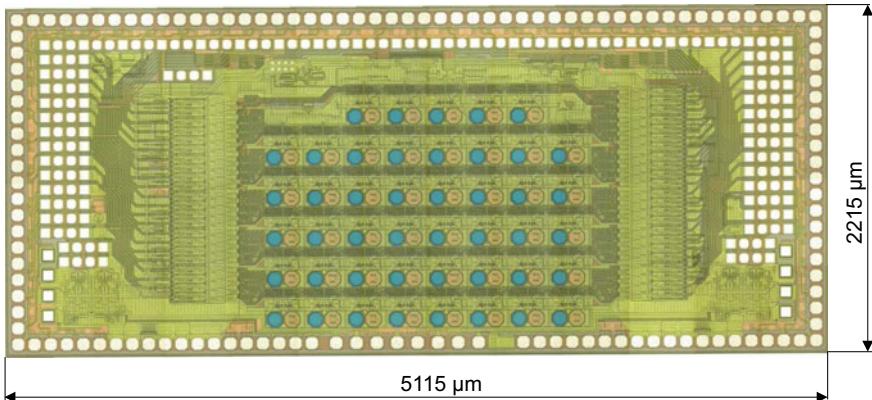


Fig. 6.154 Chipphoto of 45-channel receiver

massive parallel electron beams for maskless lithography in production of ASICs in low volumes. Focused light beams from an array of VCSELs were directed through a glass window into the ultra-high vacuum of the electron-beam equipment. Therefore, the optical receiver had to operate at a temperature of 85 °C, because of missing convection cooling. A 36-channel receiver was fabricated in 0.6 μm BiCMOS with integrated PIN photodiodes (see Sect. 2.3.2 [31]). A fully differential structure with a metal layer above the dummy photodiodes shielding them against light incidence was implemented to keep the crosstalk between the channels small. The photodiodes with a diameter of 90 μm had a pitch of 250 μm in x- and y-directions. Their responsivity was 0.33 A/W at 850 nm. This OEIC had a total power consumption of 809 mW including laser driver for a return channel and a LOP (loss of power) detector. Thanks to the differential topology, the crosstalk between channels was below -40 dB. Each channel achieved a sensitivity of -19.3 dBm (corrected for an extinction ratio of infinity) at a data rate of 3 Gb/s with 850 nm light, BER = 10^{-9} , and PRBS = $2^{15} - 1$. The total data rate of the 36-channel receiver was 108 Gb/s [161]. A negative substrate bias and an equalizer functionality were essential to achieve such a high data rate at such a long wavelength with a large penetration depth into silicon.

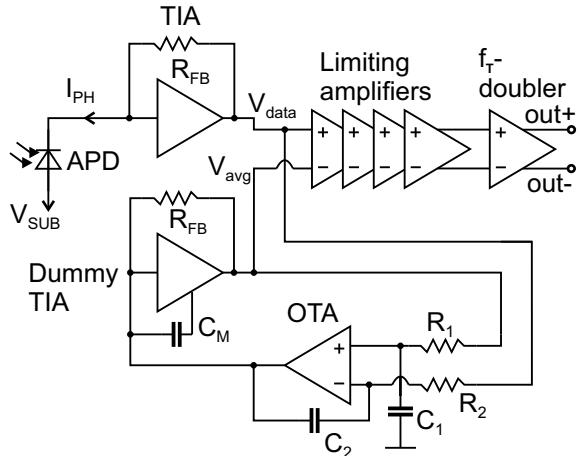
Later, a 45-channel version with 3.125 Gb/s in each channel achieving a total data rate of 140 Gb/s [162] was designed and fabricated also in 0.6 μm BiCMOS technology. Figure 6.154 shows the chip photo of the 45-channel receiver. It dissipated less than 950 mW with about 20 mW in each channel inclusive 50 Ω output driver and its operating temperature was up to 100 °C.

The sensitivity of a channel at 3.125 Gb/s was -20 dBm for 670 nm and -17.5 dBm for 850 nm with PRBS7 and BER = 10^{-9} . The crosstalk between the channels was less than -42 dB [162].

OWC with APD Photodiode Receivers

The pin-photodiode receiver in 0.35 μm BiCMOS (see Fig. 6.151) achieved a data rate of 3 Gb/s over 19 m distance, however, with a limited receiving angle of 9° due

Fig. 6.155 Block diagram of high-speed receiver



to the lens used at the receiver side [159, 163]. In order, to increase the receiving angle, the lens was omitted and an avalanche photodiode (APD) was implemented to compensate for the missing optical gain of the lens and to still achieve a large transmission distance. A high-voltage CMOS process was chosen to allow for a high reverse bias of the APD. The APD described in Sect. 2.2.12 and shown in Fig. 2.43 was applied in the $0.35\text{ }\mu\text{m}$ HV-CMOS receiver IC [164]. Figure 6.155 shows the block diagram of the high-speed channel of this receiver. The differential approach with the TIA and the dummy TIA reduces the sensitivity to substrate noise and power supply noise. The dummy TIA is a replica of the TIA. The only difference is that in the dummy TIA a capacitance C_M is added between gate and drain of the input transistor to reduce the bandwidth and the noise contribution of the dummy TIA. The dummy TIA generates the second input voltage V_{avg} of the differential limiting amplifier with the help of R_1 , R_2 , C_1 , C_2 , and the OTA acting as proportional integral controller. A transit-frequency doubler is used as 50Ω output driver to drive the measurement equipment.

Figure 6.156 shows the folded-cascode TIA. Folding the cascode allows to use a larger drain-source saturation voltage, which reduces the width of M1 and M2 leading to smaller parasitic capacitances compared to an unfolded cascode. The feedback resistor had a value of $3.7\text{ k}\Omega$ [164]. C_{FB} had a value of 33 fF . The TIA drew 3 mA at a supply voltage of 3.3 V . The postamplifier had a gain of 34.9 dB . The transit-frequency doubler circuit is also depicted in Fig. 6.156. This f_T doubler increased the bandwidth of this output driver stage because its input capacitances are only one half of C_{GS1} and one half of C_{GS4} , which result from the series connection of C_{GS1} and C_{GS2} seen from the input V_{in1} and from the series connection of C_{GS4} and C_{GS3} seen from the input V_{in2} , respectively.

The OWC receiver had four satellite photodiodes (simple PN-junction diodes as described in [165]) to allow centering of the beam on the APD of the high-speed channel. Two differential TIAs (Diff-TIAs) amplified the signal of two opposite PN

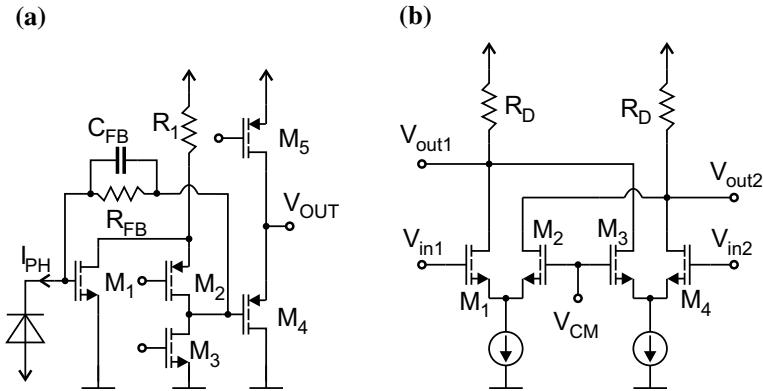
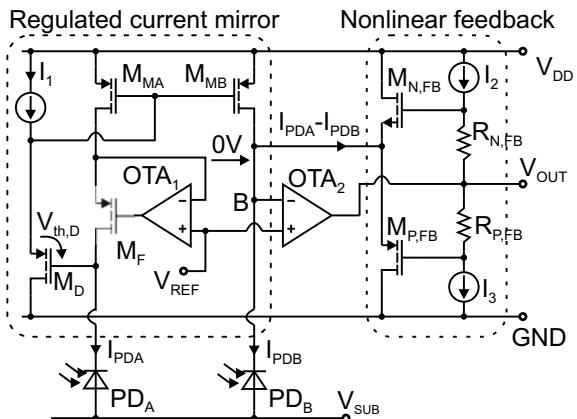


Fig. 6.156 Simplified circuit diagrams of folded-cascode TIA (a) and transit-frequency doubler (b)

Fig. 6.157 Circuit of highly sensitive differential TIA



photodiodes, each. Figure 6.157 shows the simplified circuit diagram of one highly sensitive differential TIA. To suppress background light, a current mirror topology and nonlinear feedback were used [164]. The nonlinear differential TIA is formed by a current mirror, an OTA and nonlinear feedback. The current mirror transistors M_{MA} and M_{MB} were implemented in 8-fold common-centroid layout to reduce their mismatch. The photocurrent of diode PD_A is mirrored to diode PD_B (located opposite of each other in the array) and therefore the magnitude of ($I_{PD_A} - I_{PD_B}$) flows into or out of the nonlinear feedback circuit, which exploits a push-pull stage with $M_{N,FB}$ and $M_{P,FB}$. These two transistors operate in the subthreshold region, i.e. they obey exponential behavior. The current sources I_2 and I_3 together with $R_{N,FB}$ and $R_{P,FB}$ set the initial operating point of the feedback transistors. A logarithmic function of $V_{OUT}(I_{PD_A} - I_{PD_B})$ results due to OTA2 [164]. In order to avoid systematic deviations between the drain-source voltages of M_{MA} and M_{MB} , the drain potential of M_{MA} is regulated to V_{REF} by OTA1 (node B and therefore the drain potential of M_{MB} is at

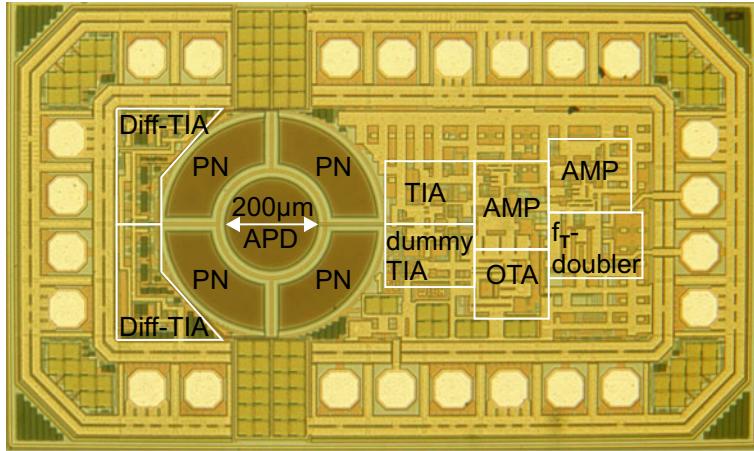


Fig. 6.158 Microphotograph of HV-CMOS OWC receiver

V_{REF} thanks to OTA2, zero offset voltage assumed). Thanks to connecting the gates of M_{MA} and M_{MB} to the source of M_D a wide control range was enabled [164]. The dynamic range for photocurrents from background light was larger than 10^7 from pA to several tens of μA . Figure 6.158 shows the chip photo of the OWC $0.35\text{ }\mu\text{m}$ HV CMOS APD receiver with an area of $1615 \times 965\text{ }\mu\text{m}^2$.

Figure 6.159 shows the output voltage of the differential TIA in dependence on the difference of the optical power in the two photodiodes. A difference of the optical power of -90 dBm was detectable (without background light, i.e. light only in one photodiode and the other one in darkness) and for larger differences than about -80 dBm the behavior was logarithmic. With 500 lux background light (BGL), the minimum detectable difference in optical power was about -60 dBm . The transimpedance of the DIFF TIA varied from about $5\text{ G}\Omega$ to $400\text{ k}\Omega$. Without BGL, the bandwidth of the DIFF TIA was between 900 Hz and 14 MHz increasing for optical power from -80 to -20 dBm [164].

According to Fig. 6.160 the high-speed channel achieved a transmission distance of 7.3 m with a BER of less than 10^{-9} at 1 Gb/s with a 680 nm VCSEL at 0.81 mW. The dependence of BER on background illuminance is shown in Fig. 6.161 for a transmission distance of 3 m. The BER is below 10^{-9} up to 2000 lux. The DC photocurrent caused by the BGL, which produced additional shot noise, is also shown in this figure.

The sensitivity of this $0.35\text{ }\mu\text{m}$ HV CMOS APD receiver with an APD area of $31,416\text{ }\mu\text{m}^2$ was -31.8 dBm at 1 Gb/s with 675 nm. Compared to -19.6 dBm at 1.25 Gb/s with 660 nm of a $0.6\text{ }\mu\text{m}$ BiCMOS receiver with a pin-photodiode area of $132,548\text{ }\mu\text{m}^2$ [166] and compared to -23 dBm at 1.25 Gb/s with 660 nm of a $0.5\text{ }\mu\text{m}$ BiCMOS receiver also with a pin-photodiode area of $132,548\text{ }\mu\text{m}^2$ [167], the sensitivity is much better thanks to the integrated APD. In a $0.35\text{ }\mu\text{m}$ CMOS technology a sensitivity of -22 dBm at 2.4 Gb/s with 800 nm and an avalanche photodiode

Fig. 6.159 DC response of the differential TIA

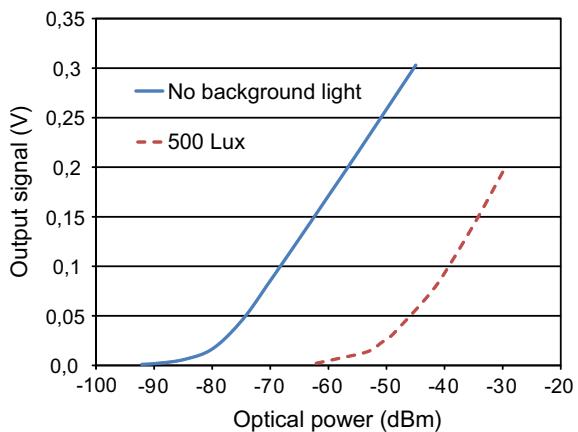


Fig. 6.160 Measured BER over distance between transmitter and receiver at 1 Gb/s

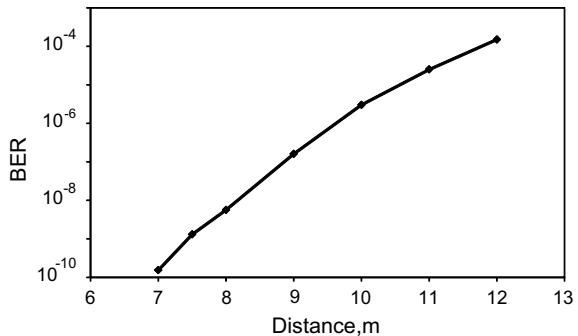


Fig. 6.161 Measured BER of the high-speed receiver in dependence on background illumination for a distance of 3 m between transmitter and receiver at 1 Gb/s and photocurrent caused by background illumination

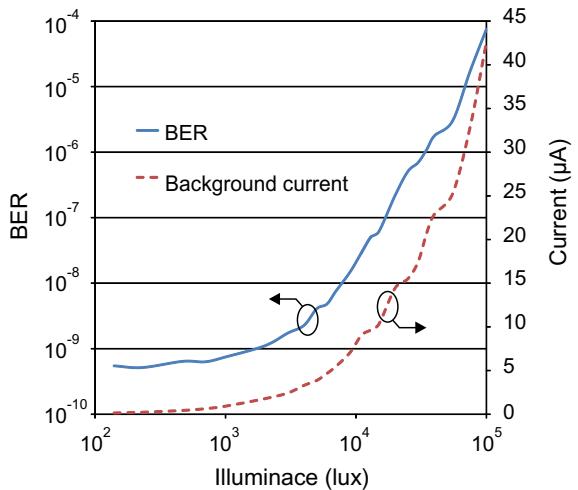
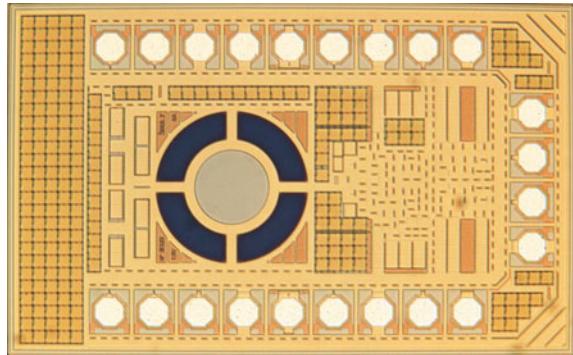


Fig. 6.162 Chipphoto of 200 μm BiCMOS APD receiver



area of $8,284 \mu\text{m}^2$ was reported [168]. Compared to these results, the sensitivities of -3.8 dBm at 3.125 Gb/s [169] and -3.2 dBm at 4 Gb/s [170] of a 65 nm CMOS receiver with a photodiode area of $62,500 \mu\text{m}^2$ and 670 nm are rather moderate. A redesigned $0.35 \mu\text{m}$ HV CMOS APD receiver with a $200 \mu\text{m}$ diameter APD achieved a sensitivity of -35.5 dBm at 1 Gb/s [171]. A receiver with a $400 \mu\text{m}$ diameter APD reached a sensitivity of -34.7 dBm [171].

Also in order to increase the receiving angle over that of a $0.35 \mu\text{m}$ pin photodiode receiver (see Fig. 6.151) by omitting the receiver lens and still to achieve large transmission distances, an avalanche photodiode (APD) in the linear mode was integrated in an OEIC in $0.35 \mu\text{m}$ BiCMOS technology. In addition, the bipolar transistors of a $0.35 \mu\text{m}$ BiCMOS technology allow to achieve a higher data rate at a similar or even better sensitivity as the $0.35 \mu\text{m}$ CMOS receiver. This BiCMOS receiver with a $200 \mu\text{m}$ APD was described in [172]. The photo of this OEIC is shown in Fig. 6.162. It achieved a sensitivity of -32.2 dBm at a BER of 10^{-9} , at 2 Gb/s , and at 675 nm . Figure 6.163 shows the cross section of the APD and the receiver's block diagram [173].

The beam of a single-mode VCSEL at 680 nm having an optical power of 0.85 mW and an extinction ratio of 8 was collimated using a lens and adjusted via a MEMS mirror (Fig. 6.164) to the APD on the receiver chip [173]. The beam had a divergence angle of about 0.5 mrad (FWHM). Figure 6.165 shows the BER for a data rate of 2 Gb/s in NRZ in dependence on the distance between transmitter and receiver for perpendicular incidence on the receiver's APD [174] in the presence of room lighting of 500 lux . For $\text{BER} = 10^{-9}$, OWC over a distance of 6.5 m was possible. The maximum receiving angle of 22° was determined at a distance of 6 m at 2 Gb/s and a PRBS of $2^{31} - 1$. This angle was limited due to optical interferences in the isolation and passivation stack of the receiver chip because of the absence of an anti-reflection coating on the APD.

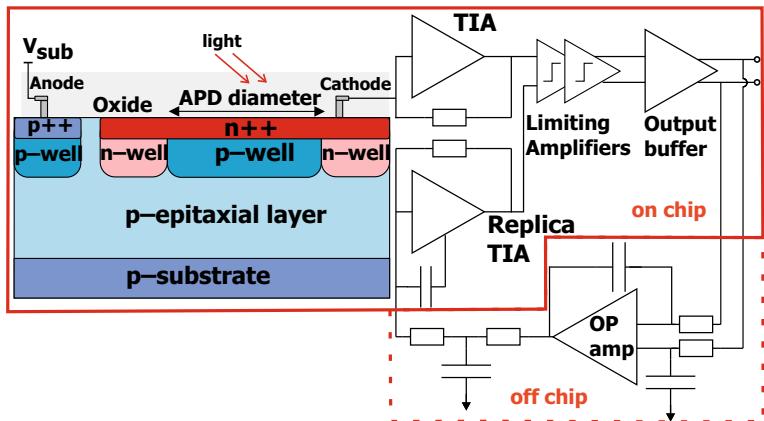


Fig. 6.163 Cross section of APD and block diagram of receiver circuit

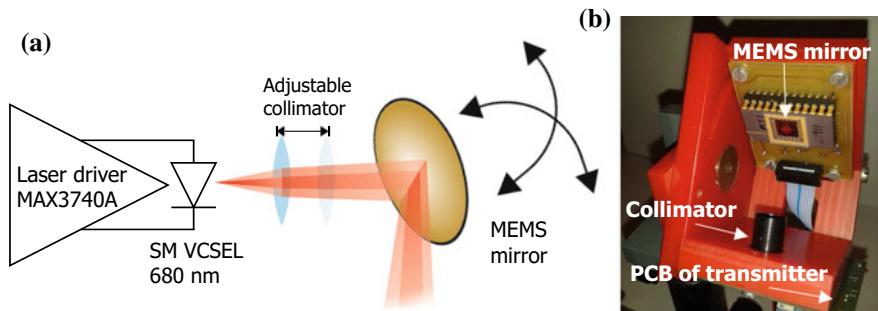


Fig. 6.164 Transmitter set up for OWC. **a** Laser diode and collimating system, **b** photo of transmitter with MEMS beam steering mirror [174]

An APD receiver with $400\mu\text{m}$ photodiode diameter in the same technology was also designed [175]. It achieved a sensitivity of -30.6 dBm at 2 Gb/s . In an

Fig. 6.165 BER in dependence on distance for $200\mu\text{m}$ APD receiver at 2 Gb/s

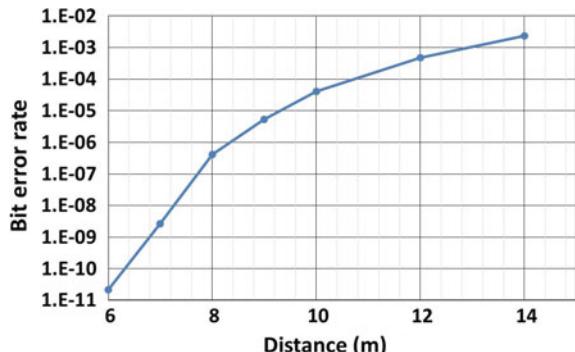


Fig. 6.166 BER in dependence on distance for 400 μm APD receiver at 2 Gb/s

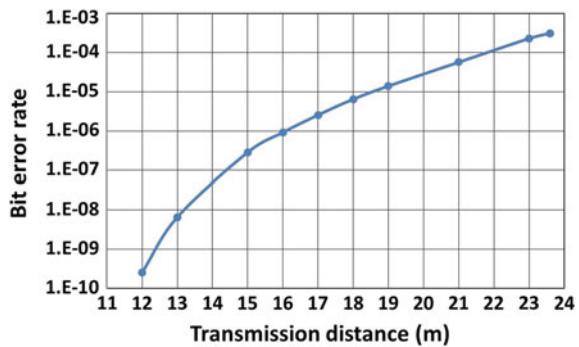
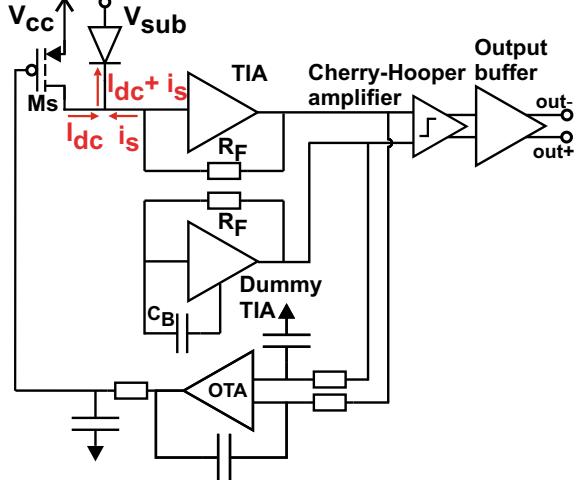


Fig. 6.167 Block diagram of 600 μm APD receiver



OWC experiment this receiver allowed to increase the distance to 12 m at 2 Gb/s and $\text{BER} = 10^{-9}$ (Fig. 6.166).

Figure 6.167 shows the block diagram of a receiver containing a 600 μm diameter APD [176]. This APD was modulation doped, leading to a larger bandwidth at the expense of a higher breakdown voltage. The feedback loop with the OTA controls the PMOS transistor Ms to deliver the current to the APD, which is caused by its dark current and ambient light, and to adjust the right operating point for the differential limiting amplifier.

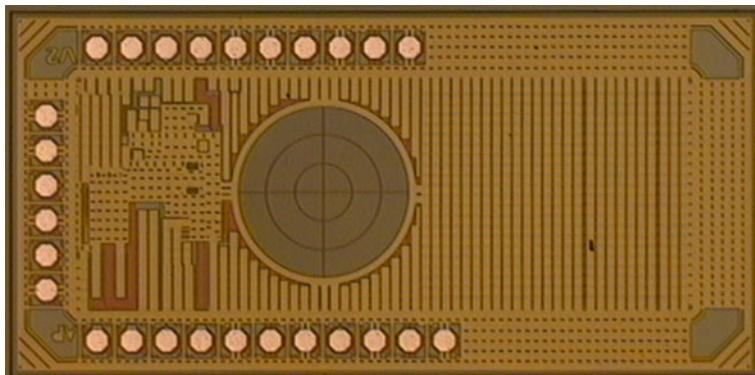


Fig. 6.168 Chipphoto of 600 μm BiCMOS APD receiver

Figure 6.168 shows the microphotograph of the receiver OEIC with the 600 μm diameter APD in 0.35 μm BiCMOS technology. The sensitivity of the 600 μm APD receiver was -31.8 dBm at 1 Gb/s for 675 nm and -29.7 dBm at 2 Gb/s with 680 nm light, $\text{BER} = 10^{-9}$ and PRBS31 [176]. Finally, a 800 μm diameter APD was integrated in an optimized 0.35 μm BiCMOS receiver and sensitivities of -33 and -29.3 dBm were obtained at 1 Gb/s and 2 Gb/s, respectively [171]. Distances of 22 m at 1 Gb/s and of 15.5 m at 2 Gbit/s with $\text{BER} = 10^{-9}$ were possible with the 600 μm APD receiver in OWC experiments.

In order to compare receivers for different date rate and with different photodiode areas, the following figure of merit (FoM) can be defined.

$$\text{FoM} = 10 \cdot \log \frac{\text{data rate (Gbps)} \cdot \text{APD area (\mu m}^2)}{\text{R}_0 \text{ (A/W)} \cdot \text{sensitivity (mW)}} \quad (6.102)$$

Table 6.10 compares the OWC APD receivers to the state of the art. The integrated PIN photodiode receivers' sensitivity is much better than that of the P-N photodiode receivers. However, the P-N photodiode receivers achieve the highest data rates. The best sensitivities and the best FoM values are obtained for the integrated APD receivers using the pin-photodiode technology (see Fig. 2.44 [159, 177, 178]).

OWC with SPAD Receivers

The SPAD-based receiver introduced in [184] was used for OWC experiments [185] at 50 Mb/s in NRZ. A laser at 635 nm with external modulator was used. This light was coupled into a single-mode fiber and a Thorlabs collimator F280FC-B was used to obtain a divergence angle of 0.01°. The receiver inside a black box was located in a distance of 2 m from the transmitter. The black box had only a small window

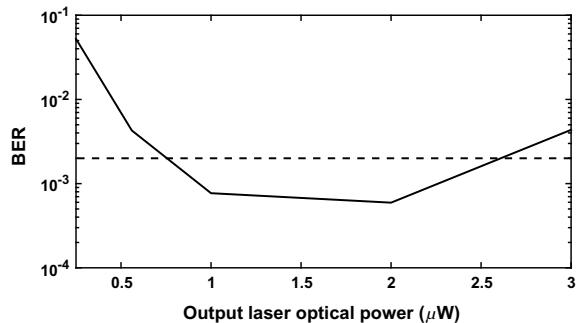
Table 6.10 Monolithically integrated optical receivers with large area photodiodes for OWC - state of the art

Reference	Technology	Type of photodiode	λ (nm)	R_0 (A/W)	PD area (μm^2)	DR (Gb/s)	Sensitivity (BER = 10^{-9}) (dBm)	FoM
[164]	0.35 μm HV CMOS	APD	675	0.41	31400	1	-31.8	80.64
[179]	0.35 μm BiCMOS	APD	675	0.435	31400	1	-35.5	84.1
						2	-32.2	83.8
[175]	0.35 μm BiCMOS	APD	675	0.445	125600	1	-34.6	92.12
						2	-30.6	88.12
[176]	0.35 μm BiCMOS	APD	675	0.48	282600	1	-31.8	89.39
						2	-29.7	90.23
[171]	0.35 μm BiCMOS	APD	675	0.45	502400	1	-33	93.48
						2	-29.3	92.78
[159]	0.35 μm BiCMOS	PIN	675	0.54	33113	3	-23.4	76.11
[180]	0.6 μm BiCMOS	PIN	660	0.36	74558	2.5	-20.1	77.25
[167]	0.5 μm BiCMOS	PIN	660	0.5	132548	1.25	-23	78.32
[181]	0.18 μm CMOS	P-N	660	0.21	785000	0.6	-10.65	74.16
[182]	0.18 μm CMOS	P-N	850	0.052	5625	5	-3.67	61
[183]	0.13 μm CMOS	P-N	850	0.05	4900	8.5	-3.87	63
[170]	65 nm CMOS	P-N	670	0.36	62500	4	-3.87	62.28

PD: photodiode

DR: data rate

Fig. 6.169 BER in dependence on optical emitter power at 2 m distance



formed by an interference filter Thorlabs FL635-10. The results of such free-space transmission are shown in Fig. 6.169. Less than 1 μW optical transmitter power is necessary to achieve a BER below 2×10^{-3} owing to the very good sensitivity of the SPAD receiver and the good collimation of the light beam.

With the same 4-SPAD receiver [184], a 650 nm RC-LED, and with an aspherical lens in front of the RC-LED, at a data rate of 50 Mb/s an OWC distance of 5 m was achieved at a BER of better than 2×10^{-3} (see Fig. 6.170) and background light up

Fig. 6.170 BER at 50 Mb/s in dependence on distance

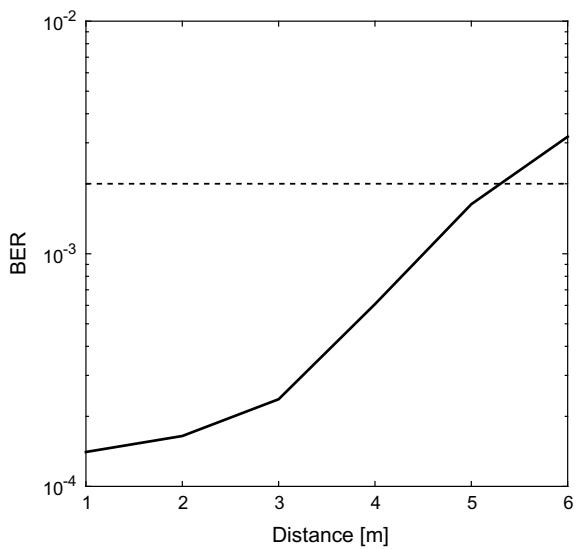
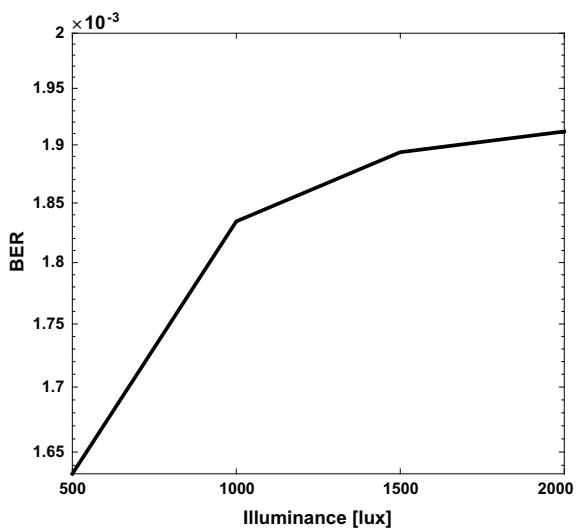


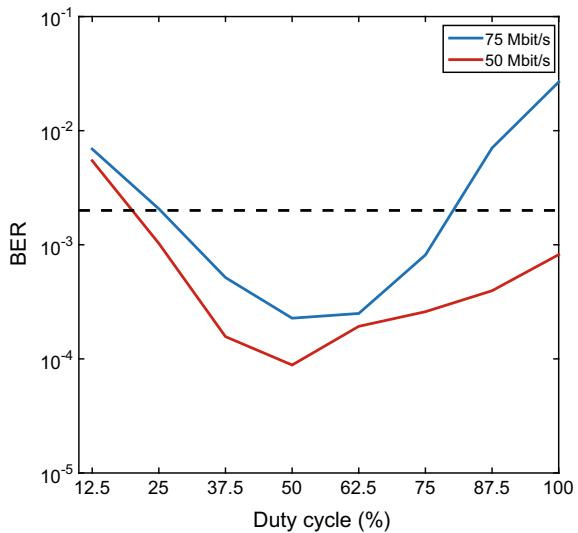
Fig. 6.171 BER in dependence on illumination from background light at 5 m distance



to 2000 lux (see Fig. 6.171) could be tolerated [186]. For RZ, the duty cycle was varied (see Fig. 6.172). At 3 m distance and 50 Mb/s with RZ at a duty cycle of 50% instead of NRZ the BER was reduced by almost an order of magnitude [187]. At 3 m distance, therefore, a data rate of 75 Mb/s with RZ was verified experimentally [187].

Other work on OWC with SPAD receivers is described in [188, 189]. Visible light communication (VLC) at 200 Mb/s over a very short distance using a receiver with 60 SPADs was reported in [188]. In [189] a total data rate of 60 Mb/s over 2 m

Fig. 6.172 BER in dependence on duty cycle



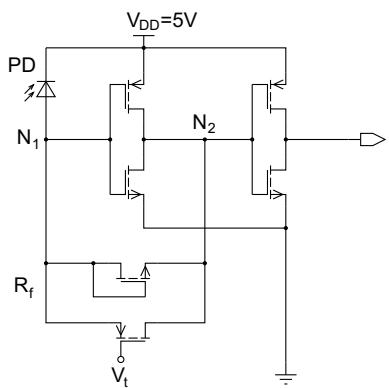
with three 20 Mb/s receiver RGB channels using a 128×32 SPAD-array each was obtained.

6.4.16 Hybrid Receivers

The optical absorption coefficient of GaAs and several related compounds is much higher than that of silicon in the visible and near infrared spectral range. III-V photodetectors, therefore, can be thinner and faster than silicon photodetectors with the same quantum efficiency. Consequently, III-V photodiodes hybrid integrated on silicon circuits are highly desirable. Polyimide bonding described in Sect. 3.3 as a wafer-scale integration of photonic devices was applied to integrate GaAs PIN photodiodes with $0.8 \mu\text{m}$ CMOS transimpedance amplifier circuits [190]. The photodiode had a $3 \mu\text{m}$ thick intrinsic GaAs absorption layer realized in a mesa with $40 \mu\text{m}$ diameter. The capacitance of the hybrid integrated photodiode was 50 fF including almost no parasitics. The responsivity of this photodiode was 0.33 A/W . The dark current was smaller than 120 pA below 5 V [190].

Figure 6.173 shows the CMOS receiver circuit consisting of two amplifier stages. Two active MOS resistors are implemented as feedback elements in the transimpedance input stage. An NMOS transistor is always present. The resistance of the PMOS transistor connected in parallel to the NMOS resistor can be controlled by the bias V_t . The second stage consists of an inverter as a voltage amplifier. For a feedback resistance $R_f = 5 \text{ k}\Omega$ a -3 dB bandwidth of 660 MHz was simulated for $C_D = 200 \text{ fF}$. For $C_D = 50 \text{ fF}$ a bandwidth of 1120 MHz was obtained. A reduction of the photodiode capacitance to 50 fF , which was in the range of the amplifier input

Fig. 6.173 Circuit of CMOS transimpedance receiver used in hybride OEIC with III/V photodiode [190]



capacitance, was an effective way to increase the bandwidth [190]. At the same time, the transistor widths could be chosen small for capacitive matching to C_D . In such a way, the low photodiode capacitance led to a high bandwidth and to a low power consumption. A power consumption between 7.5 and 10 mW at 5 V was measured finally.

According to the nominal value of $5\text{ k}\Omega$ for R_f and a voltage gain of 10 for the second amplifier stage, a transimpedance gain of $95\text{ dB}\Omega$ was achieved at the output of the polyimide bonded OEIC. A photocurrent change of $53\text{ }\mu\text{A}$ caused an output voltage swing of 3 V [190]. This results in a sensitivity large enough for chip-to-chip interconnects since VCSELs can emit even up to several milliwatts of optical power.

The receiver operated up to 800 Mb/s. At a BER of 10^{-9} , the measured sensitivities were -18.2 , -16.1 , -9.2 , and -8.5 dBm for bit rates of 155, 311, 622, and 800 Mb/s, respectively [190].

The polyimide bonding allows a variety of device combinations. InGaAs photodiodes for wavelengths up to 1550 nm also can be hybrid bonded to silicon circuits. The same group improved their results with GaAs and InGaAs photodiodes for 850 and 1550 nm, respectively, bonded to $0.5\text{ }\mu\text{m}$ CMOS receiver circuits [191]. The GaAs and InGaAs photodiodes with a diameter of $30\text{ }\mu\text{m}$ both had an intrinsic layer thickness of $3\text{ }\mu\text{m}$. Without antireflection coating their responsivities were 0.42 and 0.8 A/W , respectively. The dark currents were 2.5 pA and 20 nA , respectively, for a 5 V reverse bias [191].

The circuit working at a supply voltage of 3.3 V and shown in Fig. 6.174 is small and simple. The amplifier was designed with a transimpedance input stage and an inverter as voltage amplifier as well as two inverters with resistive feedback as an output buffer. This buffer had a bandwidth of more than 1 GHz, a voltage gain of 1, and an output impedance of 50Ω [191]. The voltage supply lines were divided into four sections to avoid feeding back amplified signals to the sensitive input part through these lines. The receiver had a high sensitivity and a high bandwidth due to the direct attachment of III-V photodiodes and due to the absence of any parasitic capacitance. A bandwidth of about 1 GHz was possible for $R_f = 5\text{ k}\Omega$ [191].

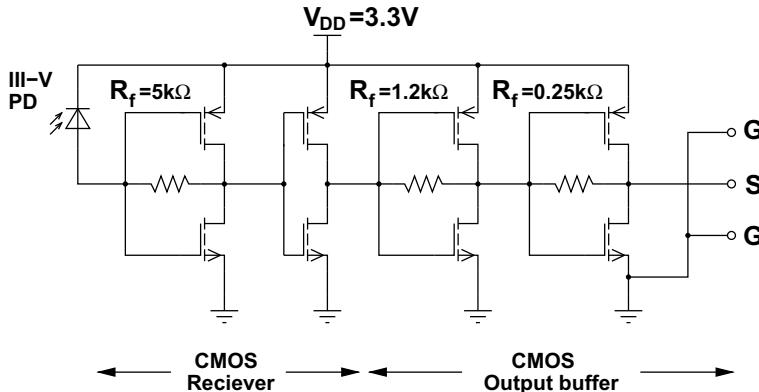


Fig. 6.174 Circuit diagram of III-V CMOS hybrid receiver [191]

Due to the high R_f value optoelectrical conversion efficiencies of 10,900 and 15,900 V/W were obtained for 850 and 1550 nm, respectively. For the GaAs-CMOS receiver (850 nm) and a BER of 10^{-9} the sensitivities were -30.1 and -27.4 dBm for bit rates of 622 and 1000 Mb/s, respectively. Wide dynamic ranges of 22.2 and 19.5 dB were observed for the respective bit rates. For the InGaAs-CMOS receiver (1550 nm) and a BER of 10^{-9} the sensitivities were -31.4 and -28 dBm with dynamic ranges of 22.4 and 18.0 dB. The receivers operated up to 1.3 Gb/s with a total power consumption below 30 mW [191].

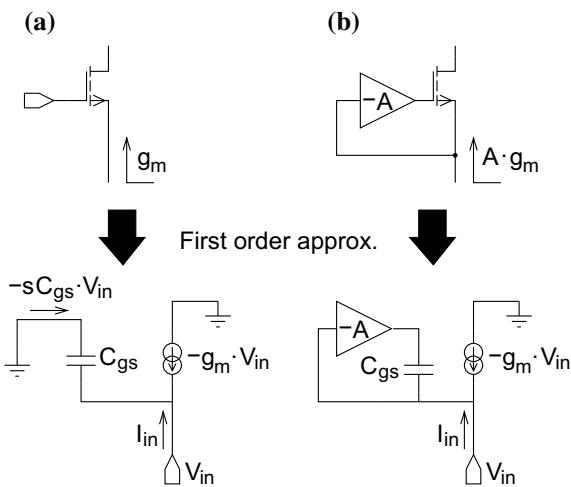
6.4.17 Speed Enhancement Techniques

g_m Enhancement Technique

High-frequency circuits in CMOS technology generally suffer from a lower transconductance and larger parasitic capacitances compared to their HBT or BJT counterparts [192, 193]. Although higher transconductances can be obtained at the expense of a higher power consumption and larger device size, i.e. larger transistor width, the parasitic capacitances finally limit the signal bandwidth. To increase the bandwidth and the gain, i.e. the sensitivity, of a CMOS transimpedance amplifier, a g_m enhancement technique as well as an inductive peaking technique, however, can be applied. Let us have a look on the g_m enhancement technique first.

Typical high-frequency circuits adopt a common-gate input stage. For an amplifier with a common-gate input configuration, the conversion gain can be boosted by increasing the transconductance g_m of the input transistor M1. Compared to the conventional common gate input stage (Fig. 6.175a) the effective transconductance is increased by the feedback amplifier gain ($-A$) for the circuit shown in Fig. 6.175b.

Fig. 6.175 Input impedance analysis without (a) and with (b) local feedback loop [194]



On the other hand, the input impedance of the transimpedance amplifier with a g_m -enhanced common-gate input stage as shown in Fig. 6.175 is lowered by the factor A . This is especially advantageous for a high input node capacitance introduced by large-area photodiodes or external PIN photodiodes where also bondpad capacitances are involved. The inverting amplifier has to be designed for a unity gain bandwidth larger than that of the transimpedance amplifier for gain and bandwidth enhancement. Let us now describe the second technique applied in a 2.5 GHz CMOS transimpedance amplifier.

Active Inductors

Inductors instead of resistive load elements can be implemented in order to eliminate their parasitic capacitance effect and their noise contribution. In [195] spiral inductors were integrated needing a large area, however. It is much better for a small chip area to use active inductors. An active inductor can be formed by an NMOS transistor and a resistor (see Fig. 6.176).

The NMOS transistor is operated in the saturation region. The resistor can be realized by a PMOS transistor operating in the triode region. The output impedance looking from the source of the NMOS transistor can be approximated by [194]:

$$Z_{\text{out}} = \frac{1}{g_m} \frac{1 + s R_s C_{\text{gs}}}{1 + s \frac{1}{g_m} C_{\text{gs}}} \quad (6.103)$$

with a zero at $\omega_{\text{zero}} = -1/(R_s C_{\text{gs}})$ and a pole at $\omega_{\text{pole}} = -g_m/C_{\text{gs}}$. For Z_{out} to behave as an inductor, it is necessary that $g_m > 1/R_s$. Z_{out} can be modelled as an ideal inductor L in series with a passive resistor R_1 and with another resistor R_2 in parallel as shown in Fig. 6.176 in the inductive region $\omega_{\text{zero}} < \omega < \omega_{\text{pole}}$. It is possible to tune

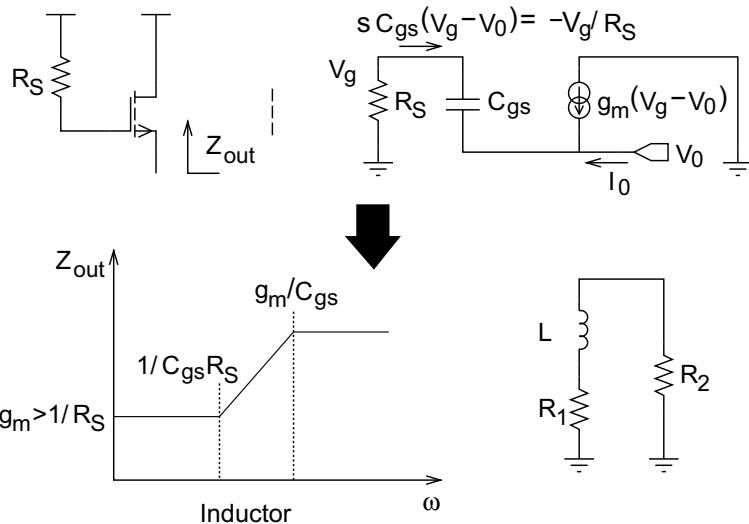


Fig. 6.176 Principle of active inductors [194]

the inductive region and the inductance by adjusting the locations of the pole and zero. For a better gain and boosted bandwidth of a transimpedance amplifier, the inductive region was designed to cover the desired -3 dB bandwidth [194].

The schematic of the transimpedance amplifier proposed in [194] combining the g_m enhancement technique with active inductors is shown in Fig. 6.177. R_{s1} and M_{r1} form the active inductor load of the input transistor M1 operating in common-gate configuration. M2 operates in common-source configuration with the active inductor load formed with R_{s2} and M_{r2} . A current-injection technique is also implemented. To increase the current in M1 and thereby its g_m , the current through transistor Mb is added to the current flowing through the active inductor load of M1. In such a way the dc voltage drop across the active inductor can be kept low and the width of transistor M_{r1} can be reduced. In such a way, the self-resonance frequency of the active inductor can be increased and the voltage headroom required by the active inductor can be reduced.

The open-loop transimpedance of the circuit shown in Fig. 6.177 is approximately [194]:

$$T_{ol}(0) = Z_1 g_{m2} Z_2 \quad (6.104)$$

where Z_1 and Z_2 are the inductances of the first and second active inductor, respectively. A value of $62.8\text{ dB}\Omega$ was reported for T_{ol} . The common-source gain stage provided only unity gain to avoid the Miller effect [194]. The feedback resistor R_f was chosen to be $3\text{ k}\Omega$ for effective transimpedance and bandwidth optimization. The closed-loop transimpedance

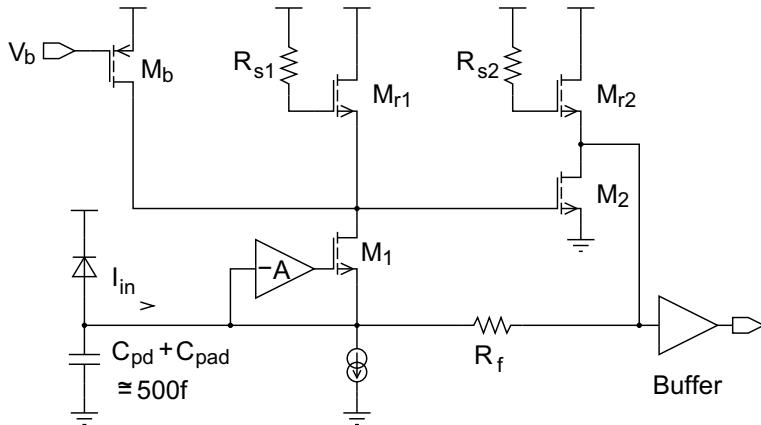


Fig. 6.177 Circuit schematic of TIA with active inductor loads [194]

$$T_{cl}(0) = \frac{T_{ol(0)}}{1 + T_{ol(0)} \frac{1}{R_f}} \quad (6.105)$$

therefore was about $60 \text{ dB}\Omega$ [194].

For comparison simulated results were given in [194] for a conventional transimpedance amplifier with resistive loads and without g_m enhancement. For such a conventional transimpedance amplifier (TIA) the dominant pole is at the source of M1 with a -3 dB frequency of $f_{-3 \text{ dB}} = \frac{1}{2\pi} \frac{g_{m1}}{C_{in}} \approx 630 \text{ MHz}$. A conversion gain of $45 \text{ dB}\Omega$ belongs to this conventional TIA [194].

With current injection increasing g_{m1} a conversion gain of $54 \text{ dB}\Omega$ and a -3 dB bandwidth of 1.2 GHz were achieved. When the feedback amplifier with $A = 15 \text{ dB}$ and a -3 dB bandwidth of 5 GHz for g_m enhancement was added, the pole at the source of M1 became $A \frac{1}{2\pi} \frac{g_{m1}}{C_{in}} \approx 3.7 \text{ GHz}$ [194]. This input pole is far away from the signal band of interest and the -3 dB bandwidth is dominated by the pole at the input of the common-source gain stage, which is given by $f_{-3 \text{ dB}} = \frac{1}{2\pi} \frac{1}{Z_1 C_1} \approx 2.6 \text{ GHz}$ [194], where C_1 is the parasitic capacitance at the drain of transistor M1. The effect of the active inductors when also added in the simulations was rather small. The -3 dB bandwidth was extended to 2.7 GHz with a transimpedance gain of $54 \text{ dB}\Omega$ [194].

A transimpedance gain of $54.5 \text{ dB}\Omega$ and a bandwidth of 2.5 GHz were measured for the transimpedance amplifier fabricated in TSMC $0.35 \mu\text{m}$ 1P4M digital CMOS process. In this technology the core area of the transimpedance amplifier occupied only $45 \times 55 \mu\text{m}^2$. The measured RMS input noise current was 800 nA in a 2 GHz bandwidth, which is a rather high value. The power consumption was 22.5 mW with a 3 V supply [194].

Electric-Field Enhancement Technique

Optoelectronic integrated circuits usually suffer from slow carrier diffusion of photo-generated carriers in the integrated photodiodes due to light penetration depth larger than the width of the space-charge/drift region caused by doping concentrations of 10^{15} cm^{-3} and higher as well as by limited chip supply voltages. Bandwidths of many integrated photodiodes are lower than several tens of MHz [84, 85]. Base-collector photodiodes in standard-buried-collector based bipolar and BiCMOS processes achieve several hundred MHz, however, with a low quantum efficiency [93, 119, 120]. Double photodiodes perform similarly concerning speed partially with a higher responsivity [105, 142]. Integration of PIN photodiodes with low-doped intrinsic regions allows wider drift regions and high quantum efficiencies in CMOS technology with little or no additional process complexity [101, 128, 144]. In bipolar and BiCMOS processes larger process modifications are necessary for PIN photodiode integration [86, 87]. Lateral photodiodes in a SOI film with a thickness of the order of one micrometer eliminate or reduce the slow-diffusion effect, however, suffer from a low quantum efficiency [196]. Another possibility to speed up integrated photodiodes is to use a second higher supply voltage for the photodiode to increase the electric field, i.e. the drift velocity, and the width of the space-charge region. A second supply voltage of 30 or 24 V was also necessary for lateral PIN photodiodes on SOI [118, 124]. Due to the thickness of the SOI layer of $2 \mu\text{m}$ the quantum efficiency was only about 10% at 850 nm.

Many applications, especially consumer applications, however, do not allow to use a second, higher supply voltage for the photodiode due to cost reasons. With steadily reducing structure sizes of new silicon technologies towards the nanometer regime, chip supply voltages reduce steadily, leading to reduced drift velocity and increasing drift times, i.e. rise and fall times of the integrated photodiodes. Therefore, an innovative OEIC containing an integrated voltage-up-converter (VUC) to generate the high photodiode supply voltage from the circuit supply voltage on chip was suggested [197]. The VUC-OEIC, therefore, only needs one external supply voltage for the circuits and for speed enhancement of the integrated photodiode.

In [197] a PIN photodiode allowing the use of a higher reverse bias than the circuit supply voltage [86] with a large I-layer thickness was implemented leading to a quantum efficiency of 89% for a wavelength of 670 nm and 50% at 850 nm. Due to autodoping problems in epitaxy [86] it is difficult to achieve a low doping concentration throughout the whole intrinsic region. Here the VUC also helps to relax demands on epitaxy and to achieve a high speed of the integrated photodiodes nevertheless. The VUC actually allowed to extend the data rate for a given technology from about 50 Mb/s to 1.5 Gb/s [197].

The OEIC consisted of a PIN photodiode, an amplifier for the photocurrent and a charge pump which acts as a VUC. The photodiode had a capacitance of 160 fF at a reverse bias of 15 V and a responsivity of 0.48 A/W for 670 nm. The VUC shown in Fig. 6.178 is based on a 4-stage Dickson charge pump [198]. It consists of an inverter as a predriver which produces the necessary phase shift of 180° between the clock signals and uses three additional inverters. The clock signal was connected

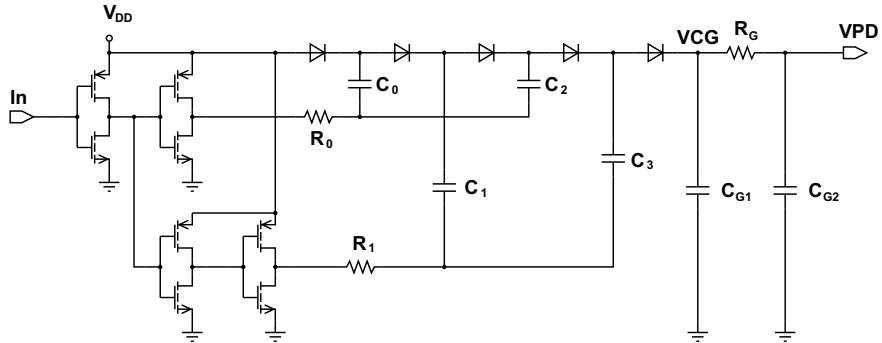


Fig. 6.178 Circuit schematic of the VUC [197]

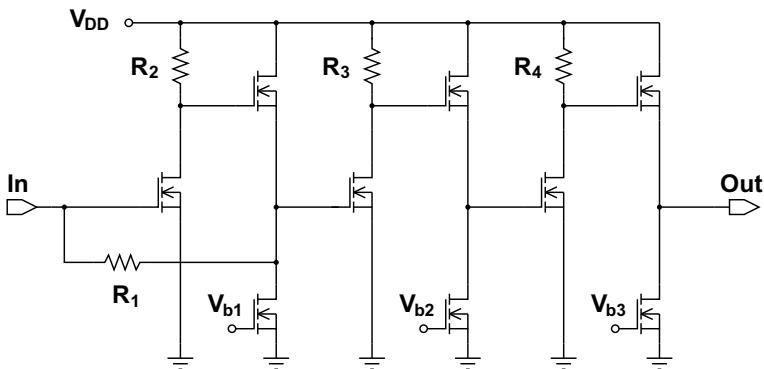


Fig. 6.179 Circuit schematic of the CMOS TIA implemented in the VUC-OEIC [197]

from outside the chip to allow for a high flexibility to characterize the test chip. The capacitors C_0 , C_1 , C_2 , and C_3 had values of 10 pF . C_{G1} was equal to 20 pF . To reduce the voltage ripple of the supply VCG for the photodiode there was a filter implemented formed by $R_G = 10\text{ k}\Omega$ and $C_{G2} = 20\text{ pF}$ [197]. The photodiode was connected to the node VPD (see Fig. 6.178). The rectifier diodes were implemented as base/emitter diodes of a bipolar NPN transistor. The charge pump had a current consumption of about 2 mA at a clock frequency of 20 MHz .

Figure 6.179 shows the whole amplifier which consists of a transimpedance preamplifier with a feedback resistor $R_1 = 1.5\text{ k}\Omega$ followed by two voltage amplifier stages. This results in an overall transimpedance of $11\text{ k}\Omega$. To achieve a high bandwidth only NMOS transistors with minimum gate lengths ($0.6\text{ }\mu\text{m}$) were used. The amplifier drew a current of 33 mA from a 5 V supply. The OEIC had separate analog and digital supplies for the amplifier and the charge pump to suppress unwanted digital noise. The power consumption of the whole chip at a supply voltage of 5 V was 175 mW . Figure 6.180 shows the micrograph of the VUC-OEIC chip with an area

Fig. 6.180 Chipfoto of VUC-OEIC [199]

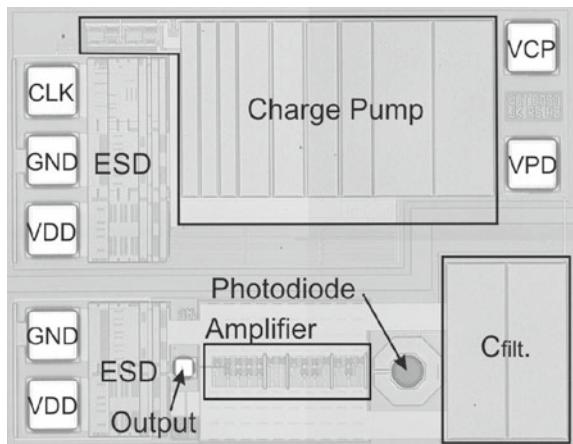
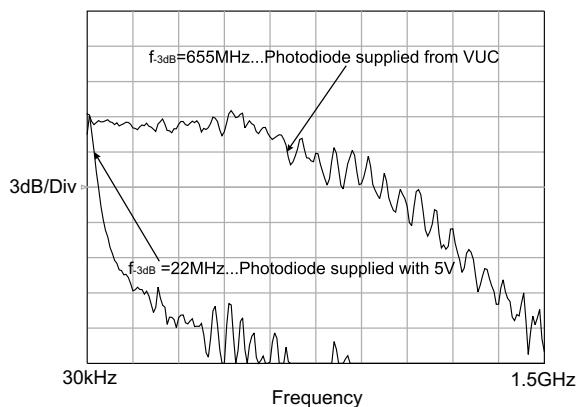


Fig. 6.181 Frequency response of the VUC-OEIC [197]



of $1240\mu\text{m} \times 960\mu\text{m}$. The chip was manufactured in a $0.6\mu\text{m}$ BiCMOS process [197].

For measurements, a 670 nm laser diode was modulated via a bias-T by a HP8753E network analyzer or a digital 2.5-Gb/s ECL pattern generator. A Tektronix communication analyzer CSA8000 was used to measure eye diagrams and determine sensitivity values of the VUC OEIC. The output signal of the OEIC was measured with a 3-GHz picoprobe having an input capacitance of 100fF .

The improvement of the frequency response due to the VUC can be seen in Fig. 6.181. With the charge pump a cutoff frequency of 655 MHz was obtained compared to only 22 MHz without VUC [197]. The rise and fall times measured at the OEIC output without VUC were 13.3 and 12.1 ns. With the VUC, these values reduced to 0.55 and 0.57 ns, respectively [197].

The maximum achievable data rate is 1.5 Gb/s (see Fig. 6.182) with VUC compared to only about 50 Mb/s without VUC.

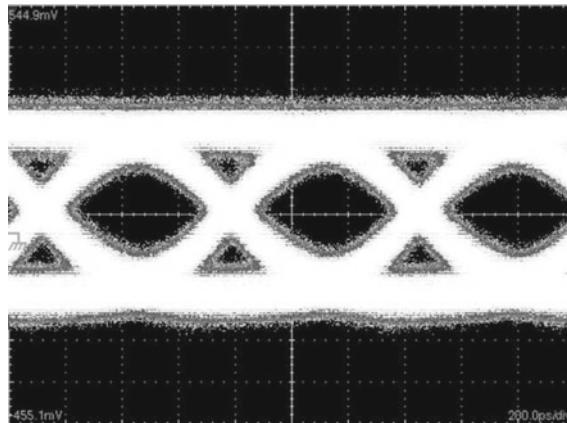


Fig. 6.182 Eye diagram of the VUC-OEIC at 1.5 Gb/s, $\lambda = 670$ nm, $\text{BER} = 10^{-9}$ [199]

Table 6.11 Comparison of sensitivity for external supply $\text{UPD} = 16.3$ V and for VUC ($\lambda = 670$ nm, $\text{BER} = 10^{-9}$) [199]

Data rate (Mb/s)	Sensitivity with UPD = 16.3 V (dBm)	Sensitivity with VUC (dBm)
622	-17.5	-14.3
1000	-17.5	-14.1
1250	-17	-14.1
1500	-16.8	-13.1

Table 6.11 lists the sensitivity results of the VUC-OEIC for $\lambda = 670$ nm and a bit error rate of 10^{-9} . The chip was wire-bonded to a PCB. Both analog and digital pads were connected to the same 5 V power supply. The bias voltage of the photodiode $\text{UPD} = 16.3$ V was measured at the VPD pad. For comparison, for the photodiode biased with 16.3 V from an external power supply sensitivities for the OEIC of -17.5, -17.5, -17, and -16.8 dBm were found for data rates of 0.622, 1.0, 1.25, and 1.5 Gb/s, respectively [199]. These values were not corrected for about 1.5 dB due to the picoprobe noise and were limited by the non-optimized MOS amplifier. The corresponding sensitivity values of the VUC-OEIC were -14.3, -14.1, -14.1, and -13.1 dBm, indicating that the VUC reduces the sensitivity by up to about 3.5 dB. For the VUC the sensitivity for decreasing data rates remains almost constant, indicating that there was some cross-talk or substrate noise from the VUC to the amplifier or photodiode. An influence of the VUC output voltage ripple could be excluded due to the R-C-filtering of the photodiode bias. The problem is to be solved in a redesign by an improved layout to reduce coupling from VUC to substrate and from there into the photodiode [197]. The amplifier noise can also be reduced in a redesign by an optimized MOS or BiCMOS amplifier.

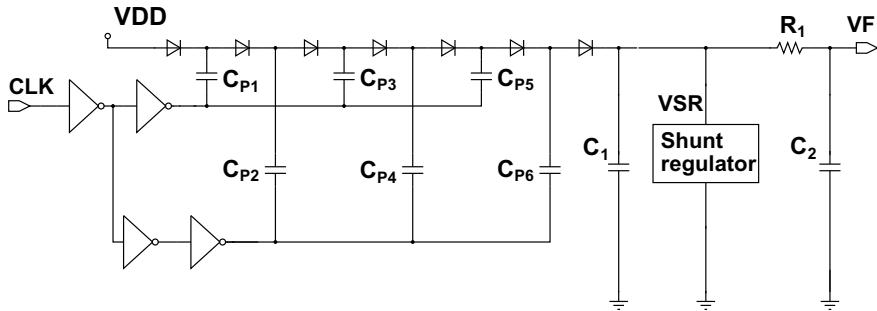


Fig. 6.183 Circuit schematic of the VUC with regulator [200]

In another investigation, the bandwidth of the photodiode in an optoelectronic integrated circuit with a single 5 V supply was extended from 20 to 771 MHz by an innovative on-chip voltage-up-converter [200]. In this approach, a shunt-regulator keeps the die area small and exploits breakdown voltages of available devices best. Rise and fall times below 0.5ns were achieved allowing operation at data rates in excess of 1 Gbit/s. A possible receiver sensitivity of -22.5 dBm was obtained for a wavelength of 670 nm.

In [200] a monolithically integrated OEIC, which incorporates the same photodiode as in [197], was presented. The slow carrier-diffusion effect in the photodiode was significantly reduced by extending the space-charge region with the help of the innovative voltage-up-converter. The OEIC in 0.6 μm BiCMOS technology implemented a new design concept consisting of a charge pump with regulator and a photodiode with a transimpedance amplifier followed by a buffer to drive the 50Ω measurement equipment [200]. The charge pump generated the high voltage (14.5 V) needed for the supply of the photodiode from the circuit supply voltage of $VDD = 5 \text{ V}$. It consisted of a Dickson-type [198] voltage multiplier (Fig. 6.183) with six stages and a shunt regulator at its output.

The shunt regulator (Fig. 6.184) helps to minimize the influence of the variable load current (the photodiode's current, i.e. the photocurrent) on the output voltage in order to guarantee high photodiode speed for all light intensities and to reduce the output ripple present at C_1 (5 pF). The output ripple voltage is further reduced with the help of an RC filter (R_1 and C_2 in Fig. 6.183). The clock signal could be in the frequency range from 25 to 100 MHz coming from an external source [200]. At 50 MHz, the pump could deliver $100 \mu\text{A}$.

With the help of several inverting stages the pump signal and an inverted pump signal is generated from the clock (CLK) signal. The clock is applied externally for flexibility of the test chip. Without regulator, the value of the unloaded output voltage of the charge pump VSR would be about two times the value of the regulated voltage (14.5 V) [200]. Under this condition, the maximum output power for a given clock frequency and a fixed pump-capacitor area is available. A shunt regulator was chosen to keep the output voltage at the lower fixed level. The unloaded voltage

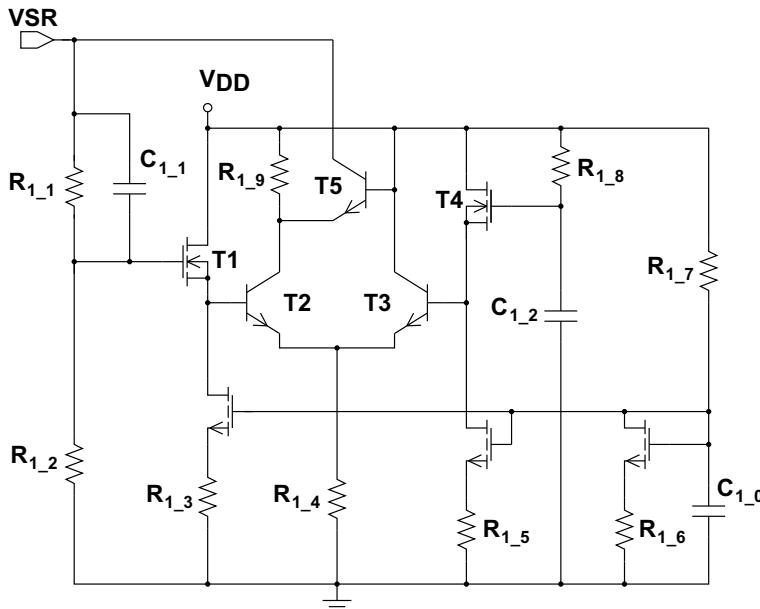


Fig. 6.184 Circuit schematic of the shunt regulator [200]

condition for the charge pump never occurs (as it would with a series regulator). The current difference between the maximum deliverable charge-pump current and the photocurrent is flowing through the shunt regulator. Therefore, the pump itself has always the same load, independent of photocurrent, and has constant power consumption, too.

Keeping the free running (but never occurring) voltage of the charge pump higher and using more stages has a further advantage: The maximum reverse voltage the rectifier diodes have to withstand is lowered. In this case, the reverse voltage across the diodes is about 5 V. The diodes were realized with bipolar transistors. With the low reverse voltage it was possible to use the more efficient base-emitter diode instead of the collector-base diode, which is slower according to simulations. In such a way, the high frequencies mentioned above were applicable. This reduced the pump capacitors $C_{P1}-C_{P6}$ to 1.2 pF only (compared to 10 pF in [197]) and, therefore, saved chip area [200].

As mentioned before, the shunt regulator keeps the pump output voltage fixed allowing low breakdown voltages of the poly-poly capacitors in the charge pump. Therefore, shunt regulators are preferred against series regulators. Figure 6.184 shows the regulator used. It consists of a FET-input bipolar differential stage for high gain and a high voltage cascode transistor T5 with a biasing resistor R1_9 in parallel. The FET-input stage is necessary because of the high-resistance voltage divider needed. The regulator was designed to sink at least 1 mA and takes its reference directly from the supply voltage VDD [200]. The RC filter consisting of R1_8

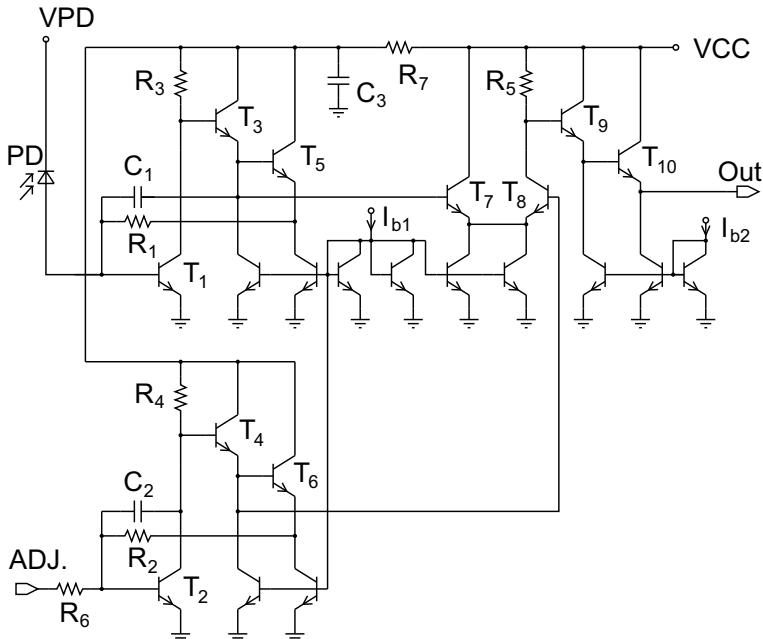


Fig. 6.185 Circuit schematic of the receiver [200]

and C1_2 serves to smoothen the reference voltage. Due to its structure and due to C1_1, fast responses to load current changes are accomplished.

The receiver shown in Fig. 6.185 consists of a photodiode (PD) with a light-sensitive diameter of $50\text{ }\mu\text{m}$ followed by a transimpedance amplifier formed by T1, R3, T3, T5, C1, and R1. Together with a dummy amplifier formed by T2, R4, T4, T6, C2 and R2 the voltage difference is amplified with a differential amplifier (T7, T8 and R5) and buffered with two emitter followers (T9 and T10) for driving the 50Ω output. The usage of a nearly identical dummy amplifier helps to reduce the VUC switching noise coupled through the substrate [200]. The dummy amplifier has an additional input pad (ADJ) only for evaluation purposes, in a final chip this bond pad is not necessary.

Figure 6.186 shows the resulting chip with the strictly separated charge pump (left side) and optical receiver (right side). The active diameter of the photodiode is $50\text{ }\mu\text{m}$, but it has an overall dimension of $130\text{ }\mu\text{m}$ which includes a light shield and the connection for the cathode. The active area of the amplifier itself is only $80\text{ }\mu\text{m} \times 160\text{ }\mu\text{m}$. The whole chip occupies an area of $1080\text{ }\mu\text{m} \times 870\text{ }\mu\text{m}$.

The complete OEIC was bonded on a PCB. The output of the receiver was directly connected via a 50Ω micro-strip line to a SMA-connector. The clock for the charge pump was externally generated from an impulse generator. For the comparison of the speed enhancement, the photodiode was first connected to 5 V and then to the regulated output of the charge pump. The photodiode supply VPD (see Fig. 6.185)

Fig. 6.186 Chipphoto of receiver with VUC and shunt regulator [200]

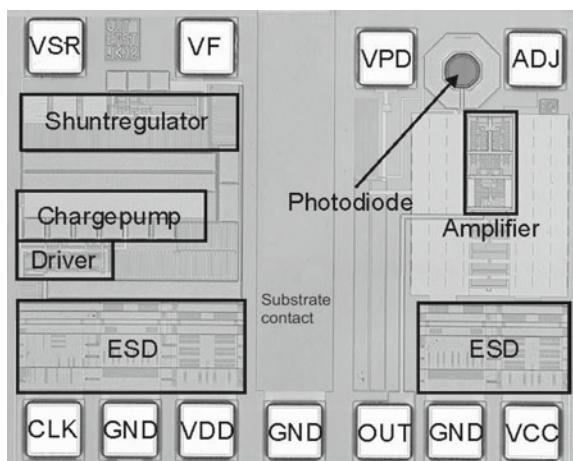
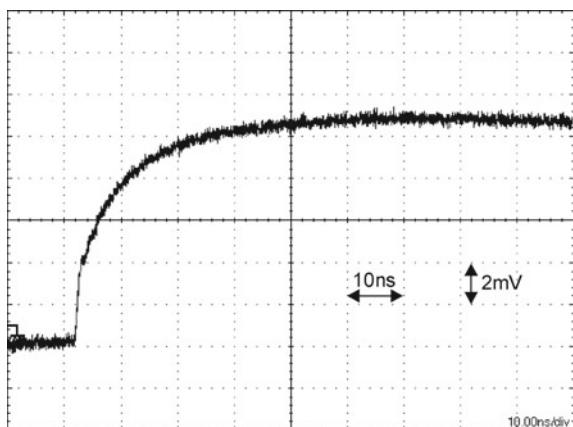


Fig. 6.187 Step response of receiver without VUC, i.e. for $VPD = 5 \text{ V}$ [200]



was connected to the output of the charge pump VF (see Fig. 6.183) and to an external chip capacitor which acts together with the internal $10\text{k}\Omega$ resistor R1 as a low pass. The value of this supply blocking capacitor in parallel to the on-chip capacitor C2 (only 2pF) was 10nF and was realized as a small SMD-chip capacitor. The charge pump generated a voltage of 14.5 V and was clocked at a speed of 50 MHz , for which it can supply a current of $100\mu\text{A}$. The current consumption of the charge pump is low compared to that of the receiver and has the value of 2 mA [200].

The photodiode was stimulated by a 670 nm laser to which the test signals were fed via a bias-T. The output of the receiver was connected to a Tektronix Oscilloscope CSA8000 for the measurement of transient behavior. A 2.5 Gbit/s pattern generator modulated the laser via the bias-T. In Figs. 6.187 and 6.188 the step response can be seen for the case that the photodiode was supplied from $VDD = 5\text{ V}$ and from the charge pump, respectively. In both figures, 256 measurements were averaged to

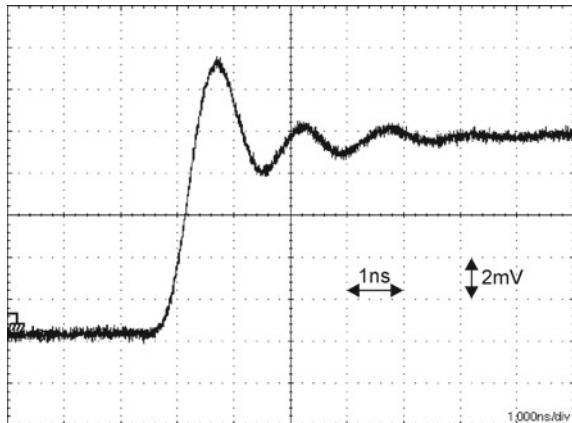


Fig. 6.188 Step response of receiver with VUC and shunt regulator ($\text{VPD} = 14.5 \text{ V}$) [200]

Table 6.12 Summary of speed enhancement ($\lambda = 670 \text{ nm}$, $\text{VDD} = \text{VCC} = 5 \text{ V}$) [200]

	OEIC with VUC ($\text{VPD} = 14.5 \text{ V}$)	OEIC without VUC ($\text{VPD} = 5 \text{ V}$)
Bandwidth (MHz)	771	20
Rise time (ps)	492	27500
Fall time (ps)	481	25800

reduce noise for rise/fall time determination. In Fig. 6.188 the asynchronous charge pump noise is also averaged over 256 measurements. The rise and fall times are reduced from above 25 ns by a factor of approximately 50 to below 0.5 ns, because the higher photodiode supply voltage generated by the voltage-up-converter (VUC) increases the width of the space-charge region and thereby eliminates slow diffusion of photogenerated carriers. A HP8753 network analyzer was used to measure the frequency response of the OEIC. The bandwidth enhancement due to the voltage-up-converter is from 20 to 771 MHz indicating an improvement by a factor of 38. In Table 6.12 the results are summarized.

Due to the switching function of the charge pump, a small amount of cross talk of about 12 mVpp was observed at the output of the amplifier. The receiver without charge pump produced an output noise voltage of 2.2 mVeff. Without the SMD capacitor, but with a $10\text{k}\Omega$ resistor between VF and VPD (activating an additional RC filter together with a 5 pF blocking capacitor integrated close to the photodiode), the cross talk signal at the output was 22 mVpp. After a redesign, i.e. the optimization of the integrated RC filter, neither the external SMD capacitor nor the additional $10\text{k}\Omega$ resistor will be necessary [200]. When this OEIC is used for data communication at a BER of 10^{-9} , the estimated sensitivity for ISI-free data rates is -22.5 dBm with a laser source which has an infinite extinction ratio [200]. The power penalty due to the switching noise of the charge pump can be determined by about 1.5 dB .

considering that the sensitivity of the receiver without the noise of the charge pump is -24 dBm [200]. The current consumption of the receiver alone was 17 mA , which means a power dissipation of 85 mW .

Let us summarize. The OEIC described in [200] used a charge pump to improve the bandwidth of integrated photodiodes from 20 to 771 MHz with a single supply of 5 V. This bandwidth is sufficient for 1.25 Gbit/s receiver operation. The charge pump produced a voltage of 14.5 V with a current capability of $100 \mu\text{A}$ at a clock frequency of 50 MHz. The estimated upper bound for the optical power penalty due to the switching noise was only 1.5 dB. After a redesign for reduction of overshoot, the sensitivity of -22.5 dBm can be obtained at a data rate of 1.25 Gbit/s [200], which is more than 8 dB better compared to [197], where no regulator was implemented.

A current consumption of 95 mW was achieved for the complete chip including charge pump, shunt regulator, and amplifier. Compared with [197] the current consumption was halved, the bandwidth higher, the sensitivity was much better and the chip area was smaller. Chip size can be reduced further in a redesign to about $920 \times 770 \mu\text{m}^2$ by eliminating the external connections from the charge pump to the photodiode, integrating a clock generator and reducing the spacing between VUC and receiver [200].

6.4.18 Plastic-Optical-Fiber Receivers

Many applications require fast and sensitive optical sensors with a large light-sensitive area. Industrial automation and optical data transmission via plastic optical fibers (POFs) in automobiles or via free space and local area networks as well as optical interconnects are examples for such applications. Large-area sensors relax demands on mechanical adjustment and POFs have rather large core diameters of up to 1 mm [201]. Therefore, optical sensors with large-area photodetectors are advantageous or even required.

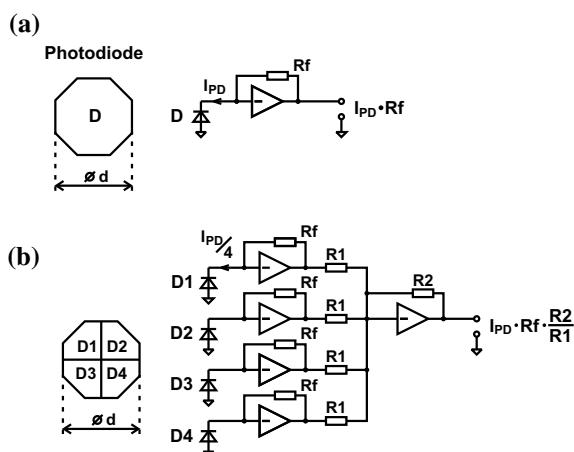
One-Channel and Four-Channel Receiver

But the high junction capacitance of a photodiode with a large diameter limits both the speed and the sensitivity of transimpedance amplifiers (TIAs) connected to the photodiode (Fig. 6.189a). A photoreceiver using a photodiode with a diameter of $700 \mu\text{m}$, having a capacitance of 20 pF , achieved a maximum data rate of 20 Mb/s and a sensitivity of -20 dBm [202]. According to [203], the -3 dB bandwidth of a transimpedance amplifier can be estimated as follows

$$f_{3 \text{ dB}} = \frac{A + 1}{2\pi R_F C_T} \quad (6.106)$$

where A is the open-loop voltage gain of the inverting amplifier, R_F is the resistance of the feedback resistor, and C_T is the sum of the photodiode capacitance C_D and the

Fig. 6.189 Block diagrams of the optical sensors: transimpedance amplifier connected to a large-area photodiode (a) and four transimpedance amplifiers connected to four quarters of a large-area photodiode and a summation amplifier (b) [204]



input capacitance C_{in} of the amplifier. To achieve higher data rates, it is important to reduce the photodiode capacitance C_D . However, even with a low-capacitance PIN structure offering a capacitance of only $0.011\text{ fF}/\mu\text{m}^2$ [31, 101], an octagonal photodiode with a diameter of $400\text{ }\mu\text{m}$ shows a capacitance of 1.6 pF . Decreasing the resistance of the feedback resistor would increase the bandwidth at the cost of a reduced sensitivity. To further enhance the bandwidth of the optical receiver without reducing sensitivity, therefore, the photodiode was divided into four sections [204]. Each of the four-quarter photodiodes was connected to a TIA. The output voltages of the four TIAs were combined with a summation amplifier (Fig. 6.189b). The capacitance of each of the four-quarter photodiodes is only one fourth of the capacitance of the unseparated photodiode, therefore the bandwidth of the four TIAs can be almost four times (if C_{in} is small) as high as the bandwidth of the receiver shown in Fig. 6.189a.

All amplifiers shown in Fig. 6.189a, b consist of three inverter stages (Fig. 6.190), because inverters are very area-efficient. The PMOS diodes P2, P4 and P6 reduce the gain of the amplifier, increase its bandwidth and ensure stability of the TIA [96]. The feedback resistor of the TIA shown in Fig. 6.189a as well as the feedback resistors of the four TIAs shown in Fig. 6.189b are formed by identical PMOS transistors P7, which have a small-signal resistance of $80\text{ k}\Omega$. P7 is not present in the summation amplifier. The resistors R1 and R2 are formed by polysilicon resistors. The summation amplifier (Fig. 6.189b) uses the same amplifier as the TIAs, but shows a higher bandwidth because the parasitic capacitance on the summation node between R1 and R2 is much smaller than the photodiode capacitances.

PIN photodiodes, similar to that described in [31, 101], but with an area 60 times as large were applied. An antireflection coating (ARC) was used to achieve a high photodiode quantum efficiency $\eta = 96.5\%$ at $\lambda = 670\text{ nm}$. Rise times of 610 ps and fall times of 515 ps were measured for the photodiode. The unseparated photodiode D of the optical receiver shown in Fig. 6.189a has a diameter of $400\text{ }\mu\text{m}$ and a

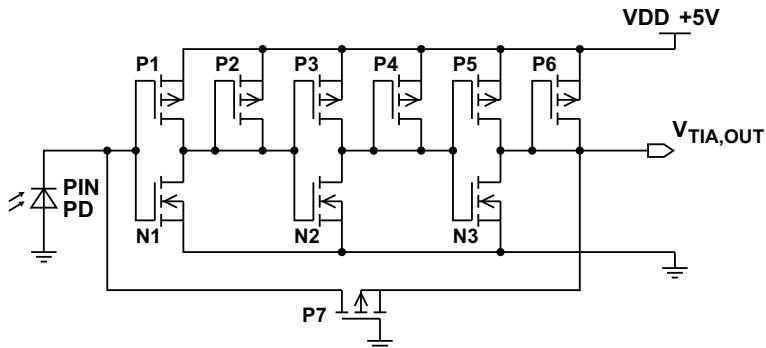
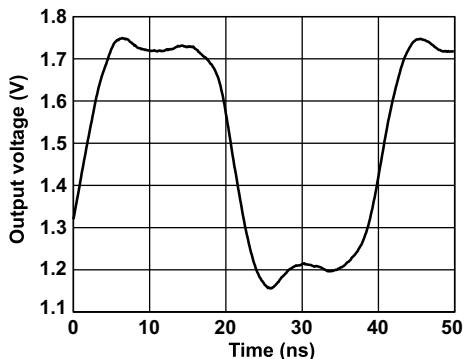


Fig. 6.190 Schematic of transimpedance amplifiers [204]

Fig. 6.191 Transient response of the optical sensor with the unseparated photodiode for $\lambda = 670\text{ nm}$, $P_{\text{opt}} = 10\mu\text{W}$ [204]



capacitance of 1.6 pF at a reverse voltage of 2.5 V . A second photodiode with a diameter of $400\text{ }\mu\text{m}$ was divided into four sections. These four-quarter photodiodes, forming the photodiodes D1–D4 shown in Fig. 6.189b, have a capacitance of 415 fF at 2.5 V each [204].

The chip was fabricated using a $0.6\text{ }\mu\text{m}$ CMOS process [204]. Both optical sensors occupied a die area of $700 \times 780\text{ }\mu\text{m}^2$. The receivers were measured on wafer level. For all measurements, the supply voltage VDD was 5 V . The light was coupled into the photodiodes via an optical fiber adjusted on a wafer prober. The light source was a laser diode with an optical wavelength of 670 nm modulated by a 2.5 Gb/s generator via a bias-tee. The output voltages were measured with a picoprobe (input capacitance 0.1 pF , bandwidth 3 GHz). The transient responses were measured with a digital storage oscilloscope Tektronix CSA8000. Figure 6.191 shows the transient response of the optical sensor with the unseparated photodiode.

Rise times of 5.11 ns and fall times of 4.55 ns were measured for the receiver with the unseparated photodiode [204]. The transient response of the optical receiver with the quartered photodiode is shown in Fig. 6.192. Rise times of 1.7 ns and fall times of 1.73 ns were measured for the receiver with the quartered photodiode. This means that the sensor with the quartered photodiode is about three times faster

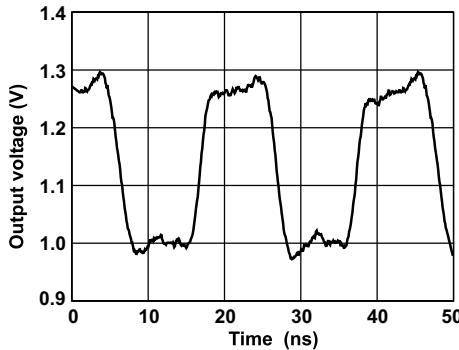


Fig. 6.192 Transient response of the optical sensor with the quartered photodiode for $\lambda = 670 \text{ nm}$, $P_{\text{opt}} = 2.5 \mu\text{W}$ [204]

than the receiver with the unseparated photodiode. The maximum data rate DR can be estimated from the measured rise times and fall times by $DR = 1/(t_r + t_f)$. Therefore maximum data rates of 104 Mb/s for the receiver with the unseparated photodiode as well as 292 Mb/s for the receiver with the quartered photodiode can be achieved. For 300 Mb/s and a bit error rate of 10^{-9} , an average optical input power of $1.48 \mu\text{W}$ was determined. Further results of both optical receivers are compared in Table 6.13. DC photo-sensitivities of $36.8 \text{ mV}/\mu\text{W}$ as well as $75 \text{ mV}/\mu\text{W}$ were measured. The photo-sensitivity of the receiver with the quartered photodiode was 2.04 times higher than the photo-sensitivity of the standard receiver due to the resistance ratio R_2/R_1 , which defines the amplification of the summation amplifier (Fig. 6.189b). The simulated values of the input-referred spectral noise densities at 100 MHz are shown in Table 6.13, which could not be measured because of bad noise behavior of the picoprobe. The lower noise current density of the receiver with the quartered photodiode is the result of the lower capacitance of each of the quarter photodiodes. The power consumption of each amplifier was 5.2 mW. Since the power consumption of the output driver consisting of a source-follower stage (not shown in Fig. 6.189a, b) was 18.8 mW, the values of 24 and 44.7 mW resulted for the two different sensors [204].

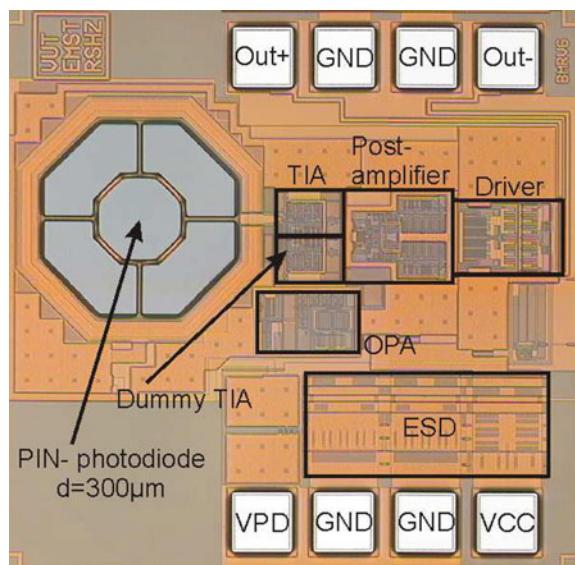
An optical sensor using a quartered photodiode, four transimpedance amplifiers and a summation amplifier was presented. This new concept allowed speed and sensitivity enhancement of optical sensors with large-area photodetectors [204]. With a PIN photodiode of $400 \mu\text{m}$ in diameter, a POF receiver achieved a maximum data rate of 300 Mb/s with a sensitivity of -28.3 dBm compared to values of 20 Mb/s and -20 dBm , respectively, reported in [202].

A 2.5 Gb/s receiver OEIC using the pin photodiode of Fig. 2.63 [112] with a diameter of $300 \mu\text{m}$ was introduced in [205]. The receiver circuit was basically the same as in [126], which is described in Sect. 6.4.13 (subsection on BiCMOS receivers) and shown in Fig. 6.108. The much larger photodiode area and its therefore much higher photodiode capacitance will reduce the sensitivity compared to the

Table 6.13 Comparison of the optical sensors with unseparated and quartered photodiode ($\lambda = 670$ nm, VDD = 5 V) [204]

	Unseparated photodiode	Quartered photodiode
Photo-sensitivity (mV/ μ W)	36.8	75.0
Bandwidth (MHz)	79.1	223
Rise time (ns)	5.11	1.70
Fall time (ns)	4.55	1.73
Input-referred spectral noise current density at 100 MHz (pA/ $\sqrt{\text{Hz}}$)	5.35	3.29
Power consumption (mW)	24.0	44.7

Fig. 6.193 Microphotograph of receiver with large-diameter pin photodiode

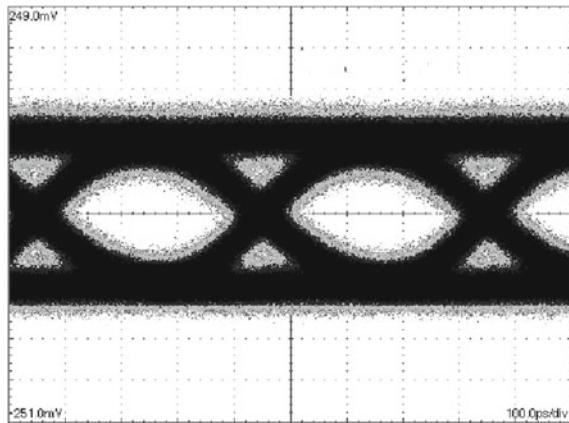


receiver described in Sect. 6.4.13 and Fig. 6.108 according to the noise theory of Chap. 5. In fact, however, this OEIC in 0.5 μ m BiCMOS was designed to show its superiority compared to a GaAs-HEMT OEIC with MSM photodiode having the same photodiode diameter [206].

The feedback resistor in the TIA had a value of 840 Ω , which is a lower value compared to the receiver of [126], because of the much larger photodiode area. The chipphoto of this large-area pin-photodiode receiver is shown in Fig. 6.193. Its chip area is 870 \times 890 μm^2 , which is much smaller than the 4.5 mm² of the GaAs-HEMT OEIC of [206]. In addition the power consumption of the 0.5 μ m silicon BiCMOS OEIC was 170 mW instead of 500 mW [205].

The large-area pin-photodiode OEIC showed a measured -3 dB bandwidth of 1.35 GHz at 660 nm. The measured sensitivity for PRBS31 at this wavelength was

Fig. 6.194 Measured eye diagram of receiver with large-diameter pin photodiode at 2.5 Gb/s with 660 nm, PRBS31, BER = 10^{-9} and an average optical input power of -20.1 dBm



-20.1 dBm at 2.5 Gb/s [205]. Figure 6.194 shows the eye diagram for this optical power at 2.5 Gb/s. With 850 nm wavelength the measured sensitivity of the $0.5 \mu\text{m}$ BiCMOS OEIC at 2.5 Gb/s was -17.2 dBm compared to -15.7 dBm of the GaAs-HEMT OEIC [206].

Receivers for Multi-level Transmission

Usage of more than two signal levels can increase the amount of transmitted data. In contrast to binary optical receivers, which typically implement limiting post amplifiers, multi-level optical receivers need linear TIAs and linear post amplifiers.

The block diagram of the multi-level optical receiver front-end is shown in Fig. 6.195. The first element in the optical receiver is the PIN photodiode. There are two identical PIN photodiodes, one to receive the optical signal and the other is shielded to balance the differential transimpedance amplifier (TIA). This improves the power supply rejection ratio very efficiently. The large diameter of the PIN photodiode ($300 \mu\text{m}$) makes the use of large core diameter POF easier. The PIN photodiode is followed by a TIA which converts the photocurrent coming from the PD into a voltage. An automatic gain control circuit (AGC) controls the gain of the TIA in order to avoid the overloading of the TIA and to increase the dynamic range of the optical receiver. This wide dynamic range for the optical receiver allows using it to receive multi-level signals. The use of multi-level signals instead of binary signals allows the use of an optical receiver with a smaller bandwidth and relaxes the frequency constraints on the circuit design. On the other hand the circuit complexity increases since the receiver must deliver a linear response over a large dynamic range. This leads to a more sophisticated design of the AGC compared to the conventional receiver, where a significant part of the large dynamic range is realized with simple limiting amplifiers. So, the conventional limiting receiver for binary data will not amplify the different symbol levels equally. As a result, the voltage levels for the output signal will not be equally spaced. This fact will make the signal detection and decoding

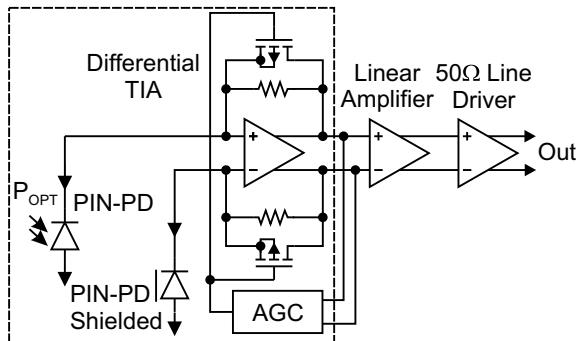


Fig. 6.195 Block diagram of a multi-level POF receiver

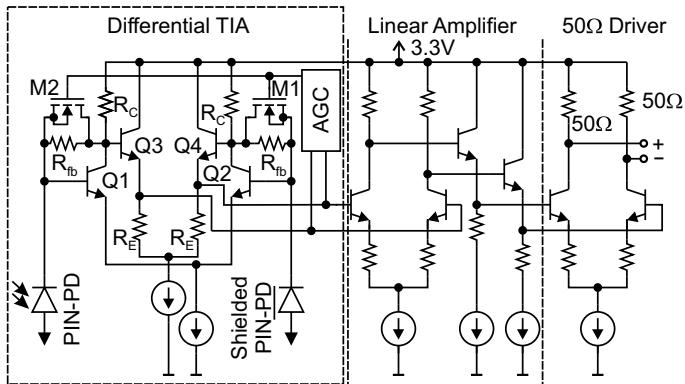


Fig. 6.196 Circuit diagram of multi-level POF receiver [207]

more difficult or even impossible. However, the wide range linear AGC-receiver has variable gain and always operates in the linear region. As a result, each level of the output multi-level signal will be amplified by the same gain. The complete front-end is designed for a symbol rate of 1.25 Gbaud and a maximum overall transimpedance of approximately $40\text{ k}\Omega$. The front end is supplied by a single 3.3 V supply voltage. The last stage in the front-end, which forms the interface with the following off-chip signal processing units, is a 50Ω output driver (Fig. 6.196). The micrograph of the fabricated optical receiver in $0.6\text{ }\mu\text{m}$ BiCMOS with the two integrated PIN photodiodes is shown in Fig. 6.197.

The optical receiver's frequency response was measured with a network analyzer (HP 8753E). A calibration was performed to cancel the effect of the laser source and the connected measurement cables on the receiver frequency response. The measured receiver's -3 dB bandwidth was 622 MHz. With this bandwidth a data rate of 1.25 Gbit/s can be received using binary signals. The data rate can be doubled to 2.5 Gbit/s by using 4-PAM signaling at the same bandwidth. Sensitivity measurements were carried out at 660 nm wavelength. For these measurements a red VCSEL

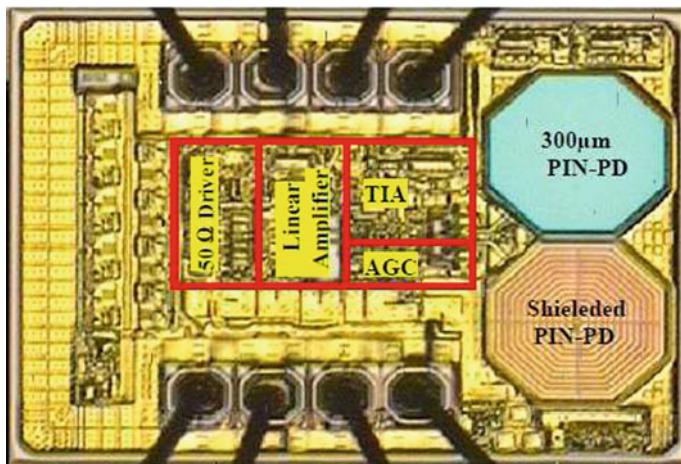
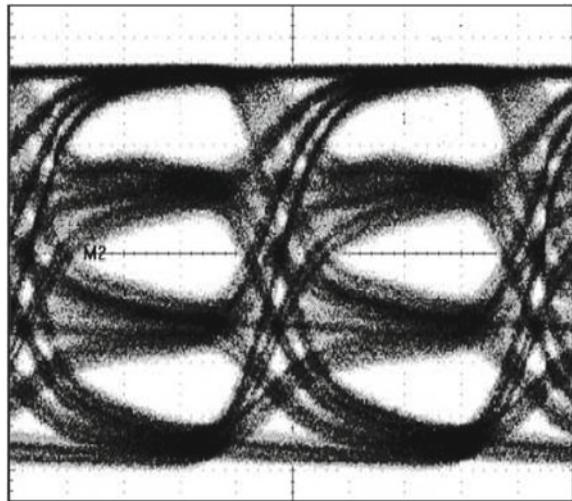


Fig. 6.197 Microphotograph of multi-level POF receiver

was modulated by a pseudo-random bit sequence (PRBS) with a length of $2^{31} - 1$. A communication signal analyzer was used to analyze the output signal and to determine the bit error rate of the optical receiver. For a bit error rate of 10^{-9} the measured sensitivity was -24 dBm . In the beginning of our multilevel experiments the 4-PAM signal is generated using the method introduced in Sect. 2.6.1, Figs. 2.6 and 2.7 in [201]. Due to the bad source's eye diagram generated by this method the transmitted data rate was limited to 1.4 Gbit/s . The measured output voltage of the optical receiver is constant and equal to 750 mV for any input optical power of the highest level larger than $20 \mu\text{W}$. This results in equally spaced levels (e.g. 250 mV for $M = 4$) due to the long time constant (about $100 \mu\text{s}$) of the AGC and enables the correct detection of the multilevel signal at constant threshold voltages. Figure 6.198 shows the measured output eye diagram of the optical receiver using a 4-PAM signal at $\text{DR} = 1.4 \text{ Gbps}$, $\text{PRBS } 2^{31} - 1$, a wavelength of 675 nm and an average optical power of -11 dBm . The eye diagram for the 4-PAM signal shows an equal eye opening for each level. For sensitivity measurements a fast 670 nm laser diode was modulated by 4-PAM with a PRBS length of $2^7 - 1$ at different optical power levels. Another sensitivity measurement was made with a PRBS length of $2^{31} - 1$. A communication signal analyzer (CSA8000) was used to analyze the output signal eye diagram, measure the mean voltage level and the noise variance for each level which was used to calculate the symbol error rate (SER) from relation (2-22) in [201].

The SER for $\text{DR} = 1 \text{ Gbps}$, 1.4 Gbps and $\text{PRBS} = 2^7 - 1$ as well as $2^{31} - 1$ is calculated after laser extinction ratio correction from 3.5 to 10 was made using equation (4-6) in [201]. The proposed optical receiver reaches sensitivities of -14.8 and -11.9 dBm for DR of 1 and 1.4 Gb/s , respectively, at a wavelength of 675 nm with a BER of 10^{-9} and a PRBS length of $2^7 - 1$. With a PRBS length of $2^{31} - 1$ and under the same conditions, sensitivities of -12.1 and -11.2 dBm for DR of 1 and

Fig. 6.198 Measured eye diagram of a 4-PAM signal (PRBS = $2^{31} - 1$, 1.4 Gb/s and Popt = −11 dBm) [207]



1.4 Gb/s were measured [207].

Highly Linear POF Optical Receiver

Many researchers proved that by using multicarrier modulation schemes like OFDM the POF bandwidth limitations can be overcome. OFDM is seen as promising technology for low-cost Gigabit transmission over step-index POF (SI-POF) [208]. A major problem of OFDM is that the multicarrier signals usually have a large envelop fluctuation. This means that the peak-to-average power ratio (PAPR) of multicarrier signals can be high. These large peaks increase the amount of intermodulation distortion (IMD) resulting in an increase in the error rate. A high-linearity receiver with AGC is required for OFDM to reduce the IMD. The AGC adjusts the gain of the amplifier to obtain the desired output signal strength. In conventional AGCs the signal amplitude is typically estimated using a peak detector. This adequately works for signal amplitudes with fixed PAPR such as sinusoids, but is unreliable for high-PAPR signals. These issues excluded the use of a conventional AGC with OFDM [209]. The wireless local area network receiver presented in [209] implemented an AGC, which uses RMS detection. This was found to be adequate for estimating the OFDM amplitude by integrating for the duration of a training symbol. Here an integrated linear optical receiver consisting of a TIA with AGC followed by an amplifier and a line driver is presented. Additionally two main control loops are present, one for background-light (BGL) cancellation and one for the gain control. The speciality of this linear optical receiver is that the gain is only controlled by BGL, which is always present in optical transmission systems due to laser diode biasing above the threshold (limited extinction ratio). Compared to peak-detecting AGC commonly used a better linearity can be achieved with this BGL-AGC especially for pulsed signals or more general signals with a high PAPR where the pulse repetition rate is

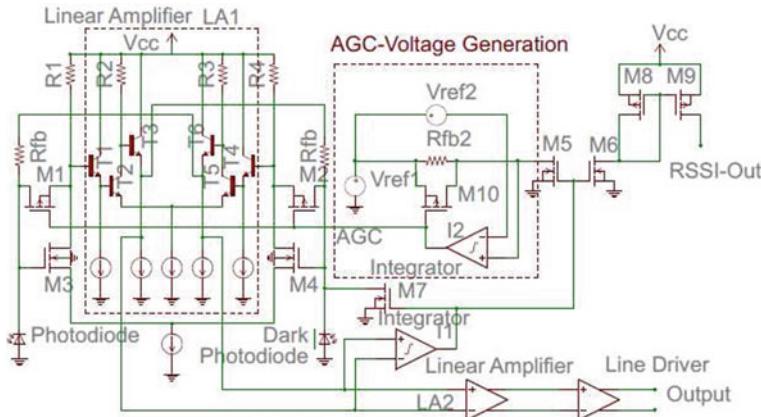


Fig. 6.199 Highly linear integrated optical receiver [210]

low. When peak detection is used with this kind of signals, large storage capacitors would be necessary to store the peak value. Additionally large capacitors cannot easily be charged very fast and accurate. Here these large capacitors are not needed with the BGL-AGC [210]. Nearly all the previous attempts to design a linear optical receiver for short-range communication include only simulation results. No measurements were presented to verify the optical receiver linearity. A CMOS common-gate differential TIA was presented in [211] to obtain a better linearity and to reduce the IMD. A 40 dBc third-order intermodulation product (IMP3) was obtained using HSPICE. Reference [212] has shown analytically that there are significant benefits in linearity when choosing common-emitter feedback (CEFB) over traditional resistive feedback. There, CEFB had an output third-order intercept point of 23 dBm.

Figure 6.199 shows the circuitry of the integrated optical receiver. There are two identical $400\text{ }\mu\text{m}$ diameter Si PIN-photodiodes. One receives the optical signal and the other is kept dark. The integrated large-area photodiode (PD) makes it easy to couple and position the large-core POF. The dark PD is used to balance the differential TIA which has two amplifying stages and two feedback resistors (Rfb). The differential topology of the TIA has the advantage of high immunity against common-mode and power supply noise. The input referred noise current of this TIA is 70 nA . The PD antireflection coating is optimized for red light with a responsivity of 0.5 A/W . The first stage is a differential MOSFET amplifier (M3, M4) which is shunted by PMOSFETs (M1, M2) to reduce the gain of the TIA by a steering voltage. The second stage of the TIA is a linear amplifier (LA1) consisting of a bipolar differential stage with emitter followers. This configuration of the TIA has two big advantages: first a very wide dynamic range of the TIA can be achieved without any stability problems, therefore complex and performance critical capacitor switching can be avoided. The second advantage is that large photocurrents (I_{ph}) in the mA-range can be processed if M1 and M2 are fully conductive, since the drain current of the first stage is also in the order of mA to achieve overall low noise.

The first control loop cancels the BGL by injecting a current via M7 into the dark side of the TIA. M7 is steered by an integrator (I1), which senses the differential voltage of the TIA. Therefore the average differential voltage at the TIA output is held at zero. M5 also generates photocurrent (I_{ph}); therefore it is connected to a dummy structure consisting of R_{fb2} and M10. Basically the dummy defines the current transimpedance of the TIA; therefore with a second control loop (I2) the AGC-voltage is controlled in such a way that the voltage at the dummy is held constant for all possible I_{ph} . This voltage is defined by V_{ref2} , and it is a representation of the maximum linear range of the TIA. V_{ref1} is a reference voltage of the dummy circuit of R_{fb2} and M10 which give a bias voltage equal to the voltage at the TIA (M3 and M4 drain voltages). The output voltage will be constant over a wide input optical power range for a fixed extinction ratio (ER). M6, M8 and M9 replicate the average I_{ph} to a received signal strength indication (RSSI) output for diagnostic purposes. An AGC sets the gain of the TIA to avoid overloading of the TIA and to increase the dynamic range of the optical receiver in the linear region. This wide linear input dynamic range makes the receiver ideally suited for OFDM signals. The AGC circuitry decreases the TIA gain for increasing total input optical power to ensure that the output voltage of the TIA is constant over a wide input dynamic range. As a result, each level of the output multilevel signal will be amplified by the same gain, so the output signal will have equally spaced voltage levels. The AGC outputs control the gate voltage of the PMOS transistors M1 and M2. As the average input optical power increases the AGC output voltage decreases. This leads to a decrease in the PMOS resistance of M1 and M2. Decreasing the PMOS resistance has the effect of decreasing the gain of the TIA. This is due to the shunt configuration between the PMOS and the feedback resistor R_{fb} .

The output signal of the TIA is amplified by a linear post amplifier LA2. The last stage in the receiver, which forms the interface to the following off-chip signal processing unit, is an emitter follower which can drive a load current up to 24 mA. The integrated optical receiver is supplied by a single 3.3 V supply and consumes 33 mW without output load. The test chip is fabricated in 0.6 m technology and has an area of about 0.87 mm² (0.84 mm × 1.04 mm). The optical receiver chip micrograph is shown in Fig. 6.200.

The optical receiver's frequency response was measured with a network analyzer (HP 8753E). A calibration was performed to cancel the effect of the laser source and the connected measurement cables on the receiver frequency response.

The measured receiver's -3 dB bandwidth was 112 MHz at maximum amplification ($300\text{ k}\Omega$) and 280 MHz at the lowest amplification ($2.5\text{ k}\Omega$). With the 112 MHz bandwidth a data rate of 250 Mb/s can be received using a binary signal. The data rate can be doubled to 500 Mb/s by using 4-PAM signaling at the same bandwidth [201]. For sensitivity measurements, a binary and a 4-PAM signal with a symbol rate of 250 Mbaud were generated on a personal computer with MATLAB software. The signals were transmitted by a 12-bit arbitrary waveform generator PCI-Card (Acquitek DA11000-16M). The generated signals were used to modulate a commercial low price 655 nm laser diode with an extinction ratio of ER = 2.5. The optical signal from the laser was transmitted through the single-mode glass optical

Fig. 6.200 Microphotograph of highly linear integrated POF receiver

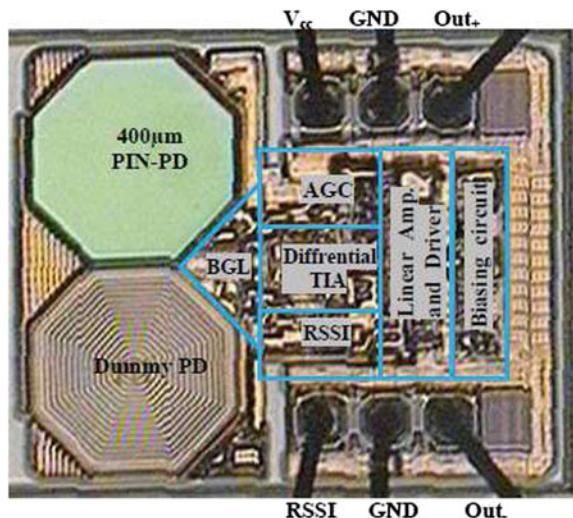
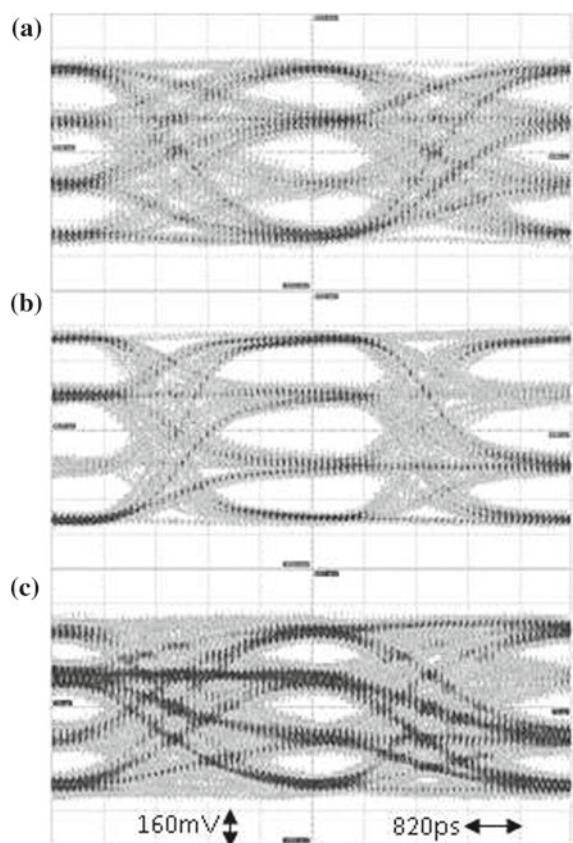


Fig. 6.201 Measured 4-PAM eye diagrams of highly linear integrated POF receiver obtained in back-to-back transmission with 1 m GOF (PRBS11, 500 Mb/s, extinction ratio = 2.5, and received optical power = 8 μ W (a), received optical power = 650 μ W (b), and received optical power = 9 μ W after 40 m PMMA SI-POF (c))



fiber (GOF) and detected by the presented optical receiver. The sensitivities of the optical receiver for binary and 4-PAM signals were measured at different average optical power values. The measured four-level eye diagram shows the receiver's high linearity when the received average optical power changes from 5 to $650\text{ }\mu\text{W}$ (maximum available power in our lab); equally spaced voltage levels and a constant output swing are depicted in Fig. 6.201. The post-layout simulation shows that the receiver can work with a high linearity up to $800\text{ }\mu\text{W}$ average input optical power. A 1-GHz digital oscilloscope (Lecroy 6100) was used to display the output signal, create the 4-PAM eye diagram and to measure the mean value and the noise variance for each signal level which was used to calculate the SER for 4-PAM signal, relation (2–22) in [201]. The measured BER versus the received average optical power for $\text{DR} = 500\text{ Mbit/s}$ and $\text{PRBS} = 2^{11} - 1$ is illustrated in Fig. 6.202. The BER for a binary signal at $\text{DR} = 250\text{ Mbit/s}$ and $\text{PRBS} = 2^{11} - 1$ is also included in Fig. 6.202. The results in Fig. 6.202 consider a laser extinction ratio (ER) correction from 2.5 to infinity. There is a power penalty of 6 dB for 4-PAM compared to binary (4.8 dB theoretically). The extra 1.2 dB penalty is due to laser non-linearity and ISI effects. The proposed optical receiver reaches sensitivity for binary signal of -31 dBm at a DR of 250 Mbit/s at a wavelength of 655 nm with a BER of 10^{-9} and a PRBS length of $2^{11} - 1$. Another receiver presented [213] with AGC-TIA and two integrated $430\text{ }\mu\text{m}$ diameter PDs had an estimated sensitivity of -28 dBm at 10^{-9} BER using a binary signal at a DR of 150 Mbit/s [213]. Our presented receiver shows a better measured sensitivity (3 dB improvement) at nearly the double data rate. The presented optical receiver shows a sensitivity of -25 dBm ($\text{BER} = 10^{-9}$) at $\text{DR} = 500\text{ Mb/s}$ using a 4-PAM signal. There is an improvement by a factor of two in the DR by using the 4-PAM signal compared to binary signal. On the other hand there is a measured power penalty of 6 dB (theoretical value 4.8 dB for $M = 4$). For linearity measurements, the 675 nm laser source with an $\text{ER} = 3$ was modulated by a single tone (20 MHz). The measured THD was 1% at Popt equal to -23 dBm and 1.7% at -3.5 dBm , Fig. 6.203. The receiver THD is actually better, since the laser source alone has a THD of 0.7%. The receiver's simulated THD is less than 0.5% and 0.3% for Popt equal to -3.5 and -23 dBm , respectively [210].

The IMP3 were measured at different Popt values. The fundamental measured power (two tones at 100 and 101 MHz) and IMP3 are plotted in Fig. 6.204. The AGC starts to work at a Popt of -23 dBm . The fundamental frequency of the output signal has a constant output power when Popt increases from -23 to -6 dBm . The IMP3 is less than -40 dBc at Popt less than -6 dBm . For lower frequencies (two tones at 20 and 21 MHz) the optical receiver shows an IMP3 of -50 dBc at $\text{Popt} = -3.5\text{ dBm}$ (Fig. 6.205).

For comparison, the AGC introduced in [214] fabricated in $0.25\text{ }\mu\text{m}$ SiGe BiCMOS technology with an active area of 0.225 mm^2 has a THD of 0.9% at the lowest gain and its low and high cut off frequencies are 68 kHz and 95 MHz, respectively. The presented BGL-AGC circuit has a chip area of 0.16 mm^2 , measured cut off frequencies of 0.6 kHz and 112 MHz, respectively, and a THD of 0.5% at the lowest gain. This comparison shows that our AGC circuit has a better linearity, wider bandwidth and needs a smaller chip area. Also the convergence of the BGL-AGC was

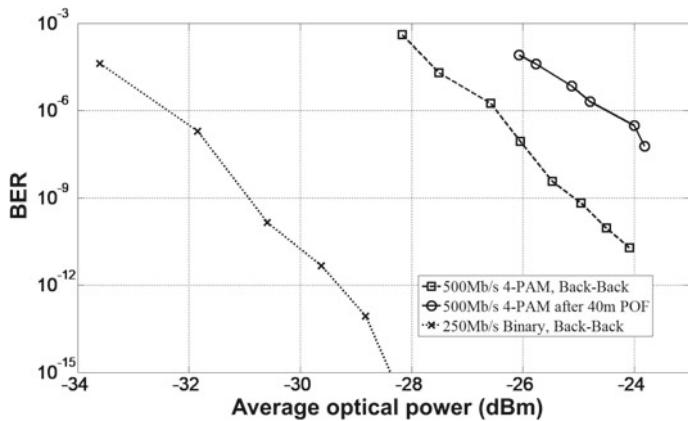


Fig. 6.202 Measured BER versus average optical power for binary and 4-PAM signals of highly linear integrated POF receiver obtained in back-to-back transmission with 1 m GOF as well as after 40 m PMMA SI-POF

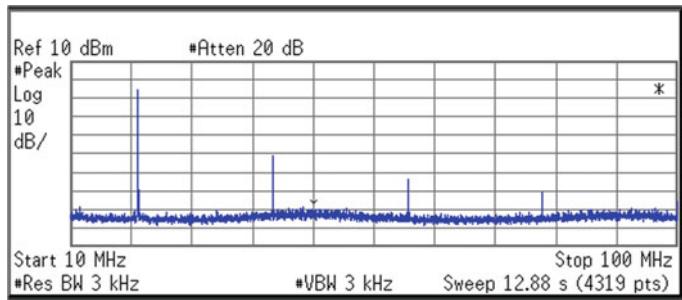


Fig. 6.203 Measured harmonics spectrum of the highly linear integrated POF receiver with single-tone input (20 MHz) at -3.5 dBm average input optical power

simulated using SPECTRE with an OFDM signal. The result for low-gain adjustment from a high input P_{opt} , is shown in Fig. 6.206. At $1\ \mu\text{s}$ the modulation starts and the output signal is constant from onset of modulation. The BGL is always present and constant in a certain optical system, so the BGL-AGC adjusts signals to the desired level instantaneously. As a conclusion the specialty of the presented linear optical receiver is that the gain is only controlled by the background-light (BGL) photocurrent, which results in immediately constant output signals. Compared to peak-detecting AGC commonly used, a better linearity can be achieved with BGL-AGC especially for signals with a high PAPR.

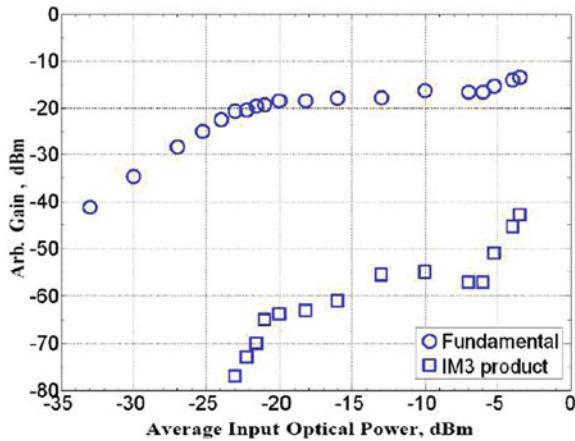


Fig. 6.204 Measured two-tone third-order intermodulation (IMP3) and fundamental power of highly linear integrated POF receiver for fundamentals of 100 and 101 MHz at different average input optical power values

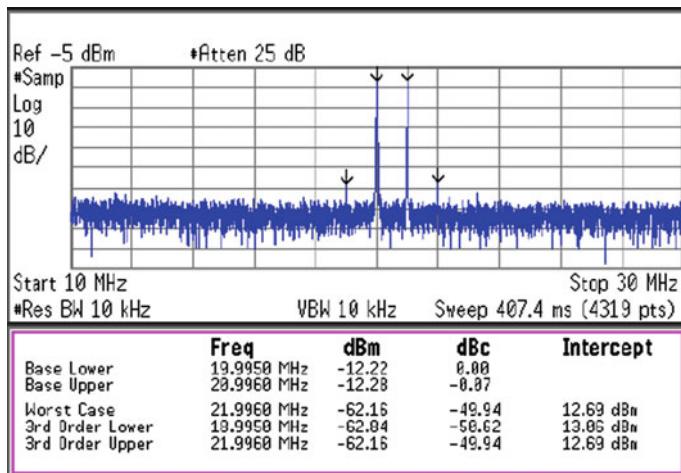


Fig. 6.205 Two-tone third-order intermodulation for fundamentals of 20 and 21 MHz at -3.5 dBm average input optical power values

6.4.19 Burst-Mode Optical Receivers

The demand for broadband access networks has been rapidly increasing in the last years. An asynchronous transfer mode passive optical network (ATM-PON) is one of the best means to satisfy this demand in terms of bandwidth and cost [215]. Figure 6.207 shows an ATM-PON system in which several Optical Network Units (ONUs) are connected to an Optical Line Terminal (OLT) through optical fiber and

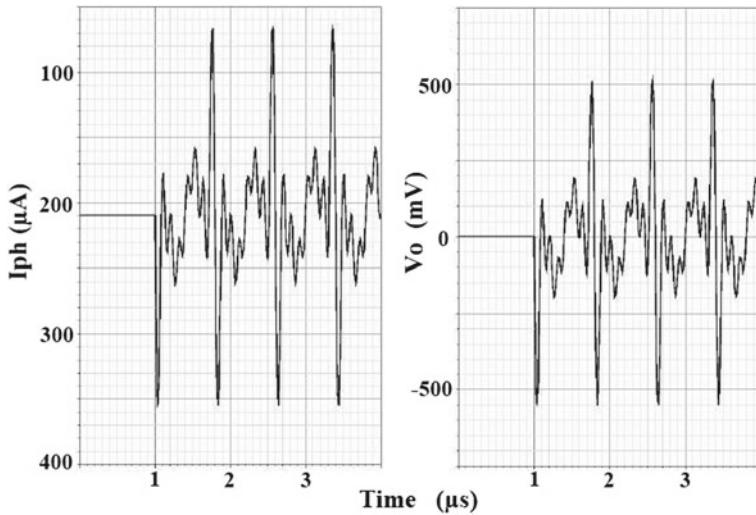
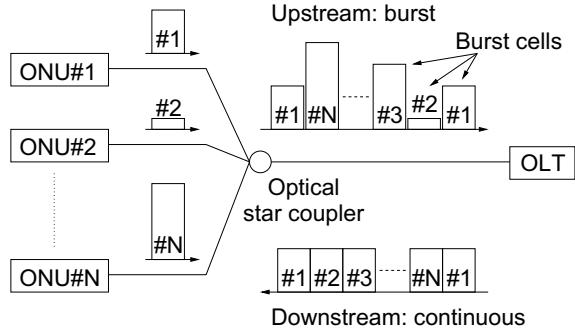


Fig. 6.206 AGC performance with OFDM signals in low-gain adjustment for a background-light input optical power of -3.5 dBm when modulation starts at 1 smus (left: input photocurrent, right: receiver output)

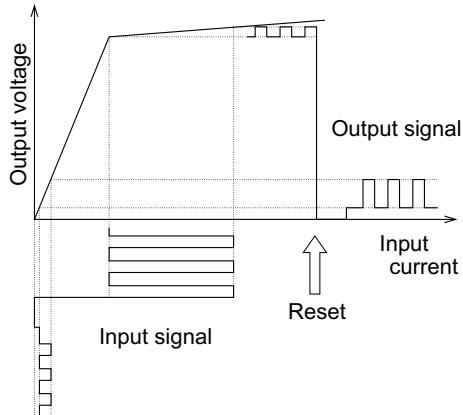
Fig. 6.207 Principle of optical burst-mode transmission [216]



a 1:N star coupler. The downstream transmission is in continuous mode whereas the upstream transmission is in cell-based Time Division Multiple Access (TDMA) burst mode. In downstream direction each ONU receives packages with constant optical power. There can be large differences in received optical power between different ONUs, however, depending on the fiber length between individual ONUs and the star coupler. As a consequence of the different fiber length resulting in different attenuation of the signals sent by the ONUs, the OLT receives packages with different optical power. The sensitivity of the OLT receiver, therefore, has to be changed very fast between two cells. The name burst mode stems from the different signal height of the cells received by the OLT.

According to the global standard G.983.1 class C announced by ITU-T in 1998, the burst cells at an OLT can have a very large power difference [216]. In addition,

Fig. 6.208 Operation of bit-AGC [216]



the laser diodes are biased above threshold to achieve a high data rate and a low jitter. The receiver in an OLT, therefore, must realize high sensitivity, wide dynamic range (more than 30dB difference between strong and weak cells), and it must receive signals with an extinction ratio as low as 10dB.

Conventional preamplifiers, which control their transimpedance bit by bit have problems to receive large signals with a low extinction ratio because of the nature of logarithmic amplifier operation [217–220]. In these preamplifiers, a current-bypass diode or current-bypass circuit is connected in parallel with the feedback resistor. When the output voltage of the transimpedance preamplifier exceeds the turn-on voltage of the bypass circuit, current flows through this circuit lowering the transimpedance. This type of transimpedance control was called bit-AGC (bit automatic gain control) in [216].

If a large input signal with a low extinction ratio is applied to such a bit-AGC preamplifier, the output waveform has a large dc part (see Fig. 6.208). The ac amplitude of the output signal is therefore reduced and it is difficult to decide between “0” and “1” properly. To solve the problem of output signal reduction, a novel circuit controlling the transimpedance cell by cell was proposed [216]. This type of control was called cell-AGC. The cell-AGC (see Fig. 6.209) is based on a bottom level detector (BLD), a gain control circuit (GCC), a reset circuit, and a MOSFET connected in parallel with the feedback resistor.

BLD has quickly to detect the output signal of the three-stage transimpedance amplifier. A capacitor in BLD holds this bottom level. Depending on this level, the GCC generates a constant voltage during operation in a cell and determines the resistance of the MOSFET connected in parallel to R_f via its gate source voltage V_{GS} .

Between two cells, the reset signal is applied to BLD, the hold capacitor is charged, and the output of GCC returns to its initial state [216]. To increase transmission quality, a fast response from BLD and GCC is necessary during the the first bit in the new cell. The response of cell-AGC to input signals with different power levels

Fig. 6.209 Block diagram of 3-stage burst-mode receiver [216]

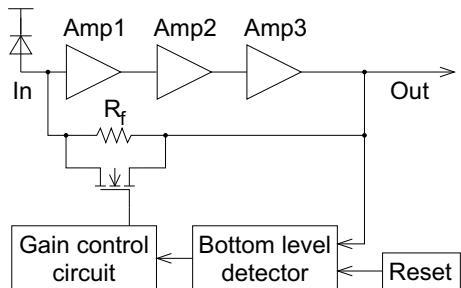
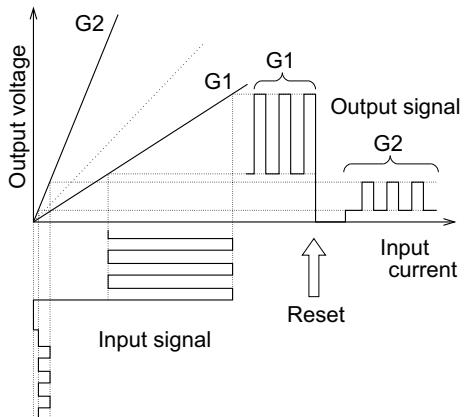


Fig. 6.210 Operation of cell-AGC [216]

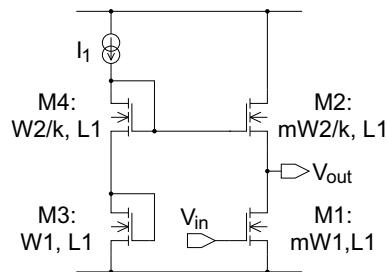


is illustrated in Fig. 6.210. For a large-signal cell, the transimpedance is set to G_1 instead of G_2 for a weak-signal cell. Because the output voltage is proportional to the input current, the dc background level for the “0” level is not as large as that in bit-AGC. With the help of this circuit, therefore, a decision between “0” and “1” can be performed properly and burst cells with a low extinction ratio can be received.

A $0.25\text{ }\mu\text{m}$ CMOS technology was selected for the realization of the cell-AGC burst-mode receiver aiming at noise reduction for a high sensitivity. A feedback resistor with a value of $40\text{ k}\Omega$ was implemented in the transimpedance preamplifier. The transconductance g_m of the input MOSFET was set to about 50 mS . Stability is the major problem to be solved for three-stage transimpedance amplifiers. Therefore, the influence of changes in g_m with process deviations on the stability has to be suppressed and the value of g_m has to be kept close to the minimum for a low power consumption. This requirement can be met with the series MOSFET load configuration shown in Fig. 6.211. Each of the three amplifier stages in Fig. 6.209 consists of the circuit shown in Fig. 6.211.

Due to the condition of $V_{in} = V_{out}$ for negative feedback, V_{GS} of M1 is equal to V_{GS} of M3 and V_{GS} of M2 is equal to V_{GS} of M4. The transconductances are given by:

Fig. 6.211 Configuration of g_m -over- g_m amplifier stage [216]



$$g_{m1} = \sqrt{2\mu_n C_{ox} \frac{mW_1}{L_1} I_1 g_{m2}} = \sqrt{2\mu_n C_{ox} \frac{mW_1}{kL_1} I_1} \quad (6.107)$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per area, I_1 is a reference current, and k is the ratio of the gate widths. The gain of this amplifier is equal to the ratio of the transconductances. This amplifier therefore is called g_m -over- g_m amplifier.

$$G = \frac{g_{m1}}{g_{m2}} = \sqrt{k} \quad (6.108)$$

The gain G of such an amplifier stage only depends on the parameter k . It is completely independent from process deviations and operating temperature. The current flowing through M1 is $m \times I_1$, such that the gain G and g_m can be stabilized also under power supply deviations. As G is stabilized, the bandwidth $f_{3\text{dB}}$ is kept stable, i.e. constant, due to the relation $f_{3\text{dB}} = \frac{1+G}{2\pi R_f C_f}$. The bandwidth — important for constant integrated noise — therefore can be designed to be stable around the optimum bandwidth.

The preamplifier in a 0.25 μm CMOS technology with a chip size of $1.3 \times 1.12 \text{ mm}^2$ was characterized at a supply voltage of $2.5 \text{ V} \pm 5\%$ with an external photodiode having a responsivity of 0.9 A/W ($\lambda = 1.3 \mu\text{m}$) and a capacitance of 0.6 pF [216]. The bandwidth varied from 122 to 164 MHz in the operating temperature range from -40 to $+85^\circ\text{C}$ and also due to remaining R_f and C_f deviations. The power consumption was 60–71.4 mW at 2.5 V supply voltage. A sensitivity of -39.3 dBm for a BER of 10^{-10} at a data rate of 156 Mb/s was reported [216]. The maximum optical input power was -6 dBm .

6.4.20 Deep-Sub- μm Receivers

Optical communications is rapidly expanding into applications in short distance ranges. Low-cost applications like infrared wireless links and fiber-to-the-home (FTTH) are needed. CMOS implementations of optical receivers, therefore, are attractive with respect to costs and system size especially when systems-on-a-chip

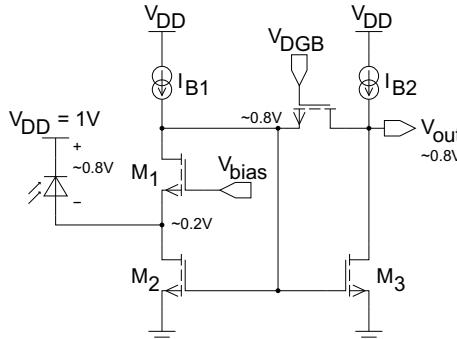


Fig. 6.212 Transimpedance amplifier for operation at 1 V [222]

solutions are considered. But the trend towards lower supply voltages in CMOS poses new problems for the design of transimpedance amplifier front-ends. Traditionally, low-voltage operation has not been a requirement. Below 2 V the performance of conventional transimpedance amplifiers, however, is seriously degraded. One design using low-threshold devices achieved 1.2 V operation at a burst-mode data rate of 50 Mb/s [221]. In [222] an optical front-end for 1 V operation needing no special devices was described.

The difficulties in 1 V operation lie in a wide dynamic range and that the photodiode is provided with a sufficiently high reverse bias voltage in addition to maximizing the gain and the sensitivity for a given bandwidth. The wide-swing low-voltage transimpedance amplifier shown in Fig. 6.212 enables a bias voltage of 0.8 V for the photodiode [222]. The circuit consists of a sub-1 V current amplifier [223] in transimpedance configuration. It achieves a closed-loop gain approaching $-R_f$ for large current gains. The common-gate input stage with M1 sets the input voltage to $V_{bias} - V_{GS1}$ which can be adjusted and reduced to the saturation voltage of transistor M_2 , V_{DSsat2} , to keep M_2 working as a constant current source. The resulting photodiode reverse voltage is $V_{DD} - V_{DSsat2}$ which is about 80% of the 1 V supply voltage [222]. The output is biased at $V_{GS3} = V_{Th,n} + V_{DSsat3}$ and it can swing down to V_{DSsat3} . The amplifier, therefore, has a wide output swing equal to the threshold voltage $V_{Th,n}$ which was about 60% of the 1 V supply voltage in a 0.35 μm CMOS process with a typical threshold voltage of 0.6 V for the NMOS transistor and -0.65 V for the PMOS transistor [222].

By adapting the transimpedance gain in accordance to the signal strength, the dynamic range of the front-end can be further enhanced in addition to a wide output swing. Variable-gain transimpedance amplifiers, however, have been a challenge to stabilize [146]. This problem is overcome in the design described in [222] by replacing the voltage amplifier by a current amplifier [224]. As a consequence, a constant bandwidth being ideally independent of the transimpedance gain is obtained. Out-of-band noise, therefore, is not a matter for this design. An NMOS feedback resistor instead of a PMOS device is preferred because of its lower resistance for

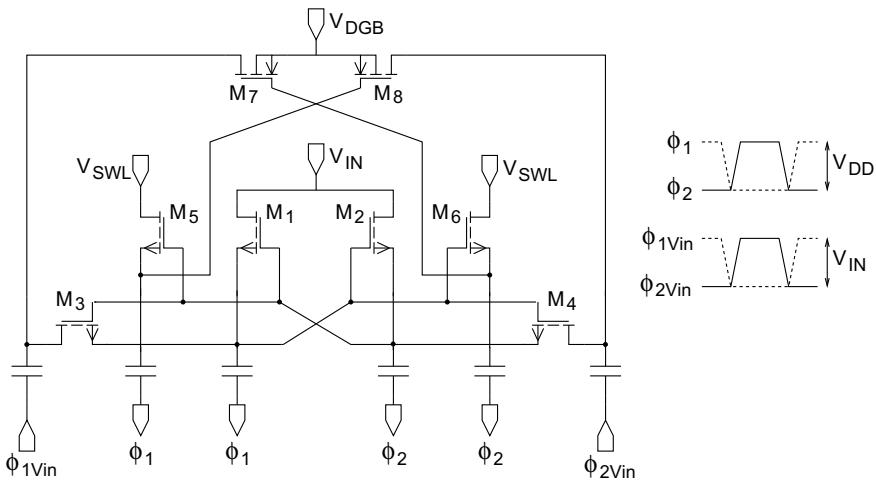


Fig. 6.213 Sub-1 V bias voltage doubler [222]

strong photocurrents. The NMOS feedback resistor realizes soft limiting further enhancing the dynamic range [222]. The source and drain potentials of the NMOS feedback transistor lie near the supply. For a 1 V supply and without low-threshold devices, a charge pump is needed to bias the gate of the NMOS feedback transistor above the supply voltage. For a constant sensitivity of the receiver, the gate bias voltage has to be stable and free of ripple. By driving the gate directly from the output of the charge pump (called dynamic gate biasing: DGB), no current is drawn from the charge pump and the output ripple is minimized. The charge pump is shown in Fig. 6.213.

The charge pump is a voltage doubler with two unique characteristics. First, the voltage doubler has a separate input, V_{IN} , not to double spikes on the front-end supply voltage. Second, in order to overcome the limitation that the charge pump supply voltage must be at least 0.5 V above the threshold voltage [225], the standard charge pump had to be improved to take advantage of the full supply voltage when driving the switches. The improved voltage doubler implements three tightly coupled charge pumps. The inner-most charge pump consisting of the devices M_1 and M_2 generates level-shifted clock signals with the full supply swing. These clock signals are used to drive the outer-most charge pump which performs the actual doubling of the bias voltage using the transistors M_3 and M_4 . The clock signals Φ_{1Vin} and Φ_{2Vin} have a reduced voltage swing which is equal to the input voltage V_{IN} . The final charge pump with transistors M_5 and M_6 generates full-swing clock signals, but here the low level is shifted to V_{SWL} which is optimized for driving the PMOS output switches M_7 and M_8 . The full-swing clock signals Φ_1 and Φ_2 were generated from an integrated, non-overlapping, two-phase clock generator.

The architecture of the optical front-end test chip fabricated in a $0.35\text{ }\mu\text{m}$ CMOS process is shown in Fig. 6.214. The transimpedance amplifier is followed by two

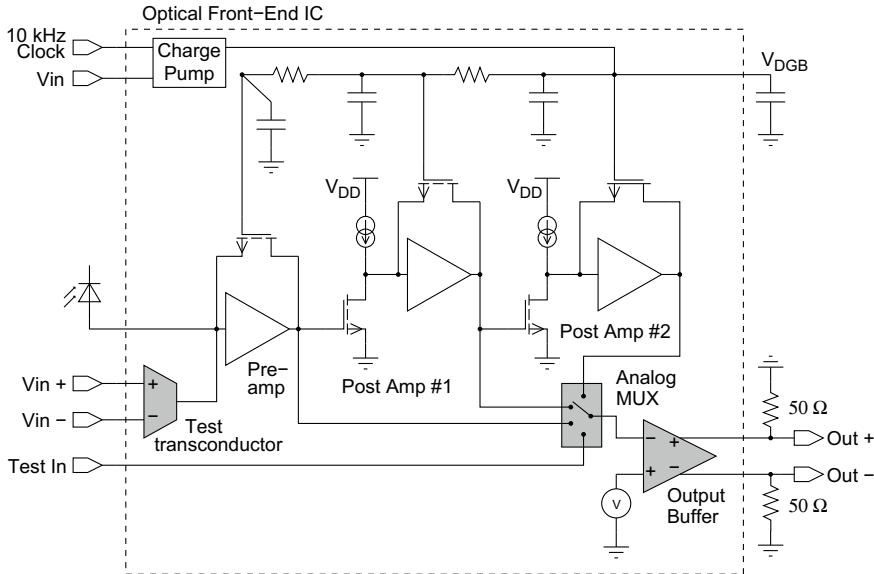


Fig. 6.214 Block diagram of 1 V optical receiver front-end [222]

gain stages that reuse the optimized transimpedance design in a transconductance-transimpedance topology, i.e. the output voltage of a transimpedance stage is converted to a current signal by an NMOS transistor in common-source configuration with a constant current load to obtain a current input signal for the following transimpedance amplifier. RC-filtering of the bias voltage V_{DGB} reduces ripple due to charge injection from the switches and isolates the gain stages in addition. In the test chip, additional circuitry as the test transconductor, an analog multiplexer, and a $50\ \Omega$ output buffer were incorporated. The preamplifier alone achieved a transimpedance gain of $2.4\text{ k}\Omega$ with a bandwidth of 45 MHz, whereas the complete front-end provided an effective transimpedance gain of $210\text{ k}\Omega$ with a bandwidth of 50 MHz [222]. The overall gain of the front-end was adjustable from $210\text{ k}\Omega$ down to $19\text{ k}\Omega$ by changing the gate bias voltage from 1.68 to 2 V [222]. At the maximum gain the input-referred noise current density was $11\text{ pA}/\sqrt{\text{Hz}}$. Operation at 75 Mb/s was demonstrated with a photodiode having a capacitance of 1 pF [222]. A maximum photocurrent of $40\ \mu\text{A}$ was reported. The active chip area was 0.13 mm^2 and the total test chip area was 1.6 mm^2 . The power dissipation was 1 mW at 1 V.

6.4.21 Receivers Aiming Towards the Quantum Limit

Due to their very high gain, SPADs can eliminate the limits set by electronic noise and the ultimate sensitivity of optical receivers using ideal SPADs is determined by

the Poisson statistics (see Sect. 5.4.10). An ideal SPAD would have a photon detection probability (PDP) of 100%, zero dark count rate (DCR) and zero afterpulsing probability (APP). Real SPADs, however, suffer from lower PDP and DCRs up to several 10 kcps as well as APP often larger than 1%. Therefore, a SPAD firing may be from a dark count or an afterpulse, i.e. a logical 1 instead of a logical 0 may have been detected. To reduce the probability of such bit errors below the limits being necessary for successful error correction [226, 227], several SPADs and detection of a photon in some of them will be necessary. As a first attempt to come closer to the quantum limit (see Sect. 5.4.10) than receivers using APDs in the linear mode, a 4-channel SPAD receiver (see Fig. 6.215a) was designed [184]. This receiver was fabricated in 0.35 μm CMOS and uses 4 thick SPADs (see Sects. 2.2.12 and 2.2.13). The SPAD array had a diameter of 200 μm . A cascaded active quencher (see Fig. 6.215b) was implemented to achieve a maximum excess bias voltage of 6.6 V using the fast MOS-FETs of this technology developed for a supply voltage of 3.3 V. The chip photo of this SPAD receiver is shown in Fig. 6.216. A quenching circuit (QC) has a size of 134 \times 130 μm .

With a detection threshold of 100 mV below V_{PLUS} ($V_{\text{PLUS}} = 6.6 \text{ V}$, $V_{\text{REF}} = 6.5 \text{ V}$) the transistor M5 switched on 560 ps after this detection and discharged the SPAD completely in another 440 ps according to postlayout simulations when using an SPAD capacitance of 60 fF. Therefore, after the absorption of a photon, the SPAD quenches passively via M1 until M5 takes over actively. After a recovery time, which was implemented as 6.5 ns, the lower switch S_{Li} , i.e. M5, is opened and the upper switch S_{Ui} , i.e. M2, is closed and charges the SPAD's cathode to 6.6 V with a slew rate of 4.5 V/ns, i.e. in approximately 1.5 ns. The total dead time therefore was about 9 ns [184].

For data transmission experiments, a high-extinction-ratio 635 nm light source was modulated by a bit pattern generator and the bit stream (NRZ PRBS7 or RZ with duty ratio of 0.5 for 50 Mb/s and 0.1 for 100 Mb/s) was coupled to the 4-SPAD array via an adjusted optical fiber within a dark box. The four outputs were connected to a 4-channel 5 GS/s oscilloscope with 8-bit resolution and data blocks of 2 ms lengths were recorded. Data streams of 10^6 bits were post-processed and compared to the input data streams with MATLAB on a personal computer. Digital and analog post processing were performed [184]. The obtained BER results are shown in Fig. 6.217.

For 50 Mb/s in NRZ and $\text{BER} = 2 \times 10^{-3}$, an average optical input power of 4 nW or -54 dBm was necessary with analog post-processing. With digital post-processing, 7.6 nW or -51.2 dBm was necessary. Using RZ (duty ratio 0.5) improved the sensitivities to 2.7 nW or -55.7 dBm for analog post-processing and to 4.3 nW or -53.7 dBm for digital post-processing.

For 100 Mb/s in RZ (duty ratio 0.1) and $\text{BER} = 2 \times 10^{-3}$, an average optical input power of 7 nW or -51.6 dBm for analog post-processing and of 16.5 nW or -47.8 dBm for digital post-processing was necessary. Because of the rather long dead time of 9 ns compared to the duration of a bit of 20 ns at 50 Mb/s, RZ leads to a better sensitivity. The reason why analog post-processing leads to better sensitivities than digital post-processing is that from detection of a photon in a channel this channel stays dead with digital post-processing until the next bit starts and this can

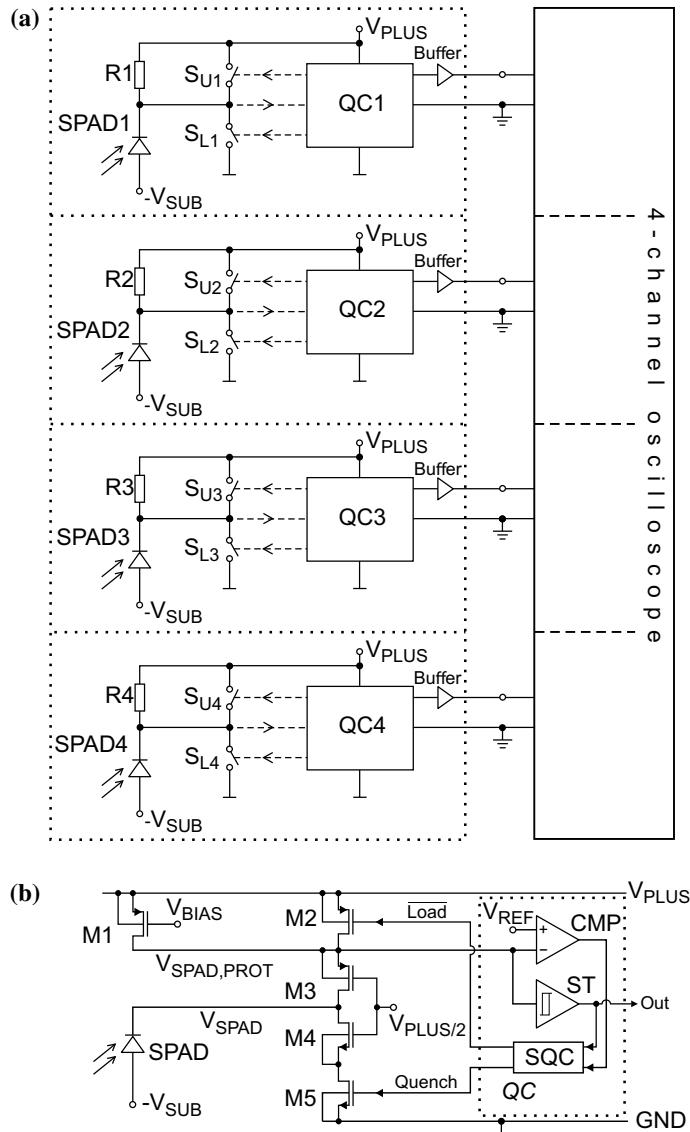


Fig. 6.215 Block diagram of 4-channel SPAD optical receiver (a) and principle of quenching circuit (b) [184]

Fig. 6.216 Microphotograph of 4-channel SPAD optical receiver

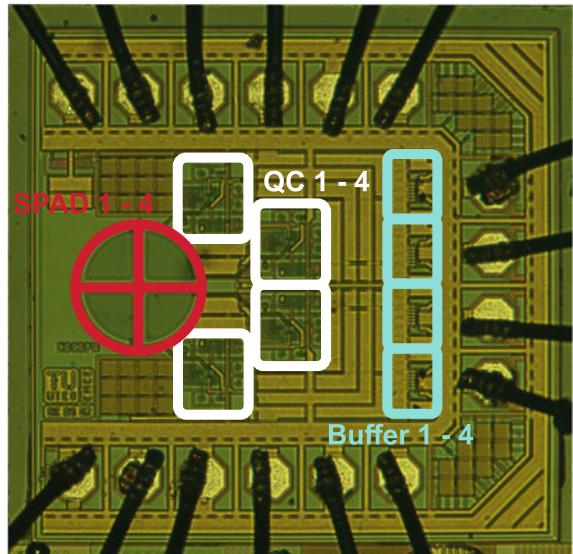
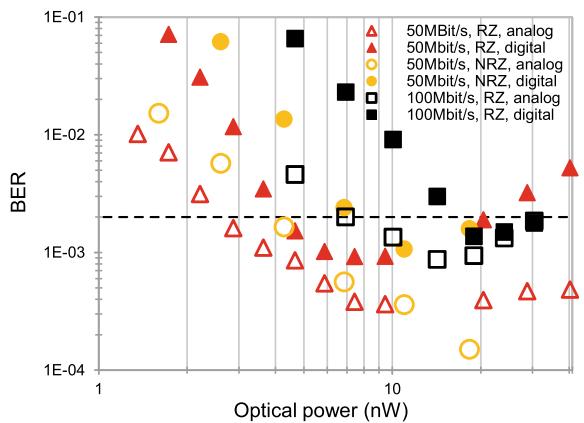


Fig. 6.217 Bit error rate in dependence on average optical input power



take longer than the dead time of 9 ns. In the analog post-processing filtering helped in addition to improve the sensitivity [184].

These sensitivity results were better than those of linear-mode APD receivers (see also Fig. 6.233). The $400\text{ }\mu\text{m}$ APD receiver of [175] had a sensitivity of -33.9 dBm at 500 Mb/s and 675 nm ($\text{BER} = 10^{-9}$), which corresponds to a distance of 24.4 dBm to the quantum limit. The distance to the quantum limit of the receiver described in [228] with a sensitivity of -38 dBm at 280 Mb/s and 860 nm was 23.8 dB ($\text{BER} = 10^{-9}$). The distance to the quantum limit of -55.7 dBm of the 4-SPAD receiver at 50 Mb/s and 635 nm light wavelength is 18.7 dB compared to the distance of a 32×32 SPAD receiver from -31.7 dBm to the quantum limit of 31.8 dB at 100 Mb/s and 450 nm [229]. It should be mentioned that the receiver of [229] was

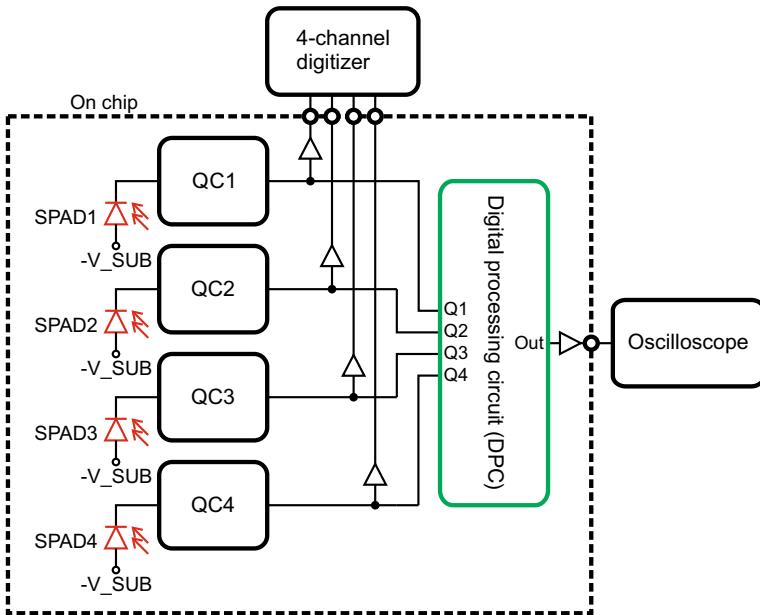


Fig. 6.218 Block diagram of 4-channel SPAD optical receiver with on-chip digital processing [230]

designed for a high dynamic range and that it achieved a BER of 10^{-9} . The APD receivers were also characterized for a BER of 10^{-9} .

In a next step the digital post-processing was included in the SPAD receiver chip, the diameter of the 4-SPAD array was reduced to $117.4\text{ }\mu\text{m}$ and a shorter dead time of 3.5 ns was implemented in the receiver published in [230] to reach a higher data rate. The same $0.35\text{ }\mu\text{m}$ CMOS technology was used for fabrication as for the SPAD receiver of [184]. The block diagram of the new receiver is depicted in Fig. 6.218.

The schematic diagram of the digital processing circuit (DPC) is shown in Fig. 6.219. The inputs Q1 to Q4 are connected to the outputs of the four quenching circuits. A “1” from a quencher output is latched in a D-flip-flop (DFF) with the help of three inverters generating a falling edge to the clock input of the DFF. The DFFs are enabled during a bit and they are reset at the end of the bit with the Dump input. The outputs of the DFFs are combined by an AND gate. A “1” is stored in DFF5 only when all four SPADs showed an avalanche event in the same bit. To optimize the sensitive time, the read out is made 1.5 ns before the latches are reset.

The microphotograph of the SPAD receiver is shown in Fig. 6.220. Its chip area is $1400 \times 1040\text{ }\mu\text{m}^2$. Each quencher occupied an area of $130\text{ }\mu\text{m}$ in square. The digital block was only 0.014 mm^2 in size. The outputs and buffers of all four quencher outputs were present for characterization purposes; if they are omitted a large part of the chip area can be saved.

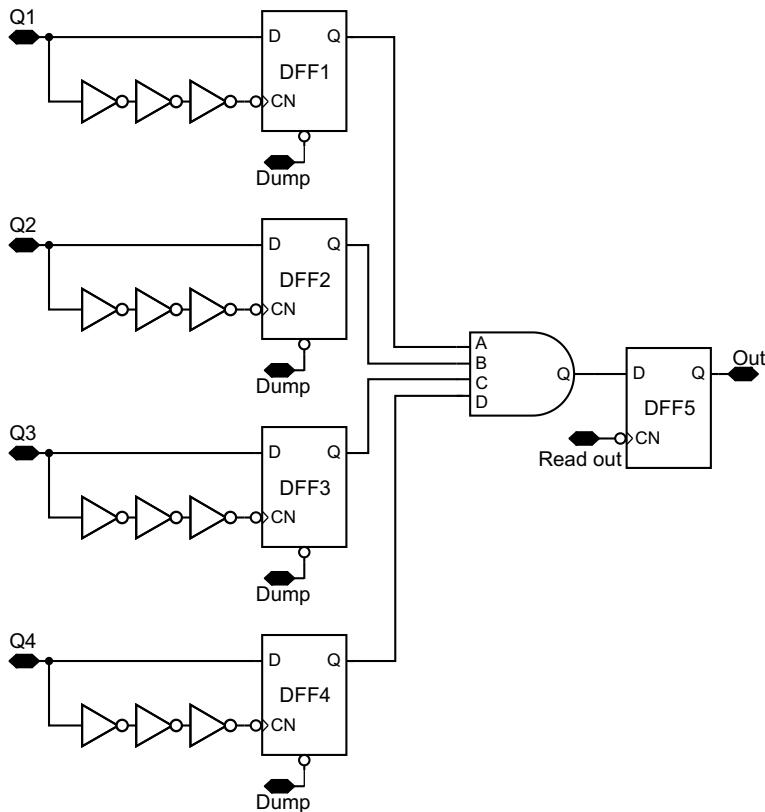


Fig. 6.219 Digital processing circuit (DPC) [230]

Return-to-zero (RZ) data coding with a 20% duty cycle was used for the characterization of the receiver. Digital latch-type processing of the 4 quencher outputs with MATLAB was compared to on-chip integrated digital processing. Figure 6.221 shows the BER at 50 Mb/s for thresholds of 1, 2, 3, and 4 avalanche events with digital MATLAB processing and for a fix threshold of 4 avalanche events with the integrated DPC. Figure 6.222 shows the BER at 100 Mb/s also for thresholds of 1, 2, 3, and 4 avalanche events with digital MATLAB processing and for a fix threshold of 4 avalanche events with the integrated DPC. The dash-dotted line represents the BER of 2×10^{-3} necessary for concatenated Reed-Solomon forward error correction [226, 227]. The dashed line represents the BER of 6.5×10^{-3} necessary for e.g. a RS(255,239)/CSOC super FEC code [227]. For BER = 2×10^{-3} at 50 Mb/s the sensitivity was -51.2 dBm (7.6 nW) with MATLAB post-processing and -51.4 dBm (7.2 nW) with the integrated DPC. At 100 Mb/s, the sensitivity was -46.1 dBm (24.7 nW) with MATLAB processing and -46.3 dBm (23.5 nW) with the

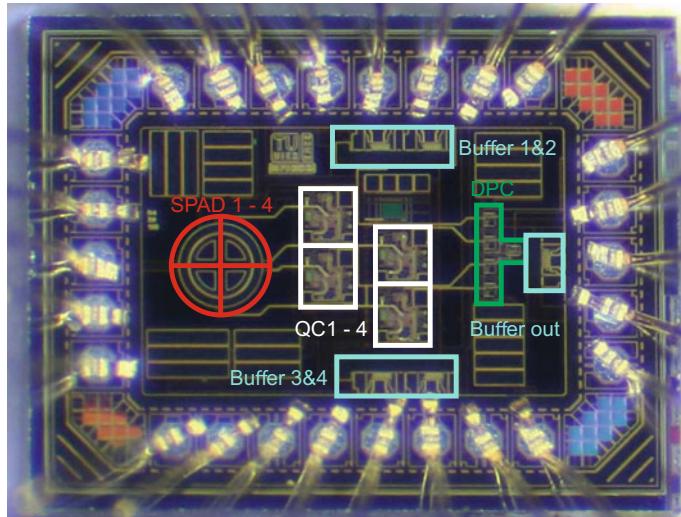
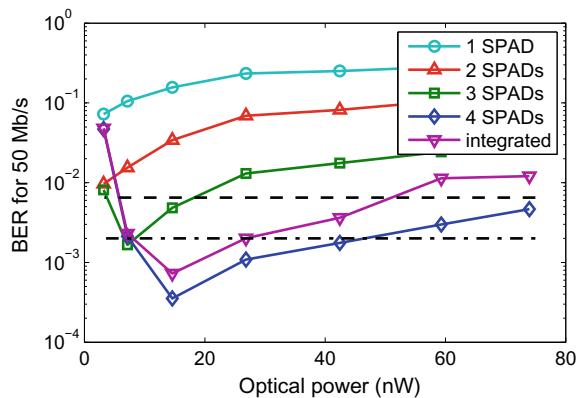


Fig. 6.220 Microphotograph of 4-channel SPAD optical receiver with on-chip digital processing

Fig. 6.221 Bit error rate for an RZ data rate of 50 Mb/s in dependence on average optical input power

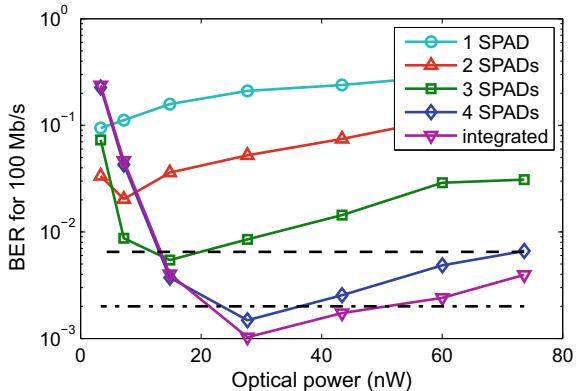


integrated DPC for $\text{BER} = 2 \times 10^{-3}$. At 150 and 200 Mb/s, the sensitivity for $\text{BER} = 6.5 \times 10^{-3}$ was -46.1 dBm (24.3 nW) and -43.7 dBm (42.8 nW), respectively [230].

Compared to [184] these sensitivities for 50 and 100 Mb/s are somewhat worse due to the shorter deadtime and the in turn higher APP. The smaller diameter of the 4-SPAD array did not compensate this effect fully. However, these sensitivities are still better than that of integrated linear-mode APD receivers [230].

In [231] the active quenching circuit in $0.35 \mu\text{m}$ CMOS was equipped with a variable deadtime and described in detail. The schematics of the quenching circuit is shown in Fig. 6.223a and the circuit diagram of the active quenching amplifier is depicted in Fig. 6.223b. The differential amplifier AMP contains a pull-down output stage being connected to the SPAD's cathode in positive feedback. This enables a

Fig. 6.222 Bit error rate for an RZ data rate of 100 Mb/s in dependence on average optical input power



fast comparator action for reference voltages V_{REF} from 3.2 to 0 V. The output of AMP can pull the output from V_{PLUS} (3.3 V) down to -3.3 V (see Fig. 6.223b). The maximum excess bias voltage is therefore 6.6 V. M3 acts as a cascode transistor and ensures that the voltages across M2, M7, the input of AMP and the Schmitt trigger ST1 stay in allowed ranges. Transistor M3 connects the cathode of the SPAD to the non-inverting input of AMP as long as the output of AMP (out_{AMP}) does not pull the SPAD's cathode to -3.3 V. When the output of AMP pulls the SPAD's cathode to -3.3 V, M3 sets the non-inverting input of AMP to GND plus its threshold voltage protecting the devices at this node. To obtain a fast active quenching, the open-drain output stage with MC5 and M15 as well as the protecting transistor M3 are prebiased. The current mirror M1-M2 defines and provides this prebiasing current.

The operation and transient response are shown in Fig. 6.224. At the beginning the cathode of the SPAD is charged to V_{PLUS} , the output of ST1 is low, C_{TQ} is charged, and AMP is active whereby V_{off} is low and V_{on} is high causing that the charging transistor M7 is off. When the absorption of a photon starts an avalanche at t_0 , the avalanche current causes a voltage drop across M2 (start of passive quenching at t_0) and when this becomes larger than $V_{PLUS}-V_{REF}$ at t_1 , AMP starts its comparator action, the passive quenching of the SPAD, however, continues for 0.56 ns (reaction time or delay of AMP) until t_2 . At t_2 the active quenching starts and the SPAD's cathode is discharged to -3.3 V (t_3). The time interval from t_2 to t_3 is 0.48 ns according to postlayout simulations [231], which is a bit longer than the 0.44 ns of [184] because of the somewhat larger capacitance of the SPAD. To keep the duration of the initial passive quenching phase short, V_{REF} should be set as close as possible below V_{PLUS} .

ST1 detects the active quenching, switches off M6 and C_{TQ} starts to discharge via M5. The discharging is detected by ST2, the output of AMP is switched off at t_4 , and M7 is switched on recharging the SPAD's cathode until ST1 switches (t_5). The dead time t_D is defined by $t_D = t_6 - t_0$. In the presented circuit the dead time was variable from 9.5 to 17 ns. From t_6 on, the next photon can be detected [231].

The quenching AMP's circuit is depicted in Fig. 6.223b. It uses two differential amplifier stages with R1, R2 and M8–M13 to obtain a low dynamic load at the

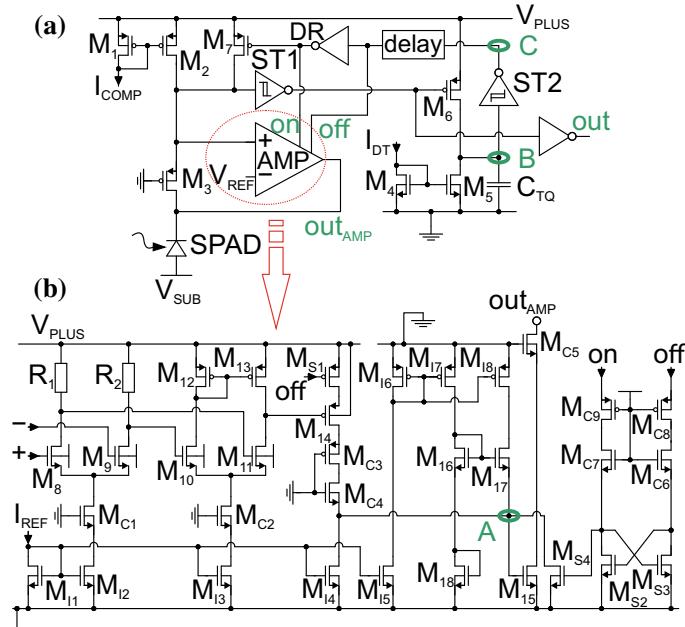


Fig. 6.223 Schematic of quenching circuit (a) and circuit diagram of active quenching amplifier (b) [231]

input and a high gain. The third stage (M14 and M14 with cascodes MC3 and MC4) represents a level shifter and drives the output transistor M15, which is cascoded by MC5 for 6.6 V voltage capability. The current-limited source follower M17 prebiases M15 for a fast switching. MS1, MS4 and the voltage protected latch MS2, MS3, MC6–MC9 enable the switch-off procedure.

The APP was measured in dependence on the reference voltage and the results are shown in Fig. 6.225. For $V_{EX} = 6.6\text{ V}$, the APP decreases from 14.7 to 4.8% when V_{REF} is raised from 0 to 3.2 V [231]. Please note that with $V_{REF} = 0\text{ V}$, the SPAD quenches passively until the cathode is discharged from 3.3 V down to 0 V. Therefore the time duration of passive quenching is much shorter and the avalanche charge is much smaller, when with $V_{REF} = 3.2\text{ V}$ the SPAD discharges only from 3.3 V down to 3.2 V until the avalanche event is being detected by AMP.

The PDP of the SPAD (see Fig. 2.44) for four different wavelengths measured with the active quenching circuit of Fig. 6.223 is shown in Fig. 6.226 in dependence on the excess bias voltage up to 6.6 V. The PDP is maximum (35.1%) for 635 nm light at $V_{EX} = 6.6$ V. However, because of the thick absorption layer the PDP is still 22% for 850 nm and $V_{EX} = 6.6$ V. A minimum APP of 0.9% at $V_{EX} = 3.3$ V and at a dead time of 17 ns was reported [231].

A fully integrated gating SPAD receiver containing only one SPAD was described in [232]. It was designed and fabricated in the same $0.35\text{ }\mu\text{m}$ CMOS technology as

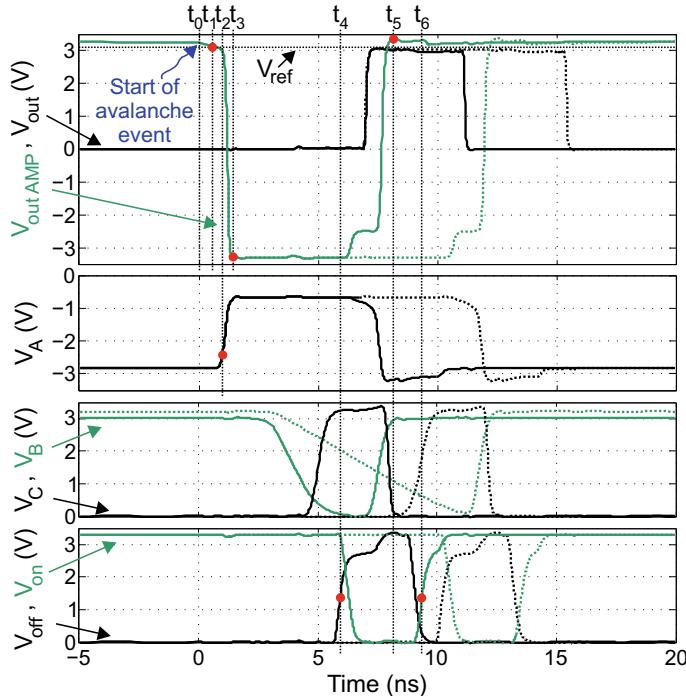
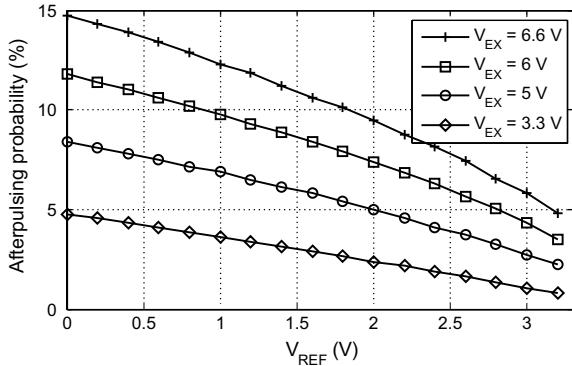


Fig. 6.224 Postlayout-simulated timing diagram of quenching circuit (solid lines: dead time 9.5 ns and dashed lines: dead time 13.5 ns) [231]

Fig. 6.225 Afterpulsing probability in dependence on the reference voltage [231]



the receivers [184, 230] and the active quenching circuit (AQC) [231] described above. The SPAD had a diameter of $50 \mu\text{m}$. This gater exploited also cascoding to increase the excess bias voltage from the usual circuit supply voltage of 3.3–6.6 V. Transistors N0, N1, P0 and P1 in Fig. 6.227 represent the cascaded switching stage, which gates the SPAD with a step height of 6.6 V. The SPAD's anode was supplied

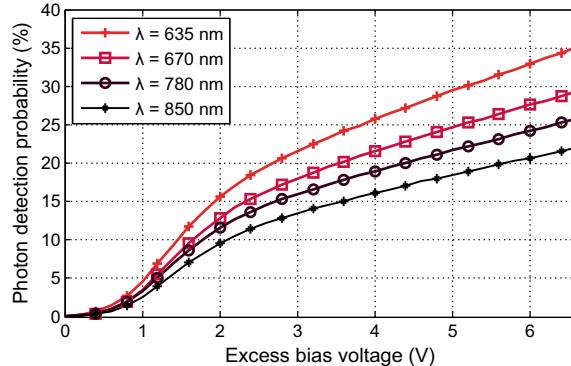


Fig. 6.226 Photon detection probability in dependence on the excess bias voltage [231]

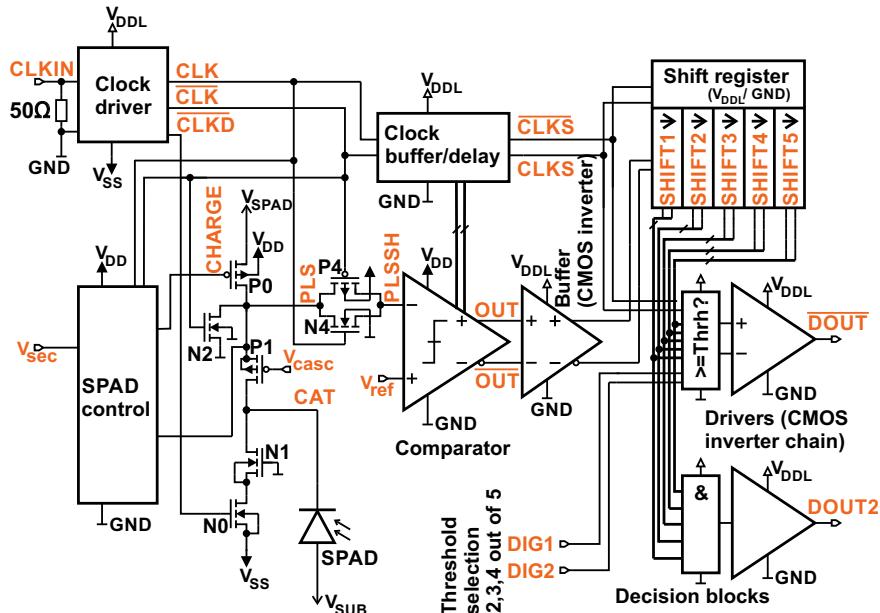


Fig. 6.227 Block diagram of gated SPAD receiver with only one photodiode and 5 sub-bits [232]

with $V_{\text{SUB}} < -30 \text{ V}$ ($V_{DD} = 3.5 \text{ V}$, $V_{DDL} = 3.3 \text{ V}$, $V_{SS} = -3.3 \text{ V}$). In the reset phase, $\text{CLK} = \text{CLKD} = 0 \text{ V}$, $\text{N}0$ conducts and pulls the cathode CAT of the SPAD to V_{SS} through the cascode transistor $\text{N}1$, which reduces the SPAD's reverse bias below its breakdown voltage. $\text{N}2$ switches node PLS to GND (0 V). $\text{P}1$ with the adjustable gate bias of about -1 V prohibits that PLS can reach V_{SS} and protects the devices from large voltage differences. During the reset phase the transmission gate $\text{N}4-\text{P}4$ is off [232].

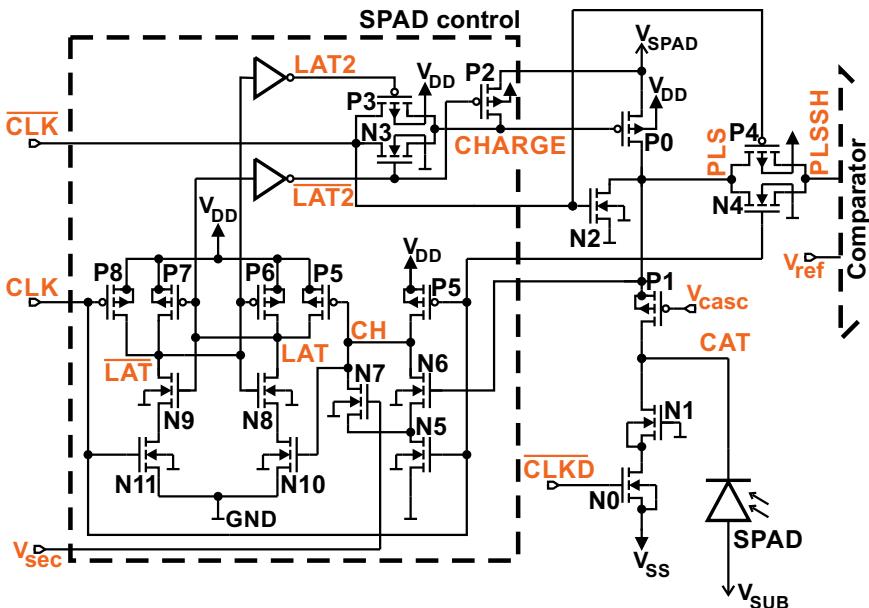


Fig. 6.228 Control unit for the SPAD [232]

$\text{CKL} = 3.3 \text{ V}$ and $\overline{\text{CLKD}} = -3.3 \text{ V}$ switches off $\text{N}0$ and $\text{N}2$, $\text{P}0$ charges the nodes PLS and CAT to V_{SPAD} and the reverse voltage of the SPAD exceeds its breakdown voltage making the SPAD ready for single-photon detection. When PLS approaches V_{SPAD} , the SPAD control (see Fig. 6.228) turns off $\text{P}0$. When a photon triggers an avalanche event (or a dark count or an afterpulse happen), the SPAD discharges node PLS to about 0 V (limited by $\text{P}1$) and CAT to the breakdown voltage level, i.e. the SPAD quenches itself. This voltage drop is typically about equal to the excess bias voltage. The transmission gate $\text{N}4-\text{P}4$ is on and during the following reset the state of PLS is stored on PLSSH dynamically, so that the avalanche event is detected by the comparator (see Fig. 6.229). The first latch (left in Fig. 6.229) is in a metastable state (i.e. ready for a decision) when the SPAD is charged and active [232].

When the first latch is in reset, the clocked inverters (see Fig. 6.229) are deactivated and the second latch on the right side of Fig. 6.229 holds the previous decision of the comparator. The pulses from the outputs of the second latch are through an inverter buffer fed into a 5-tab shift register (see Fig. 6.227). The decision blocks issue a logic high only when the number of counts in the shift register is equal to the threshold or exceeds it. For the output DOUT , a threshold of 2, 3, or 4 can be defined via the digital inputs DIG1 and DIG2 . If five counts are detected, DOUT2 issues a logic high [232].

The SPAD control block (Fig. 6.228) works like this. When the SPAD is in reset, $\text{CLK} = \overline{\text{CLKD}} = 0 \text{ V}$, $\text{LAT} = \text{CH} = V_{\text{DD}}$, $\text{LAT} = 0 \text{ V}$ and PLS is approximately 0 V. The transmission gate $\text{P}3-\text{N}3$ is switched on, transistor $\text{P}2$ is switched off, CHARGE

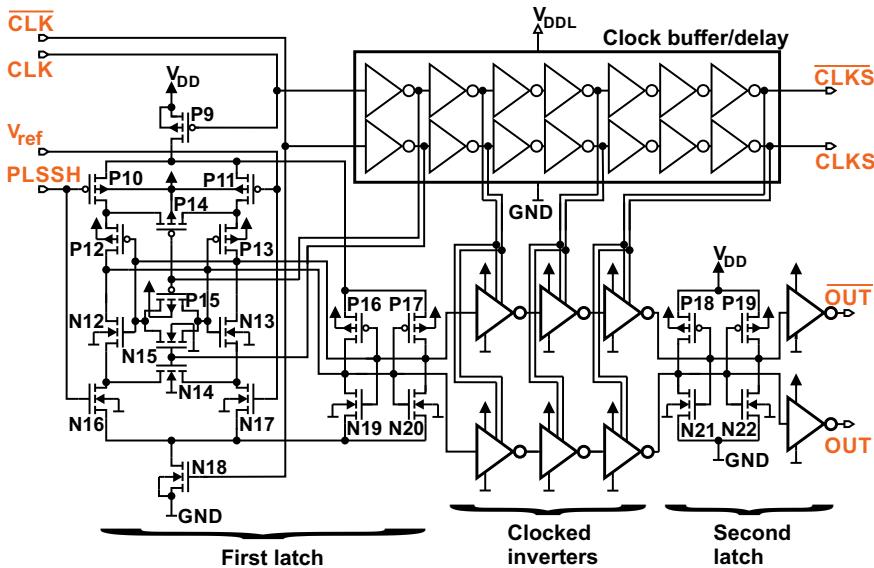


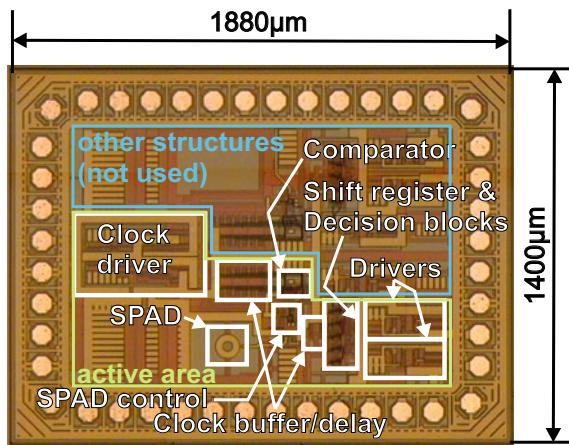
Fig. 6.229 Circuit of clocked comparator with second latch for storing its decision during reset and clock buffer [232]

$= \overline{CLK} = V_{DD} = 3.3\text{ V}$ and $P0$ is off. $N0$ and $N2$ are on. To prepare the SPAD for photon detection ($CLK = 3.3\text{ V}$, $\overline{CLK} = 0\text{ V}$, $CLKD = V_{SS} = -3.3\text{ V}$), initially $LAT = CH = V_{DD}$ and $LAT = 0\text{ V}$, transistors $N3$ and $P3$ are on, $P2$ is switched off, $CHARGE = \overline{CLK} = 0\text{ V}$, $P0$ charges the nodes CAT and PLS until PLS approaches V_{SPAD} . $N6$ detects this approach to V_{SPAD} and switches of $P0$ through the latch ($N8$ - $N11$, $P5$ - $P8$), two buffering inverters, $N3$ - $P3$ and $P2$. Then the SPAD's cathode is floating and the SPAD is ready for photon detection [232].

The comparator (see Fig. 6.229) can handle rail-to-rail input swing. In the reset phase ($CLK = 0\text{ V}$), the first latch consisting of inverters $N12$ - $P12$, $N13$ - $P13$ and $N19$ - $P16$, $N20$ - $P17$ is brought into the metastable state by the reset transistors $N14$, $N15$, $P14$, and $P15$, whereby the supplies are disconnected by transistors $N18$ and $P9$. In addition, the clocked inverters between the 1st and 2nd latch are switched off and the previous decision is kept in the second latch. CKL changing to V_{DDL} turns off the reset transistors and $P9$ and $N18$ connect the 1st latch to the supplies, node $PLSSH$ is compared with V_{ref} . When an avalanche was detected, the $PLSSH$ potential is lower than V_{ref} , the 1st latch switches accordingly and through the turned-on clocked inverters, the 2nd latch switches OUT to V_{DD} . When no avalanche event was detected, OUT is set to 0 V [232].

The photo of a test chip is visible in Fig. 6.230. The test chip had dimensions of 1.4 times 1.88 mm^2 whereby the gated receiver occupied about half of this area (including bondpads). The active area of the gating receiver (without bondpads) was 0.66 mm^2 [232]. A 635 nm light source with an extinction ratio larger than 100

Fig. 6.230 Microphotograph of gated SPAD receiver test chip [232]



was modulated with a NRZ pseudo random bit sequence having a length of $2^7 - 1$ (PRBS7). The PCB with the gated receiver was placed on a Peltier element to keep its temperature constant at 25 °C inside a dark box. The light was coupled into the SPAD with a single-mode fiber. The data rate was one fifth of the clock frequency. The BER was minimized by adjusting V_{SUB} and V_{ref} . At 100 MHz clock frequency the SPAD control and the comparator consumed 7.2 mW increasing to 13 mW at 250 MHz. The clock delay blocks, shift registers, and decision blocks consumed about 28 mW at 250 MHz according to simulations [232].

Measured BER results of the gating receiver are shown in Figs. 6.231 and 6.232. With a decision threshold for a logical “1” of 2 out of 5 sub-bits, the best sensitivity at 20 Mb/s was -64 dBm. Increasing the threshold to 5 out of 5 sub-bits, reduces the sensitivity to slightly better than -60 dBm, but reduces the BER to a minimum of below 10^{-6} . For 50 Mb/s, the sensitivity was -57 dBm for a decision threshold of 2. At 50 Mb/s the gated receiver achieved a 3 dB better sensitivity as the 4-SPAD receiver of [184] with NRZ.

Figure 6.233 gives an overview of sensitivities of receivers with APDs in the linear mode and of integrated CMOS SPAD receivers. The gap to the quantum limit is smaller for SPAD receivers than for linear-mode APD receivers. However, SPAD receivers were so far only operated up to 100 Mb/s and with somewhat worse sensitivity up to 200 Mb/s [230], whereas linear-mode APD receiver OEICs in the same 0.35 μ m CMOS technology reached data rates of 1 Gb/s and in BiCMOS even 2 Gb/s [172]. It also should be mentioned that the APD receivers were characterized for $\text{BER} = 10^{-9}$.

Until submission of this book into print, the smallest gap to the quantum limit of 12.7 dB was reached in NRZ with the gated receiver described above. It is, however, to be expected from the results of [184] that this gated receiver will achieve a better sensitivity and therefore will approach closer to the quantum limit in RZ.

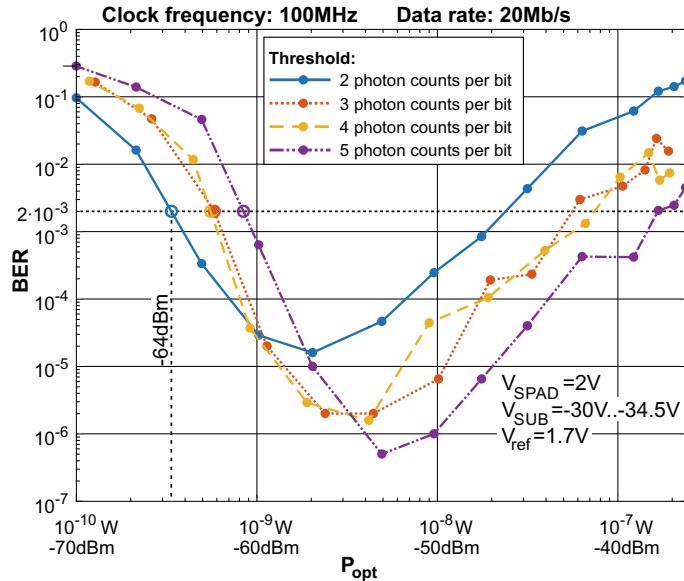


Fig. 6.231 BER results of gated SPAD receiver for different thresholds and NRZ data with PRBS7 in dependence on average optical input power at 20Mb/s [232]

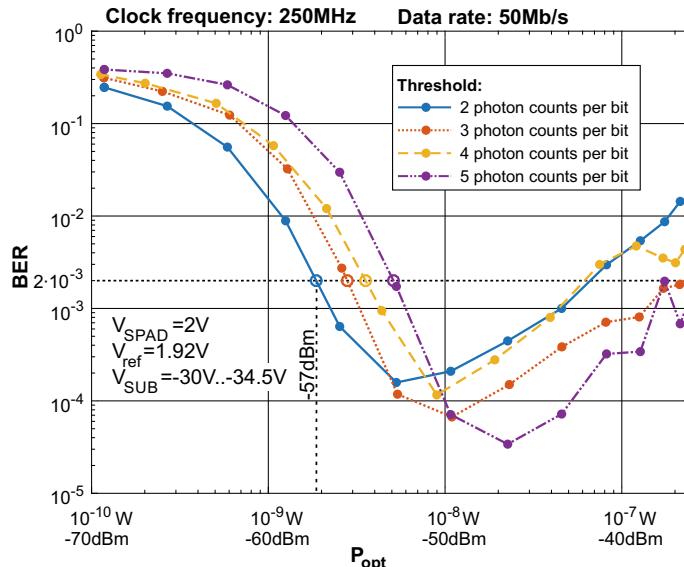
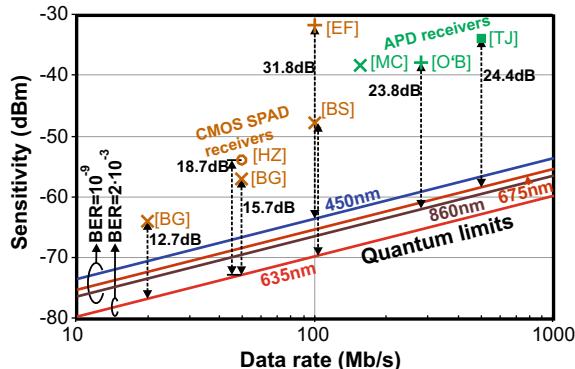


Fig. 6.232 BER results of gated SPAD receiver for different thresholds and NRZ data with PRBS7 in dependence on average optical input power at 50Mb/s [232]

Fig. 6.233 Comparison of distances to the quantum limit for linear-mode APD receivers and SPAD receivers [232], [MC] = [233], [O'B] = [228], [TJ] = [175], [EF] = [229], [BS] = [230], [HZ] = [184], [BG] = [232]



6.4.22 Comparison of Fiber Receivers

It is worthwhile to compare published results on silicon OEICs in Table 6.14. Polyimide bonding was applied to integrate GaAs PIN photodiodes with $0.8\text{ }\mu\text{m}$ CMOS transimpedance amplifier circuits resulting in data rates up to 800 Mb/s [190]. The same group achieved high sensitivities at data rates up to 1.3 Gb/s with GaAs and InGaAs photodiodes for 850 and 1550 nm , respectively, hybridized to $0.5\text{ }\mu\text{m}$ CMOS receiver circuits [191]. A hybrid receiver-transmitter circuit consisting of a $0.8\text{ }\mu\text{m}$ CMOS amplifier and of a flip-chip bonded GaAs-AlGaAs multi-quantum-well modulator, which also could be used as a PIN photodiode, has been reported to operate at 625 Mb/s [234]. For a hybrid OEIC with a GaAs photodetector and an amplifier in a $0.25\text{ }\mu\text{m}$ CMOS technology, finally a data rate of 1.25 Gb/s has been obtained [235]. A SiGe OEIC with a PIN photodiode and heterojunction bipolar transistors achieved a bandwidth of 460 MHz corresponding to a bit rate of about 690 Mb/s with a photodiode bias of 9 V [113]. A lateral PIN photodiode was used in an NMOS receiver OEIC, which operated at a bit rate of 300 Mb/s [116], when biased at $\text{VDD}=8\text{ V}$ and with a photodiode bias $V_{PD}=30\text{ V}$. In a redesigned version, the NMOS OEIC achieved a data rate of 1 Gb/s at a sensitivity of -9.3 dBm [117]. Furthermore, a receiver OEIC on high-resistivity bulk silicon exhibited a sensitivity of -31.9 dBm at 622 Mb/s with a wavelength of 850 nm , with $\text{VDD}=3.5\text{ V}$, and $V_{PIN}=30\text{ V}$ [118]. With a lateral PIN photodiode in a $3.0\text{ }\mu\text{m}$ thick N-type (100)-oriented SOI layer and an NMOS transimpedance amplifier with the circuit topology of Fig. 6.98 a sensitivity of -15.3 dBm at 622 Mb/s and at a BER of 10^{-9} was obtained for $\text{VDD}=3\text{ V}$ and $V_{PIN}=3\text{ V}$ with $\lambda=850\text{ nm}$ [118]. With higher supply voltages of $\text{VDD}=5\text{ V}$ and $V_{PIN}=5\text{ V}$ a sensitivity of -12.0 dBm at a data rate of 1.5 Gb/s was found. A sensitivity of -12.2 dBm finally was reported with $\text{VDD}=5\text{ V}$ and $V_{PIN}=20\text{ V}$ for a data rate of 2.0 Gb/s . These impressive results are due to the optimized SOI layer thickness allowing the suppression of the slow drift in the depth between the N^+ - and P^+ -fingers, which is present in the lateral PIN photodiode on high-resistivity bulk silicon.

Table 6.14 Comparison of silicon receiver OEICs with small photodiode areas

Process (μm)	VDD (V)	λ (nm)	BR_{PR} ($\frac{\text{Mb}}{\text{s}}$)	SPR (dBm)	V_{PD} (V)	BR_{PD} or f_3 dB	R_{PD} ($\frac{\text{A}}{\text{W}}$)	η_{PD} (%)
0.8 CMOS-GaAs [190]	5	850	155	-18.2	2.5	-	0.33	47
0.8 CMOS-GaAs [190]	5	850	311	-16.1	2.5	-	0.33	47
0.8 CMOS-GaAs [190]	5	850	622	-9.2	2.5	-	0.33	47
0.8 CMOS-GaAs [190]	5	850	800	-8.5	2.5	-	0.33	47
0.5 CMOS-GaAs [191]	3.3	850	622	-30.1	1.7	-	0.42	60
0.5 CMOS-GaAs [191]	3.3	850	1000	-27.4	1.7	-	0.42	60
0.5 CMOS-GaAs [191]	3.3	850	1300	-18.5	1.7	-	0.42	60
0.5 CMOS-InGaAs [191]	3.3	1550	622	-31.4	1.7	-	0.8	64
0.5 CMOS-InGaAs [191]	3.3	1550	1000	-28.0	1.7	-	0.8	64
0.5 CMOS-InGaAs [191]	3.3	1550	1300	-22.8	1.7	-	0.8	64
0.8 CMOS-MQW [234]	5	850	625		2.5	-	0.5	75
0.25 CMOS-MQW [235]	3.3	850	1250		-	-	-	-
Bipolar SiGe [113]	6	850	690		9	460 MHz	0.3*	43*
1.0 NMOS [116]	8	870	300		30	500 Mb/s	0.52*	74*
1.0 NMOS [117]	1.8	850	1000	-9.3	30	1.0 Gb/s	0.54*	80*
1.0 NMOS [118]	3.5	850	622	-31.9	30	234 MHz	0.57*	83*
1.0 NMOS [118]	3.5	850	1000	-23.2	30	234 MHz	0.57*	83*
1.0 NMOS [118]	3.5	850	622	-23.2	10	124 MHz		
1.0 NMOS SOI [118]	3	850	622	-15.3	3		0.20*	29*
1.0 NMOS SOI [118]	5	850	1500	-12.0	5	900 MHz		
1.0 NMOS SOI [118]	5	850	2000	-12.2	20	2.8 GHz		
0.13 CMOS SOI [124]	3.2	850	2000	-16.6	24.0	5 GHz	0.07	10
0.13 CMOS SOI [124]	3.2	850	3125	-15.4	24.0	5 GHz	0.07	10
0.13 CMOS SOI [124]	3.2	850	5000	-10.9	24.0	5 GHz	0.07	10
1.5 Bipolar [236]	5	850	150		4.2	150 Mb/s	0.21	30
Bipolar [86]	5	780	50		3.0	300 MHz	0.35	56
Bipolar [87]	5	830	150		3.0	280 MHz	0.5*	75*
0.6 BiCMOS [119]	3.3	850	531	-13.1	2.5	700 MHz	0.07	10
0.6 BiCMOS [120]	3.3	670	622	-16.6	2.5	700 MHz	0.16	29
0.8 BiCMOS [121]	5	638	531		3.3	531 Mb/s	0.49*	95*
0.6 BiCMOS [122]	5	670	1250	-22.7	5	1.25 Gb/s	0.40	74
0.6 BiCMOS [122]	5	670	622	-24.5	17	1.5 Gb/s	0.40	74
0.6 BiCMOS [122]	5	670	1000	-24.3	17	1.5 Gb/s	0.40	74
0.6 BiCMOS [122]	5	670	1250	-24.1	17	1.5 Gb/s	0.40	74
0.6 BiCMOS [122]	5	670	1500	-22.1	17	1.5 Gb/s	0.40	74
0.6 BiCMOS [197]	5	670	1250	-14.1	VUC	1.5 Gb/s	0.40	74
0.6 BiCMOS [197]	5	670	1500	-13.1	VUC	1.5 Gb/s	0.40	74
0.6 BiCMOS [200]	5	670	1250	-22.5	VUC	1.5 Gb/s	0.40	74

(continued)

Table 6.14 (continued)

Process (μm)	VDD (V)	λ (nm)	BR_{PR} ($\frac{\text{Mb}}{\text{s}}$)	SPR (dBm)	V_{PD} (V)	BR_{PD} or $f_{3\text{ dB}}$	R_{PD} ($\frac{\text{A}}{\text{W}}$)	η_{PD} (%)
0.35 CMOS [134]	3.3	850	1000	-6.3	10	1.0 Gb/s	0.04	5.9
0.35 CMOS [134]	3.3	850	1000	-8.6	10	1.0 Gb/s	0.04	5.9
0.25 CMOS [133]	3.3	860	700	-18.7	1.7	0.7 Gb/s	0.1	15
0.25 CMOS SOI [136]	2.0	850	1500		1.5	1.0 GHz	0.4	59
1.0 CMOS [101]	5	638	622	-14	3	1.7 GHz	0.25	49
1.0 CMOS [101]	3.3	638	622		1.8	1.4 GHz	0.48*	94*
1.0 CMOS [144]	5	638	1000	-15.4	3	1.7 GHz	0.25	49

*With ARC

BR = bit rate

PR = photoreceiver

PD = photodiode

The same research group finally switched over to IBM's 130 nm CMOS process. With this process on a 2 μm thick SOI material, allowing for a quantum efficiency of about 10% for 850 nm, a photodetector speed of 5 GHz with a reverse bias of -20 V [124] was achieved. With a 1 GHz design, a receiver sensitivity of -19 dBm was reported. With a faster 3 GHz circuit, sensitivities of -16.6, -15.4, and -10.9 dBm for data rates of 2, 3.125, and 5 Gb/s, respectively, were obtained for a BER of 10^{-9} [124].

With a bipolar OEIC [236] using the BEST-process of AT&T with 1.5 μm design rules [237], a data rate of 150 Mb/s was achieved. An N⁺/P-substrate photodiode limited the speed to this data rate. In [86, 87], vertical PIN photodiodes have been integrated with bipolar transistor technology. The optical receivers described in these two articles demonstrated a data rate of 50 Mb/s [86] and a frequency response of 147 MHz [87] at a supply voltage of 5 V although the PIN photodiodes showed bandwidths of ≈ 300 MHz at a bias of 3 V.

The thin P⁺/N-collector/N⁺-buried collector PIN photodiode in a 0.6 μm BiC-MOS process was used together with a MOS amplifier in [119, 120] with a rather low responsivity of the photodiode. A double photodiode in a standard 0.8 μm BiC-MOS technology enabled a bit rate of the OEIC with a bipolar amplifier in excess of 531 Mb/s [105, 121]. A 0.6 μm BiCMOS OEIC with a photodiode similar to that described in [86] achieved a sensitivity of -22.7 dBm at 1.25 Gb/s for $\text{BER} = 10^{-9}$ with $\lambda = 670$ nm at a single 5 V supply [122]. With a second (external) supply of 17 V for the photodiode, sensitivities of -24.5, -24.3, and -24.1 dBm were obtained at bit rates of 622 Mb/s, 1.0 Gb/s, and 1.25 Gb/s, respectively. The sensitivity for 1.5 Gb/s operation finally was -22.7 dBm. With a photodiode bias of 16.3 V internally generated on the chip from $\text{VDD} = 5$ V with a voltage-up-converter (VUC), i.e. without an external supply voltage for the photodiode, sensitivities of -14.1 dBm at 1.25 Gb/s and of -13.1 dBm at 1.5 Gb/s were achieved [197]. With an improved approach for the VUC, a sensitivity of -22.5 dBm was obtained at 1.25 Gb/s finally [200].

A very low responsivity of 0.04 A/W has been reported for the P^+/N -well photodiode of a 1 Gb/s OEIC in a $0.35 \mu\text{m}$ CMOS technology [134]. The most sophisticated approach with a spatially-modulated-light detector (SML detector) [132] in standard CMOS 0.6 and $0.25 \mu\text{m}$ [133] technology enabled data rates of 250 and 700 Mb/s , with sensitivities of -18 and -18.7 dBm , respectively, at 860 nm and a BER of 10^{-9} . The SML detector, however, suffers from a low quantum efficiency of 15% [132], because half of the detector area is covered by metal and because carriers photogenerated below the N -well/ P -substrate space-charge region do not contribute. This low detector quantum efficiency finally limits the sensitivity of SML receivers. The power consumption of the $0.25 \mu\text{m}$ receiver with 2.5 mW per channel [133], however, was remarkably low. An avalanche photodiode in a SOI CMOS technology enabled an OEIC with a bandwidth of 1 GHz corresponding to a bit rate of about 1.5 Gb/s at a supply voltage of only 2 V [136].

Summarizing, a low responsivity has been present in order to achieve a high data rate in the investigations [119, 120, 134, 236], or a high voltage for the photodiode was needed [113, 116, 117, 122, 124], or a high additional process complexity has been needed for the integration of fast and highly efficient photodiodes as in [86, 87]. Compared to the sophisticated detectors in [133, 134, 136], the vertically integrated PIN photodiode developed in the CMOS DVD project and described in [101] achieved a higher speed and a much higher quantum efficiency with and without an antireflection coating. The CMOS-integrated vertical PIN photodiode, although slower than the lateral SOI PIN photodiodes, showed the largest speed-responsivity product of all integrated silicon photodiodes reported so far whereby standard or near-standard processes have been used.

It can be concluded that with CMOS receiver OEICs comparable or even better data rates can be obtained than with the bipolar OEICs described in [86, 87]. In contrast to the integration of PIN photodiodes in bipolar circuits, the integration of vertical PIN photodiodes in CMOS circuits requires little additional process complexity. The vertical PIN photodiodes combine a high data rate and a high quantum efficiency at a low reverse bias with a single power supply voltage for the OEIC. Low cost PIN-CMOS receiver OEICs for optical data transmission and for optical interconnects on boards and between boards via optical backplanes seem feasible.

Table 6.15 compares newer small-area photodiode receiver OEICs. The two first SPAD receivers were introduced using large arrays of SPADs to achieve a high dynamic range [229, 238]. The newest ones [184, 230, 232] use a high fill factor and only 4 SPADs or even 1 SPAD, the cascoding technique for a high PDP and achieve the best sensitivities. These newest SPAD receivers eliminate electronic noise, but suffer still from dark counts and afterpulsing.

Table 6.15 Comparison of newer silicon receiver OEICs

Process (μm)	VDD (V)	λ (nm)	BR_{PR} ($\frac{\text{Mb}}{\text{s}}$)	SPR (dBm)
0.13 CMOS [229]	1.5	450	100	-31.7
0.18 CMOS [238]	1.8	860	20	-
0.35 CMOS [184]	6.6	635	50	-55.7
0.35 CMOS [184]	6.6	635	100	-51.6
0.35 CMOS [230]	6.6	635	150	-46.2
0.35 CMOS [230]	6.6	635	200	-43.8
0.35 CMOS [232]	6.6	635	20	-64
0.35 CMOS [232]	6.6	635	50	-57
0.35 CMOS [168]	3.3	800	2400	-22
0.18 CMOS [239]	1.8	850	3000	-19
0.13 CMOS [240]	1.2	850	4500	-3.8
0.18 CMOS [182]	1.8	850	5000	-3
0.13 CMOS [183]	1.2	850	8500	-3.2
0.18 CMOS [241]	1.8	850	10000	-6
65 nm CMOS [169]	1.2	670	3125	-3.8
65 nm CMOS [170]	1.0	670	4000	-3.2

BR = bit rate

PR = photoreceiver

PD = photodiode

In a 0.35 μm CMOS technology a sensitivity of -22 dBm at 2.4 Gb/s with 800 nm and an avalanche photodiode area of $8,284 \mu\text{m}^2$ was reported [168]. Reference [239] achieved a sensitivity of -19 dBm with an integrated p-n photodiode having an area of $2500 \mu\text{m}^2$ thanks to an accurately adjusted equalizer. Compared to these results, the sensitivities of -3.8 dBm at 3.125 Gb/s [169] and -3.2 dBm at 4 Gb/s [170] of a 65 nm CMOS POF receiver with a photodiode area of $62,500 \mu\text{m}^2$ and with 670 nm are rather moderate. The low supply voltage of deep-sub-micrometer and nanometer CMOS ICs, the large penetration depth of the used light wavelengths and carrier diffusion limit the sensitivity of nanometer CMOS receiver OEICs (see also [245]).

Table 6.16 lists BiCMOS receivers with pin photodiodes. The pin-photodiode (Fig. 2.63) integrated in 0.5 μm BiCMOS enabled a considerable improvement of data rate and sensitivity. All photodiodes of the receivers in this table had an area of $2070 \mu\text{m}^2$, with the exception of the photodiode of [205], which had a diameter of 300 μm . It should be mentioned that the receiver of [244], which achieved a data rate of even 11 Gb/s, suffered from the transistors' transit frequency of only about 25 GHz. Receivers with avalanche photodiodes are listed in Table 6.10.

Table 6.16 Comparison of newer silicon receiver OEICs with PIN photodiodes and small photo-diode areas

Process (μm)	VDD (V)	λ (nm)	BR_{PR} ($\frac{\text{Mb}}{\text{s}}$)	SPR (dBm)	V_{PD} (V)	BR_{PD} or $f_{3\text{ dB}}$ (MHz)	R_{PD} ($\frac{\text{A}}{\text{W}}$)	η_{PD} (%)
0.5 BiCMOS [111]	5	660	1000	-29.4	-	615	0.36	66
0.5 BiCMOS [111]	5	660	1250	-27.0	-	615	0.36	66
0.5 BiCMOS [242]	5	660	1000	-28.4	5	-	0.34	63
0.5 BiCMOS [110]	5	660	622	-30.4	5	-	0.36	66
0.5 BiCMOS [110]	5	660	622	-30.7	12	-	0.36	66
0.5 BiCMOS [108]	5	660	622	-31.6	5	-	0.36	66
0.5 BiCMOS [108]	5	660	1000	-29.2	5	-	0.36	66
0.5 BiCMOS [108]	5	660	1000	-30.4	12	-	0.36	66
0.5 BiCMOS* [205]	5	660	2500	-20.1	12	-	0.36	66
0.5 BiCMOS [243]	5	660	3000	-24.3	11	-	0.36	66
0.5 BiCMOS [243]	5	850	3000	-21.9	11	-	-	-
0.5 BiCMOS [126]	5	660	5000	-20.5	11	-	-	-
0.5 BiCMOS [127]	5	660	6000	-21.0	17	-	-	-
0.5 BiCMOS [127]	5	850	6000	-18.2	17	-	-	-
0.5 BiCMOS [244]	5	850	10000	-10.2	17	2200	-	-

*Photodiode diameter 300 μm

BR = bit rate

PR = photoreceiver

PD = photodiode

6.4.23 Special Circuits

In [246] a new opto-electrical phase-locked-loop (OE-PLL) was introduced. This OE-PLL is based on the CMOS photonic mixer device (CMOS PMD) described in [26]. The PMD combines the detection of the light and the mixing of this optical signal with an electrical signal in itself [26, 27]. The CMOS PMD, therefore, can be used as a phase detector in a phase-locked loop (PLL). An OE-PLL consequently can be manufactured with the complete readout electronics for the retiming and reshaping in low-cost CMOS technology. The OE-PLL, for instance, can be applied in optical fiber and wireless communication.

Figure 6.234 shows the block diagram of the OE-PLL. The CMOS PMD receives light pulses in a return-to-zero (RZ) mode from an optical fiber or via free space. This optical input signal is mixed in the PMD with the differential electrical output signal of the voltage-controlled oscillator (VCO). The static frequency f_{center} of the VCO is located close to the known value of the clock rate f_{bit} of the incoming binary signal carrying information. The difference signal $P D_{\text{out}}$ is used to adjust the frequency and the phase of the VCO. Therefore, the difference signal $P D_{\text{out}}$ is low-pass filtered

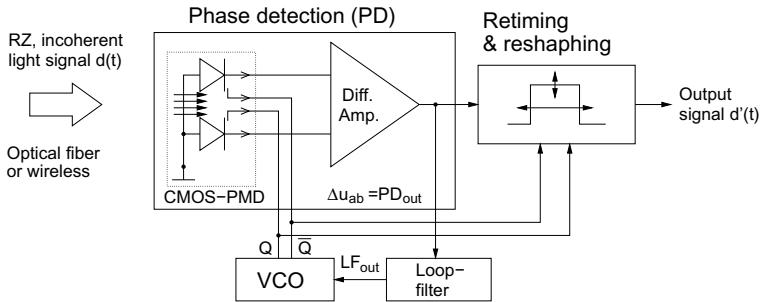
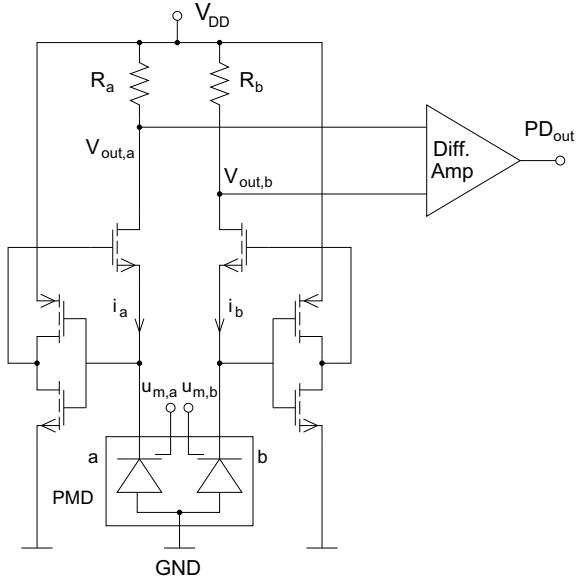


Fig. 6.234 Block diagram of an optoelectronic phase-locked loop [246]

Fig. 6.235 PMD readout circuit with differential amplifier as a phase detector [246]



allowing LF_{out} to be used as the input voltage of the VCO as it is done in conventional electrical PLLs. In order to allow for a safe locking of the PLL, a synchronization sequence precedes the data stream. A locking time of 450 ns was reported in [246] for a jump of the data rate from 60 to 65 Mb/s.

The PMD readout circuit is depicted in Fig. 6.235. The charges separated in the PMD to its outputs a and b according to the modulation inputs u_{am} and u_{bm} lead to the photocurrents i_a and i_b . The low-impedance readout circuit consists of an inverter and a control transistor. The PMD output voltages are amplified by the inverters and fed back via the source follower control transistors. Due to this feedback circuit the cathode voltage of the PMD is adjusted to the inverter threshold of about 2.5 V independent of the drain voltage of the control transistor. The photocurrents are converted to voltages across the resistors R_a and R_b .

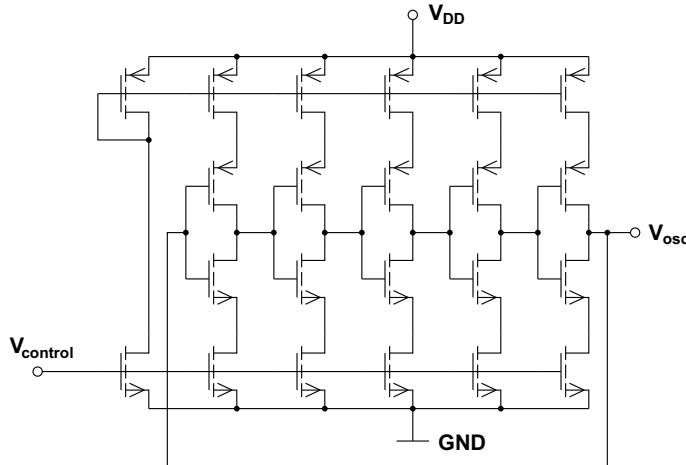


Fig. 6.236 Five-stage current-starved voltage-controlled oscillator [246]

The difference between the two voltages $v_{\text{out},a}$ and $v_{\text{out},b}$ is a measure for the phase-shift between the light signal and the signal at the input gates u_{am} and u_{bm} of the PMD. This difference is amplified with a gain of 250, whereby the output of the amplifier referred to 2.5 V for identical input voltages [246]. It should be mentioned that a high CMRR of the amplifier is essential for a good suppression of background light. Also an output driver is necessary in the amplifier to obtain a low output impedance being necessary to drive the loop filter and the following VCO.

A common oscillator topology in monolithic PLLs is the ring oscillator, in which a cascade of M gain stages with a total phase shift of 180° is placed in a feedback loop. This phase requirement can be achieved by implementing an odd number of CMOS inverters. The loop oscillates with a period $T = 2MT_d$, where T_d is the delay of each stage with a fan-out of one. To vary the frequency of oscillation, the delay of each stage has to change. This can be realized with the current-starved VCO shown in Fig. 6.236. An NMOS and a PMOS current source is added to each inverter to limit and to control the current available to the inverters. The current for the PMOS sources has to be the same as for the NMOS sources. This is achieved by mirroring the NMOS source current from the control NMOS device at the input to the PMOS sources. This current I_D determines the oscillation frequency f_{osc} :

$$f_{\text{osc}} = \frac{I_D}{MC_{\text{tot}}VDD}. \quad (6.109)$$

M is the number of inverter stages, C_{tot} is the inverter output capacitance. For the use in a PLL, a threshold switch is placed to the VCO output. The complementary signal is obtained by an inverter stage. The tuning range of the VCO was approximately 15–95 MHz in the input-voltage range 1.5–3.5 V [246].

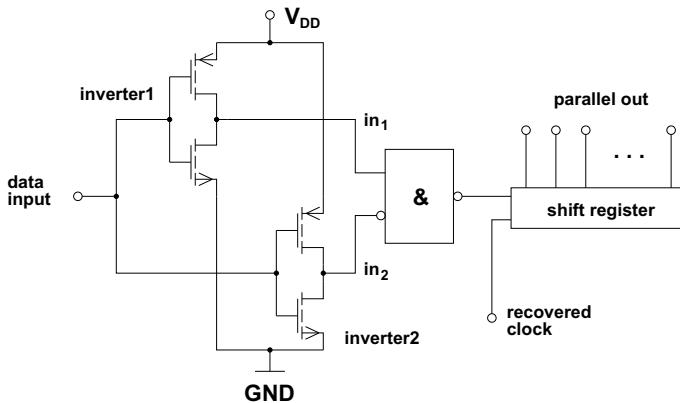


Fig. 6.237 Data recovery circuit [246]

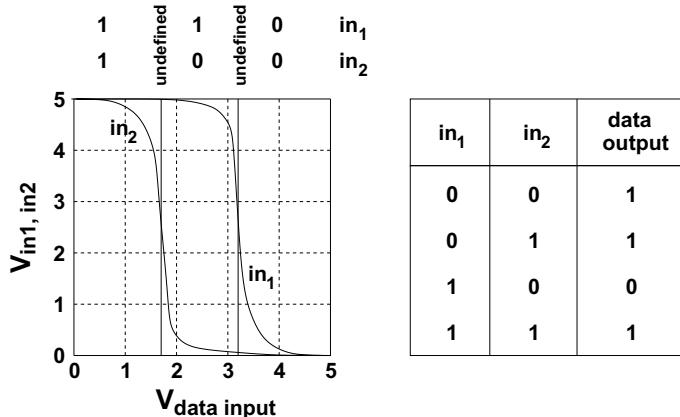


Fig. 6.238 DC characteristics and truth table of the NAND gate with the inverted input in_2 in the data recovery circuit [246]

The output signal of the amplifier PD_{out} goes from 2.5 V via 5 V back to 2.5 V and then to 0 V within one period of the RZ signal for a transmitted “1” [246]. For a logical “0”, PD_{out} stays at 2.5 V, however. Therefore, a circuit is needed, which delivers a high output level for an input signal close to 0 V and close to 5 V, whereas its output level has to be low for an input signal around 2.5 V. Such a circuit is illustrated in Fig. 6.237. The inverters 1 and 2 have different switching points at 1.7 V and 3.2 V, respectively (Fig. 6.238). The two inverters, therefore, hand over three different logical states to the NAND gate with one inverted input.

The truth table of this NAND gate is included in Fig. 6.238. The whole circuit causes a 5 V data output for data input voltages from 0 to 1.7 V and from 3.2 to 5 V. For data input voltages between 1.7 and 3.2 V the data output level becomes low (0 V) [246]. Therefore, each data bit “1” (light on) which reaches the optical input of

the PLL causes a high level at the data output of the recovery circuit. For a “0” (light off), the data output becomes low. This characteristics fulfills exactly the function of a data recovery circuit [246].

6.5 Summary

OEICs span over a huge variety of circuit topologies and applications. Digital optical CMOS receivers based on sense-amplifier flip-flops, which require small die areas and are therefore very interesting for the application in massively parallel optical interconnects, were described. An innovative SML detector was combined with a sense amplifier. OEICs with current mirror amplifiers and current comparators were shown to be appropriate for the wafer-level test of digital CMOS and BiCMOS circuits with considerably increased frequencies.

Many analog photoreceiver circuits were included in this chapter. For instance, a bipolar circuit for optical flame detection with a very high transimpedance was described. The pixel circuits of an amorphous-silicon-CMOS imager with a dynamical range of 100 dB and of adaptive cameras-on-a-chip as well as complex smart-pixel circuits were described. Active pixel sensors up to 390 Mpixels were included. Several approaches towards optical distance measuring chips and 3D sensors were discussed. SPAD sensors enable distance measurements up to 6 km.

The most important results for the development of OEICs for optical storage systems are: a PIN CMOS OEIC requiring a very small chip area for DVD applications with a bandwidth of 147 MHz was realized in full custom design. This bandwidth is the same as that of former BiCMOS OEICs. Innovative bandwidths enhancement techniques finally lead to single-stage TIAs having a performance of 600 MHz with a transimpedance of $200\text{ k}\Omega$.

The CMOS-integrated PIN photodiodes can handle much higher data rates ($>1\text{ Gb/s}$) than are necessary for DVD applications. Therefore, a $1.0\text{ }\mu\text{m}$ PIN CMOS OEIC for fiber receiver applications with a non-return-to-zero (NRZ) data rate of 1.0 Gb/s was demonstrated. This data rate was limited by the amplifier in $1.0\text{ }\mu\text{m}$ CMOS technology. OEICs with data rates in excess of 1 Gb/s , therefore, are possible with submicrometer CMOS processes. $0.6\text{ }\mu\text{m}$ BiCMOS OEICs with PIN photodiodes achieved a data rate of 1.5 Gb/s . A $0.5\text{ }\mu\text{m}$ BiCMOS OEIC with PIN photodiode and equalizer achieved a data rate of 10 Gb/s . Integrated voltage-up-converters increase the bandwidth of photodiodes strongly. Avalanche photodiodes in the linear mode used in $0.35\text{ }\mu\text{m}$ BiCMOS improved the sensitivity over that of pin-photodiode OEICs considerably and enabled larger photodiode areas. Possible applications for PIN CMOS, PIN BiCMOS, APD BiCMOS OEICs seem to be Local Area Networks (LANs), such as the Gigabit Ethernet or the Fiber Channel with 850 nm light. APD receiver OEICs enable low-cost optical wireless communication over distances of up to 20 m at 1 Gb/s and up to 15 m at 2 Gb/s . First SPAD-based optical receivers eliminated electronic noise and reduced the gap to the quantum limit to 12.7 dB .

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Chapter 7

Circuits for Electronic-Photonic Integration



In this chapter newest research on three-dimensional integration is described. Three promising methods for 3D integration of using copper micro pillars, interwafer connects, and through-silicon vias are introduced. The application of these 3D-integration techniques in the integration of photonic chips on top of electronic chips is described subsequently. Four application examples, a multi-node optical switch, a transceiver, a sensor for optical tomography, and a sensor for 3D microimaging are explained in detail from system architecture down to the transistor level.

7.1 3D-Integration Technologies

7.1.1 Copper Pillar Connection

In the IRIS European project the electrical connections between electronic IC (EIC) and photonic IC (PIC) were realized with copper micro pillars (see Fig. 7.1). The electronics wafers (CMOS wafers) containing EICs were post-processed with micro-pillars using a semi-additive electroplating process of a Ti/Ni/Cu metallic stack through a thick resist mask [1, 2]. An eutectic solder (e.g. SnAg) is deposited on top of the micro-pillars. Under bump metallization (UBM) pads with a Cu/Ni/Au stack are formed on the photonic wafer. Flip-chip assembly followed. A pitch of $50\text{ }\mu\text{m}$ for interconnect arrays was achieved easily.

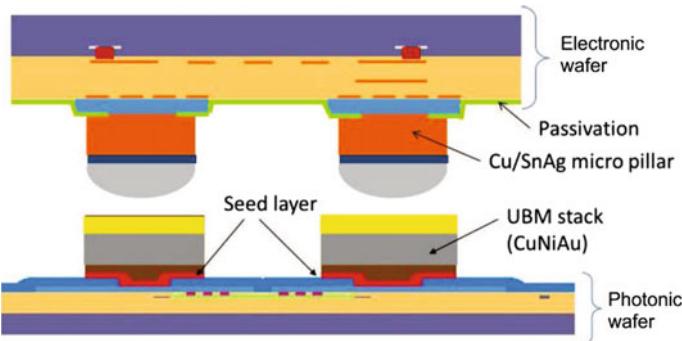


Fig. 7.1 Cross section of photonic wafer and electronic wafer with UBM stack and micro pillars [1]

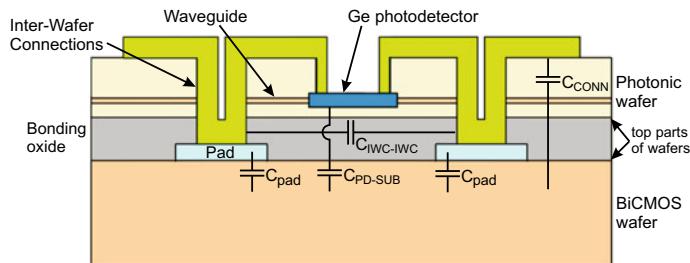


Fig. 7.2 Cross section of 3D-integrated OEIC using IWC connections [6]

7.1.2 Through Oxide Vias

Through Oxide Via (TOV) is another technique to connect two wafers vertically through a (thin) oxide layer after oxide-to-oxide wafer bonding and removing the backside silicon completely. The TOV technique was developed at IBM (face-to-back bonding) [3] and MIT (face-to-face bonding) [4]. Even wafer-scale 3D integration of InP-based photodiode arrays on silicon readout circuitry was done by wafer bonding and TOV [5]. An InGaAs absorption layer on the InP substrate allowed infrared sensitivity. A 150-mm-diameter InP wafer was directly bonded to a SOI wafer and connected to the silicon circuits by TOVs. The array had a size of 32×32 with $6\text{-}\mu\text{m}$ pixels. This was the smallest pixel size being half as large as what could be achieved with flip-chip bonding.

The TOV technique fits very well to electronic-photonic integration. In [6] a TOV technique was applied, which was called inter-wafer connection (IWC). A lateral Ge PIN waveguide photodiode in a photonic SOI layer was connected via IWCs to a TIA in the silicon BiCMOS chip below. Figure 7.2 shows the cross section of this wafer-scale 3D-integration technique.

The pad capacitance on the BiCMOS chip, the capacitance between the photodiode and the silicon substrate C_{PD-SUB} , and the connection structures' capacitance

C_{CONN} together was about 15 fF. The capacitance between two neighboring IWCs was about 0.3 fF [6].

7.1.3 Through Silicon Vias

Through-silicon vias (TSVs) seem to be the heart of the oldest 3D integration method [7]. TSVs were applied for many applications as e.g. [8–10]. In [10], a TSV and the whole connection path of Ge photodiode and TIA had a parasitic capacitance of 7 fF.

A wafer-to-wafer 3D-integration technology was exploited in [11]. An image sensor was fabricated with the 3D 2-tier Terrazos's FaStack process being based on 130 nm CMOS. With this process two standard CMOS wafers are face-to-face bonded using copper to copper bonds, which were called direct bond interfaces (DBIs). These copper areas had a diameter of 0.6 μm . Through-silicon-vias (TSVs) were implemented in the top wafer (the photodiode wafer). These TSVs with a diameter of about 1.2 μm were formed by 6 μm high tungsten pillars, which were connected to metal 1 of the top wafer. The pitch of the DBIs was 4 μm . After wafer-to-wafer bonding the top wafer was thinned to about 4.2 μm exposing the TSVs and allowing metallization and fabrication of bondpads. The backside-illuminated SPAD introduced and similar to the one described for frontside illumination in [12] was present in the top wafer together with MOS transistors for passive quenching and for buffering. The bottom wafer contained massive signal processing electronics (please see Sect. 7.4).

7.2 Optical Switch

Advanced optical switches are needed for 5G applications and efficient data centers [13]. Optical switches were realized using Mach-Zehnder interferometers on SOI [14] and MEMS technology [15]. The optical switch developed in the European project IRIS consists of electronic IC (EIC) and photonic IC (PIC), which contains grating coupler, waveguides, micro-ring (MR) resonators, and Ge photodiodes (see Fig. 7.3). The 3D-integration technique depicted in Fig. 7.1 is applied to connect the EIC to the PIC.

Ring resonators are a highly interesting solution for optical switches [1]. They can be tuned by changing the temperature using heating resistors being integrated together with the ring resonators in a SOI layer. For each ring resonator a heating resistor and a heater driver circuit are necessary. When using an analog heater driver circuit, electrical power is also dissipated in the electronics chip. For integrated optical switches with many nodes, however, the analog heater control is not acceptable due to too strong overall heating and detuning of the ring resonators [1]. Therefore, a digital pulse width modulation (PWM) heater control has to be used. The driver is operated only in two states: completely on with maximum current but almost zero voltage drop across the output switching transistor and completely off with the supply

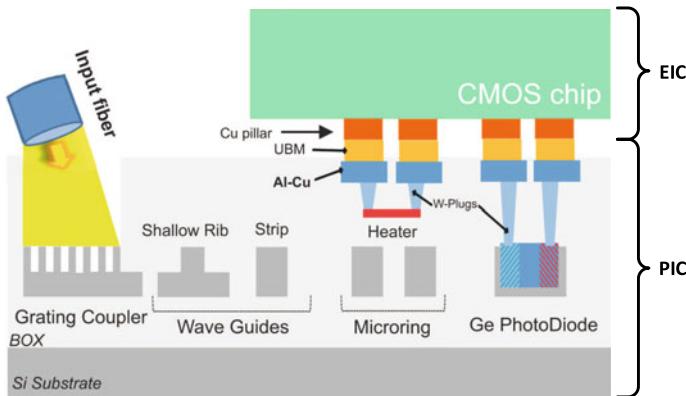
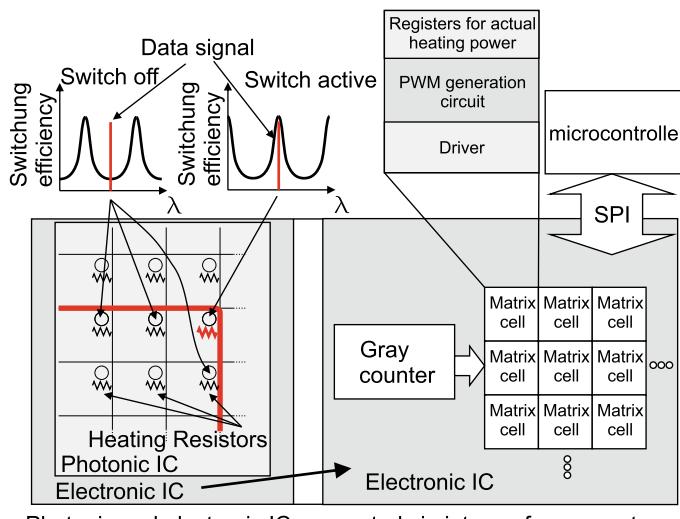


Fig. 7.3 Schematic cross section of optical switch



Photonic and electronic IC connected via inter wafer connects

Fig. 7.4 Block diagram of an optical switch with digital heater control [16]

voltage across the output transistor but with zero current. The switching between the two states is being done rather in the ps range than in the ns range in deep-sub- μm CMOS. By changing the PWM duty ratio, the heater power and the resonance frequency of the ring resonator can be varied. In the IRIS project, this PWM approach was applied as described in the following.

Digital Heater Control

The electronic and the photonic chip are 3D-integrated on each other (see Fig. 7.4) [16]. The electronic chip contains the main blocks Gray counter and the matrix with the control cells having the same pitch as the ring resonators in the photonic layer.

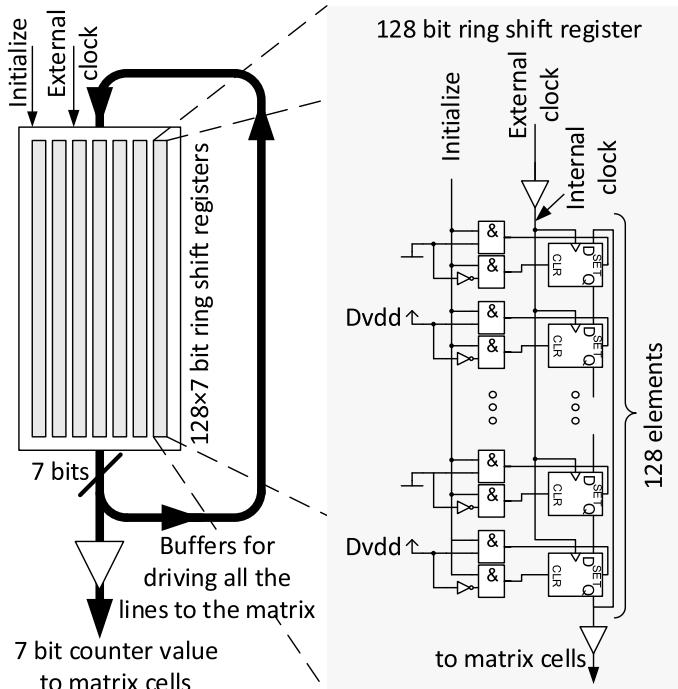


Fig. 7.5 Circuit diagram of Gray counter [16]

The heating power of each cell can be set via a serial peripheral interface (SPI) with a microcontroller.

The Gray counter (see Fig. 7.5) was chosen because in this counter architecture only one bit differs in two successive states, which leads to a high energy efficiency and a compact design, since considering glitches when more bits change between successive states is not necessary. Only one Gray counter is on the chip and a 7-bit bus distributes the counter values to all matrix cells. The power consumption of the Gray counter in 0.16 μm CMOS is about 83 mW for a 1 GHz clock.

The circuit of each matrix control cell is shown in Fig. 7.6. The heater resistor of the ring resonator switch element is connected via a copper pillar to the drain of the heater driver NMOS transistor. The 7-bit word representing the desired heater power can be read via a shift register into the data register. A 7-bit asynchronous digital compare circuit sets a flip-flop when the counter reaches the value stored in the data register. In such a way the PWM signal for driving the heater resistor is generated. The electrical power consumption of a control cell is 210 μW for a 1 GHz clock.

The photo of a test chip fabricated in the CMOS part of a 0.16 μm BCD technology containing a small matrix with 9 control cells is shown in Fig. 7.7 [16]. Because a photonic chip was not available yet, the heater resistor was integrated in each cell on the electronic test chip. The chip area of each matrix cell was $79 \times 105 \mu\text{m}^2$.

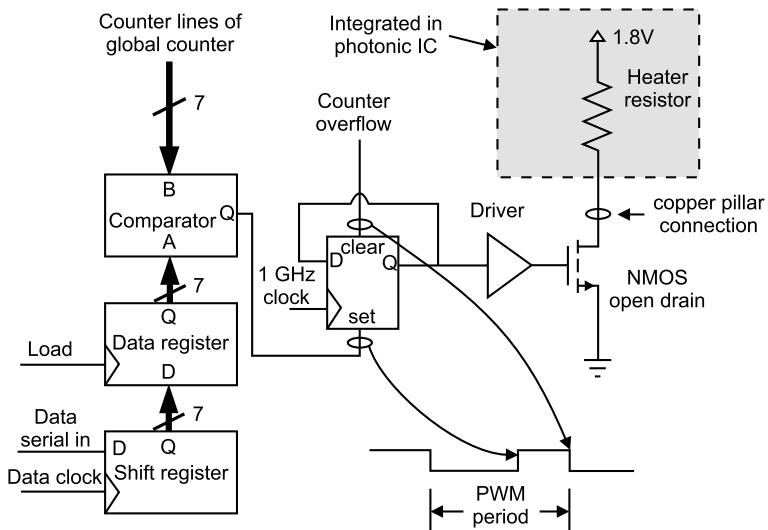


Fig. 7.6 Circuit diagram of a digital heater control matrix cell [16]

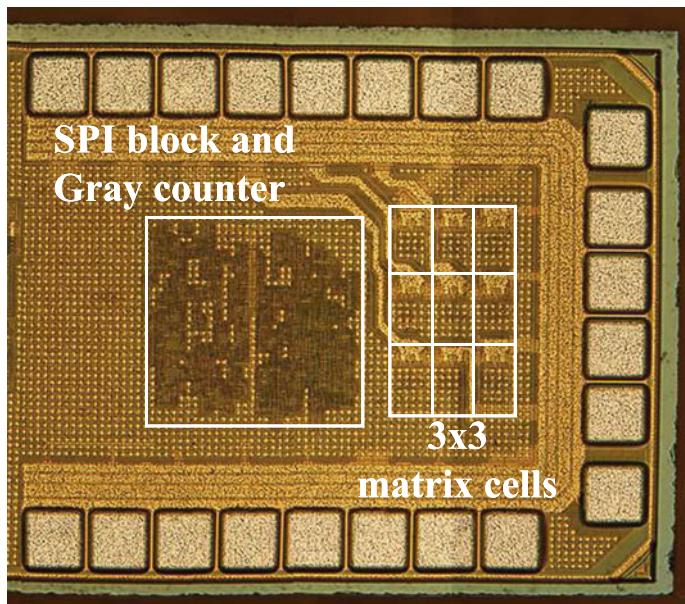
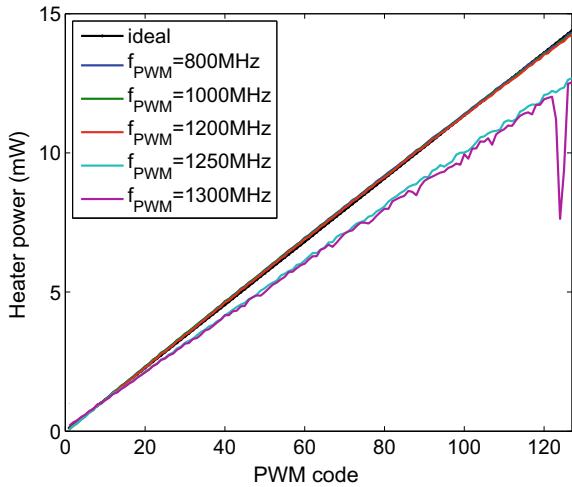


Fig. 7.7 Chipphoto of test chip for digital heater control approach

Fig. 7.8 Heater power obtained with digital heater control approach for all PWM codes and for different clock frequencies [16]



For the micro-ring resonators as in [17] a minimum PWM frequency of 7.58 MHz was necessary in order to keep the thermal ripple caused by the PWM control small enough. The 7-bit resolution for tuning the ring resonators then requires a minimum clock frequency of 970 MHz. The control circuit therefore was designed to work with a clock above 1 GHz, which comes to the limit of the technology used. The measured results shown in Fig. 7.8 verify the feasibility of the approach up to a clock frequency of 1.2 GHz. At 1.25 GHz the digital comparator is not fast enough anymore to detect when the counter reaches the value stored in the data register and the output stays off leading to lower mean heater power. At even higher clock frequency, the counter will also stop working properly [16].

Compared to [16] the heater resistor changed during the project from 230 to 110Ω . Figure 7.9 compares the power dissipation for the analog approach (constant voltage approach) to the digital approach for this lower resistor value making the same assumptions for the on- and off-switches as in [16]. It can be seen that the digital approach saves a lot of electrical power and the heat generated by the electronics is much smaller than the power needed in the heater resistors.

Analog-Digital Heater Control

An even better heater control approach than the digital one described above was introduced. The analog-digital heater control approach (see Fig. 7.10) uses analog input to a sample and hold circuit and generates in each matrix cell a pulse-width modulated (digital) signal to drive the heater resistor [18].

The circuit diagram of an analog-to-PWM converter cell is shown in Fig. 7.11 [18]. Realized in the CMOS part of a $0.16\mu\text{m}$ BCD technology the area of this circuit without the pad for connection to the heater resistor was about $2800\mu\text{m}^2$. The OTA is rather acting as a comparator. Two tapered CMOS inverters are implemented to ensure fast switching of the NMOS transistor M1, which is a high-frequency transistor

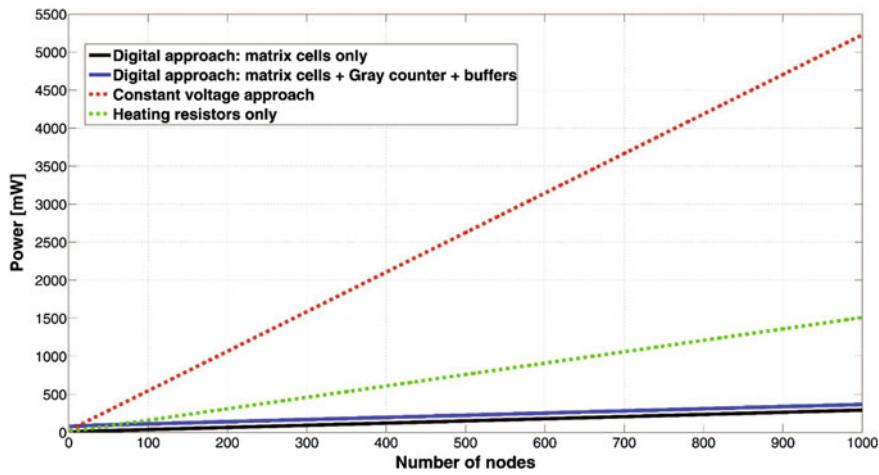


Fig. 7.9 Power dissipation in dependence on the number of photonic switch nodes for the digital heater control approach and for the constant voltage heater control approach in comparison to the power dissipated by the heating resistors. Only non-active microrings tuned for compensating process variations are considered [16]

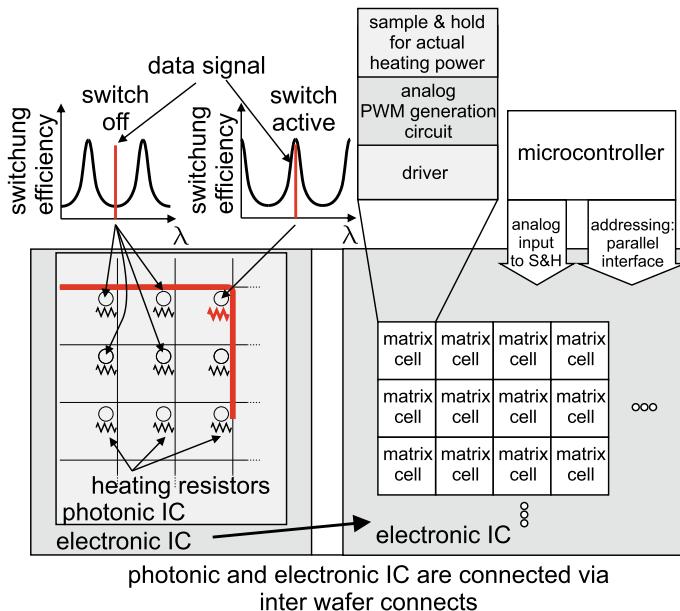


Fig. 7.10 Block diagram of an optical switch with analog-digital heater control [18]

Fig. 7.11 Circuit diagram of analog-digital heater control cell [18]

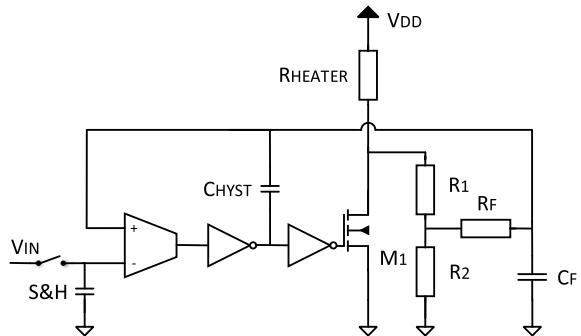
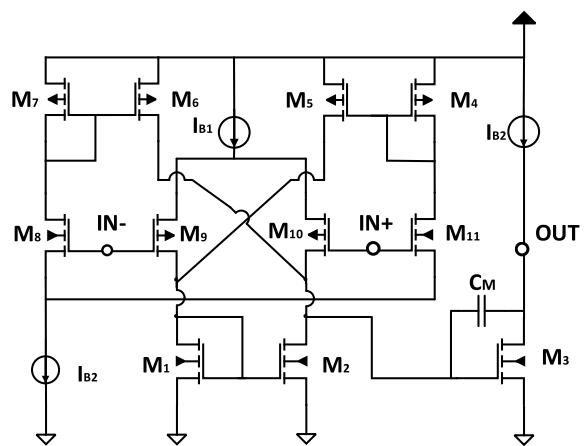


Fig. 7.12 Circuit diagram of rail-to-rail OTA



consisting of 20 fingers and a total gate width of $184 \mu\text{m}$. The voltage divider ($R_1 = 2.5 \text{ k}\Omega$ and $R_2 = 21.5 \text{ k}\Omega$) sets the input voltage range to $0\text{--}1.6 \text{ V}$ (for $V_{DD} = 1.8 \text{ V}$). It ensures that M_1 can be switched off also for a worst-case input offset voltage of the OTA. R_1 , R_2 , RF , CF , and $Chyst$ determine the time constant, which should be matched to the thermal time constant of the heating resistor to minimize the thermal ripple of the ring resonators.

The OTA (see Fig. 7.12) has rail-to-rail capability [19]. The frequency of this control circuit cell was at a maximum at 78 MHz in the middle of the input voltage range. This value is much higher than the PWM frequency of the digital heater control approach leading to a smaller temperature ripple of the ring resonators than with the digital approach. An additional advantage is that the area and power consumption of the Gray code counter can be saved.

This first analog-digital heater control circuit, however, had the disadvantage that the heater power increased for decreasing input voltage. This could be dangerous when the refresh of the sample and holds should fail and the hold capacitors discharge in a matrix with a large number of cells leading to strong heating of the complete chip. Therefore, the improved analog-digital heater control cell (see Fig. 7.13) was developed [20].

Fig. 7.13 Circuit diagram of improved analog-digital heater control cell

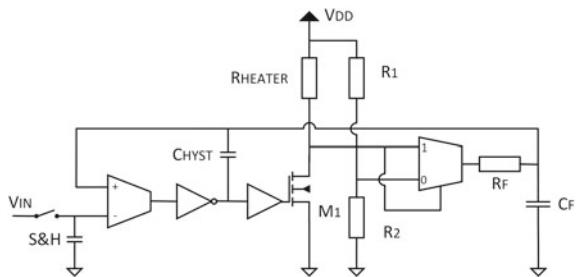
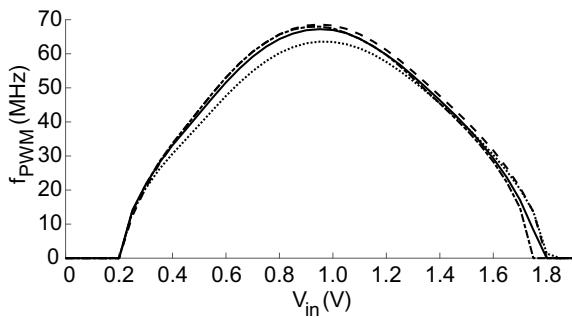


Fig. 7.14 PWM frequency of four selected MR heater control circuits versus input voltage



The logic function was inverted compared to the old analog-digital heater control cell and an offset of 0.2 V was added by implementing the voltage divider formed by R1 and R2. The analog multiplexer connects RF either to the drain of M1 (when it is at VDD) or to the voltage divider at 0.2 V (when the drain of M1 is almost at ground). This analog multiplexer contains two transmission gates and an inverter. The width of the driver NMOS transistor M1 was increased to $420 \mu\text{m}$ to be able to drive also heater resistors of arrayed-waveguide gratings (AWGs) and interleavers, which are also integrated in the PIC.

Measured results of the PWM frequency are depicted in Fig. 7.14. The start of the increasing curves at 0.2 V guarantees that the heaters can be turned off completely also for worst-case OTA offset voltages [20]. The PWM frequency is not constant but depends on the input voltage V_{IN} , whereby its maximum is at around 70 MHz in the middle of the input voltage and heater power range. This value is much higher than the constant PWM frequency of 7.58 MHz [16] of the purely digital heater control approach described above and therefore leads to less temperature ripple of the ring resonators.

The mean heater power increases linearly from 0.2 V on (see Fig. 7.15) [20]. The maximum heater power is obtained for $V_{IN} = 1.8 \text{ V}$ instead of 0 V as in [18]. This is advantageous to avoid that leakage currents discharge the hold capacitor and switch all heaters on the PIC to maximum heater power in case the refresh would fail. The slight mismatch of the curves being visible in Figs. 7.14 and 7.15 can be solved by calibration, which has to be done because of tolerances of the photonic components anyway.

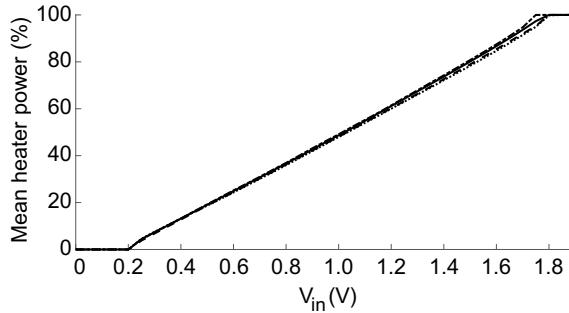


Fig. 7.15 Mean heater power of four selected MR heater control circuits versus input voltage

Figure 7.16 shows the microphotograph of the full-matrix (16×48) EIC, which uses the new analog-digital approach for heater control. The fabricated EIC has dimensions of 5.7×3.7 mm. The fabricated PIC is shown in Fig. 7.17. The PIC has dimensions of 8.4×7.8 mm allowing the mounting of the EIC on top of it and to connect the EIC through bondpads on the PIC. Figure 7.18 shows the photo of the 3D-integrated transponder aggregator (TPA) with a fiber ribbon mounted to the PIC part.

The electronic-photonic integrated transponder aggregator (TPA) was characterized optically. Figure 7.19 shows the obtained results for use of two switch nodes aligned in ADD configuration [20]. A channel is added to direction 4 for two scenarios (switch A or B active) of switching an odd or even wavelength. The temperature of the TPA was kept at 38.8°C during the measurements. The interleavers (INTs) and arrayed-waveguide gratings (AWGs) were aligned with dedicated heaters. Figure 7.19 shows the transmission spectra at different locations in the TPA. An optical power of 6 dBm was inserted into the input fiber from a tunable laser and the output signal was detected by an InGaAs photodiode. On the left side of Fig. 7.19 the signal paths are shown. The signal visible in the top panel represents the measured transmission from the input to the output. Two transmission peaks corresponding to the selection of an odd or even channel by switch A or B are visible. The total insertion loss was -22 dBm , the 1-dB channel bandwidth was 80 GHz , and the channel isolation was better than -35 dB [20]. The spectra measured with the integrated Ge monitor photodiodes at the interleaver output, at the AWG output, and at the AWG input are presented in the second, third, and fourth panel of Fig. 7.19, respectively. These signals are normalized to the signal of the first Ge photodiode behind the input grating coupler. The panel at the bottom of this figure depicts the transmission of the interleaver verifying the splitting of the signal at the input into even and odd wavelengths. The device loss is almost 0 dB on the channels and the channel isolation is better than 25 dB . The free spectral range was 19 nm and the total on-chip device loss was -15 dB resulting in a total insertion loss of -22 dB inclusive the input and output grating coupler losses [20]. The results of the optical characterization confirm the full functionality of the new analog-digital (hybrid) heater control approach.

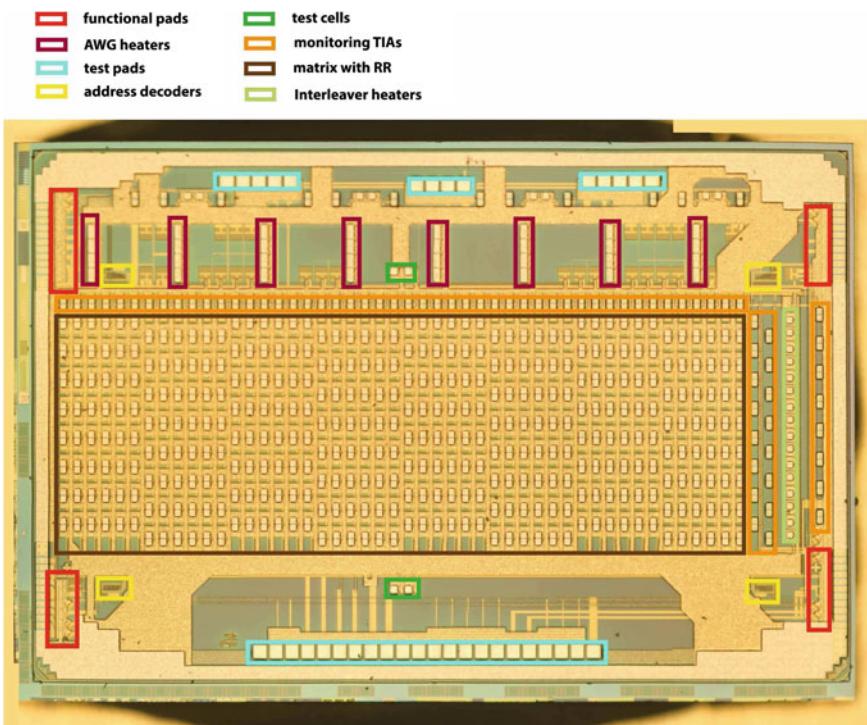
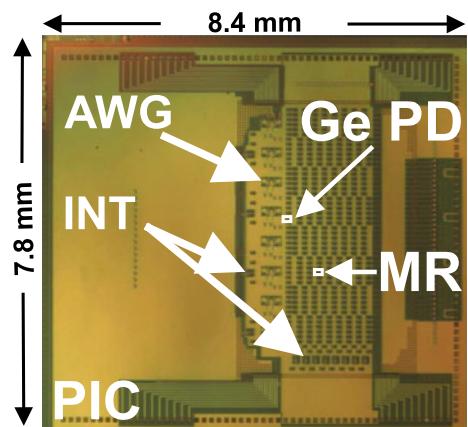


Fig. 7.16 Microphotograph of full-matrix EIC

Fig. 7.17 Microphotograph of full-matrix PIC



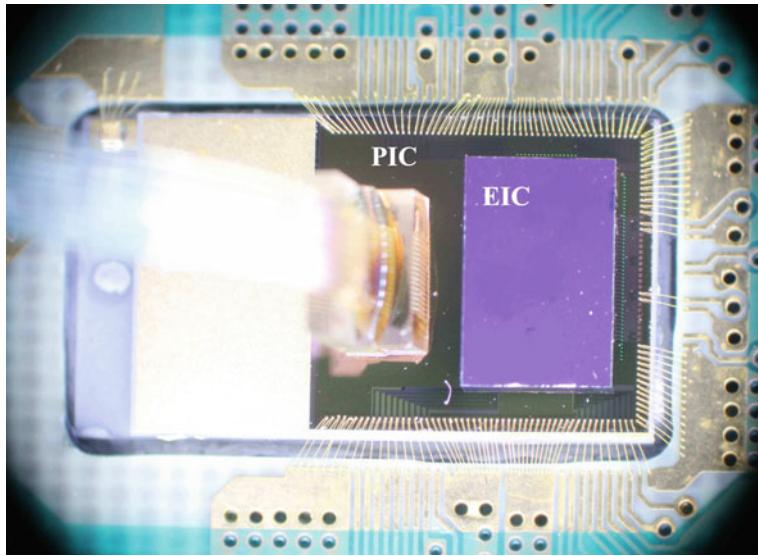


Fig. 7.18 Photo of electronic-photonic integrated TPA wire-bonded to PCB. The EIC is turned top-side down

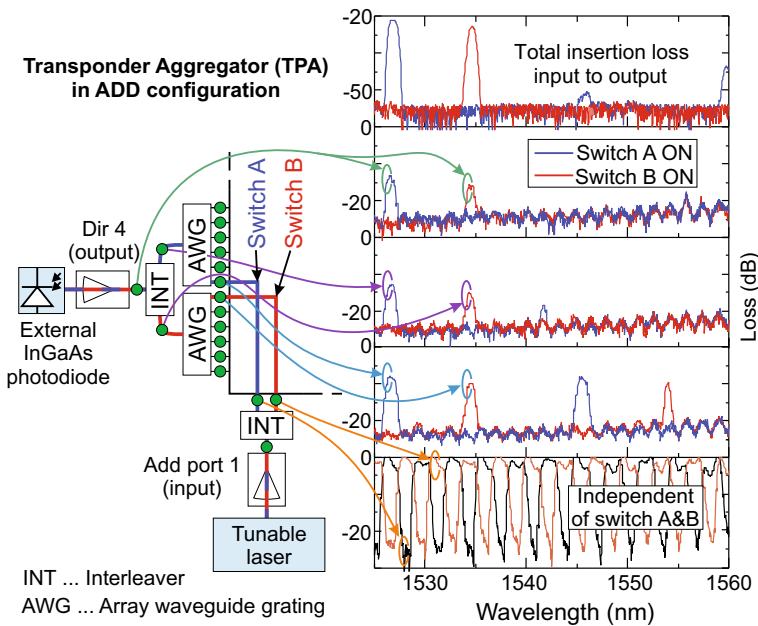
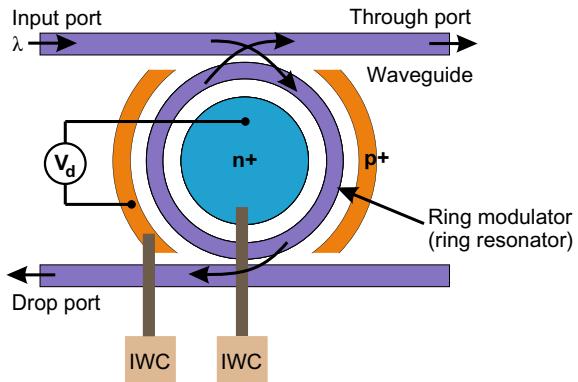


Fig. 7.19 Measured properties of electronic-photonic integrated TPA

Fig. 7.20 Sketch of micro-ring resonator coupled to two waveguides with connections to IWCs



The analog-digital (hybrid) heater control circuits in the 768-nodes switch matrix inside the EIC consumed 220 mW compared to 1.15 W of the heaters' power. For comparison, the power consumption of 768 purely analog (constant voltage) heater control circuits was estimated to be 4 W. Compared to this power dissipation, the hybrid heater control circuits need only 5.5 % of the power [20].

7.3 Optical Transceiver

An electronic-photonic integrated optical transceiver consisting of pulse amplitude modulation (PAM-4)/binary transmitter and PAM-4/binary receiver was introduced in [6]. For the transmitter branch, a micro-ring modulator in the photonic SOI layer was implemented for binary and PAM-4 modulation. For the receiver branch, a Ge lateral waveguide PIN photodiode in the photonic layer was used (see Fig. 7.2).

Figure 7.20 shows the schematical sketch of the micro-ring resonator [21]. The central n+ region forms the cathode, the ring waveguide the intrinsic region, and the outer p+ regions the anode of a pin diode. The driving voltage V_D controls the density of free carriers and thereby the refractive index of the ring, which determines the resonance wavelength of the ring modulator. For forward bias, the electro-optic modulation is via carrier injection, and for reverse bias, the modulation is via depletion. The modulation frequency can be higher for the depletion based modulation, since the carrier injection based modulation is limited by the carrier lifetime. Therefore, the free-carrier depletion based modulation was exploited for the ring modulator shown in Fig. 7.20. The capacitance of the ring modulator's pn junction was 20 fF at 0 V and 9 fF at -3 V [6].

The optical transmission of a ring resonator is usually nonlinear [21, 22], i.e. equidistant driving voltages do not result in equidistant optical output amplitudes for PAM-4 modulation. The driver circuit has to compensate the nonlinearity of the micro-ring resonator modulator. In the following, a driver circuit will be described,

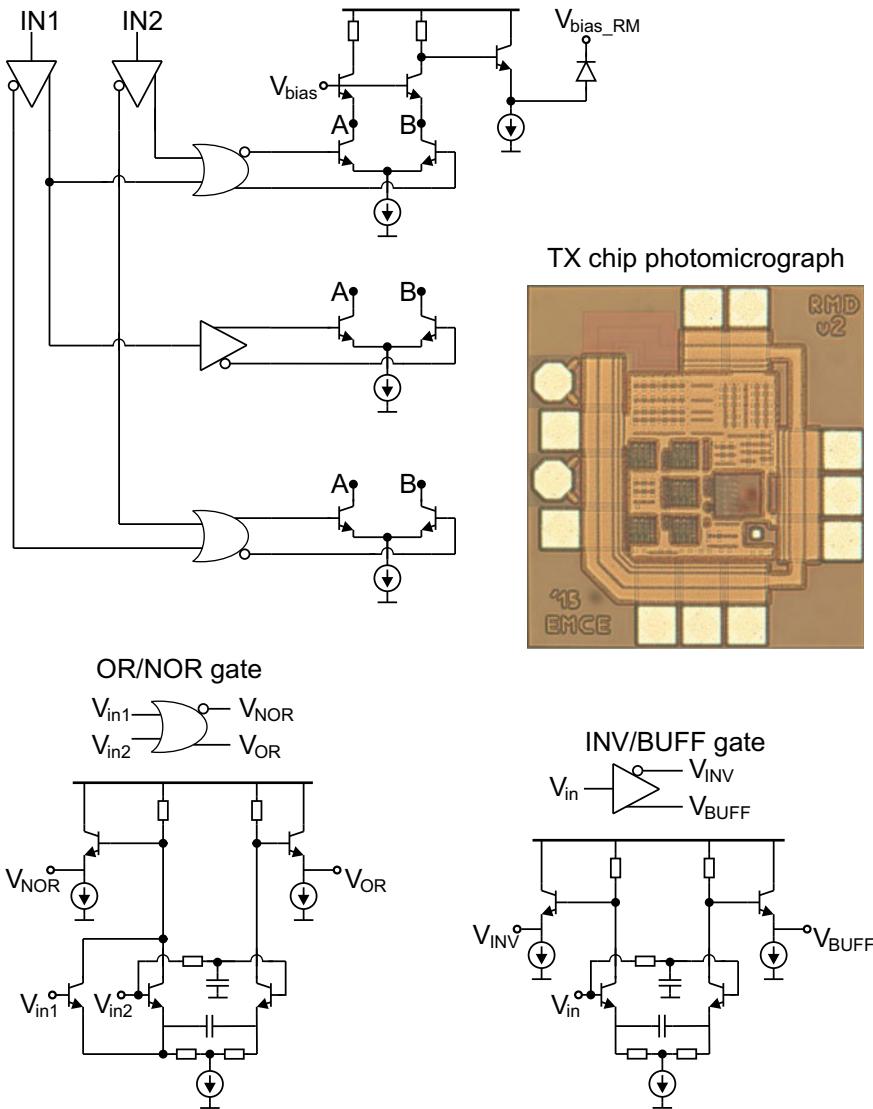
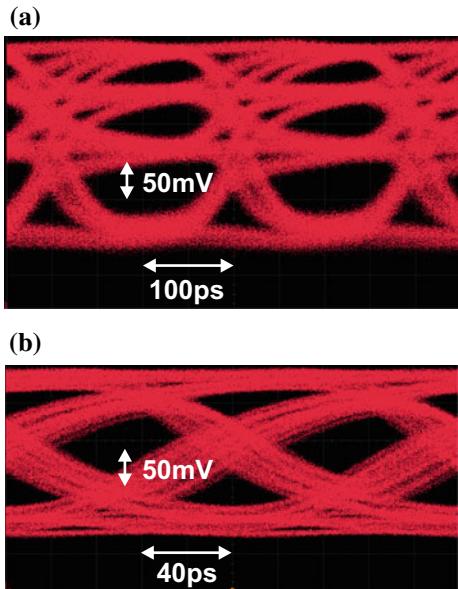


Fig. 7.21 Ring modulator driver circuit usable for PAM-4 and binary modulation

which can deliver voltage levels being independent from each other in order to optimally compensate the ring modulators nonlinearity.

Figure 7.21 shows the driver circuit [6], which biases the ring resonator in reverse direction, i.e. in depletion. Two independent binary input streams are combined to a PAM-4 signal. When both inputs are connected, a binary modulation is obtained. The output of the driver is connected to the ring modulator's anode. The cathode

Fig. 7.22 Eye diagrams measured at the output of the ring modulator driver. **a** PAM-4 and **b** binary modulation. Note that the output signals of the modulator driver are 10 times larger because of the attenuation of the picoprobe



of the ring modulator is biased by a more positive voltage to always keep the ring modulator in depletion.

ECL-like bipolar logic gates are used in the input part, which prevent saturation of the transistors. Each gate consumed 14.9 mW. Average voltage levels without needing additional bias voltages were generated with the R-C combinations between two bases from the inputs V_{in} and V_{in2} . The logic gates direct the three currents I_{ss1} , I_{ss2} , and I_{ss3} to the 250Ω resistor of the branch B depending on the inputs IN1 and IN2 to generate the PAM-4 levels or the binary levels (if IN1 and IN2 are connected to one binary signal). In order to be able to compensate the nonlinearity of the ring modulator optimally, the three current sources are controllable by bias voltages V_{b1} , V_{b2} , and V_{b3} . The cascode transistors with the constant base bias V_{bias} are necessary to make the nodes A and B low ohmic because of the three collector-substrate capacitances being located at these nodes each and because of the low collector-emitter breakdown voltage of 2.4 V of the high-speed transistors with a transit frequency of 70 GHz. The emitter follower at the output makes this node more low ohmic and increases the bandwidth. The driver in $0.35\mu\text{m}$ SiGe BiCMOS was designed for 10Gb/s in binary mode (with one NRZ 10Gb/s stream at both input) and in PAM-4 mode (with two 5Gb/s streams as input). Figure 7.22 shows the driver's output eye diagrams [6]. The output voltage of the driver fabricated as a test structure for electrical characterization was measured with a 26 GHz picoprobe having 50 fF input capacitance and a 10-fold attenuation. This picoprobe added some noise to the waveforms. In the fully 3-D integrated transmitter the load capacitance to the driver output will be smaller and faster rise and fall times are to be expected.

Table 7.1 Performance summary and comparison with the state-of-the-art optical transmitters

References	Technology	Connection type	Power consumption (energy efficiency)	Output swing or ER	Data-rate (Gb/s)	Modulation format
[23]	130 nm SOI	Monolithic	207 mW (8.28 pJ/bit)	2 V ^a	25	NRZ binary
[31]	180 nm bulk CMOS	Monolithic	1.75 mW (0.35 pJ/bit)	7.6 dB	5	NRZ binary
[32]	45 nm CMOS SOI	Monolithic	0.15 mW (0.03 pJ/bit) ^a	>6 dB	5	NRZ binary
[28]	65 nm CMOS and SOI	Wire-bonded	113.5 mW (4.5 fJ/bit)	4 V 5.3 dB	25	NRZ binary
[29]	28 nm CMOS	Wire-bonded	30.5 mW (610 fJ/bit)	1.5 V (13.7 dB)	50	NRZ binary
[24]	40 nm CMOS	3D	1.35 mW (135 fJ/bit)	2 V	10	NRZ binary
[33]	65 nm CMOS	3D	0.6 mW (100 fJ/bit)	1.2 V	6	NRZ binary
[34]	40 nm CMOS	3D	26.1 mW (1.31 pJ/bit)	>7 dB	20	NRZ binary
[35]	65 nm CMOS	Wire-bonded	121.5 mW (3.04 pJ/bit)	7 dB	40	4-PAM
[36]	IBMCMOS9WG	Monolithic	135 mW (4.8 pJ/bit)	6.5 dB	56	4-PAM
[37]	40 nm CMOS	Wire-bonded	5.8 mW (290 fJ/bit)	893 μW ^c	20	4-PAM
[30]	0.35 μm SiGe BiCMOS and SOI	3D	8 × 160 mW (160 pJ/bit)	3 V (5.04 dB)	8 × 1	NRZ binary/4-PAM
[6]	0.35 μm SiGe BiCMOS	N.A. ^b	160 mW (16 pJ/bit)	3 V	10	NRZ binary/4-PAM

^aTotal consumption and efficiency with serializer are 0.85 mW and 0.17 pJ/bit, respectively

^bElectrical test-chip

^cThe optical eye opening was reported corresponding to an optical power

The input logic gates are supplied with 2.5 V and the output part (branches A and B) are supplied with 5.7 V resulting in a total power dissipation of 160 mW or 16 pJ/bit at a voltage swing of 3 V. This power dissipation is somewhat smaller than that of 207 mW of a binary 25 Gb/s in 0.13 μm CMOS [23]. Compared to recent nanometer CMOS binary modulator driver realizations with lower power dissipations [24–28] the 0.35 μm BiCMOS realization enables cheaper chips in low ASIC production volumes because of much lower mask costs than for nanometer CMOS ASICs. It also should be mentioned that the drivers of [25, 28] were wire-bonded. A Mach-Zehnder modulator was driven differentially, which is not possible with ring modulators, and provided 4 V differential voltage to the modulator [28]. More transmitters are compared in Table 7.1. The driver for a ring modulator of [29] worked asymmetrically, whereby in reverse direction a swing of 1 V and in forward direction a swing of 0.5 V was used. There are several 4-PAM drivers mainly for Mach

Zehnder modulators for which a DAC architecture or a modulator segmented into two parts with binary modulator each was applied. The 3D-integrated ring modulator and other photonic components did not reach the desired performance and therefore only 1 Gb/s operation was achieved with the described ring modulator driver [30].

The receiver within the 3D-integrated transceiver was designed for a Ge waveguide pin photodiode similar to that in [38] with a bandwidth of 42 GHz. The receiver circuit is introduced in Fig. 7.23. A pseudo differential input structure of TIA and dummy TIA is used to be better immune against power supply noise. Post amplifiers (PA) and output buffer (OB) are fully differential to increase the output voltage swing and to reduce temperature and process tolerance influences in addition. The bandwidth of the dummy TIA is reduced with C_M to keep its noise contribution low. The receiver is capable of being used for binary and PAM-4 modulation. This is achieved by extending the Cherry-Hooper broadband PAs with a gain control mechanism by adding a four-quadrant multiplier feature. With V_{gc} , the gain can be reduced in the PAM-4 mode to avoid the limiting of PAM-4 voltages (which would occur in the binary mode). The output buffer's bandwidth is 6 GHz for $V_b = 0$ V and can be reduced to 4.9 GHz by setting V_b to 3.3 V. The supply voltage of the receiver was 3.3 V with a power consumption of 180 mW.

It was noted that the Ge photodiode's capacitance of 4 fF and the IWC's plus connection capacitance of 15 fF should be negligible to the input capacitance of the TIA of 241 fF [6]. With a wire-bonded photodiode (adding also two bondpad capacitances) the total input node capacitance can be twice as large easily and bandwidth and/or sensitivity would be worse. The 3D-integration, however, allows with a photodiode responsivity of 0.9 A/W for 1.55 μm at 10Gb/s a sensitivity of -27 dBm (binary) and of -22 dBm (PAM-4) due to postlayout simulation. Figure 7.24 presents post-layout simulated eye diagrams of the 3D-integrated receiver. The receiver shows linear behavior in PAM-4 mode.

For electrical characterization a test chip with an integrated 10 kΩ resistor connected in series to the input was fabricated. This resistor allows measurements with a network analyzer by converting the NWA's output voltage to a current emulating a photocurrent. Therefore, a bondpad capacitance of about 70 fF is present at the input of the test chip. The stray capacitances of the integrated resistor and its connection, however, were estimated to be of about the same value of a 3D-connected Ge photodiode. The electrical characterization of a test receiver chip resulted in a measured bandwidth of 7.2 GHz (binary mode) and of 6.4 GHz (PAM-4 mode). The larger values compared to simulation were explained by parasitic inductances on the PCB. These larger bandwidths, however, increased the noise compared to simulation. Sensitivities of -26.5 dBm (in binary mode) and -21.7 dBm (in PAM-4 mode) were measured. Figure 7.25 shows eye diagrams and bit-error ratio versus optical input power measured with the electrical test chip.

Compared to binary receivers in nanometer CMOS [22, 24, 25, 31, 33, 39–42] a much better sensitivity is achieved. In comparison to a 10Gb/s binary 0.35 μm BiCMOS receiver with a sensitivity of -16.4 dBm and a power consumption of 195 mW [43], the receiver of [6] shows a much better performance. The receiver of [10] with a sensitivity of -23.1 dBm (due to a photodiode responsivity of 0.5 A/W) at 10 Gb/s

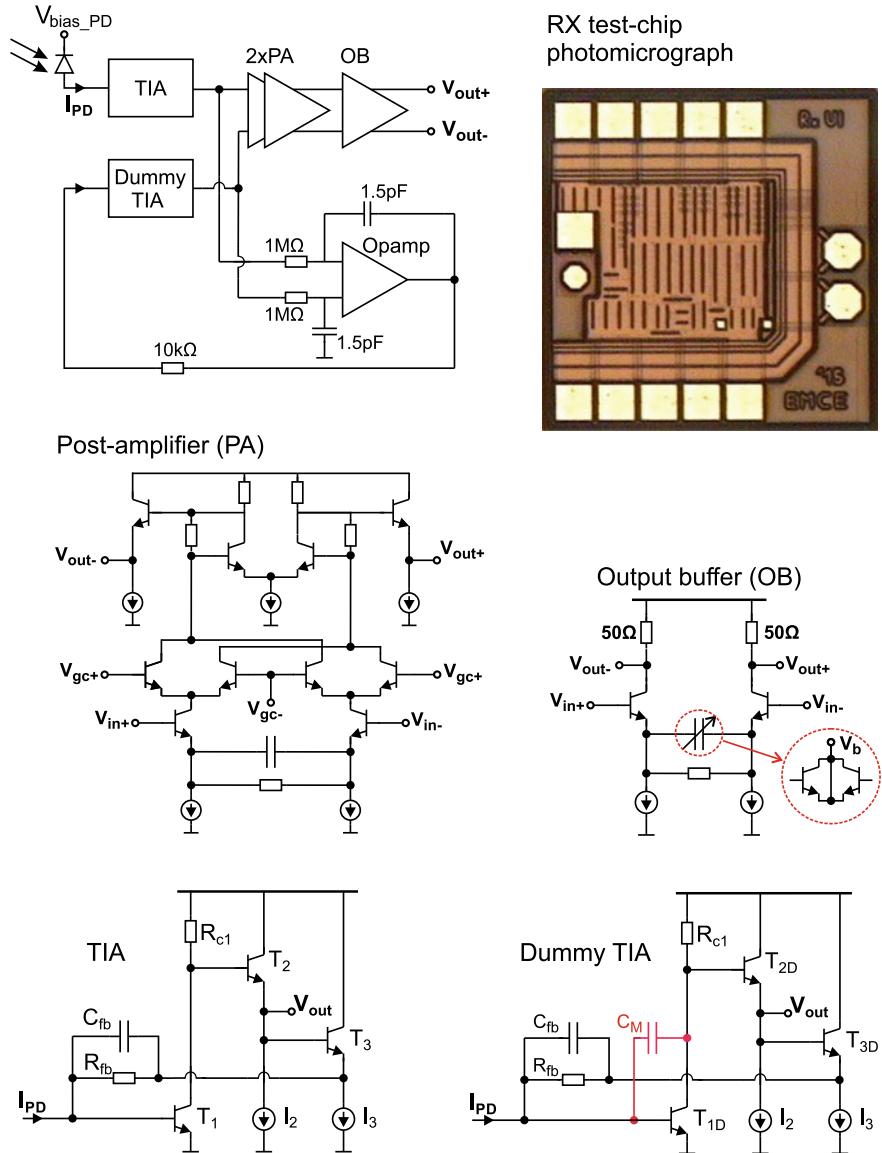


Fig. 7.23 Block diagram with laser, grating coupler, waveguide and photodiode (upper left), circuit diagrams of the blocks, and chip photo of a fabricated test chip (upper right)

was fabricated in the same $0.35\text{ }\mu\text{m}$ SiGe BiCMOS technology, but only for binary operation. Also compared to a 2.5 Gb/s PAM-4 BiCMOS receiver in $0.6\text{ }\mu\text{m}$ technology [44], this 10 Gb/s receiver in $0.35\text{ }\mu\text{m}$ Si Ge BiCMOS achieves a much better sensitivity (-22 dBm compared to -16 dBm). Table 7.2 compares more receivers.

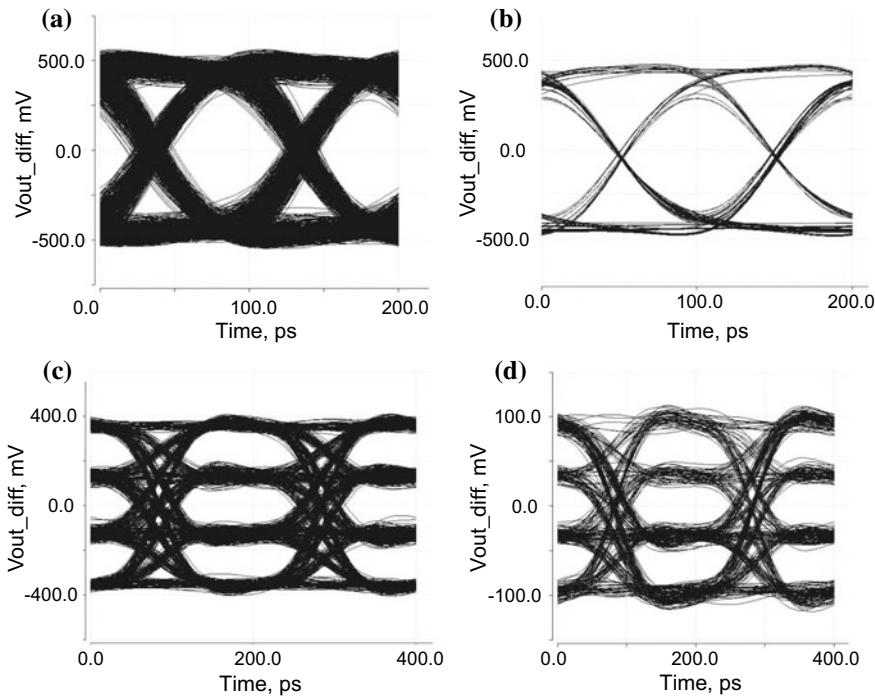


Fig. 7.24 Simulated eye diagrams with transient noise at the output of the receiver. **a** binary and -27 dBm , **b** binary and -9 dBm , **c** PAM-4 and -22 dBm , and **d** PAM-4 and -17 dBm average optical input power

When summarizing, the $0.35\text{ }\mu\text{m}$ SiGe BiCMOS receiver's very good sensitivity has to be paid for with a high power consumption (18.8 pJ/bit). In addition in a $0.35\text{ }\mu\text{m}$ SiGe BiCMOS transceiver containing the receiver and the ring modulator driver the very good sensitivity of the receiver causes a high power consumption of the transmitter.

7.4 Sensor for Optical Tomography

The wafer-to-wafer 3D-integration method described in Sect. 7.1 was exploited for an optical tomography line sensor in 130 nm 3D-CMOS technology [11]. An SPAD similar to the one introduced in [12] was implemented, however, in back-side illuminated configuration. The SPAD was formed by a circular n-type low-doped drain to p-well junction. Its breakdown voltage was 16.5 V . The photon detection probability of this SPAD was about 12% in the spectral range from 650 to 800 nm at an excess bias voltage of 1.5 V .

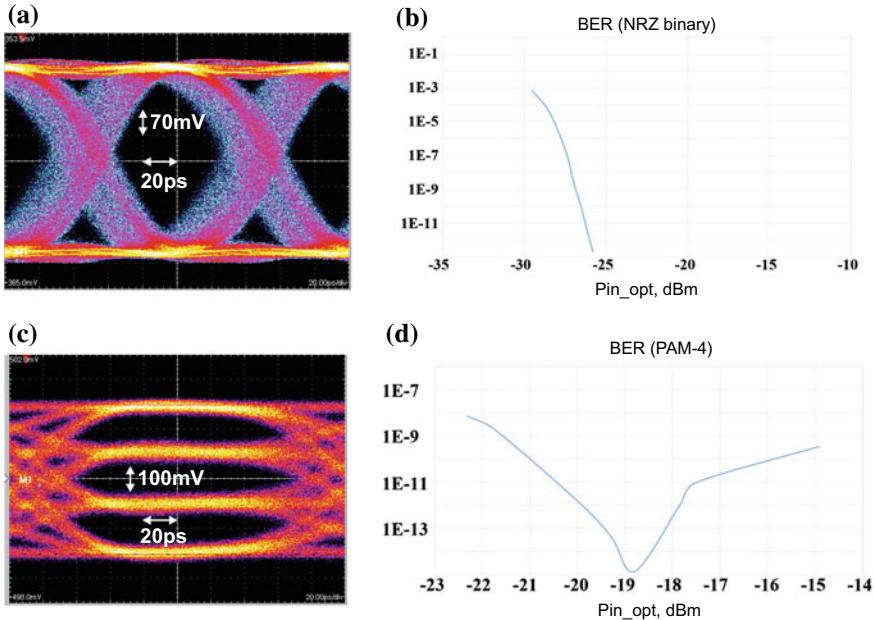


Fig. 7.25 Measured eye diagrams with PRBS31; **a** binary and -26 dBm , **c** PAM-4 and -21.7 dBm average optical input power. **b** Bit-error ratio for binary mode and **d** bit-error ratio for PAM-4 mode

The pixels implemented had a light-sensitive area of about $28 \mu\text{m}^2$. A guard ring of about $1.1 \mu\text{m}$ was implemented. The pixel pitch was $11.75 \mu\text{m}$ and the optical fill factor was 23.3% [11]. However, the potential of the technology to achieve fill factors of 70% was mentioned [11]. A p-channel MOSFET (TQ) was used as active resistor with a resistance of about $100 \text{ k}\Omega$ for passive quenching (see Fig. 7.26). Another p-MOS transistor (TB) was implemented together with this transistor TQ in the top wafer (photodiode wafer) as a buffer to the electronics wafer in order to keep the loading to the SPAD's cathode small. So, the number of MOSFETs was kept low in the top wafer (photodiode wafer) to obtain a large fill factor. The PMOS transistor used as a quenching resistor also was used for recharging the SPAD. Its deadtime (recovery time) was adjustable via VQCH [11]. TQ, TB, TI, TP, and TN were thicker gate oxide transistors. MN and MP were thin-oxide transistors. TQ and TB were in the top wafer (photodiode wafer). TI, TP, TN, MP, and MN were in the bottom wafer (electronics wafer).

The complete sensor chip contained two arrays of 400 SPADs each in the top wafer and 100 signal processing blocks in the electronics wafer [11]. Each processing block contained a winner-takes-all (WTA) circuit, a time-to-digital converter (TDC), and a 2-port static random access memory (SRAM). So the SPADs were clustered in groups of 8 pixels. After detection of a photon, the TDC belonging to this cluster calculated the time stamp for the photon. This time stamp was stored in the clusters SRAM until it was read out via a multiplexer [11].

Table 7.2 Performance summary and comparison with the state-of-the-art broadband optical receivers with a pin photodiode

References	Technology	Connection with PD	Data rate	Sensitivity	BER	Responsivity	Power consumption (energy efficiency)
[23]	130 nm CMOS and SOI	Monolithic	25 Gb/s	-6 dBm	10^{-12}	0.8 A/W	256 mW (10.24 pJ/bit)
[33]	65 nm CMOS and SOI	3D	7 Gb/s	-14.5 dBm	10^{-12}	0.73 A/W	1.96 mW (0.28 pJ/bit)
[45]	40 nm CMOS	Wire-bonded	20 Gb/s	-10.8 dBm	10^{-12}	0.53 A/W	22.6 mW (1.13 pJ/bit)
[27]	28 nm CMOS and AIST SOI	3D	25 Gb/s	-6 dBm	10^{-12}	0.8 A/W	50 mW (2 pJ/bit)
[46]	28 nm CMOS	3D	25 Gb/s	-14.9 dBm	10^{-12}	0.2 A/W	4.3 mW (0.17 pJ/bit)
[47]	14 nm FinFET CMOS	3D	32 Gb/s	-11.7 dBm	10^{-12}	0.52 A/W	45.12 mW (1.41 pJ/bit)
[10]	0.35 μ m SiGe BiCMOS	3D ^a	10 Gb/s	-23.1 dBm ^b	10^{-9}	0.5 A/W	175 mW (17.5 pJ/bit)
[48]	130 nm SiGe BiCMOS	Wire-bonded	32 Gbaud	-3 dBm	10^{-3}	0.44 A/W	165 mW (2.58 pJ/bit)
[49]	0.6 μ m BiCMOS	Monolithic	1.25 Gbaud	-16 dBm	10^{-9}	0.52 A/W	100 mW (40 pJ/bit)
[30]	0.35 μ m SiGe BiCMOS and SOI	3D	8×10 Gb/s	-8.5 dBm	10^{-9}	0.75 A/W ^c	8×185 mW (18.5 pJ/bit)
[6]	0.35 μ m SiGe BiCMOS	N.A.	10 Gb/s	-25.3 dBm ^d	10^{-9}	0.75 A/W	188 mW (18.8 pJ/bit)

^aAn optical receiver designed for a 3D integration with through-silicon vias; the 3D integration was not performed

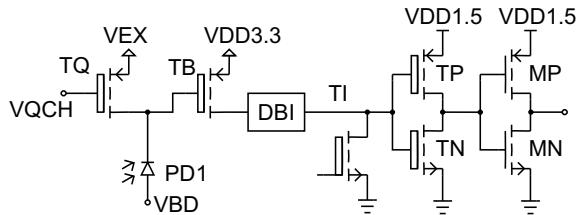
^bSimulated value for the 3D-integrated optical receiver for the expected responsivity of 0.5 A/W

^cMaximum value of PD responsivity measured on a separate photonic test-wafer was assumed; exact value of PD responsivity on the measured receiver could not be determined

^dTest-chip with an electrical input, where 3D integration was not performed; sensitivity is calculated based on the assumed value of PD responsivity

Although the detection rate in near-infrared optical tomography (NIROT) is quite low (about 1%), the loss of photons during the conversion time of the TDC required to choose the cluster size of 8 pixels leading to only 4% data loss of totally detected photons [11]. To avoid the high power consumption of ring oscillators in the GHz range, when many TDCs are active [50], a dual-speed ring oscillator was proposed, which operates only in a small fraction of the conversion time in the GHz range. The five most significant bits were determined with an oscillator frequency of 246 MHz

Fig. 7.26 Pixel circuit with SPAD and buffer (DBI = direct bond interface)



using a low-speed counter. Then the ring oscillators frequency was increased to 2.52 GHz and a high-speed counter determined the other 7 bits. In such a way 12 bit TDC resolution was achieved at low power consumption. One LSB corresponded to 49.7 ps time resolution. The standard deviation of this resolution over the whole array was reported to be 0.8 ps. The rms jitter was 1.22 LSB. The SPAD's FWHM jitter was 260 ps. The TDC's range was 200 ns and a dynamic power consumption of 15 μ W at 500 kS/s was reported at a static power consumption of 7 mW in the dark [11]. The source-detector distance was in the range from 2 to 4 cm.

7.5 Sensor for 3D Microimaging

Frequency-modulated continuous-wave (FMCW) LIDAR (light detection and ranging) achieves at small distances a better distance measurement accuracy than time-of-flight ranging. An electronic-photonic integrated FMCW LIDAR 3D imager was presented in [51]. A CMOS IC in 0.18 μ m technology and a 250 nm silicon photonic chip were 3D integrated and connected with 50 μ m-diameter, 200 μ m high through silicon vias (TSVs) in the photonic chip. Both chips were $3 \times 3 \text{ mm}^2$ in size. Techniques for precise laser frequency modulation introduced with bench-top devices [52, 53] were implemented. A phase-locked loop (PLL) modulated the frequency of a tunable laser diode at 1530 nm (1550 nm in [54]). In FMCW the optical frequency of a laser is linearly modulated with time. The laser frequency changes during the travelling time of the light from the laser to the object and back to the detector. Therefore, there results a difference frequency f_R , which is proportional to the object distance D, when the two light beams interfere:

$$f_R = \frac{2\gamma}{c_0} D \quad (7.1)$$

where γ is the change rate of the laser frequency and c_0 is the vacuum light velocity.

The electronic part of the electro-optical (EO) PLL for precise laser frequency variation was integrated in the CMOS chip [51]. The silicon photonic chip contained input optical couplers, waveguides, an asymmetric Mach-Zehnder interferometer (MZI) and photodiodes. The asymmetry of the MZI was necessary to obtain a beat tone with a constant delay between the two arms of the MZI. The beat frequency at

the output of the MZI was proportional to the deviation of the modulation slope γ . This EO-PLL was used to lock the beat frequency to an electronic local oscillator fixing γ to a constant value. A value of $\gamma = 22 \text{ GHz}/\mu\text{s}$ was used. Without the EO-PLL the nonlinearity of the distributed Bragg reflector (DBR) laser diode using carrier injection tuning could result in a distance measurement error of $65 \mu\text{m}$. This would for instance be too bad for application in 3D printers, which can achieve depths resolutions of about $20 \mu\text{m}$. A TIA and a limiting amplifier converted the photocurrent of the MZI Ge pin photodiode [54] to a square voltage as an input to the phase detector charge pump. The TIA exploited a low-impedance g_m -boosted input transistor and a current comparator with a high-pass current mirror to filter the low-frequency part of the MZI output signal due to laser intensity fluctuations.

The experimental setup for distance measurements was completed by off-chip optics, photodiode and post-processing. With a gear at a distance of 40 cm from the sensor's lens, a precision σ of $11 \mu\text{m}$ was achieved with $100 \mu\text{s}$ per measurement. An rms depth resolution of $8 \mu\text{m}$ at distances of less than $+/- 5 \text{ cm}$ from the range baseline was reported. A maximum range of 1.4 m at a precision of 4.2 mm was given [51].

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