A VLSI Array of Low-Power Spiking Neurons and Bistable Synapses With Spike-Timing Dependent Plasticity

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***Abstract*—We present a mixed-mode analog/digital VLSI device comprising an array of leaky integrate–and–fire (I&F) neurons, adaptive synapses with spike–timing dependent plasticity, and an asynchronous event based communication infrastructure that allows the user to (re)configure networks of spiking neurons with arbitrary topologies. The asynchronous communication protocol used by the silicon neurons to transmit spikes (events) off-chip and the silicon synapses to receive spikes from the outside is based on the "address–event representation" (AER). We describe the analog circuits designed to implement the silicon neurons and synapses and present experimental data showing the neuron's response properties and the synapses characteristics, in response to AER input spike trains. Our results indicate that these circuits can be used in massively parallel VLSI networks of I&F neurons to simulate real–time complex spike–based learning algorithms.**

***Index Terms*—Address–event representation (AER), analog VLSI, integrate-and-fire (I&F) neurons, neuromorphic circuits, spike-based learning, spike-timing dependent plasticity (STDP).**

I. Introduction

A growing interest in pulse–based neural networks is driving the design and fabrication of an increasing number of VLSI networks of integrate–and–fire (I&F) neurons [1]–[7]. These new types of devices are used to implement specific models of cortical processing for scientific investigation [3], [5], [6], with the aim of developing the technology and infrastructure for engineering applications.

Several examples of successful multichip networks of spiking neurons have been recently proposed [6], [8], [9]; however, there are still a number of practical problems that hinder the development of truly large–scale, distributed, massively parallel networks of VLSI I&F neurons. Three of the most important ones are: 1) how to access the individual synapses of the network for providing input signals, and how to read from each neuron for generating output signals; 2) how to set the weight of individual synapses in the network; and 3) how to (re)configure the network topology on the same chip.

In this paper, we present a VLSI device with a one-dimensional array of I&F neurons, and a two-dimensional (2-D) matrix of adaptive plastic synapses that use the "address–event representation" (AER) [10]–[13] to transmit and receive spikes. We will show how the use of the AER communication protocol allows us to simultaneously solve problems 1) and 3) above, while the plastic synaptic circuits allow us to cope with problem 2) by setting the synaptic weights via a learning algorithm.

While mean rate Hebbian learning algorithms are difficult to implement using analog circuits, spike-timing-based learning rules map directly onto silicon [4], [7], [14], [15]. A promising class of spike-driven learning rules that is particularly well suited to VLSI implementation is the one based on the spike-timing dependent plasticity (STDP) mechanism [16], [17]. In STDP the precise timing of spikes generated by the pre- and postsynaptic neurons have an important role in shaping the synaptic efficacy. If a presynaptic spike arrives at the synaptic terminal before a postsynaptic spike is emitted, within a critical time window, the synaptic efficacy is increased. Conversely, if the postsynaptic spike is emitted soon before the presynaptic one arrives, the synaptic efficacy is decreased. Several modeling studies have developed learning algorithms based on STDP, and demonstrated how systems that use these types of algorithms can carry out complex information processing tasks [18]–[21].

We describe in detail the circuit implementation of the STDP learning mechanism in Section IV, but first we describe the general architecture of the VLSI device, the principle of operation of the AER communication protocol in Section II, and the circuital implementation of the I&F neuron in Section III. Section VI contains the discussion and concluding remarks.

II. VLSI Device

The device, implemented using a standard AMS 0.8 μm CMOS process. It comprises a linear array of 32 low–power I&F neurons, a 2-D array of 32×8 synaptic circuits, and input/output AER interfacing circuits (see Fig. 1). Each neuron receives input current from two inhibitory and six excitatory synapses. The neuron circuitry occupies an area of 83×31 μm^2, while the inhibitory and excitatory synapses measure 55×31 μm^2 and 145×31 μm^2, respectively.

The 6×32 excitatory synapses are divided into two groups that have independent bias settings for the synaptic weights parameters. All other bias parameters are global. The two sets of independent bias settings for the excitatory synapses allow us to model populations of synapses with different characteristics (e.g., long and short time constants, weak and strong excitatory weights, etc.). In addition to the synaptic input, the neurons

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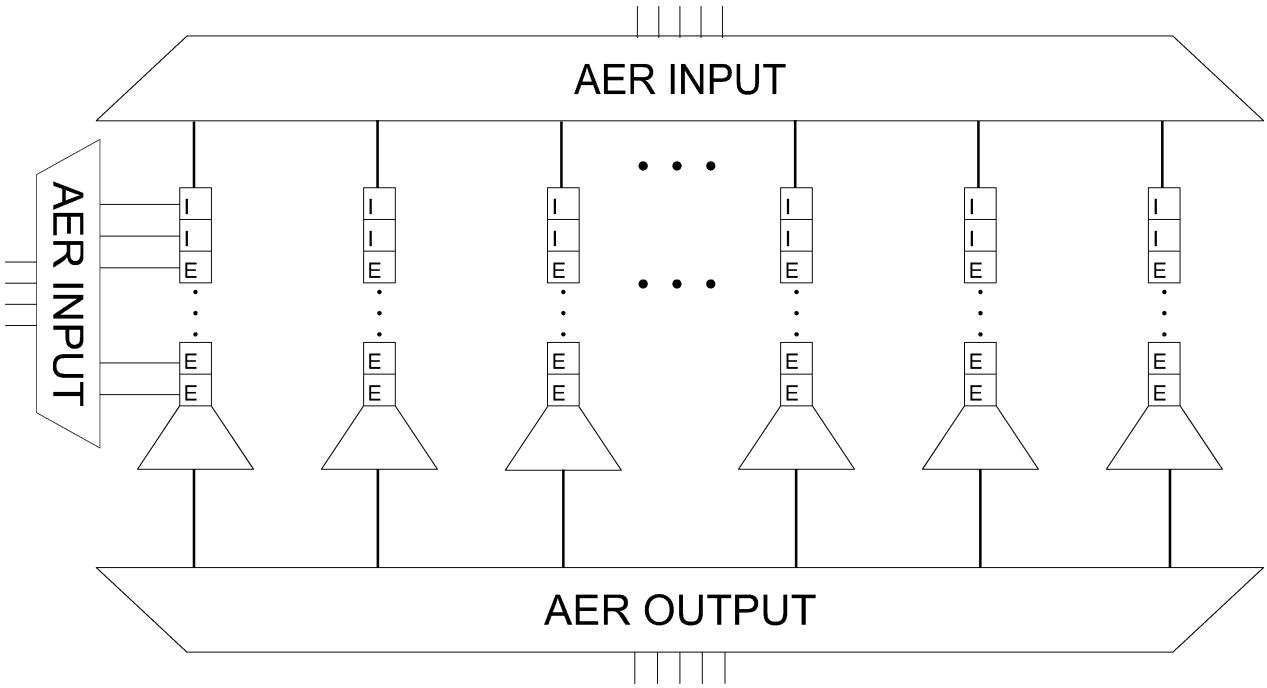


Fig. 1. Block diagram of the chip's architecture. Squares represent excitatory (E) and inhibitory (I) synapses; trapezoids represent I&F neurons. When an AER input signal arrives, the column and row encoders generate an input pulse on the addressed synapse. The I&F neuron's output spikes are sent to the on–chip AER output circuits which generate address–event signals.

in the array can be stimulated by direct current injection. The injection currents are applied through 32 parallel p-type transistors driven by a common gate voltage. Each of the 32 neurons' output spikes are transmitted off-chip via the AER output circuits and so can be routed to an arbitrary number of input synapses either on the same chip or on a different one, via an AER-based communication infrastructure. In AER, each spiking element is assigned an address that is written on a digital bus, using asynchronous logic, each time a spike is emitted. A four-phase handshaking protocol is used to manage the asynchronous communication. Input and output spikes (events) are transmitted as real–time asynchronous binary data streams that carry analog information in their temporal structure. Event collisions (cases in which multiple sending nodes generate events at the same time) are handled by on-chip arbitration circuits. Systems containing multiple AER chips can be constructed by implementing special purpose off–chip arbitration schemes [13], [22]. Once in the digital domain, address events can be remapped from multiple sending nodes to a single receiving node, or from a single sending node to multiple receiving nodes, allowing the user to arbitrarily reconfigure the network connectivity within the constraints imposed by the resources available.

III. VLSI Device's Neurons

Generally, VLSI I&F neurons integrate presynaptic input currents and generate a voltage pulse when the integrated voltage reaches a threshold. A very simple but influential circuit implementation of this model is the "Axon–Hillock" circuit, proposed by Mead in the late eighties [23]. In this circuit, an integrating capacitor is connected to two inverters, a feedback capacitor, and a reset transistor driven by the output inverter. A spike is emitted when the integrated voltage crosses the switching threshold of the first inverter. The Axon–Hillock circuit is very compact, comprising only six transistors and two capacitors, but it has a major drawback: it dissipates significant amounts of power. This dissipation occurs because the input to the first inverter (the voltage on the capacitor) changes typically with time constants of the order of milliseconds, with the result that the inverter spends a large amount of time in the region in which both transistors conduct a short-circuit current. A further drawback is that the Axon–Hillock circuit has a spiking threshold that depends only on CMOS process parameters (the switching threshold of the inverter), and does not model additional neural characteristics, such as spike-frequency adaptation properties or refractory period mechanisms [24].

An alternative design in which an explicit threshold voltage can be set and which implements spike-frequency adaptation is proposed in [25]. This design, however, also has large power consumption for the same reasons as the Axon–Hillock circuit. In [26], van Schaik proposed a circuit with an amplifier at the input that compares the voltage on the capacitor with a desired spiking threshold voltage. When the input exceeds the spiking threshold, the amplifier drives the inverter strongly, making it switch very rapidly. This circuit consumes less power than previously proposed ones, but still lacks spike-frequency adaptation.

An I&F circuit optimized with respect to power consumption, but still lacking spike-frequency adaptation, refractory period and spiking threshold modulation capabilities, was recently proposed in [27]. Here, we propose a compact leaky I&F circuit optimized for power consumption based on the design proposed in [27], that implements spike-frequency adaptation as well as a tunable refractory period, and voltage threshold modulation. The spike frequency adaptation mechanism used in our silicon

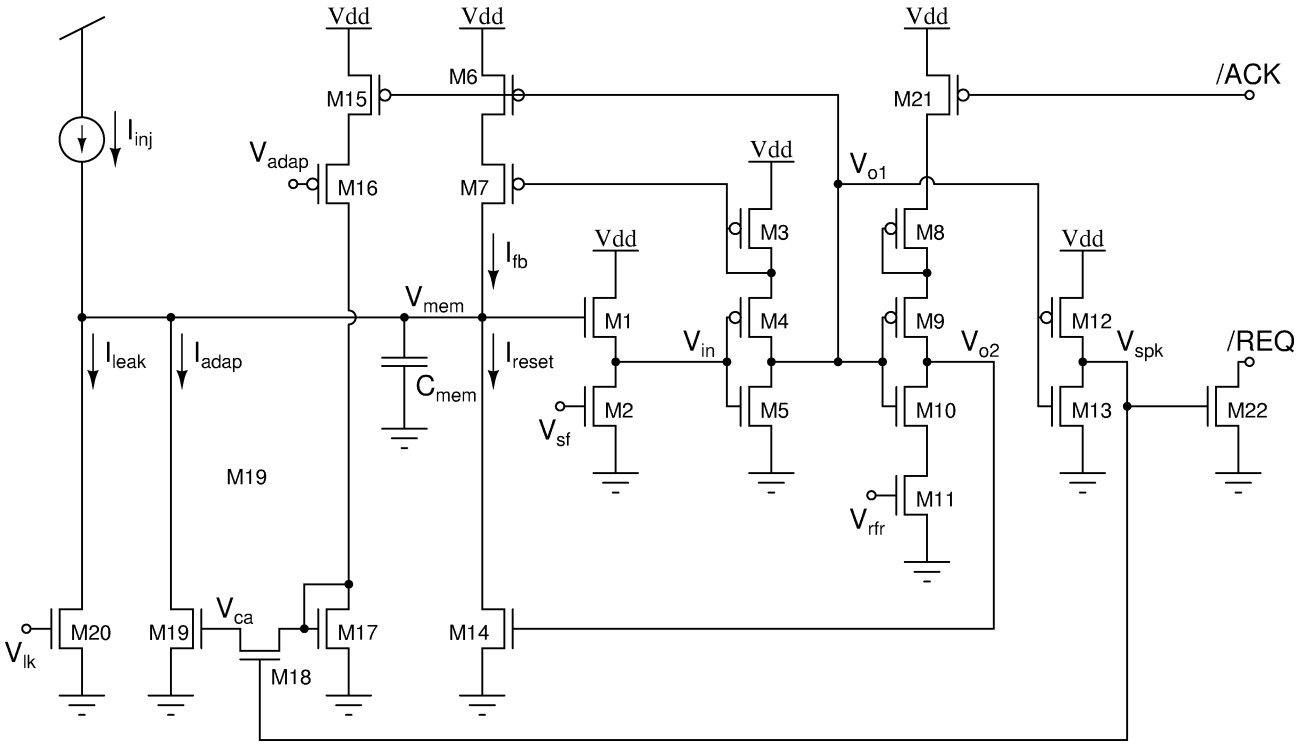


Fig. 2. Circuit diagram of the I&F neuron. See Section III-A for a detailed description of circuit operation.

neuron models the effect of calcium-dependent afterhyperpolarization potassium currents ($I_{\rm ahp}$) present in biological neurons [28] (see Section III-A). Continuous improvements in VLSI technology allow for the fabrication of AER devices containing vasts numbers of spiking elements operating in parallel. These devices will be practically realizable only if the spiking neuron circuits have minimal power consumption locally, implement pulse-frequency saturation (refractory periods) for limiting the power consumption globally, and contain spike frequency adaptation mechanisms to reduce communication bandwidth for the transmission of address-events.

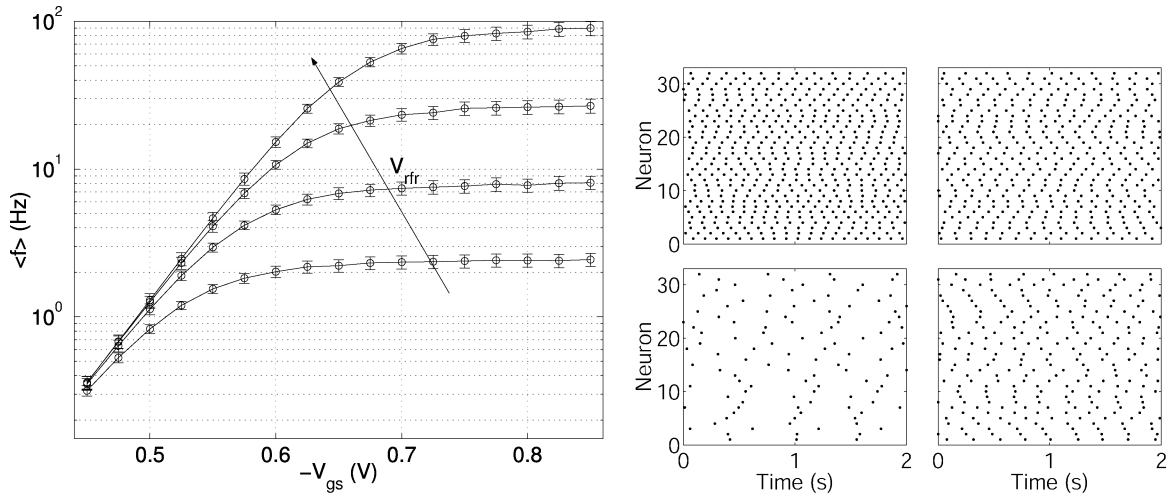
A. I&F Circuit Operation

The circuit diagram of the I&F neuron we propose is shown in Fig. 2. The circuit comprises an integrating capacitor $C_{\rm mem}$; a source follower M1-M2, used to control the spiking threshold voltage; an inverter with positive feedback M3-M7, for reducing the circuit's power consumption; an inverter with controllable slew-rate M8-M11, for setting arbitrary refractory periods; an inverter M12-M13, for generating digital pulses; a current integrator M15-M19, for spike-frequency adaptation, the transistor M20 for setting a leak current; and M21-M22 for receiving and producing the AER handshaking signals */ACK* and */REQ*, respectively.

The input current $I_{\rm inj}$ is integrated by $C_{\rm mem}$ onto $V_{\rm mem}$. In the current implementation $C_{\rm mem}$ is 432 fF, and its layout occupies an area of 244 μm^2. Typical injection currents are of the order of tens of picoamperes. The source-follower M1-M2, produces $V_{\rm in} = \kappa(V_{\rm mem} - V_{\rm sf})$, where $V_{\rm sf}$ is a constant subthreshold bias voltage and κ is the subthreshold slope coefficient [29]. As $V_{\rm mem}$ increases and $V_{\rm in}$ approaches the switching voltage of the first inverter, the feedback current $I_{\rm fb}$ starts to flow through M6-M7, increasing $V_{\rm mem}$ and $V_{\rm in}$ more rapidly. The positive feedback has the effect of making the inverter M3-M5 switch very rapidly, reducing dramatically its power dissipation.

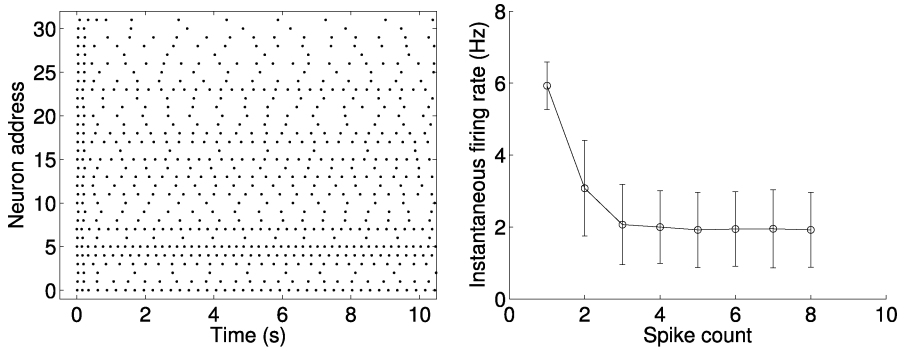
When $V_{\rm mem}$ increases enough to make the first inverter switch, the voltage $V_{\rm spk}$ is driven to $V_{\rm dd}$, and the AER request signal */REQ* is pulled to ground (i.e., a request to transmit is signaled to the output AER circuits). Provided that the AER handshaking signal */ACK* (driven from the output AER circuits) is low, V_{o2} is brought to $V_{\rm dd}$, the membrane capacitor $C_{\rm mem}$ is quickly discharged back to ground through the reset transistor M14, and the voltage $V_{\rm spk}$ is reset to zero. During the spike emission period (while $V_{\rm spk}$ is high), a current with amplitude set by $V_{\rm adap}$ is sourced into the gate-to-source parasitic capacitance of M19 on node $V_{\rm ca}$. Thus, the voltage $V_{\rm ca}$ increases with every spike, but when there is no spiking activity $V_{\rm ca}$ slowly leaks to zero through leakage currents. As $V_{\rm ca}$ increases, a negative adaptation current $I_{\rm adap}$ that is exponentially proportional to $V_{\rm ca}$ is subtracted from the input, and the spiking frequency of the neuron is reduced over time. When $V_{\rm mem}$ is discharged to ground V_{o1} is driven back to $V_{\rm dd}$, thus turning M10 fully on. The voltage V_{o2} is then discharged through the path M10-M11, at a rate set by $V_{\rm rfr}$ (and by the parasitic capacitance on node V_{o2}). As long as V_{o2} is sufficiently high, the reset transistor M14 is active and $V_{\rm mem}$ is clamped to ground. During this "refractory" period, the neuron cannot spike, as all the input current $I_{\rm inj}$, typically smaller than the reset current, is absorbed by M14.

We tested the response properties of the I&F neurons in the array by injecting constant currents to the neurons (bypassing the synapses) and measuring their firing rates, for different settings of the refractory period bias voltage $V_{\rm rfr}$. We generated currents exponentially proportional to the gate-to-source voltage $V_{\rm gs}$ of the p-fets connected to each neuron in the array,



(a) (b)

Fig. 3. (a) Mean response of all neurons in the array to increasing values of a global input current, for four different refractory period settings (set by biasing $V_{\rm rfr}$ of Fig. 2 to 0.30, 0.35, 0.40, and 0.45 V, respectively). The error bars represent the standard deviation of the responses throughout the array. (b) Raster plots showing the activity of the whole array in response to the input current set by $V_{\rm gs} = -0.575$ V, for the same four increasing values of $V_{\rm rfr}$ (counterclockwise from the bottom left box).



(a) (b)

Fig. 4. (a) Raster plot showing the response of the array of neurons to a step input current, with spike-frequency adaptation activated ($V_{\rm adap} = 4.15$ V). (b) Instantaneous firing rate as a function of spike count, averaged throughout the array. The error-bars represent the standard deviation of the neurons' firing rates throughout the array.

and measured their mean firing rates (see Fig. 3). Given the exponential relationship between $V_{\rm gs}$ and the injected current [29], Fig. 3(a) shows how the firing rate increases linearly with the input current, saturating at higher asymptotic values for increasing values of $V_{\rm rfr}$ (decreasing refractory period duration). Fig. 3(b) shows four *raster plots* of the activities of all neurons in the array in response to uniform input current, for increasing (clockwise from the top left box) refractory period durations.

To show the effect of spike-frequency adaptation, we plotted in Fig. 4(a) spike raster plots measured immediately after the onset of a constant stimulus input current to the whole array, with the adaptation rate set to $V_{\rm adap} = 4.15$ V. As the capacitor used to store the adaptation bias voltage $V_{\rm ca}$ is very small (a parasitic capacitance in the layout), mismatch in adaptation current is quite high. Fig. 4(b) shows the instantaneous firing rate of all neurons in the array as a function of spike count averaged throughout the array. The error-bars, representing the standard deviation of the firing rate, show that there is a much higher variability across the array of I&F neurons when they fire in their adapted state [compare also with the error-bars of Fig. 3(a), where the spike frequency adaptation was switched off]. The raster-plot data of Figs. 3 and 4 was collected using a custom PCI–AER board, able to interface AER chips to workstations, and to record the address events generated by the chip [22].

B. Modeling the Neuron's Subthreshold Behavior

The circuit shown in Fig. 2 does not implement a simple linear model of an I&F neuron. Rather its positive feedback and spike-frequency adaptation mechanisms represent additional features that increase the model's complexity (and its computational capabilities). The overall current integrated by $C_{\rm mem}$ is $I_{\rm inj} - I_{\rm leak} + I_{\rm fb} - I_{\rm adap}$, where $I_{\rm inj}$ is the circuit's external input current, $I_{\rm leak}$ is a leakage current set by a constant bias voltage V_{lk}, $I_{\rm fb}$ is the positive feedback current and $I_{\rm adap}$ is the adaptation current generated by the spike-frequency adaptation mechanism. We can use the transistor's weak-inversion equations [29] to compute the adaptation current

$$I_{\rm adap} = I_0 {\rm e}^{\kappa V_{\rm ca}/U_T}(1 - {\rm e}^{-V_{\rm mem}/U_T}) \qquad (1)$$

where I_0 is the transistor's dark current [29] and U_T is the thermal voltage. A similar equation can be written for $I_{\rm leak}$, with V_{lk} in place of $V_{\rm ca}$.

If we denote with C_a the parasitic gate-to-source capacitance on node $V_{\rm ca}$ of M19, and with C_p the parasitic gate-to-drain capacitance on M19, then

$$V_{\rm ca} = V_{\rm ca_0} + \gamma V_{\rm mem} \tag{2}$$

where γ is given by the capacitive divider ratio $C_p/(C_p + C_a)$ and $V_{\rm ca_0}$ is the steady-state voltage stored on C_a, updated with each spike.

To model the effect of the positive feedback we can assume, to first order approximation, that the current mirrored by M3,M7 is

$$I_{\rm fb} = I_1 {\rm e}^{\kappa V_{\rm in}/U_T} \tag{3}$$

where I_1 is a constant current flowing in the first inverter when both M4-M5 conduct, and $V_{\rm in} = \kappa(V_{\rm mem} - V_{\rm sf})$ is the output of the source-follower M1-M2.

The equation modeling the subthreshold behavior of the overall circuit is

$$C_0 \frac{d}{dt} V_{\rm mem} = I_{\rm inj} - I_{\rm leak} + I_{\rm fb} - I_{\rm adap} \tag{4}$$

where $C_0 = C_m + \gamma\, C_a$ is the total capacitance seen at the input node. Substituting $I_{\rm adap}$ and $I_{\rm fb}$ with the equations derived above we obtain

$$\begin{aligned} C_0 \frac{d}{dt} V_{\rm mem} = {} & I_{\rm inj} - I_0 {\rm e}^{\kappa V_{lk}/U_T} \left(1 - {\rm e}^{-V_{\rm mem}/U_T}\right) \\ & + I_1 {\rm e}^{-\kappa^2 V_{\rm sf}/U_T} {\rm e}^{\kappa^2 V_{\rm mem}/U_T} \\ & - I_0 {\rm e}^{\kappa V_{\rm ca_0}/U_T} {\rm e}^{\kappa\gamma V_{\rm mem}/U_T} \left(1 - {\rm e}^{-V_{\rm mem}/U_T}\right). \end{aligned} \tag{5}$$

For values of $V_{\rm mem} \geq 4U_T$ the above equation simplifies to

$$\begin{aligned} & C_0 \frac{d}{dt} V_{\rm mem} \\ & = I_{\rm net} + I_1 {\rm e}^{-\kappa^2 V_{\rm sf}/U_T} {\rm e}^{\kappa^2 V_{\rm mem}/U_T} - I_0 {\rm e}^{\kappa V_{\rm ca_0}/U_T} {\rm e}^{\kappa\gamma V_{\rm mem}/U_T} \end{aligned} \tag{6}$$

where $I_{\rm net}$ is the net input current (the injection current minus the leak current). This simplified equation has been shown to correctly fit experimental data [30] and can be used to reliably simulate (in software) arbitrary networks of spiking neurons implemented using the circuit of Fig. 2.

C. Power Dissipation Characteristics

The main sources of power dissipation of the integrate and fire neurons are the short-circuit currents that flow through the inverters during the switching time and the DC current that flows through the source-follower M1-M2 during the periods in which $V_{\rm mem} > (V_{\rm sf} + 4U_T)$ (see Fig. 2). When no input current is applied (in resting conditions) the leakage current brings $V_{\rm mem}$ to zero, transistor M1 of the source follower does not conduct, and the inverters do not switch. In this condition the power dissipation is nil. When input current is applied, the power dissipation is a function of firing rate, of the source-follower bias $V_{\rm sf}$, and of the power supply voltage $V_{\rm dd}$. We measured the circuit's power dissipation in a device implemented using a 0.35 μm CMOS technology. With *optimal* bias settings the whole neuron, including spike frequency adaptation, refractory period, and source-follower circuits, dissipates approximately 900 pJ per spike.

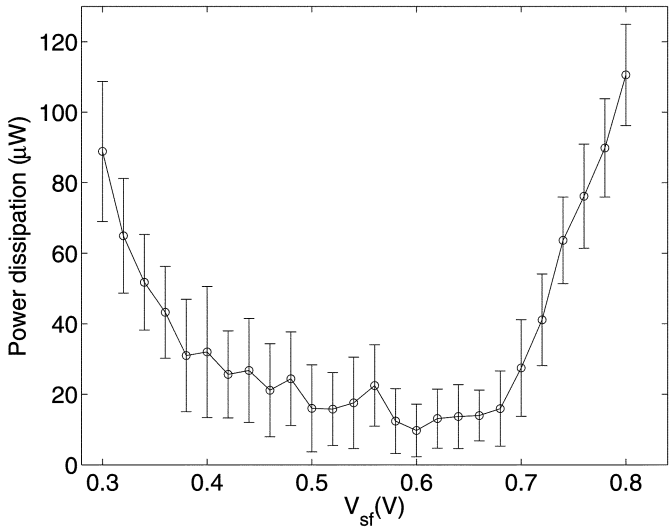


Fig. 5. Mean power dissipation of the neuron as a function of $V_{\rm sf}$ for an average output firing rate of about 100 Hz and typical operating condition bias settings (see text for details). The error bars represent the data's standard deviation measured over 100 trials.

We also measured the circuit's power dissipation in *typical* operating conditions: refractory period set to limit the maximum firing rate to about 200 Hz ($V_{\rm rfr} = 225$ mV), and spike frequency adaptation enabled ($V_{\rm adap} = 2.9$ V). Under these conditions we show, in Fig. 5, how the power disspiation depends on the circuit's source-follower's bias $V_{\rm sf}$. The power supply voltage was 3.3 V and the injection current $I_{\rm inj}$ was adjusted to generate spike trains at a mean rate of approximately 100 Hz. As expected, the mean power dissipation increases with $V_{\rm sf}$, for high bias values. Power dissipation is also high for very low values of $V_{\rm sf}$ due to the fact that the source follower acts as a low-pass filter on the falling edge of the spike, thus increasing the switching time of the inverter M4-M5 of Fig. 2. For comparison, simulations of the Axon–Hillock circuit under similar operating conditions predicted average power-dissipation values more than two orders of magnitude larger.

IV. VLSI Device's Synapses

Silicon synapses are circuits typically used in VLSI networks of I&F neurons for implementing models of biological synapses [12], [31]–[34]. Recent developments in the neuroscience community provide evidence that synapses are not simple interfacing elements for transmitting signals between neurons, but play an important computational role in biological neural networks [35]. One of the key properties of biological synapses is their ability to exhibit *short–* and *long–term* plasticity. The former type of plasticity produces dynamic modulation of the synaptic strength by the timing of the input stimulation [36]; while the latter produces long term changes in synaptic strength, induced by the spiking activity of the pre- and postsynaptic processes [37], [38].

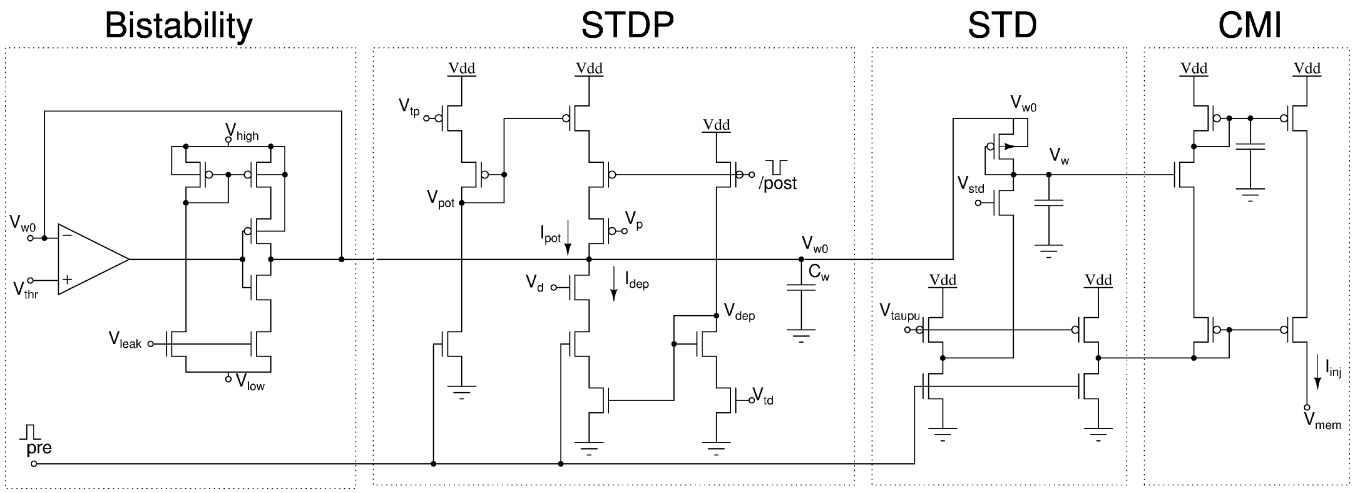
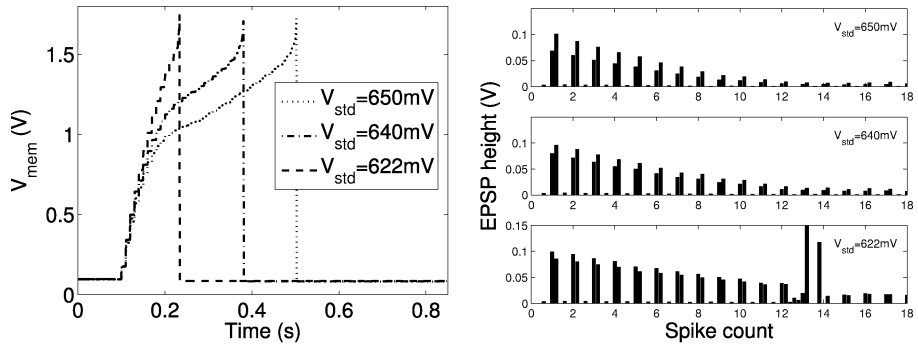


Fig. 6. Excitatory synapse circuit. The bistability circuit compares the voltage V_{w0} to a threshold and drives it to one of two asymptotic values ($V_{\rm low}$ or $V_{\rm high}$). The STDP circuit increases (or decreases) V_{w0} with every post- (pre-) synaptic spike provided the pre- (post-) synaptic spike was emitted shortly before. The STD circuits implement short-term depression decreasing the synaptic weight V_w with every presynaptic spike, at a rate set by $V_{\rm std}$. The CMI circuit implements a current-mirror-integrator and generates a postsynaptic current that is injected into the neuron.



(a) (b)

Fig. 7. (a) Spike traces obtained by stimulating the short-term depressing synapse with an input train of 100 Hz, for increasing values of the adaptation bias $V_{\rm std}$. (b) EPSP height as a function of spike count, for three different values of $V_{\rm std}$ (see text for details).

Silicon implementations of synapses that exhibit *short-term* plasticity are suitable for evaluating the computational roles of synaptic adaptation in large networks of spiking neurons using complex stimuli and in real-time [39], [40]. Implementations of *long-term* plasticity circuits allow us to implement learning algorithms and set synaptic weights of synapses automatically, without requiring dedicated pins or wires for individual synapses.

The excitatory synaptic circuit we propose (see Fig. 6) implements both types of plasticity mechanisms. In this circuit, long–term plasticity is implemented using the "STDP" and "bistability" blocks (described in Sections IV-B and IV-C, respectively), while short–term plasticity is implemented by the "STD" block (described in Section IV-A). The integrating properties of the synapse itself are achieved by using a current–mirror integrator (CMI) circuit [12]. Functionally, the CMI circuit operates in the following way: each time an input spike arrives on the node "pre" of Fig. 6, an amount of charge set by the synaptic weight voltage V_w is injected into the CMI's integrating capacitor and the current $I_{\rm inj}$ is increased accordingly. In the absence of spikes, the charge decays through the diode connected transistor and the synaptic current goes to zero. A thorough analysis of this compact and elegant nonlinear integrator circuit, in which an explicit analytical solution that does not require a steady-state assumption is derived, is presented in [34].

In the device proposed here, 32×6 synapses are excitatory and plastic (as shown in Fig. 6), while 32 pairs of synapses are inhibitory, do not exhibit learning properties, and are implemented using a cascoded n–type CMI. The output currents $I_{\rm inj}$ of all eight synapses connected to a specific neuron are integrated in the corresponding neuron's membrane capacitor ($C_{\rm mem}$ of Fig. 2).

A. Short–Term Depression (STD) Circuit

The STD circuit is used to implement local gain control for stimulus specific adaptation and for nonlinear temporal summation. These characteristics occur also in biological synapses [38], [41] and provide useful computational operators for network processing [42].

The circuit acts on the synaptic weight voltage V_w of Fig. 6: At steady state, V_w settles to the voltage V_{w0}, set by the STDP circuits. During stimulation (applied by a sequence of spikes on the "pre" node) the synaptic weight V_w is gradually reduced at a rate set by the bias voltage $V_{\rm std}$. As a consequence the synapse has a high-pass response: its weight is maximum at the onset of the stimulation, and it gradually decreases throughout the duration of the stimulation. Fig. 7(a) shows spike traces obtained

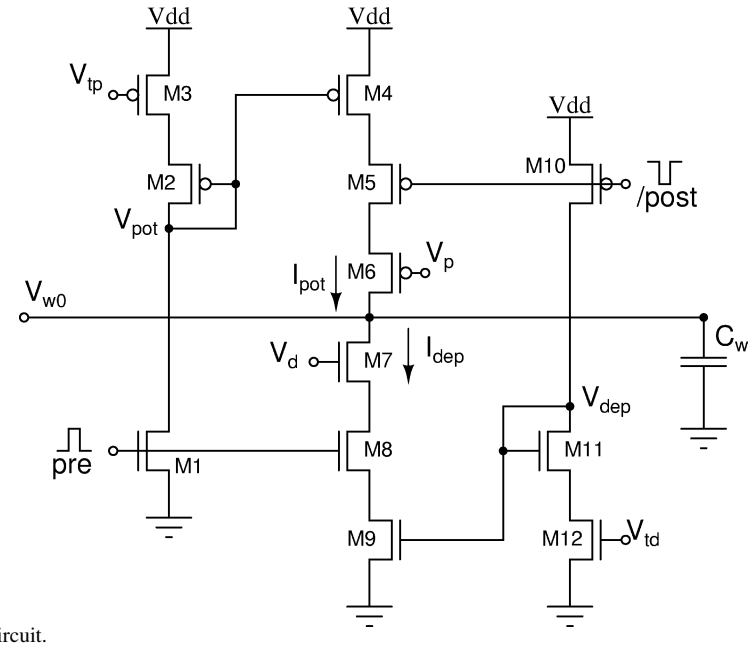


Fig. 8. Synaptic efficacy STDP circuit.

by stimulating an excitatory synapse with a 100-Hz input spike train, for three different values of the short-term depression bias $V_{\rm std}$. As shown, the neuron requires an increasing number of spikes to reach threshold with increasing rates of short-term depression (set by $V_{\rm std}$). The initial change in the slope of the membrane potential traces [around 0.2 s in Fig. 7(a)] is due to the fact that the weight decreases to a low steady-state value. Conversely, the increase in the slope of the membrane potential traces when they are close to the spiking threshold is due to the positive feedback current $I_{\rm fb}$, generated by the neuron [see (3) of Section III-B].

Fig. 7(b) shows the excitatory postsynaptic potential (EPSP) height as a function of the spike count. This data was derived by analyzing the derivative of the traces of Fig. 7(a). The discontinuity in the bottom plot of Fig. 7(b), is due to the fact that the neuron being stimulated produced an output spike upon arrival of the thirteenth input spike. The STD circuit decreases the initial value of the synaptic weight V_{w0} to a steady-state value proportional to the depression rate itself. A detailed analysis of the STD block, with comparison to models of biological depressing synapses is described in [40].

B. STDP Circuits

The circuit required to implement STDP in a network of I&F neurons is shown in Fig. 8. This circuit increases or decreases the analog voltage V_{w0}, depending on the relative timing of the pulses *pre* and */post*. The circuit of Fig. 8 is fully symmetric: upon the arrival of a presynaptic pulse *pre*, a waveform $V_{\rm pot}(t)$ (for potentiating V_{w0}) is generated. Similarly, upon the arrival of a postsynaptic pulse */post*, a complementary waveform $V_{\rm dep}(t)$ (for depotentiating V_{w0}) is generated. Both waveforms have a sharp onset and decay linearly with time, at a rate set, respectively, by $V_{\rm tp}$ and $V_{\rm td}$. The pre- and postsynaptic pulses also switch on two gates (*M*8 and *M*5) that allow the currents $I_{\rm dep}$ and $I_{\rm pot}$ to flow, resulting in a weight increase or decrease. The bias voltages V_p on transistor *M*6 and V_d on *M*7 set an upper bound for the amount of current that can be injected into or removed from the capacitor C_w. If transistors *M*4 – *M*9 operate in the subthreshold regime [29], the analytical expressions for $I_{\rm pot}(t)$ and $I_{\rm dep}(t)$ are

$$I_{\rm pot}(t) = \frac{I_0}{e^{-(\kappa/U_T)V_{\rm pot}(t-t_{\rm pre})} + e^{-(\kappa/U_T)V_p}} \tag{7}$$

$$I_{\rm dep}(t) = \frac{I_0}{e^{-(\kappa/U_T)V_{\rm dep}(t-t_{\rm post})} + e^{-(\kappa/U_T)V_d}} \tag{8}$$

where $t_{\rm pre}$ and $t_{\rm post}$ are the times at which the pre- and postsynaptic spikes are emitted. The change in synaptic efficacy ΔV_{w0} is then

$$\begin{cases} \Delta V_{w0}^{+} = \frac{I_{\rm pot}(t_{\rm post})}{C_p}\Delta t_{\rm spk} & \text{if } t_{\rm pre} < t_{\rm post} \\ \Delta V_{w0}^{-} = -\frac{I_{\rm dep}(t_{\rm pre})}{C_d}\Delta t_{\rm spk} & \text{if } t_{\rm post} < t_{\rm pre} \end{cases} \tag{9}$$

where $\Delta t_{\rm spk}$ is the pre- and postsynaptic spike width, C_p and C_d are the parasitic capacitances of nodes $V_{\rm pot}$ and $V_{\rm dep}$, respectively (not shown in Fig. 8).

Experimental data showing how ΔV_{w0} changes as a function of $\Delta t = t_{\rm pre} - t_{\rm post}$ for different values of $V_{\rm td}$ and $V_{\rm tp}$ are plotted in Fig. 9(a). Similarly, Fig. 9(b) shows plots of ΔV_{w0} versus Δt for three different values of V_p and three different values of V_d. As there are four independent control biases, it is possible to set the maximum amplitude and temporal window of influence independently for positive and negative changes in V_{w0}.

The data of Fig. 9 were obtained from a device implemented in a 1.6-μm CMOS process, using a paired-pulse protocol similar to the one used in physiological experiments [16]: One single pair of pre- and postsynaptic spikes was used to measure each ΔV_{w0} data point, by systematically changing the delay $t_{\rm pre} - t_{\rm post}$ and by separating each stimulation session by a few hundreds of milliseconds (to allow the signals to return to their resting steady-state). Data obtained from the device presented in this paper, showing the characteristics of STDP at the network level, are presented in Section V.

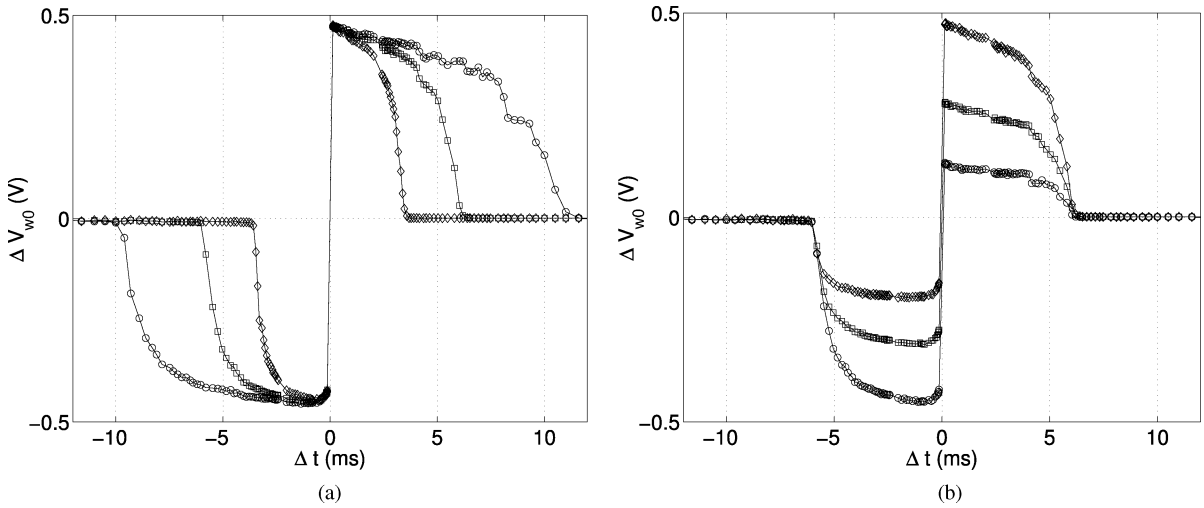


Fig. 9. Changes in synaptic efficacy, as a function of the difference between pre- and postsynaptic spike emission times $\Delta t = t_{\rm pre} - t_{\rm post}$. The curves in the left plot were obtained for six different values of $V_{\rm tp}$, $V_{\rm td}$ (see Fig. 8), while the curves in the right plot were obtained for six different values of V_p and V_d.

C. Bistability Circuit

This circuit, that drives the synaptic weight to one of two possible states on long time scales, was implemented in order to cope with the problem of long term storage of analog values in CMOS technology. Conventional VLSI capacitors are not ideal in that they slowly leak the charge they are supposed to store. Several solutions have been proposed for long term storage of synaptic efficacies in analog VLSI neural networks. One of the first suggestions was to use the same method used for dynamic RAM: to periodically *refresh* the stored value. This involves discretization of the analog value to N discrete levels, a method for comparing the measured voltage to the N levels, and a clocked circuit to periodically refresh the value on the capacitor. An alternative solution is to use analog-to-digital (ADC) converters, an off–chip RAM and digital-to-analog converters (DAC), but this approach requires bulky ADC and DAC circuits, as well as discretization of the values to N states. A more recent suggestion is to use *floating gate* devices [31]. These devices can store very precise analog values for an indefinite amount of time using standard CMOS technology [29], but for spike-based learning rules they would require a control circuit (and, thus, a large area) per synapse. To implement dense arrays of neurons with large numbers of dendritic inputs the synaptic circuits should be as compact as possible.

An approach that uses a very small amount of area per synapse is to use *bistable synapses*. These synapses contain minimum feature-size circuits that locally compare the value of the synaptic efficacy stored on the capacitor with a fixed threshold voltage and slowly drive that value either toward a high analog voltage or toward a low one, depending on the output of the comparator [3]. The assumption that on long time scales synaptic efficacy can only assume two values is not too severe given networks of neurons with large numbers of synapses. It has been argued that the efficacy of biological synapses can indeed be discrete on long time-scales. These assumptions are compatible with experimental data [37] and are supported by experimental evidence [43]. From a theoretical perspective, it has been shown that the performance of associative networks is not necessarily degraded if the dynamic range of the synaptic efficacy is reduced even to the extreme (two stable states), provided that the transitions between stable states are stochastic [44].

The bistability circuit of Fig. 6 generates a constant leak current. In the absence of activity (and, hence, learning) this current will drive the weight toward one of two stable states; if the STDP circuits decrease the synaptic weight V_{w0} below the threshold ($V_{w0} < V_{\rm thr}$), the bistability circuits generate a negative current that actively drives the weight toward the analog value encoding its depressed state $V_{\rm low}$. Conversely, if $V_{w0} > V_{\rm thr}$ the bistability will source a positive current into C_w driving V_{w0} toward $V_{\rm high}$. The signal $V_{\rm thr}$ is a threshold voltage that can be set externally. The bistability circuit drives V_{w0} in two ways, depending on the difference between the value of V_{w0} and the asymptote: if $|V_{w0} - V_a| > 4U_T$ the bistability circuit drives V_{w0} toward V_a linearly, where V_a represents either $V_{\rm low}$ or $V_{\rm high}$, depending on the sign of $(V_{w0} - V_{\rm thr})$

$$\begin{cases} V_{w0}(t) = V_{w0}(0) + \frac{I_{\rm leak}}{C_w} t, & \text{if } V_{w0} > V_{\rm thr} \\ V_{w0}(t) = V_{w0}(0) - \frac{I_{\rm leak}}{C_w} t, & \text{if } V_{w0} < V_{\rm thr} \end{cases} \tag{10}$$

where C_w is the capacitor of Fig. 8 and

$$I_{\rm leak} = I_0 e^{(\kappa V_{\rm leak} - V_{\rm low})/U_T}.$$

As V_{w0} gets close to the asymptote and $|V_{w0} - V_a| < 4U_T$, V_{w0} begins to approach the asymptote exponentially

$$\begin{cases} V_{w0}(t) = V_{\rm high} - V_{w0}(0) e^{-(I_{\rm leak}/C_w U_T)t}, & \text{if } V_{w0} > V_{\rm thr} \\ V_{w0}(t) = V_{\rm low} + V_{w0}(0) e^{-(I_{\rm leak}/C_w U_T)t}, & \text{if } V_{w0} < V_{\rm thr} \end{cases}. \tag{11}$$

Over long time scales, the dynamics of V_{w0} are governed by the bistability circuit, while on short time-scales they are governed by the STDP circuits and the precise timing of pre- and postsynaptic spikes.

When the STDP circuits drive the weight V_{w0} from the low state to a value above $V_{\rm thr}$ and the bistability circuits maintain V_{w0} in a high state, we say that LTP has occurred. Conversely, we say that LTD occurs when the STDP circuits drive the weight

V_{w0} from the high state to a value below $V_{\rm thr}$ and the bistability circuits maintain V_{w0} in a low state.

V. Learning Experiments

Positive and negative updates of the synaptic weight V_{w0} are generated by the STDP circuits in response to both the pre- and postsynaptic activities. The number of these updates affects the probability of crossing the bistability threshold $V_{\rm thr}$, i.e., the LTP and LTD probabilities. Positive weight updates ΔV_{w0}^{+} are triggered by postsynaptic spikes and occur only if at least one presynaptic spike is emitted within a time window of width τ_{+} before the postsynaptic spike. It is important to note that in our circuit implementation only the last presynaptic spike contributes to the update of the weight. Given a postsynaptic Poisson-distributed spike train of mean frequency $\nu_{\rm post}$, the mean number of positive updates ΔV_{w0}^{+} per second is

$$\overline{N_{+}} = P(n_{\rm pre} \geq 1, \tau_{+})\nu_{\rm post} \tag{12}$$

where $P(n_{\rm pre} \geq 1, \tau_{+})$ is the probability of having at least one presynaptic spike in a time window of width τ_{+}. Given a presynaptic Poisson spike train of mean frequency $\nu_{\rm pre}$, $P(n_{\rm pre} \geq 1, \tau_{+})$ is defined as

$$P(n_{\rm pre} \geq 1, \tau_{+}) = 1 - P(n_{\rm pre} = 0, \tau_{+}) = \left(1 - e^{-\nu_{\rm pre}\tau_{+}}\right). \tag{13}$$

Negative weight updates ΔV_{w0}^{-} are triggered by presynaptic spikes and occur only if at least one postsynaptic spike is emitted within a time window of width τ_{-} before the triggering event. As for the positive updates, only the last postsynaptic spike counts for generating ΔV_{w0}^{-}. The mean number of negative updates per second is given by

$$\overline{N_{-}} = P(n_{\rm post} \geq 1, \tau_{-})\nu_{\rm pre} \tag{14}$$

where $P(n_{\rm post} \geq 1, \tau_{-})$ is the probability of having at least one postsynaptic spike in a time window of width τ_{-}

$$P(n_{\rm post} \geq 1, \tau_{-}) = 1 - P(n_{\rm post} = 0, \tau_{-}) = \left(1 - e^{-\nu_{\rm post}\tau_{-}}\right). \tag{15}$$

When the synaptic weight is low, LTP can occur if the number of positive updates $\overline{N_{+}}$ is large enough to overcome the effect of both negative updates $\overline{N_{-}}$ and leak current $-I_{\rm leak}$, thereby driving V_{w0} above the bistability threshold $V_{\rm thr}$. When the weight V_{w0} is high, LTD occurs if $\overline{N_{-}}$ is large enough to overcome the effect of $\overline{N_{+}}$ and $+I_{\rm leak}$, thus driving V_{w0} below the bistability threshold.

In spite of a symmetric weight change mechanism for a single pair of pre- and postsynaptic spikes (as shown in Fig. 9), there is an inherent asymmetry in our STDP circuits when multiple spikes are involved. This asymmetry tends to favor LTP if the presynaptic firing rate is lower than the postsynaptic one, and LTD if the presynaptic firing rate dominates. Let us consider the first case $\nu_{\rm pre} < \nu_{\rm post}$, assuming that pre- and postsynaptic spike trains are uncorrelated. For a single presynaptic event several postsynaptic spikes are likely to occur in the LTP and LTD time windows with the same probability. While multiple postsynaptic spikes in the LTP time window produce multiple upward weight updates, only the last of the postsynaptic spikes in the LTD time window produces a downward weight update, therefore biasing the learning dynamics toward LTP. The same reasoning can be applied for presynaptic rates higher than the postsynaptic ones: in this case the learning dynamics will be biased toward LTD. Furthermore, for low values of $\nu_{\rm pre}$ and $\nu_{\rm post}$, irrespective of $\nu_{\rm pre} \gtrless \nu_{\rm post}$, the probabilities of LTP and LTD tend to zero as $P(n_{\rm pre} \geq 1, \tau_{+})$ and $P(n_{\rm post} \geq 1, \tau_{-})$ become negligible [see (13) and (15)].

To characterize the learning properties of the VLSI synapses experimentally, we measured the probabilities of potentiating the synaptic efficacies (LTP) or depressing them (LTD) as a function of mean pre- and postsynaptic firing rates. We stimulated each synapse on the chip with Poisson-distributed spike trains via the PCI–AER board, and generated postsynaptic firing rates by injecting constant currents into the neurons. To measure the probability for LTP of a synapse we first reset its weight to its low asymptotic value ($V_{\rm low}$ of Fig. 6). We then applied pre- and postsynaptic stimulation for 2.5 s. We subsequently determined the state of the synapse by clamping the weight to its learned asymptotic value (i.e., by setting $V_{\rm leak}$ of Fig. 6 to 1 V), and by measuring the response of the postsynaptic neuron to a regular presynaptic spike train. We repeated this procedure 50 times and averaged the data across trials. To measure the probability for LTD of a synapse we applied a similar experimental protocol, but first initializing the synapse's state to its high value $V_{\rm high}$.

Fig. 10 shows the mean probabilities of LTP and LTD measured from the chip as a function of mean pre- and postsynaptic firing rates. The particular shape and the position of the region where LTP/LTD occurs can be modified by varying the parameters of the bistability and the STDP circuits. For these experiments we biased the synaptic circuits to produce an asymmetric weight update curve, with a large ΔV_{w0}^{+} and a short τ_{+}, and a small ΔV_{w0}^{-} and a long τ_{-}. As expected, for low values of mean postsynaptic firing rates $\nu_{\rm post}$ LTP does not occur [see Fig. 10(a)], while for high and increasing values of $\nu_{\rm post}$ the probability of LTP varies with a bell-shape dependence on the mean presynaptic firing rates $\nu_{\rm pre}$. The measured probability of LTD shown in Fig. 10(b) is also in accordance with our theoretical predictions.

The data of Fig. 10 were averaged over all synapses of all neurons in the array. The LTP and LTD probability distributions of single synapses are qualitativey similar to the curves of Fig. 10 and do not deviate significantly from the mean.

VI. Conclusion

We presented a VLSI array of low-power, adaptive I&F neurons with bistable, plastic, and adaptive synapses that use the Address–Event Representation to receive and transmit spikes. We showed that the low power neurons respond to constant currents in a consistent and reliable way throughout the array. Using a PCI–AER board we stimulated the plastic synapses of the array with address–events and demonstrated their learning properties. The weight of any synapse in the array can be changed by setting the pre- and postsynaptic mean firing rates to appropriate values. This property allows us to implement learning mechanisms useful for real–time unsupervised learning tasks,

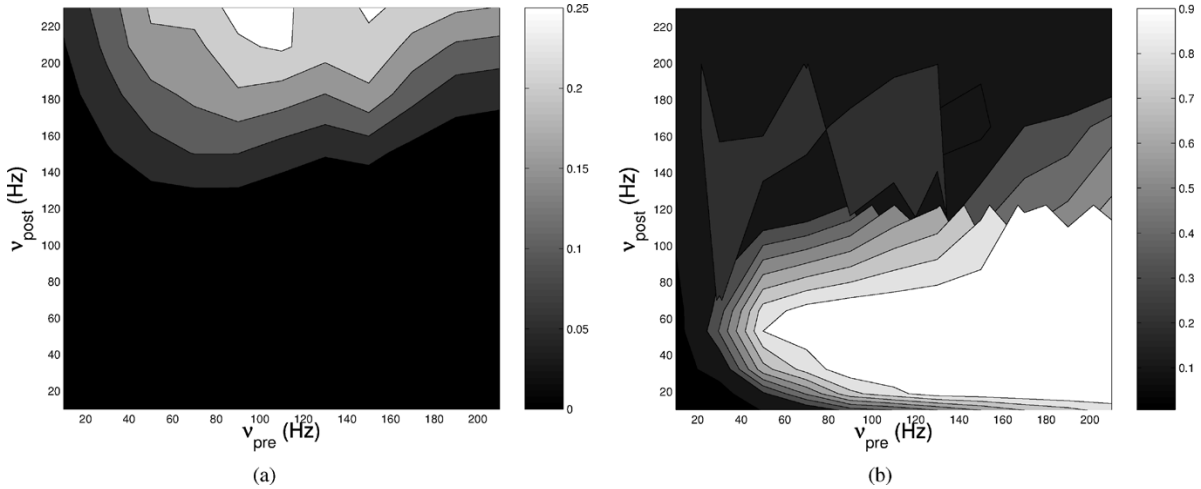


Fig. 10. (a) Mean probability of LTP over all STDP synapses in the array, as a function of pre- and postsynaptic firing rates. (b) Mean probability of LTD. The relevant circuit bias parameters used for this set of data are: $V_p = 3.9$ V, $V_d = 0.65$ V, $V_{\rm tp} = 4.36$ V, and $V_{\rm td} = 0.33$ V (see Fig. 8).

or to arbitrarily set (bistable) synaptic weights in a supervised way, without requiring dedicated wires for each synapse. The STD subcircuits in the synapses can be activated during or after learning to implement local gain-control mechanisms and introduce an additional degree of adaptation.

The chip proposed was fabricated using a standard 0.8-μm CMOS process, and implemented a network with 32 neurons and 256 synapses in an area of 1.6 mm^2. We are currently designing new chips using a more advanced 0.35-μm technology. These chips implement networks with 32 neurons and 8000 synapses using less than 10 mm^2 of silicon real-estate. The circuits proposed are to a large extent technology independent and operate fully in parallel. In principle networks of this type can scale up to any arbitrary size. In practice the network size is limited by the maximum silicon area and AER bandwidth available. Given the current speed and specifications of the AER interfacing circuits [45], and the availability of silicon VLSI technology, there is room for increasing network size by at least two orders of magnitude.

Our results indicate that the circuits proposed can be used in massively parallel VLSI networks of I&F neurons for real–time simulation of complex spike–based learning algorithms. Furthermore these types of devices, when interfaced to neuromorphic AER sensors such as silicon retinas [27], [46], [47] or silicon cochleas [48], are ideal for constructing compact VLSI sensory systems with adaptation and learning capabilities.

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REFERENCES

[1] R. J. Vogelstein, U. Mallik, and G. Cauwenberghs, "Silicon spike-based synaptic array and address-event transceiver," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2004, pp. 385–388.

[2] F. Tenore, R. Etienne-Cummings, and M. Lewis, "A programmable array of silicon neurons for the control of legged locomotion," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2004, pp. 349–352.

[3] E. Chicca, D. Badoni, V. Dante, M. D'Andreagiovanni, G. Salina, S. Fusi, and P. Del Giudice, "A VLSI recurrent network of integrate–and–fire neurons connected by plastic synapses with long term memory," *IEEE Trans. Neural Netw.*, vol. 14, no. 5, pp. 1297–1307, Sep. 2003.

[4] S. Fusi, M. Annunziato, D. Badoni, A. Salamon, and D. Amit, "Spike-driven synaptic plasticity: Theory, simulation, VLSI implementation," *Neural Comput.*, vol. 12, pp. 2227–2258, 2000.

[5] P. Merolla and K. Boahen, "A recurrent model of orientation maps with simple and complex cells," in *Advances in Neural Information Processing Systems*. Cambridge, MA: MIT Press, 2004, vol. 16, pp. 995–1002.

[6] S.-C. Liu and R. Douglas, "Temporal coding in a silicon network of integrate-and-fire neurons," *IEEE Trans. Neural Netw.*, vol. 15, no. 5, pp. 1305–1314, Sep. 2004.

[7] A. Bofill-i Petit and A. F. Murray, "Synchrony detection and amplification by silicon neurons with STDP synapses," *IEEE Trans. Neural Netw.*, vol. 15, no. 5, pp. 1296–1304, Sep. 2004.

[8] T. Y. W. Choi, B. E. Shi, and K. Boahen, "An on-off orientation selective address event representation image transceiver chip," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 2, pp. 342–353, Feb. 2004.

[9] G. Indiveri, "A neuromorphic VLSI device for implementing 2-D selective attention systems," *IEEE Trans. Neural Netw.*, vol. 12, no. 5, pp. 1455–1463, Nov. 2001.

[10] J. Lazzaro, J. Wawrzynek, M. Mahowald, M. Sivilotti, and D. Gillespie, "Silicon auditory processors as computer peripherals," *IEEE Trans. Neural Netw.*, vol. 4, no. 3, pp. 523–528, May 1993.

[11] M. Mahowald, *An Analog VLSI System for Stereoscopic Vision*. Boston, MA: Kluwer, 1994.

[12] K. Boahen, "Communicating neuronal ensembles between neuromorphic chips," in *Neuromorphic Systems Engineering*, T. S. Lande, Ed. Norwell, MA: Kluwer, 1998, pp. 229–259.

[13] S. R. Deiss, R. J. Douglas, and A. M. Whatley, "A pulse-coded communications infrastructure for neuromorphic systems," in *Pulsed Neural Networks*, W. Maass and C. M. Bishop, Eds. Cambridge, MA: MIT Press, 1998, ch. 6, pp. 157–178.

[14] G. Indiveri, "Neuromorphic bistable VLSI synapses with spike-timing-dependent plasticity," in *Advances in Neural Information Processing Systems*. Cambridge, MA: MIT Press, 2002, vol. 15, pp. 1091–1098.

[15] P. Häfliger, M. Mahowald, and L. Watts, "A spike based learning neuron in analog VLSI," in *Advances in Neuralinformation Processing Systems*, M. C. Mozer, M. I. Jordan, and T. Petsche, Eds. Cambridge, MA: MIT Press, 1997, vol. 9, pp. 692–698.

[16] H. Markram, J. Lübke, M. Frotscher, and B. Sakmann, "Regulation of synaptic efficacy by coincidence of postsynaptic AP's and EPSPs," *Science*, vol. 275, pp. 213–215, 1997.
[17] G.-Q. Bi and M.-M. Poo, "Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type," *J. Neurosci.*, vol. 18, no. 24, pp. 10 464–10 472, 1998.
[18] L. F. Abbott and S. Song, "Asymmetric Hebbian learning, spike timing and neural response variability," *Adv. Neural Inf. Process. Syst.*, vol. 11, pp. 69–75, 1999.
[19] R. Kempter, W. Gerstner, and J. L. van Hemmen, "Hebbian learning and spiking neurons," *Phys. Rev. E*, vol. 59, no. 4, pp. 4498–4514.
[20] M. C. W. van Rossum, G.-Q. Bi, and G. G. Turrigiano, "Stable Hebbian learning from spike timing-dependent plasticity," *J. Neurosci.*, vol. 20, no. 23, pp. 8812–8821, 2000.
[21] W. Senn, "Beyond spike timing: The role of nonlinear plasticity and unreliable synapses," *Biol. Cybern.*, vol. 87, pp. 344–355, 2002.
[22] V. Dante, P. Del Giudice, and A. M. Whatley, "PCI-AER hardware and software for interfacing to address-event based neuromorphic systems," *Neuromorph. Eng. Newslett.*, vol. 2, no. 1, pp. 5–6, 2005.
[23] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison-Wesley, 1989.
[24] E. M. Izhikevich, "Which model to use for cortical spiking neurons?," *IEEE Trans. Neural Netw.*, vol. 15, no. 5, pp. 1063–1070, Sep. 2004.
[25] S. R. Schultz and M. A. Jabri, "Analogue VLSI 'integrate-and-fire' neuron with frequency adaptation," *Electron. Lett.*, vol. 31, no. 16, pp. 1357–1358, Aug. 1995.
[26] A. van Schaik, "Building blocks for electronic spiking neural networks," *Neural Netw.*, vol. 14, no. 6–7, pp. 617–628, Jul.–Sep. 2001.
[27] E. Culurciello, R. Etienne-Cummings, and K. Boahen, "Arbitrated address-event representation digital image sensor," *Electron. Lett.*, vol. 37, no. 24, pp. 1443–1445, Nov. 2001.
[28] B. W. Connors, M. J. Gutnick, and D. A. Prince, "Electrophysiological properties of neocortical neurons in vitro," *J. Neurophysiol.*, no. 48, pp. 1302–1320, 1982.
[29] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbrück, and R. Douglas, *Analog VLSI:Circuits and Principles*. Cambridge, MA: MIT Press, 2002.
[30] D. D. Ben Dayan Rubin, E. Chicca, and G. Indiveri, "Characterizing the firing proprieties of an adaptive analog VLSI neuron," in *Proc. BioADIT*, vol. 3141/2004, LCNS, M. M. Auke Jan Ijspeert and N. Wakamiya, Eds., Lausanne, Switzerland, Jan. 29–30, 2004, pp. 189–200.
[31] C. Diorio, P. Hasler, B. Minch, and C. Mead, "A single-transistor silicon synapse," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1972–1980, Aug. 1996.
[32] G. Indiveri, R. Mürer, and J. Kramer, "Active vision using an analog VLSI model of selective attention," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 48, no. 5, pp. 492–500, May 2001.
[33] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbruck, T. Burg, and R. Douglas, "Orientation-selective aVLSI spiking neurons," *Neural Netw.*, vol. 14, no. 6/7, pp. 629–643, 2001.
[34] E. Chicca, G. Indiveri, and R. Douglas, "An adaptive silicon synapse," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2003, pp. I–81–I–84.
[35] W. Maass and E. D. Sontag, "Neural systems as nonlinear filters," *Neural Comput.*, vol. 12, no. 8, pp. 1743–72, 2000.
[36] R. S. Zucker and W. G. Regehr, "Short-term synaptic plasticity," *Annu. Rev. Physiol.*, vol. 64, pp. 355–405, 2002.
[37] T. V. P. Bliss and G. L. Collingridge, "A synaptic model of memory: Long term potentiation in the hippocampus," *Nature*, vol. 31, p. 361, 1993.
[38] A. M. Zador and L. E. Dobrunz, "Dynamic synapses in cortex," *Neuron*, vol. 19, pp. 1–4, 1997.
[39] C. Rasche and R. Hahnloser, "Silicon synaptic depression," *Biol. Cybern.*, vol. 84, no. 1, pp. 57–62, 2001.
[40] M. Boegerhausen, P. Suter, and S.-C. Liu, "Modeling short-term synaptic depression in silicon," *Neural Comput.*, vol. 15, no. 2, pp. 331–348, Feb. 2003.
[41] F. S. Chance, S. B. Nelson, and L. F. Abbott, "Synaptic depression and the temporal response characteristics of v1 cells," *J. Neurosci.*, vol. 18, no. 12, pp. 4785–99, 1998.
[42] L. Abbott, K. Sen, J. Varela, and S. Nelson, "Synaptic depression and cortical gain control," *Science*, vol. 275, no. 5297, pp. 220–223, 1997.
[43] C. C. H. Petersen, R. C. Malenka, R. A. Nicoll, and J. J. Hopfield, "All-or-none potentiation at CA3-CA1 synapses," *Proc. Nat. Acad. Sci.*, vol. 95, p. 4732, 1998.
[44] D. J. Amit and S. Fusi, "Dynamic learning in neural networks with material synapses," *Neural Comput.*, vol. 6, p. 957, 1994.
[45] K. Boahen, "A burst-mode word-serial address-event link III: Analysis and test results," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 7, pp. 1292–1300, Jul. 2004.
[46] P. Lichtsteiner, T. Delbruck, and J. Kramer, "Improved ON/OFF temporaly differentiating address-event imager," in *Proc. 11th IEEE Int. Conf. Electronics, Circuits, and Systems*, Dec. 2004, pp. 211–214.
[47] J. Kramer, "An integrated optical transient sensor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 49, no. 9, pp. 612–628, Sep. 2002.
[48] A. van Schaik and S. Liu, "AER EAR: A matched silicon cochlea pair with address event representation interface," in *Proc. 2005 IEEE Int. Symp. Circuits and Systems*, Kobe, Japan, May 2005, pp. 4213–4216.

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