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Ionic/Electronic Hybrid Materials Integrated in a Synaptic Transistor with Signal Processing and Learning Functions

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Signal processing, memory, and learning functions are established in the human brain by modifying ionic fluxes in neurons and synapses.[1,2] Through a synapse, a potential spike signal in a presynaptic neuron can trigger an ionic excitatory postsynaptic current (EPSC) or inhibitory postsynaptic current (IPSC) that temporally lasts for ~1–10^4 ms in a postsynaptic neuron.[2] This enables the postsynaptic neuron to collectively process the EPSC or IPSC through 10^3–10^4 synapses to establish spatial and temporal correlated functions.[3,4] The synaptic transmission efficacy can be modified by temporally correlated pre- and post-synaptic spikes via spike-timing-dependent plasticity (STDP).[2,5–9] For example, if a postsynaptic spike is triggered momentarily after a presynaptic spike by a few milliseconds, the synaptic efficacy will be increased, resulting in long-term potentiation (LTP), but if the temporal order is reversed, the synaptic efficacy will be decreased, resulting in long-term depression (LTD). The synaptic efficacy can also be modified with reversed polarities in STDP in different types of synapses.[7] STDP is essential to modify synapses in a neural network for learning and memory functions of the brain.[3,10–14]

Electronic materials, devices, and circuits have been explored extensively to emulate synapses,[15–21] but to date they have not been able to match the synaptic functions in the brain. Synaptic transistors with nonvolatile analog memory were fabricated by integrating a charge-storage[15] or ferroelectric[16] materials onto the gate structure of Si metal-oxide-semiconductor (MOS) transistors, but these devices cannot emulate the essential synaptic dynamic functions such as EPSC/IPSC or STDP. Electronic neuromorphic circuits have been designed and fabricated to supply EPSC/IPSC and STDP,[17–21] but these nonlinear dynamic analog circuits require many transistors and several capacitors to emulate a single synapse. The large capacitor size, complex architecture, and energy consumption of these synaptic circuits limited the number of synapses that could be integrated onto a single chip to about 10^2–10^5. The lack of a small, cheap device with the essential synaptic dynamic properties for signal processing, learning, and memory prohibits the circuits from approaching the scale and functions of the human brain that contains ~10^{14} synapses.

We have designed and fabricated a synaptic transistor based on ionic/electronic hybrid materials by integrating a layer of ionic conductor and a layer of ion-doped conjugated polymer, onto the gate of a Si-based transistor. In analogy to the synapse, a potential spike can trigger ionic fluxes with a temporal lapse of a few milliseconds in the polymer, which in turn spontaneously generates EPSC in the Si layer. Temporally correlated pre- and post-synaptic spikes can modify ions stored in the polymer, resulting in a nonvolatile strengthening or weakening of the device transmission efficacy with STDP. A single hybrid transistor can replace presently utilized complex and energy-consuming electronic circuits to emulate the synapse for spike signal processing, learning, and memory, which could provide a new pathway to construct neuromorphic circuits approaching the scale and functions of the brain.

The synaptic transistor has a Si n-p-n source-channel-drain structure of a conventional MOS transistor, with the Si channel covered by a 3-nm-thick SiO_2 insulating layer (Fig. 1a). A 70-nm-thick conjugated polymer layer of poly[2-methoxy-5-(2′-ethylhexyloxy)-p-phenylene vinylene] (MEH-PPV) and a 70-nm-thick ionic conductive layer of $RbAg_4I_5$ were sandwiched between the gate SiO_2 insulator and an Al/Ti electrode. To emulate synaptic functions, presynaptic spikes were applied to the transistor gate, and postsynaptic currents, I^{ps}, were measured from the source. Postsynaptic spikes were also applied to the source. A spike was composed of a 1 ms-wide positive voltage pulse with an amplitude $V^+ = 3$–5 V immediately followed by a 1 ms-wide negative voltage pulse with an amplitude $V^- = -3$ to -5 V (Fig. 1a, Inset). After the spike, the transistor was operated at its rest state under a subthreshold condition by setting the gate voltage $V_g = 0$ V. A drain voltage $V_d = 0.1$ V was applied continuously.

When a presynaptic spike with amplitudes of $V^+/V^- = 4\,\text{V}/-5\,\text{V}$ was applied to the transistor gate, the typical I^{ps} is

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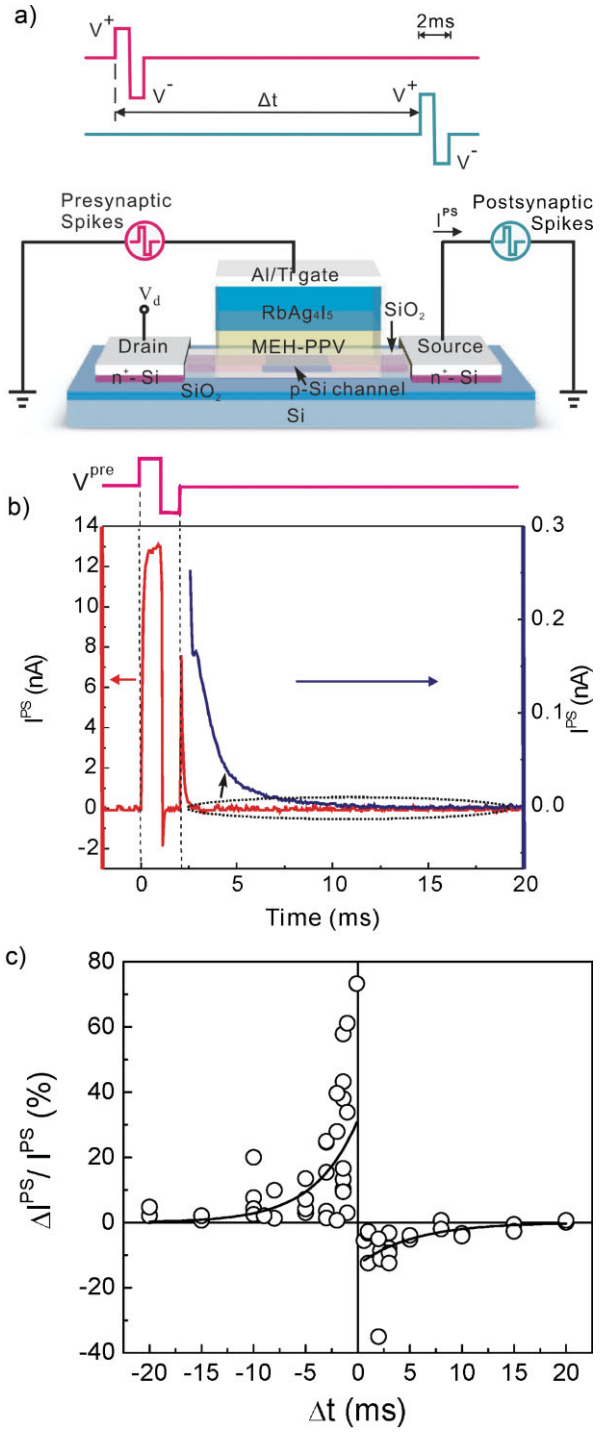

Figure 1. a) A schematic diagram showing the structure of a synaptic transistor. A pre- and postsynaptic spike pair applied on the transistor gate and source electrodes, respectively, with a time interval, Δt, is shown in the inset. b) The postsynaptic current, I^{PS}, monitored through the source current, is shown in red as a function of time when a presynaptic spike was applied to the transistor gate. The low postsynaptic current after the spike, or EPSC, is magnified and shown in blue line with its unit labeled on the right axis. c) 120 pairs of temporally correlated pre- and postsynaptic spikes were applied, and the relative changes of the postsynaptic currents, $\Delta I^{PS}/I^{PS}$, measured after spike pairing modifications are shown as a function of Δt. The solid lines are the fitting curves for the experimental data.

shown as a function of time in Figure 1b. The postsynaptic current was turned on during the positive pulse of the spike, and turned off during the negative pulse of the spike. After the spike, an EPSC was triggered, which gradually decayed back to a static equilibrium value within ~15 ms. The temporal profile of the EPSC is comparable with those observed in biological synapses.[2,5–8] The average energy consumption for such a synaptic transistor is ~10 pJ per spike operation, and after the spike the power consumption in the rest state is ~0.1 pW.

The learning function of the synaptic transistor was demonstrated by following a typical spike pairing protocol used in biological synaptic studies.[2,5–8] A pair of temporally correlated pre- and postsynaptic spikes with with amplitudes $V^+/V^- = 4\,V/-5\,V$ and $V^+/V^- = 5\,V/-4\,V$ was applied to the gate and source of the transistor, respectively, with a time interval Δt between their onsets (Fig. 1a). The spike pair was applied at a frequency of 1 Hz for 2 min (120 repetitions). The postsynaptic currents were measured before and 30 minutes after the spike pair applications, and the relative changes of the postsynaptic currents, $\Delta I^{ps}/I^{ps}$, which represents the long-term nonvolatile modification of the synaptic efficacy, are shown in Figure 1c as a function of the time interval Δt. STDP was observed in the synaptic transistor: when the presynaptic spikes were applied before the postsynaptic spikes ($\Delta t > 0$), the postsynaptic current decreased, resulting in LTD; when the presynaptic spikes were applied after the postsynaptic spikes ($\Delta t < 0$), the postsynaptic current increased, resulting in LTP. The experimental data measured within the temporal windows for LTP and LTD can each be fitted with an exponential function $\Delta I^{ps}/I^{ps} = A\,e^{-\Delta t/\tau}$, with the result that $A^+ = 31.5\%$ and $\tau^+ = -4.16$ ms for LTP, and $A^- = -13.0\%$ and $\tau^- = 5.36$ ms for LTD. The A and τ values are comparable with those observed in biological synapses.[2,5–8] The postsynaptic currents were also modified reversibly by applying spike pairs with alternative positive/negative Δt (Supporting Information). The STDP data points shown in Figure 1c have a significant statistical scatter, which has also been observed in biological synapses. After the transistor was modified to a specific efficacy, further tests showed that the device remained essentially unchanged for more than ten days (Supporting Information).

To understand the properties of the ionic/electronic hybrid materials and the operation mechanism of the synaptic transistor, a gate capacitor (Fig. 2a) with the same structure of the transistor gate was fabricated and studied. Pulses with different amplitudes and polarities were applied to the gate capacitor, and the changes of the charge stored in the devices, ΔQ, were derived by integrating the current measured from the device with respect to the time. As shown in Figure 2b, the device was charged by the pulses; after the pulse ended, ΔQ gradually decayed to a non-zero stable value within ~5–20 ms. In other words, the positive (negative) pulses induced a nonvolatile increase of positive (negative) charge stored in the device. The amount of nonvolatile charge stored in the device and the post-pulse discharge time increased with increasing pulse magnitudes. A control capacitor with an identical structure as the gate capacitor was fabricated, except the polymer layer was removed in the control capacitor (Supporting Information). When a pulse was applied on the control capacitor, the device was charged; after the pulse ended, the charge in the device decayed to zero within 3 ms. From the

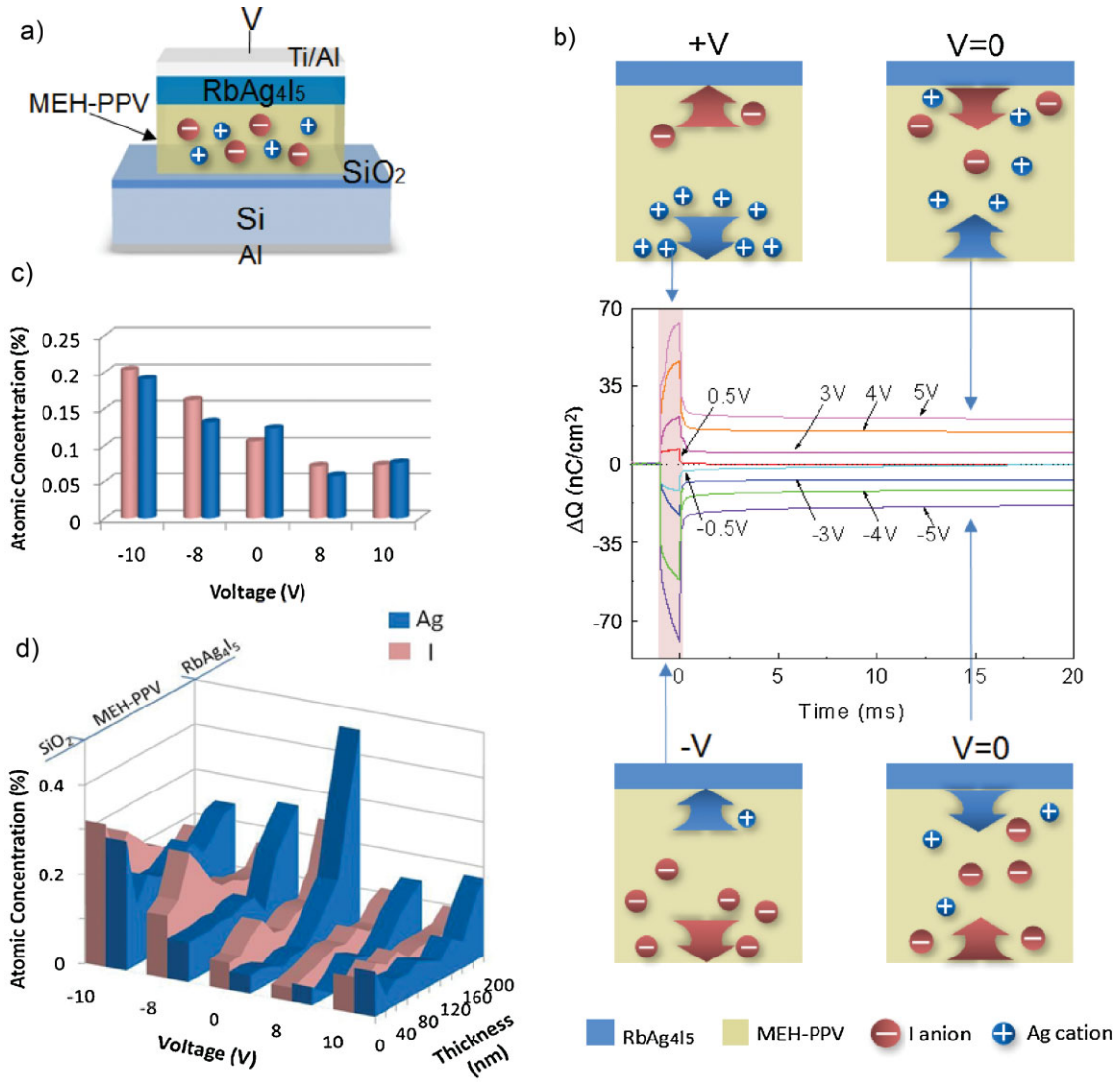

Figure 2. a) The schematic diagram showing the structure of a gate capacitor. b) The change of the average area densities of charges stored in a gate capacitor, ΔQ, versus time when 1 ms-wide voltages pulses with different amplitudes and polarities were applied. The schematics showing the modulation of ionic concentrations in the polymer layer in the gate capacitor when a positive or negative voltage bias was applied to the device, and after the positive or negative voltage bias was removed. c) Average concentrations and d) chemical depth profiles of Ag (blue) and I (magenta) atoms in the MEH-PPV layer of gate capacitors that experienced ±10 V, ±8 V, and 0 V (control) voltage biases.

comparison of the gate and control capacitors, the slow discharge process and the nonvolatile charge that remained in the gate capacitor are likely related to ionic charges in the polymer. The ionic mobility in the polymer is significantly lower than the electronic mobility, and thus the observed ionic discharge process in the polymer took ~5–20 ms, which is comparable with the temporal scale of post-spike ionic fluxes observed in biological synapses.[2,5–8]

The ionic modulation in the polymer layer of the gate capacitor was further investigated by X-ray photoelectron spectroscopy (XPS). The thickness of the MEH-PPV layer in the gate capacitors for the XPS experiments was increased to 200 nm in order to improve the resolution of the XPS chemical depth profile, and the voltage biases applied to the devices were also increased accordingly. The XPS results indicate that only I and Ag concentrations in the polymer layers were modified significantly by the voltage biases; no perceptible modifications of the other elements have been observed. As shown in Figure 2c, negative (positive) biases induced an increase (decrease) of the I concentrations in the polymer. Surprisingly, the negative biases also induced an increase of the average Ag concentrations in the polymer, but the positive biases did not induce any obvious increase of the average Ag concentrations in the polymer.

The ionic modulation likely resulted from the different characteristics of the Ag cations and I anions in the polymer. Ag cations have a high mobility and concentration in the $RbAg_4I_5$ ionic conductor.[22] I anions have a much larger radius than Ag cations and can form a large I_3^- ionic complex and chemically bond with the MEH-PPV polymer.[23,24] Therefore, the I anions

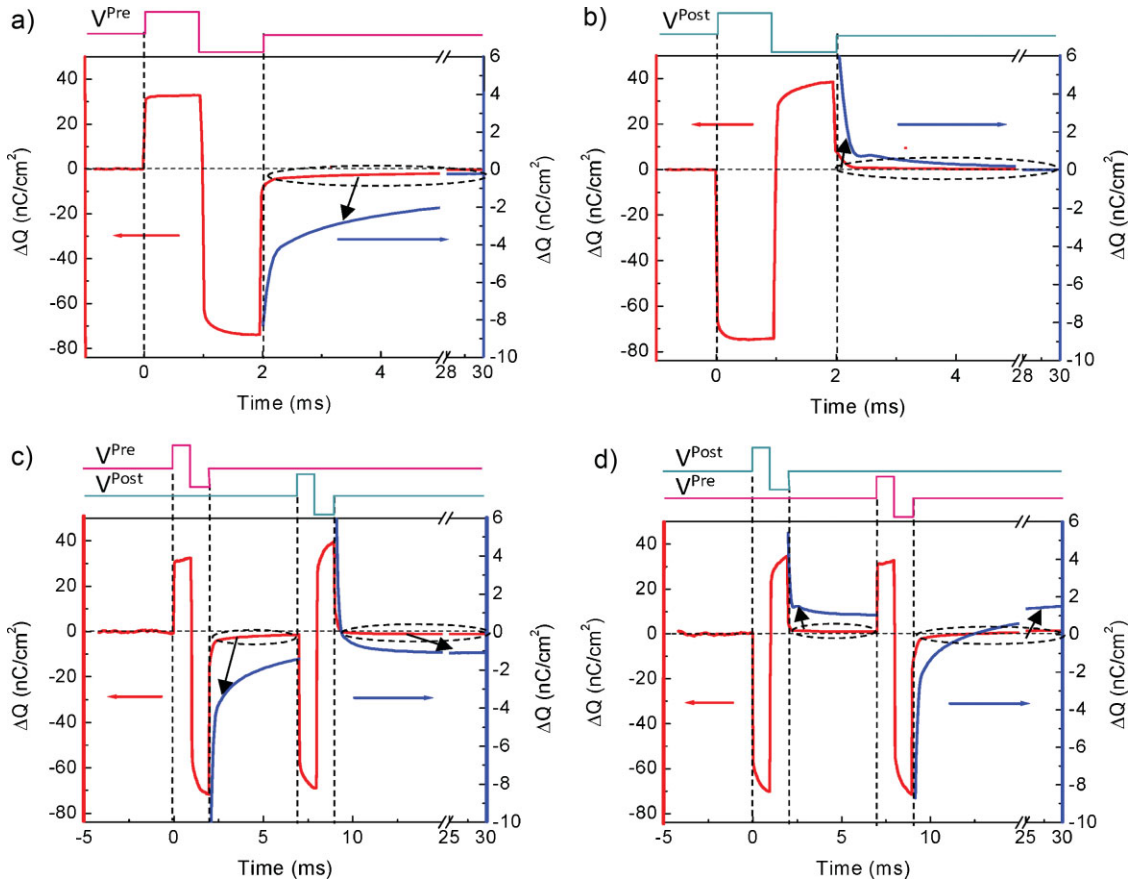

Figure 3. The change of average area densities of charges, ΔQ, in a gate capacitor versus time: a) A presynaptic spike was applied on the Al/Ti gate electrode. b) A postsynaptic spike was applied on the Si layer. c) The first presynaptic spike and the second postsynaptic spike were applied with a time interval of 7 ms ($\Delta t = 7$ ms). d) The first postsynaptic spike and the second presynaptic spike were applied with a time interval of 7 ms ($\Delta t = -7$ ms). The post-spike decays of ΔQ are magnified and shown as blue lines with their units labeled on the right axes.

have significantly lower mobility than the Ag cations in the polymer, and remain immobile when the electric field is below a threshold value. When a negative voltage bias was applied to the device, the Ag cations were driven from the polymer toward the $RbAg_4I_5$, and the I anions were driven from the $RbAg_4I_5$ into the polymer, resulting in the accumulation of the I anions near the MEH-PPV/SiO_2 interface (as shown experimentally in Fig. 2d and schematically in the inset of Fig. 2b). After the voltage bias was removed, some Ag cations drifted back into the polymer, attracted by the relatively immobile I anions, and therefore both I and Ag concentrations in the polymer were increased after the negative voltage bias. The ionic fluxes gradually reduced the internal electric field in the polymer, and when the internal electric field was reduced below a threshold value, the I anions would stop drifting in the polymer due to the bonding between the I anions and the polymer matrix. The excess I anions in the polymer induced the nonvolatile increase of the negative charge in the device. When a positive voltage bias was applied to the device, the Ag cations were driven into the polymer, and the I anions were driven out from the polymer. After the voltage bias was removed, the mobile Ag cations could diffuse back to their quasi-equilibrium profile in the polymer skewed toward the $RbAg_4I_5$ (Fig. 2d), and therefore no significant increase of the Ag cationic concentrations was observed by XPS in the polymer after a positive bias. The deficiency of I anions resulted in the nonvolatile decrease of the negative charge in the device.

When a spike composed of a pair of positive and negative pulses was applied to a gate capacitor, the pulses in the spike each could induce nonvolatile modulations of the ionic charges in the polymer. However, by the proper choice of the amplitudes of the pulses in the spike, the net change of the ionic charge was adjusted to make the sum of the charge changes during the positive pulse (ΔQ^+), negative pulse (ΔQ^-), and post-spike (ΔQ^P) stages to be equal to zero ($\Delta Q = \Delta Q^+ + \Delta Q^- + \Delta Q^P = 0$). Under this condition, as shown in Figure 3a and b, a presynaptic spike with amplitudes $V^+/V^- = 4\,V/-3\,V$ or a post-synaptic spike with amplitudes $V^+/V^- = 3\,V/-4\,V$ induced the transient modification of ionic charge and the post-spike ionic discharge in the polymer, but after the spike the device returned to the same ionic charge as that before the spike ($\Delta Q = 0$). A presynaptic spike applied on the gate has an equivalent effect on the modification of ionic charges in the polymer as a postsynaptic spike applied on the source with reversed amplitudes. The ionic discharge triggered by the presynaptic spike was mirrored by the counter electronic

discharge in the p-Si layer of the synaptic transistor, inducing EPSC (Supporting Information).

A pair of temporally correlated spikes can induce a nonvolatile change of ionic charge in the polymer and STDP. Figure 3c shows that when the first presynaptic spike with amplitudes $V^+/V^- = 4\,V/-3\,V$ and the second postsynaptic spike with amplitudes $V^+/V^- = 3\,V/-4\,V$ were applied to the gate capacitor with a time interval of 7 ms, a nonvolatile increase of negative charge ($\Delta Q < 0$) was observed after the device reached its static state. Since the pulse amplitudes in the spikes were balanced, the second spike alone would not induce the nonvolatile charge change ($\Delta Q_2 = 0$). However, the second spike was applied before the negative charge induced by the first spike decayed to zero, which interrupted the charge balance and resulted in excess negative ionic charge in the polymer ($\Delta Q_1 < 0$). The spike pair cooperatively induced a nonvolatile increase of the negative ionic charge in the polymer ($\Delta Q_1 + \Delta Q_2 < 0$), and led to a corresponding increase of positively charged holes in the p-type Si channel and the decrease of the source-drain current in the transistor; thus, the correlated pair of spikes induced LTD in the transistor. The ionic discharge triggered by the first spike decreased with time (Fig. 1b), therefore when the time interval (Δt) between the two spikes was shortened, more nonvolatile negative ionic charge was preserved in the polymer; and consequently the larger LTD (Fig. 1c). When a pair of the same spikes with reversed temporal sequence was applied (Fig. 3d), the first postsynaptic spike induced the post-spike decay of the positive ionic charge in the polymer, and the second presynaptic spike interrupted the positive ionic discharge, resulting in the increase of the nonvolatile positive charge in the polymer ($\Delta Q_1 + \Delta Q_2 > 0$) and LTP in the transistor. The decrease of the time interval (Δt) between the two spikes resulted in the increase of nonvolatile positive ionic charge in the polymer and the larger LTP.

In summary, we integrated an $RbAg_4I_5$ ionic conductor layer and an ion-doped MEH-PPV conjugated polymer layer onto the gate structure of a Si-based MOS transistor to emulate the dynamic modulation of ionic fluxes in the synapses. A potential spike applied on the gate of the synaptic transistor induces ionic discharge flux in the MEH-PPV polymer, triggering EPSC in the source of the synaptic transistor for signal processing. A pair of temporally correlated pre- and post-synaptic spikes can modify the nonvolatile ionic charges in the polymer, inducing STDP for learning and memory. The dynamic temporal lapse for EPSC is 5–15 ms, and the temporal modification window for STDP is 5–20 ms, which are comparable with the corresponding temporal parameters observed in biological synapses.[9,12] The temporal characteristics of the transistor are influenced by the ionic mobility in the polymer, and can be adjusted to desired values by integrating appropriate ions and polymers in the transistor gate. Different types of synaptic transistors that generate IPSC and/or STDP with opposite polarities (i.e., $\Delta t > 0 \rightarrow$ LTP; $\Delta t < 0 \rightarrow$ LTD) can be achieved by replacing the p-type Si channel with an n-type one in the transistor, or changing the ion-dopants in the polymer. The average energy consumed by the transistor per spike is $\approx$10 pJ, and the average power for operating a transistor at rest state is $<$0.1 pW. In principle, the synaptic transistors can be miniaturized to the nanoscale[25] to further lower its energy consumption, and readily integrated in large-scale Si MOS circuits for the emulations of brain functions.

Experimental

The synaptic transistors were fabricated on a silicon-on-insulator (SOI) wafer. The p-type Si channel was doped with a boron concentration of $3 \times 10^{17}\,cm^{-3}$, and has a width of 1–5 μm, a thickness of 50 nm, and a length of 10 μm. The n-Si source and drain were doped with a phosphorous concentration of $1 \times 10^{20}\,cm^{-3}$. A 3-nm-thick SiO_2 insulating layer was prepared by thermal oxidation to cover the Si channel. A 70-nm-thick MEH-PPV polymer layer was spin-coated on the SiO_2 layer. A 70-nm-thick $RbAg_4I_5$ ionic conducting layer was deposited on the MEH-PPV layer by thermal evaporation [25–27]. Finally, a Ti/Al gate electrode was deposited on the $RbAg_4I_5$ layer by electron-beam evaporation. Gate capacitors were fabricated on a p-Si wafer with a boron doping concentration of $3 \times 10^{15}\,cm^{-3}$. A 100-nm-thick Al layer was deposited on the backside of the Si wafer as the bottom electrode. The SiO_2, MEH-PPV, $RbAg_4I_5$ and gate metal layers were subsequently fabricated as described above. The lateral area of the gate capacitor was $\sim$3 mm^2. The control apacitors were fabricated by following the same process for the gate capacitors except the step to deposit the MEH-PPV polymer layer was omitted. After the application of voltage biases to the gate capacitors, their top Al/Ti metal electrodes were then glued to a glass slide with an epoxy, and the Al/Ti/$RbAg_4I_5$/MEH-PPV top layers were physically peeled off from the SiO_2/p-Si substrate to expose the MEH-PPV polymer layer. The XPS chemical depth profiles in the polymer layers were subsequently analyzed by ion-milling the exposed polymers using a PHI Quantera Scanning ESCA. The electrical measurements were conducted using a HP4156B semiconductor parameter analyzer, Agilent 33220A and 33250A function generators, a Tektronix TDS3054B oscilloscope, and a Keithley 428-PROG current amplifier.

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