Nanoscale Electronic Synapses Using Phase Change Devices

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The memory capacity, computational power, communication bandwidth, energy consumption, and physical size of the brain all tend to scale with the number of synapses, which outnumber neurons by a factor of 10,000. Although progress in cortical simulations using modern digital computers has been rapid, the essential disparity between the classical von Neumann computer architecture and the computational fabric of the nervous system makes large-scale simulations expensive, power hungry, and time consuming. Over the last three decades, CMOS-based neuromorphic implementations of "electronic cortex" have emerged as an energy efficient alternative for modeling neuronal behavior. However, the key ingredient for electronic implementation of any self-learning system—programmable, plastic Hebbian synapses scalable to biological densities—has remained elusive. We demonstrate the viability of implementing such electronic synapses using nanoscale phase change devices. We introduce novel programming schemes for modulation of device conductance to closely mimic the phenomenon of Spike Timing Dependent Plasticity (STDP) observed biologically, and verify through simulations that such plastic phase change devices should support simple correlative learning in networks of spiking neurons. Our devices, when arranged in a crossbar array architecture, could enable the development of synaptronic systems that approach the density ($\sim 10^{11}$ synapses per sq cm) and energy efficiency (consuming $\sim$1pJ per synaptic programming event) of the human brain.

Categories and Subject Descriptors: C.1.3 [**Processor Architectures**]: Other Arduteaher Styles—*Neural nets*

General Terms: Design, Experimentation, Porfromance

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1. INTRODUCTION

One of our chief tools in unraveling the computational principles of the brain is neural simulation. Simulations allow us to investigate ideas, test hypotheses, and inspire experiments in a manner that is complementary to experimental neuroscience. The avenues for neural simulation fall into two principal approaches: software simulations on general purpose computers (or supercomputers) [Rochester et al. 1956], and emulation on special purpose neuromorphic hardware [Mead 1990]. The former approach has the advantages of flexibility and availability, but requires heroic efforts to scale to large problems [Ananthanarayanan et al. 2009; Ananthanarayanan and Modha 2010; Mead 1990; Djurfeldt et al. 2008; Izhikevich and Edelman 2008]. The latter approach in principle, is much more attractive in terms of the speed and scale of simulation achievable in terms of energy consumption, physical size and economics [Silver et al. 2007]. Perhaps most enticingly, advances in neuromoprhic hardware design and architecture [Gao and Hammerstrom 2007; Hynna and Boahen 2007; Indiveri et al. 2006; Lazzaro 1992; Likharev and Strukov 2005] have buoyed hopes of rapidly translating neuroscientific discoveries into practical, portable cognitive technologies.

To date, a critical roadblock to progress on neuromorphic brain emulation has been the development of an electronic device capable of mimicking the plasticity of biological synapses at the physical scale and with the energy efficiency observed in nature. The nascent field of synaptronics seeks to leverage novel materials to design nanoscale devices that emulate biological synapses. The development of small, readilymanufacturable, low power synaptronic devices is of fundamental importance because the computation, memory, and communication requirements of a neural emulation all scale with the number of synapses [Ananthanarayanan et al. 2009; Ananthanarayanan and Modha 2010]. These devices must recapitulate the plasticity of biological synapses because synaptic plasticity is thought to be the "fundamental mechanism for information storage" [Kandel 2000] and higher order brain function (for a good review, see Abbott and Nelson [2000]). High density, low energy, durable, variable-state resistors that could be used as the basis for synaptronic devices are therefore a critical enabling technology for the roadmap of future neuromophic hardware development. Such non-volatile, programmable resistors could be configured in a dense crossbar array (Figure 1) above the silicon substrate, efficiently sharing peripheral circuitry and creating a unified fabric for synaptronic-neuromorphic computation. Promising technologies for realizing such resistive devices include metal oxides [Choi et al. 2009; Waser et al. 2009], solid-electrolytes [Hasegawa et al. 2010; Jo et al. 2010], carbon nanotubes [Friesz et al. 2007], organic electronics [Scott and Bozano 2007; Tour et al. 2002], magnetic tunnel junctions [Gallagher and Parkin 2006], and phase change elements (PCE) [Raoux and Wuttig 2009; Ovshinsky 2004b]. To date, no single technology has emerged as the clear leader, meeting all the design criteria with an elegance and efficiency that matches biological synapses. However, due to favorable scaling trends [Burr et al. 2010] we expect PCE to provide the requisite footprint, energy efficiency, and plasticity required of neuromorphic systems.

In this report, we introduce two programming schemes that are able to reproduce well-known biological synaptic plasticity dynamics in 40nm mushroom and 10nm pore

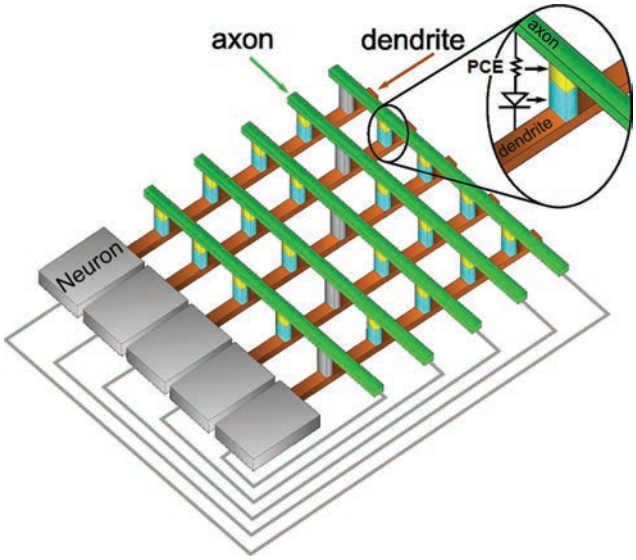

Fig. 1. Diagram of a proposed crossbar array of phase change material for neuromorphic systems. At the junction between axons and dendrites lies the phase change element (PCE, yellow) and access device (blue). The neurons in this scheme are configured as circuits at the periphery of the array.

Phase Change Elements (PCE), at programming energies below 5 pJ/event. To foreshadow the utility of such devices, we provide computational evidence that the properties of these electronic synapses support the learning of simple temporal sequences by spiking neural networks. The invention of these PCE programming schemes, and their demonstration on real hardware devices, marks a significant step towards the realization of high density, low power, programmable synaptronic arrays.

2. FROM BIOLOGICAL OBSERVATION TO ELECTRONIC TESTS

Emulating biological synaptic plasticity in solid-state electronics is the immediate objective of synaptronics. While the exact mechanism of biological synaptic plasticity remains controversial, there is growing evidence that correlated pre- and postsynaptic activity drives plasticity [Abbott and Blum 1994; Blum and Abbott 1996; Brader et al. 2007; Gerstner et al. 1996; Hopfield and Brody 2004; Mehta et al. 2000; Minai and Levy 1993; Rao and Sejnowski 2001; Roberts 1999; Song et al. 2000]. One popular model, Spike Timing Dependent Plasticity (STDP), holds that spiking of the presynaptic neuron followed shortly by spiking of the postsynaptic neuron (causal) increases effective synaptic conductance, while spiking in the opposite (anticausal) temporal order decreases conductance. The closer the two spikes occur in time, the greater the average conductance change, and the longer the delay, the smaller the change [Bell et al. 1997; Bi and Poo 1998; Dan and Poo 2004; Debanne et al. 1998; Egger et al. 1999; Feldman 2000; Magee and Johnston 1997; Markram et al. 1997; Zhang et al. 1998] (Figure 2). Although there has been no definitive demonstration that this phenomenology is either necessary or sufficient for cognition, STDP is among the most studied mechanisms for synaptic modification [Song et al. 2000; Izhikevich 2006] and has become the basis of many promising synaptronic technologies [Arthur and Boahen 2006; Bofill et al. 2001].

To mimic spike timing dependent behavior in hardware while maximizing energy efficiency, we propose that device programming should occur only due to the combined action of electrical signals applied by the pre- and postsynaptic neurons. To reproduce changes in synaptic efficacy over the 100 ms spike pairing window observed in

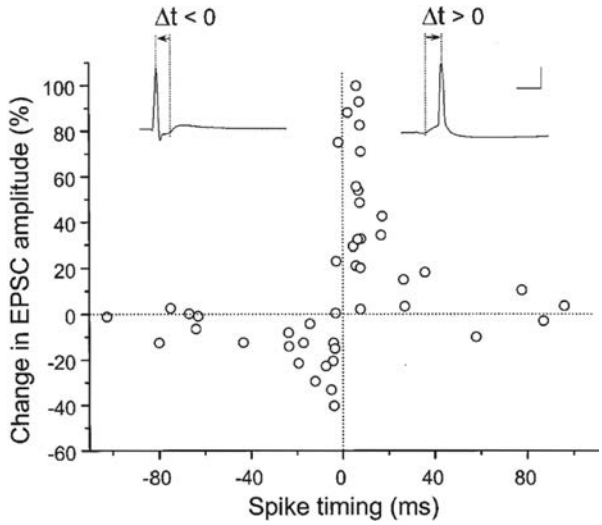

Fig. 2. Spike Timing Dependent Plasticity (STDP) as observed in rat hippocampal neurons. Reprinted with permission from [Bi and Poo 1998] (© Journal of Neuroscience). Synaptic potentiation and depression was measured by monitoring the excitatory post synaptic current (EPSC) 20–30min after the repetitive correlated spiking (60 pulses at 1Hz). Spike timing was defined by the time interval (Δt) between the onset of the excitatory postsynaptic potential and the peak of the post-synaptic action potential during each cycle of repetitive stimulation.

biology, every neuron or synapse should have some form of book-keeping apparatus to remember and relay the information about its last firing event over a similar timescale. The many orders of magnitude that separate this timescale, the timescale over which decisions about plasticity are made ($T_{max} = 100$ ms), from the nanoscale timescales of device physics and conventional chip clock rates make the design of an efficient book-keeping scheme challenging. This is greatly exacerbated by the observation that any satisfactory bookkeeping mechanism cannot depend on extensive logic or memory at the individual synapse, because such logic would quickly come to dominate the size and density of the manufacturable devices. Here we present PCE device programming schemes that simultaneously satisfy all these requirements. The schemes illustrated here can be modified to implement many synaptic plasticity rules that depends only on the relative timing of pairs of pre- and postsynaptic spikes. To illustrate the versatility of our approach, we will use PCE cells to implement: a) standard STDP behavior [Abbott and Blum 1994; Song et al. 2000; Bi and Poo 1998] in the mushroom cell using a scheme that captures information about neuronal firing events in the spiking signal itself, and b) anti-STDP behavior, observed in the electrosensory lobe of electric fish [Bell et al. 1997], in the pore cell using a scheme that uses internal neuron circuits for the book-keeping.

2.1. Device and Circuit Primitives for Synaptronics

Nanoscale crossbar arrays with programmable resistors at the junctions can be employed to implement arbitrary and plastic connectivity between neuron circuits. An access device (also known as a control device or switch) such as a diode or an FET could be connected in series with the resistor at every crossbar junction to prevent crosstalk during signal communication (neuronal firing events and synaptic programming events) and to minimize leakage and power consumption (Figure 1). In this scheme, the neurons are configured as circuits at the periphery of a crossbar array. In addition

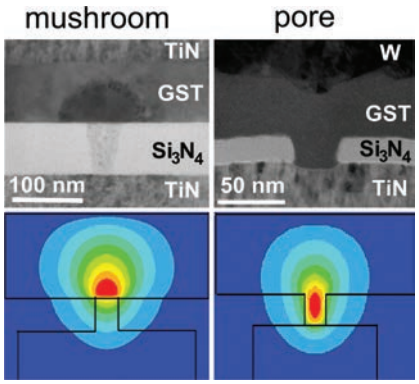

Fig. 3. Tranmission Eelectron Microscope (TEM) images of the two PCE device configurations presented in this study. The mushroom cell consists of a titanium nitride bottom electrode contacting GST through a 40nm via through a silicon nitride insulating layer. An amorphous plug appears as a dark hemisphere in the GST. The pore cell consists of a GST film (shown fully crystalline in this case) contacting the titanium nitride bottom electrode through a small opening in the silicon nitride layer. While a 30nm (nominal) device is shown here, PCM pore experiments shown later were performed on a 10nm nominal (19nm actual) device. Simulated thermal profiles during programming are presented below each TEM.

to being simple to design and fabricate, a crossbar architecture makes efficient use of the available real estate. Note that the complete connectivity inherent to the full crossbar array can be converted to any arbitrary connectivity by electrical initialization or omitting lithographic mask steps at undesired locations during fabrication. Therefore this architectural principle can mimic all the direct wiring combinations observed in biological neural networks. This architecture scheme deviates markedly from the conventional von Neumann scheme in that the computation is completely asynchronous and spike driven, while bypassing the physical bottleneck for data transfer by shrinking the logic and memory blocks to the junctions of the crossbar array. With the advent of techniques such as nanoimprint lithography [Chou et al. 1996], it is now possible to fabricate crossbar arrays at a pitch of 25–50nm; this, along with nanoscale plastic electronic synapses, will make the goal of realizing immensely parallel, connected networks of interacting neurons through plastic synapses an achievable reality.

2.2. Phase Change Elements

Phase Change materials, most commonly containing the elements Ge, Sb and Te (e.g., $Ge_2Sb_2Te_5$), exist in either a metastable amorphous phase, or in a stable crystalline phase, with markedly different optical and electrical properties [Ovshinsky 1968; Wuttig and Yamada 2007]. These materials can be programmed electrically by Joule heating to transform between the poorly conductive amorphous phase and the highly conductive poly-crystalline phase [Lai and Lowrey 2001]. Even though earlier work has hinted at the idea of building cognitive systems based on chalcogenide memory materials [Ovshinsky 2004a, 2004b], there has been no clear demonstration so far that establishes the synaptronic properties of phase change materials approaching the physical scale and energy efficiency of biological synapses.

The key requirement for any synaptic candidate is the retention of the level of coupling between two neurons, which can be modeled as a bounded but continuously-varying conductance value. Additionally, the synapses must be plastic, so that learning rules (e.g., STDP) can alter their conductance, providing a potential mechanism for experience based learning. Two commonly used memory device configurations were fabricated to study the neuromorphic properties of chalcogenide alloys (Figure 3). In

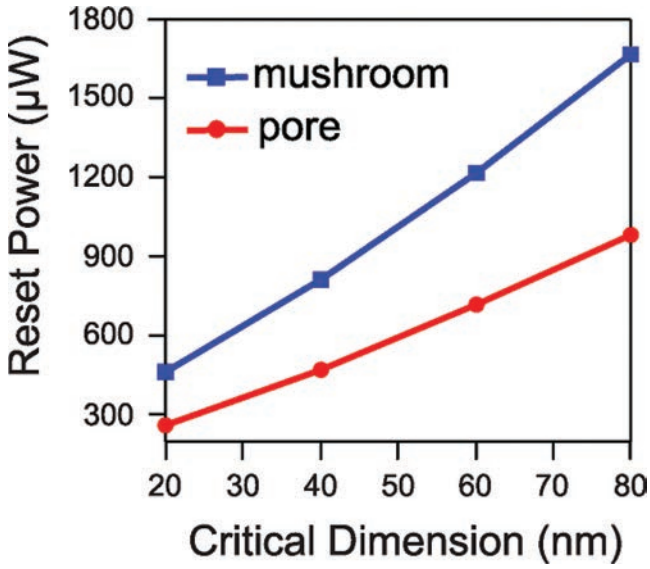

Fig. 4. Required PCE programming power for a range of actual critical dimensions, defined as the diameter of the silicon nitride openings for the device structures used in this study. The PCE pore devices require less programming power compared to the mushroom devices at identical critical dimensions, due to the optimized thermal profile of the structure.

the first implementation, called the mushroom device, a 100nm thick layer of phase change material, $Ge_2Sb_2Te_5$ (GST) is contacted by a ∼40nm diameter electrode embedded in Si_3N_4 [Nirschl et al. 2007]. In the second implementation, called the pore device, a ∼20nm diameter pore formed in a thin Si_3N_4 layer is filled with the phase change material [Breitwisch et al. 2007]. Electro-thermal simulations indicate that the pore device has a more optimized thermal profile compared to the mushroom device, thereby allowing programming with smaller power to obtain similar resistance contrast (Figure 4).

Programming a device to the poorly conductive "off" state is achieved by applying a large enough current through the device to melt a certain critical volume of the phase change material near the electrode; abrupt termination of the input current then quenches the molten volume to the amorphous state, effectively blocking the critical current path near the bottom electrode (Figure 3). The highly conductive on state is obtained by joule heating to above the crystallization temperature, where higher atomic mobility allows relaxation to the crystalline form. It is also possible to tune the size and shape of the amorphous volume in the current path, allowing access to intermediate resistance levels, simply by modulating the input current amplitude and duration [Nirschl et al. 2007]. The current-voltage (I-V) curve of a typical pore device is shown in Figure 5, illustrating the memory switching effect with a resistance contrast exceeding 100. This plot also illustrates the nonlinear voltage-to-current relationship for both the on and off states. The conductivity in the off state remains low until the voltage exceeds a threshold, after which the conductivity increases spontaneously (and reversibly). This phenomenon, called Ovonic Threshold Switching (OTS), is fast (<1ns) and is believed to be electronic in nature [Ovshinsky 1968; Adler et al. 1978; Redaelli et al. 2008].

2.3. Electronic Implementation of Synaptic Plasticity I

Our first coding scheme to generate STDP explicitly encodes neuronal firing delays within the electronic pulses arriving at the synapse (consisting of an access device,

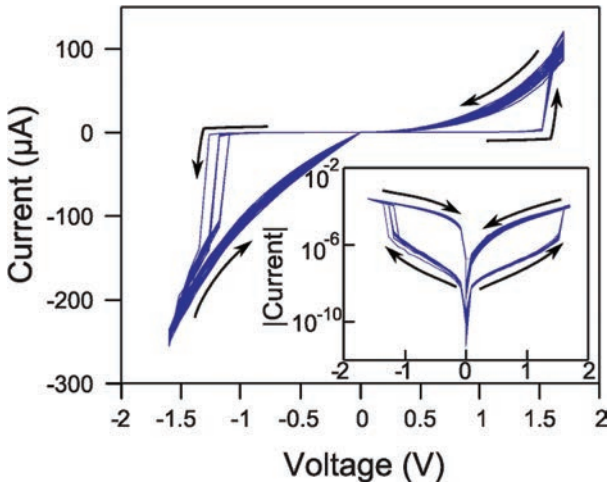

Fig. 5. Current-voltage characteristics of a 30nm nominal (30–35nm actual) phase change pore cell (in series with 3kΩ resistor), illustrating the non-linear response. A resistance contrast of more than 100 between the 'on' and 'off' states is evident in the logarithmic plot (inset).

FET, in series with a mushroom PCE). This insight removes the need for complicated timing circuitry at each synapse, and instead places the burden at the periphery, where several synapses can share common drive circuitry. This mechanism is best understood from a synaptic perspective. One long signal (duration of ∼200ms, defined here as $2T_{max}$) will arrive at the synapse from the axon with zero delay after the *pre-synaptic* neurons spikes. This pulse is intentionally asymmetric, with the early portion of the pulse (higher amplitude) encoding the possibility of conductance decrease, while the latter portion (lower amplitude) encodes a conductance increase. The destination of this long signal is the gate of the synaptic FET (Figure 6). A short (∼60ns in this experiment) signal will arrive from the dendrite with a delay of $T_{max} \sim$ 100ms after the *postsynaptic* neuron spikes. This pulse is applied directly to the PCE (Figure 6). The FET only permits programming (and the associated energy consumption) during the brief overlap between the two signals (Figure 7). During asynchronous neuronal firing, any causal parings (pre-before-post, $\Delta t > 0$ in Figure 6) will cause the shorter pulse to coincide with the lower amplitude portion of the long pulse. This scenario will draw only enough power to heat the phase change material to its crystallization temperature (Figure 7), thus increasing conductance. By contrast, anti-causal pairings (post-before-pre, $\Delta t < 0$ in Figure 6) will draw sufficient power to melt-quench the volume near the GST-electrode interface (Figure 7), thus decreasing conductance. The long signal increases over the first 100ms and decreases afterwards, so that maximum programming current (and hence the largest changes in conductance) occur in the vicinity of $|\Delta t| = 0$. Note that straightforward modification of the long signal can generate other forms of conductance change as a function of the neuronal firing delay. For instance, if waveform $f(t)$ applied at the gate of the FET implements STDP behavior (Figure 6), then $f(2T_{max} - t)$ generates anti-STDP behavior.

To emulate the asynchronous neuronal firing observed in biology, we apply the two waveforms associated with the pre- and postsynaptic neurons with random delay using arbitrary function generators. The device conductance measured before (G_i) and after (G_f) each pair of pulses is used to determine the effective change in conductance,

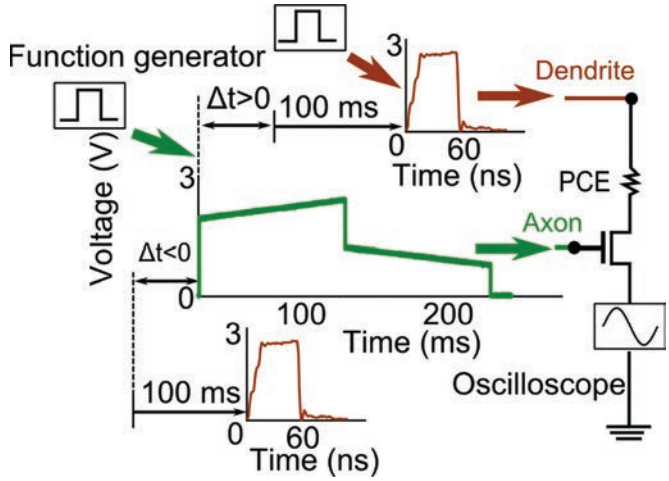

Fig. 6. Implementation of STDP on a 40nm mushroom PCE. Algorithm: the spiking neuron immediately transmits a 200ms signal to the axon (gate terminal of the transistor), followed 100ms later by a short (60ns) gating pulse at the dendrite, connected directly to the PCE. The 200ms signal is intentionally asymmetric, such that for $\Delta t < 0$, overlap of the two signals passes large currents sufficient for melt-quenching (conductance decrease), while for $\Delta t > 0$ currents are sufficient only for recrystallization (conductance increase). In the circuit configuration on the right, it is assumed that the axon of a presynaptic neuron is connected to the gate terminal, while the dendrite of a *distinct* postsynaptic neuron is connected directly to the PCE.

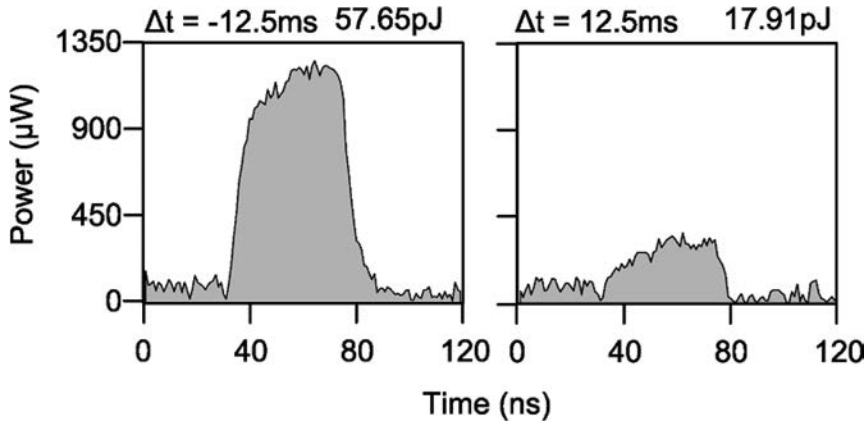

Fig. 7. Plot of instantaneous power consumption in the mushroom PCE during negative ($\Delta t = -12.5$msec) and positive ($\Delta t = +12.5$msec) pulse overlap. The integrated energy consumed during programming is 57.76 pJ and 17.91 pJ respectively.

defined as

$$\Delta G = \frac{G_f - G_i}{min(G_f, G_i)}. \tag{1}$$

This experiment revealed that when the initial conductance was low (diamonds in Figures 8 and 9), the pre-before-post pairings ($\Delta t > 0$) caused large (up to $20x$) increases in conductance. However, post-before-pre pairings ($\Delta t < 0$) caused little change, due to saturation in device conductance. The inverse relationship was observed when the initial conductance was high. Figure 8 plots the effective change in PCE device conductance as a function of Δt, clearly demonstrating the same analog STDP observed

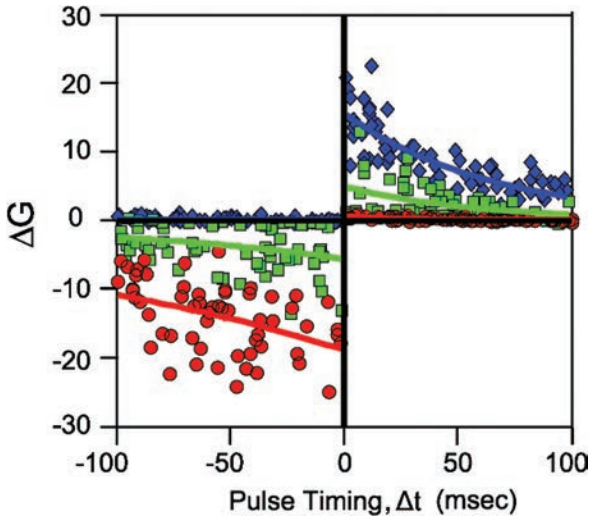

Fig. 8. Aggregate STDP results from 1000 pulses with random pulse timing in the mushroom PCE. The effective change in conductance ΔG, defined as the ratio of $G_f - G_i$ to $\min(G_f, G_i)$ is plotted as a function of the pulse timing, Δt. Diamonds correspond to low initial conductance values of PCE ($<0.5\mu S$), squares to medium conductance values ($>0.5\mu S$ and $<5\mu S$) and circles to high conductance values ($>5\mu S$). When the initial conductance was low (diamonds), the pre-before-post pairings ($\Delta t > 0$) caused large (up to $20x$) increases in conductance. However, post-before-pre pairings ($\Delta t < 0$), which would normally cause a reduction in conductance, caused little change to this initially low conductance population due to saturation in device conductance. When the initial conductance state was relatively large (circles), the inverse relationship was observed.

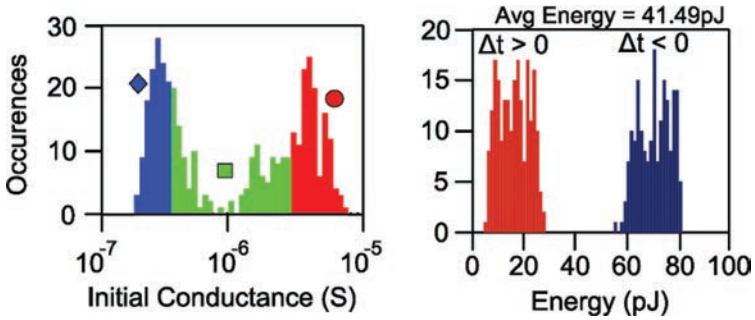

Fig. 9. Histogram of conductance values (initial state for Figure 8) and energy per programming event for all pulse timings: positive (red) and negative (blue).

in biological synapses. Figure 9 shows the histogram of initial conductances and energy per programming event for positive and negative Δt.

Implementing plasticity is only one aspect of engineering a functional synaptronic system. Each neuron must also transmit its spike, weighted by the associated synaptic strength, to all downstream neurons. With our PCE devices, such transmission might involve superimposing short spikes (10–100ns long) onto the axonal signal. While the spiking rate could exceed the biological rate of 10–100 Hz, the synaptic modification rate remains limited to $1/(2T_{max})$. In the next section, we illustrate an alternate method to mimic biological synaptic behavior that does not require an access device for energy minimization, per se, and at the same time, allows more frequent synaptic updates.

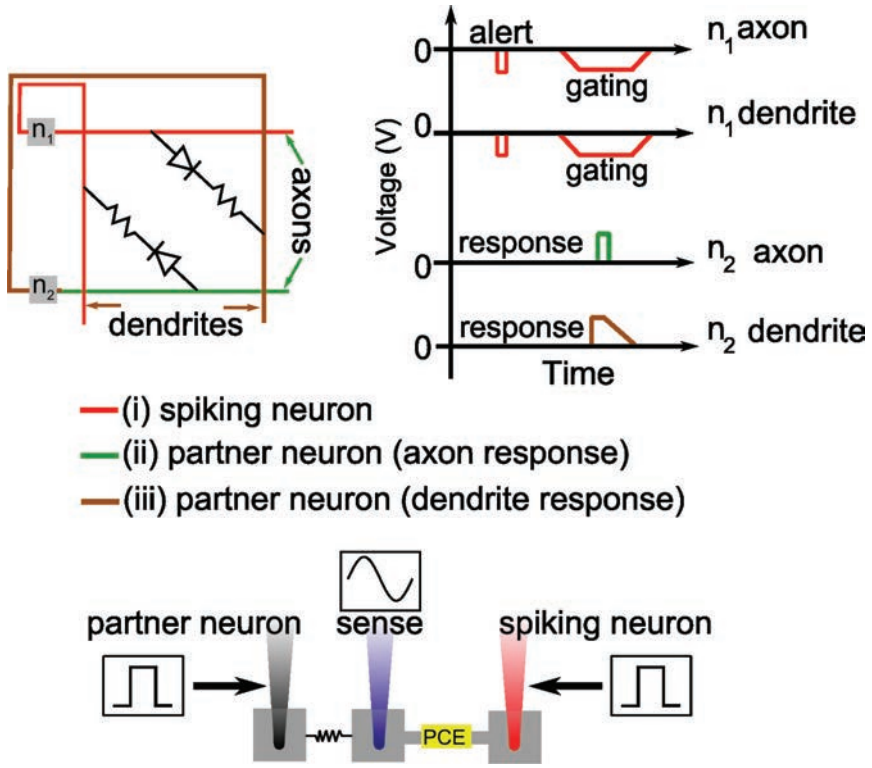

Fig. 10. Algorithm to implement aSTDP in PCE devices: spiking neuron (n_1) sends alert pulse to all connected neurons via axons and dendrites; once alerted, each synaptic partner (n_2) uses its capacitor voltage to return separate axon and dendrite response pulses V_t, which arrive at the PCE devices together with a gating pulse from n_1. Triangular axon pulses are designed to increase conductance of the PCE element; rectangular dendrite pulses decrease conductance. In Figures 11–14, this RC-timing synaptic programming scheme is used to implement anti-STDP behavior on a 10nm nominal (19nm actual) pore-type PCE.

2.4. Electronic Implementation of Synaptic Plasticity II

In our second programming algorithm, the delay since the last spiking event is not encoded within a long signal ($2T_{max}$) applied to the synapse; rather it is tracked internally within each neuron by a simple RC circuit. In this scheme, spiking neurons initialize a capacitor to some predetermined voltage, V_0. This voltage is allowed to decay through a resistor such that after a time interval t,

$$V_c(t) = V_0 \exp(-t/RC), \tag{2}$$

where R is the series resistance associated with the internal capacitance, C. In this section, we describe this programming algorithm, and then use it to implement anti-STDP behavior on a pore-type PCE. In this experimental demonstration, the RC-delays are computed by a control computer, but the resulting pulses are used to program and then read a real 10nm nominal (19nm actual) diameter pore-type PC.

The key insight behind this scheme is that this memory of each neuron's latest firing event is converted to a spike timing-dependent change in synaptic conductance through an asynchronous handshaking mechanism. This mechanism dictates that when a neuron spikes, it not only initializes its capacitor, but also sends a short "alert" pulse to all synaptic partners (Figure 10). This pulse serves to alert the synaptic partners to check the instantaneous voltage across their capacitors, V_c, and send a response pulse whose

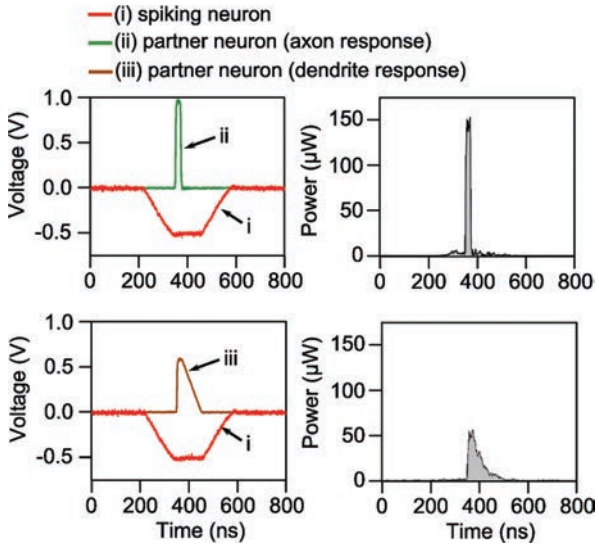

Fig. 11. Representative voltage and power traces under positive ($\Delta t = +3.1$ ms) and negative ($\Delta t = -3.2$ ms) spike arrival intervals, respectively, for a 10nm nominal (19nm actual) diameter pore PCE implementing anti-STDP behavior using the RC-timing programming algorithm.

amplitude is given by,

$$V_t = V_{offset} + V_c(t), \tag{3}$$

where the offset, V_{offset}, may be added to provide enough power to program the PCE.

The response pulse is sent after a constant delay such that its arrival at the synapse is coincident with a gating pulse sent by the spiking neuron. Given the nonlinear current-voltage relationship of phase change devices (Figure 5), only the superposition of the gating and response pulses can draw enough power to program a device (Figure 11). Thus, in a large crossbar array, only the synapses associated with the spiking neuron are programmed. The width of the gating pulse compensates for any unintended temporal jitter between the arrival of the alert and response pulses. The magnitude of the synaptic change is determined by the amplitude of the response pulse, V_t, while the shape of the response pulse is determined by whether the response pulse was applied to an axon or a dendrite (Figure 10). Responses generated by the axon are square pulses, so that the generated programming current in the PCE quenches abruptly, resulting in a decrease in the device conductance, while the responses generated by the dendrite are triangular pulses, so that the generated programming current in the PCE decreases more gradually, increasing the device conductance. The exponential time dependence of RC circuits ensures that the neurons that have not spiked recently send low magnitude response pulses. Note that we tune V_0 and V_{offset} separately for optimal axonal (conductance decrease) and dendritic (conductance increase) programming of the phase change devices (Figure 12). Also, the circuitry associated with converting V_c to V_t can be modified to produce arbitrary forms of timing dependent synaptic plasticity.

Since neuronal spiking duration is now determined by the alert (nanoseconds), delay (nano- to microseconds), and gating pulses (nano- to microseconds), the total programming duration is on the order of a few microseconds. This could allow both neuronal spiking and synaptic update rates to surpass 100 KHz—exceeding biological observations—while still maintaining delay memory out to $T_{max} \sim 100$ms. Note that

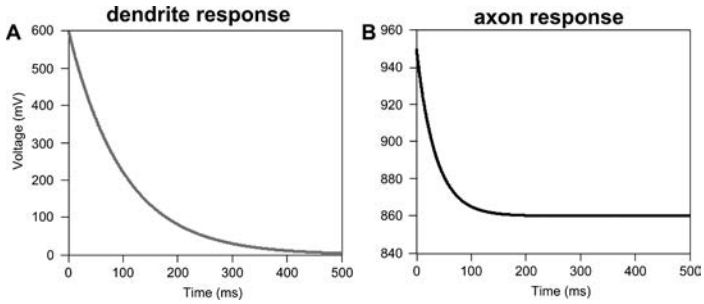

Fig. 12. The tuned RC responses used for experimental implementation of the RC-delay synaptic programming algorithm with a 10nm nominal (19nm actual) pore-type PCE. These curves governed the mapping from stochastic spike timing to the amplitude of the PCE programming pulse, through equations (2) and (3). The following parameters are used for dendrite responses: $V_{offset} = 0$ mV, $V_0 = 600$ mV and RC = 100 ms; for axon responses: $V_{offset} = 860$ mV, $V_0 = 90$ mV and RC = 35 ms.

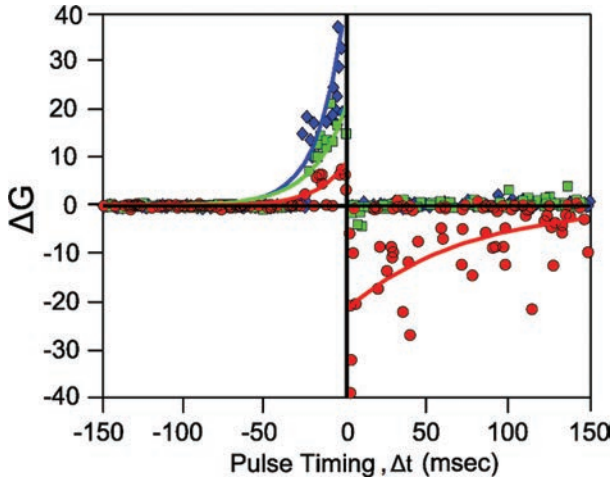

Fig. 13. Aggregate anti-STDP results from more than 400 pulses with random pulse timing for a 10nm nominal (19nm actual) diameter pore PCE. The effective change in conductance ΔG, defined as the ratio of $G_f - G_i$ to $\min(G_f, G_i)$ is plotted as a function of the pulse timing, Δt. Diamonds correspond to low initial conductance values of PCE ($<0.5\mu$S), squares to medium conductance values ($>0.5\mu$S and $<5\mu$S) and circles to high conductance values ($>5\mu$S). When the initial conductance was low (diamonds), the post-before-pre pairings ($\Delta t < 0$) caused large (up to $40x$) increases in conductance. In this low conductance regime, pre-before-post pairings ($\Delta t > 0$) caused little change, due to saturation in device conductance.

although programming of synaptic elements could be achieved without access devices, in a large crossbar array a diode (or FET) would help minimize crosstalk (Figure 10).

We implemented the RC delay based aSTDP learning scheme in a 10nm nominal (19nm actual) diameter pore PCE. The aggregate result of more than 400 pulse pairings with randomly selected timing is presented in Figure 13, again strongly resembling biological aSTDP. The distribution of energy per synaptic programming event is shown in Figure 14, indicating that synaptic plasticity is achievable with less than 5pJ (average was 2.74pJ) in these 10nm PCE devices. In plotting this historgram, we have excluded 13 programming events that were observed to have spurious noise spikes, though we have accounted for them in estimating the average energy of 2.74pJ. Excluding these spurious events gives an average energy of 2.50pJ.

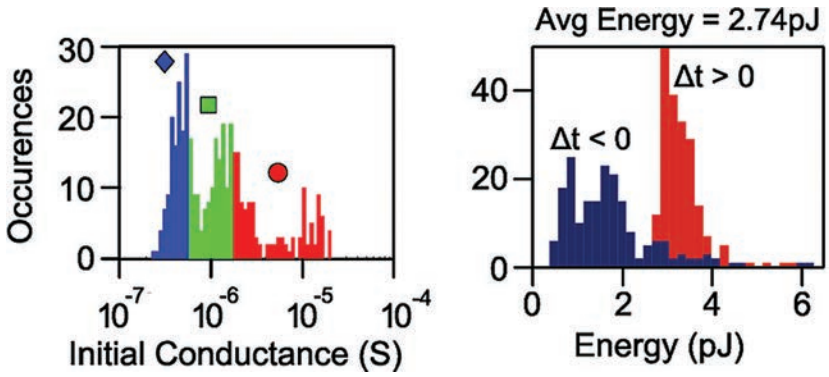

Fig. 14. Histogram of typical conductance values (initial state for figure 13) and energy per programming event for positive (red) and negative (blue) timing for the pore PCE device implementing aSTDP. Average energy is computed to be 2.74pJ.

3. SIMULATIONS

3.1. Phenomenological Model of the PCE Devices

In order to examine the expected computational properties of networks of PCE synapses, we developed a phenomenological model of the PCE device amenable to efficient numerical simulation. This model uses initial conductance and pre-post spike timing to determine the probability of making a state transition. If a random number draw indicates that a transition should occur, a new device conductance is drawn from a log-Gaussian distribution. The pre-before-post pairings are treated entirely separately from post-before-pre pairings, each requiring a distinct set of model parameters. For either type of pairing, the model gives the probability of the PCE device making transitions between the crystalline and amorphous states as a steep sigmoidal function of the pre-post spike timing Δt, modulated by the initial device resistance R_i according to

$$P(transition) = \left(1 + \exp\left[\frac{\Delta t + \alpha \log_{10} R_i + \beta}{\kappa}\right]\right)^{-1}, \tag{4}$$

where α, β and κ are parameters that control the timescale, threshold, and dependence on initial resistance of the sigmoid, respectively. The probability of choosing a resistance $R_f = 10^x$ is given by

$$P(x) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left[-\frac{(x - \mu \exp(\gamma \Delta t))^2}{2\sigma^2}\right], \tag{5}$$

where μ, σ and γ are parameters that control the mean, standard deviation, and dependence on spike timing of the log normal distribution, respectively. The three free parameters of each of the two model stages are fit separately to device data for pre-before-post and post-before-pre pairings, for a total of twelve model parameters. Parameter values depend on the physical characteristics of the device as well as the pulse protocol used to initiate phase changes. The model closely reproduces both the distribution of conductances and the STDP-like dynamics (Figure 15) measured for the physical PCE device presented in Figure 6.

3.2. Temporal Sequence Learning Based on PCE STDP

Temporal sequence learning is a simple, biologically relevant problem amenable to solutions by networks of STDP synapses. To assess whether PCE synapses can learn simple temporal sequences, we performed simulations on a network of 100 leaky

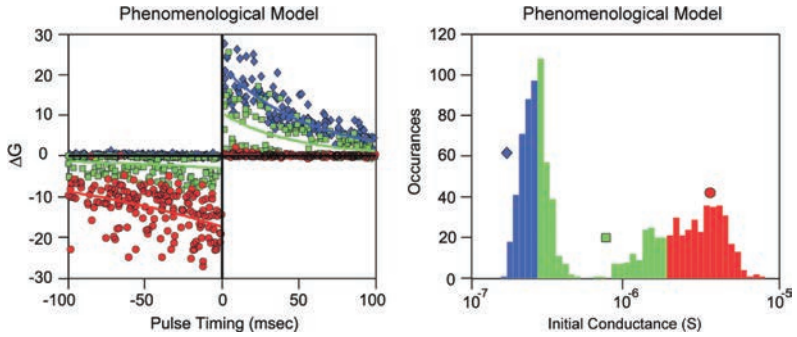

Fig. 15. The probabilistic model for PCE programming based on spike-timing as per equations (4) and (5) reproduces the STDP-like behavior of the PCE device from Figure 8. The phenomenological PCE model for device conductance (mixture of log Gaussians) also matched to measured device properties from Figure 9. These numerically simulated device characteristics are used to implement temporal sequence learning in the simulated network.

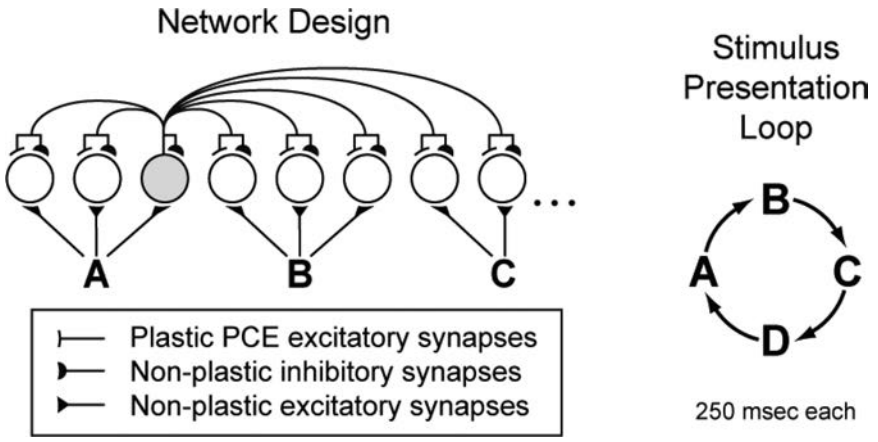

Fig. 16. Schematic of simulated network of leaky integrate-and-fire neurons for temporal sequence learning. Each neuron makes an excitatory connection to every other neuron via a plastic PCE synaptic device, like the crossbar array of Figure 1. Four pools of ten neurons each receive extra excitatory input during their associated stimulus condition. Non-plastic connections transmit global inhibitory signals. For clarity, forward projections from only one neuron in pool A are shown. Four stimuli (A, B, C, D) are successively presented during each cycle of temporal sequence learning. The task of this network is to learn to predict the next item in the sequence.

integrate-and-fire neurons connected with both plastic excitatory synapses (governed by our phenomenological PCE model) and static inhibitory connections; the task of this network is to learn to predict the next item in a repeating sequence of four stimuli (Figure 16).

The simulated network consisted of 100 leaky integrate-and-fire neurons suitable for straightforward implementation in hardware [Brader et al. 2007]. The membrane equations were updated once per millisecond of simulated time. Each neuron received an independently drawn Poisson input stream of 5 spikes per second, delivered through fixed-strength excitatory synapses. During the presentation of any given virtual 'stimulus' a fixed set of 10 neurons experienced an elevated input drive of 100 spikes per second throughout the duration of the stimulus phase (250ms). The set of neurons receiving this extra input drive during the presentation of stimulus A is termed Pool A, and so on for stimulus B though D.

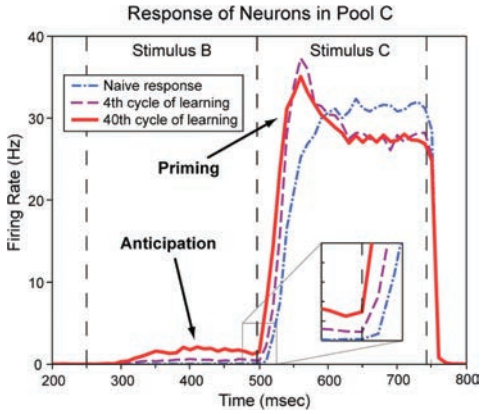

Fig. 17. Response of the ten Pool C neurons averaged over 2000 repetitions, changing from a sluggish to a brisk (primed) response by the fourth stimulus cycle with learning active. By the 40th stimulus cycle, pool C neurons have acquired a consistent, low-level response to stimulus B (anticipation).

The neurons communicated with each other through inhibitory and excitatory connections. The inhibitory connections had a uniform and constant synaptic strength and connected each neuron in the network to every other neuron in the network (including itself). The excitatory connections between neurons were the only plastic element in the network, and connected each neuron in the network to every other neuron (excluding itself). The strengths of these connections were governed by the phenomenological synaptronic model described above. The impact of a single presynaptic spike on the post-synaptic neuron's membrane potential was proportional to the conductance of the PCE device given by our phenomenological model. The conduction delay through any arc in the network was fixed at one millisecond. The strengths of the simulated PCE synapses were initialized to be 90% from the low conductance state and 10% from the high conductance state (Figure 18). Other initializations yield similar results, so long as the proportion of synapses in the high conductance state is not so high as into induce violent reverberant firing of the network.

Before learning, the neurons in any particular subset (say, pool C) are observed to respond only during the presentation of that particular stimulus, and require 100 msec to reach peak firing rate (Figure 17, blue broken line). By the fourth learning cycle the response of these neurons became substantially more brisk and vigorous (Figure 17, purple dashed line), an indication that the pool is 'primed' for the onset of the stimulus. On the fortieth learning cycle, the onset of their response is even more brisk, and each pool has acquired a modest anticipatory firing response to the predictive stimulus (e.g., pool C anticipates during stimulus B). This response profile, exhibiting temporal sequence prediction both in the form of priming and anticipation, remains stable even after hundreds of additional trials of learning, and can be explained in terms of the changes in synaptic strength of PCE synapses between pools of neurons (Figure 18).

The naïve response of the network (Figure 17) is determined by the initial weight distribution, and as would be expected, each pool of neurons only gives a significant response to the stimulus it is constructed to be selective for. As the initial conductance distribution is random, neurons in each pool can only respond to the external stimulus they receive. However, once trained, the response of the network show temporal sequence prediction both in the form of primed response and anticipatory firing (Figure 17). This can be explained by the evolution in the conductance state of the PCE synapses. Figure 18 shows the weight distribution for one snapshot during the 40th repetition of the stimulus cycle. The weights show potentiation in the predictive direction;

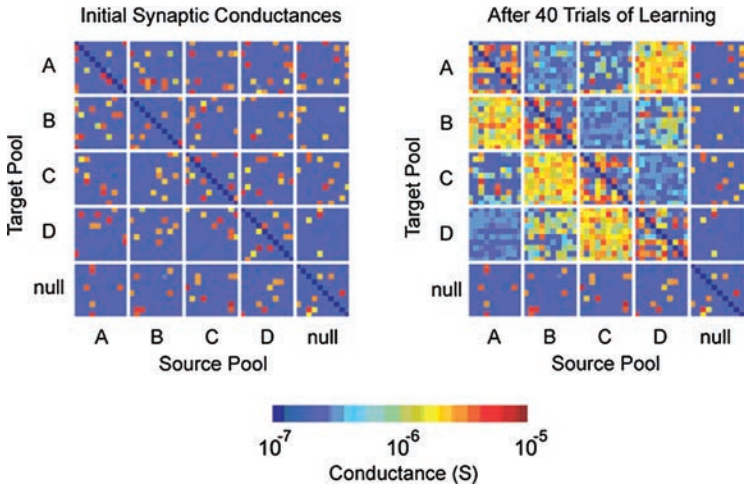

Fig. 18. Pseudocolor plot of simulated PCE conductances, initially (left) and after the 40th cycle of learning (right). For clarity, only 50×50 of the 100×100 simulated crossbar array is plotted. After learning, synaptic connections in the predictive direction (from pool A to B, from B to C, etc.) are strongly potentiated.

in particular, the patches of the array showing connections from pool A to pool B, from B to C, from C to D, and from D to A are now almost entirely conductances of above 10^{-6} Siemens. When neurons from a particular pool are active, this activity provides positive (excitatory) input to the next pool of neurons, leading to anticipatory firing from them.

Patches showing connections within a pool have a mixture of high and low conductance synapses as a result of the random pre-post pairings within that pool when that pool is driven directly by the stimulus. The states of these synapses is highly dynamic, changing radically during each stimulus presentation. However, the qualitative pattern of connectivity and the basic response profile of the network remains stable over hundreds of additional presentation of the stimulus cycle. It was also observed that if the temporal sequence is reversed or scrambled, the network rapidly shifts its responses to reflect the new stimulus order. Such changes in the temporal sequence order are quickly reflected in the response profile of the network, because the network is able to dynamically adjust the connectivity to unlearn the old sequence and relearn the new one.

It is worth noting that the continual rapid changes in synaptic strength of the within-pool connections of the stimulated pool have a dampening effect on the overall firing of the network. Freezing the synaptic strengths at any given postlearning state results in an increase in the firing rate of the network to the presentation of a stimulus. This increase in network activity in one pool in turn drives substantially larger anticipatory responses in neighboring pools. This observation does not particularly impact the interpretation of the network as having successfully completed temporal sequence learning, but instead underscores that the dynamic, learning network behaves differently than one with entirely static synaptic weights.

4. OUTLOOK

The synaptronic element we propose represents a significant advance in neuromorphic synaptic device design, but how does it compare to a real biological synapse? Physical size has important functional ramifications because the sheer number of synapses involved in cortical computation is so vast. On this count, our device fares well. Biological synapses vary widely in size but are typically a few hundred nanometers in diameter, whereas phase change devices are roughly one tenth that size: manufacturable at

45nm today and eventually 22nm using optical lithographic techniques, and down to as small as 10nm using electron beam lithography or nanoimprint lithography.

A second critical point of comparison is durability. The lifespan of an artificial cognitive system will, in part, be determined by the switching endurance of the synaptic element. Since phase change devices have been demonstrated to exhibit endurance exceeding 10^{12} cycles [Lai and Lowrey 2001] the synaptic lifespan even in the worst case that programming events occurred at 10Hz would be greater then 3,000 years. However, if the device endurance was only 10^9 this would correspond to a worst case synaptic life span of approximately 3 years (30 years assuming more realistic programming rate of 1Hz). A third consideration is energy consumption. High energy consumption rates impose restrictions on portability. The same assumed upper bound of a 10Hz programming rate and 2.7pJ per programming operation implies that 200 trillion synapses require ∼5kW of power. In contrast, the human brain needs only 20 W to operate a similar number of synapses. Though our synaptronic power efficiency is ∼250 times below biological standards, it is a dramatic improvement when compared to the estimated several hundred megawatts that a supercomputer might require to simulate an equivalent number of synapses in software.

The most important points of comparison, of course, are the functional properties of information transmission and plasticity. On these points, meaningful comparison is difficult because neuroscience cannot yet say which properties of biological synapses are relevant for function. Our devices far outstrip the reliability of information transmission though biological synapses (which may fail as much as 50% of the time) [Allen and Stevens 1994], though it is not entirely clear that this is necessarily a functional advantage [Maass and Natschlager 2000]. One point of dissimilarity between biological synapses and PCE is the propensity for resistance drift of the amorphous volume [Pirovano et al. 2004; Boniardi et al. 2009]. Although, it is unclear how this resistance drift would affect large scale neuromorphic systems, early indications are that it would further quiet synapses that have already been effectively turned off. Thus, drift should have little functional relevence. As was our objective, our devices reproduce the gross phenomenology of STDP Hebbian plasticity, but no final word is available on that mechanism's role in cognition. Fortunately, the general PCE programming principles we have described here can be readily adapted to emulate other forms of spiking timing dependent plasticity as their relevance for function becomes clearer.

The correspondence between the properties of biological and electronic synapses will undoubtedly improve with time. Further studies will be required to reduce power usage, and to identify electronic elements and programming schemes that can mimic the complexity and variety inherent to the biological brain (e.g., neurotransmitter types, neuromodulators, short-term plasticity, electrical synapses, structural plasticity, etc). Separate from these are the architectural and integration challenges inherent to the fabrication of vast arrays of PCE synapses coupled to CMOS neurons. We are optimistic that these technical concerns can be addressed in the near term, and that a new generation of neuromophic-synaptronic chips will allow us to explore computation in networks with synapse-to-neuron ratios heretofore unimaginable, yet within reasonable power and space constraints. Our hope is that these devices will facilitate great strides, either towards the engineering of artificial cognitive systems with unprecedented computing power, or towards improved understanding of our own highly-evolved brains, or—in the best case—both.

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