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Emerging Memory Devices for Neuromorphic Computing

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A neuromorphic computing system may be able to learn and perform a task on its own by interacting with its surroundings. Combining such a chip with complementary metal–oxide–semiconductor (CMOS)-based processors can potentially solve a variety of problems being faced by today's artificial intelligence (AI) systems. Although various architectures purely based on CMOS are designed to maximize the computing efficiency of AI-based applications, the most fundamental operations including matrix multiplication and convolution heavily rely on the CMOS-based multiply–accumulate units which are ultimately limited by the von Neumann bottleneck. Fortunately, many emerging memory devices can naturally perform vector matrix multiplication directly utilizing Ohm's law and Kirchhoff's law when an array of such devices is employed in a cross-bar architecture. With certain dynamics, these devices can also be used either as synapses or neurons in a neuromorphic computing system. This paper discusses various emerging nanoscale electronic devices that can potentially reshape the computing paradigm in the near future.

1. Introduction and Background

Over the last few decades von Neuman architecture,[1] powered by Moore's law,[2] has revolutionized computing, driven every advancement in the technology revolution and brought us to the information age we are living in today. In 1965, Intel cofounder Gordon Moore predicted the number of transistors in each new generation chip will double, hence doubling the compute capability compared to the previous generation for the same cost of production. Prior to the existence of Moore's law, John von Neumann described the design architecture of an electronic stored program computer, the so-called von Neumann machine. Von Neuman architecture gave an opportunity to the designers in the era of Moore's law to exploit the ever-increasing processing power of the microprocessors to build various complex computational systems.

Today, we use our computers for playing games, watching videos, listening to music, preparing documents, and so on, all by using essentially the same system. This is possible because the modern computers are still largely based on the von Neumann architecture, and designed as a general-purpose machine, which make computers useful and convenient to use, but they are highly inefficient for data intensive tasks. The bus connecting memory and processor becomes a bottleneck for data transfer, referred to as the von Neumann bottleneck.[3] To improve the performance of computing systems in the so-called "big data" era, we must fundamentally change the way we compute today. Instead of being compute-centric, we should transgress to a data-centric paradigm.

Neuroscientists and psychologists, all around the world have been studying the functional architecture of the human brain for centuries, which inspired data-centric computing methods such as artificial neural networks (ANNs) and machine learning (ML). The human brain can be characterized by its massive parallel reconfigurable connections (synapses or memory) connecting billions of neurons (the main processing unit).[4] Synapses play a very important role in achieving learning and adaptability of the human brain. The weight of a synapse shows connection strength between the two neurons linked by that synapse. In the learning phase, the synaptic weight changes in an analog fashion based on the learning rules.[5] ML and ANNs use a high-level abstract concept of human cognition and are referred to as brain-inspired computing. To further leverage and exploit the potential advantages and capabilities of the human brain, we may need to more faithfully mimic its functionality on hardware. Emerging devices that can be used for such neuromorphic computing with different levels of brain-inspiration will be our topic of discussion in this paper.

In recent years, neuromorphic computing has emerged as a promising technology for the post-Moore's law era. Neuromorphic computing systems are highly connected and parallel, consume relatively low power and process in memory. To implement a neuromorphic system on hardware, it is important to realize: (1) artificial neurons that mimic biological neurons and (2) artificial synapses that emulate biological synapses, both of which must be power-efficient, scalable, and capable of implementing relevant learning rules to facilitate large-scale neuromorphic functions. To this end, over the last few years, numerous efforts have been made to realize artificial synapses using post-CMOS devices, including resistive random-access memory (ReRAM) (drift[6] and diffusive[7] memristors),

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phase change memory devices,[8] magnetoresistive random-access memory (MRAM),[9] ferroelectric field effect transistor (FeFET),[10] and others. More recently, attempts have also been made to develop a non-CMOS neuron, based on emerging devices. In this paper, we will discuss the major emerging memory technologies that hold the promise for neuromorphic computing and highlight some recent significant progress on device studies. We will also assess the advantages and challenges for each device technology, and comment on their future directions in the context of neuromorphic computing.

2. ReRAM

Narrowly defined, memristors (commonly called ReRAM for memory applications) are two-terminal resistance switches that can retain their internal resistance states depending on the history of applied voltages/currents.[11] They have attracted special and intensive interests because of their promising properties including scalability,[12] CMOS compatibility,[13] low power consumption,[14] and analog conductance modulation,[15] standing out as one of the most promising technologies for memory and unconventional computing.[11] Memristors usually have a simple metal/insulator/metal structure. The memristive switching phenomena have been observed in various materials, such as oxides,[16] nitrides,[17] perovskite,[18] chalcogenides[19] as well as organic materials.[20] Based on the filament rupture mechanism, there are two types of memristive devices that are important for neuromorphic computing, namely, drift, and diffusive memristors.[7] In this section we will discuss the drift memristor, and diffusive memristors will be discussed separately in the next section. Classified by the switching mechanisms, memristors can be simply grouped into ionic or electronic switching devices. The electronic switching devices are mostly relying on the electron trapping/detrapping phenomenon while the ionic devices can be categorized into cation and anion devices depending on the mobile species. In the cation devices, also called as electrochemical metallization memory, the switching is attributed to the formation and the rupture of the conduction channel(s) by the motion of cations from electrochemically active materials, such as Cu or Ag, that are commonly used as electrodes or embedded in the insulating layers.[21] Similarly, in anion devices, the motion of anions, e.g. oxygen ions in metal oxides or equivalently oxygen vacancies, leads to valence changes of the metal (cations) and, hence, changing the resistance of the metal oxide material, which is the reason why these devices are also called valence change memory (VCM).[21]

The exact mechanisms for most memristive systems have not been fully understood yet since the active region is usually confined at the nanoscale, making it challenging to clearly study the dynamic switching processes.[22] Thanks to the rapid progress of state-of-the-art physical and chemical characterization techniques, such as in situ and ex situ high resolution transmission electron microscopy,[23] researchers are able to obtain in-depth information. Recently as reported by Wedig et al.[24] based on their scanning tunneling microscopy (STM) studies, metal cations may also be mobile in traditional anion or VCM devices. The sample used in their studies has 2 nm thin TaO_x deposited on Ta bottom electrodes and the sample was then annealed to further increase the conductivity of the oxide layer. As shown in **Figure 1**, with an anodic tip voltage of 1 V and with Ta electrodes grounded, no change was observed.

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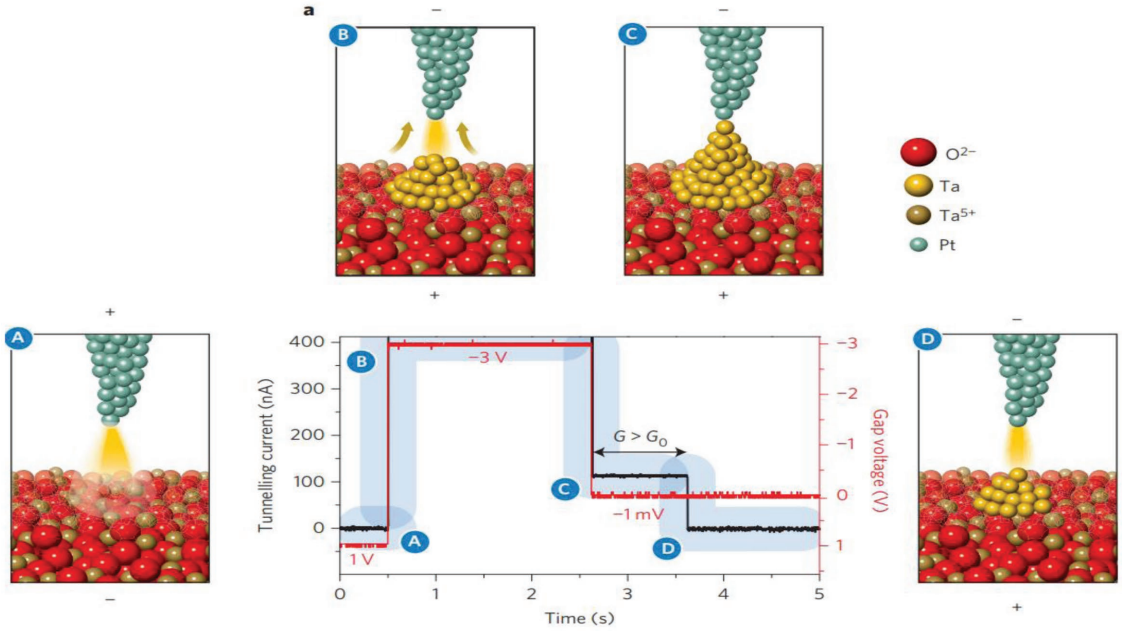

Figure 1. Time dependence of the STM tip current measured on a 2 nm thin TaO_x film under UHV conditions. Tip voltage varied from +1 V to −3 V to −1 mV. The strong increase in current at −3 V indicate switching of the device to LRS(B). Measured resistance at a read voltage of −1 mV was 9.6 kΩ, which corresponds to a conductance higher than the quantum point contact conductance G_0 ($G = 1.3G_0$), indicating the formation of a metallic quantum point contact between STM tip and diffused Ta ions that is temporarily stable after removal of the high electric field. All panels reproduced with permission.[24] Copyright 2016, Springer Nature.

While changing the tip voltage to −3 V, a significant jump in current was detected, indicating the resistance switching from high-resistance state (HRS) to low-resistance state (LRS), with the LRS conductance being 1.3 times the atomic point contact quantum conductance G_0. The observed switching resulted from the motion of Ta cations and formation/rupture of Ta metallic channels. Similar results were also revealed in HfO_x and TiO_x systems. The studies concluded that in these well-known VCM materials, not only oxygen vacancies, but also cations can play an important role during switching, providing fundamentally new insight into the memristive switching mechanisms. Incorporation of cations into the conduction channel in hafnium oxide was directly captured by ex situ transmission electron microscopy (TEM) studies, which served as solid evidence to the above conclusion.[25]

The basic understanding of switching induced by ionic motion helps the studies of memristors which are extended to more interesting materials, e.g., organic–inorganic halide perovskite materials.[26] Such kind of materials have been widely used for solar cells and photodetectors, and previous studies have shown that the charged defects can migrate in them under an electric field or with light illumination, suggesting more than one way to control the switching in these materials. As an important example, Zhu et al.[26] observed reliable switching in devices based on $CH_3NH_3PbI_3$ ($MAPbI_3$) films sandwiched between two electrodes (**Figure 2**a). Figure 2b shows the typical DC *I*–*V* sweeps, where the device can be set at 0.32 V and reset at −0.13 V with a 10^7 ON/OFF ratio. Based on energy-dispersive X-ray spectroscopy analysis, the switching should be attributed to the formation and annihilation of iodine vacancies. As expected, light illumination can affect the ionic migration process and hence the switching behavior. Figure 2c shows a simple example where the device can be switched from LRS to HRS by light illumination and can achieve reliable switching cycles with electrical pulses to set the device, while using light illumination to reset. The results helped the development of coupled electronic, ionic and photonic devices, providing insight into and triggering more interest of engineering memristive devices for various properties and applications.

As the analog internal state of the memristor is determined by the history of electric signal, memristors could be used to simulate both neuronal[27] and synaptic dynamics including spike-timing-dependent plasticity (STDP).[15,28] However, RRAM may face reliability issues due to the intrinsic randomness associated with the growth and rupture of conducting filaments. The analog modulation of device conductance is a very critical requirement when memristors are used for computing.[11,29] To update the conductance state, or weight, the relationship between the device conductance and the number of identical programming pulses is desired to be linear and symmetric for a direct mapping of the weights in the algorithms to the conductance in the devices.[29] Although a lot of effort have been made to engineer the devices, in real scenarios, most of devices still show nonlinear and asymmetric behavior on weight update. At the same time, the uncontrollable ion transport through the defects in the oxide layer, created due to device operation, can result in 3D stochastic filament formation leading to significant variations in device switching behavior (cycle-to-cycle and device-to-device).

Although a certain degree of variation can be tolerated when larger memristor arrays are used as neural networks, the requirement on the uniformity is still very important,

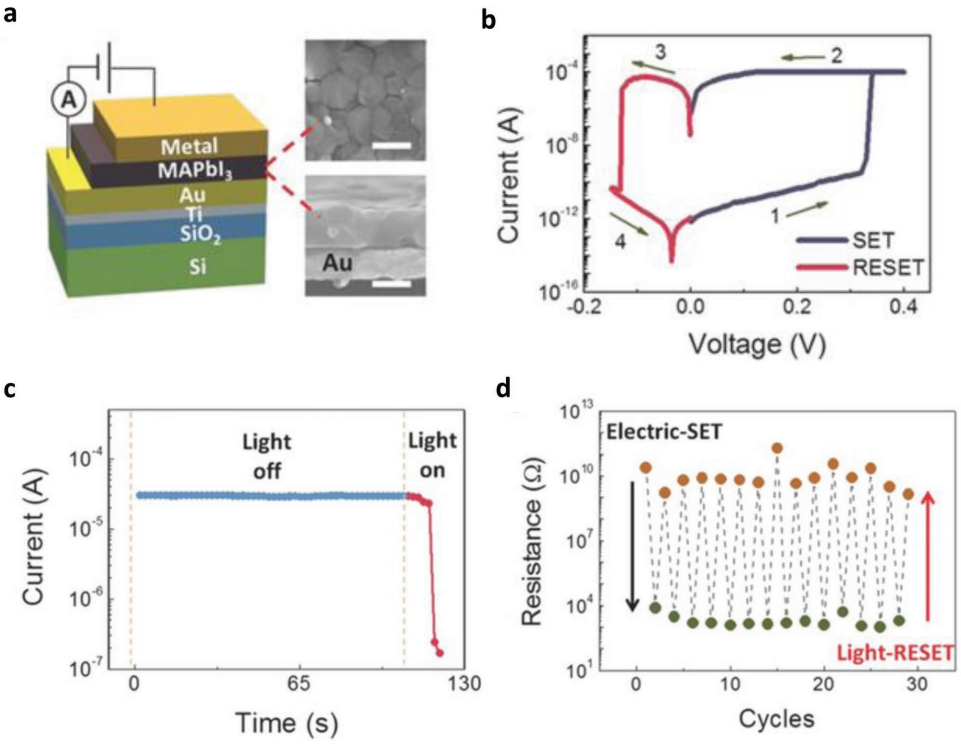

Figure 2. Resistive switching in MAPbI3. a) Schematic of the device structure with the measurement setup, and SEM image of the top and side view of the MAPbI3 film. b) Typical *I–V* measurement curve of the Au/MAPbI3/Au device. c) Device resistance evolution, measured at 0.1 V: for the first 105 s device is in dark and remain in LRS, followed by light illumination which switches device to HRS. d) Cycling of the electric-SET and light-RESET. All panels reproduced with permission.[26] Copyright 2017, Wiley-VCH.

especially for offline training[29] where the network nonidealities cannot be compensated in the training process. A group from MIT has explored a potential solution to reduce switching variabilities by utilizing crystalline materials as the switching layer and confining the active region to a 1D channel.[30] As shown in **Figure 3**a, a smartly designed device exploits threading dislocations in an epitaxial SiGe layer to restrict formation and rupture of Ag channels, resulting in linear analog switching with a large on/off ratio and enhanced uniformity as shown in Figure 3b,c, respectively. Simulated results show that the artificial neural network based on characteristics of such devices to perform supervised learning can have comparable accuracy to that obtained by software. More studies like this are needed to provide new directions for better engineering of memristive devices.

3. Diffusive Memristor

The hardware implementation of neuromorphic computing calls for emerging devices with biorealistic temporal dynamics.[11] Diffusive memristors with Ag active metal species are volatile threshold switches featuring the spontaneous rupture of conduction channels under zero bias. The unique temporal dynamics of the conductance evolution, originating from the underlying electrochemical and diffusive dynamics of the active metals, have enabled faithful emulation of synaptic plasticity with the relaxation process (spontaneous OFF switching).[7] The delay in metallic filament formation could simulate leaky integrate-and-fire and lead to unsupervised learning when paired with drift memristive synapses in a fully memristive neural network.[31]

To investigate the physics of the threshold switching, a planar Au/SiO_xN_y:Ag/Au diffusive memristor was fabricated with a nanogap (**Figure 4**a). The in situ TEM images (Figure 4b) show that the filament was formed with voltage induced electrochemical growth of Ag nanoparticles within the gap. After powered off, the conducting bridge of nanoparticles contracted from a wire to a sphere, implying that the minimization of the interfacial energy between the Ag nanoparticles and the dielectric serves as the driving force of the relaxation dynamics.

The diffusive memristor, in its vertical stack, has been used to emulate synaptic functions, with both short- and long-term synaptic plasticity demonstrated. It began with paired-pulse depression (PPD) and transitioned to paired-pulse facilitation (PPF) once the rate of the stimulation pulses was increased (**Figure 5**a). The facilitation was turned into depression by excessive high frequency pulses, which result in the gradual depletion of Ag at one electrode and accumulation at the other electrode. The depression was intensified with the reduced spiking frequency. In addition, being paired with nonvolatile drift memristors, STDP has been demonstrated, with nonoverlapping spikes, using the relaxation dynamics of the diffusive memristor, to time the interval between pre- and postsynaptic spikes. (Figure 5b)

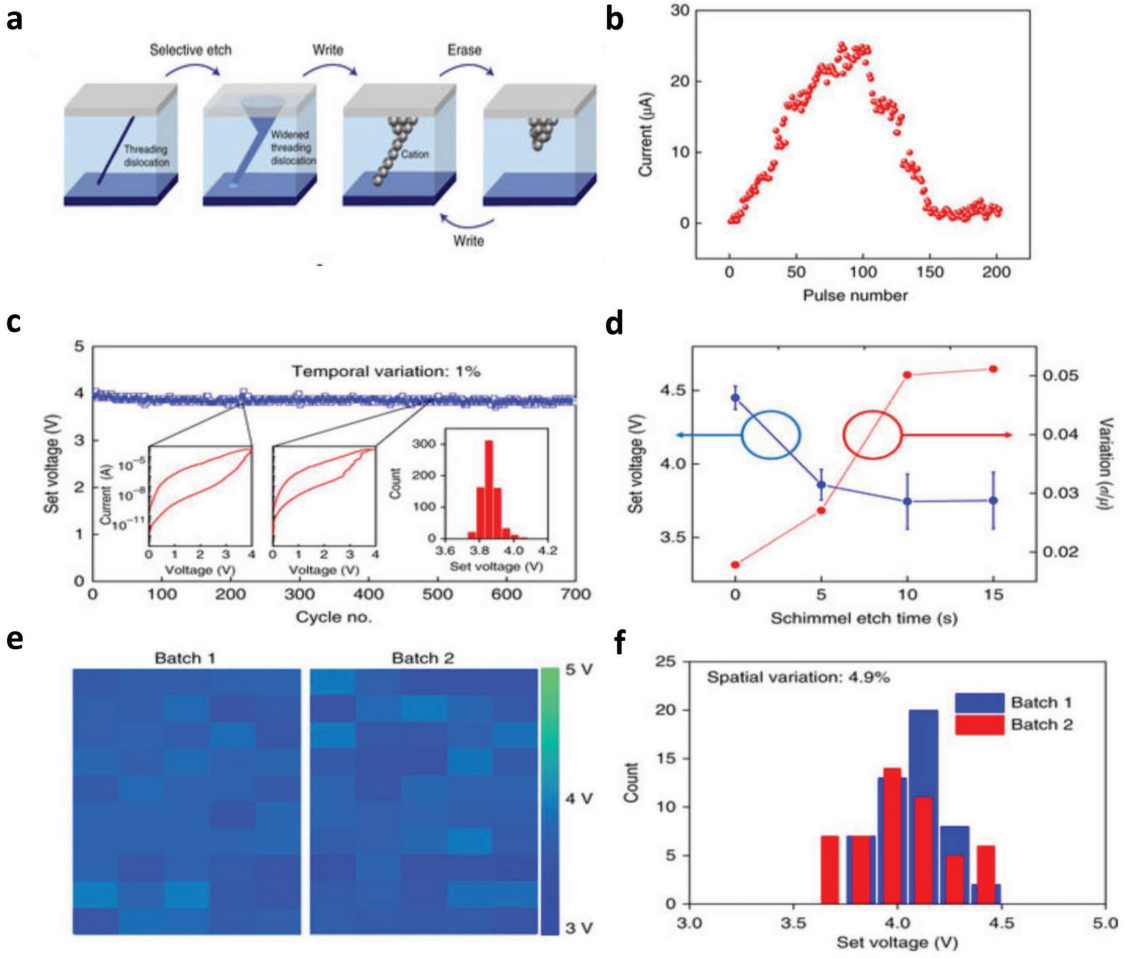

Figure 3. a) Cartoon of switching process in the epiRAM. b) Device shows linear potentiation and depression. c) Temporal variation of the epiRAM set voltage. d) Set voltage variation with respect to the defect-selective etch time. e) Colormap showing device-to-device set voltage variation. f) Histogram of the colormap shown in (e), showing spread of the set voltage. All panels reproduced with permission.[30] Copyright 2018, Springer Nature.

With sufficient parallel capacitance, the diffusive memristor could serve the role of an ion-channel near the neuron's soma, with membrane capacitance and axial resistance represented by a capacitor C_m and a resistor R_a. (**Figure 6**a) The charge up of membrane capacitance increases the voltage across the diffusive memristor. Once the threshold is reached, the diffusive memristor is switched ON, which discharges the capacitor (Figure 6b), mimicking the leaky integrate-and-fire behavior of biological neurons.

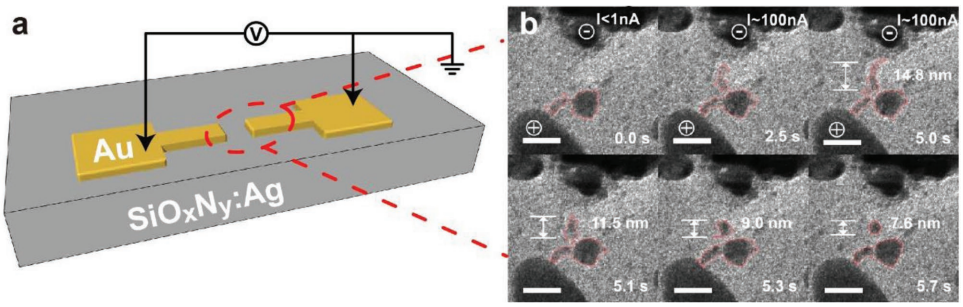

Figure 4. a) Schematic of a lateral Au/SiO_xN_y:Ag/Au diffusive memristor with two Au electrodes embedded in the dielectrics, and the measurement circuit. b) In situ TEM observation of the threshold switching of the lateral diffusive memristor. Voltage was applied at time zero. Ag nanocrystals formed and bridged the electrodes at 2.5 s. When the voltage was switched OFF at 5.0 s, the filament started to deform and shrink to a round spherical nanocluster, suggesting the relaxation is a diffusion process driven by interfacial energy minimization. All scale bars are 20 nm. All panels reproduced with permission.[7] Copyright 2017, Springer Nature.

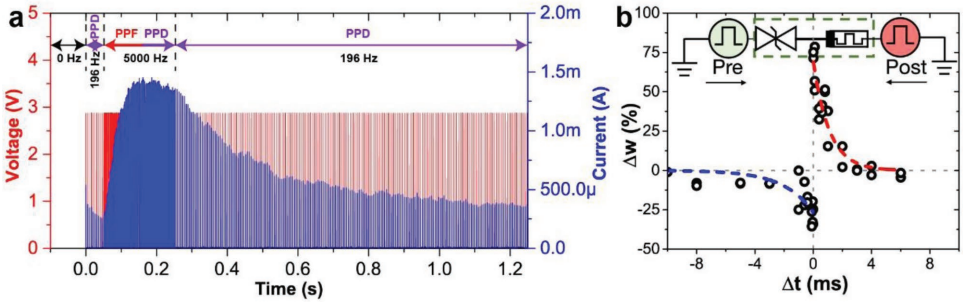

Figure 5. a) Experimental observation of short-term synaptic plasticity of the diffusive memristor. The device showed PPD upon low frequency stimulation and then PPF with increased stimulation frequency. The brief facilitation was followed by depression again because of the depletion of Ag. b) The conductance (weight) change of the drift memristor synapse in series with a diffusive memristor, as a function of the interval between pre and postsynaptic spikes, showing biorealistic STDP. All panels reproduced with permission.[7] Copyright 2017, Springer Nature.

A prototypical memristor neural network with diffusive memristor neurons and drift memristor synapses was built (**Figure 7**a),[31] where $Pd/HfO_2/Ta$ drift memristors were in series with accessing transistors (Figure 7b). The junction of diffusive memristor is illustrated in Figure 7c. With specially designed learning protocol and peripheral circuitry, unsupervised synaptic weight update was demonstrated with lateral inhibition between neurons to enhance the discrimination of the inputs (Figure 7d–f). The initial conductance of synapses concentrated around ≈100 µS. The synapses were programmed by the simple STDP rule and gained similarity with the means of input patterns which triggered firing of the associated neurons.

4. Phase Change Memory (PCM)

PCM devices rely on the resistivity difference between two phases of a chalcogenide material (phase change material): the crystalline phase (low resistivity) and the amorphous phase (high resistivity). PCM devices are among most mature devices discussed here and can be used as an electronic synapse.[32,33] SET operation of PCM devices can be made incremental by applying multiple SET pulses which incrementally crystallizes the high resistance amorphous phase. The challenge lies in achieving incremental RESET which tends to be an abrupt process as it involves melting and rapid cooling of the crystallized matrix. To address this issue two-PCM devices have been used as one synaptic device[34] to implement STDP. In this approach only SET (crystallization) operation is used in both PCM devices to implement either long-term depression (LTD) or long-term potentiation (LTP). Using this approach, Burr et al. experimentally demonstrated a three-layer neural network made-up of PCM synapses.[35]

The switching mechanism of PCM devices are well understood, therefore the direction of further scaling can be engineered depending on the application. High density integration of the device for neuromorphic application is of utmost importance, which needs small cell size. Since temperature plays a very important role in the resistance change of PCM devices, thermal management is a challenge, particularly for scaled devices. As reset current for the device is high, it poses another challenge in designing the selection device and scaling it. Stability of the amorphous state is determined by the kinetics of amorphous-to-crystalline-phase-transition, which creates an issue of resistance drift of the amorphous state.[36] The melt-quench process during the device RESET is the process that limits the device endurance, hence the applications should be designed such that the number of RESET operations are minimized.

As shown in **Figure 8**, Tuma et al. have recently proposed a PCM-based neuron where the evolution of the membrane

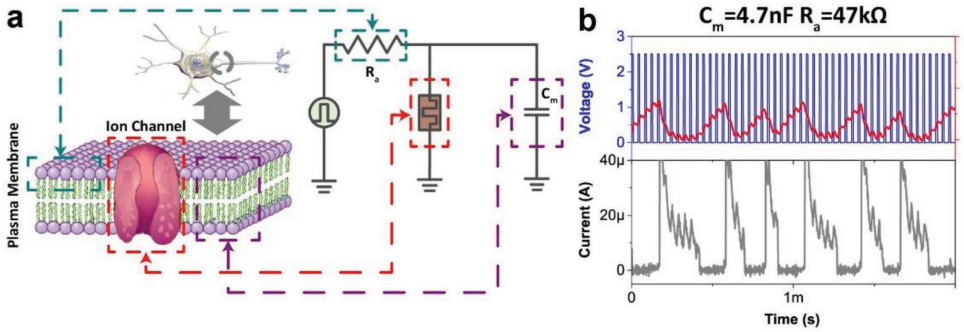

Figure 6. a) Illustration of the analogy between a biological neuron and a diffusive memristor-based artificial neuron. The presynaptic inputs are integrated on the capacitance of the membrane (or equivalently C_m) and the ion channel (or equivalently diffusive memristor) opens if the threshold condition is reached. b) Response of the integrate-and-fire circuit to consecutive presynaptic spikes. The current pulse across the diffusive memristor coincided with the discharge of the capacitor indicating that the circuit actively fired a pulse of stored charge. All pamels reproduced with permission.[31] Copyright 2018, Springer Nature.

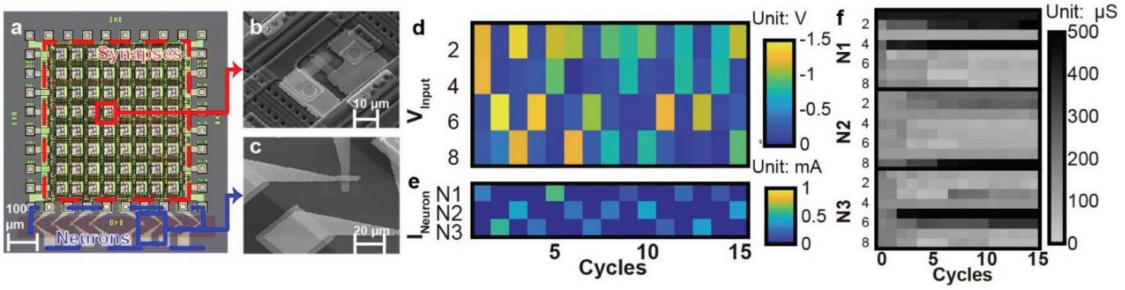

Figure 7. a) Optical image of the integrated memristive neural network. The 8 × 8 1-transistor-1-drift-memristor (1T1R) crossbar array interfaced with eight diffusive memristor artificial neurons with external capacitors. b,c) Scanning electron images of a single 1T1R cell and diffusive memristor junction, respectively. d–f) The input patterns (peak voltages of waveforms), peak neuronal currents, and synaptic weights at each training cycle of the unsupervised weight update. The weight of synapses was initially ≈100 μS and gained similarity with input patterns which triggered the plasticity of the associated neurons. All panels reproduced with permission.[31] Copyright 2018, Springer Nature.

potential in a biological neuron is mimicked by the crystal growth dynamics of the phase-change device.[38] Inherent stochastic dynamics of phase change devices has been exploited here to generate a distribution of the interspike intervals, leading to population-based coding. Furthermore, the proposed PCM-based neuron is used to detect temporal correlations within a large number of event-based data streams. A PCM-based synapse with STDP learning rules has also been demonstrated.[34] A complete PCM-based neuromorphic circuit which is made up of PCM-based neurons and PCM-based synapses has also been revealed.[39]

5. Ferroelectric Field-Effect Transistor

FeFET is a three-terminal device (FET), which uses a ferroelectric thin film as gate insulator. A ferroelectric material can be reversibly switched between the two remnant polarized states which could be used as two digital states of the memory. In principle, because of the Coulomb interaction between the ferroelectric polarization and the carriers in the channel, the carrier density is modulated depending on the polarization direction, which can be controlled in a nonvolatile manner by applying a gate voltage.[41] Ferroelectricity has been very extensively studied by the solid-state physicists,[42,43] which can be put to use for designing future ferroelectric memories.

Traditional ferroelectric materials contained lead,[10] i.e., lead zirconat titanate, PZT, which is hazardous to the environment, so there was an urgent need to develop a lead free, CMOS compatible ferroelectric material. The ferroelectric properties of thin HfO_2-based films were first revealed in 2011 by Böscke et al.[44] HfO_2 film shows ferroelectric properties when it is doped with Si,[44] Zr,[45] Y,[46] Al,[47] Gd,[48] Sr,[49] and La,[50] with calculated dose followed by a heat-treatment. The HfO_2 thin film is widely used as a high-k dielectric in MOSFETs with great CMOS compatibility.

The multidomain polarization switching capability of polycrystalline HZO (hafnium–zirconium–oxide) thin film can be utilized to tune the FeFET threshold voltage which in turn can modulate FeFET channel conductance. The FeFET channel's multiconductance levels can be used to record synaptic weight.[51,52] Recently, Jerry et al. demonstrated an FeFET-based synaptic device using $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as ferroelectric material.[53] The device structure is shown in **Figure 9**a upper panel, 10 nm HZO was ALD deposited as gate insulator and, afterward, the device was subjected to a 600 °C annealing which resulted in generating multiple ferroelectric domains. In this work, the multiferroelectric domain was partially polarized by applying appropriate voltage pulses as shown in lower panel of Figure 9a. The device conductance change in response to three different pulse schemes were studied (Figure 9b–d), where scheme 3 resulted in the highest number of analog states, i.e., 32 (5 bit), as well as symmetric potentiation and depression conductance change, a highly desirable feature for electronic synapses. STDP has also been demonstrated with FeFETs.[54,55]

Although FeFET demonstrates some promising features to be used as an electronics synapse, such as fast programming

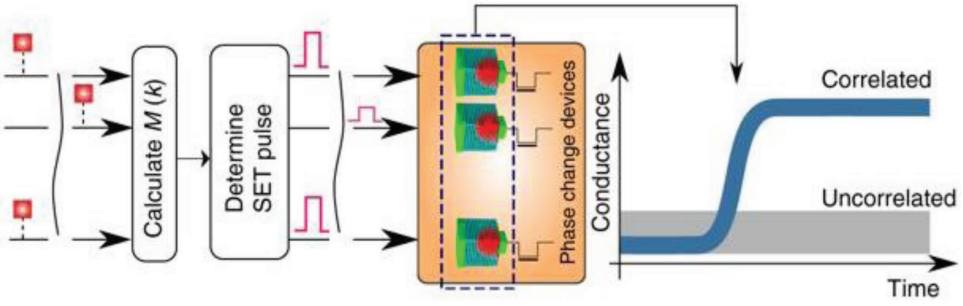

Figure 8. Correlation detection realized using phase change-based computational memory. Each process is fed to a single-phase change device which is SET if the process takes a value 1. The correlated group could be identified by monitoring the conductance of the memory devices. Reproduced with permission.[37] Copyright 2017, Springer Nature under the terms of the CC-BY Creative Commons Attribution 4.0 International License.

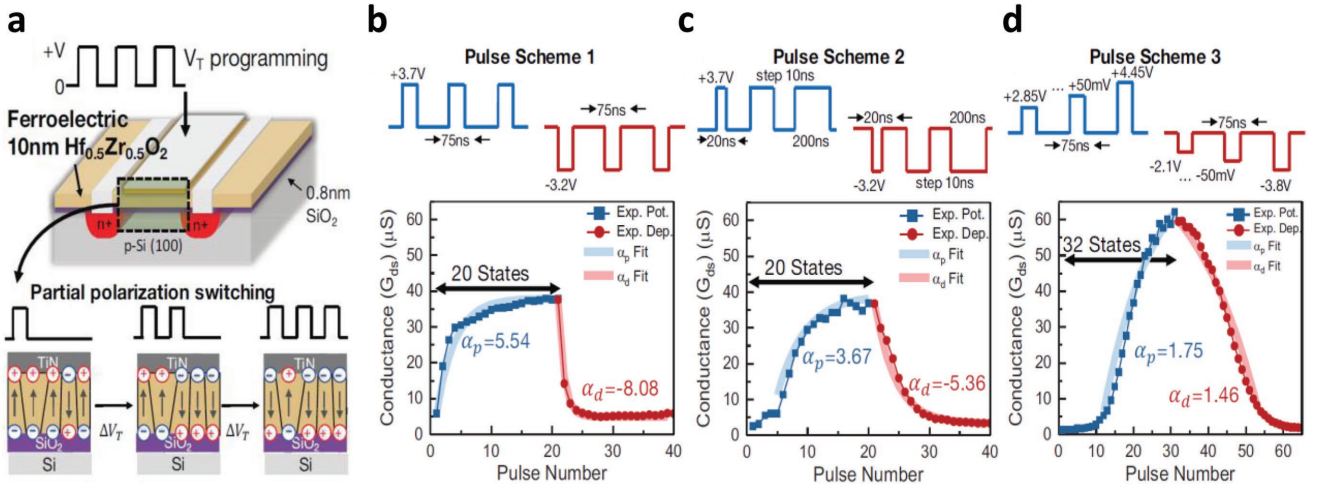

Figure 9. a) Device structure and its operating principle. Analog states were obtained by using partial polarization of the ferroelectric layer. Potentiation and depression plots for pulse schemes 1–3. b) Pulse scheme 1 has fixed amplitude train of pulses. c) Pulse scheme 2 has gradually increasing pulse width. d) Pulse scheme 3 has gradually increasing pulse amplitude. All panels reproduced with permission.[53] Copyright 2018, IEEE.

operations, symmetric potentiation and depression curves and large ON/OFF ratio, there are still a number of issues to be addressed. As devices need to be scaled down for high-density integration, the domain size should also be reduced proportionally to maintain the multilevel conductance capability of the device,[56] which might need new device engineering to retain the great analog behavior. The FeFET are charge-based memories and hence they suffer from the same scaling limitations as DRAM and floating gate memories do, i.e., increased cell leakage current, reduced cell reliability, increased manufacturing difficulties, reduced possibilities to significantly improve capacity/energy, reduced reliable sensing as charge storage unit size reduces, etc.

6. Spintronics Devices

Spintronics based MRAM, mainly consists of a tunneling oxide layer sandwiched by two metallic ferromagnetic layers: the free layer and the pinned layer. This trilayer structure is also called magnetic tunnel junction (MTJ). The spin polarization of the pinned layer is fixed in a particular direction, while the free layer magnetization can be altered using external current or magnetic field. Depending on whether the magnetization directions in the two layers are parallel or not, devices can exhibit a high resistance (opposite or antiparallel) state or a low resistance (parallel) state. The inherent stochasticity in switching time of these devices can be exploited to implement a stochastic synapse.[57]

Multiple resistance states in an MTJ device can be achieved by incorporating domain walls in its free layer. The domain wall separates two oppositely polarized magnetic domains. The device conductance can be modulated by moving this domain wall using spin-torque transfer (STT) phenomenon, which changes the relative proportions of parallel and antiparallel domain in the free layer by transferring spin-torque from spin-polarized stimulation currents. Based on this concept, Lequeux et al. have experimentally demonstrated a magnetic synapse using MgO (**Figure 10**) based multilevel STT-MTJ.[58] Recently, an all-spin neural network has been proposed in simulation.[59] In this network, both Neurons and synapse functionality can

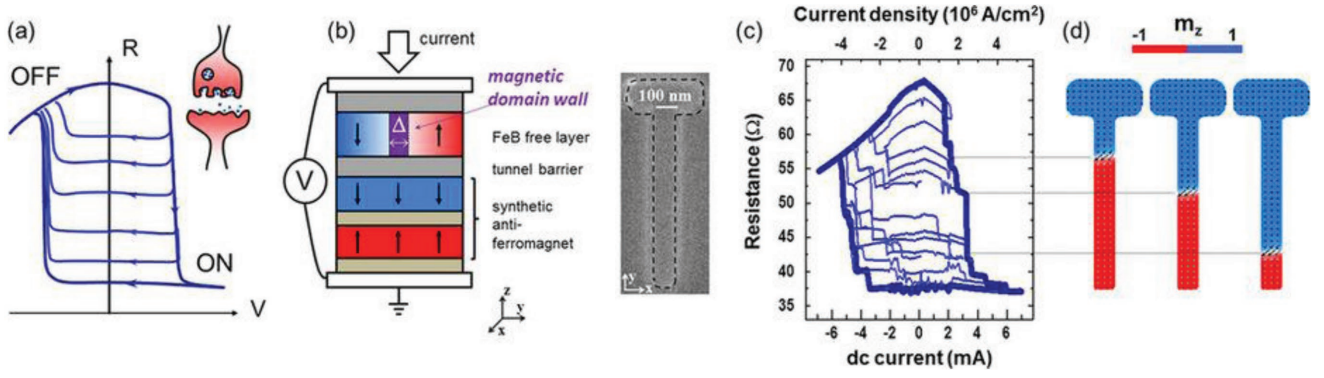

Figure 10. a) Typical resistance versus voltage characteristic of the device. b) Left panel shows schematic of the device material stack and right panel shows image of the sample. c) Plot showing resistance versus vertically injected DC current, measured at an external field Hz = 85 Oe. d) Micromagnetic simulations of the domain wall propagating in a magnetic track of 100 nm width. a–d) Reproduced with permission.[58] Copyright 2016, Springer Nature under the terms of the CC-BY Creative Commons Attribution 4.0 International License.

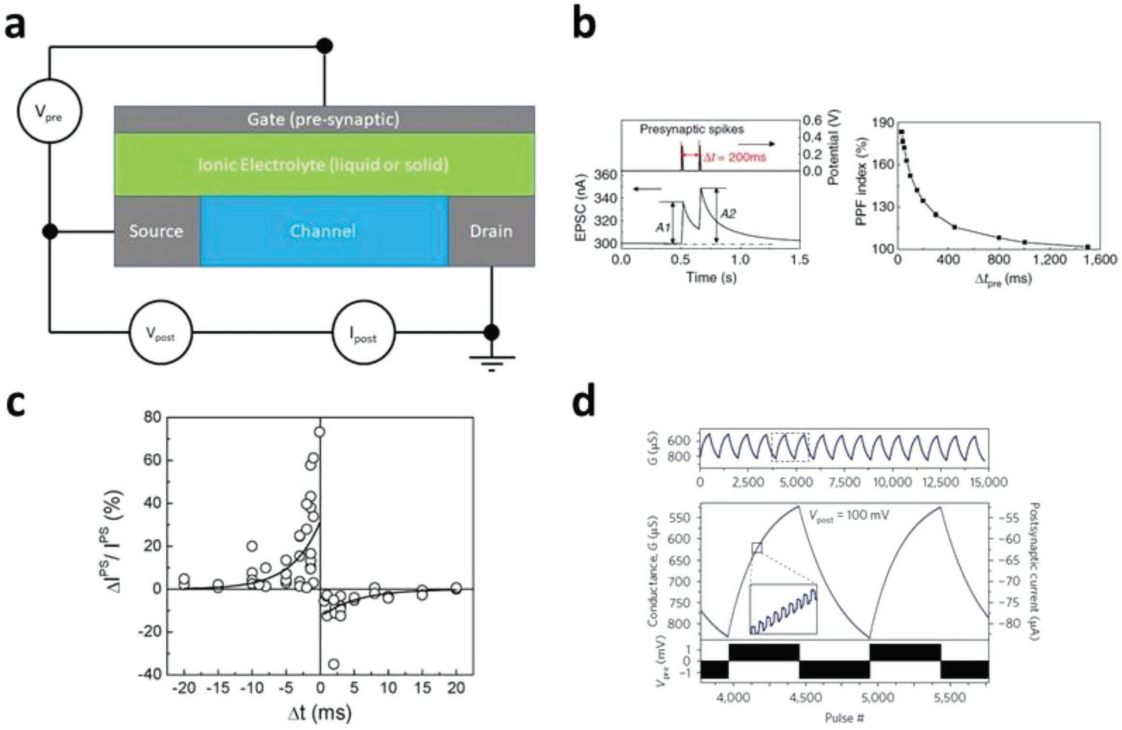

Figure 11. a) Schematic of a typical synaptic transistor. b) Left panel shows a pair of presynaptic pulses that triggered postsynaptic current spikes in an indium–zinc oxide-based synaptic transistor. The right panel shows the ratio of postsynaptic current spikes plotted versus inter-presynaptic pulse interval. b) Reproduced with permission.[58] Copyright 2016, Springer Nature. c) Spike time-dependent plasticity of an ionic-electronic hybrid-based synaptic transistor. Reproduced with permission.[70] Copyright 2010, Wiley-VCH. d) Long-term potentiation and depression of an ENODe device as a result of voltage pulses. Reproduced with permission.[73] Copyright 2012, Springer Nature.

be implemented by a single spintronic device which acts as a fundamental building block in the network. Using a magnetic-CMOS hybrid system, Mizrahi et al. have demonstrated neural-like population coding.[60] Borders et al. have shown associative memory operations using spin–orbit torque device.[61] They have used 36 individual spin devices in a circuit being controlled by an FPGA.

Although, till now single device level demonstration has been done in this direction, there are still a number of problems to be addressed for an array level implementation of neuromorphic system using spin devices. MRAMs show cycle to cycle and device to device variations, which could be a problem until it is brought down to a certain range tolerable by a neuromorphic system. Switching speed of these devices could be in the range of 5–10 ns, while energy consumption per operation could be as low as 100 fJ. Although the ON/OFF resistance ratio is not very high for these devices (≈5 at room temperature) compared to other emerging memories, theoretically their endurance could be infinite because there is no atomic motion occurring in the material structure during switching operations. Pertaining to the complicated material stack with multiple metal layers in the devices, the etching process may greatly impact device variability once scaled down. In addition, the dry etching option for Fe-containing magnetic layer is limited because of nonvolatile chemical reaction byproduct of Fe, which poses another challenge for scaling of the device.

Multiferroic tunnel junction (MFTJ) combines the properties of both MTJs and ferroelectric tunneling junctions (FTJs) by either replacing the tunnel barrier by a ferroelectric barrier in an MTJ structure[62] or by creating heterojunctions of the ferromagnetic and ferroelectric layers (artificial MFTJ)[63–65] These devices intrinsically exhibit multiresistance state and can be used as an electronic synapse.[66]

7. Synaptic Transistors

Three-terminal artificial synapses, structurally inspired by a transistor, have been under investigation for some time now for their potential application in a neuromorphic system. **Figure 11**a shows schematic of a typical synaptic transistor. Gate terminal (presynapse) is used to manipulate the conductance (synaptic weight) of the channel (postsynapse) that could either be volatile (short-term plasticity) or nonvolatile (long-term plasticity). This would mean decoupling write operation (modulating the synaptic weight using the gate terminal) from read operation (reading the synaptic weight using source–drain terminals) which is something the two-terminal memristive devices lack. Over the years, the operating mechanism that is responsible for conductance change has evolved from electric double layer[67] to ferroelectric[54] and battery-like.[68]

In electric double layer transistors (EDLTs), two layers of opposite charges accumulate on either side of the electrode (channel) and electrolyte (dielectric) interface under the influence of gate bias and in turn modifies channel conductance. Short-term plasticity (STP) such as PPF and PPD have

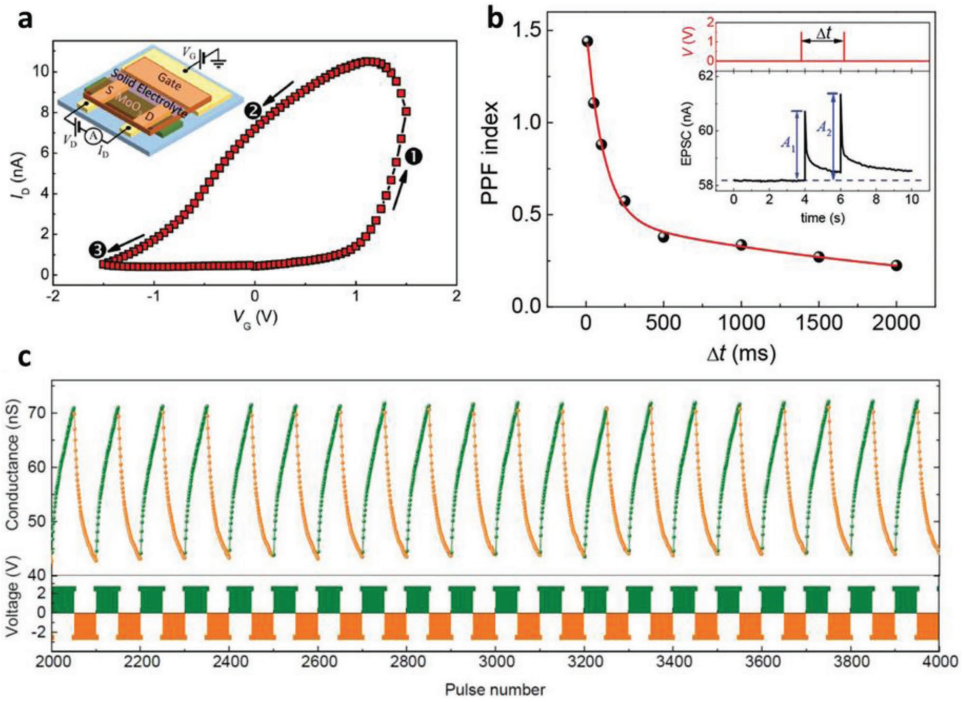

Figure 12. a) I_D–V_G characteristics of a typical three-terminal electrochemical transistor based on quasi-2D α-MoO_3. b) Short-term plasticity demonstration through paired pulse facilitation (PPF). c) Long-term potentiation and depression in MoO_3 conductance as a function of presynaptic pulses. All panels reproduced with permission.[74] Copyright 2018, Wiley-VCH.

been truly demonstrated by EDLTs[67,69] as shown in Figure 11b. They are also known to exhibit LTP such as STDP,[70,71] as shown in Figure 11c, and spike-rate dependent plasticity (SRDP).[72]

Lai et al. modulated a p-Si channel conductivity by modifying nonvolatile ionic charges in the polymer gated dielectric and demonstrated STDP.[70] Change in electrode conductance was harnessed while a battery charges and discharges in devices such as Li-ion synaptic transistor for analog computation[68] and electrochemical neuromorphic organic device (ENODe).[73] In a selective conductance range, a fairly linear potentiation and depression with identical presynaptic pulses has been obtained for neuromorphic computation as shown in Figure 11d. In addition, very high dynamic range with more than 200 nonvolatile conductive states has been demonstrated. Achieving all this at a mere cost of a few picojoules or even less has been very promising and a driving factor toward brain-inspired energy efficient neuromorphic computing.

A promising technology involving 2D van der Waals layered crystals or quasi-2D transition metal-oxide whose properties can be tuned with ion gating has been shown to exhibit both STP and LTP.[74–77] High-frequency pulses to the gate can transform the system from STP to LTP. This is attributed to lithium-ion intercalation into the channel that yields a nonvolatile state before they can diffuse back into the electrolyte (volatile behavior). These devices have shown almost linear potentiation and depression with multiple conductance states, SRDP, as well as very low energy consumption of 30 fJ per spike. Zhu et al. presented an ionic-gating-modulated synaptic transistor in which the channel is made-up of a 2D van der Waals layered crystal such as WSe_2, $NiPS_3$, and $FePSe_3$.[75] A challenge with this device is its very small conductance change (around 300 pS) which might pose a significant hurdle for its application in the real-world. John et al. proposed a molybdenum disulfide (MoS_2)-based three-terminal devices with three different gating approaches: electronic-mode, ionotronic-mode, and photoactive-mode.[78] Electronic only mode was used to demonstrate STP/STD, a train of pulses or optical stimuli could take the device state to achieve LTP/LTD and the three modes are combined to modulate Hebbian STDP plasticity. Classical conditioning was also demonstrated by using electronic and photoactive modes. Although this device shows some very interesting behaviors, its structure is very complex (e.g., having three different types of gate controls), which makes it very challenging to use these devices in an array. Another MoS_2-based three-terminal device having hybrid properties of both transistor and memristor (called memtransistor) has been proposed recently.[79] Switching is attributed to dynamic Schottky barrier modulation aided by defect kinetics. These MoS_2-based memtransistors have been demonstrated to exhibit heterosynaptic plasticity with multiple terminals. However, the operating voltages are impractical and need to be improved before harnessing the device functionality for a neuromorphic application.

Yang and co-workers[75] exploited the layered structure of α-MoO_3 to demonstrate LTP/STP with very low channel conductance while lithium reversibly intercalates into it. **Figure 12**a shows ID-VG characteristics of their electrochemical synaptic transistor. STP has been demonstrated with PPF (Figure 12b) and LTP as a function of presynaptic pulses is shown in Figure 12c. Sharbati et al.[77] used Li^+ ion intercalation/deintercalation in graphene, which is usually used as the anode of a battery, to realize plasticity using their three-terminal device.

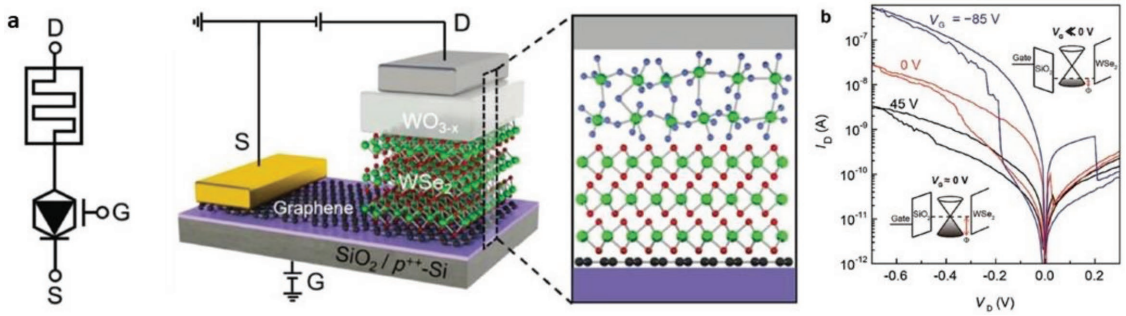

Figure 13. a) Device schematic of a synaptic barristor. b) I_D–V_D characteristics with three different cases of gate voltage. All panels reproduced with permission.[80] Copyright 2018, Wiley-VCH.

A very interesting concept and structure were presented in a work by Huh et al.[80] They demonstrated a 2D heterostructure-based three-terminal devices with an electrically modifiable energy barrier at the van der Waals interfaces, which was called the barristor. This device can be considered a gate controlled memristor composed of a $Ag/WO_{3-x}/WSe_2$-based resistive memory and a WSe_2/graphene-based barristor, whose schematic is shown in **Figure 13**a. As we know, the work function of graphene can be tuned electro-statistically, which produces a variable barrier of the Schottky diode at the WSe_2/graphene heterojunction. This gate-controlled variable-barrier Schottky diode can be used to control current flow through the entire device. I_D–V_D characteristics of this device is shown in Figure 13b. This device could implement some fundamental synaptic functions, including STP, PPF, LTP, and LTD. Although this device demonstrates a relatively better dynamic range of conductance, it does not show a gradual or linear change in conductance while performing potentiation or depression, which might be improved by using some other memristor in conjunction with the barristor. This device also needs very high gate control voltages which are not compatible with the current state of the art CMOS-based circuit boards. Alternatively, Shi et al.[71] demonstrated a synaptic transistor based on oxygen ion exchange between ionic liquid and a rare-earth nickelate. A comparison of various reports in this field is presented in **Table 1**.

Scalability of synaptic transistor devices could be of concern if the electrolytes used are ionic liquid or a gel-based.[71,75] However, this challenge may be tackled by introducing solid-state electrolytes such as poly(vinyl alcohol) (proton conductor)[76] and $LiClO_4$ in poly(ethylene oxide) (Li^+ ion conductor).[74,77] Despite exhibiting a great performance in some aspects, including surpassing the energy efficiency of biological synapses in some cases, these devices still face other obstacles to overcome, such as endurance, speed, and stability of electrolyte (especially of Li^+ ion based). In addition, there is still a lack of network level demonstration with these devices, which could raise some more issues such as sneak path problems and self-discharge. This could be mitigated by using access devices at the expense of area and energy efficiency. A better endurance might be achieved by improving the quality of thin films. The operation speed of the devices could be improved by enhancing the ion mobility with appropriate selections of ions and solid-state electrolytes and by shrinking the thickness of the thin films, with a potential risk of compromising the stability and other performance though.

8. Discussion and Conclusion

In this review, we have discussed the promising emerging devices that can be used to realize neurons and synapses in a neuromorphic system. Each of these devices has its own strengths and weaknesses. One type of devices can be preferred over the others depending on the requirements for a specific application. Although attempts have been made to implement logic circuits using emerging devices,[81] however, at least in the near future, neuromorphic systems still need the mature and reliable CMOS circuitry to implement peripheral components, which means neuromorphic systems and CMOS circuits will complement rather than replace each other. To make the neuromorphic system self-reliant these new device technologies must improve by leaps and bounds. There still exist areas for continued development, thus moving forward with a strong

Table 1. Material and performance comparison of different types of synaptic transistors.

Ion	Channel	Electrolyte	Switching energy	Conductance range	Work
Li^+	$LiCoO_2$	LiPON (solid)	–	180–230 µS	[68]
Li^+	MoO_3	$LiClO_4$:PEO (solid)	≈2 pJ	42–75 nS	[74]
Li^+	MoS_2	PVA (solid)	≈20 pJ	–	[76]
Li^+	Graphene	$LiClO_4$:PEO (solid)	≈500 fJ	100–1100 µS	[77]
Li^+	WSe_2	$LiClO_4$:PEO (gel)	≈30 fJ	260–570 pS	[75]
H^+	PEDOT:PSS/PEI	Nafion (solid)	≈10 pJ	525–825 µS	[73]
Ag^+	p-Si	$RbAg_4I_5$/MEH-PPV (solid)	≈10 pJ	–	[70]
O^{2-}	$SmNiO_3$	$(CF_3SO_2)C^-$ (liquid)	–	–	[71]

collaboration among material scientists, device engineers, hardware designers, computer architects, and programmers will help to facilitate the cross-disciplinary dialogue to solve many challenges being faced by neuromorphic community.

Although, our understanding of how the human brain functions are still very limited, the scientific community has used that limited knowledge to build some impressive brain-inspired systems, which will lead to much more powerful neuromorphic systems as our understanding of the human brain grows. As discussed in this paper, emerging memory devices could be used to build systems, which can emulate biological neural networks faithfully. These brains emulating systems can in turn help advancing neuroscience research. One good example of a similar research effort could be the European Human Brain Project.[82] A recent study to estimate the level of parallelism in the human brain using fMRI data, revealed interesting results.[83] In an abstract sense, this is like trying to figure out the number of "CPU cores" which is required to perform a task. Authors claimed that even for a complex visual-motor task, the number of independent brain processes is in the order of 50 to 60, which means an artificial brain-like cognitive system does not require a massively parallel connection at the single neuron level, but rather a cleverly designed set of limited processes which run in parallel at a much lower scale.

Today there are CMOS-based hardware accelerators available in the market, tailored to maximize the efficiency of AI-based computing, but they still face the von Neumann bottleneck (time and energy spent in moving data between memory and processor) and may have limited room for improvement. Therefore, a bold approach will be to eventually eliminate transistors and realize fully analog in-memory-computing, which may have the potential to significantly accelerate computing speed while reducing power consumption. To fully harness the computing power of the biological neural networks, a possible approach is to faithfully replicate the biological spiking neural networks (SNNs) with electronic building blocks. This requires that the artificial synapses and the neurons share similar dynamics with that of the biological counterparts. However, CMOS is not built for simulating temporal, neural, and synaptic behaviors, although it has been used to build SNNs with complicated circuits and high-power consumption. Therefore, new physics-based compact devices, such as diffusive memristors,[7] with intrinsic similarity to biological synapses and neurons at the physical level, might make it feasible and more efficient to replicate the biological neural network behaviors in a novel computing paradigm.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

artificial synapses, emerging memory technologies, memristors, neuromorphic systems, synaptic transistors

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[1] J. von Neumann, *IEEE Ann. History Comput.* **1993**, *15*, 27.
[2] G. E. Moore, *IEEE Solid-State Circuits Newsl.* **2006**, *11*, 33.
[3] J. Backus, *Commun. ACM* **1978**, *21*, 513.
[4] E. R. Kandel, J. H. Schwartz, T. M. Jessell, *Principles of Neural Science*, McGraw Hill, New York **2015**.
[5] N. K. Upadhyay, S. Joshi, J. J. Yang, *Sci. China Inf. Sci.* **2016**, *1*, 1.
[6] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat. Nanotechnol.* **2008**, *3*, 429.
[7] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G. L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.
[8] G. W. Burr, M. J. Breitwisch, M. Franceschini, D. Garetto, K. Gopalakrishnan, B. Jackson, B. Kurdi, C. Lam, L. A. Lastras, A. Padilla, B. Rajendran, S. Raoux, R. S. Shenoy, *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.* **2010**, *28*, 223.
[9] A. D. Kent, D. C. Worledge, *Nat. Nanotechnol.* **2015**, *10*, 187.
[10] N. Setter, D. Damjanovic, L. Eng, G. Fox, S. Gevorgian, S. Hong, A. Kingon, H. Kohlstedt, N. Y. Park, G. B. Stephenson, I. Stolitchnov, A. K. Taganstev, D. V. Taylor, T. Yamada, S. Streiffer, *J. Appl. Phys.* **2006**, *100*, 109901.
[11] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, *8*, 13.
[12] S. Pi, P. Lin, Q. Xia, *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.* **2013**, *31*, 06FA02.
[13] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, R. S. Williams, *Nano Lett.* **2009**, *9*, 3640.
[14] M. D. Pickett, R. Stanley Williams, *Nanotechnology* **2012**, *23*, 215202.
[15] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **2010**, *10*, 1297.
[16] A. Sawa, *Mater. Today* **2008**, *11*, 28.
[17] B. J. Choi, A. C. Torrezan, J. P. Strachan, P. G. Kotula, A. J. Lohn, M. J. Marinella, Z. Li, R. S. Williams, J. J. Yang, *Adv. Funct. Mater.* **2016**, *26*, 5290.
[18] K. Szot, W. Speier, G. Bihlmayer, R. Waser, *Nat. Mater.* **2006**, *5*, 312.
[19] K. Terabe, T. Hasegawa, T. Nakayama, M. Aono, *Nature* **2005**, *433*, 47.
[20] J. C. Scott, L. D. Bozano, *Adv. Mater.* **2007**, *19*, 1452.
[21] R. Waser, R. Dittmann, G. Staikov, K. Szot, F. Fake, F. Facke, F. Faik, *Adv. Mater.* **2009**, *21*, 2632.
[22] C. S. Hwang, *Adv. Electron. Mater.* **2015**, *1*, 1.
[23] Y. Yang, P. Gao, S. Gaba, T. Chang, X. Pan, W. Lu, *Nat. Commun.* **2012**, *3*, 732.
[24] A. Wedig, M. Luebben, D. Y. Cho, M. Moors, K. Skaja, V. Rana, T. Hasegawa, K. K. Adepalli, B. Yildiz, R. Waser, I. Valov, *Nat. Nanotechnol.* **2016**, *11*, 67.
[25] H. Jiang, L. Han, P. Lin, Z. Wang, M. H. Jang, Q. Wu, M. Barnell, J. J. Yang, H. L. Xin, Q. Xia, *Sci. Rep.* **2016**, *6*, 1.
[26] X. Zhu, J. Lee, W. D. Lu, *Adv. Mater.* **2017**, *29*, 1700527.
[27] M. Al-Shedivat, R. Naous, G. Cauwenberghs, K. N. Salama, *IEEE J. Emerging Select. Top. Circuits Syst.* **2015**, *5*, 242.

[28] T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, M. Aono, *Nat. Mater.* **2011**, *10*, 591.
[29] S. Yu, *Proc. IEEE* **2018**, *106*, 260.
[30] S. Choi, S. H. Tan, Z. Li, Y. Kim, C. Choi, P. Y. Chen, H. Yeon, S. Yu, J. Kim, *Nat. Mater.* **2018**, *17*, 335.
[31] Z. Wang, S. Joshi, S. Savel'ev, W. Song, R. Midya, Y. Li, M. Rao, P. Yan, S. Asapu, Y. Zhuo, H. Jiang, P. Lin, C. Li, J. H. Yoon, N. K. Upadhyay, J. Zhang, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Electron.* **2018**, *1*, 137.
[32] D. Kuzum, R. G. D. Jeyasingh, B. Lee, H. S. P. Wong, *Nano Lett.* **2012**, *12*, 2179.
[33] B. L. Jackson, B. Rajendran, G. S. Corrado, M. Breitwisch, G. W. Burr, R. Cheek, K. Gopalakrishnan, S. Raoux, C. T. Rettner, A. Padilla, A. G. Schrott, R. S. Shenoy, B. N. Kurdi, C. H. Lam, D. S. Modha, *ACM J. Emerging Technol. Comput. Syst.* **2013**, *9*, 1.
[34] M. Suri, O. Bichler, D. Querlioz, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, B. DeSalvo, *2011 IEEE Int. Electron Devices Meeting (IEDM)*, IEEE, Washington, DC **2011**, pp. 4.4.1–4.4.4.
[35] G. W. Burr, R. M. Shelby, S. Sidler, C. Di Nolfo, J. Jang, I. Boybat, R. S. Shenoy, P. Narayanan, K. Virwani, E. U. Giacometti, B. N. Kurdi, H. Hwang, *IEEE Trans. Electron Devices* **2015**, *62*, 3498.
[36] A. Pirovano, A. L. Lacaita, F. Pellizzer, S. A. Kostylev, A. Benvenuti, R. Bez, *IEEE Trans. Electron Devices* **2004**, *51*, 714.
[37] A. Sebastian, T. Tuma, N. Papandreou, M. Le Gallo, L. Kull, T. Parnell, E. Eleftheriou, *Nat. Commun.* **2017**, *8*, 1115.
[38] T. Tuma, A. Pantazi, M. Le Gallo, A. Sebastian, E. Eleftheriou, *Nat. Nanotechnol.* **2016**, *11*, 693.
[39] A. Pantazi, S. Woźniak, T. Tuma, E. Eleftheriou, *Nanotechnology* **2016**, *27*, 355205.
[40] Y. Nishitani, Y. Kaneko, M. Ueda, E. Fujii, A. Tsujimura, *Jpn. J. Appl. Phys.* **2013**, *52*, 04CE06.
[41] S. Y. Wu, *IEEE Trans. Electron Devices* **1974**, *21*, 499.
[42] L. D. Landau, *Zh. Eks. Teor. Fiz.* **1937**, *7*, 19.
[43] A. F. Devonshire, *London, Edinburgh Dublin Philos. Mag. J. Sci.* **1949**, *40*, 1040.
[44] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, U. Böttger, *Appl. Phys. Lett.* **2011**, *99*, 102903.
[45] J. Müller, T. S. Böscke, D. Bräuhaus, U. Schröder, U. Böttger, J. Sundqvist, P. Kcher, T. Mikolajick, L. Frey, *Appl. Phys. Lett.* **2011**, *99*, 0.
[46] S. Starschich, D. Griesche, T. Schneller, R. Waser, U. Böttger, *Appl. Phys. Lett.* **2014**, *104*, 202903.
[47] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, T. Mikolajick, *Adv. Funct. Mater.* **2012**, *22*, 2412.
[48] S. Mueller, C. Adelmann, A. Singh, S. Van Elshocht, U. Schroeder, T. Mikolajick, *ECS J. Solid State Sci. Technol.* **2012**, *1*, N123.
[49] T. Schenk, S. Mueller, U. Schroeder, R. Materlik, A. Kersch, M. Popovici, C. Adelmann, S. Van Elshocht, T. Mikolajick, *Eur. Solid-State Device Res. Conf.*, IEEE, Bucharest, Romania **2013**, pp. 260–263.
[50] J. Muller, T. S. Boscke, S. Muller, E. Yurchuk, P. Polakowski, J. Paul, D. Martin, T. Schenk, K. Khullar, A. Kersch, W. Weinreich, S. Riedel, K. Seidel, A. Kumar, T. M. Arruda, S. V. Kalinin, T. Schlosser, R. Boschke, R. Van Bentum, U. Schroder, T. Mikolajick, *Tech. Dig. – Int. Electron Devices Meeting (IEDM)*, IEEE, Washington, DC **2013**.
[51] H. Ishiwara, *Jpn. J. Appl. Phys.* **1993**, *32*, 442.
[52] S. Oh, T. Kim, M. Kwak, J. Song, J. Woo, S. Jeon, I. K. Yoo, H. Hwang, *IEEE Electron Device Lett.* **2017**, *38*, 732.
[53] M. Jerry, P. Y. Chen, J. Zhang, P. Sharma, K. Ni, S. Yu, S. Datta, *Tech. Dig. – Int. Electron Devices Meeting (IEDM)*, IEEE, San Francisco, CA **2018**, pp. 6.2.1–6.2.4.
[54] Y. Nishitani, Y. Kaneko, M. Ueda, T. Morie, E. Fujii, *J. Appl. Phys.* **2012**, *111*, 124108.
[55] Y. Kaneko, Y. Nishitani, M. Ueda, *IEEE Trans. Electron Devices* **2014**, *61*, 2827.
[56] H. Mulaosmanovic, S. Slesazeck, J. Ocker, M. Pesic, S. Muller, S. Flachowsky, J. Muller, P. Polakowski, J. Paul, S. Jansen, S. Kolodinski, C. Richter, S. Piontek, T. Schenk, A. Kersch, C. Kunneth, R. Van Bentum, U. Schroder, T. Mikolajick, *Int. Electron Devices Meeting (IEDM)*, IEEE, Washington, DC **2015**, pp. 26.8.1–26.8.3.
[57] A. F. Vincent, J. Larroque, N. Locatelli, N. Ben Romdhane, O. Bichler, C. Gamrat, W. S. Zhao, J. O. Klein, S. Galdin-Retailleau, D. Querlioz, *IEEE Trans. Biomed. Circuits Syst.* **2015**, *9*, 166.
[58] S. Lequeux, J. Sampaio, V. Cros, K. Yakushiji, A. Fukushima, R. Matsumoto, H. Kubota, S. Yuasa, J. Grollier, *Sci. Rep.* **2016**, *6*, 31510.
[59] A. Sengupta, Y. Shim, K. Roy, *IEEE Trans. Biomed. Circuits Syst.* **2016**, *10*, 1152.
[60] A. Mizrahi, T. Hirtzlin, A. Fukushima, H. Kubota, S. Yuasa, J. Grollier, D. Querlioz, *Nat. Commun.* **2018**, *9*, 1533.
[61] W. A. Borders, H. Akima, S. Fukami, S. Moriya, S. Kurihara, Y. Horio, S. Sato, H. Ohno, *Appl. Phys. Express* **2017**, *10*, 013007.
[62] M. Gajek, M. Bibes, A. Barthélémy, K. Bouzehouane, S. Fusil, M. Varela, J. Fontcuberta, A. Fert, *Phys. Rev. B: Condens. Matter Mater. Phys.* **2005**, *72*, 296.
[63] R. Soni, A. Petraru, H. S. Nair, O. Vavra, M. Ziegler, S. K. Kim, D. S. Jeong, H. Kohlstedt, *Nanoscale* **2016**, *8*, 10799.
[64] D. Pantel, S. Goetze, D. Hesse, M. Alexe, *Nat. Mater.* **2012**, *11*, 289.
[65] V. Garcia, M. Bibes, L. Bocher, S. Valencia, F. Kronast, a. Crassous, X. Moya, S. Enouz-Vedrenne, A. Gloter, D. Imhoff, C. Deranlot, N. D. Mathur, S. Fusil, K. Bouzehouane, a. Barthélémy, *Science* **2010**, *327*, 1106.
[66] W. Huang, Y. W. Fang, Y. Yin, B. Tian, W. Zhao, C. Hou, C. Ma, Q. Li, E. Y. Tsymbal, C. G. Duan, X. Li, *ACS Appl. Mater. Interfaces* **2018**, *10*, 5649.
[67] L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi, Q. Wan, *Nat. Commun.* **2014**, *5*, 3158.
[68] E. J. Fuller, F. El Gabaly, F. Lïonard, S. Agarwal, S. J. Plimpton, R. B. Jacobs-Gedrim, C. D. James, M. J. Marinella, A. A. Talin, *Adv. Mater.* **2017**, *29*, 1604310.
[69] K. Kim, C. L. Chen, Q. Truong, A. M. Shen, Y. Chen, *Adv. Mater.* **2013**, *25*, 1693.
[70] Q. Lai, L. Zhang, Z. Li, W. F. Stickle, R. S. Williams, Y. Chen, *Adv. Mater.* **2010**, *22*, 2448.
[71] J. Shi, S. D. Ha, Y. Zhou, F. Schoofs, S. Ramanathan, *Nat. Commun.* **2013**, *4*, 2676.
[72] Y. Yang, J. Wen, L. Guo, X. Wan, P. Du, P. Feng, Y. Shi, Q. Wan, *ACS Appl. Mater. Interfaces* **2016**, *8*, 30281.
[73] Y. Van De Burgt, E. Lubberman, E. J. Fuller, S. T. Keene, G. C. Faria, S. Agarwal, M. J. Marinella, A. Alec Talin, A. Salleo, *Nat. Mater.* **2017**, *16*, 414.
[74] C. Sen Yang, D. S. Shang, N. Liu, E. J. Fuller, S. Agrawal, A. A. Talin, Y. Q. Li, B. G. Shen, Y. Sun, *Adv. Funct. Mater.* **2018**, *28*, 1804170.
[75] J. Zhu, Y. Yang, R. Jia, Z. Liang, W. Zhu, Z. U. Rehman, L. Bao, X. Zhang, Y. Cai, L. Song, R. Huang, *Adv. Mater.* **2018**, *30*, 1800195.
[76] J. Jiang, J. Guo, X. Wan, Y. Yang, H. Xie, D. Niu, J. Yang, J. He, Y. Gao, Q. Wan, *Small* **2017**, *13*, 1700933.
[77] M. T. Sharbati, Y. Du, J. Torres, N. D. Ardolino, M. Yun, F. Xiong, *Adv. Mater.* **2018**, *30*, 1802353.
[78] R. A. John, F. Liu, N. A. Chien, M. R. Kulkarni, C. Zhu, Q. Fu, A. Basu, Z. Liu, N. Mathews, *Adv. Mater.* **2018**, *30*, 1800220.
[79] V. K. Sangwan, H. S. Lee, H. Bergeron, I. Balla, M. E. Beck, K. S. Chen, M. C. Hersam, *Nature* **2018**, *554*, 500.
[80] W. Huh, S. Jang, J. Y. Lee, D. Lee, D. Lee, J. M. Lee, H. G. Park, J. C. Kim, H. Y. Jeong, G. Wang, C. H. Lee, *Adv. Mater.* **2018**, *30*, 1801447.
[81] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, R. S. Williams, *Nature* **2010**, *464*, 873.
[82] *Human Brain Project*, https://www.humanbrainproject.eu/en/.
[83] H. V. Georgiou, *Artificial Intelligence*, **2014**, pp. 0–10, http://arxiv.org/abs/1410.7100.