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All-memristive neuromorphic computing with level-tuned neurons

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Abstract

In the new era of cognitive computing, systems will be able to learn and interact with the environment in ways that will drastically enhance the capabilities of current processors, especially in extracting knowledge from vast amount of data obtained from many sources. Brain-inspired neuromorphic computing systems increasingly attract research interest as an alternative to the classical von Neumann processor architecture, mainly because of the coexistence of memory and processing units. In these systems, the basic components are neurons interconnected by synapses. The neurons, based on their nonlinear dynamics, generate spikes that provide the main communication mechanism. The computational tasks are distributed across the neural network, where synapses implement both the memory and the computational units, by means of learning mechanisms such as spike-timing-dependent plasticity. In this work, we present an all-memristive neuromorphic architecture comprising neurons and synapses realized by using the physical properties and state dynamics of phase-change memristors. The architecture employs a novel concept of interconnecting the neurons in the same layer, resulting in level-tuned neuronal characteristics that preferentially process input information. We demonstrate the proposed architecture in the tasks of unsupervised learning and detection of multiple temporal correlations in parallel input streams. The efficiency of the neuromorphic architecture along with the homogenous neuro-synaptic dynamics implemented with nanoscale phase-change memristors represent a significant step towards the development of ultrahigh-density neuromorphic co-processors.

Keywords: neuromorphic systems, computational nanotechnology, phase-change devices

1. Introduction

The capabilities of future information-processing systems will involve learning, performing computations and responding in real time on huge volumes of data. Deriving inspiration from the highly efficient biological neural system is the key aspect of the emerging neuromorphic computing paradigm [1, 2]. Similar to biology, in these systems, memory and logic coexist at the same physical location, overcoming the classical von Neumann limitations. Typical implementations of neuromorphic computing architectures are spiking neural networks (SNNs), in which neurons upon sufficient excitation generate a signal called spike [3]. The

spikes propagate asynchronously through multi-neuron and multi-layer network topologies. Learning rules, such as spike-timing-dependent plasticity (STDP), are employed to modify the strength of the corresponding synapses as a function of the relative timing of their pre- and postsynaptic spikes [4, 5]. Computational power is enhanced by competitive winner-take-all network realizations [6–8]. In these schemes, only a winning neuron is allowed to spike at a given time, and the other neurons are suppressed. Such network architectures are explored for information-processing tasks, including pattern recognition and classification [9, 10]. Future emerging applications, like data-centric computing and knowledge extraction from big data sources, demand further research on enhanced and energy-efficient neural architectures.

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Major benefits in terms of density, circuit integration and power dissipation can be gained by using nanoscale memristive devices to emulate the neuro-synaptic dynamics [11–14]. Phase-change memristors in particular have been used for the realizations of nanoscale synapses, demonstrating the implementation of STDP [15, 16]. Recently, a memristor-based neuron in which the membrane potential is stored in the atomic configuration of a phase-change device was demonstrated, thereby implementing the integrate-and-fire (IF) of an artificial neuron [17]. Exploiting the physics of these nano-devices lays the foundations for the realization of compact large-scale neural networks. For example, phase-change devices were integrated into artificial neural network architectures implementing the synaptic weight element [18]. Furthermore, research studies have demonstrated the potential of memristor-based SNN architectures mainly using memristor models and software simulations [19]. We have recently presented a neuromorphic architecture using a single spiking neuron and an array of hardware phase-change-based synapses performing unsupervised learning tasks [20].

In this paper, we introduce an all-memristive SNN neuromorphic computing architecture. Phase-change memristors are incorporated into the architecture implementing the IF functionality of the neurons as well as the plasticity of the synaptic elements. The neuron's internal information is exploited in the neural network interconnection to generate sets of level-tuned neurons. The level-tuned neurons demonstrate selectivity related to the input signals. In this mechanism, the selection of the winning neuron is based on characteristics of the input pattern. The proposed phase-change-based SNN architecture is used for the task of unsupervised learning of multiple temporal correlations in parallel input streams. In addition, we present experimental results of continuous learning and detecting image patterns in the presence of noise.

2. All-memristive single-neuron computational primitive

The main computational unit in SNNs is a single spiking neuron that processes the incoming information through a large number of synaptic connections. Here, we present a realization of this computational primitive using phase-change devices that implement the core of the neuro-synaptic dynamics. Figure 1 shows a schematic illustration of an all-memristive computational primitive. The key computational unit is an artificial phase-change-based neuron. The neuron is of the IF type and its main element, the neuronal membrane, is emulated with a phase-change cell. The membrane potential is evolving according to the total postsynaptic potential (tPSP) generated by the neuronal input signals. The postsynaptic potentials are provided by the phase-change synapses that weight the spike-based presynaptic signals. A feedback mechanism in the form of STDP is responsible for tuning the synaptic weights, here emulated by phase-change cells. The computational primitive constitutes the main building block for large, dense and highly efficient SNN

implementations. The use of phase-change neuron and synapses aims to leverage the key features of this technology, naming, low latency, nanoscale dimensions, inherent plasticity and high scalability [21, 22]. Phase-change materials have two stable states with high resistivity contrast, namely, the crystalline (low resistivity, SET) and the amorphous (high resistivity, RESET) state. The fundamental current–voltage characteristic of a phase-change cell enables the programming between the two states and is depicted in 2(a). From the amorphous state, the current increases with the voltage in a nonlinear way. When the voltage reaches a critical value, the cell resistivity drops drastically and the cell is in the dynamic ON state in which programming occurs. From the crystalline state, the current–voltage characteristic follows a highly conductive path. Intermediate states between the amorphous and crystalline configurations can be programmed and the stored information is reflected in the current–voltage characteristics as depicted in figure 2(a) [23, 24].

Next, in this section, we describe how the phase-change physical properties can be used to emulate the required features of neurons and synapses in the computational primitive implementation. Experimental results of the neuro-synaptic operation using phase-change devices are provided. The experiments were performed using mushroom-type cells with doped $\text{Ge}_2\text{Sb}_2\text{Te}_5$ as the phase-change material situated between a wide top and a narrow bottom electrode, as is schematically depicted in figure 2(b) [23, 25]. The bottom electrode was created via a sub-lithographic key-hole process [26]. The study is performed using a prototype phase-change chip consisting of 2×2 Mcells integrated in 90 nm CMOS technology [27]. The chip, illustrated in 2(c), contains in addition the addressing circuit, an on-chip ADC for cell readout and the write driver circuitry for cell programming. The neuromorphic computing architectures are implemented in an experimental platform that combines a software-based environment and an FPGA with an embedded processor that controls the phase-change prototype chip. The hardware platform further comprises off-chip peripherals such as power supplies, reference voltages and external DACs. Finally, a data acquisition module is implemented in the FPGA for device characterization and real-time data collection and processing [28].

2.1. Phase-change neurons

In a phase-change neuron, the neuronal membrane potential is stored in the phase configuration within the nanoscale device. The possibility of programming the cells in different intermediate amorphous/crystalline configurations using the crystal growth dynamics is exploited to emulate the evolution of the neuronal membrane potential. The membrane potential is updated by electrical pulses whose amplitude and/or duration are based on the strength of the tPSP signal (depicted in figure 1, inset (a)). Successive application of these crystallizing pulses progressively reduces the amorphous region and increases the cell conductance. This inherent accumulation feature of the phase-change materials provides the physical means for implementing a simplified form of an IF

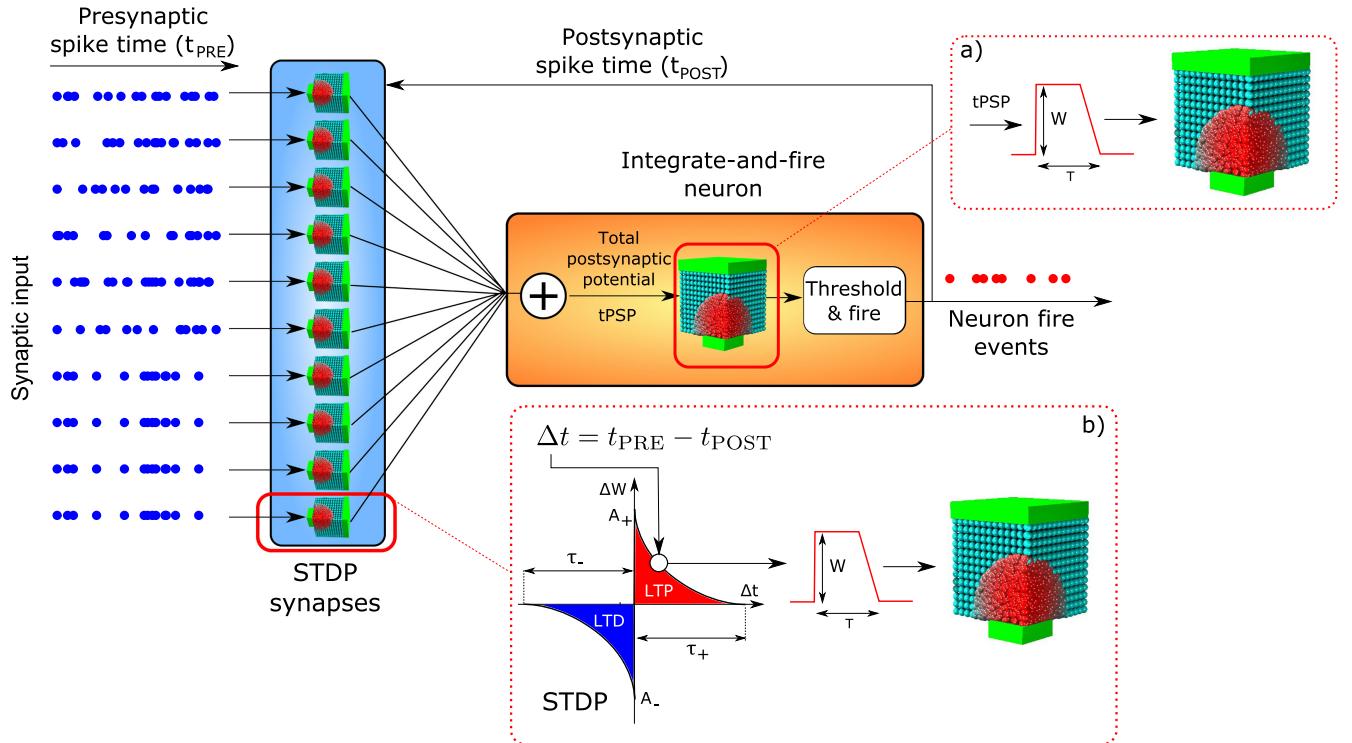


Figure 1. Schematic illustration of an all-memristive computational primitive. The neuronal membrane potential and the synaptic weights are emulated in the phase configuration of nanoscale phase-change devices. This single neuron phase-change-based primitive constitutes the main building block for high-density nanoscale SNN implementations.

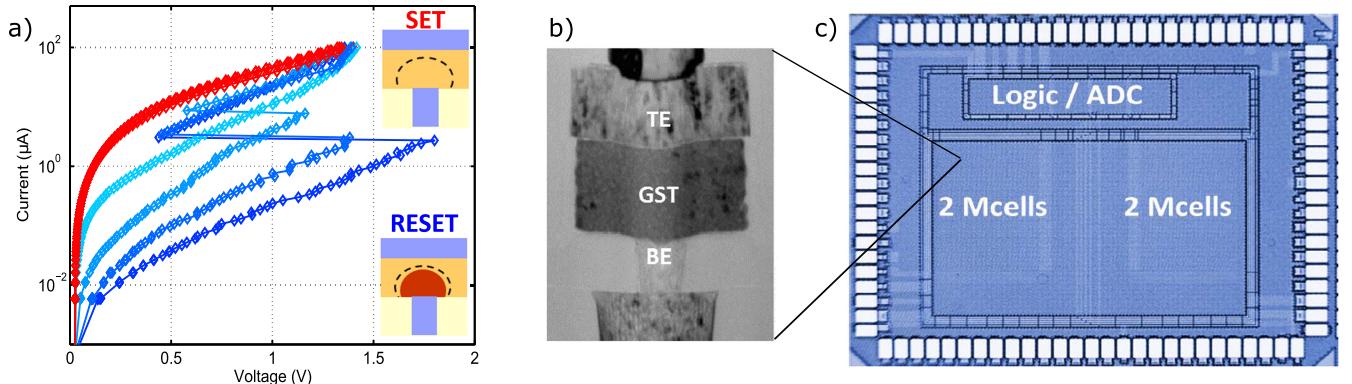


Figure 2. (a) Measured current–voltage characteristics of a typical phase-change cell. (b) Transmission electron micrograph of a phase-change mushroom cell. (c) Photograph of the 2×2 Mcells prototype chip.

neuron [17]. Neuron firing occurs once the cell conductance crosses a given threshold value. Subsequently, a high power pulse with an abrupt cut-off (reset pulse) re-creates the amorphous region through the melting and quenching process.

Experimental results using an array of phase-change cells are shown in figure 3. Specifically, figure 3(a) shows the evolution of the average cell conductance G of a population of neurons as a function of the number of crystallizing pulses applied. After a certain number of input pulses, the conductance increase causes the membrane potential to cross the firing threshold and trigger a postsynaptic spike generation. As shown in figure 3(a), the conductance gradient increases with the duration of the crystallizing pulse. In the neuron

implementation, the strength of the tPSP signal determines the duration of the crystallizing pulse, thereby firing is more frequent when the cumulative action of the presynaptic spikes is higher. Figure 3(b) shows the average firing response of a population of phase-change neurons as a function of the applied pulse width for a periodic input excitation. Specifically, for a range of pulse widths, we measured the average number of pulses required for a neuron firing event in response to a sequence of pulses of fixed period. The average firing frequency is determined by the inverse of the interspike interval. As shown in figure 3(b), the firing frequency is an approximately linear function of the pulse width and saturates for high values of the applied pulse duration. Note that the characteristics of the phase-change neuron firing response can

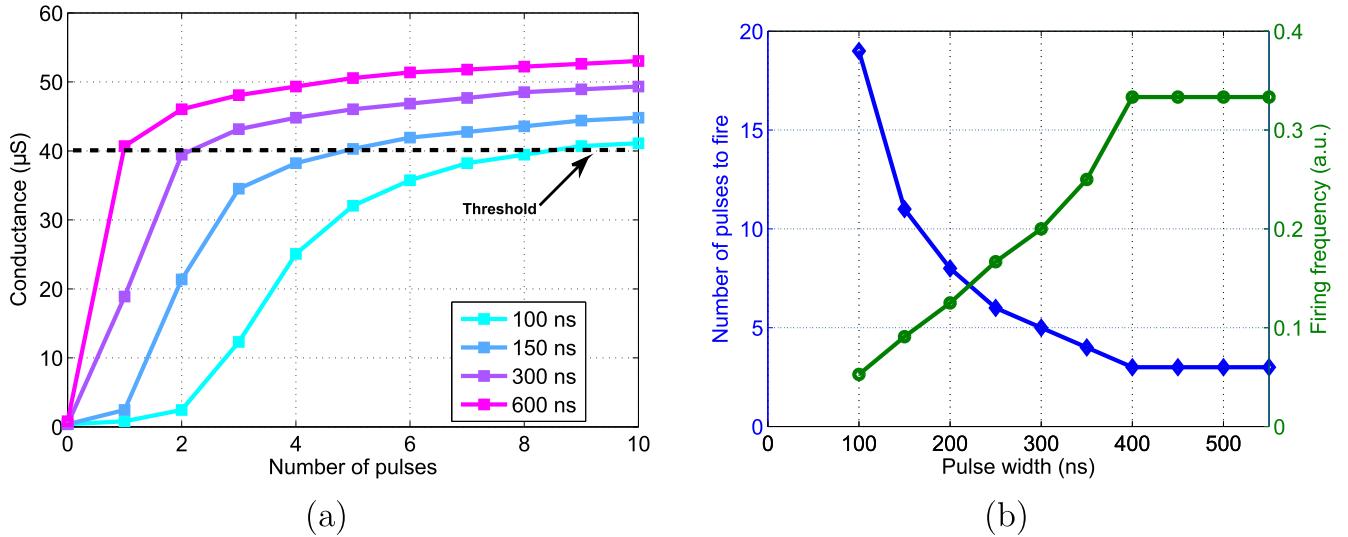


Figure 3. Experimental realization of phase-change neuronal dynamics. (a) Evolution of the average cell conductance of a sample population of 400 neurons as a function of the number of the applied crystallizing pulses. The number of pulses required for a neuron firing event is a function of the pulse duration for a given power. The amplitude of the crystallizing pulse current was set to $130 \mu\text{A}$. After application of the crystallizing pulse the cell conductance was measured at a constant read voltage of 200 mV . (b) Average firing rate response of a sample population of 400 neurons as a function of a fixed pulse-width input. The firing frequency is an approximately linear function of the crystallizing pulse width.

be tuned by modulating the crystallizing pulse power. Here, a crystallizing pulse with an average power of less than $100 \mu\text{W}$ was used for each membrane potential update.

2.2. Phase-change synapses

Besides the neuronal IF functionality, the continuous state evolution of the phase-change cell configuration provides the key requirement for the weight changes of an analog synapse implementation. A learning mechanism is responsible for adjusting the synaptic weight empowering the synaptic elements with computational features along with the memory storage. In a phase-change synapse, the synaptic weight is encoded in the cell conductance altered by modulating the pulse width applied to the cell (depicted in figure 1, inset (b)). Figure 4(a) shows the experimentally measured average conductance as a function of the width of the crystallizing pulse and the initial state of the cell. We observe a gradual increase in the conductance as a function of the applied pulse duration. Furthermore, we notice that the effective change in conductance is an inherent function of the actual cell state and the increase becomes smaller as the conductance reaches its maximum. Specifically, this property relates to the crystal-growth dynamics of the phase-change material, modeled by

$$\frac{du_a(t)}{dt} = -v_g(T_{\text{int}}(u_a)), \quad (1)$$

where the rate of change of the amorphous thickness u_a is determined by the temperature-dependent crystal-growth velocity v_g [29]. The temperature T_{int} at the interface between amorphous and crystalline regions is a recurrent function of u_a and is given by $T_{\text{int}} = P_{\text{inp}} R_{\text{th}}(u_a) + T_{\text{amb}}$, where T_{amb} is the ambient temperature, P_{inp} the input pulse power and R_{th} the thermal resistance of the phase-change cell. The inherent

feedback in the crystal-growth dynamics, as also verified experimentally, enables practical implementations of learning mechanisms enhanced with weight-dependent features.

Traditionally, SNNs use STDP as a learning mechanism that produces a change in the synaptic weight Δw taking into account the relative timing of individual signals occurring at both sides of the synapse. Specifically, $\Delta w = f(\Delta t)$ is expressed as a function of the difference $\Delta t = t_{\text{post}} - t_{\text{pre}}$ in the timing of the pre- and postsynaptic spikes. The magnitude of the weight change is often approximated as an exponential function: $f(\Delta t) = A_{\pm} e^{-|\Delta t|/\tau_{\pm}}$ [30]. A plot of the STDP rule, known as additive STDP because of its weight independency, is schematically depicted in figure 1, inset (b). The STDP learning function $f(\Delta t)$ strengthens the synaptic weight when $\Delta t > 0$, meaning that the presynaptic neuron spikes before the postsynaptic neuron, and vice versa. During operation of the additive STDP rule, it is desirable to keep the weights bounded within an interval to avoid unlimited weight increase and destabilization of the neural system. Alternatively, a weight dependence can be added in the STDP rule, as shown in (2), where the weight dependence has the form of a power law with an exponent $\mu > 0$ and the weight w is normalized to $[0, 1]$:

$$g(\Delta t, w) = \begin{cases} (1-w)^{\mu} f(\Delta t) & \text{if } \Delta t > 0 \\ w^{\mu} f(\Delta t) & \text{if } \Delta t \leq 0 \end{cases}. \quad (2)$$

In weight-dependent STDP, the amount of synaptic modification, either potentiation or depression, decreases as the weight approaches the boundary conditions. For example, figure 4(b) shows the synaptic weight values with the occurrence of multiple consecutive inputs corresponding to a fixed Δt value for the additive and weight-dependent updates. It has been demonstrated that the weight-dependent synaptic updates are

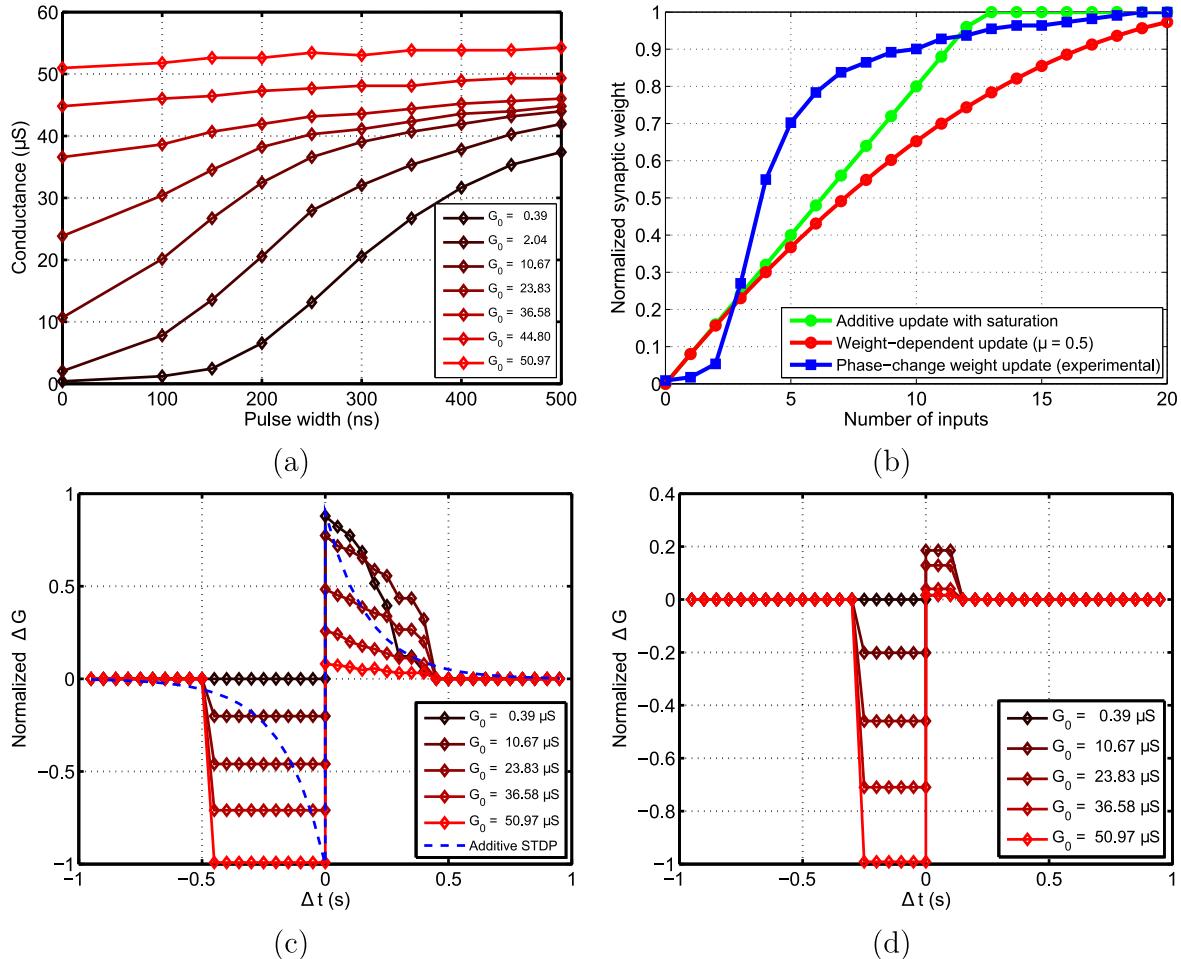


Figure 4. Experimental realization of phase-change synaptic dynamics. (a) Evolution of cell conductance as function of the width of the crystallizing pulse for various initial cell states. The data were obtained by averaging the measurements from 400 phase-change cells. The amplitude of the crystallizing pulse current was set to $130 \mu\text{A}$. After application of the crystallizing pulse the cell conductance was measured at a constant read voltage of 200 mV . (b) Evolution of synaptic weight changes with the occurrence of a fixed pre/post spike configuration for linear, weight-dependent and phase-change STDP realizations. (c) Phase-change STDP realization with the causal part emulating classical STDP characteristics using crystallizing pulses. In the acausal part of the learning, a reset pulse always initializes the synaptic weight. (d) Simplified form of the phase-change STDP requiring a constant-width crystallizing pulse.

essential for SNN systems with efficient and stable learning characteristics [31]. Simulation studies have shown ways to implement memristor-based STDP rules following additive or multiplicative updates [32, 33]. Phase-change synapses, because of their internal feedback dynamics described above, have the intrinsic capability to implement a form of weight-dependent STDP. In figure 4(b), we experimentally demonstrate the phase-change weight update in comparison to the additive and weight-dependent STDP. Thus, phase-change synapses can support weight-dependent learning mechanisms in a low-complexity hardware implementation.

The learning rule proposed in this work is a simplified asymmetric STDP rule tailored to the physical properties of the phase-change dynamics. As discussed earlier, the gradual crystallization dynamics described by (1) are exploited to emulate the synaptic potentiation occurring at the causal part of the STDP learning window. In the acausal part, synaptic depression requires amorphization of the phase-change material using reset pulses. The amorphization procedure, besides

the higher power required for creating the amorphous region, cannot progressively update the state of the cell. Unlike crystallization, here the resulting state is only a function of the applied pulse power. Therefore, a power-efficient implementation enabling both the increase and the decrease of the phase-change synaptic weight might be challenging. A differential configuration comprising two cells has been suggested, in which a weight decrease is realized through an increase of a negatively contributing second cell [18, 19]. In our approach, a single cell is used to represent the synaptic weight, and an STDP realization suitable for the characteristics of the phase-change material is proposed. Specifically, as shown in figure 4(c), the causal part corresponds to the characteristics of the classical STDP, whereas at the acausal part of the learning window, a reset pulse always re-creates the amorphous region and thus initializes the synaptic weight. Figure 4(d) shows a simplified form of the proposed STDP in which a single crystallization pulse is used for synaptic potentiation. In addition to the low implementation

complexity, this simplified asymmetric STDP rule allows for smaller gradual increases in the synaptic weight.

The proposed all-memristive single-neuron computational primitive consists of two main components; the phase-change neuron implementing the basic IF mechanism and an array of phase-change synapses operating with a simplified asymmetric STDP learning rule. The realization of this homogeneous fundamental building block forms the basis for implementing powerful large-scale multi-neuron architectures.

3. Multi-neuron architecture with input-level tuning

The single-neuron computational primitive has been explored in learning input correlations [17, 31]. Recently, we have demonstrated an experimental realization with phase-change synapses [20]. Learning is achieved by strengthening certain patterns among the synaptic connections that cause the firing of the neuron when the former appear at the input. A neural network architecture is required to extend the capabilities of the single-neuron primitive towards the learning of multiple correlations. Typically, in fully connected feedforward networks, lateral inhibition is used, where each neuron inhibits the integration of all other neurons in the same layer for a time interval after the spike event [5]. This feature increases the ability of the network to discriminate the input information. In biology, means of tuning the neuronal response to specific stimulus parameters are key in creating a reliable input representation. For example, neurons tuned to various sound levels, known as level-tuned neurons, appear in the primary auditory cortex. They preferentially respond to a particular sound level and have low sensitivity to higher and lower levels [34]. Thanks to this property, the auditory system is capable of sound-level discrimination.

Here, we propose a neuromorphic architecture in which the single-neuron primitive is the main building block and a bio-inspired level-tuning concept provides enhanced learning capabilities. The neuromorphic architecture consists of a one-layer feedforward network with N output neurons and M synapses per neuron, with each of the latter being connected to a corresponding input source. An overview of the SNN architecture is depicted in figure 5(a). To enhance the selectivity of the individual neurons to features related to the level of the input stimuli, we interconnect the neurons based on their internal states and do not use inhibitory links. The neuron internal state information is generated by processing of the input signals. Therefore, it provides better reliability and further insights on the features of the input data than the information provided by the presence or absence of an output spike. As a remark, one can associate the proposed approach to the soft-decision detection methodology in the information theory framework.

In the proposed architecture, the tPSP signal forms the basis of the interconnection between a selected primary neuron and a dependent set of neurons in the architecture as

shown in figure 5(b). Specifically, the tPSP is the internal neuron signal that progressively modifies the neuron membrane potential, emulated here by the phase-change conductance, and that drives the firing response of the neuron (see figure 1). The procedure is initiated by the arrival of presynaptic spike events that generate postsynaptic potential events, which are the weighted signals from the corresponding synapses. The postsynaptic events are the inputs to the neuron. In sequence, the neuron performs a sum of the incoming events generating the tPSP. Specifically, the tPSP _{k} for the k_{th} neuron is defined as

$$\text{tPSP}_k = \sum_{i=1}^M w_{ki} x_i, \quad (3)$$

where w and x denote the weight and the input of the corresponding synapse, respectively. Therefore, the tPSP signal reflects the strength of the cumulative contribution of the synapses, which are activated at each time instance based on the incoming events. Furthermore, the amplitude of the tPSP signal is determined by the number of inputs that correspond to a specific pattern. Conclusively, in the neuromorphic architecture shown in figure 5(b), the level-tuning is defined by the tPSP signal of a selected primary neuron and is communicated between the coupled neurons in the same layer to enable their activity.

The level definition by means of the tPSP leads towards level-tuned neurons with enhanced selectivity to input patterns based on their cumulative characteristics. Different threshold range conditions are used for enabling each neuron, such that it preferentially processes input information corresponding to a certain range of the tPSP signal. Specifically, the membrane potential V_j of a level-tuned neuron j evolves according to

$$\frac{dV_j}{dt} = \begin{cases} \text{tPSP}_j & \text{if } l_{\min}^j < \text{tPSP}_p < l_{\max}^j, \\ 0 & \text{otherwise} \end{cases}, \quad (4)$$

where tPSP _{p} corresponds to the primary neuron and l_{\min}^j , l_{\max}^j are the minimum and maximum level values of the level-tuned neuron. As described in the phase-change neuron configuration the membrane potential is emulated by the dynamics of the phase change cell and the tPSP _{j} value is mapped to an applied crystallizing pulse width determining the firing frequency. Therefore, to further tune the neuronal response, this mapping can be scaled with the preferred maximum value of the tPSP signal.

The proposed concept of level-tuned neurons provides additional means in the SNN for discriminating multiple patterns of information in the input sequences. In the described realization, the level is defined as the cumulative contribution of the weighted sum of the incoming events. This definition of the level can be adapted depending on the needs of the computational task. For example, a level computed using a subset of the incoming signals could enable selectivity to predefined features of the input.

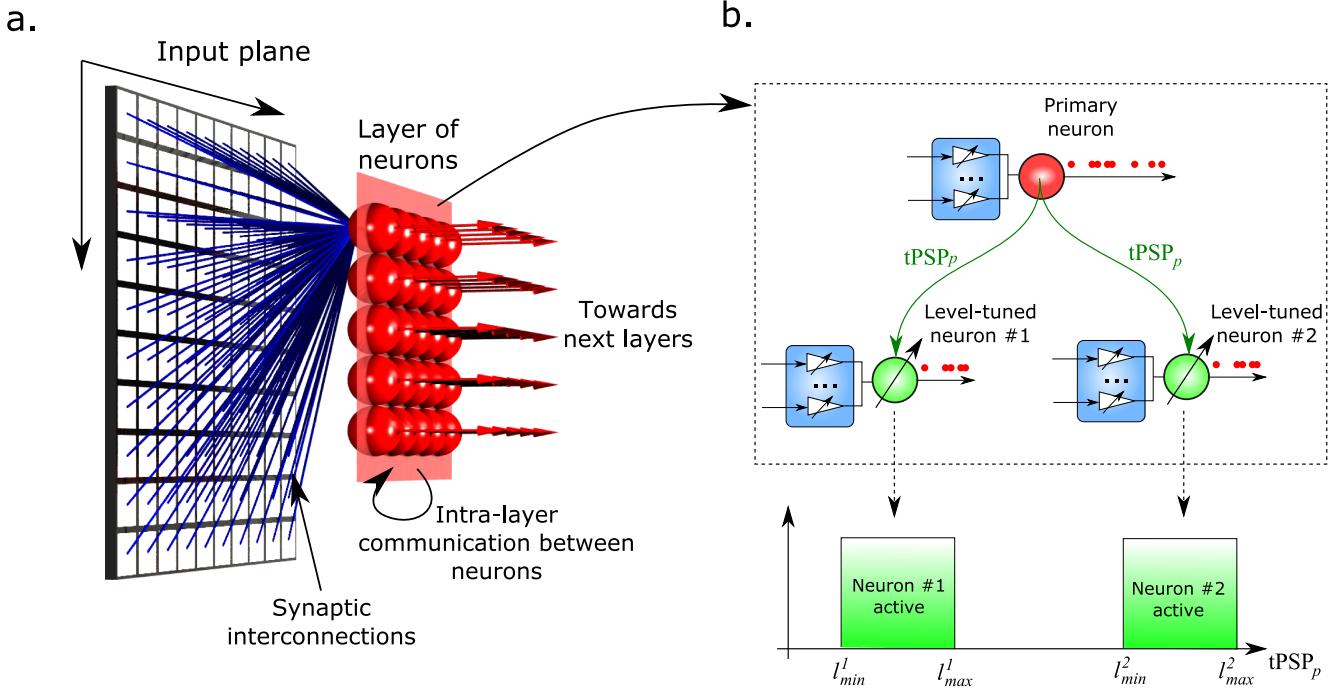


Figure 5. Schematic of neuromorphic architecture with level-tuned neurons. (a) Spiking neural network overview: a one-layer feedforward network in which neurons are interconnected based on their internal states. (b) Concept of level-tuned neurons. The internal state of a primary neuron provides information on the cumulative characteristics of the input and is used to enable a set of level-tuned neurons.

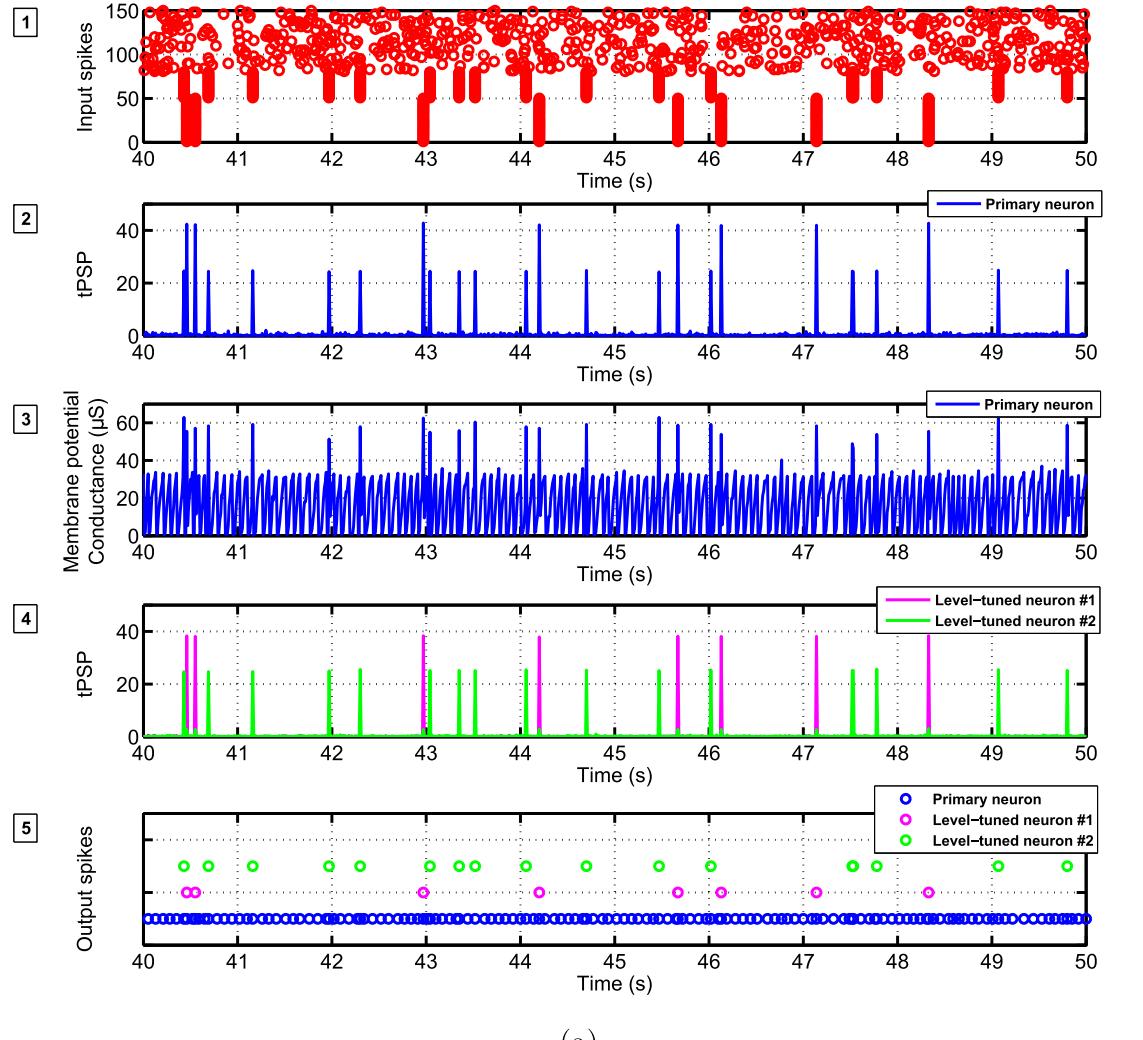
4. Application to correlation detection

The all-memristive computational primitive and the neuromorphic architecture framework outlined in the previous sections can be used to implement important computational tasks. Here, we will explore experimental realizations for unsupervised learning of temporal correlations in parallel input streams. Specifically, the input streams are generated by sampling a stationary Poisson process with a fixed rate and are divided into groups of spike trains with different correlation characteristics and numbers of inputs. We focus on a realization of the architecture depicted in figure 5 consisting of a primary phase-change neuron and two level-tuned phase-change neurons (number of neurons, $N = 3$) with their corresponding arrays of phase-change synapses (synapses per neuron, $M = 400$). The objective is that the primary neuron computational primitive, through continuous learning, will strengthen the synaptic connections corresponding to all correlated events. Moreover, the concept of level-tuning is used in the other two neurons to distinguish the different correlated groups of input streams by the distribution of the weights and also to determine the arrival times of those data streams by the firing of neurons.

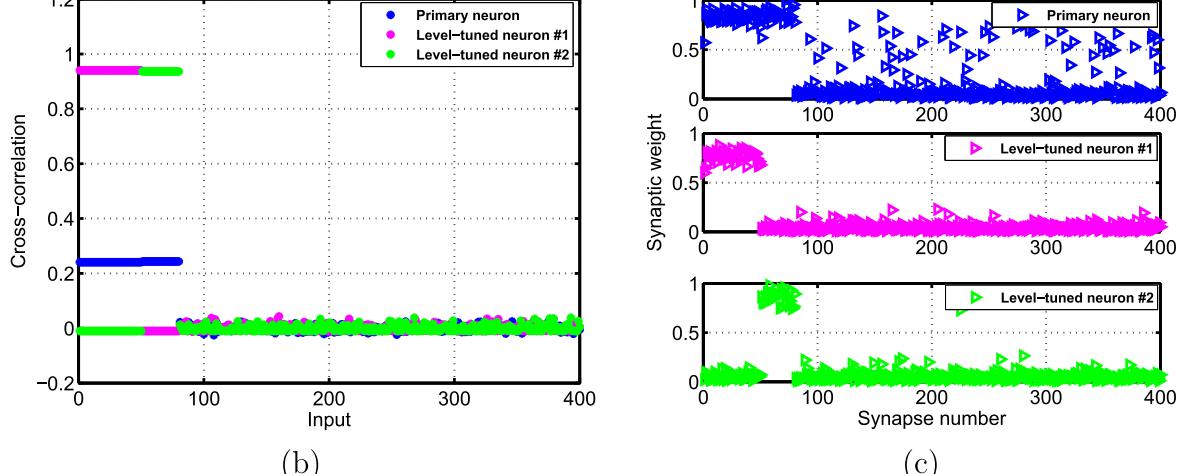
In an experimental realization, we first study strongly correlated groups (correlation coefficient, $c = 1$) comprising fixed sets of inputs with concurrent arrival times. The incoming signals that generate the presynaptic spikes consist of two correlated groups of 50 and 30 input streams, respectively, and 320 input streams that are statistically independent. Figure 6(a1) shows a snapshot of the input spike sequences, where the concurrent arrival of the correlated

inputs and a part of the random arrival of the uncorrelated inputs are shown. With the continuous arrival of the correlated events, the STDP feedback mechanism progressively potentiates the corresponding synapses of the primary neuron. Consequently, based on (3), the tPSP neuronal state signal produces an increased value at the time instances corresponding to the arrival of the correlated inputs. Besides the amount of synaptic potentiation, the amplitude of the tPSP signal is determined by the number of inputs participating in the correlated activity. Figures 6(a2) and (a3) show the evolution of the tPSP state information and its effect on the measured membrane potential of the primary neuron, respectively. We observe that after the initial learning interval (not shown in the figure), the tPSP amplitude reflects the number of inputs in the correlated group. It exhibits a higher value at the appearance of the first correlated group than at that of the second. In contrast, the synapses of the uncorrelated group are instantaneously depressed at the occurrence of each acausal event. Therefore, their cumulative contribution on the tPSP signal is minimal. From the above description, we see that the tPSP internal variable of the primary neuron provides significant information on the collective characteristics of the input spikes.

The information on the collective dynamics of the input is exploited in the proposed architecture to distinguish the various correlated groups. Specifically, the tPSP of the primary neuron is used as an enabling signal for the two other level-tuned neurons. The threshold-enabling conditions of the level-tuned neurons ensure that the arrival of each correlated group event always activates the same neuron. Figure 6(a4) shows the tPSP of the level-tuned neurons,



(a)

**Figure 6.** Experimental results of detecting temporal correlations for correlation coefficient $c = 1$.

where it is already apparent that the two neurons are selective to different correlated groups. This is also reflected in the spiking activity of the neurons shown in the figure 6(a5). We observe that the firing events of the primary neuron are driven

not only by the arrival of the correlated inputs, but that also several instances exist that the primary neuron responds to the accumulated effect of the noise input from the uncorrelated events. In contrast, the firing of the level-tuned neurons is

driven almost exclusively by the events of the two correlated groups.

To quantify the dependence of the neuron firing on the input signals, we use the Pearson's correlation coefficient defined by

$$r = \frac{\sum_{i=1}^n (x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\sum_{i=1}^n (x_i - \bar{x})^2} \sqrt{\sum_{i=1}^n (y_i - \bar{y})^2}}, \quad (5)$$

where x, y are two spike trains of n values and \bar{x}, \bar{y} are the corresponding mean spike values [35]. Figure 6(b) shows the correlation coefficient between the neuron output spike train and each of the M input spike trains for all three neurons in the architecture. The correlation between the primary neuron output and the correlated inputs is higher than with the uncorrelated inputs, where the coefficient is almost zero. Using the output of the primary neuron, it is not possible to distinguish the multiple correlations because the firing of the neuron is driven by all correlated groups. On the contrary, the level-tuned neurons are selective to one correlated group, and the corresponding correlation coefficient is almost equal to one. Note that correlations equal to one correspond to exactly aligned input/output events.

Finally, the correlation between the input-firing events in turn creates a progressive increase in the crystallization of the corresponding phase-change synapses. Conversely, the feedback mechanism depresses the synapses of the uncorrelated group. Figure 6(c) shows a snapshot of the normalized weights at the end of the experiment. The primary neuron computational primitive has clearly detected both groups of correlated synapses. The noise observed in the synaptic weights is due to the firing events driven by the uncorrelated inputs. The correlated synapses corresponding to the two groups can be clearly detected from the weight distribution of the level-tuned neurons as shown in figure 6(c).

Next, we study the effects of inputs with reduced correlation strength. In this experimental realization, the incoming signal consists of two correlated groups of 50 input streams with correlation coefficient $c = 1$ and $c = 0.6$, respectively. The remaining 300 input streams are statistically uncorrelated. The experimental results of this realization are shown in figure 7. In this case, owing to the simplified STDP designed based on the non-accumulative depression features of the phase-change cells, the synapses of the weakly correlated group undergo several depression events. Even though particular weakly correlated synapses are fully depressed in each acausal incident, they are quickly potentiated again attracted by the majority of the correlated synapses that continuously drive the neuron response. Specifically, figure 7(c) shows that, at a specific time instance, the synaptic weights of the third level-tuned neuron have a wider spread than the synapses of the second neuron. On average, though, the synaptic weights of the weakly correlated group have distinguishable weight that allows them to have control of the firing of the third level-tuned neuron, as shown in figure 7(b).

These experimental results prove that, for detecting correlations, it is not crucial that all synaptic weights remain continuously potentiated. Therefore, a simplified learning rule

can reveal the underlying features and successfully drive the system response. Furthermore, information for a correlated activity can usually be inferred from the synaptic weights, even if a part of them is depressed at some time instances. This is particularly essential for the phase-change synaptic realization, in which complicated circuit and programming pulse configurations will be required to enable progressive depression features in the learning rule. Finally, note that essential components in maintaining the stability of this feedback-enabled neurosynaptic configuration are the inherent weight-dependent accumulative characteristics of the phase-change synapses and the linear evolution of the phase-change neuronal membrane potential described in the previous sections.

5. Detecting spatio-temporal patterns

In this section, we demonstrate how the neuromorphic architecture introduced above can be used to discriminate spatio-temporal image patterns in a large set of input signals. The image patterns, used as an input stimuli, consist of 100×100 pixels. All pixels are connected consecutively row by row to three sets of 10 000 phase-change synapses. We randomly present two correlated groups of inputs derived from two images: one representing the 'Watson' logo and the other a sample text. The inputs corresponding to the on-pixels of the image patterns are temporally encoded as joint bursts of spikes, whereas Poissonian noise is generated for the remaining pixels. The average spiking frequency of the image input and the noise signals is the same and was chosen equal to 1 Hz. Figures 8(a) and (b) show the time-lapse sequences of the learning process. Specifically, 8(a) shows selected instances of the synaptic input signal along with the arrival times of the two patterns. Figure 8(b) presents the three sets of synaptic weights experimentally realized with a total of 30 000 phase-change cells. For each neuron in the architecture, the corresponding output spikes are also shown. We observe that the two level-tuned neurons (depicted in figures 8(b2) and (b3)) become selective to a specific image and that the corresponding synapses progressively increase their synaptic weights. The output of the neurons is synchronized with the arrival times of the input patterns. On the contrary, the first neuron (depicted in figure 8(b1)), which continuously processes the input signals, becomes sensitive to both correlated groups and serves here as enabling neuron for the two level-tuned neurons.

Figure 8(c) shows the evolution of the average conductance of the synapses corresponding to the two input images and the average conductance of the synapses corresponding to the noise inputs. For the primary neuron (see figure 8(c1)), we observe the gradual increase of the synaptic conductance for both image patterns, following the rate of occurrence of these events. After the synapses have reached a high conductance value, they maintain the separation from the rest of the synapses, indicating the presence of image patterns in the input. The selectivity of the level-tuned neurons to a single pattern is also confirmed by the average conductance

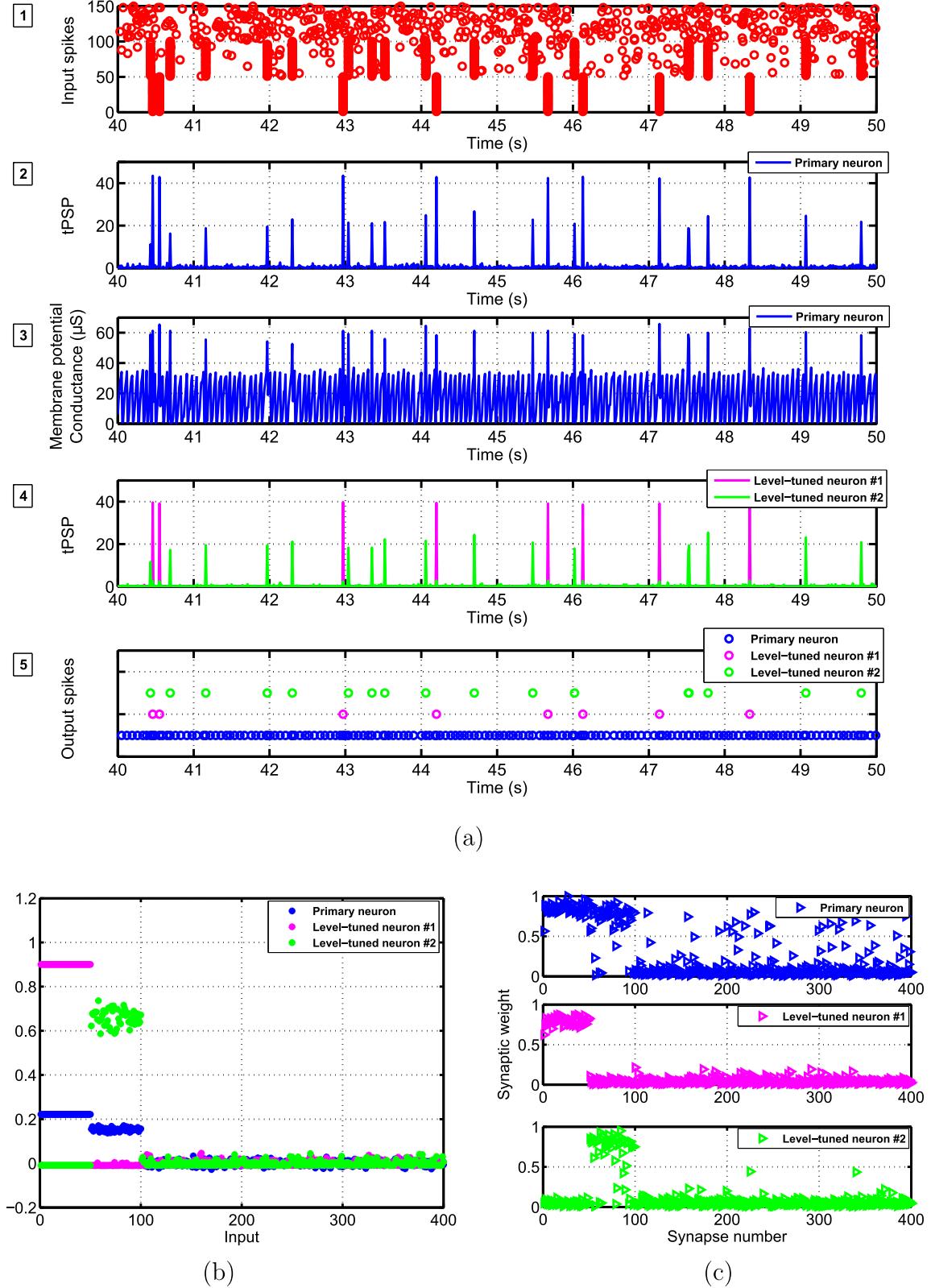


Figure 7. Experimental results of detecting temporal correlations for correlation coefficient $c = 0.6$.

plots shown in figures 8(c2) and (c3). The two images have overlapping pixels, and this reflects in the average conductance corresponding to the synapses of the non-selected image. Furthermore, a strong potentiation of the synapses of

the first neuron is required to generate a sufficient cumulative effect that is first mapped to the tPSP signal and subsequently enables the level-tuned neurons. Therefore, the potentiation process for the synapses of the level-tuned neurons initiates

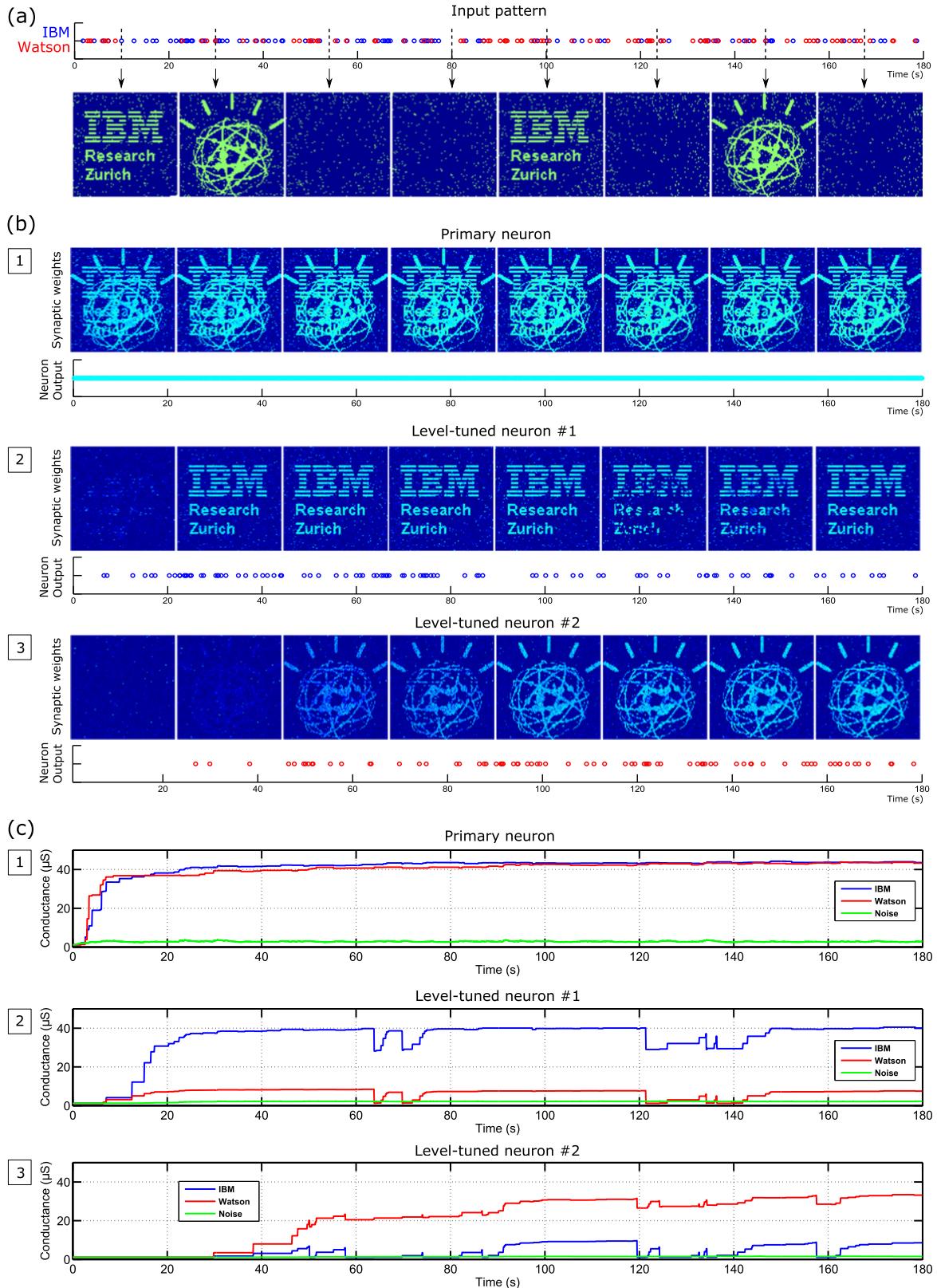


Figure 8. Experimental results of detecting spatio-temporal patterns.

after a certain selectivity has accumulated in the synapses of the primary neuron.

The results show that the level-tuned neurons have distinguished the input features and are able to detect their

arrival times in the input sequence. In rare events, e.g., when both patterns arrive at very close time instances, the common pixels may be depressed because of the simplified STDP mechanism (see figure 8(c2), at $t = 121$ s). However, the

system quickly recovers without affecting the performance of the detection mechanism of the spiking neuron. A more advanced STDP learning rule could provide further precision in the system, at the cost of a more complicated implementation. It is remarkable, though, that using the simplified STDP and despite the inherent variability of the phase-change neuron-synaptic realization, the level-tuned neurons are capable of learning multiple input patterns in the presence of input noise.

6. Summary and future work

With this paper, our contribution is two-fold. Firstly, we presented how the single-neuron building block of a SNN can be realized with nanoscale phase-change devices in an all-memristive configuration. Secondly, this computational primitive was incorporated into a neuromorphic architecture enhanced with the biologically-inspired scheme of level-tuning neurons. We demonstrated experimentally that the proposed all-memristive neuromorphic architecture is capable of learning multiple correlations from a large number of input streams in an unsupervised manner.

Inherent characteristics of phase-change memristors, such as multilevel storage, accumulation, and state-dependent dynamics, render them a promising technology for all-memristive neuro-synaptic implementations. Combining the above with their proven characteristics of high speed, low energy and excellent scalability developed in emerging memory applications, an all-memristive computational primitive offers all the key features for application in large-scale neuromorphic systems. The experimental studies presented in this work demonstrate that despite the simplified neuro-synaptic implementation and the inherent variability of the phase-change cells, the memristive components provide the required neuromorphic functionality. However, open issues related to the interconnectivity and the integration of the memristive components in a neuromorphic processor chip, remain to be addressed. Further work should also discuss the algorithmic implications of the variability, stochasticity and storage resolution of the memristive neurons and synapses in more complex neural network configurations.

In biology, architectures with highly variable components can adapt and perform specialized operations in a robust way. Key features of biological systems are the best source of inspiration for building compact and efficient artificial neural systems for computing applications, such as big data analytics and sensory information processing. In this paper, inspired by specialized coders of low-sound levels in the auditory cortex, we incorporated the level-tuned neuron approach for detecting multiple correlated input patterns. To implement level-tuned neurons, state information already present in the neuronal structure was exploited. This information provided powerful insights into the characteristics of the input data streams, which proved instrumental for the experimental demonstration of multiple pattern detection. Therefore, we believe that this development could function as the basis for

further research in enhanced large-scale neural network configurations.

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