

3D ICs in the Real World

Dick James
Chipworks Inc.
Ottawa, Canada
djames@chipworks.com

Abstract— There has been much discussion (hype, even!) of 3D chip stacking taking over when the device shrinkage described by Moore’s Law comes to an end. To hear some industry commentators, through-silicon vias (TSVs) will enable a revolution in performance and enable the next several generations of electronics evolution.

In fact the transition to commercial 3D stacking of heterogeneous components is taking much longer than was predicted a few years ago. While commodity parts such as flash memory or DRAM have achieved impressive levels of density, true system-in-package parts are a rarity, or limited to niche markets such as MEMS or image sensors. The use of TSVs has so far been limited to products such as image sensors, high-end FPGAs, and a minority of MEMS devices.

However, the packaging industry has been making great strides in multi-chip packaging, just not in the directions that have received the media attention. The rapid evolution of mobile devices has driven major changes in the packaging arena, and there have been remarkable developments as a consequence.

Chipworks, as a supplier of competitive intelligence to the semiconductor and electronics industries, has monitored the evolution of chip packaging as new developments come into commercial production. Chipworks has obtained parts from the leading edge products, and performed structural analyses to examine the new features of the devices.

The paper reviews some of the different packaging technologies that we have seen in recent years, and looks at some examples of both the ‘new normal’ and unusual packages in use.

Keywords— 3D Packaging; Through-Silicon Vias; Chip Stacking.

I. INTRODUCTION

In recent years the terms “3D” and “2.5D” have become familiar for anyone in the semiconductor packaging business, or looking for “more than Moore” performance. These terms seem to have no formal definition, but the informal definitions appear to be that “3D” is the co-packaging of heterogeneous devices using copper-filled through-silicon vias (TSVs); and

“2.5D” is also co-packaging dissimilar parts, but side-by-side on an interposer, and again using TSVs.

If we take that relatively limited definition of 3D, then we can say that only image sensors have reached volume production. None of the memory-based 3D stacks such as the Hybrid Memory Cube [1] have achieved this state, at least at the time of writing. There are 2.5D products, notably the Virtex 2000T from Xilinx [2], but they are expensive and produced in relatively low volume.

If we expand that limited definition to a more intuitive version of 3D, i.e. packages that contain a stack of different interconnected chips, then we have a much broader range of devices to examine. The packaging industry has been pushing its boundaries in several directions, with advancements in wire bonding, microbumps, chip stacking, face-to-face packaging, and package-on-package (PoP) techniques, amongst others. Because of the need for compact and cost-efficient packaging, many of these advancements are seen in mobile phones.

As an example, Fig. 1 shows a cross-section of the Apple iPhone 5s motherboard, with the Apple A7 processor on the topside, in the lower half of a PoP, and two Elpida SDRAM chips in the upper half; and a SK Hynix flash package on the bottom side, with the flash controller in the centre with a spacer die separating it from two 64-Gbit NAND flash dies – perhaps a good example of “3D, but not 3D”.

As an aside, the Elpida parts are wire-bonded using silver wire, the first time this was observed by Chipworks.

II. COMMODITY MEMORY

A. Sandisk 32-GB NAND Flash Stack

Commodity memory has achieved some impressive density improvements over the years, thanks to developments in wafer thinning and wire bonding techniques (in addition to process technology!). The Micro-SD card format is particularly challenging since it is so compact, but it is now available in a

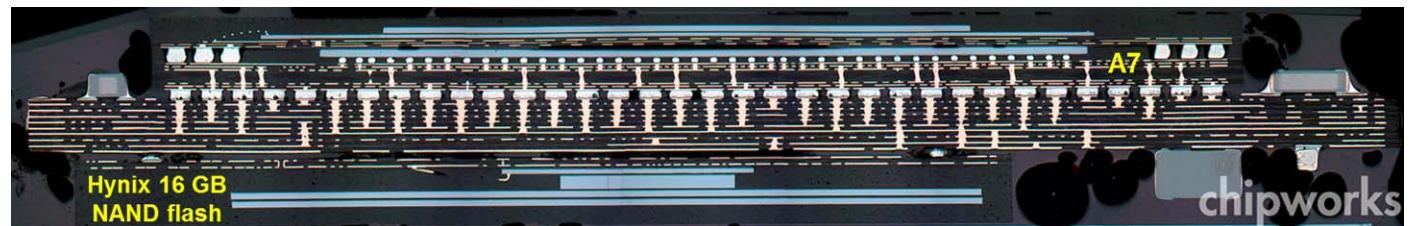


Fig. 1 Cross-section through iPhone 5s motherboard

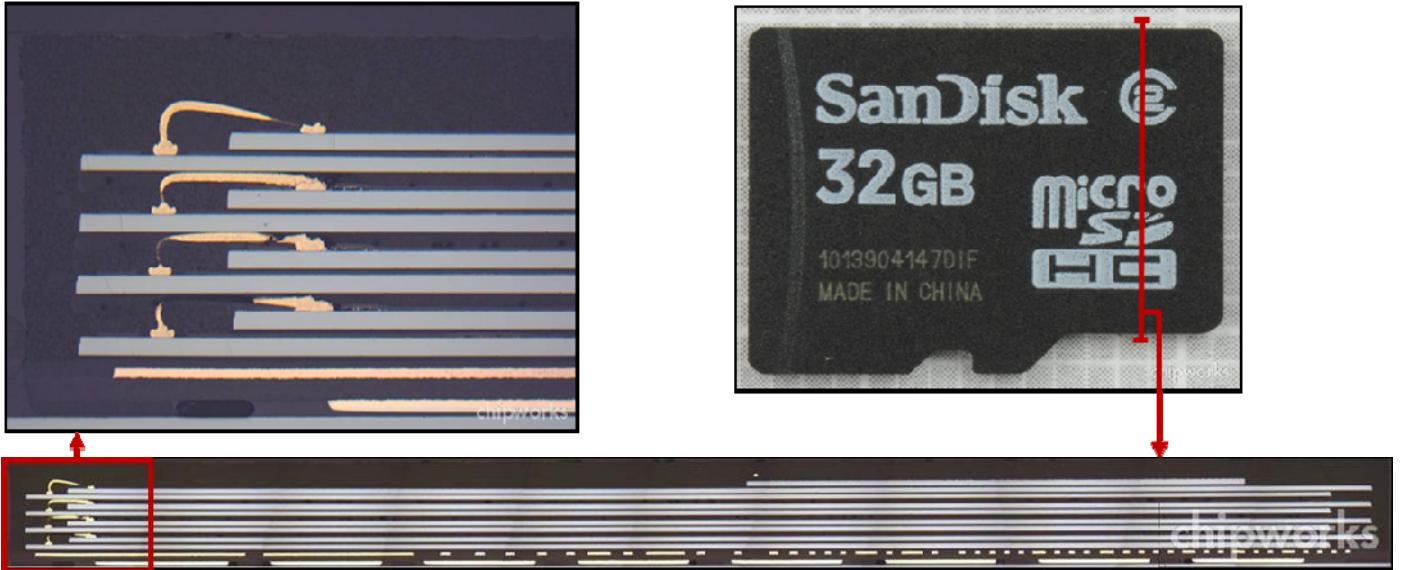


Fig. 2 Cross-section of Sandisk Micro-SD flash memory card

128 GB density.

Fig. 2 shows an example of a 32-GB Micro-SD card from Sandisk, containing eight 32-Gb flash chips together with a controller chip. The Micro-SD standard [3] specifies a thickness of 1.0 mm, including the contact metal.

To achieve this, the dies have been thinned down to $\sim 35\text{ }\mu\text{m}$, and we have some remarkably low profile wire bonding. If we look closely we can see that stub bonds have been placed on the top die of each pair, and the bond wires have been taken from a ball bond on the lower die to a wedge bond on the upper stub bond.

Another innovation is the use of a flowable plastic layer on the base of the top three of the pairs of dies, so that it can mould around the wirebonds on the die below.

The continuous density increases in flash memory now means that by using eight 128-Gb dies, we can now obtain 128 GB Micro-SD cards for our phone or camera!

B. Samsung 64 GB NAND Flash

Samsung has taken a different approach to die stacking; in Fig. 3 we have a 64-GB part taken from a 64-GB iPhone. The chips have similarly been thinned to $\sim 35\text{ }\mu\text{m}$, but they are not stacked in alternating pairs, but in overlapped groups of four.

In this case we have sixteen 32-Gb dies stacked in a 1-mm thick package; the die layout allows for “nose-to-tail” wire bonding, so that less space is needed between the dies. No controller is needed, since that is integrated into the applications processor in the phone.

Remarkable though this is, Samsung actually has a 32-stack package in their roadmap [4].

C. Chipsip 4 Gb DDR2 SDRAM

Chipsip is a small Taiwanese company that specializes in compact chip stacking by using sophisticated wire-bonding.

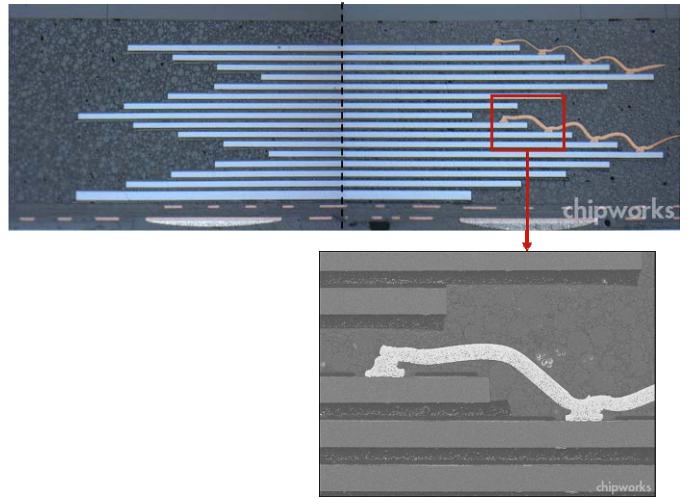


Fig. 3 Cross-section of Samsung 64GB NAND flash memory

The example shown here was taken from a digital point-and-shoot camera.

Initially there is not much to remark on when looking at the plan-view x-ray, until we remember that this is a stack of four dies, and the bond wires go to pads down the centre line of

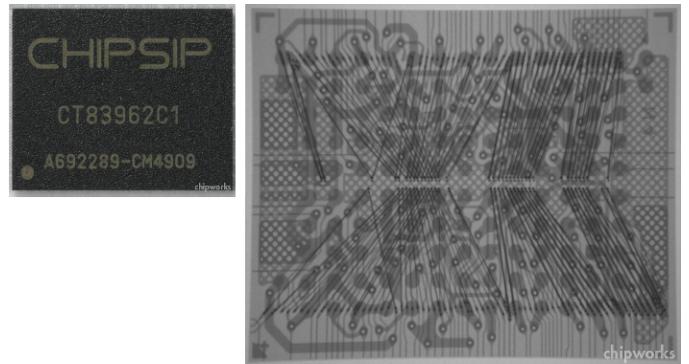


Fig. 4. Plan-view x-ray of Chipsip 4-Gb SDRAM

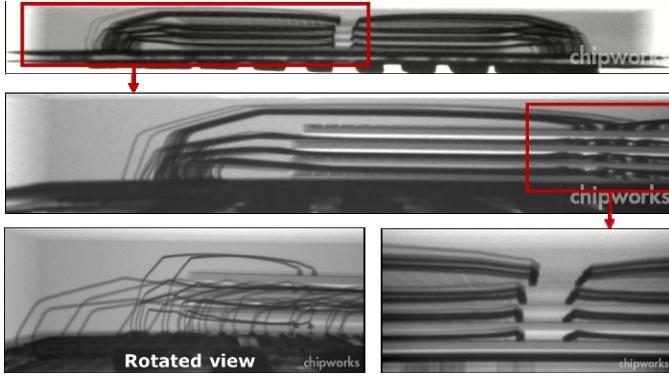


Fig. 5 Side-view x-rays of Chipsip 4 Gb SDRAM

each die (not the edge, as in the flash examples above).

When we look at the x-rays from the end of the chip, the challenging nature of the wire bonding becomes clear. Not only are the wire loops low-profile, they are also some of the longest that we have ever seen at Chipworks.

III. SYSTEM-IN-PACKAGE

“System-in-Package” (SiP) parts have been available since the industry became capable of putting multiple chips in the same package, and can also be described as multi-chip modules. Most SiPs that we see have the dies mounted on a common substrate (2D), but occasionally we see examples where they have been stacked in 3D fashion, and we illustrate some below.

A. Renesas/NEC MC-10149 “Camera Engine”

NEC has been one of the regular proponents of die stacking for selected products, and Renesas has kept the technology going since the corporate merger.

The MC-10149 (Fig.6) is referred to as a “camera engine”, and provides image processing in a small package adjacent to the image sensor chip. In this version of the part we have the image-processing SoC at the base of the stack, with spacer, Elpida SDRAM, and Macronix flash dies above. Conventional wire bonding is used, so this is a straightforward version of 3D, with no layout requirements necessary for the packaging.

B. Sony CXD5315GG Applications Processor

The Sony CXD5315GG was the microprocessor found in the Sony Playstation Vita. It incorporates a quad-core ARM Cortex-A9 device with an embedded Imagination

SGX543MP4+ quad-core GPU. At the time it was a leading-edge combination, better than seen in most tablets.

Sony’s specification stated that there was 512 MB (4 Gb) regular DRAM, plus 128 MB (1 Gb) VRAM (video RAM), but there were no memory chips on the motherboard other than the flash chip. We expected to see the DRAM in a PoP stack, as in a phone, but the x-ray image indicated that the part was a five-die stack within the package, and that was confirmed with a physical cross-section (Fig. 7).

At the base we have the processor chip; face to face with it is a Samsung 1-Gb wide I/O SDRAM; and the top three dies comprise two Samsung 2-Gb mobile DDR2 SDRAMs, separated by a spacer die, and conventionally wire-bonded. The base die is ~250 µm thick, and the others ~100 – 120 µm.

This type of face-to-face connection between two dies showed up back in 2006 in the original Sony PSP, and Toshiba had dubbed it “semi-embedded DRAM”, now they are calling it “Stacked Chip SoC” [5]; the packaging industry jargon seems to be “chip-on-chip”. The ball pitch is an impressive ~45 µm.

When we look at the die photos of the processor and the 1-Gb memory (Fig. 8), we can see that they are purposely laid out for the stacked-chip configuration, since in the centres of both is an array of matching bond pads.

Close examination reveals that there are 1080 pads in two blocks of 540 (4 blocks of 45 rows of 6 pads), so likely 2 x 512 bit I/O operation, possibly sub-divided into 4 x 128.

At ISSCC 2011, Samsung described a similar wide I/O DRAM using TSVs [6], claiming a data bandwidth of 12.8 Gb/s, four times the bandwidth of an equivalent LPDDR2 part.

By combining the processor with the different memories in the same package in the Vita, Sony and Toshiba have produced one of the few true SiP parts that we have seen.

C. Invensense MPU-6050 Motion Processing Unit

Invensense specializes in MEMS sensors using a unique die stacking technology that integrates the MEMS and signal processing dies into a very compact SiP [7]. The MPU-6050 is a nine-axis motion processing unit, incorporating a three-axis gyroscope and a three-axis accelerometer in a single chip, plus a custom digital motion processor (DMP) ASIC die. It can also interface with a third-party magnetometer via I²C, to provide full nine-degrees-of-freedom motion sensing.

Fig. 9 illustrates the top view of the device after de-

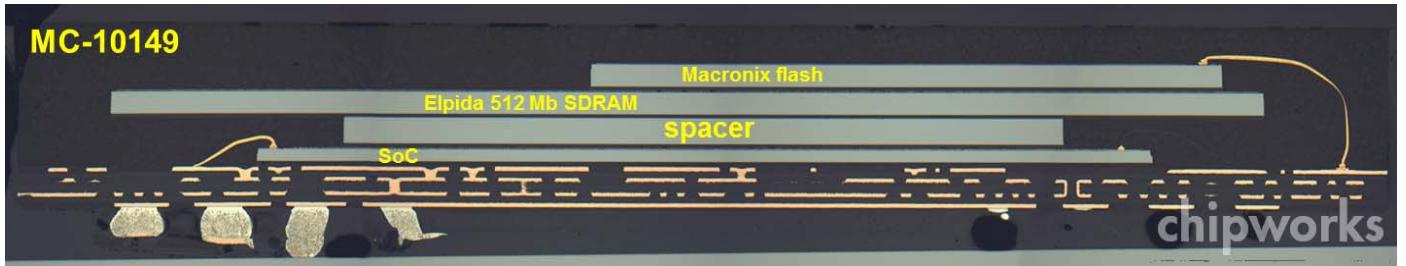


Fig. 6 Cross-section of Renesas/NEC MC-10149 “Camera Engine”

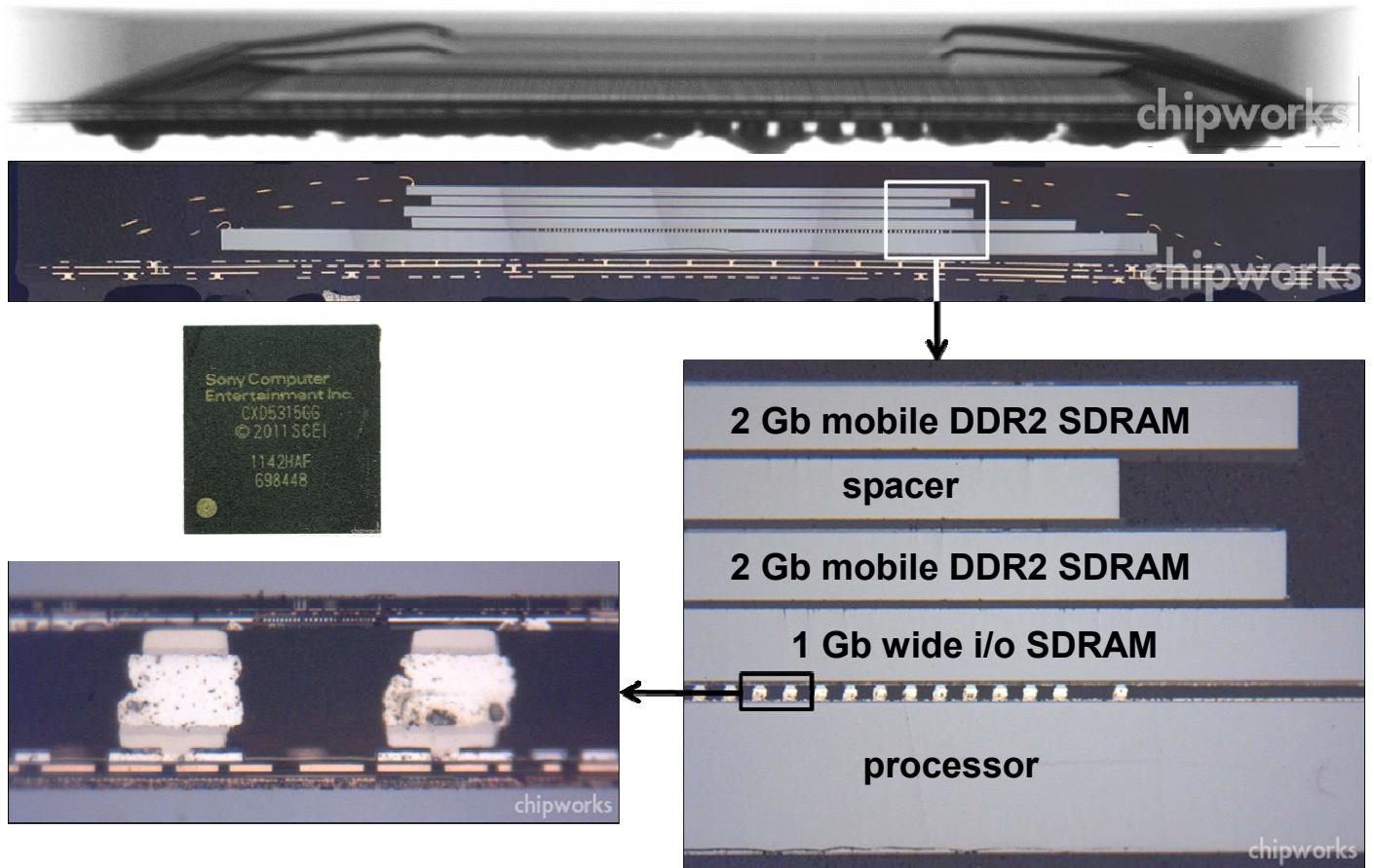


Fig. 7 X-ray and optical images of Sony CXD5315GG Applications Processor

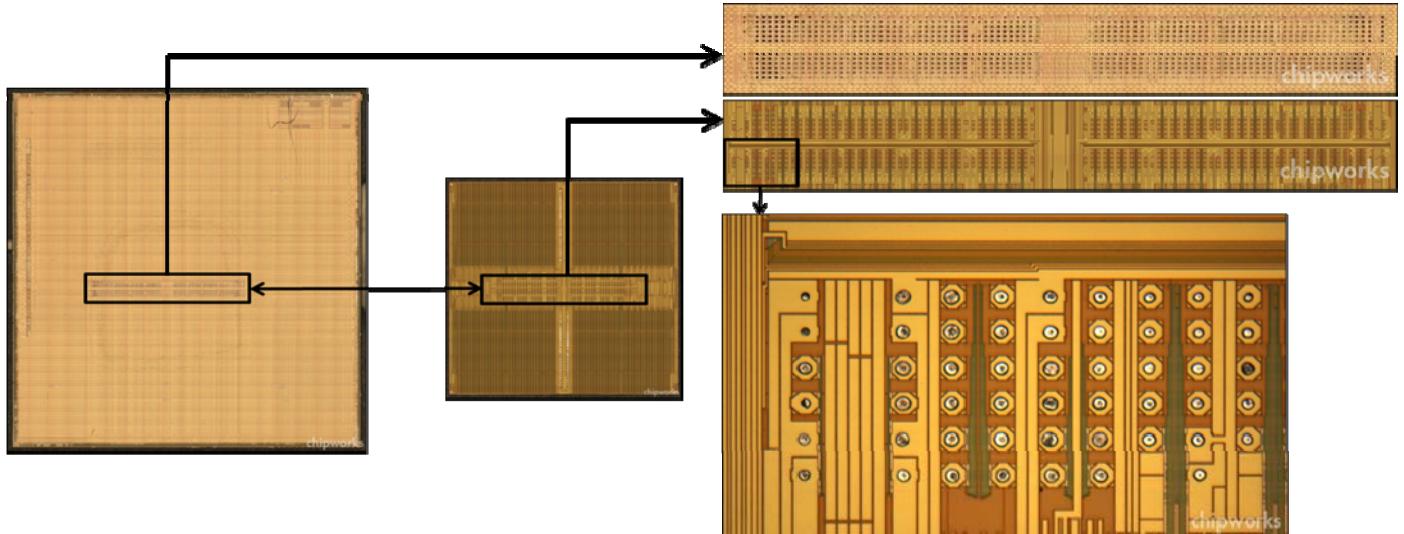


Fig. 8 Microbump layout of Sony application processor and Samsung VRAM

capsulation. At left is the decapsulated device, with the MEMS capping die still on; at centre the cap has been removed, showing the MEMS device; at right the MEMS die has been removed and the DMP ASIC can be seen. So the device is actually a three-die stack, with the ASIC die on the bottom, the MEMS die layered on the ASIC, and a capping die

to seal the MEMS. The DMP die is larger than the MEMS so that the DMP can be wire bonded.

The MEMS die and cap are manufactured using a bulk Si micromachining MEMS process, while the ASIC die is manufactured using a 180 nm BCDMOS process, with some bulk etching to provide cavities under the x- and y-axis

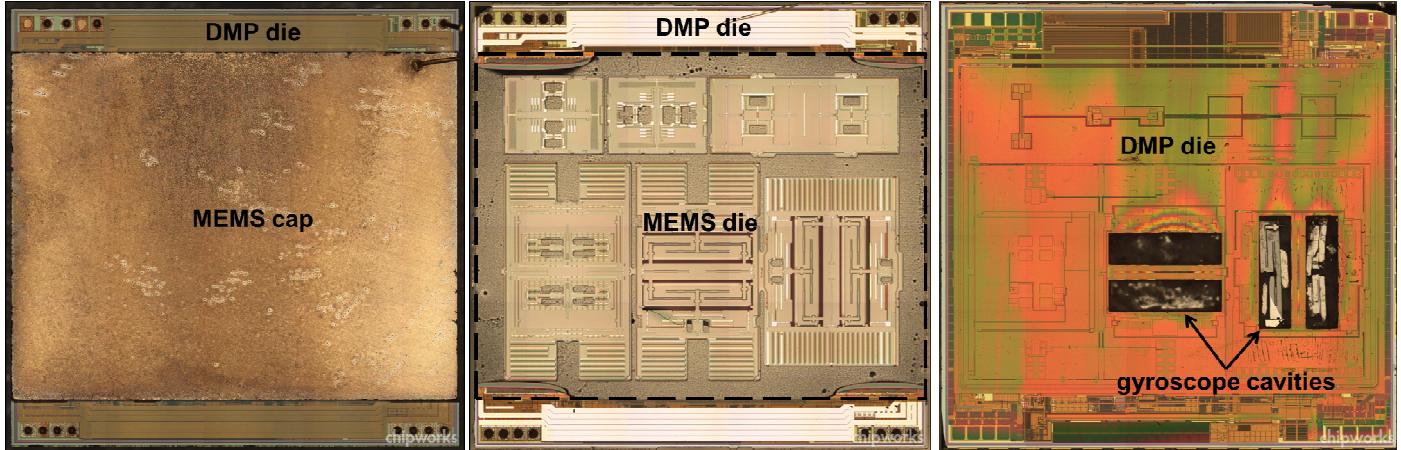


Fig. 9 Plan-view photos of Invensense MPU6050 dies

gyroscopes in the MEMS (the movable masses in these flex in the z-direction).

Conventional MEMS devices are also often three-die stacks, but with the ASIC on top of the sealed MEMS unit, with the two connected by wire bonds. The MEMS also has a cap die on top of the MEMS die.

The distinguishing feature of the Invensense device is that the MEMS die is thinned to sit on top of the ASIC, which acts

as the MEMS substrate, and the three are integrated at the wafer scale. The MEMS electrodes are directly connected to the top metal of the ASIC, with no wire bonding between the two.

The cross-section of the package is shown in Fig. 10; the cavities in the cap are clearly visible, but this section does not go through any of the cavities in the ASIC. We can also see that the ASIC uses a 6-metal process. The MEMS die is ~30 µm thick, and the cap and ASIC dies are 200 and 290 µm,

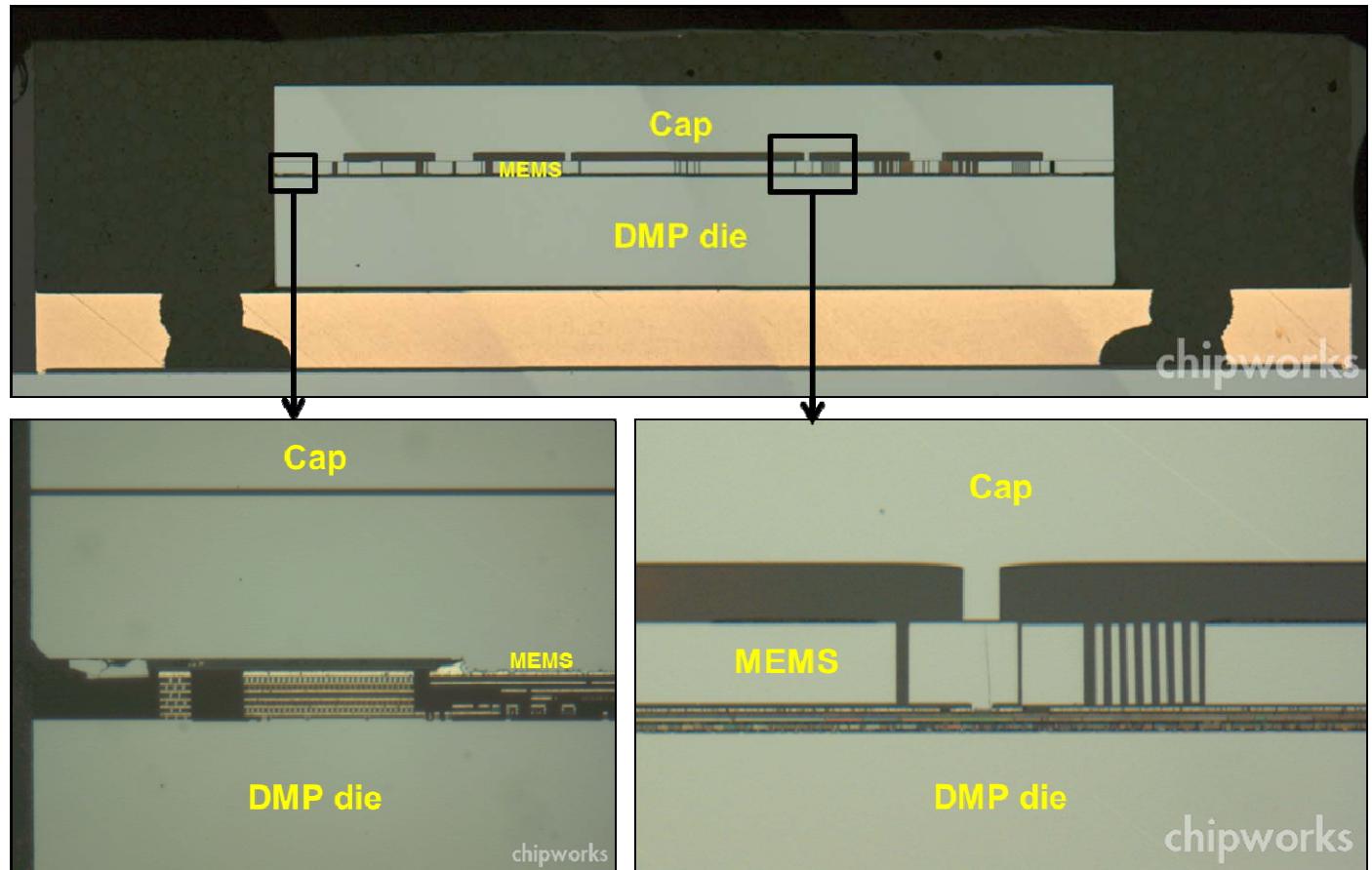


Fig. 10 Cross-sections of Invensense MPU6050

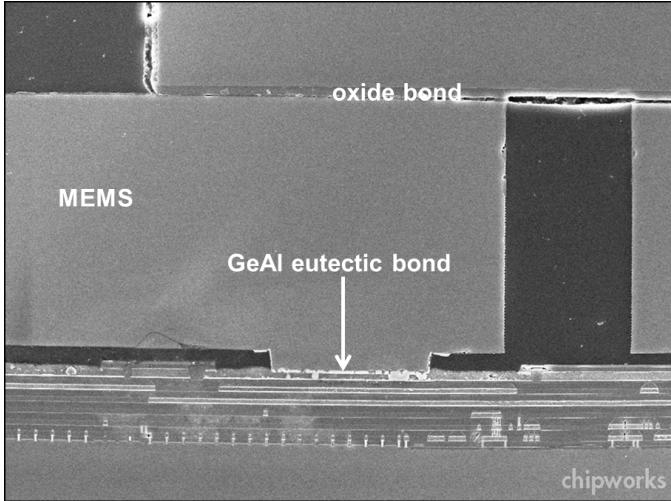


Fig. 11 SEM cross-section showing die bonding in Invensense MPU-6050 respectively.

The bonding between the cap and MEMS die is through oxide-to-oxide fusion bonding. The MEMS die and ASIC are bonded through a GeAl eutectic bond between a Ge layer formed on the bottom of the MEMS Si pedestals, and the Al metal 6 line of the ASIC (Fig. 11).

Once the die stacking has been completed, the assembly is conventionally wire-bonded (Fig. 12) and encapsulated.

D. Sony IMX135 13-Mpixel CMOS Image Sensor

Sony introduced their Exmor-RS stacked, back-illuminated CMOS image sensors (CIS) in 2013. The image sensor wafer is fabricated so that the photodiodes and optical layers are on the bottom of the wafer (as conventionally viewed). It is then flipped over and bonded to the wafer containing the image processor chips, so that the pixels face upwards. This increases the effective pixel size (compared to a front-illuminated sensor), since there is no metallization to get in the way of the light.

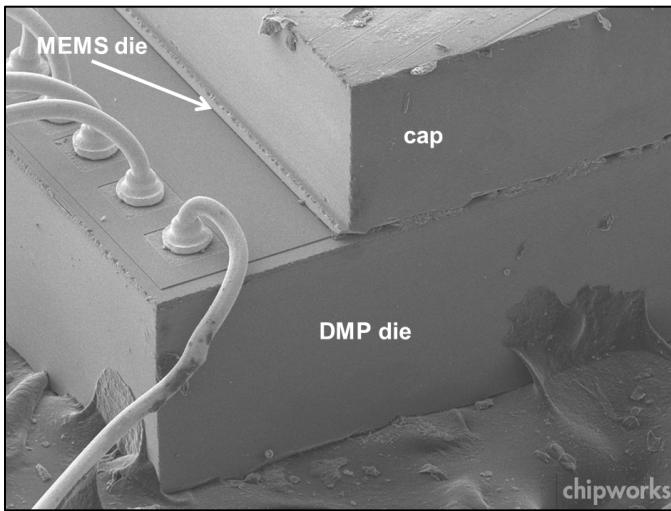


Fig. 12 SEM image of wire-bonded die stack in Invensense MPU-6050

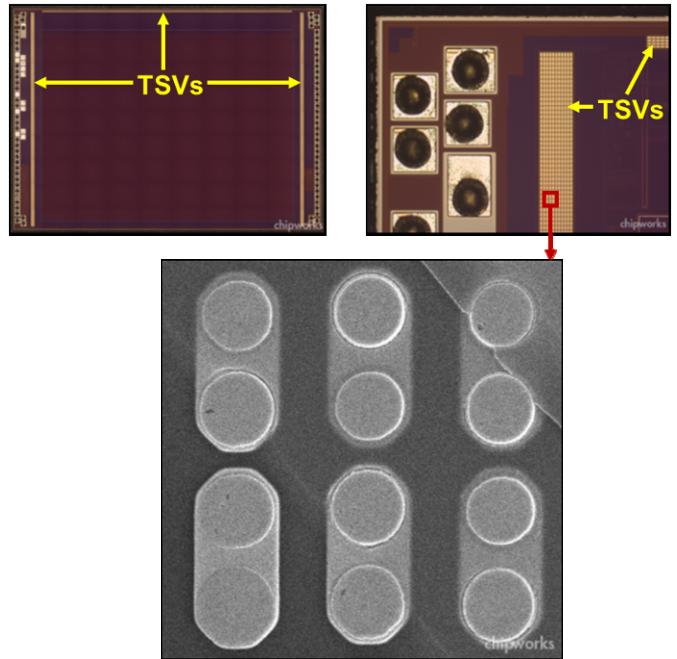


Fig. 13 TSVs in Sony IMX135 image sensor – plan view

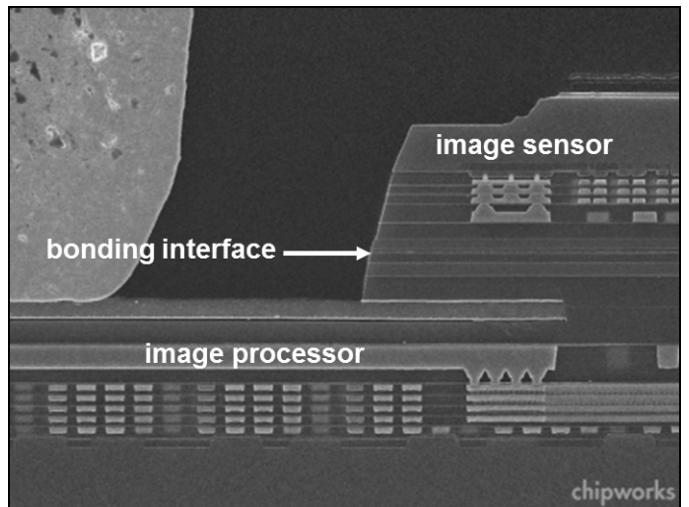


Fig. 14 Cross-section of Sony IMX135 image sensor

Fig. 13 shows plan-view images of the CIS, indicating the arrays of TSVs, and zooming in on a block of six TSV pairs. Fig. 14 is a cross-section of the die stack, and we can see the die bonding interface, and that the CIS die is inverted on to the processor die (since the metal vias are mirror-image).

Fig. 15 examines the TSV structure; because the wafers are bonded face-to-face, and not bottom-to-top, the TSVs have to be “up and over” to connect the metallization layers of the two dies.

The bottom metal of the CIS die is connected to the top metal of the processor die. If we look closely we can see that the aluminum has been etched out of the processor metal, and copper plated into the cavity.

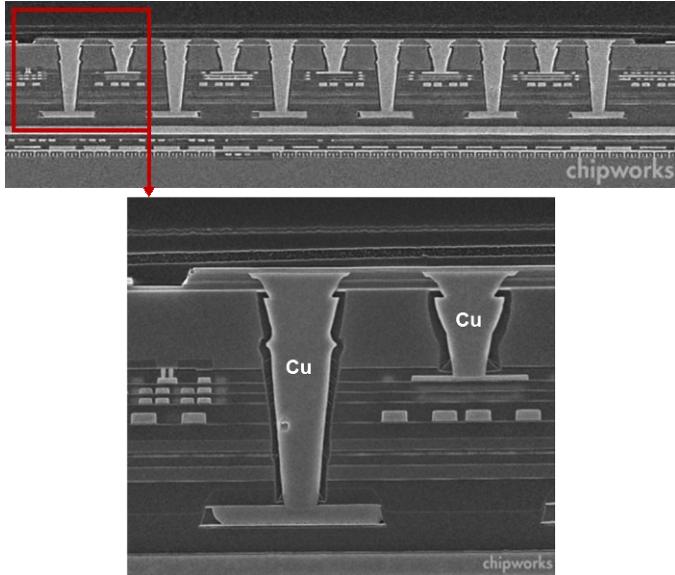


Fig. 15 Cross-section of TSVs in Sony IMX135 image sensor

IV. SUMMARY AND CONCLUSIONS

We have reviewed eight multichip packages that we have seen in the last few years. While not meeting the industry marketing definition of 3D, these structures are undeniably innovative and have enabled much of the increased performance and size reduction that we have seen in the mobile electronics industry.

Apart from the Renesas/NEC device, the common characteristic displayed by the SiP parts is that they are all deliberately laid out for die stacking; until industry standards are defined, this requirement is likely to limit 3D assembly to IDMs (such as Sony) or fabless companies willing to take on the extra design effort.

REFERENCES

- [1] J. T. Pawlowski, "Hybrid Memory Cube (HMC)", Hot Chips 23, 2011
- [2] L.Madden, "Heterogeneous 3-D stacking, can we have the best of both (technology) worlds?", 2013 International Symposium on Physical Design
- [3] <https://www.sdcard.org/developers/overview/capacity/>
- [4] <http://www.samsung.com/global/business/semiconductor/support/package-e-info/overview>
- [5] <http://www.toshiba-components.com/ASIC/SiP.html>
- [6] J-S. Kim et al., "A 1.2V 12.8GB/s 2Gb Mobile Wide-I/O DRAM with 4×128 I/Os Using TSV-Based Stacking", ISSCC 2011, pp. 496 – 498.
- [7] S. Nasiri, "Wafer-Scale Packaging and Integration Are Credited for New Generation of Low-Cost MEMS Motion Sensor Products," International Wafer-Level Packaging Conference, 2007.