# An ultra low power current-mode filter for neuromorphic systems and biomedical signal processing

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***Abstract*— Current-mode log-domain CMOS filters have favorable properties, such as wide dynamic range at low supply voltage, compactness, linearity and low power consumption. These properties are becoming increasingly important for biomedical applications that require extremely low-power dissipation and neuromorphic circuits that attempt to reproduce the biophysics of biological neurons and synapses. We present a current-mode log-domain integrator circuit with tunable gain that is extremely compact, compared to analogous state-of-the-art solutions. We show how the circuit proposed can implement a wide range of cut-off frequencies, extending over four orders of magnitude and dissipates less than $1nW$ for cutoff frequencies lower than 100Hz. We derive the circuit's linear and non-linear characteristics through analytical derivations, present SPICE simulations that are in accordance with the theoretical analysis, and show measurements from a test chip comprising the VLSI implementation of the circuit proposed.**

## I. Introduction

Since the early 90's there has been growing interest in current-mode design approach [1]. Current-mode circuits have been shown to have a wide variety of useful features, including the capability of operating with large bandwidth at low supply voltages [2]. Current-mode CMOS circuits operated in the subthreshold, or weak-inversion, regime can be used to implement *log-domain filters* [3]. The log-domain paradigm has the advantage of producing linear building blocks by dealing with non linearities at the component level and, as any other companding technique [4], it improves the circuit's dynamic range [5].

In this paper we present a low-power current-mode linear integrator, the "Diff-Pair Integrator" (DPI), that has the same properties of classical log-domain first order low pass filters [3], but with the additional advantage of providing tunable gain independent from the (tunable) time constant, compact layout, better matching properties and lower power consumption.

The DPI's low-power and compactness features, combined with its capabilities of generating low cut-off frequencies make it ideal for biomedical applications [6], [7], as well as neuromorphic systems that require large filter bank arrays, such as silicon cochleas or pulse-based neural network devices [8], [9]. In the next sections we present the circuit description, SPICE simulations results, and experimental results measured from a prototype chip, fabricated using a standard AMS $0.35\mu$ CMOS technology.

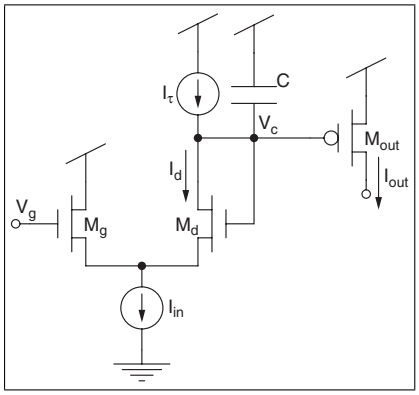


Fig. 1. Diff-pair integrator circuit schematics. The $I_{in}$ and $I_\tau$ current sources are implemented with single MOSFETs biased in subthreshold.

## II. The diff-pair integrator circuit

The DPI is a CMOS current-mode circuit that operates in the subthreshold regime [10]. As shown in Fig. 1, it comprises only 3 n-FETs, 2 p-FETs and 1 capacitor. The two current sources of Fig. 1 are implemented using two subthreshold MOSFETs: one n-FET for the $I_{in}$ current and one p-FET for the $I_\tau$ current.

In subthreshold, the output p-FET $M_{out}$ produces a current that changes exponentially with its gate voltage $V_c$. Specifically:

$$I_{out} = I_0 e^{-\frac{\kappa(V_c - V_{dd})}{U_T}}, \quad (1)$$

where $V_{dd}$ is the power supply voltage, $I_0$ is the leakage current, $\kappa$ is the subthreshold slope factor, and $U_T$ is the thermal voltage [10]. Similarly, the subthreshold branch current $I_d$ of the differential pair, formed by the current source $I_{in}$, $M_g$, and $M_d$, can be expressed as:

$$I_d = I_{in} \frac{e^{\frac{\kappa V_c}{U_T}}}{e^{\frac{\kappa V_c}{U_T}} + e^{\frac{\kappa V_g}{U_T}}}, \quad (2)$$

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assuming that the subthreshold slope factor k is the same for both NMOS and PMOS. If we multiply the numerator and denominator of eq. (2) by $e^{-\kappa\frac{V_{dd}}{U_T}}$ and consider eq. (1), we can rewrite $I_d$ as:

$$I_d = \frac{I_{in}}{1+\left(\frac{I_{out}}{I_g}\right)}, \tag{3}$$

where the term $I_g = I_0 e^{-\frac{\kappa(V_g - V_{dd})}{U_T}}$ represents a virtual p-type subthreshold current that is not generated by any p-FET in the circuit.

Following the log-domain paradigm, we can differentiate eq. (1) with respect to $V_c$ and combine it with the $C$ capacitor equation $C\frac{d}{dt}V_c = -(I_d - I_\tau)$ to obtain:

$$\tau\frac{d}{dt}I_{out} = -I_{out}\left(1-\frac{I_d}{I_\tau}\right), \tag{4}$$

where $\tau = \frac{CU_T}{\kappa I_\tau}$. Replacing $I_d$ from eq. (3) into eq. (4) we obtain:

$$\tau\frac{d}{dt}I_{out} + I_{out} = I_{in}\cdot\frac{(I_{out}/I_\tau)}{1+(I_{out}/I_g)}. \tag{5}$$

This is a first-order *non-linear* differential equation. Its steady state solution can be easily derived however:

$$I_{out} = \frac{I_g}{I_\tau}(I_{in} - I_\tau)\,. \tag{6}$$

If the DC component of the input signal $I_{in}$ is much greater than $I_\tau$, then $I_{out} \gg I_g$. In this condition the second term of eq.(5) reduces to $I_{in}\frac{I_g}{I_\tau}$ and we obtain a *linear* first order differential equation characteristic of linear filters, but with tunable gain $\frac{I_g}{I_\tau}$. In the Laplace domain the DPI transfer function is therefore:

$$\frac{I_{out}}{I_{in}} = \frac{I_g}{I_\tau}\cdot\frac{1}{1+\tau s}\,, \tag{7}$$

and the response of the DPI to a current pulse of amplitude $I_{in}$ arriving at $t_0$ and ending at $t_1$ is:

$$I_{out}(t) = \frac{I_g I_{in}}{I_\tau}\left(1-e^{-\frac{(t-t_0)}{\tau}}\right) + I_{out}(t_0)e^{-\frac{(t-t_0)}{\tau}}, \tag{8}$$

for the charge phase, and

$$I_{out}(t) = I_{out}(t_1)e^{-\frac{(t-t_1)}{\tau}}, \tag{9}$$

for the discharge phase, where $I_{out}(t_0)$ and $I_{out}(t_1)$ represent the initial conditions at $t_0$ and $t_1$ respectively.

For comparison, we show in Fig. 2 the classical log-domain integrator proposed by Frey [3], with equivalent functionality. This circuit's linear transfer function can be easily derived by applying the translinear principle on the $V_{gs}$ loop highlighted by the arrows in Fig. 2: given the exponential relationship between the subthreshold currents of the p-FETs and their $V_{gs}$ voltages we can write: $I_{in}\cdot I_\tau = I_{out}\cdot I_d$, where $I_{out}$ is the same as in eq. (1). Similar to the DPI analysis, differentiating $I_{out}$ with respect to $V_c$ and combining the result with the capacitor equation $C\frac{d}{dt}V_c = -(I_d - I_\tau)$ we derive the standard first order differential equation:

$$\tau\frac{d}{dt}I_{out} + I_{out} = I_{in} \tag{10}$$

As this circuit requires p-FETs with isolated wells it occupies more silicon area than the DPI.

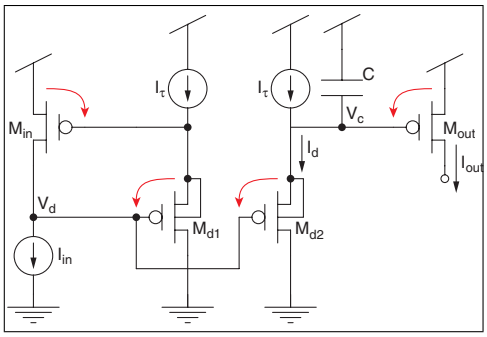


Fig. 2. Classical log-domain first order linear filter. The arrows show the $V_{gs}$ loop used for the translinear principle application.

TABLE I

DIMENSIONS OF ELEMENTS USED IN SIMULATIONS AND IN THE CIRCUIT IMPLEMENTATION. THE MOSFET ENTRIES SHOW THEIR W/L VALUES (EXPRESSED IN $\mu m/\mu$), WHILE THE (MOSCAP) CAPACITOR AREA YIELDS A CAPACITANCE OF $770fF$.

| | | | |
|---|---|---|---|
| $M_{in}$ | 6.3/3 | $M_g$ | 1/3 |
| $M_d$ | 1/3 | $M_\tau$ | 1.7/2.2 |
| $M_{out}$ | 13.5/2.2 | C | $170\mu m^2$ |

## III. SIMULATION RESULTS

We carried out SPICE simulations of the DPI circuit using $0.35\mu m$ AMS process parameters, with both $3.3V$ and $1.2V$ power supply settings. The transistor dimensions and capacitance value used for the simulations match the ones of the layout of Fig. 6 and are listed in Tab. I.

In Fig. 3 we plot the AC simulation results, in which we studied the properties of the DPI in the frequency domain, as a function of its time-constant and gain. Fig. 3(a) shows the simulation results for different values of the DPI time constant, obtained by changing the current bias $I_\tau$. Even with relatively small capacitor values (see Tab. I), the DPI integrator can produce time constants of values as long as hundreds of milliseconds, providing a very low cutoff-frequency low-pass filter. The gain of the DPI transfer function decreases in a geometric fashion, when the cut-off frequency increases linearly, because $I_\tau$ appears in transfer function's denominator (see eq. (7)). Fig. 3(b) shows the simulation results for different values of the bias voltage $V_g$, that is modulated to change the DPI's gain. The simulations confirm the theoretical analysis: different settings of $V_g$ affect the circuit's gain, while leaving the cut-off frequency unchanged. Analogous results have been obtained measuring the step response of the DPI circuit from the prototype chip we fabricated (see Sec. IV).

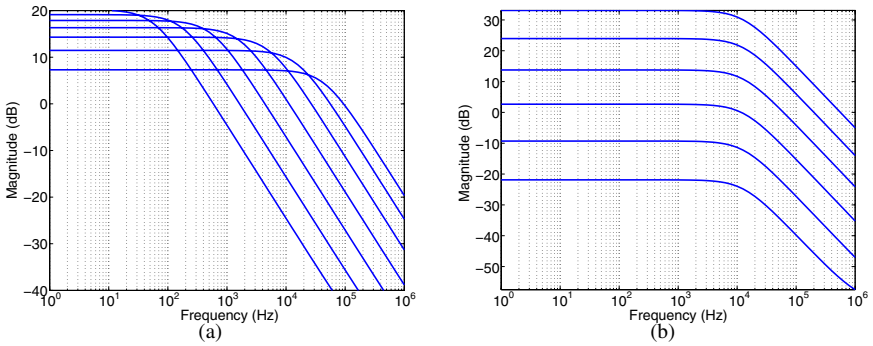


Fig. 3. Simulated DPI circuit transfer function, for a DC input current value of $10nA$; (a) plots with different values of $I_\tau$, ranging from $0.3nA$ to $1.5nA$; (b) plots with different values of $V_g$ ranging from $2.6V$ to $2.85V$.

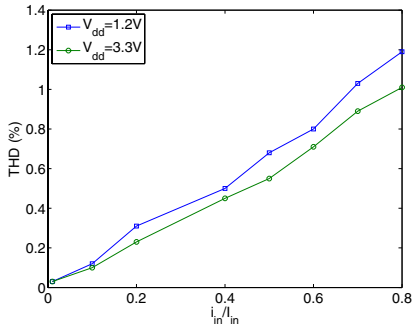


Fig. 4. Simulated Total Harmonic Distortion (THD) of DPI circuit, for two values of the supply voltage $V_{dd}$.

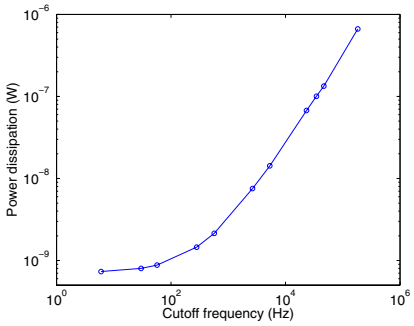


Fig. 5. Simulated power dissipation for increasing values of cutoff-frequency (set by $I_\tau$)

To test the linearity condition derived in Section II, we stimulated the DPI circuit with input currents with a DC component $I_{in}$ greater than $I_\tau$, and different values of AC component $i_{in}$. In the simulations we set $V_g = V_{dd} - 0.4V$, $I_\tau = 1$pA, $I_{in} = 10$pA, and the frequency of the AC input signal was matched to the filter's cutoff-frequency of 6Hz. In Fig.4 we plot the circuit's Total Harmonic Distortion (THD) as a function of $i_{in}/I_{in}$, for two different values of supply voltage.

The values used in the simulations above are typical in neuromorphic and biomedical applications [9], [7]. In these conditions (and with $V_{dd} = 1.2V$) the circuit dissipates less than 1nW. In Fig.5 we plot the DPI's power dissipation as a function of desired cutoff-frequency. In this experiment we set $V_g = V_{dd} - 0.4V$, fixed the $i_{in}/I_{in}$ ratio to 0.5 (for a THD of approximately 0.6%), set $I_{in} = 10I_\tau$, and varied $I_\tau$ from 1pA to 50nA. For each value of $I_\tau$ we computed the cutoff frequency, stimulated the DPI with the same frequency and measured the average power dissipation. As shown, the power consumption is proportional to the desired cutoff frequency (*i.e.* to $I_\tau$), and for frequencies lower than 100Hz it is extremely efficient.

## IV. Experimental results

In this section we present experimental results from the VLSI implementation of the DPI circuit. We fabricated a prototype VLSI chip comprising the DPI circuit among other test structures using a standard AMS $0.35\mu m$ CMOS technology.

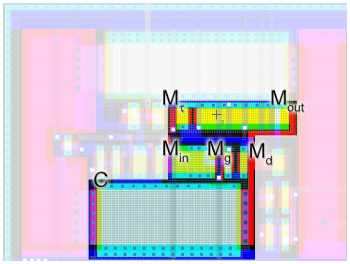


Fig. 6. Layout of the DPI test circuit. The highlighted area corresponds to the schematic of Fig. 1. The light gray area shows additional testing structures not described in this paper.

The DPI circuit does not require isolated well structures (as opposed to the circuit of Fig. 2), therefore its total layout area requirement is very small (see Fig. 6). The highlighted part of Fig. 6 corresponds to the schematic diagram of Fig. 1, and occupies an area of $464.750\mu m^2$.

We measured the DPI circuit's response to input subthreshold current pulses, for different time constant and gain settings. In Fig. 7(a) we show the circuit's response with a small $I_\tau$ current, and as a function of different $V_g$ gain settings. The background shaded lines represent the measured data, while the solid, dashed and dot-dashed curves represent fits with eq. (8) and eq. (9). The time-constant estimated from the fits does not change with $V_g$ and is of the order of seconds. In Fig. 7(b) we show the DPI response to input current pulses,

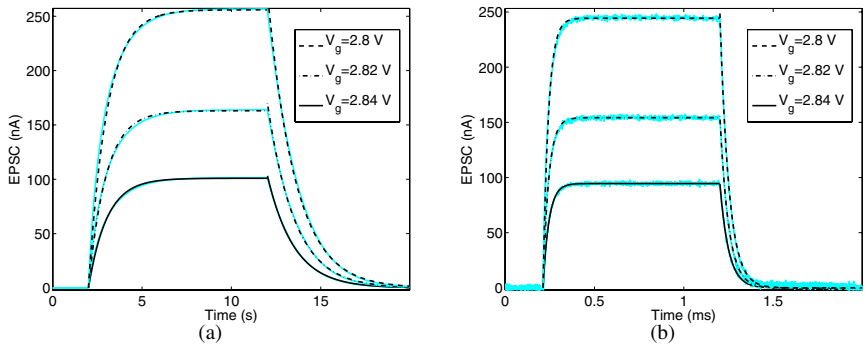


Fig. 7. Measured DPI step response for different gain and time constant settings. The shaded curves show the DPI response measured over multiple repetitions; The superimposed dashed curves represent the fits of the data with eq. (8) and eq. (9). In (a) $I_\tau$ is set to be very small (the p-FET used to generate $I_\tau$ has a $V_{gs} = 150mV$), and the circuit time constant is about one second. In (b) $I_\tau$ is set to be relatively large ($V_{gs} = 570mV$) in order to obtain a time constant of the order of $\mu s$ (note the different time scale on the abscissa axis).

TABLE II

SPECIFICATIONS OF THE DPI CIRCUIT.

| | |
|---|---|
| Area (without pads and guard rings) | $464.750\mu m^2$ |
| Power dissipation @ $I_\tau = 1pA$, $V_{dd} = 1.2V$ | $0.7nW$ |
| Supply voltage | $1.2V - 3.3V$ |
| $f_c$ tuning range | from $1Hz - -50KHz$ |
| THD @ $i_{in}/I_{in} = 0.1$ | -60dB |
| THD @ $i_{in}/I_{in} = 0.8$ | -41.4dB |

for larger values of $I_\tau$ which produce time constants of the order of micro-seconds (note the different scale on the abscissa axis). These results are in accordance with both theoretical derivation and simulation results: decreasing $V_g$ increases the DPI gain exponentially, while the DPI time constant, set by adjusting the current $I_\tau$, does not change with $V_g$.

## V. CONCLUSION

We designed and implemented a low-power current-mode log-domain integrator circuit. We described its properties by means of formal analysis, SPICE simulations, and experimental results. The results shown in each of these cases are consistent with each other and show that the DPI circuit has typical standard log-domain filter properties [3], with the additional feature of independently tunable gain. We derived from the circuit's theoretical analysis a linearity condition that sets a constraint on the ratio between the input current and the time constant current. We verified this linearity condition with SPICE simulations and estimated the THD for typical operating conditions in biomedical and neuromorphic applications [11]. Next to providing a tunable gain, the strength of this circuit is its compactness: with respect to the standard log-domain integrator [3] its layout doesn't need isolated well structures and can therefore be implemented using much less silicon area.

The design of the DPI integrator was carried out in the context of neuromorphic analog VLSI research, with the aim of realizing a faithful VLSI models of biological synapses. The result of this research lead to the design of a novel log-domain filter, with tunable gain and adjustable time constant, that differs from classical log-domain filters designed using translinear principles or log-domain synthesis techniques. The favorable properties of this novel circuit make it suitable also for other application domains such as biomedical signal processing.

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## REFERENCES

[1] C. Tomazou, F. J. Lidgey, and D. G. Haigh, Eds., *Analogue IC design: the current-mode approach*. Stevenage, Herts., UK: Peregrinus, 1990.

[2] J. Ramirez-Angulo, M. Robinson, and Sanchez-Sinencio, "Current–mode continuous-time filters: Two design aprroaches," *IEEE Transactions on Circuits and Systems*, vol. 39, no. 6, pp. 337–341, June 1992.

[3] D. Frey, "Future implications of the log domain paradigm," in *IEE Proceedings Circuits Devices Systems*, vol. 147, no. 1, February 2000, pp. 65–72.

[4] E. Seevinck, "Companding current-mode integrator: A new circuit principle for continuous-time monlithic filters," *Electronics Letters*, vol. 26, no. 24, pp. 2046–2047, Nov. 1990.

[5] D. R. Frey, "Log-domain filtering: An approach to current-mode filtering," *IEE Proceedings G: Circuits, Devices and Systems*, vol. 140, no. 6, pp. 406–416, Dec. 1993.

[6] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and N. H., "A very low-power CMOS mixed-signal ic for implantable pacemaker applications," *IEEE Jour. of Solid-State Circuits*, vol. 39, no. 12, pp. 2446–2456, Dec. 2004.

[7] S. Sol'is-Bustos, J. Silva-Martínez, F. Maloberti, and E. Sánchez-Sinencio, "A 60-db dynamic-range CMOS sixth-order 2.4-hz low-pass filter for medical applications," *IEEE Transactions on Circuits and Systems II*, vol. 47, no. 12, pp. 1391–1398, Dec. 2000.

[8] A. van Schaik and S.-C. Liu, "AER EAR: A matched silicon cochlea pair with address event representation interface," in *IEEE International Symposium on Circuits and Systems*, vol. V, no. 4213-4216, May 2005.

[9] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI array of low-power spiking neurons and bistable synapses with spike–timing dependent plasticity," *IEEE Transactions on Neural Networks*, vol. 17, no. 1, pp. 211–221, Jan 2006.

[10] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbrück, and R. Douglas, *Analog VLSI:Circuits and Principles*. MIT Press, 2002.

[11] G. Indiveri, *Smart Adaptive Systems in Silicon*. Kluwer Academic Publishers, 2004, ch. Neuromorphic Engineering, pp. 67–84.