Synthesis of log-domain integrators for silicon synapses with global parametric control

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***Abstract*— We present a series of circuits for implementing silicon synapses with biologically plausible temporal dynamics and independent global control over gain and time-constant. These types of circuits are useful for implementing synaptic dynamics in neuromorphic networks of spiking neurons, and adaptive or homeostatic mechanisms for controlling the synaptic weights. We demonstrate very compact circuit solutions, with as few as six transistors, that can be used as synaptic elements which behave like linear-integrators. The integrators are designed with translinear loops and provide an intuitive and flexible synthesis methodology.**

I. Introduction

In neuromorphic systems, a silicon synapse is typically implemented as a controlled current source that produces a post-synaptic current (EPSC) upon receiving a pulsed input from a pre-synaptic neuron. Figure. 1 shows a cartoon of a synapse on top and its corresponding VLSI model below. Specifically, the *EPSC generation* block of Fig. 1 is responsible for generating the actual synaptic current, with a biologically realistic temporal dynamics, and an amplitude proportional to its synaptic weight. Within the context of pulse based neural networks, modeling the detailed dynamics of postsynaptic currents can be a crucial step for learning neural codes and encoding spatiotemporal patterns of spikes [1]. Various VLSI models of synaptic dynamics have been implemented in the past [2], [3] and more recently [4], [5], with a comprehensive review presented in [6]. In Fig. 1, the *Synaptic weight* essentially provides a *local* control over the gain of individual EPSC. This gain can be set by a constant voltage reference, or can change with the network activity, *e.g.* to implement synaptic plasticity [7]. In such types of systems it is desirable to also have a *global* control of the gain, across all synapses connected to each neuron, to provide homeostatic and global gain control adaptive mechanisms [8]. At the same time, independent control of the time-constants is necessary to model different kinds of biological synapses, such as AMPA and NMDA.

Theoretical models of synaptic transmission have shown that a first order linear integrator with equal exponential rise and fall time is good approximation of the EPSC [9] (see Fig. 2(a)). Linear integrators can be implemented in VLSI with very few transistors when their exponential transfer function is considered. In [10] this was demonstrated with a family of 'log-domain' filters based on the translinear behavior of bipolar transistors. Since then, considerable amount of work has been done in translinear filter design, using both bipolar and

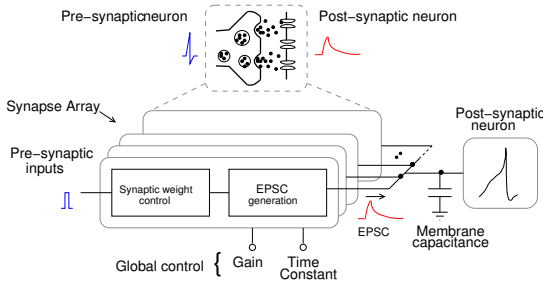

Fig. 1. A cartoon of a synapse shows the generation of post-synaptic current (red) while receiving a pre-synaptic input (blue). Corresponding model of a VLSI synapse is shown below. Each synapse in the array should have a mechanism for local control of their weights (from activity dependent modification) and also global controls for their gain and time constants.

MOS transistors. However, only few of the silicon synapses proposed in the literature take advantage of such log-domain circuits to model the temporal dynamics of real synapses [4]. Other attempts, presented in [6] and [11], uses approximations of a first order log-domain filter.

Here we address, for the first time, the problem of designing circuits for modeling synaptic dynamics using pure log-domain integrator with independent controls over gain and time-constant settings. In the following sections, we propose different possible log-domain circuit solutions, and analyze the merits of the possible implementations as a function of the area and power consumption. Since the response of such a log-domain integrator, operating as the *EPSC generation* block (Fig. 1), will be linear with the frequency of the input spikes, we can even share this unit among all the synapses of a neuron, drastically reducing the area consumption.

II. First order log-domain integrator

A canonical log-domain integrator core is shown in the dashed box of Fig. 2(b) where v_i and v_o are the input and output voltages. In order to make the circuit linear with respect to the current variables, a log-input and an antilog-output circuit are required. The simplest log (**L**, that converts a current to a logarithmic voltage) and antilog (**A**, that converts voltage to an exponential current) circuits are also shown in Fig. 2(b). The translinear loop, formed by the three transistors with arrowheads between source and gate, set the gain of the

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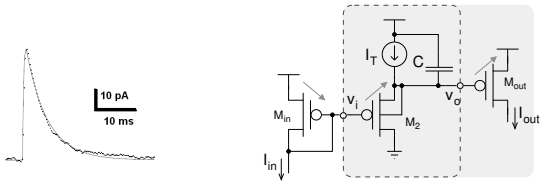


(a) (b)

Fig. 2. (a) Data fit for a typical EPSC according to the linear integrator model (adapted from [9]). (b) A basic log-domain integrator with its core shown within the dashed area. The gray shaded area represents a part of the synaptic circuit that will be used in other circuits.

integrator. Applying KCL at gate of M_{out}:

$$C\frac{dv_o}{dt} = I_s e^{\frac{\kappa(v_i - v_O)}{U_T}} - I_T \;\Rightarrow \tau \dot{I_{out}} + I_{out} = \frac{I_{in} I_s}{I_T} \qquad (1)$$

where $\tau = \frac{CU_T}{\kappa I_T}$. As seen from the equation, the gain ($\frac{I_s}{I_T}$) is a function of the temperature dependent pre-exponential current I_s. This relation originates from the unequal number of **L** and **A** elements in the translinear loop. In this circuit, the current I_T controls the time-constant of the integrator but is also affects the gain. It can be proved that the gain of a generic integrator of this type is the ratio of the currents in **L** elements to that of the **A** elements. Notice that in order to design an integrator with a gain independent of the time constant (and also without a dependence on I_s), the translinear loop should have at least three **L** and three **A** elements. Hence, it has to be biased by four current sources (say $I_{1..4}$), apart from the input (I_{in}) and the output (I_{out}), that establishes the gain (say $\frac{I_1 I_3}{I_2 I_4}$). Now, if I_3 and I_4 are both chosen to be I_T, the ratio of $\frac{I_1}{I_2}$ will give a gain independent of the time constant.

III. Translinear Loop Design

Among the various possibilities of arranging the six **L** and **A** elements in the translinear loop, we show the ones that have the same structure as the gray area in Fig. 2(b). In this way, it is easy to compare the area and power requirement. However, other alternatives that offer a better solution are also reported here. Fig. 3 shows the most obvious arrangement where three **L** elements (down arrow) are followed by three **A** elements (up arrow) in a stack. The circuit is biased to use the least number of current sources which are placed in appropriate order to provide a gain ($\frac{I_{g1}}{I_{g2}}$) independent of I_T. However, this is not a very useful solution since it requires four PMOS transistors with bulk-source connection. In bulk-CMOS process such transistors have to be placed in isolated wells that consume much larger area than individual transistors.

The circuit shown in Fig. 4(a) uses translinear elements in the order **LALLAA**. The antilog elements are biased using a clever scheme that requires fewer matched current sources [12]. As shown in Fig. 4(b), in this method known as EP (Enz-Punzenberger) bias, M_b dynamically biases the translinear element M_1 and also supplies any extra current required to be sourced from node x. This circuit is slightly smaller in size as the number of isolated wells have decreased from four

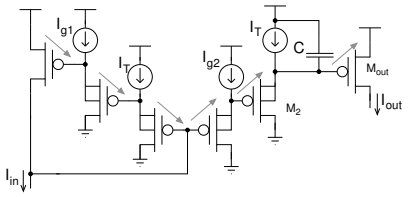
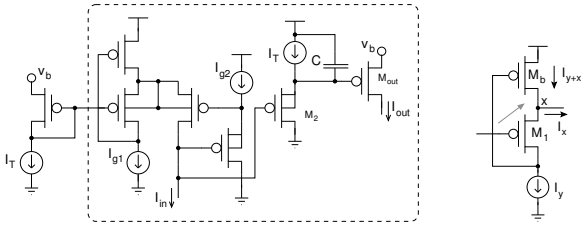


Fig. 3. The simplest translinear circuit that can be used for a synapse with independent gain and time constant control. The biasing scheme used here minimizes the requirement of matched current sources.



(a) (b)

Fig. 4. (a) A synaptic circuit that can share part of its translinear loop with other synapses. The area outside the dashed line can be common to all synapses. This circuit is biased using EP biasing [12]. (b) Negative feedback loop in EP biasing scheme.

to three. In this configuration, unlike the previous circuit, a part of the loop (outside the dashed line) can be shared with other synaptic circuits. This leads to lower power and area consumption per synapse. However, the loop should have its ends tied to a bias voltage V_b ($< V_{DD}$) which requires an extra wire to be carried to individual synapses.

Another interesting circuit can be obtained by arranging the translinear elements in **LLALAA** format (see Fig. 5). Using EP biasing and sharing more transistors among synapses, the area and power consumption per synapse are further reduced.

One very useful property of MOS translinear loops arise from alternate placement of the **L** and the**A** elements. Unlike other circuits, in these structures a translinear behavior can be obtained by connecting the bulk of all transistors to a single potential, instead of their individual sources. We exploit this property to design an even more compact linear integrator shown in Fig. 6. Here, translinear elements are placed in **ALALAL** format and uses EP biasing in three consecutive lo-

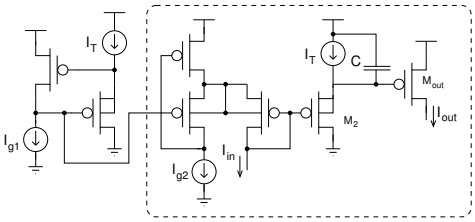


Fig. 5. More transistors can be shared among synapses thus reducing the size of each synapse. This also reduces the power consumption in each synapse as two current sources are moved out to the common area (outside dashed line).

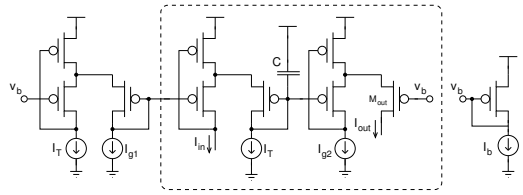


Fig. 6. Alternate placement of log and antilog translinear elements do not require the bulk-source of each transistor to be connected together. Extensive use of EP biasing scheme reduces the need for matched current sources.

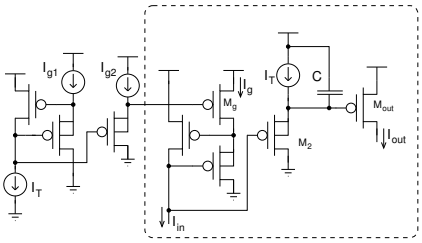


Fig. 7. Two translinear loops are used together to obtain the desired control over gain and time constant. The area consumed by the circuit inside each synapse can be reduced by connecting all the bulks to V_{DD}, in expense of a nonlinearity in the gain.

cation. Here, the output stage of the synaptic circuit is different from that of Fig. 2(b) but provides the same functionality. This circuit occupies the least area compared to all the previous solutions. The bias voltage v_b should be considerably lower than V_{DD} and can be generated using a current source (I_b) much larger than the maximum I_{out}.

A. Synapse with two Translinear loops

In all the circuits shown before a single translinear loop is used to provide the necessary ratio of currents. As shown in Fig. 7, this is also possible by using two translinear loops. In this case, the part of the circuit inside the dashed line forms a linear integrator of gain $\frac{I_g}{I_T}$. The external circuit (common to all synapses) consisting of I_{g1}, I_{g2} and I_T includes M_g in a translinear loop, thus generating I_g=$\frac{I_{g1}I_T}{I_{g2}}$. The final gain of the integrator can be written as the usual I_{g1}/I_{g2}.

This circuit includes two isolated wells, resulting in a larger area than the one shown in Fig. 5. However, due to the possibility of placing I_{g1} and I_{g2} physically close to each other, this might be a better choice when mismatch is concerned. At the same time, if bulks of the two transistors inside the dashed line (see Fig. 7) are connected to V_{DD} (instead of their respective sources), the area consumed becomes similar to that of Fig. 5. Here the gain of the integrator becomes a nonlinear function of the control currents, i.e., : $(I_{g1}/I_{g2})^{\kappa}$ (where κ is the subthreshold slope factor).

Table. I shows a comparison between the different solutions highlighting their area and power consumption requirements. The list includes a variant of Fig. 7, with all the bulks connected to V_{DD} (Fig. 7a). The number of transistors, isolated wells and bias wires represents a measure of the area covered by individual synapses. Where as the number of DC current sources is directly proportional to the power consumption. As stated earlier, reducing the number of isolated wells translates into the most compact design. Shaded in gray are the two best solutions in terms of both area and power consumption.

TABLE I

COMPARISON AMONG SYNAPSES.

Fig.	# MOS transistors	# Isolated wells	# Bias wires	# Current sources
3	10	4	4	4
4	9	3	4	3
5	6	2	2	2
6	8	0	3	2
7	6	2	2	2
7a	6	0	2	2

IV. SIMULATION RESULTS

We carried out transient analysis of the translinear circuits in $0.35\mu m$ AMS process parameters, with $3.3V$ power supply using T-Spice® simulator. We supplied a current pulse of magnitude of 5nA and 30ms wide as I_{in} to each circuit. This wide pulse is used to demonstrate the features of the log-domain integrator. In practice, the pulse width can be between hundreds of microseconds to few milliseconds, depending on how the digital input (see Fig. 1) is interfaced with the synapse. Also, the magnitude of I_{in} will be determined by the *Synaptic weight control* block.

As expected, all of the circuits described above show a behavior similar to a first-order a linear integrator. In Fig. 8 we present transient simulation results from the circuit in Fig. 7. Here two different simulation data, using the same input current pulses (dashed), are shown side by side. In the left plot, the current I_{g1} was varied between 2.5nA, 5nA and 7.5nA, keeping I_{g2} constant. In this case we set I_T to 10pA. As seen from the graph, the gain of the circuit can be independently controlled without affecting the time constant. Alternatively, in the second simulation (right), both I_{g1} and I_{g2} were kept constant while I_T was varied between 5pA to 15pA. This plot demonstrates the control of the time constant, independent of the gain. It can be noticed that the current I_{out} show a gain greater than unity even when I_{g1} and I_{g2} were equal. This is probably a result of the *early-effect* of the transistors affecting the current mirrors.

In Fig. 9(top), two consecutive current pulses (dashed) are applied to I_{in} of Fig. 6. The response of I_{out} shows a linear summation effect, as expected from a first order integrator. The use of such a circuit as a silicon synapse provides possibilities of sharing a single *EPSC generation* circuit among all synapses. The lower plot shows the response of the integrator for short input pulses (1ms). As expected, current I_{out} asymptotically reaches an average value proportional to the input frequency. Next, we measured the ratio of $I_{out,max}$ to I_{in} for different values of I_{g1}, keeping I_{g2} constant. In Fig. 10, the data in the y-axis represents the gain of the integrator ($I_{out,max}/I_{in}$) that should ideally have a linear dependence on I_{g1}. Simulation results from the circuits in Fig. 3,6,7 and 7a are plotted. All

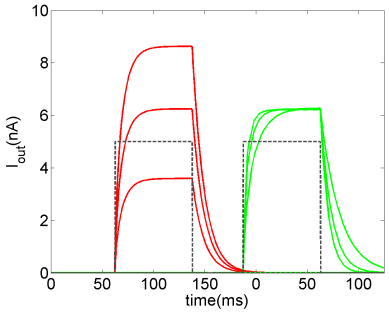


Fig. 8. Simulation data showing the temporal dynamics of I_{out} in Fig. 7 in response to a current pulse (dashed line) at I_{in}. Independent control over gain and time-constant are demonstrated on the left and the right plot respectively.

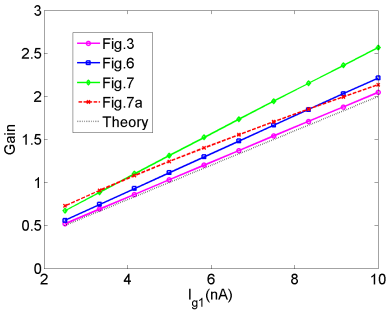


Fig. 10. Variation of gain with I_{g1} (I_{g2}=5nA) for different circuits. Fig. 7a is a variation of Fig. 7 but with all bulks connected to V_{DD}. Only 7a shows a small nonlinearity in gain.

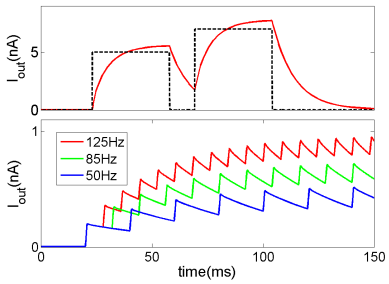


Fig. 9. Top. I_{out} shows a linear summation effect when consecutive current pulses (dashed) are applied to I_{in} (of Fig. 6). Bottom. For short current pulses (1ms wide) I_{out} asymptotically approaches an average value proportional to the input frequency.

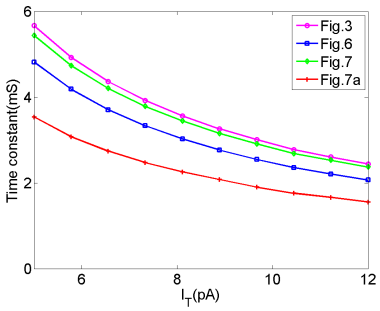


Fig. 11. Variation of time-constant with I_T for different circuits.

circuits, except Fig. 7a, demonstrate a linear behavior with Fig. 3 showing the best match with the theoretical value. In Fig. 11, we plot the change in time-constant with I_T (varied from 5pA-15pA) for the same 5nA current pulse input. The nonlinearity in the time-constant arose from the large signal nature of the input spanning many decades of current (i.e., 0-5nA). In all simulations we have purposefully used current biases varying 3 orders of magnitude (pA-nA) to demonstrate the range of values that could be used in such translinear loops. This provides a flexible method of modifying the behaviors of silicon synapses over a wide variety.

V. Conclusion

We performed a systematic analysis of log-domain linear integrators for modeling synaptic dynamics, and pointed out the circuit solutions that are ideal for use in neuromorphic networks of spiking neurons. We demonstrated the functionality of integrators with independent gain and time-constant controls, and optimized their design for area and power-consumption. In particular, the circuits of Fig. 6 and a variant of Fig. 7 are ideal for implementing densely populated bio-plausible synapses in large-scale neural networks in VLSI.

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