

Multi-terminal memtransistors from polycrystalline monolayer molybdenum disulfide

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Memristors are two-terminal passive circuit elements that have been developed for use in non-volatile resistive random-access memory and may also be useful in neuromorphic computing^{1–6}. Memristors have higher endurance and faster read/write times than flash memory^{4,7,8} and can provide multi-bit data storage. However, although two-terminal memristors have demonstrated capacity for basic neural functions, synapses in the human brain outnumber neurons by more than a thousandfold, which implies that multi-terminal memristors are needed to perform complex functions such as heterosynaptic plasticity^{3,9–13}. Previous attempts to move beyond two-terminal memristors, such as the three-terminal Widrow-Hoff memristor¹⁴ and field-effect transistors with nanoionic gates¹⁵ or floating gates¹⁶, did not achieve memristive switching in the transistor¹⁷. Here we report the experimental realization of a multi-terminal hybrid memristor and transistor (that is, a memtransistor) using polycrystalline monolayer molybdenum disulfide (MoS_2) in a scalable fabrication process. The two-dimensional MoS_2 memtransistors show gate tunability in individual resistance states by four orders of magnitude, as well as large switching ratios, high cycling endurance and long-term retention of states. In addition to conventional neural learning behaviour of long-term potentiation/depression, six-terminal MoS_2 memtransistors have gate-tunable heterosynaptic functionality, which is not achievable using two-terminal memristors. For example, the conductance between a pair of floating electrodes (pre- and post-synaptic neurons) is varied by a factor of about ten by applying voltage pulses to modulatory terminals. *In situ* scanning probe microscopy, cryogenic charge transport measurements and device modelling reveal that the bias-induced motion of MoS_2 defects drives resistive switching by dynamically varying Schottky barrier heights. Overall, the seamless integration of a memristor and transistor into one multi-terminal device could enable complex neuromorphic learning and the study of the physics of defect kinetics in two-dimensional materials^{18–22}.

Uniform polycrystalline monolayer MoS_2 films with an average grain size of $3\text{--}5\,\mu\text{m}$ were grown by chemical vapour deposition (CVD) on SiO_2/Si substrates (Methods) and characterized using X-ray photo-electron, photoluminescence and Raman spectroscopies (Fig. 1a–c and Extended Data Fig. 1). MoS_2 memtransistors were fabricated in a field-effect geometry with channel lengths (L) and widths (W) varying from $5\,\mu\text{m}$ to $150\,\mu\text{m}$ (Fig. 1d–f). Because clean interfaces between MoS_2 channels and metal electrodes were found to be critical, we developed an unconventional photolithography process based on a polymethylglutarimide (PMGI) and photoresist bilayer (Methods and Extended Data Fig. 2).

At large drain bias V_D in the sub-threshold regime (with gate bias, V_G , smaller than the threshold voltage, V_{th}), a typical memtransistor is in a high-resistance state (HRS) for the V_D sweep from $0\,\text{V}$ to $80\,\text{V}$ (sweep 1) and gradually changes to a low-resistance state (LRS)

(Fig. 2a). The device maintains the LRS during the sweep from $80\,\text{V}$ to $0\,\text{V}$ (sweep 2), is reset to the HRS during the sweep from $0\,\text{V}$ to $-80\,\text{V}$ (sweep 3), and maintains the HRS from $-80\,\text{V}$ to $0\,\text{V}$ (sweep 4). Thus, these devices act as LRS–HRS memtransistors. Figure 2b shows that when V_G is varied from $50\,\text{V}$ to $-50\,\text{V}$, both the LRS and HRS resistances change by a factor of about 10^4 and the switching ratio ($I_{\text{LRS}}/I_{\text{HRS}}$ at $V_D = 0.5\,\text{V}$) is reduced from 300 to 8 (Fig. 2e inset). Owing to the n-type MoS_2 channel, the forward-biased ($V_D > 0\,\text{V}$) device is completely off at $V_G = -50\,\text{V}$ (Fig. 2c), and the reverse-biased ($V_D < 0\,\text{V}$) device is insulating for a range of V_D values, depending on the applied V_G (Fig. 2b and Extended Data Fig. 3c). The gate leakage current (I_G) remains below $200\,\text{pA}$ during high- V_D and $-V_G$ sweeps (Extended Data Fig. 3a).

Unlike filament-based resistive switching, MoS_2 memtransistors do not require an electroforming process to train the device, although the switching ratio increases with increasing range of the V_D sweep (Extended Data Fig. 3b). The largest switching ratio, higher than 100, was obtained from devices with $W = 100\text{--}150\,\mu\text{m}$ and $L = 5\text{--}15\,\mu\text{m}$. These devices showed bipolar resistive switching, where reversing the bias polarity is essential to restoring the initial resistance states (Extended Data Fig. 3d, e). The hysteresis in the I_D – V_D curves of these MoS_2 memtransistors is fundamentally different from the commonly reported hysteresis in the transfer characteristics (I_D – V_G curves) of field-effect transistors (FETs), which are typically due to oxide-related traps^{23,24}. Instead, the I_D – V_G curves of MoS_2 memtransistors in the LRS and the HRS show large shifts (about $10\,\text{V}$) in threshold voltage, and intersect at $V_G = V_{\text{cross}}$ (Fig. 2c). Compared to the LRS, the HRS shows up to 100 times higher resistance for $V_G < V_{\text{cross}}$ and 2 times higher field-effect mobility (μ) at $V_G > V_{\text{cross}}$. Therefore, the forward-bias switching loop changes from anticlockwise (LRS to HRS) for $V_G < V_{\text{cross}}$ to clockwise (HRS to LRS) for $V_G > V_{\text{cross}}$ (Fig. 2b and Extended Data Fig. 3f).

Figure 2d shows the endurance characteristics of a MoS_2 memtransistor that was switched 475 times between the LRS and the HRS using full-sweep cycles. Within a subset of these cycles, I_D saturates at an upper value via stretched exponentials (Extended Data Figs 3g–k, 4a). Between neighbouring subsets, I_D jumps randomly to a value about 10 times smaller, followed by the same inverse exponential growth, which suggests an oxide-related trap–release process activated by large fields near the source electrode in the forward bias²³. This behaviour is reduced under reverse bias (Extended Data Fig. 4b), possibly owing to smaller band-bending near the drain electrode. Because the HRS and the LRS show similar transitory decays, the switching ratio (about 100) remains relatively constant (Fig. 2d). Individual resistance states measured within periods of up to $24\,\text{h}$ show a projected retention of distinct states for timescales of the order of years (Fig. 2e and Extended Data Fig. 4e). A statistical study of 62 devices fabricated with identical geometry on a single chip showed a logarithmic normal distribution

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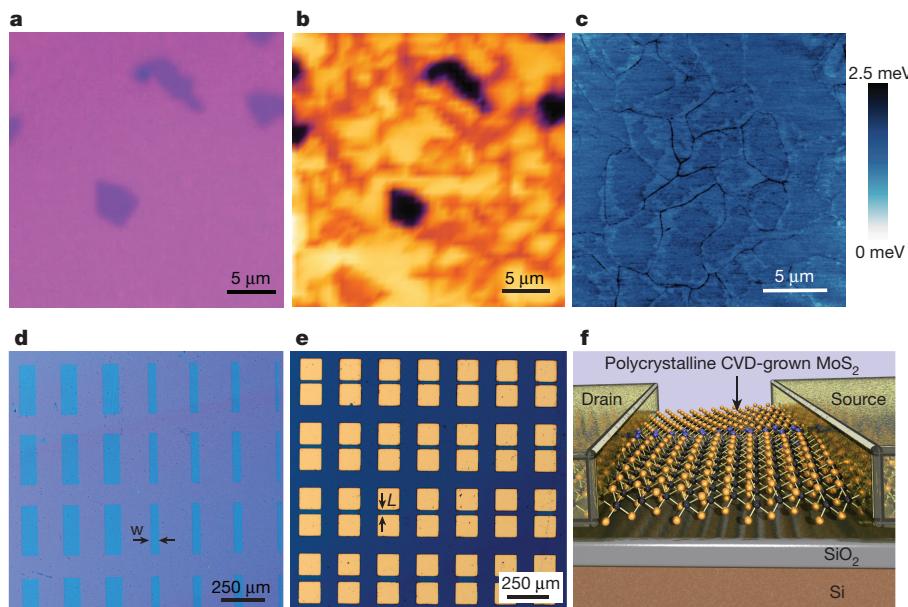


Figure 1 | Architecture of the MoS₂ memtransistor. **a**, Optical micrograph of CVD-grown polycrystalline monolayer MoS₂. The darker regions indicate sparse growth of bilayer MoS₂. **b**, Spatial mapping of photoluminescence intensity (wavelength, 670 nm) for the area shown in **a**. The darkest regions correspond to bilayer MoS₂, while the red features correspond to grain boundaries within monolayer MoS₂. **c**, Lateral force microscopy retrace image of monolayer MoS₂, showing grain boundaries

(see Extended Data Fig. 1e for topography image). The colour bar shows the photodiode readout corresponding to the cantilever tilt. **d**, Optical micrograph of an array of MoS₂ monolayer strips with varying width, *W*, etched by reactive ion etching before metallization. **e**, Optical micrograph of fabricated MoS₂ memtransistors with varying channel length, *L*. **f**, Schematic of a MoS₂ memtransistor device built on 300-nm-thick thermal SiO₂ on doped Si (gate).

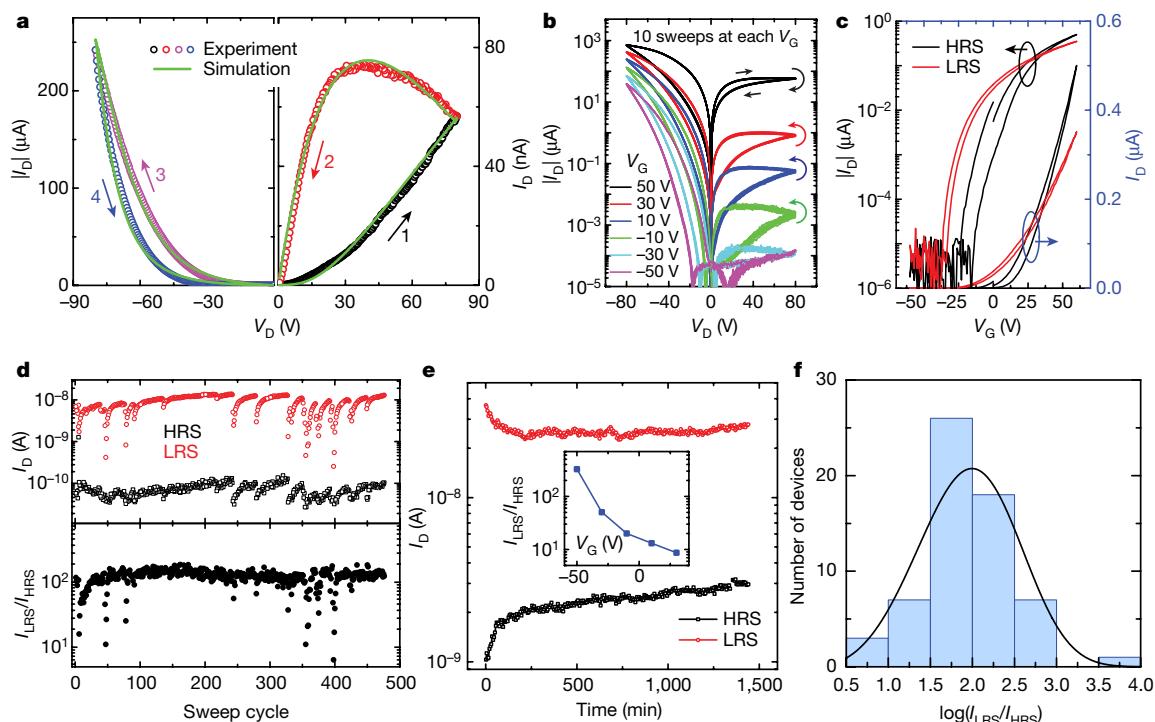


Figure 2 | Electrical characteristics of MoS₂ memtransistors. **a**, I_D – V_D curve (open circles) of a MoS₂ memristor ($L = 5\text{ }\mu\text{m}$, $W = 100\text{ }\mu\text{m}$) at gate bias $V_G = 10\text{ V}$. The direction of the drain bias (V_D) sweep 1 → 4 is indicated by coloured arrows. The sweep rate is 10 V s^{-1} throughout. The solid green line represents simulated data from a memtransistor model (see Methods and Extended Data Fig. 7). **b**, I_D – V_D curves for ten consecutive sweeps at each gate bias V_G for the same device. The switching directions are shown by the curved arrows. V_G was decreased for each consecutive sweep cycle. **c**, Transfer characteristics of a memtransistor at $V_D = 0.1\text{ V}$, showing a shift in threshold voltage and field-effect mobility from $V_{th} = 20\text{ V}$ and $\mu \approx 0.6\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ in the HRS to $V_{th} = 10\text{ V}$

and $\mu \approx 0.3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ in LRS. The curves intersect at $V_G = V_{cross} \approx 30\text{ V}$. **d**, Endurance of the current (top) and I_{LRS}/I_{HRS} (bottom) at $V_D = 0.5\text{ V}$ in the HRS (sweep 1) and the LRS (sweep 2) for 475 consecutive sweep cycles of a memristor at $V_G = 40\text{ V}$ (see Extended Data Fig. 3d–k for all I_D – V_D curves). **e**, Retention of the HRS and LRS currents at $V_D = 100\text{ mV}$ and $V_G = 0\text{ V}$ in a 24-h period. The inset shows the gate tunability of I_{LRS}/I_{HRS} . **f**, Histogram showing the largest I_{LRS}/I_{HRS} ratios of 62 distinct memtransistors ($L = 5\text{ }\mu\text{m}$, $W = 100\text{ }\mu\text{m}$). The distribution is fitted with a logarithmic normal curve with mean and variance (in $\log(I_{LRS}/I_{HRS})$) of 1.96 and 0.54, respectively.

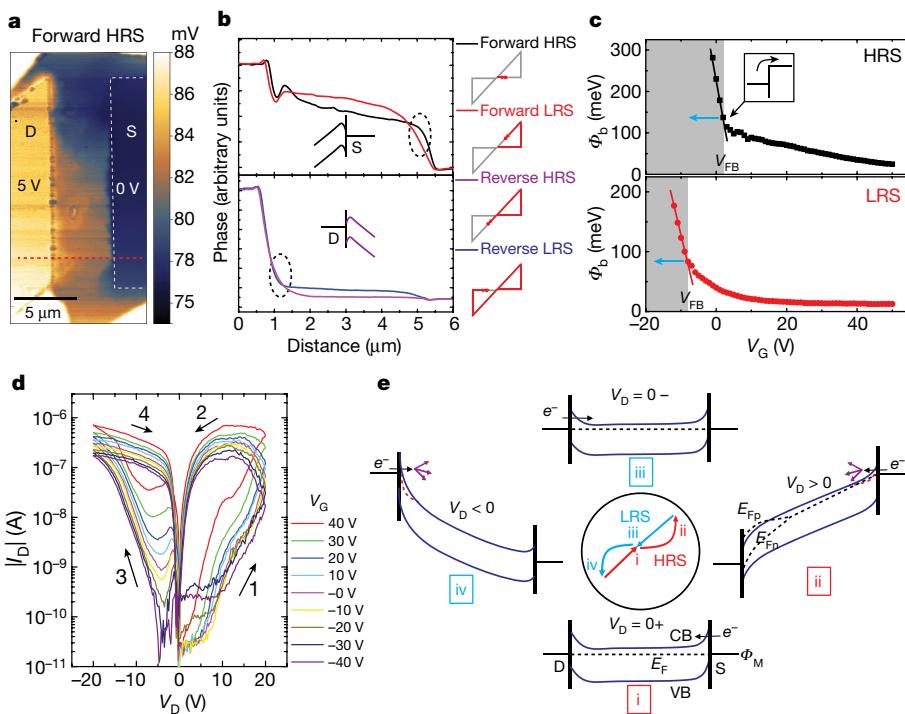


Figure 3 | In situ measurements and switching mechanism. **a**, EFM phase image of a MoS₂ memtransistor at $V_D = 5$ V, $V_S = 0$ V and $V_{\text{tip}} = 0$ V (V_{tip} , voltage of the EFM tip) in the forward-biased HRS. D, drain; S, source. **b**, Line profiles of EFM phase along the red dashed line in **a** for EFM images taken in the forward-biased HRS, forward-biased LRS, reverse-biased HRS and reverse-biased LRS, respectively, as shown schematically on the right (see Extended Data Fig. 5c–f for EFM images). The dashed-line ovals show band bending near the source electrode in forward-biased HRS and LRS, and near the drain in the reverse-biased LRS and HRS. The dip that appears near the drain in the top panel is a topography artefact. **c**, Dependence of the effective Schottky barrier height (Φ_b) on V_G , extracted from variable-temperature conductivity measurements in the HRS (top) and the LRS (bottom). For $V_G = V_{FB}$, Φ_b deviates from the linear dependence on V_G of

the thermionic emission model. The inset shows the flat-band condition at $V_G = V_{FB} = 2$ V, $\Phi_b = 125$ meV in the HRS and $V_{FB} = -8$ V, $\Phi_b = 80$ meV in the LRS (see Methods and Extended Data Fig. 6). **d**, I_D – V_D curve of an LRS–LRS MoS₂ memtransistor with an approximately 1.5-nm-thick photoresist layer under the metal contact at different V_G values. The direction of the V_D sweep 1 → 4 is indicated by arrows. V_G was decreased between V_D sweep cycles. **e**, Schematic showing the energy band diagram of an LRS–LRS memtransistor at the four switching stages shown in the centre. E_{Fp} and E_{Fn} are non-equilibrium quasi-Fermi levels for holes and electrons, respectively (see Methods and Extended Data Fig. 8 for details). CB and VB stand for conduction band and valence band, respectively. Purple arrows show defect migration. See Methods section ‘The switching mechanism’ for detailed description of stages i–iv.

of switching ratios (Fig. 2f). Device-to-device variability is attributed to spatial inhomogeneity in the CVD-grown MoS₂ film.

Owing to its two-dimensional (2D) nature, the MoS₂ channel allows the switching mechanism to be probed via *in situ* electrostatic force microscopy (EFM), as shown in Fig. 3a and b. The drain contact and conductive cantilever tip were biased independently (Extended Data Fig. 5), while the phase shift of the cantilever was recorded as the tip traced the topography profile of the MoS₂ channel and electrodes 50 nm above the surface. Because the phase shift is proportional to the square of the potential difference between the tip and the surface, the phase image provides a map of the local potential²⁰. Line profiles reveal a sharper potential drop (larger field) at the source in the forward-biased HRS compared to the forward-biased LRS, suggesting a larger contact resistance in the HRS than in the LRS (Fig. 3b). The reverse-biased HRS also shows a larger field at the drain compared to the reverse-biased LRS, although this difference is smaller, which is consistent with the smaller switching ratio at reverse bias. Multiple line profiles confirm that the differences between the HRS and LRS electric fields are consistent along the entire channel width, despite grain-boundary-induced EFM phase variations far from the contacts (Extended Data Fig. 5g–o). Because a reverse-biased Schottky diode at the source (drain) dominates I_D at $V_D > 0$ V ($V_D < 0$ V), EFM measurements provide direct evidence that the switching from the HRS to the LRS (from the LRS to the HRS) in memtransistors is caused by the dynamic tuning of Schottky barriers. Using charge-transport measurements with variable temperature (T) and assuming a 2D thermionic emission model, the effective barrier heights (Φ_b) in different states are extracted from the

slope of $\ln(I_D/T^{3/2})$ versus $1/T$ at different V_G values (Extended Data Fig. 6). Thermionic emission dominates at $V_G < V_{FB}$ (flat-band voltage), producing Φ_b values that vary linearly with V_G . Thermally assisted tunnelling through a deformed Schottky barrier begins to contribute to I_D at $V_G > V_{FB}$, resulting in deviation from the linear trend (Fig. 3c). Thus, the Schottky barrier height ($\Phi_{sb} = \Phi_b$) is extracted from the relationship $V_G = V_{FB}$. V_{FB} decreases from 2 V (HRS) to −8 V (LRS), which is consistent with a V_{th} shift of 15 V for the same device (Extended Data Fig. 6). In addition, Φ_{sb} decreases from 125 meV (HRS) to 80 meV (LRS), confirming the EFM observations.

Charge transport in MoS₂ LRS–HRS memtransistors can be described by Schottky barrier transistors (equations (1) and (2), where Φ_b is a function of an internal state variable (w) defined as the width of the region with excess dopants (Δn) (Extended Data Fig. 7a)^{1,17,25}. Tuning the Schottky barrier through increased doping near contacts ($\Phi_b \approx \sqrt{w\Delta n}$) is a standard practice in conventional FETs^{26,27}. Similarly, we propose that defects in MoS₂ act as dopants and their local migration under an applied bias is facilitated by grain boundaries, as previously observed using transmission electron microscopy and explained by *ab initio* calculations^{18,19,21}. Thus, we develop a memtransistor model in which Φ_b changes by image charge lowering and tunnelling at high biases (see Methods), resulting in the following coupled equations:

$$I_D = D \exp \left[\frac{e(V_G - V_{th})}{c_r k_B T} \right] \left[1 - \exp \left(-\frac{eV_D}{k_B T} \right) \right] \exp \left[\frac{\Phi_b(w)}{k_B T} \right] \quad (1)$$

$$\Phi_b(w) = \phi_{b0} - \frac{e}{\varepsilon_s} \sqrt{\frac{w \Delta n}{4\pi}} + \sqrt{\frac{e}{4\pi\varepsilon_s} \left[\frac{2en(\phi_{b0} + A|V_{Dl}|)}{\varepsilon_s} \right]}^{1/4} \quad (2)$$

$$\frac{\partial w}{\partial t} = EI_D \{1 - [(w - 0.5)^2 + 0.75]^p\} \quad (3)$$

where A , D , E and ϕ_{b0} are fitting parameters, and e , n , ε_s and k_B are the charge of the electron, the doping level, the dielectric constant of monolayer MoS₂ and the Boltzmann constant, respectively. Equation (3) describes the nonlinear kinetics of the dopants near the contacts by using a window function, where the degree of nonlinearity is defined by a positive integer p ($p=4$ in Fig. 2a; see Methods)²⁸. This model agrees well with the experimental data (Fig. 2a and Extended Data Fig. 7) and helps establish that the dependence of w on V_G (through I_D) is the most important feature of the MoS₂ memristor, distinguishing it from a two-terminal memristor¹⁷. To further illustrate this non-trivial switching mode, we fabricated MoS₂ devices without the PMGI-based process and used a residual photoresist layer about 1.5 nm thick as a tunnelling barrier between MoS₂ and the metal contacts (Fig. 3d, e and Extended Data Fig. 8). The tunnelling barrier minimizes pinning of the Fermi level and causes the resistance states to change abruptly upon crossing the 0 V level, resulting in LRS–LRS memristors. Overall, the switching mechanism of both LRS–HRS and LRS–LRS memristors can be described by two memristors at the contacts connected by a FET (see Methods section ‘The switching mechanism’ and Extended Data Fig. 8e).

While grain boundaries in polycrystalline MoS₂ memristors enable large switching ratios and prevent electrical breakdown by lowering Schottky barriers through dynamic defect migration, control devices without grain boundaries on single grains of CVD-grown MoS₂ show a qualitatively different, reversible breakdown phenomenon (Fig. 4a). This breakdown is marked by a sharp drop in the conductance at a voltage V_{br} during sweep 1, with a subsequent increase to the original conductance value during sweep 2. This abrupt change in charge transport is accompanied by the emergence of dendritic features (about 300–500 nm in length) close to the source electrode (upper inset in Fig. 4a and Extended Data Fig. 9a, b). Control devices reveal a linear correlation of the breakdown current (I_{br}) with the width of the source electrode (W_s) and no correlation with L (lower inset in Fig. 4a and Extended Data Fig. 9f–j). Because I_D is normally proportional to W/L , the observed deviation from this relationship at breakdown suggests that the reverse-biased Schottky diode at the source electrode creates a bottleneck for electron injection at the channel²⁷, ultimately causing electromigration at the source contact⁷. This reversible breakdown in CVD-grown MoS₂ differs from the irreversible breakdown induced in exfoliated MoS₂ by Joule heating²⁹. In the high-bias limit (± 120 V), polycrystalline MoS₂ memristors also degrade irreversibly in a manner that shows light emission in each subsequent sweep (Extended Data Fig. 9c–e).

The 2D planar geometry of the MoS₂ memristor allows the realization of multi-terminal neural circuits that mimic multiple synaptic connections in neurons. For example, in a six-terminal memristor, the conductance between any two of the four inner electrodes can be modulated by high-bias pulses applied to the two outer electrodes while the inner electrodes are disconnected (Fig. 4b and Extended Data Fig. 10). To achieve heterosynaptic plasticity, the conductance between pre-synaptic and post-synaptic neurons should be controlled by additional modulatory terminals³⁰. While this type of modulation has been demonstrated previously in Ag-based cationic memristors, this design is limited to only three terminals, owing to the requirement of filament formation across the channel^{6,30}. In contrast, the MoS₂ memristor can have a larger number of terminals and allows facile tuning through the modulation of the local Schottky barrier at each terminal (see Methods section ‘The switching mechanism’). Multi-terminal memristors also allow further tuning of heterosynaptic

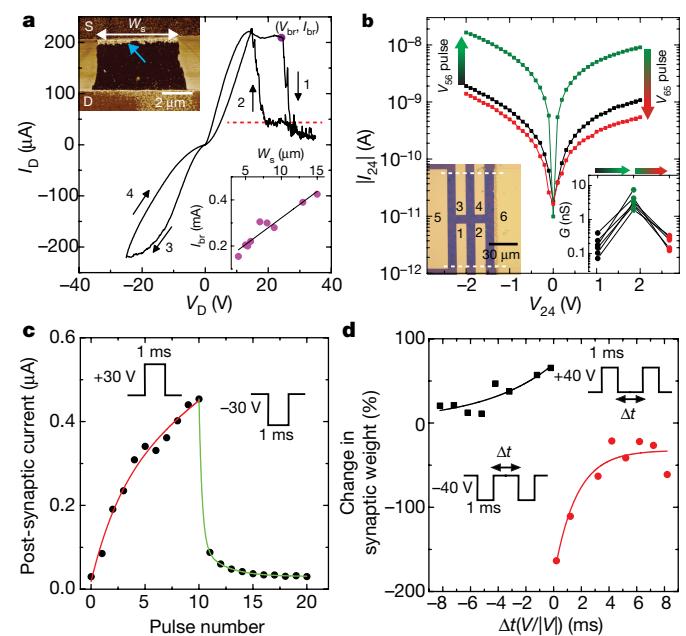


Figure 4 | Control devices and neural functions of memristors.

a, I_D – V_D curve (at $V_G = 60$ V) of a control device on an individual monolayer MoS₂ domain without grain boundaries, showing breakdown. The breakdown voltage V_{br} and breakdown current I_{br} are defined by the point preceding the sharp downward transition in sweep 1. The upper inset shows an atomic force microscopy phase image of a device with degraded material (arrow) near the source electrode. The lower inset shows the linear relation between I_{br} and the width of the source contact, W_s , for nine devices with different flake shapes (see Extended Data Fig. 9). b, I_{24} – V_{24} curve between terminals 2 and 4 of a six-terminal MoS₂ memristor (left inset) at constant $V_G = 20$ V, at the following three stages: (1) before any pulse (black); (2) after applying four pulses of -80 V between terminals 5 and 6 while terminals 1–4 were disconnected (green); and (3) after applying three pulses of -80 V between terminals 6 (drain) and 5 (ground) while terminals 1–4 were disconnected (red). The white dashed lines in the left inset show the edges of the patterned MoS₂. The right inset shows heterosynaptic plasticity, observed by reversibly changing the conductance ($G = I_{ij}/V_{ij}$) between the six combinations of four terminals ($ij = 12, 13, 14, 23, 24$ and 34) by a factor of about 10 (see Extended Data Fig. 10). c, Post-synaptic current versus pulse number, showing long-term potentiation and depression with 30 -V and -30 -V pulses. The solid lines are biexponential fits. d, Measured change in synaptic weight (normalized to maximum weight) as a function of the time interval (Δt) between paired pulses of 40 V and -40 V. The solid lines are exponential fits with time constants of 1.6 ms (red) and 5.5 ms (black) for positive and negative pulses, respectively. The inset shows the timing scheme for indirect spike-timing-dependent plasticity. $V_G = 0$ V for all measurements in c and d.

plasticity through a gate electrode, in which the switching ratio for any pair of side electrodes can be increased by about two to ten times by varying V_G from 50 V to 20 V (Extended Data Fig. 10f).

MoS₂ memristors also demonstrate long-term potentiation and depression, which mimic excitatory and inhibitory synapses in organisms (Fig. 4c). The post-synaptic current is shown to increase and decrease exponentially with the repetition of positive- and negative-bias pulses of 1 ms (Fig. 4c). The linearity of the pulse train is comparable to that of metal-oxide memristors and can be further improved by employing bipolar pulsing schemes^{11,31}. By mimicking indirect spike-timing-dependent plasticity, paired pulses separated by a time interval induce positive and negative changes in the synaptic weight using positive and negative pulses (Fig. 4d), resulting in time constants of about 2 ms and 6 ms, respectively, which are comparable to the response times of biological synapses^{11,32}.

In conclusion, MoS₂ memristors combine resistive switching with transistor gating to realize nonlinear charge transport with wide

tunability of individual states and switching ratios. In contrast to conventional devices that require single-crystal MoS₂ flakes, the utilization of polycrystalline and all-surface MoS₂ films allows the straightforward scaling of this technology to large-area integrated circuits and post-growth defect engineering. The 2D planar geometry of monolayer MoS₂ further enables the realization of multi-terminal memristors with unprecedented heterosynaptic plasticity. This technology may enable complex learning from multiple inputs in neuromorphic computing by mimicking biological neurons with multiple synapses.

Online Content Methods, along with any additional Extended Data display items and Source Data, are available in the online version of the paper; references unique to these sections appear only in the online paper.

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METHODS

CVD of MoS₂ film. Polycrystalline monolayer MoS₂ with continuous film coverage was directly grown on oxidized Si substrates by CVD using sulfur powder (Sigma-Aldrich) and molybdenum trioxide powder (MoO₃, 99.98% trace metal, Sigma-Aldrich) following the procedure reported earlier³³. Prior to growth, Si substrates were bath-sonicated for 10 min in acetone and isopropyl alcohol and subsequently cleaned under O₂ plasma (Harrick Plasma) at about 200 mTorr for 2 min with 10.2 W power applied to the radiofrequency coil. The substrates were placed downstream of 12 mg of MoO₃ powder in an alumina boat positioned in a 1-inch-diameter quartz tube furnace (Lindberg/Blue). 150 mg of sulfur powder in an alumina boat was placed about 30 cm upstream of the MoO₃ boat (outside the furnace) and was heated independently using a temperature-controlled heating belt. The tube furnace was purged using ultrahigh-purity Ar gas at 200 standard cubic centimetres per minute (scm) for 10 min. Then, the pressure was increased to 400 Torr, and the tube was evacuated to its base pressure of about 60 mTorr. The purging process was repeated twice to achieve an inert growth environment. The pressure was kept at 150 Torr with a 25-sccm flow of Ar gas during growth and cooling. After the purge process, the furnace was heated to 150 °C for 5 min and held at that temperature for 20 min to remove physisorbed contaminants from the growth environment. The furnace was then heated to 800 °C at a rate of 12 °C min⁻¹ and held at that temperature for 20 min, followed by natural cooling to room temperature. Concurrently, the heating belt around the sulfur boat was first ramped to 50 °C for 5 min and was held at that temperature for 49 min. The heating belt was then brought to 150 °C at a rate of 4.5 °C min⁻¹ and held at that temperature for an additional 23 min, after which it was allowed to cool to room temperature naturally.

Chemical characterization of monolayer MoS₂ film. The coverage and growth quality of continuous polycrystalline monolayer CVD-grown MoS₂ on 5 mm × 5 mm substrates were characterized by optical microscopy, Raman microscopy and photoluminescence spectroscopy. Raman spectra collected with a Horiba Scientific Xplora PLUS Raman microscope (Extended Data Fig. 1a) show a peak spacing of about 19 cm⁻¹ between the in-plane A_{1g} and the out-of-plane E_{2g}¹ breathing modes, thus confirming³⁴ the growth of monolayer MoS₂. Photoluminescence spectroscopy (Extended Data Fig. 1b) shows a dominant exciton A at 673 nm, typical of CVD-grown monolayer MoS₂ on SiO₂.

The chemical composition of CVD-grown polycrystalline monolayer MoS₂ films was confirmed by X-ray photoelectron spectroscopy (XPS) measurements using a Thermo Scientific ESCA Laboratory 250Xi scanning XPS instrument connected with a monochromatic K α Al X-ray line. The X-ray beam size was approximately 900 μm in diameter with an elliptical cross-section. A charge-neutralization Ar⁺ ion flood gun was also used to compensate for local electrostatic fields arising from charge buildup in the MoS₂/SiO₂ samples. All XPS spectra were analysed using Avantage software (Thermo Scientific). All Mo 3d subpeaks were fitted using floating Gaussian–Lorentzian mixing and modified Shirley background subtraction. Fitting of Mo 3d subpeaks ensured that their full-width at half-maximum values were lower than 3 eV, and doublets were also constrained to have the same full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s adventitious carbon peak at 284.8 eV. As shown in Extended Data Fig. 1c and d, the XPS spectra of the Mo 3d and S 2p orbitals are consistent with previous reports³⁵ of stoichiometric CVD-grown MoS₂ with a small amount of MoO_x in the MoS₂ film³³.

Scanning probe microscopy. The CVD-grown MoS₂ films were characterized by atomic force microscopy (AFM) in ambient conditions using an Asylum Cypher AFM system in lateral force microscopy (LFM) mode and tapping mode. For LFM, NanoWorld FMR cantilevers with a resonance frequency of about 75 kHz and contact force of approximately 5 nN were used (Fig. 1c). The LFM retrace image was acquired by scanning the tip from right to left with a contact force of about 5 nN and scan rate of 1 Hz. For the tapping mode, NanoWorld NCHR-W Si cantilevers (resonance frequency of about 320 kHz) were used (Extended Data Fig. 1e, f). A step height of 0.73 nm at the edge of a MoS₂ flake confirmed monolayer thickness. AFM measurements of individual flake devices after electrical breakdown (upper inset in Fig. 4a and Extended Data Fig. 9) were conducted in the tapping mode using a Bruker Dimension FastScan AFM system. EFM of MoS₂ memtransistors was conducted in ambient conditions using the environment cell of the Asylum Cypher AFM system and NanoWorld PointProbe EFM tips coated with PtIr (resonance frequency of about 75 kHz).

Fabrication of MoS₂ memtransistors. MoS₂ LRS–HRS memtransistors were fabricated following a photolithography process developed to minimize processing residues. First, a PMGI film was spin-coated on SiO₂/Si substrates covered by polycrystalline monolayer MoS₂ at 4500 r.p.m. for 45 s, followed by baking at 170 °C for 10 min using a hot plate. Note that the baking conditions for the PMGI layer were found to be critical. Lower temperature (160 °C) resulted in delamination during development, while higher temperature (180 °C) made it difficult to remove

PMGI during the lift-off step. Afterwards, a thin film of photoresist (S1813, Shipley Company) was spin-coated at 4000 r.p.m. for 1 min followed by another pre-baking step at 115 °C for 1 min. The bilayer resist was exposed to ultraviolet light (365 nm) for 15 s and then developed in MF319 developer (Shipley Company) for 20 s without post-baking. The samples were rinsed with deionized water and thoroughly dried before subjecting them to reactive ion etching to pattern the exposed MoS₂ film. The MoS₂ film was etched using Ar at a power of 50 W, pressure of 100 mTorr and flow rate of 50 sccm for 20 s. Subsequently, the bilayer resist mask was removed by submerging the substrate overnight in an N-methyl-2-pyrrolidone (NMP) bath heated at 80 °C. At this stage, the patterned MoS₂ strips resembled the optical image shown in Fig. 1e. Finally, source and drain electrodes were fabricated by patterning a negative photoresist NR-1000PY (Futurrex, Inc.), followed by thermal evaporation of metals (3 nm Ti and 50 nm Au) and lift-off in NMP. The MoS₂ LRS–LRS memtransistors were fabricated using the same process, but without a PMGI layer.

Electrical measurements. All room-temperature electrical measurements were carried out in a vacuum probe station at a pressure of about 5×10^{-5} Torr in the dark using a LakeShore CRX 4K probe station. Endurance, retention and neural learning tests were conducted in vacuum using pulse measure units in a Keithley 4200A-SCS Parameter Analyser and home-built LabVIEW programs. For the variable-temperature transport measurements, the devices were first switched to the HRS, and the $I_D - V_G$ data were collected at $V_D = 0.1$ V from 300 K to 75 K at a step of 25 K. A pressure of 8×10^{-7} Torr was achieved during cryogenic measurements using a built-in cryopump. The devices were allowed to heat up to room temperature overnight and were then switched to the LRS at room temperature, followed by similar variable-temperature transport measurements in the LRS. In the sub-threshold regime, the charge transport in Schottky-barrier FETs (SB-FETs) is dominated by thermionic emission^{27,36}

$$I_D = A^* T^{3/2} \exp\left(\frac{\Phi_b}{k_B T}\right) \left[\exp\left(\frac{eV_D}{k_B T}\right) - 1 \right] \quad (4)$$

where A^* is the 2D equivalent Richardson constant. The term $T^{3/2}$ comes from the 2D model (as opposed to T^2 in three dimensions). At low bias, we can extract Φ_b from the relationship of $\ln(I/T^{3/2})$ with $1/T$ at different V_G values (Extended Data Fig. 6).

Modelling the MoS₂ memtransistor. We model the memtransistor behaviour by integrating a mathematical formalism of memristive systems^{1,2,25,36,37} and memory transistors (memtransistors)¹⁷ with the charge transport model of an SB-FET^{26,27,38–41}. Memristive systems are defined as:

$$\frac{dw}{dt} = f(w, V, t) \quad \text{and} \quad I = g(w, V, t) V \quad (5)$$

where t is the time, and V and I are the input (voltage) and output (current) of the system, respectively. The internal state variable w is represented by an n -dimensional vector, g is a continuous scalar function, and f is a continuous n -dimensional vector function determined by the dimension of the vector state variable w . Subsequently, a voltage-controlled memtransistor is defined¹⁷ as:

$$\frac{dw}{dt} = f(w, V_G, V_D) \quad (6)$$

$$I_D = g(w, V_G, V_D) \quad (6)$$

$$I_G = h(w, V_G, V_D) \quad (6)$$

where h is a scalar function. The dependence of functions f , g and h on time t is determined from the voltage sweep rates. In first-order memristors, in which w is a scalar, w is usually defined by the physical region of devices with higher concentration of charged dopants or vacancies. Similarly, floating-gate metal-oxide-semiconductor FETs¹⁶ and nanoionic dielectric gated FETs¹⁵ have also been treated as first-order memtransistors, where f is a scalable function¹⁷.

In the present MoS₂ memtransistors, EFM and cryogenic-transport measurements show strong evidence of a dynamic variation in Schottky barrier height. Indeed, Schottky barrier modulation is the underlying mechanism of interface-based switching in transition-metal-oxide and ferroelectric memristors, where local segregation of mobile dopants varies the tunnelling barrier dynamically^{42–47}. Tuning the Schottky barrier by ion implantation (that is, by changing the local density of dopants) is central to contact engineering in FETs^{26,27,38,39}. Therefore, we hypothesize that the local redistribution of dopants in polycrystalline MoS₂, facilitated by grain boundaries, is the main cause of barrier modulation. Varying the density of dopants (n_1) in the region w from the contact

edge (Extended Data Fig. 9a) changes the maximum electric field ξ_m (and the effective Schottky barrier height $\Delta\Phi_{\text{image}1}$) by image charge lowering²⁷ as:

$$|\xi_m| = \frac{e}{\varepsilon_s}(n_1 w - n(d-w)) \approx \frac{en_1 w}{\varepsilon_s} \quad (7)$$

$$\Delta\Phi_{\text{image}1} \approx \frac{e}{\varepsilon_s} \sqrt{\frac{n_1 w}{4\pi}} \quad (8)$$

where d is the depletion width, n_1 is the net excess density near the contact, n is the dopant density in the channel away from the contacts and $\Delta n = n_1 - n$, as defined in Extended Data Fig. 7a. In the case of a 2D semiconductor, the metal image plane is cut by half, and thus equation (8) for a bulk semiconductor changes only by a factor of 2, which is neglected here because n_1 is a fitting parameter. However, the lowering of the image charge also depends on the drain bias V_D and the gate bias V_G and cannot be neglected at large biases. As shown previously^{27,40,41}, the easiest way to incorporate a high-bias scenario is through the geometrical factors A and B , which results in:

$$\Delta\Phi_{\text{image}2} = \sqrt{\frac{e\xi_m}{4\pi\varepsilon_s}} = \sqrt{\frac{e}{4\pi\varepsilon_s} \left(\sqrt{\frac{B(V_G - V_{\text{th}})}{t_{\text{ox}}}} + 4\sqrt{\frac{2en(\phi_{b0} + AV_D)}{\varepsilon_s}} \right)} \quad (9)$$

where t_{ox} is the thickness of the oxide dielectric. Furthermore, at high biases, tunnelling cannot be neglected and its main features can be described by the following expression⁴⁰:

$$\Delta\Phi_{\text{tunnel}} = \frac{1}{e} \left[\frac{3e\hbar(\ln 2)}{4\sqrt{2m^*}} \right]^{2/3} \left(\frac{B(V_G - V_{\text{th}})}{t_{\text{ox}}} \right)^{2/3} \quad (10)$$

where m^* is the effective mass and \hbar is the Planck constant. The net change in effective barrier height ($\Delta\Phi$) can be determined by adding equations (8), (9) and (10) to obtain

$$\Delta\Phi = \Delta\Phi_{\text{image}1} + \Delta\Phi_{\text{image}2} + \Delta\Phi_{\text{tunnel}} \quad (11)$$

$$\Delta\Phi = \frac{e}{\varepsilon_s} \sqrt{\frac{n_1 w}{4\pi}} + \sqrt{\frac{e}{4\pi\varepsilon_s} \left(\sqrt{\frac{B(V_G - V_{\text{th}})}{t_{\text{ox}}}} + 4\sqrt{\frac{2en(\phi_{b0} + AV_D)}{\varepsilon_s}} \right)} + \frac{1}{e} \left(\frac{3e\hbar(\ln 2)}{4\sqrt{2m^*}} \right)^{2/3} \left(\frac{B(V_G - V_{\text{th}})}{t_{\text{ox}}} \right)^{2/3} \quad (12)$$

A dynamically varying barrier changes the transistor's $I_D - V_D$ curve to yield a pinched hysteresis loop. Because the memristive switching ratio is largest in the sub-threshold regime (Fig. 2b), we take the following expression for the $I_D - V_D$ relationship of SB-FETs⁴⁸:

$$I_D = D \exp \left[\frac{e(V_G - V_{\text{th}})}{c_r k_B T} \right] \left[1 - \exp \left(-\frac{eV_D}{k_B T} \right) \right] \quad (13)$$

where the first exponential term gives a straight line in the logarithmic-linear plot of $I_D - V_G$ (Fig. 2c) and the corresponding (sub-threshold) slope is given by $2.3 \frac{k_B T}{e} c_r$. The second exponential term of equation (13) is responsible for the large asymmetry observed in the high-bias curve (Fig. 2a). The second term becomes negligible for $V_D > 3k_B T$, and thus the forward-bias current saturates quickly with increasing V_D (Fig. 2b). Because the variable-temperature conductivity fits well to the thermionic emission model (Fig. 3c) in the sub-threshold regime ($V_G < V_{\text{th}}$), we obtain the equation of the voltage-controlled memtransistor by multiplying equation (13) with the barrier height term from the thermionic equation (4):

$$I_D = D \exp \left[\frac{e(V_G - V_{\text{th}})}{c_r k_B T} \right] \left[1 - \exp \left(-\frac{eV_D}{k_B T} \right) \right] \exp \left(\frac{\Phi_b(w)}{k_B T} \right) \quad (14)$$

where $\Phi_b = \phi_{b0} - \Delta\Phi$, as shown schematically in Extended Data Fig. 7a, and ϕ_{b0} and Φ_b are the effective barrier heights before and after image lowering by $\Delta\Phi$, respectively. For $V_D > 0$ V, the Schottky diode at the source is reverse biased and acts as a bottleneck for the device current, whereas, for $V_D < 0$ V, the Schottky diode at the drain is reverse biased. Therefore, dopant redistribution at the two different contacts dominates in the positive and negative bias regimes, and the device can be visualized as two memristors connected by a transistor (Extended Data Fig. 8e). Local electrostatics at the two contacts is inherently asymmetric at large positive and large negative V_D values because $V_G - V_S < 0$ V at the source for $V_D > 0$ V (we note that $V_S = 0$ V), while $V_G - V_D > 0$ V at the drain for $V_D < 0$ V in the most relevant regime of $V_G < 0$ V and $|V_D| > |V_G|$. In other words, the Fermi

level of MoS₂ is located deeper into the bandgap at the source in the forward bias than at the drain in the reverse bias. Because both V_D and V_G define the Schottky barrier modulation, we need two different sets of equations for the source and drain in the forward and reverse biases. Neglecting the gate leakage current I_G (Extended Data Fig. 3a), we modify equation (6) to get equations (15), where the only differences between functions f and g and between h and j are the fitting parameters. w_d and w_s are state variables at the drain and source contacts, respectively.

$$\begin{aligned} \frac{\partial w_d}{\partial t} &= f(w_d, V_D, V_G, t) \\ \frac{\partial w_s}{\partial t} &= g(w_s, V_D, V_G, t) \\ I_D &= \begin{cases} h(w_s, V_D, V_G, t) & \text{for } V_D \geq 0 \\ j(w_d, V_D, V_G, t) & \text{for } V_D < 0 \end{cases} \end{aligned} \quad (15)$$

$$I_G = 0$$

Dynamic redistribution of dopants under bias is usually governed by drift motion. Consequently, physical models of memristors often require a nonlinear drift with the field to keep the state variable w within the boundary conditions. Dopant drift is greatly suppressed as it approaches the dimension of the device on either side, thereby avoiding irreversible hard switching or breakdown. The nonlinearity of dopant drift is usually modelled by a window function $F(w)$, and thus we obtain¹:

$$\frac{\partial w}{\partial t} = \frac{\mu R_{\text{on}} I(t)}{d^2} F(w) \quad (16)$$

where d is the range of dopant drift, μ is the dopant mobility, $I(t)$ is the current as defined in equation (5) and R_{on} is the resistance of the device when w spans the whole distance d . The window function⁴⁹:

$$F(w) = 1 - [(w - 0.5)^2 + 0.75]^p \quad (17)$$

has reproduced bipolar resistive switching in a wide range of metal-oxide memristors. It should be noted that larger p values imply larger nonlinearity. Thus, by taking $n_1 \approx \Delta n$ for large modulation in dopant density, we combine equations (12), (14), (15) and (17) to get the following set of equations for $V_D > 0$ V:

$$\begin{aligned} I_D &= D \exp \left[\frac{e(V_G - V_{\text{th}})}{c_r k_B T} \right] \left[1 - \exp \left(-\frac{e|V_D|}{c_{vd} k_B T} \right) \right] \\ &\times \exp \left(\frac{\phi_{b0} - \frac{e}{\varepsilon_s} \sqrt{\frac{w_s \Delta n}{4\pi}} + \sqrt{\frac{e}{4\pi\varepsilon_s} 4\sqrt{\frac{2en(\phi_{b0} + AV_D)}{\varepsilon_s}}}}{k_B T} \right) \end{aligned} \quad (18)$$

$$\frac{\partial w_s}{\partial t} = E I_D \{1 - [(w_s - 0.5)^2 + 0.75]^p\} \quad (19)$$

$$V_D = \begin{cases} 10t & \text{for } t = 0 \text{ s to } 8 \text{ s} \\ 80 - 10(t - 8) & \text{for } t = 8 \text{ s to } 16 \text{ s} \end{cases} \quad (20)$$

Equation (20) describes the drain bias sweep, and A , D , E and Δn are fitting parameters. The parameter $p = 4$ provides sufficient non-linearity. The geometrical factor c_{vd} has a role similar to that of c_r and limits the exponentially growing current at high negative biases. Here, we first focus on fitting the $I_D - V_D$ curve for a fixed V_G ; therefore, the terms involving the geometrical factor B in equation (12) are absorbed in the fitting parameter D . Similarity, the following set of equations describes the behaviour of the memtransistor for $V_D < 0$ V:

$$\begin{aligned} I_D &= D' \exp \left[\frac{e(V_G - V_{\text{th}})}{c_r k_B T} \right] \left[1 - \exp \left(-\frac{e|V_D|}{c_{vd} k_B T} \right) \right] \\ &\times \exp \left(\frac{\phi_{b0}' - \frac{e}{\varepsilon_s} \sqrt{\frac{w_d \Delta n}{4\pi}} + \sqrt{\frac{e}{4\pi\varepsilon_s} 4\sqrt{\frac{2en(\phi_{b0} + A'|V_D|)}{\varepsilon_s}}}}{k_B T} \right) \end{aligned} \quad (21)$$

$$\frac{\partial w_d}{\partial t} = E' I_D \{1 - [(w_d - 0.5)^2 + 0.75]^p\} \quad (22)$$

$$V_D = \begin{cases} -10(t-16) & \text{for } t = 16 \text{ s to } 24 \text{ s} \\ -80 + 10(t-24) & \text{for } t = 24 \text{ s to } 32 \text{ s} \end{cases} \quad (23)$$

where a different set of fitting parameters, A' , D' and E' , is needed owing to asymmetric electrostatics and dopant kinetics.

The experimental memtransistor characteristics are fitted well with this model, as shown in Fig. 2a. Extended Data Fig. 7b and c shows the dynamic modulation of w_d and w_s with V_D . The experimental values $c_r = 83.3$ and $V_{th} = 20$ V were used in addition to the constants $\phi_{b0} = 385$ meV and $\varepsilon_s = 4$ for monolayer⁵⁰ MoS₂. The fitting parameters in Fig. 2a are $A = 10^{-5}$, $D = 5.5 \times 10^{-9}$ and $E = 7 \times 10^{-4}$. We note that although we treat w and Δn independently in the mathematical formalism, we cannot measure them independently. Thus, we treat the product $w\Delta n$ as an internal state variable. For the fitting in Fig. 2a, we get $w_s\Delta n < 10^{10} \text{ cm}^{-2}$ and $w_d\Delta n < 3.5 \times 10^9 \text{ cm}^{-2}$ in order to get Schottky barrier heights covering the entire range of the experimental values (80–125 meV) shown in Fig. 3c (in the model, Δn has units of cm^{-3}). The fitting in Fig. 2a results in effective Schottky barrier heights ranging from 20 meV to 280 meV in the LRS and the HRS, respectively. Thus, overestimation of the simulated values in the HRS and underestimation in the LRS could result from non-idealities in the transistor transport model at high biases. Assuming that w is of the order of a few nanometres, we get maximum excess doping of $\Delta n \approx 10^{10} \text{ cm}^{-2}$, which is within the range of previous measurements of doping from MoS₂ defects⁵¹.

The smaller value of $w_d\Delta n$ compared to $w_s\Delta n$ results from the smaller fields at the drain for $V_D < 0$ V than at the source for $V_D > 0$ V, which is consistent with the smaller hysteretic loop in the reverse bias. We note that although the net device current (I_D) is determined by w_s for $V_D > 0$ V and by w_d for $V_D < 0$ V, for the device to exhibit reversible behaviour, w_d (w_s) must return to its initial value when $V_D > 0$ V ($V_D < 0$ V). This is achieved by setting appropriate fitting parameters D , E (D' , E'). In real devices, a large electric field near forward-biased Schottky diodes and redistribution of dopants to the initial configuration are also expected. Finally, by considering the first exponential term in equations (18) and (21), which contains V_G , we simulate the gate tunability of memtransistor characteristics that is consistent with the observed experimental behaviour (Extended Data Fig. 7d, e). Deviations between simulations and experiments become larger at larger V_G values owing to the decreased validity of the SB-FET model beyond the sub-threshold regime.

The switching mechanism. The switching mechanism of MoS₂ memtransistors can be understood by assuming two memristors at the source (S-memristor) and the drain (D-memristor) that are connected by a FET (Extended Data Fig. 8e). We note that gate-tunable resistive switching cannot be obtained by simply connecting two conventional memristors with a transistor. The Schottky barrier height modulation is closely connected to the operation of the SB-FET in the MoS₂ memtransistor. Thus, this distinction between memristor and transistor only serves to specify the switching mechanism. MoS₂ memtransistors with residue-free interfaces between the metal and MoS₂ (Fig. 2) undergo HRS-to-LRS switching at positive bias and LRS-to-HRS switching in negative bias and are called LRS–HRS memtransistors here. MoS₂ memtransistors with an approximately 1.5-nm-thick polymer tunnel barrier between the metal and MoS₂ (Extended Data Fig. 8a–d) undergo similar HRS-to-LRS switching at both positive and negative biases and are called LRS–LRS memtransistors. The main difference between the two types is that the LRS–HRS memtransistor retains its state while crossing the 0 V level, whereas LRS–LRS memtransistors undergo switching while crossing 0 V (Figs 2b, 3d). Both of these contrasting behaviours can be explained by the resistance table in Extended Data Fig. 8e. HD and LD are the resistance values of the HRS and LRS of the D-memristor, whereas HS and LS are the resistance values of the HRS and LRS of the S-memristor, respectively. We have $HD >> LD$ and $HS >> LS$ for both kinds of memtransistors, and their relative amplitudes determine the switching ratio. LD' and LS' are intermediate states with resistance values that differ vastly for LRS–HRS and LRS–LRS memtransistors.

For LRS–HRS memtransistors, switching events A and B dominate, while switching event C is negligible (Extended Data Fig. 8e). Switching A occurs at the bottleneck contact (that is, the source for forward bias and the drain for reverse bias), while switching B occurs at the other contact in order to restore the dopant distribution at the end of a full sweep cycle. This condition is necessitated by bipolar resistive switching, and its physical origin is well explained by the memtransistor model. Thus, intermediate states LD' and LS' have resistance values close to LD and LS, respectively.

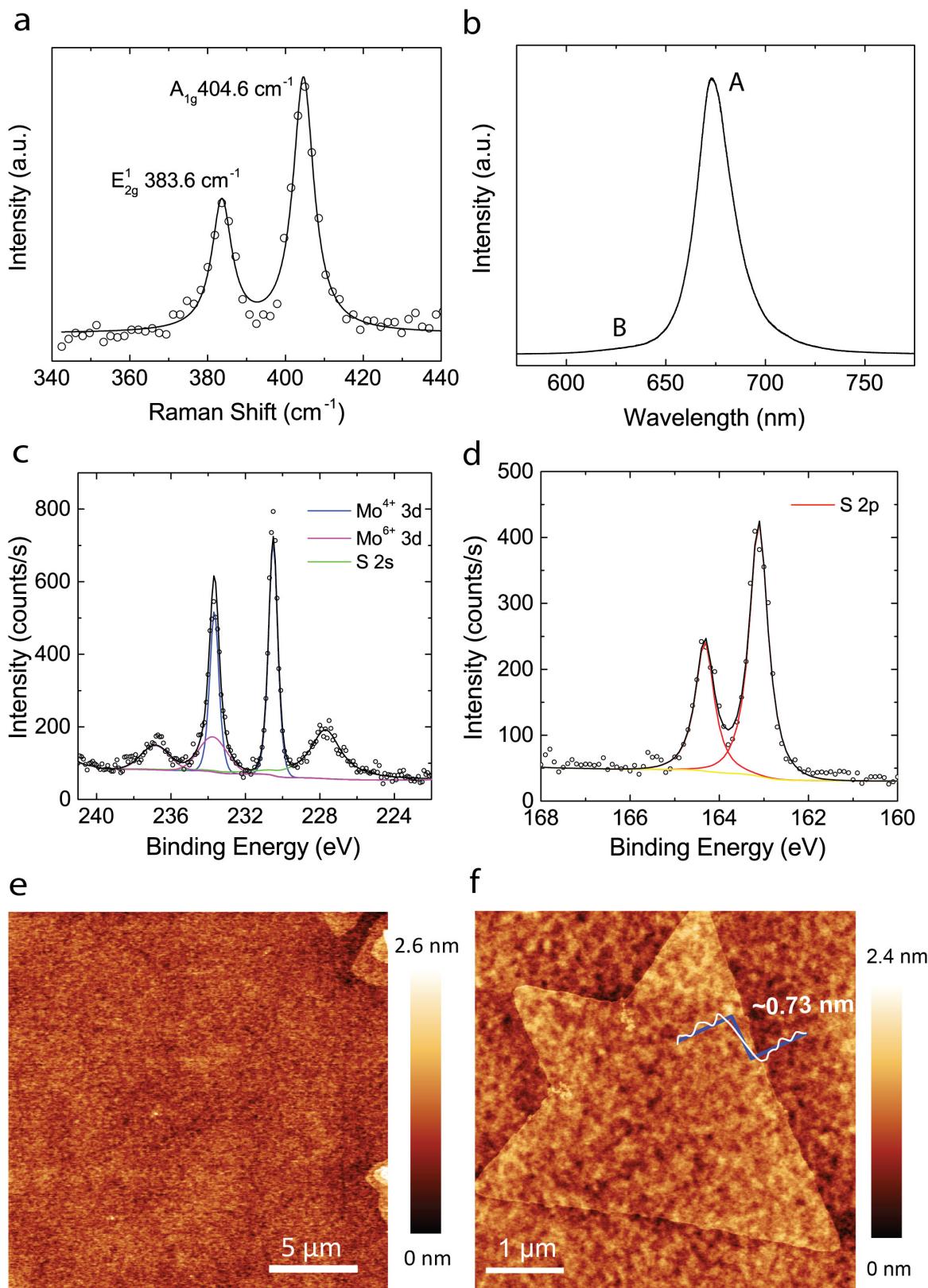
On the other hand, for LRS–LRS memtransistors, all switching events A, B and C appear. The resist layer acts at a tunnel barrier that minimizes pinning of the Fermi level of MoS₂. Similar minimization of the Fermi level has been shown in MoS₂ by employing ultrathin tunnel barriers, such as 2 nm MgO (ref. 35), 1 nm TiO₂ (ref. 52), 1.5 nm Ta₂O₅ (ref. 53) and 0.6 nm hexagonal boron nitride⁵⁴, resulting in reduction of the effective Schottky barrier height from 100 meV to 23 meV,

from 121 meV to 27 meV, from 95 meV to 29 meV and from 159 meV to 31 meV, respectively. Introduction of the tunnel barrier increases the thermionic emission contribution to the total current considerably, outweighing the additional tunnel resistance. Here, a tunnel barrier of about 1.5-nm-thick polymer resist makes the resistances of reverse-biased Schottky diodes at the source ($V_D > 0$ V) and drain ($V_D < 0$ V) more symmetric, resulting in more symmetric I_D – V_D compared to LRS–HRS memtransistors (see Figs 3d, 2b). This switching involves a dynamic negative differential resistance feature for $V_D < 0$ V common in memristors (Fig. 3d)⁵. This phenomenon increases the resistance of the intermediate states LD' and LS' so that $LD' >> LD$ and $LS' >> LS$. In other words, switching B in Extended Data Fig. 8e cannot be neglected, which explains the full switching cycles of LRS–LRS memtransistors. Compared to LRS–HRS memtransistors, LRS–LRS memtransistors show higher conductivity at the same V_D bias and switching at smaller V_G bias. This behaviour can be explained by the smaller contact resistance from the lack of Fermi level pinning or increased doping from the residue layer.

This analysis of the LRS–HRS memtransistor also sheds light on the operating mechanism of heterosynaptic multi-terminal devices (Fig. 4b). Conductance changes occur between the side electrodes 1–4 upon the application of high-bias pulses between the main electrodes (5, 6) owing to modulation of the Schottky barrier near the side electrodes. The switching ratios were observed to increase with the overlapping areas of the side electrode with the MoS₂. Thus, floating electrodes pin the Fermi level of MoS₂, and the energy level of MoS₂ under the side electrodes is lower than that of the MoS₂ region outside the side electrodes (Extended Data Fig. 10g, h), resulting in additional band-bending in the channel. Dopants are expected to be redistributed near the floating electrodes in the same manner as LRS–HRS memtransistors during sweeps 2 and 4 (Fig. 2a).

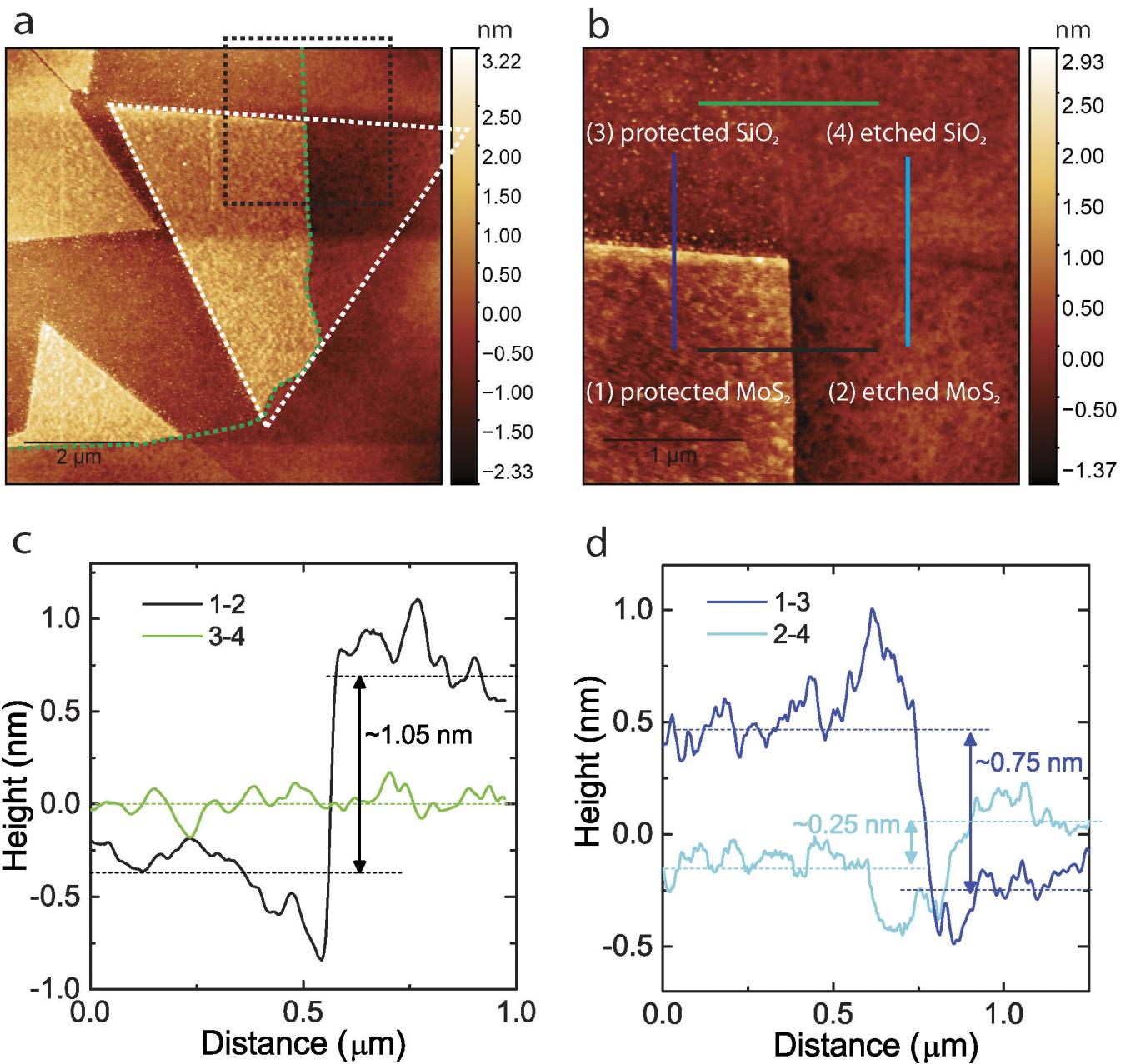
Data availability. The data that support the findings of this study are available from the corresponding author upon reasonable request.

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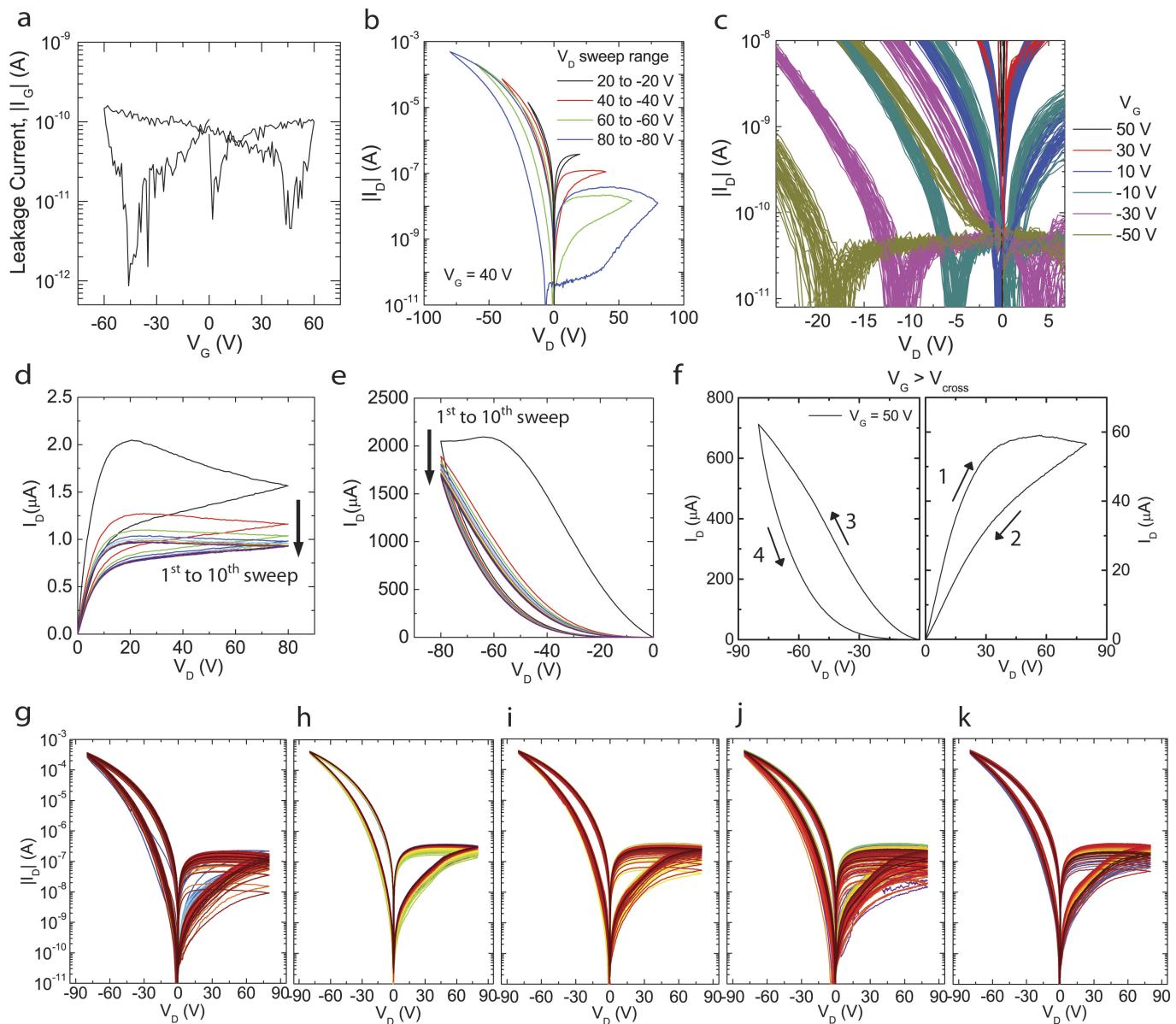
Extended Data Figure 1 | Material characterization of the MoS_2 film. **a**, Raman spectrum of CVD-grown polycrystalline monolayer MoS_2 , measured using an excitation wavelength of 532 nm. The Lorentzian peak fits correspond to the E_{2g}^1 and A_{1g} modes. **b**, Photoluminescence spectrum of MoS_2 collected with the same microscope. **c, d**, XPS spectra of MoS_2 on

a SiO_2/Si substrate, showing the Mo 3d, S 2s and S 2p peaks. **e**, AFM topography image corresponding to the lateral force microscopy image of Fig. 1c. **f**, AFM topography image of the edge of a MoS_2 flake, showing a monolayer step height of about 0.73 nm.



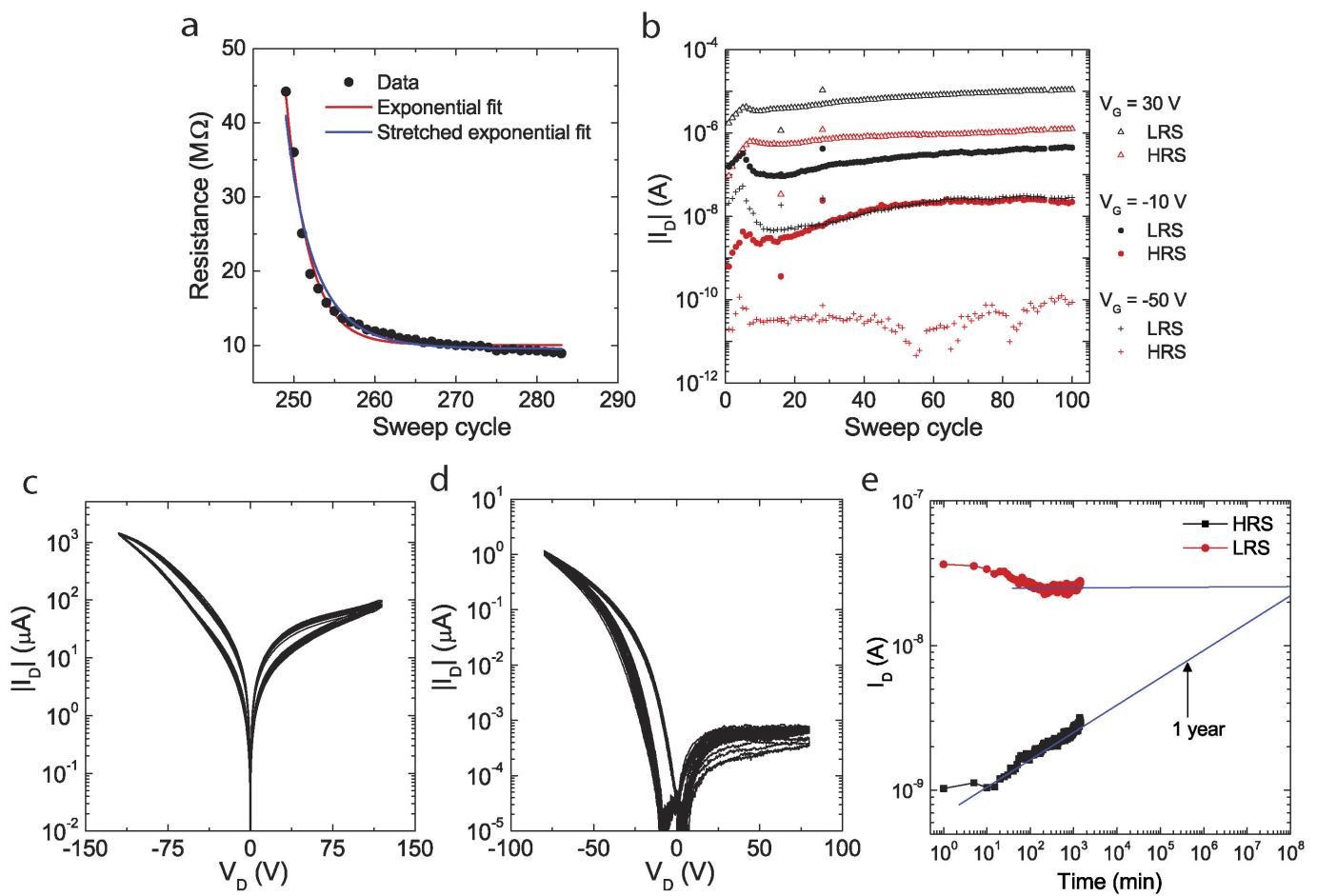
Extended Data Figure 2 | AFM analysis of a residue-free photolithography process. **a**, AFM topography image of MoS_2 crystals patterned by PMGI-assisted photolithography. The dashed green line shows the location of the edge of the patterned photoresist in the left region and the white dashed line shows the triangular MoS_2 crystal domain before reactive ion etching. **b**, Magnified AFM topography image of the region defined by the black dashed line in **a**, showing chequered

regions of protected (1) MoS_2 , (2) etched MoS_2 , (3) protected SiO_2 and (4) etched SiO_2 . **c**, Height profiles taken along the two horizontal lines in **b**, showing minimal residue left on the protected SiO_2 region. **d**, Height profiles taken along the two vertical lines in **b**, showing minor etching of SiO_2 under the etched MoS_2 region (2). The noise in the height profiles is due to surface roughness and tip artefacts.



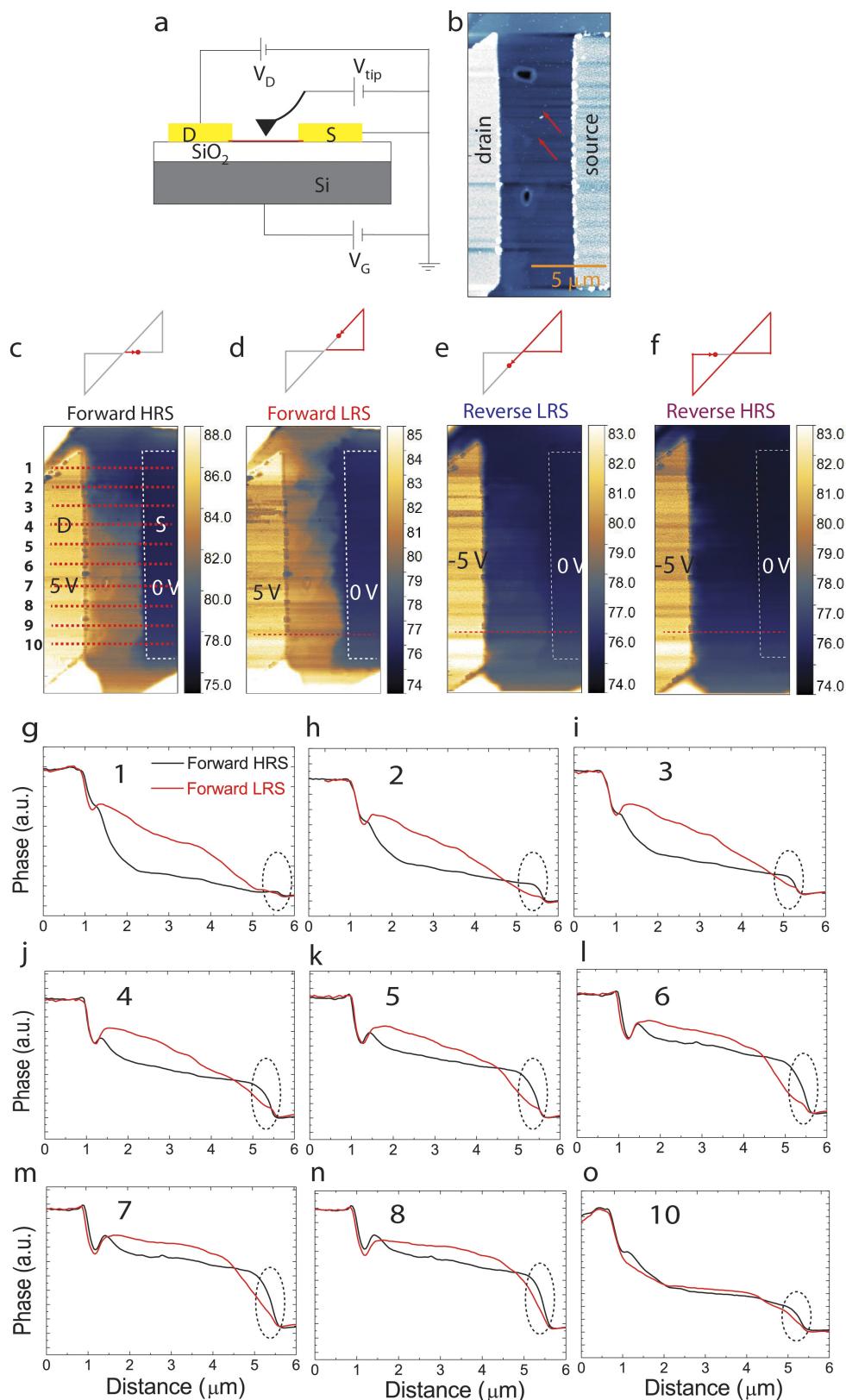
Extended Data Figure 3 | Extended electrical characteristics of the MoS₂ memtransistor. **a**, Leakage current I_G of the MoS₂ memtransistor of Fig. 2a as a function of V_G after a high-bias sweep from $V_D = 80$ V to $V_D = -80$ V. We note that the current level of 100 pA is close to the instrumentation noise floor. **b**, I_D - V_D curve of a memtransistor ($L = 15\text{ }\mu\text{m}$, $W = 150\text{ }\mu\text{m}$) for different V_D sweeps from $|20|$ V to $|80|$ V, showing increasing switching ratio with sweep range (switching ratio $>10^3$ for the range from 80 V to -80 V). **c**, Magnified view of 50 sweep cycles of the device from Fig. 2b, showing an insulating state in a range of negative V_D values that is

dependent on V_G and non-zero crossing, suggesting memcapacitance from contacts. **d**, I_D - V_D curve of a MoS₂ memtransistor during ten consecutive unipolar positive-bias sweeps from $V_D = 0$ V to 80 V. **e**, I_D - V_D curve of the same MoS₂ memtransistor during ten consecutive unipolar negative-bias sweeps from $V_D = 0$ V to -80 V. **f**, Switching from the LRS to the HRS for the MoS₂ memtransistor of Fig. 2b in the forward bias for $V_G > V_{cross}$, where $V_{cross} \approx 35$ V. I_D - V_D curve of the device of Fig. 2d during 475 voltage sweeps: **g**, sweeps 1–100; **h**, sweeps 100–200; **i**, sweeps 200–300; **j**, sweeps 300–400; **k**, sweeps 400–475.



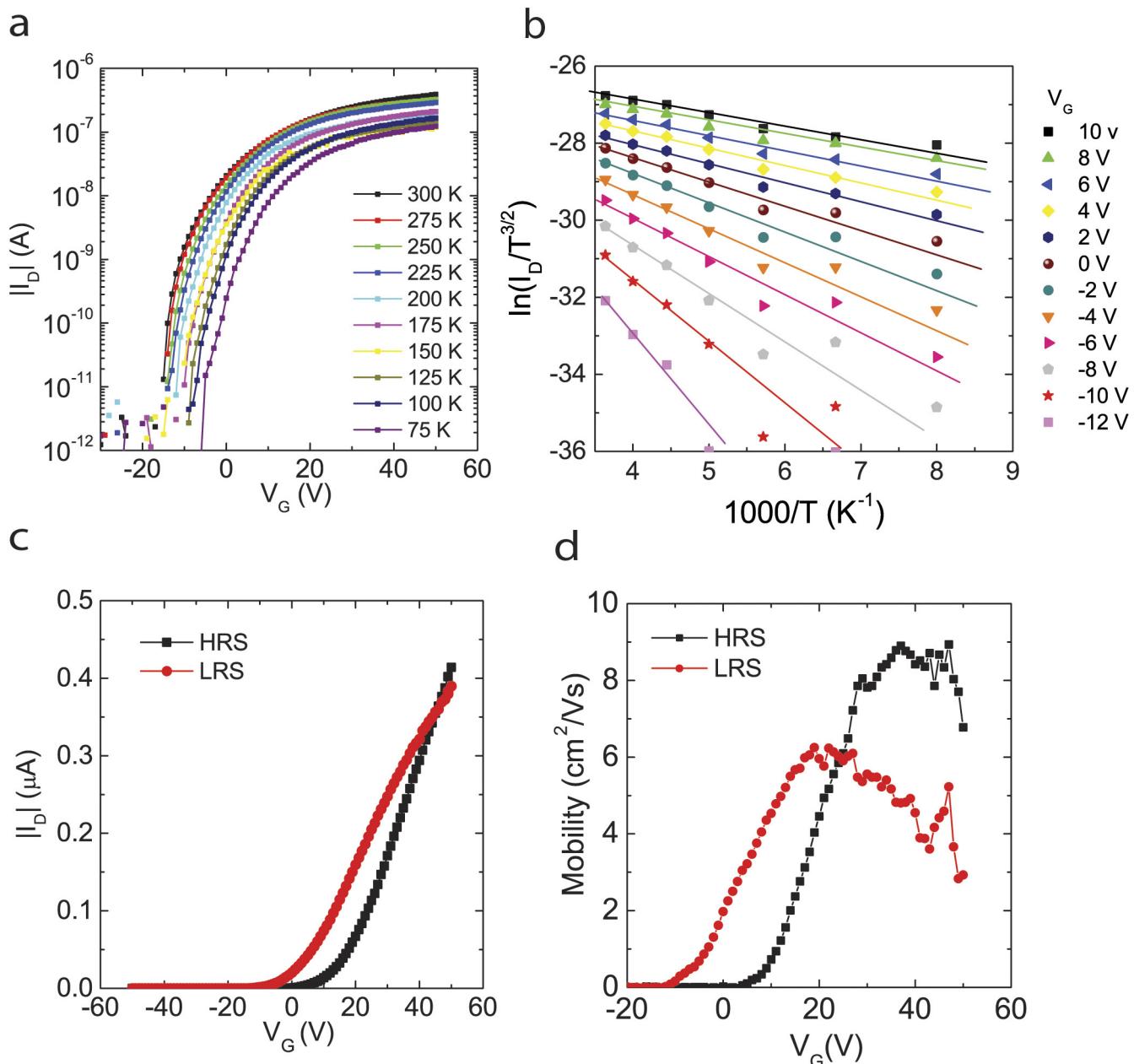
Extended Data Figure 4 | Current endurance characteristics.
a, Exponential and stretched exponential fits to a typical subset of endurance points from Fig. 2d. The stretched exponential function is defined as $I_D \approx A - Be^{C(n_0 - n)^\gamma}$, where A , B , C and n_0 are constants and $\gamma \approx 0.8$. Both the exponential and stretched exponential fits show $R^2 \approx 0.97$, but the stretched exponential shows a better fit at the tail end of the curve. **b**, Endurance characteristics of a memtransistor, showing only one exponential decay in reverse bias ($V_D = -10$ V). **c**, I_D - V_D curve

($V_G = 0$ V) of a device with $L = 20\text{ }\mu\text{m}$ and $W = 150\text{ }\mu\text{m}$, showing a negligible memristive loop (ten sweep cycles) for an unoptimized geometry. **d**, I_D - V_D curve ($V_G = 60$ V) of a device with $L = 10\text{ }\mu\text{m}$ and $W = 5\text{ }\mu\text{m}$, showing a negligible memristive loop (19 sweep cycles) for an unoptimized geometry. **e**, HRS and LRS retention characteristics from Fig. 2e plotted and extrapolated in a doubly logarithmic scale. The relaxation of the two states is faster than conventional filament-based memristors, such as TiO_2 .

**Extended Data Figure 5 | In situ EFM of a MoS_2 memtransistor.**

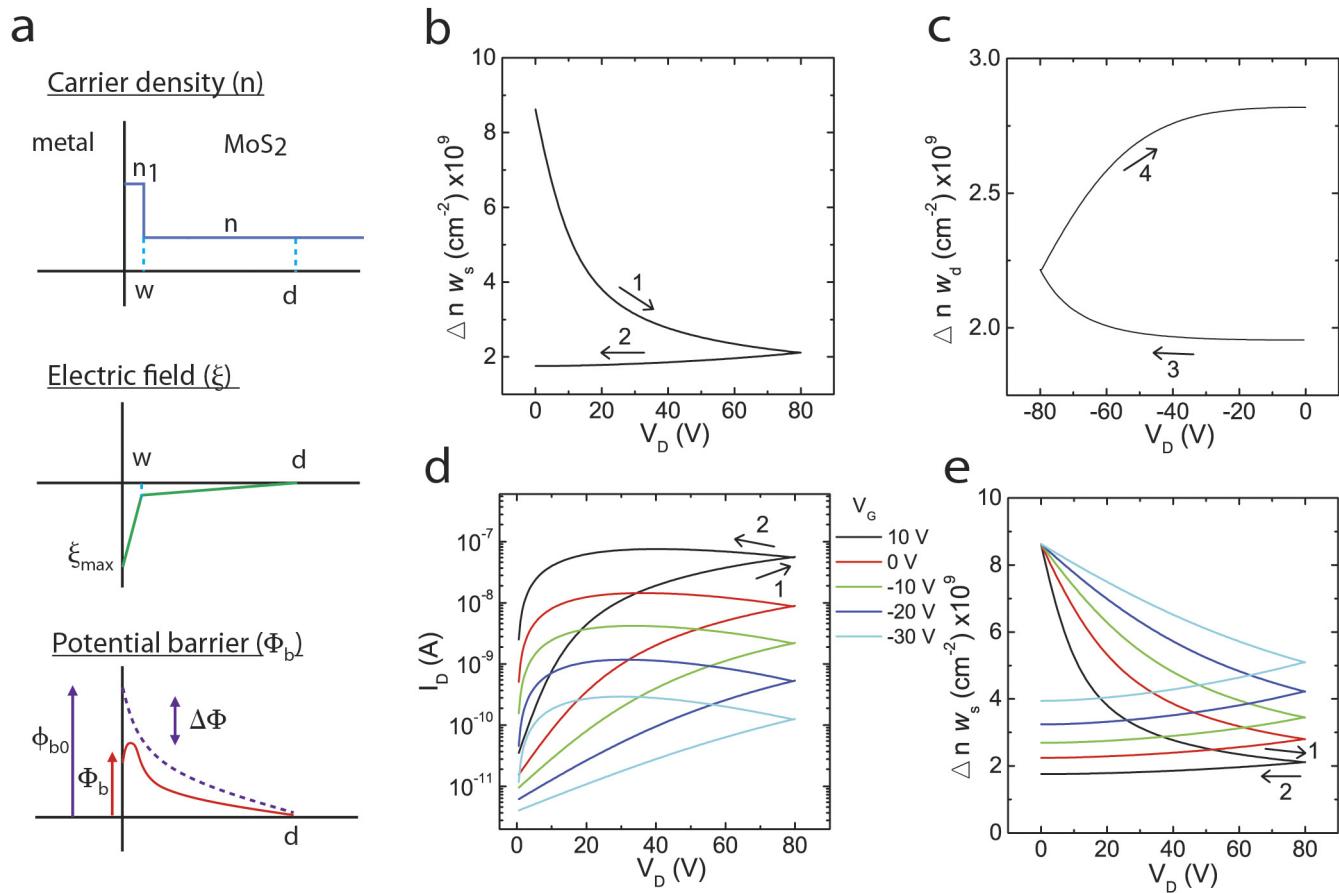
a, Schematic of the *in situ* EFM measurements of MoS_2 memtransistors. **b**, AFM topography image of the device from Fig. 3a, showing grain boundaries highlighted by red arrows. **c–f**, Reproduction of the EFM phase images of Fig. 3a in the forward HRS. **d–f**, EFM phase images in the

forward LRS, reverse LRS and reverse HRS, which were used for the line profiles shown in Fig. 3b. **g–o**, EFM phase profiles along the red dashed lines 1–8 and 10 in **c** and **d**. The EFM phase profile along line 9 is shown in Fig. 3b. All profiles are averaged over 128 lines and are normalized with the EFM phase values at the drain and source.



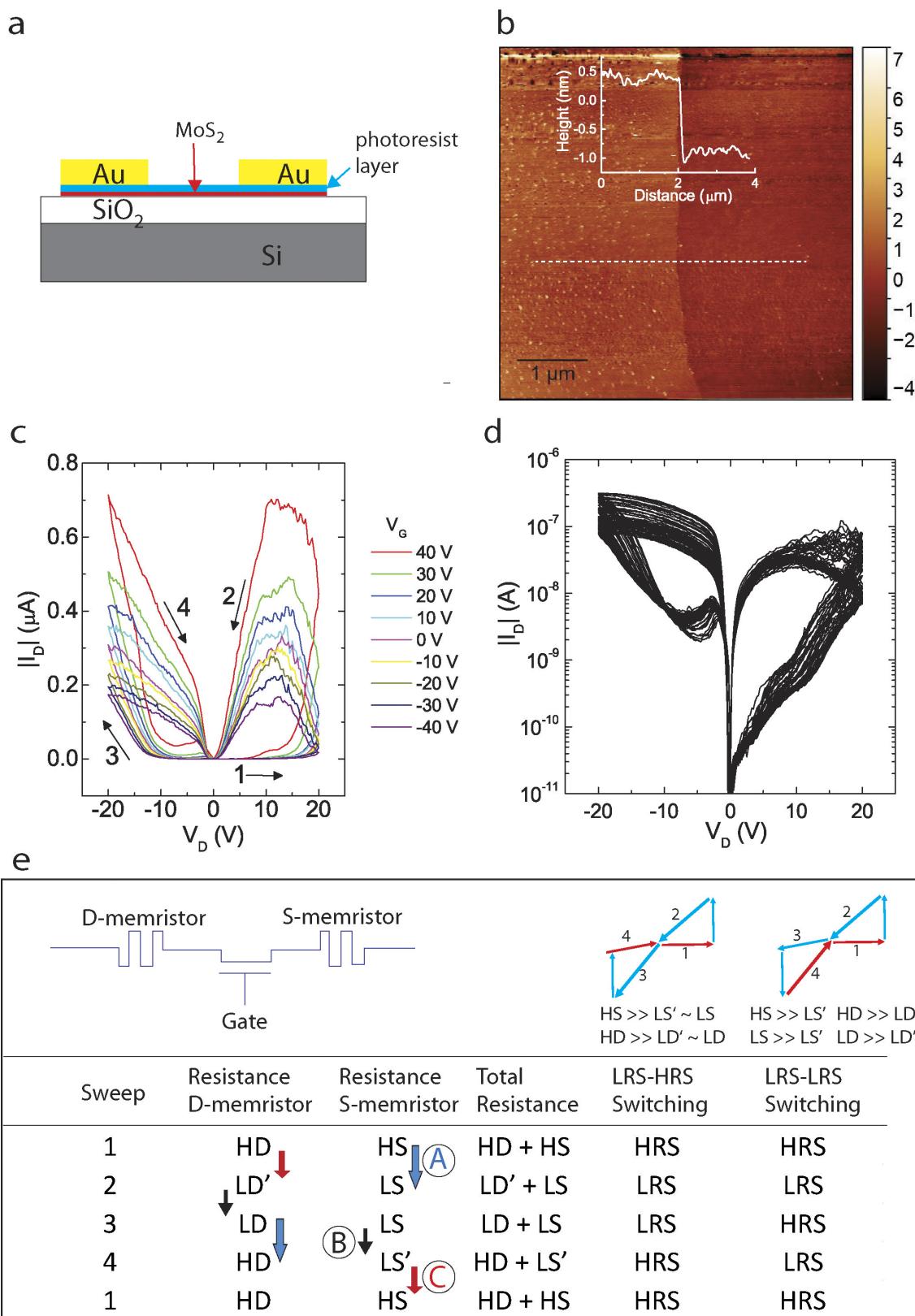
Extended Data Figure 6 | Low-temperature transport measurements of a MoS₂ memristor. **a**, I_D - V_G curve of the device shown in Fig. 3c (in the LRS) at $V_D = 0.1$ V for temperature varying from 300 K to 75 K at a step of 25 K. **b**, Plot of $\ln(I_D/T^{3/2})$ versus $1,000/T$ for different V_G values, which was used to extract the Schottky barrier height through the

thermionic emission model. **c, d**, I_D - V_G and field-effect mobility versus the V_G value of the same device in the LRS and the HRS, respectively. The crossing curves in **c** show V_{th} shifts by 15 V between the HRS and LRS and $V_{\text{cross}} \approx 42$ V.



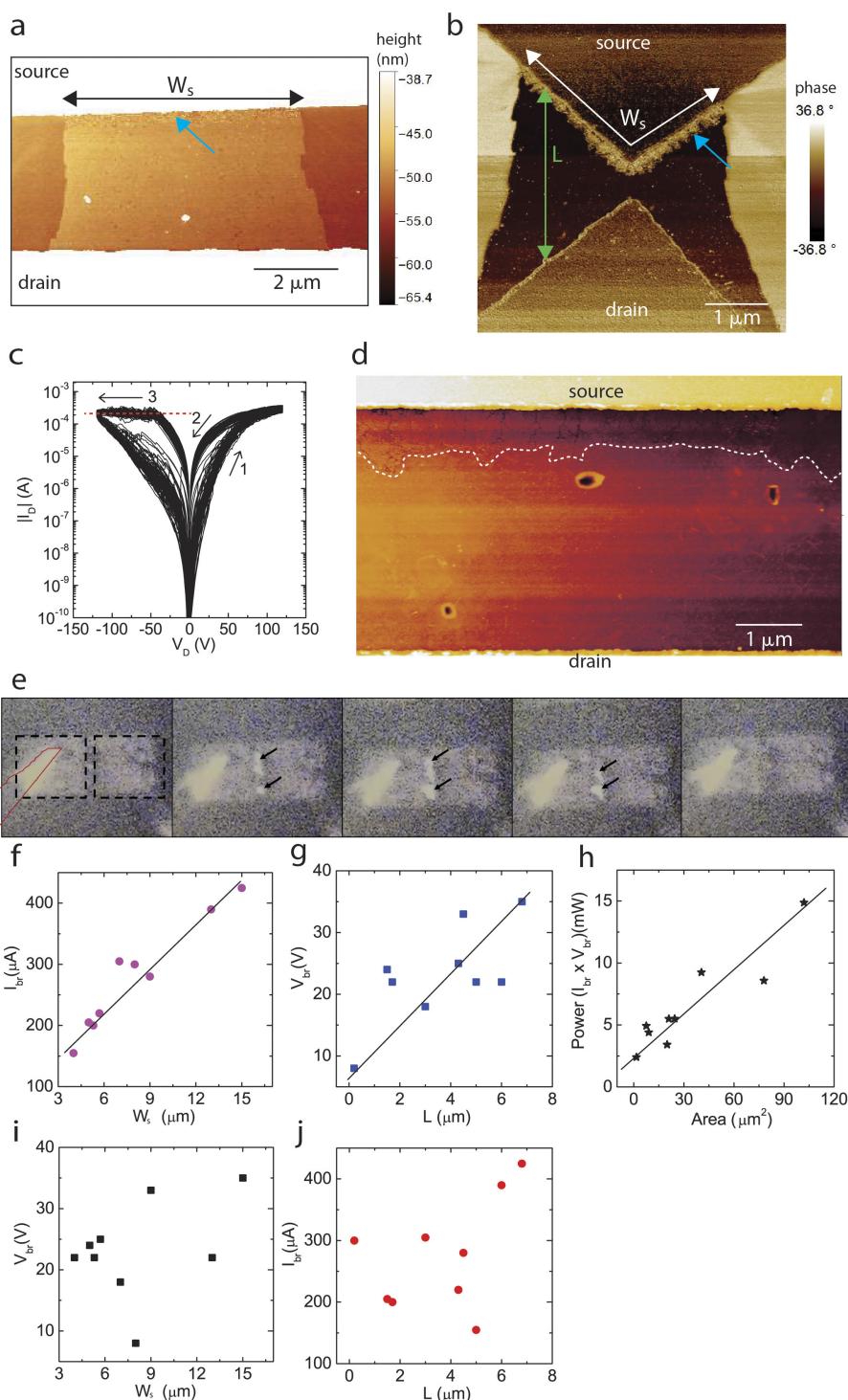
Extended Data Figure 7 | Memtransistor modelling. **a**, Schematic of the increased doping region near the contact, which results in a larger field and reduced metal–semiconductor Schottky barrier height. **b**, Simulated variation of $w_s\Delta n$ at the source contact for forward bias (sweeps 1 and 2 in Fig. 2a). **c**, Simulation variation of $w_d\Delta n$ at the drain contact for reverse

bias (sweeps 3 and 4 in Fig. 2a). **d**, Simulated I_D – V_D curve of a MoS₂ memtransistor in the forward bias with different V_G values from 10 V to –30 V. **e**, Simulated variation in $w_s\Delta n$ for the same V_G values. The key between **d** and **e** applies to both plots.



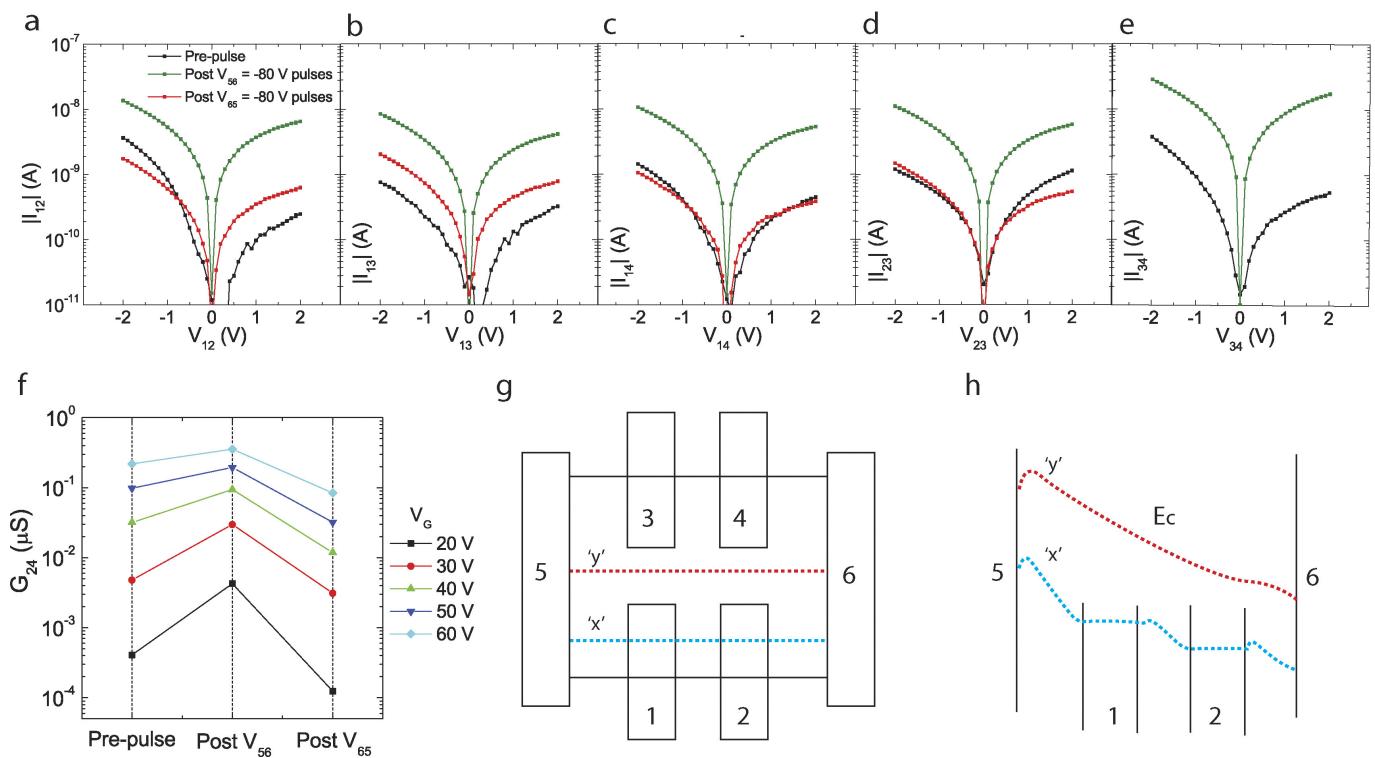
Extended Data Figure 8 | LRS–LRS MoS_2 memtransistor characteristics and mechanism. **a**, Schematic of an LRS–LRS memtransistor in which a thin photoresist layer acts as a tunnel barrier between the metal contacts and the MoS_2 film. **b**, AFM topography images, showing the step height of the remaining photoresist on a blank Si substrate after a fabrication process without using PMGI. The inset shows the height profile along the white dashed line, which reveals a thickness of about 1.5 nm. **c**, Gate-tunable $|I_D|$ – V_D curves from Fig. 3d, shown in a linear scale. **d**, $|I_D|$ – V_D

curves of 50 sweep cycles of the LRS–LRS memristor of Fig. 3d. **e**, Table showing the resistive switching characteristics of LRS–HRS and LRS–LRS memtransistors at the source and drain contacts during the four stages of a full sweep cycle. The conditions of the relative resistance values that are necessary for the two different switching behaviours are listed in the top right corner. Three kinds of resistive switching events, A, B and C, are shown by coloured arrows (see Methods section ‘The switching mechanism’ for details).



Extended Data Figure 9 | Electromigration-induced degradation in control MoS₂ devices. **a**, AFM topography images (corresponding to the upper inset of Fig. 4a), showing electromigration-induced degradation in the material (cyan arrow) near the source electrode (top). The colour scale represents height difference. **b**, AFM phase image of a device with an hourglass-shaped channel (that is, varying channel length from 5 μm to 1 μm), showing dendritic features along the entire source electrode (top). Without Schottky contacts, we expect a thermal ‘hot spot’ with high local temperature in the region of the highest electric field (V_D/L) (that is, only in the narrowest region in the centre of the channel). Absence of such localized breakdown rules out Joule heating and favours electromigration near the source contact as the dominant phenomenon. The width of the source electrode edge (W_s) is shown by the white arrows. **c**, $I_{\text{D}}-V_{\text{D}}$ curves (85 sweep cycles) of a degraded polycrystalline monolayer MoS₂ memtransistor at $V_G=0$ V ($L=5$ μm, $W=100$ μm). **d**, AFM topography

image of the device of c, showing the dendritic features above the white dashed line. **e**, A series of five successive snapshots (left to right) from a video captured by a black-and-white camera during sweep 3, as indicated by the dashed red line in c. The red outline and dashed black line in the first frame show the probe tip and electrode pads, respectively. The three middle frames show bright spots from light emission in the channel close to the source electrode (right), marked by black arrows. Light emission was observed during all 85 sweep cycles shown in c. **f**, Breakdown current I_{br} (defined in Fig. 4a), showing a linear correlation with W_s for nine single-flake control MoS₂ devices. **g**, Breakdown voltage V_{br} (defined in Fig. 4a), showing a linear correlation with L , which suggests that the potential decreases both across the channel and at the Schottky contacts. **h**, Power ($I_{\text{br}} \times V_{\text{br}}$), showing a linear correlation with the channel area ($L \times W$). **i**, V_{br} showing no correlation with W_s . **j**, I_{br} also shows no correlation with L .



Extended Data Figure 10 | Electrical characteristics of multi-terminal heterosynaptic device. **a–e**, Low-bias I_{ij} – V_{ij} curves of 5 permutations of the inner electrodes 1–4 of Fig. 4b at $V_G = 20$ V, where $ij = 12, 13, 14, 23$ and 34. I_{24} – V_{24} is shown in Fig. 4b. The key in **a** applies to all panels **a–e**. The black curves were measured before any pulsing. The green curves were measured after applying a -80 -V pulse at V_{56} (5, drain; 6, source) four times at a voltage ramping rate of 10 V s $^{-1}$. The red curves were measured after applying a -80 -V pulse at V_{65} (6, drain; 5, source) three

times at the same ramping rate. The conductance returns to the pre-pulse state for all electrode combinations. **f**, Change in the conductance between electrodes 2 and 4 (G_{24}), with V_{56} and V_{65} pulses for different V_G values showing gate tunability of heterosynaptic plasticity. **g**, **h**, Spatial profile of the MoS₂ conductance band minimum (E_c) along the two dashed lines in **g**, which pass through (*x*) and outside (*y*) the side electrodes.