"Log-Domain State-Space": A Systematic Transistor-Level Approach for Log-Domain Filtering

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***Abstract*—In this paper the properties of a low-level nonlinear continuous-time circuit element—termed a Bernoulli Cell (or Operator)—are described in a systematic way. This cell is composed of an npn BJT and an emitter-connected grounded capacitor, and is governed by a differential equation of the Bernoulli form. Although this cell has the potential for application in both linear and nonlinear analog signal processing, this paper will focus on the field of input–output linear log-domain filtering. The Bernoulli Cell can be utilized in both the analysis and synthesis of log-domain circuits. The Bernoulli Cell approach leads to the creation of a system of linear differential equations with time-dependent coefficients and state variables nonlinearly related to currents internal to the circuit; this set of equations is termed "log-domain state-space," and can be used for the synthesis of linear log-domain filters. Four design examples—including a bandpass biquad—are presented.**

***Index Terms*— Active filters, analog integrated circuits, log-domain circuits, translinear circuits.**

I. Introduction

THE operation of both translinear (TL) circuits and log-domain structures is based on the large-signal exponential characteristic of BJT's. TL circuits operate in accordance with the translinear principle (TLP) as elegantly expressed by Gilbert [1]. In general, TL circuits are not exploited for the design of frequency shaping networks, and real-time static linear and nonlinear functions seem to be their main application area [2]. The concept of log-domain signal processing was originally proposed by Adams [3] and rigorously formalized by Frey [4], [5]. Frey imposed a nonlinear (exponential) mapping on the state variables of a state-space (SS) description of a linear transfer function; the result is the creation of a set of nonlinear differential equations that can be interpreted as KCL nodal equations, yielding a novel class of circuits termed Exponential State Space (ESS) filters. Recently [6] Tsividis has classified those ESS topologies as forming part of a broader branch of structures classified as Externally Linear Internally Nonlinear (ELIN) networks.

Log-domain filters are currently attracting a great deal of theoretical and technological interest. Their operation is based on instantaneous companding [7]–[9], and they potentially offer high-frequency operation, tuneability, and extended dynamic range under low power-supply voltages [9]–[15]. Furthermore, it has been shown that the exponential dependence of MOSFET's in weak-inversion is uniquely suited for log-domain micropower applications [16], [17]. Additional performance considerations such as the noise behavior of log-domain structures and the effects of transistor nonidealities are still under investigation [10], [18]–[21].

The synthesis of log-domain filters has been addressed by Frey [5] and Perry–Roberts [22]. Frey's method (as previously outlined) is based on an ingenious exponential transformation of the SS description of a linear transfer function. The method is general, but for the implementation of filters of higher order it becomes difficult for the designer to find and manipulate the large number of state equations. The Perry–Roberts method is a more modular approach, easily extendable to the synthesis of higher-order filters. It is based on the operational simulation of LC ladder networks, with the internal signals being successively exponentiated, summed, integrated, and finally logged. In this way, a high-order signal flow graph (SFG) can be appropriately transformed for log-domain operation with the input–output linearity preserved, despite the fact that the internal signal processing is nonlinear. Although this method copes with the synthesis of a transfer function when the necessary dc-biasing conditions do not destroy the desired ac response (as is the case for a low-pass function), a modified version of this method was needed [23] for the synthesis of a bandpass biquad to be accomplished; in [23] El-Gamal and Roberts proposed the synthesis of SFG based transfer functions by means of dc-stable multi-input log-domain integrators, while in [24] they extended their approach to differential structures suitable for VHF operation.

The above methods could be characterized as "top-down" approaches, since they start from a high-level (SS or SFG) transfer function description, and end up with a circuit-level architecture of integrating nodes interconnected by TL loops. A low-level approach to log-domain filtering has been proposed based on g_m-C representations of filters [14], [25]. Furthermore, translinear strategies have also been reported [48]. An alternative low-level "bottom-up" approach allows the direct synthesis of a linear transfer function without the need for a high-level (SS or SFG) representation of the desired behavior [26], [27]. This synthesis method is based on the identification of the Bernoulli Cell. Synthesis proceeds by exploiting the form of the Bernoulli Cell capacitor currents and by implementing a continued fraction decomposition of

Manuscript received July 31, 1997; revised May 30, 1998.

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Publisher Item Identifier S 1057-7130(99)01773-5.

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the desired frequency domain transfer function. The resulting design equations are generally related to products of currents, and thus can be easily implemented using the TL principle. This approach enables the designer to take advantage of the wealth of knowledge currently developed for static translinear circuit topologies, and relate the filter parameters with products of collector currents in a direct way.

This paper aims to develop the Bernoulli Cell-based approach further and to describe how the synthesis of a linear transfer function can be simplified when the generic "log-domain state-space" is considered as starting point for the synthesis procedure [28], and is combined with a high-level (SS or SFG) representation of the desired transfer function. A further advantage of this low-level approach is to shed more light on the dc-biasing requirements inherent in log-domain structures.

This paper is organized as follows. In Section II the Bernoulli Cell is identified. Section III shows how the Bernoulli Cell can be applied to the synthesis of log-domain structures. Section III-A deals with a single Bernoulli Cell, whereas Section III-B considers the systematic interconnection of Bernoulli Cells. Section IV reveals the generic "log-domain state-space." Section V shows a means by which the log-domain state-space can be used to generate linear log-domain filters. In Section V-A the case of a lossy integrator and a low-pass biquad are considered, while in Section V-B the design issues of a lossless integrator and a bandpass biquad are addressed, along with the problem of proper dc biasing. In Section VI certain practical deviations and considerations are briefly discussed. Section VII presents simulation results corresponding to circuits described in Section V. The mathematical treatment of Sections II–V is fairly analytic to familiarize the reader with the Bernoulli Cell-based approach.

II. The Bernoulli Cell

The Bernoulli Cell is formed by connecting a grounded capacitor of value C at the emitter of a forward-biased npn BJT as illustrated in Fig. 1. Making the reasonable approximation that the BJT collector current I_C obeys the exponential law

$$I_C(t) = I_S \exp[(V_B(t) - V_C(t))/V_T] \tag{1}$$

where I_S is the technology dependent reverse saturation current, $V_B(t)$ the base voltage, $V_C(t)$ the capacitor voltage (which is equal to the emitter voltage), and V_T the thermal voltage, then

$$\frac{dV_C(t)}{dt} = \dot{V}_C(t) = i_c(t)/C = [I_C(t) - u(t)]/C. \tag{2}$$

Differentiation of (1) yields the following nonlinear differential equation:

$$\dot{I}_C(t) - \left(\frac{\dot{V}_B(t)}{V_T} + \frac{u(t)}{CV_T}\right) I_C(t) + \frac{[I_C(t)]^2}{CV_T} = 0. \tag{3}$$

Interestingly, (3) is of the well-known Bernoulli form, and so we will term the circuit of Fig. 1 a Bernoulli Cell. Despite

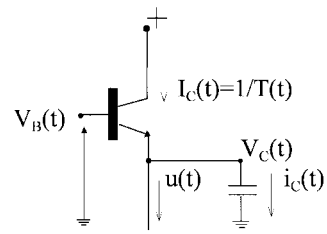

Fig. 1. The Bernoulli cell.

the fact that (3) is nonlinear, it can be linearized [29]–[32] by means of a nonlinear substitution of the form

$$I_C(t) = 1/T(t) \neq 0 \tag{4}$$

and is then transformed into

$$\frac{dT(t)}{dt} + \left(\frac{\dot{V}_B(t)}{V_T} + \frac{u(t)}{CV_T}\right) T(t) - \frac{1}{CV_T} = 0. \tag{5}$$

Equation (5) is a linear first order differential equation. Terminals $\dot{V}_B(t)$ and $u(t)$ are presently undefined and should be viewed as "free" parameters determinable by the designer. The linear operation of the cell is exploited via $T(t)$, which can be accessed/defined by manipulating $1/I_C(t)$; $1/I_C(t)$ can be easily accessed if $I_C(t)$ forms part of a suitably biased TL loop. For example, consider a translinear loop of $2m$ forward-biased base-emitter junctions:

$$cw \prod_{j=1}^{m} I_j(t) = ccw \prod_{j=1}^{m} I'_j(t) \tag{6a}$$

where $I_j(t)$ represent collector currents flowing in a clockwise (cw) direction and $I'_j(t)$ represent collector currents flowing in a counterclockwise (ccw) direction. If (for example) $I_C(t) = I_k(t)$ (i.e., cw), then $T(t) = 1/I_C(t) = 1/I_k(t)$ can be identified as

$$T(t) = \frac{1}{I_C(t)} = \frac{1}{I_k(t)} = \frac{cw \prod_{j=1}^{m,\,(j\neq k)} I_j(t)}{ccw \prod_{j=1}^{m} I'_j(t)}. \tag{6b}$$

In light of (3)–(6), we are now able to interpret in an alternative way the role of complete TL loops in log-domain structures as follows; TL loops globally linearize the differential equation which controls the Bernoulli Cell time-domain behavior, by specifying and allowing access to the parameter/condition $T(t) = 1/I_C(t)$.

III. Bernoulli Cells in Log-Domain Structures

A. A Single Input-Driven Bernoulli Cell

A convenient way of applying the Bernoulli Cell of Fig. 1 to log-domain filtering is shown in Fig. 2(a). Considering Class-A operation, the input current I_{in} is converted to a logarithmically compressed voltage V_B where

$$\dot{V}_B(t) = V_T \frac{\dot{I}_{\text{in}}(t)}{I_{\text{in}}(t)} = V_T \frac{d}{dt}[\ln(I_{\text{in}}(t))]. \tag{7}$$

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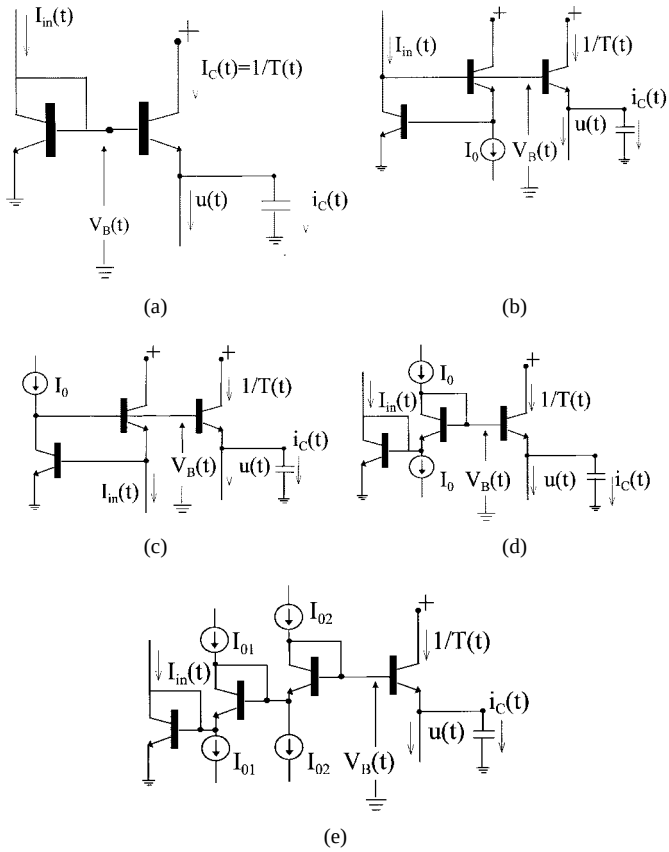

Fig. 2. (a) A single input-driven Bernoulli Cell. (b)–(e) Networks dynamically equivalent to (a).

Substitution of (7) into (5) yields

$$CV_T \frac{d}{dt}\{\ln[T(t)I_{\text{in}}(t)]\} + u(t) = \frac{1}{T(t)} = I_C(t). \quad (8)$$

Equation (8) can be interpreted as an expression for KCL at the emitter of the BJT. Thus, the capacitor current is given by

$$i_c(t) = CV_T \frac{d}{dt}\{\ln[T(t)I_{\text{in}}(t)]\}. \quad (9)$$

Obviously, this is not the only way of driving a Bernoulli Cell; in fact, any topology (*translinear or not*) which ensures that the base terminal variations $\dot{V}_B(t)$ are equal to the quantity $V_T(d/dt)\{\ln[I_{\text{in}}(t)]\}$ will realize (9). Fig. 2(b)–(e) illustrates npn-only driving topologies of this kind. It is a trivial task to show that each of these circuits ensures $\dot{V}_B(t) = V_T(\dot{I}_{\text{in}}/I_{\text{in}})$ if the base currents are neglected.

B. Interconnection of Bernoulli Cells

In Fig. 3(a), two Bernoulli Cells are connected via a voltage level shifter Q_{01}. Evidently this is not the only possible way of interconnecting two Bernoulli Cells, but this topology sustains power supply voltages at low levels. For the first cell, as previously shown,

$$C_1V_T \frac{d}{dt}\{\ln[T_1(t)I_{\text{in}}(t)]\} + u_1(t) = \frac{1}{T_1(t)} = I_{C1}(t). \quad (10)$$

The linearized expression for the second cell, according to (5), is given by

$$\frac{dT_2(t)}{dt} + \left(\frac{\dot{V}_{B2}(t)}{V_T} + \frac{u_2(t)}{C_2V_T}\right)T_2(t) - \frac{1}{C_2V_T} = 0 \quad (11)$$

where $I_{C2}(t) = 1/T_2(t)$, and C_2 is the capacitor value of the second Bernoulli Cell. From (9) is clear that

$$\frac{dV_{C1}(t)}{dt} = V_T \frac{d}{dt}\{\ln[T_1(t)I_{\text{in}}(t)]\} \quad (12)$$

and since the level shifter Q_{01} ensures that $V_{B2}(t) = V_{C1}(t) + V_T \ln(I_{01}/I_S)$, where I_{01} is a constant current source, (11) finally yields

$$C_2V_T \frac{d}{dt}\{\ln[T_2(t)T_1(t)I_{\text{in}}(t)]\} + u_2(t) = \frac{1}{T_2(t)} = I_{C2}(t). \quad (13a)$$

When the circuit of Fig. 3(a) is extended to include m interconnected Bernoulli Cells, as shown in Fig. 3(b), with level shifters ensuring $dV_{B_{k+1}}(t)/dt = (dV_{C_k}(t)/dt)(k = 1, \cdots, m-1)$, (13a) can be generalized for the last (mth) cell as

$$C_mV_T \frac{d}{dt}\{\ln[T_m(t)T_{m-1}(t)\cdots T_1(t)I_{\text{in}}(t)]\} + u_m(t) = \frac{1}{T_m(t)} = I_{Cm}(t). \quad (13b)$$

These cascaded Bernoulli cells plus level shifters can be thought of as a Bernoulli "backbone." From the previous analysis and (10)–(13), it is clear that the Bernoulli Cell capacitors $C_1, C_2, \cdots, C_m$ connected to this backbone will have currents of the form

$$\begin{aligned} i_{C1}(t) &= C_1V_T \frac{d}{dt}\{\ln[T_1(t)I_{\text{in}}(t)]\} \\ i_{C2}(t) &= C_2V_T \frac{d}{dt}\{\ln[T_2(t)T_1(t)I_{\text{in}}(t)]\} \\ &\cdots \\ i_{Cm}(t) &= C_mV_T \frac{d}{dt}\{\ln[T_m(t)\cdots T_2(t)T_1(t)I_{\text{in}}(t)]\} \\ &= C_mV_T \frac{d}{dt}\left\{\ln\left[\left[\prod_{j=1}^{m} T_j(t)\right] I_{\text{in}}(t)\right]\right\}. \end{aligned} \quad (14a)$$

Substituting the positive products $T_k(t)\cdots T_1(t)I_{\text{in}}(t)(k = 1, \cdots, m)$ for a new variable $w_k(t)$, i.e.,

$$w_k(t) = \left[\prod_{j=1}^{k} T_k(t)\right] I_{\text{in}}(t) = T_k(t)w_{k-1}(t) \quad (14b)$$

(14a) take the form

$$\begin{aligned} i_{C1}(t) &= C_1V_T \frac{d}{dt}\{\ln[w_1(t)]\} \\ i_{C2}(t) &= C_2V_T \frac{d}{dt}\{\ln[w_2(t)]\} \\ &\cdots \\ i_{Cm}(t) &= C_mV_T \frac{d}{dt}\{\ln[w_m(t)]\}. \end{aligned} \quad (14c)$$

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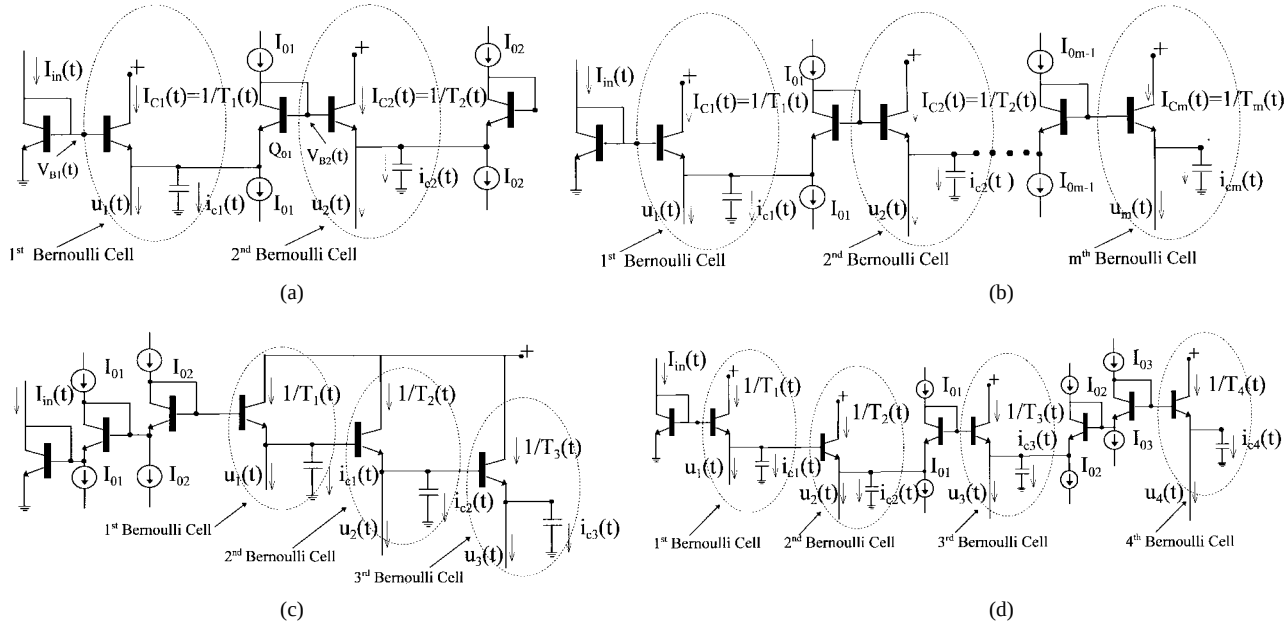

Fig. 3. (a) Two interconnected Bernoulli cells. (b) Cascaded Bernoulli cells. (c), (d) Networks dynamically equivalent to (b).

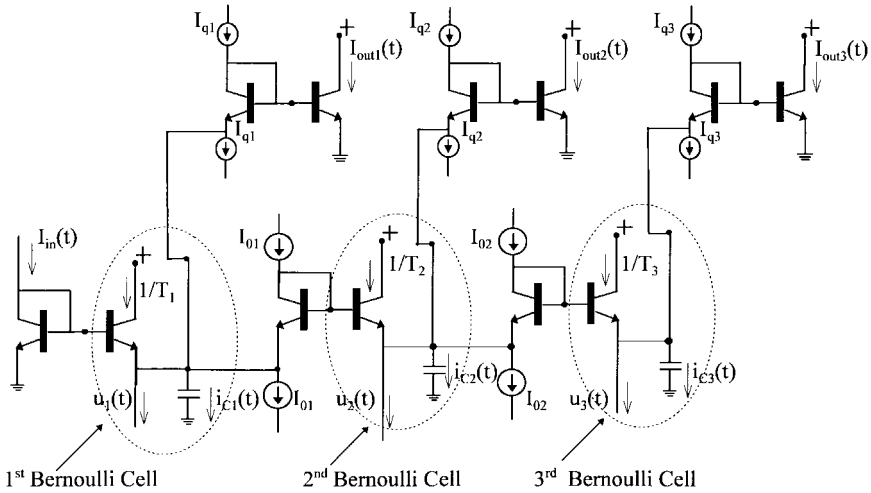

Fig. 4. Sensing of the $w_k(t)(k = 1, \cdots, m)$ variables for a cascade of Bernoulli cells.

From (14c) it can be concluded that

$$\begin{aligned} w_1(t) &= \mu_1 \exp\left[\frac{V_{C1}(t)}{V_T}\right] \\ w_2(t) &= \mu_2 \exp\left[\frac{V_{C2}(t)}{V_T}\right] \\ &\cdots \\ w_m(t) &= \mu_m \exp\left[\frac{V_{Cm}(t)}{V_T}\right] \end{aligned} \tag{14d}$$

with $\mu_1, \mu_2, \cdots, \mu_m$ representing constant in time quantities, and $V_{C1}(t), V_{C2}(t), \cdots, V_{Cm}(t)$ representing the corresponding capacitor node voltages. μ_1 is dimensionless, whereas the dimensions of μ_m will be [A(mpere)]$^{-(m-1)}$.

The validity of the exponential dependence of the $w_k(t)$ variables on the capacitor node voltage: 1) holds for any kind of $u_k(t)$ currents; and 2) is not restricted by the overall input–output behavior, which might be linear or not.

Observe that the topology of Fig. 3(b) has no specified output, and the only functional assumption is that every emitter junction involved is forward biased.

IV. A Generic "Log-Domain State-Space"

The definition of the $w_k(t)$ variables allows the reexpression of (10) and (13) in the form

$$\begin{aligned} C_1 V_T \dot{w}_1(t) + u_1(t) w_1(t) &= I_{\text{in}}(t) \\ C_2 V_T \dot{w}_2(t) + u_2(t) w_2(t) &= w_1(t) \\ &\cdots \\ C_m V_T \dot{w}_m(t) + u_m(t) w_m(t) &= w_{m-1}(t). \end{aligned} \tag{15}$$

When the currents $u_k(t)\,(k = 1, \cdots, m)$ are considered as known functions of the time t, then (15) represents a system of coupled linear ordinary differential equations which rigorously

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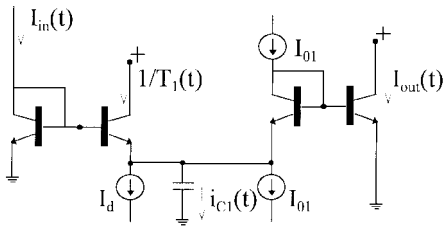

Fig. 5. A log-domain lossy integrator.

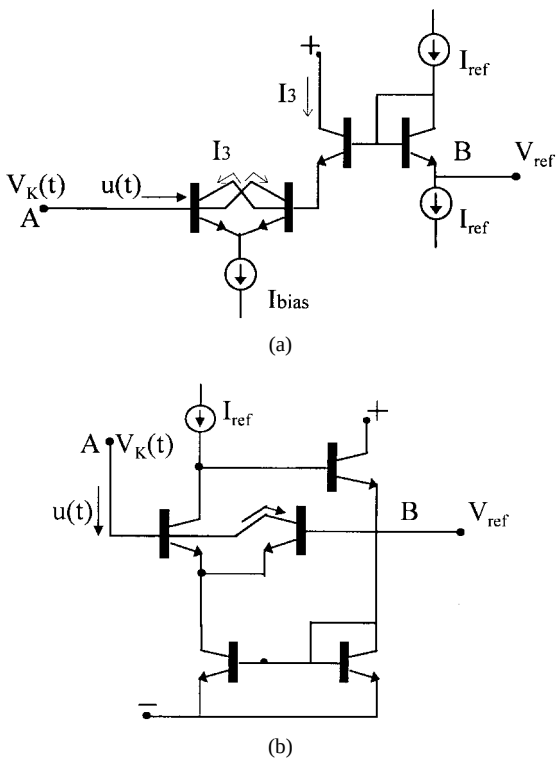

Fig. 6. Subcircuits implementing $u(t) = I_{\rm ref}\ \exp[(V_{\rm ref} - V_K(t))/V_T]$.

describe the dynamic behavior of m interconnected Bernoulli Cells. These equations can be considered as a "log-domain state-space," capable of describing and generating a multitude of linear (or nonlinear) responses. In practice, any interconnection of Bernoulli Cells which ensures that the base voltage variations $((dV_{B_k}(t))/dt)(k = 2, \cdots, m)$ of the kth cell follow the capacitor voltage variations $((dV_{C_{k-1}}(t))/dt)(k = 2, \cdots, m)$ of the previous $(k-1)$th cell will yield the same system of differential equations. Fig. 3(c) and (d) illustrates npn-only interconnections which satisfy this requirement. Observe that the designer is free to choose among various dynamically equivalent interconnections, where the forward-biased emitter junctions might either alternate [Fig. 3(d)] or be stacked [Fig. 3(c)]. In the following synthesis and analysis examples, the discussion concentrates on the interconnection shown in Fig. 3(a), (b)—which typically forms the "backbone" of log-domain filters—since this kind of topology allows integration at low power-supply levels.

The variables $w_k(t)$ can be sensed by means of additional diode-connected BJT's, as shown in Fig. 4. The output currents $I_{{\rm out}k}(t)$ can be derived by applying the TL principle

$$\begin{aligned} I_{\rm out1}(t) &= I_{q1}T_1(t)I{\rm in}(t) = I_{q1}w_1(t) \\ I_{\rm out2}(t) &= I_{q2}I_{01}w_2(t) \\ I_{{\rm out}k}(t) &= I_{qk}\left[\prod_{j=1}^{k-1} I_{0j}\right]w_k(t) \end{aligned} \tag{16}$$

with $k > 1 (k = 2, \cdots, m)$. The dimensional consistency of the log-domain state-space equations can be readily verified.

In addition to linear filtering, a structure of this kind could produce a large-scale nonlinear signal processing system. Equations (15) hold for an open topology, with the coefficients $u_k(t)$ being real-valued currents determinable by the designer, and with state-variables $w_k(t)$ being nonlinearly related to real currents. The log-domain state-space seems capable of creating and/or describing large nonlinear signal processing systems; this kind of information vanishes when an ELIN approach is adopted because the input–output relationship is bound to conform to the linearity imposed by the linear SS or SFG representation of the transfer function. Although small-scale nonlinear dynamics have been reported (e.g., translinear RMS-DC converter of Mulder *et al.* in [33], TL phase detector of Payne *et al.* [34]), it is not currently clear in which way useful large-scale nonlinear signal processing systems could be appropriately structured, although this issue has also been addressed via a systematic generalization of (15) [35]. In the following discussions, we therefore constrain ourselves to the synthesis of linear transfer functions. It should be noted, however, that the Bernoulli Cell seems to be capable of conveniently representing/realizing highly complicated dynamics like the Hodgkin–Huzley nerve axon behavior, extending accordingly the potential of logarithmic circuits [43], [49].

V. Application of the "Log-Domain State-Space" to Log-Domain Filtering

The above analysis has shown that the log-domain state-space equations described by (15) hold for any interconnection of Bernoulli Cells which ensures that the capacitor voltage variations of the previous cell are conveyed to the base terminal of the next cell. When this set of differential equations is considered as the starting point of a synthesis procedure, then the designer may easily synthesize a frequency-domain transfer function by following the steps outlined below.

1) Express the desired frequency-domain transfer function by means of a set of first-order differential equations, for example, state-space or signal-flow-graph representation.
2) Write the respective log-domain state-space generic equations; when an mth-order transfer function is required, the respective m first differential equations of system (15) describing the interconnection of m Bernoulli Cells should be considered.
3) Compare the prototype system of step 1 to the generic equations of step 2 and define
   a) the correct form of the necessary $u_k(t)$ currents, and
   b) the output as a linear function of the $w_k(t)$ variables.

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4) Implement the necessary design equations, i.e., the correct $u_k(t)$ currents, by means of any appropriate architecture, although a pure translinear design strategy seems to facilitate the implementation.

Step 3a requires a consideration of both the required ac response and the necessary dc biasing conditions, as will become clear in the following examples.

A. A Lossy Integrator and a Low-Pass Biquad

Table I summarizes the synthesis procedure for both a lossy integrator and a low-pass biquad. Column 1 shows the desired frequency domain transfer function, while column 2 gives a corresponding linear state-space representation (step 1). The third column shows the generic log-domain state-space design equations, describing the dynamic behavior of one and two Bernoulli Cells for the case of the lossy integrator and the low-pass biquad, respectively (step 2). The fourth column shows the design equations necessary to ensure that the log-domain state-space has the same form as the prototype system (step 3); in this way, it is ensured that the final log-domain structure will behave as the required original system.

Lossy Integrator Synthesis: The necessary design equations in column 4 are obtained by comparing the linear (column 2) and log-domain (column 3) state space equations. In both SS equations, the first term (left-hand term) relates to the differential of the state variable [i.e., $\dot{x}_1(t)$, $\dot{w}_1(t)$, respectively], while the third term (to the right of the $=$ sign) relates to the input signal [$U(t)$, $I_{\text{in}}(t)$, respectively]. The linear SS equation has the remaining term proportional to the state-variable $x_1(t)$, and thus the log-domain equation must similarly have the remaining term proportional to $w_1(t)$. This gives the first design equation, $u_1(t)w_1(t) \propto w_1(t)$ (i.e., $u_1 =$ constant). The second linear SS equation states that the output variable $y(t)$ is proportional to $x_1(t)$. Thus, in log-domain SS, the output current $I_{\text{out}}(t)$ must be proportional to $w_1(t)$. This gives the second design equation. Proceeding to step 4 the first design equation requires $u_1 =$ constant which is easily implemented by incorporating (at circuit level) a constant current source, i.e., $u_1 = I_d$. The second design equation is conveniently realized as shown in Fig. 4 and (16). The final circuit is shown in Fig. 5.

Referring to Table I, row 1 and Fig. 5, the log-domain SS equations can be written

$$\begin{aligned} C_1 V_T \dot{w}_1 + I_d w_1(t) &= I_{\text{in}}(t) \\ I_{\text{out}}(t) &= I_{01} w_1(t). \end{aligned}$$

Taking the Laplace transform and considering only the steady-state response

$$\begin{aligned} C_1 V_T s W_1(s) + I_d W_1(s) &= I_{\text{in}}(s) \\ I_{\text{out}}(s) = I_{01} W_1(s) &= \frac{I_{01}}{I_d + C_1 V_T s} I_{\text{in}}(s) \Rightarrow \\ \frac{I_{\text{out}}(s)}{I_{\text{in}}(s)} &= \frac{(I_{01}/C_1 V_T)}{s + (I_d/C_1 V_T)}. \end{aligned} \tag{17}$$

Equation (17) corresponds to the transfer function of a lossy integrator with pole frequency $\omega_0 = I_d/C_1 V_T$ and dc gain $K = I_{01}/I_d$. Both values are easily tuneable via current sources I_d and I_{01}.

Low-Pass Biquad Synthesis: The procedure of extracting the necessary design equations is similar to that described for the lossy integrator. In this case, a comparison of columns 2 and 3 in Table I (row 2) reveals

$$\begin{aligned} u_1(t) w_1(t) &\propto w_2(t) \\ u_2(t) w_2(t) &\propto w_2(t) \\ I_{\text{out}}(t) &\propto w_2(t) \end{aligned}$$

or, equivalently [recall that $w_k(t) = \left[\prod_{j=1}^{k} T_j(t)\right] I_{\text{in}}(t) = T_k(t) w_{k-1}(t)$],

$$u_1(t) = p_1 \frac{w_2(t)}{w_1(t)} \Rightarrow u_1(t) \frac{1}{T_2(t)} = p_1 \tag{18a}$$

$$u_2(t) = p_2 \frac{w_2(t)}{w_2(t)} \Rightarrow u_2(t) = p_2 \tag{18b}$$

$$I_{\text{out}}(t) = p_3 w_2(t) \Rightarrow \frac{1}{T_1(t)} \frac{1}{T_2(t)} I_{\text{out}}(t) \propto I_{\text{in}}(t) \tag{18c}$$

where p_1, p_2, p_2 are constant quantities.

Equation (18a)—being a product of currents—could be interpreted as corresponding to a translinear loop and can be implemented using either of the blocks shown in Fig. 6 reported previously by Frey [11], [12]. When points A and B in Fig. 6 are connected to the emitters of Bernoulli Cell BJT's Q_1 and Q_2 (see Fig. 7), (18a) is fulfilled by the formation of the translinear loop $Q_{01} T_3 T_x Q_3 Q_{03} Q_2$. Equation (18b) is met by simply adding a constant current source I_d at the emitter of the second Bernoulli Cell. Finally (18c) is met by connecting a level shifter Q_{02} and an output BJT to the second cell as described in Fig. 4 and (16).

The exact ac response of the circuit shown in Fig. 7 is derived by applying the Laplace transform to the system of log-domain state-space equations; referring to Table I (row 2) and considering Fig. 7, the design equations (18a)–(18c) can be rewritten

$$\begin{aligned} u_1(t) \frac{1}{T_2(t)} &= I_{01} I_{03} = p_1 \\ u_2(t) &= I_d = p_2 \\ \frac{1}{T_1(t)} \frac{1}{T_2(t)} I_{\text{out}}(t) &= I_{01} I_{02} I_{\text{in}}(t) = p_3 I_{\text{in}}(t) \end{aligned}$$

or, equivalently,

$$\begin{aligned} u_1(t) w_1(t) &= I_{01} I_{03} w_2(t) \\ u_2(t) w_2(t) &= I_d w_2(t) \\ I_{\text{out}}(t) &= I_{01} I_{02} w_2(t). \end{aligned} \tag{18d}$$

Substituting the design equations (18d) into the generic log domain state-space equations (see Table I)

$$\begin{aligned} C_1 V_T \dot{w}_1(t) + I_{01} I_{03} w_2(t) &= I_{\text{in}}(t) \\ C_2 V_T \dot{w}_2(t) + I_d w_2(t) &= w_1(t) \\ I_{\text{out}}(t) &= I_{01} I_{02} w_2(t). \end{aligned}$$

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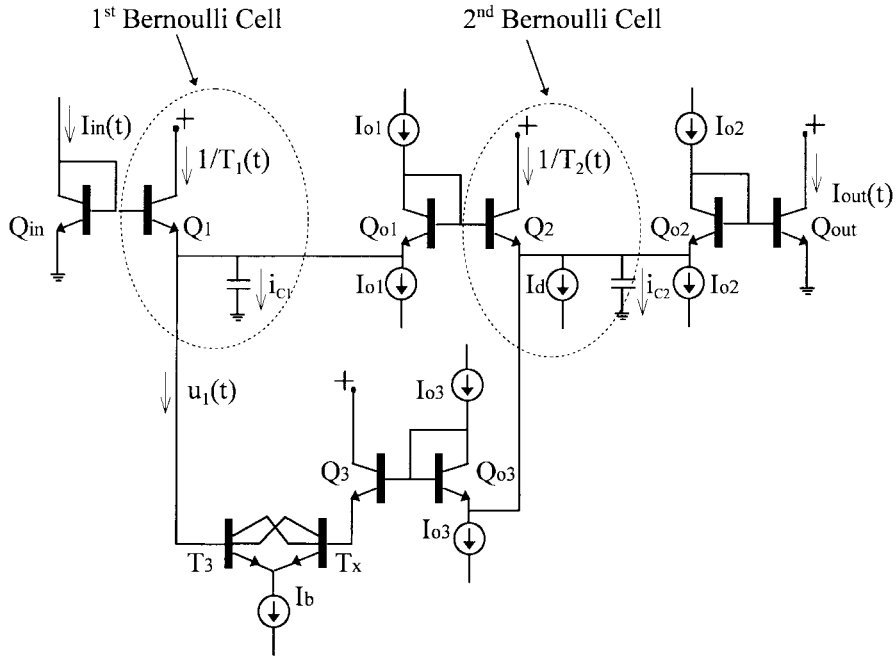

Fig. 7. A log-domain low-pass biquad.

TABLE I
LOG-DOMAIN STATE-SPACE-BASED SYNTHESIS PROCEDURE OF A LOSSY INTEGRATOR AND A LOWPASS BIQUAD

Transfer function	State-space representation	Generic "log-domain state-space" design equations	Necessary design equations
$\frac{k}{s+\omega_o}$ Lossy integrator	$\dot{x}_1(t)+\omega_0 x_1(t)=U(t)$ $y(t)=k\,x_1(t)$	$C_1V_T\,\dot{w}_1(t)+u_1(t)w_1(t)=I_{in}(t)$	$u_1(t)w_1(t)\propto w_1(t)$ $I_{out}(t)\propto w_1(t)$
$\frac{k\omega_0^2}{s^2+(\frac{\omega_0}{Q})s+\omega_0^2}$ Lowpass biquad	$\dot{x}_1(t)+\omega_0 x_2(t)=\omega_0 U(t)$ $\dot{x}_2(t)+(\frac{\omega_0}{Q})x_2(t)=\omega_0 x_1(t)$ $y(t)=k\,x_2(t)$	$C_1V_T\,\dot{w}_1(t)+u_1(t)w_1(t)=I_{in}(t)$ $C_2V_T\,\dot{w}_2(t)+u_2(t)w_2(t)=w_1(t)$	$u_1(t)w_1(t)\propto w_2(t)$ $u_2(t)w_2(t)\propto w_2(t)$ $I_{out}(t)\propto w_2(t)$

Applying the Laplace transform and considering only the steady-state solution

$$\begin{aligned} C_1V_T sW_1(s)+I_{01}I_{03}W_2(s)&=I_{\text{in}}(s)\\ (C_2V_T s+I_d)W_2(s)&=W_1(s)\ \Rightarrow\\ I_{\text{out}}(s)&=I_{01}I_{02}W_2(s)\end{aligned}$$

$$\frac{I_{\text{out}}(s)}{I_{\text{in}}(s)}=\frac{(I_{01}I_{02}/C_1C_2V_T^2)}{s^2+(I_d/C_2V_T)s+(I_{01}I_{03}/C_1C_2V_T^2)}. \quad (19)$$

Equation (19) describes a low-pass biquad with a pole frequency $\omega_0=\sqrt{I_{01}I_{03}}\Big/(\sqrt{C_1C_2}V_T)$, a quality factor $Q=\sqrt{C_2/C_1}(\sqrt{I_{01}I_{03}}/I_d)$, and a gain factor $K_g=I_{02}/I_{03}$. All these parameters are tuneable via dc currents I_{01}, I_{02}, I_{03}.

B. A Log-Domain Integrator and a Log-Domain Bandpass Biquad

In the following synthesis examples, the problem of proper dc biasing of log-domain circuits is addressed. Recalling (15), it should be stressed that *the $u_k(t)$ currents should always be greater than zero, i.e.,* $u_k(t)>0$. The opposite would lead to impossible dc conditions for the BJT of the kth Bernoulli Cell, since it would have no dc bias current. A realistic solution to the problem of suitable dc biasing, when the ac behavior dictates that a specific $u_k(t)$ current should be equal to zero, can be stated as follows: instead of nullifying the $u_k(t)$ current, *ensure that the product $u_k(t)w_k(t)$ remains constant in time*. It will be shown in the following examples that these additional "constant terms" in the log-domain state-space realization of the desired transfer function should be appropriately related to the level of dc biasing in such a way that the desired ac behavior remains undisturbed by their presence.

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TABLE II
LOG-DOMAIN STATE-SPACE-BASED SYNTHESIS PROCEDURE OF A LOSSLESS INTEGRATOR AND A BANDPASS BIQUAD

Transfer function	State-space representation	Generic "log-domain state-space" design equations	Necessary design equations
$\frac{k}{s}$ integrator	$\dot{x}_1(t) = U(t)$ $y(t) = k\, x_1(t)$	$C_1 V_T\, \dot{w}_1 + u_1(t) w_1(t) = I_{in}(t)$	$u_1(t) w_1(t) = n_1$ $I_{out}(t) \propto w_1(t)$
$\frac{k(\frac{\omega_0}{Q})s}{s^2 + (\frac{\omega_0}{Q})s + \omega_0^2}$ Bandpass biquad	$\dot{x}_1(t) + (\frac{\omega_0}{Q})x_1(t) + \omega_0 x_2(t) = \omega_0 U(t)$ $\dot{x}_2(t) = \omega_0 x_1(t)$ $y(t) = (\frac{k}{Q})x_1(t)$	$C_1 V_T\, \dot{w}_1 + u_1(t) w_1(t) = I_{in}(t)$ $C_2 V_T\, \dot{w}_2 + u_2(t) w_2(t) = w_1(t)$	$u_1(t) w_1(t) \propto (w_1(t) + w_2(t))$ $u_2(t) w_2(t) = n_2$ $I_{out}(t) \propto w_1(t)$

Before proceeding to the design of a lossless integrator and a bandpass biquad, the implementation of these constant product terms will be considered. We require

$$\begin{aligned} u_k(t) w_k(t) &= n_k \;\Rightarrow \\ u_k(t) &= \frac{n_k}{w_k(t)} \;\Rightarrow \\ u_k(t) &= \frac{n_k}{\mu_k} \exp[-V_K(t)/V_T] \\ &= p_k \exp[-V_K(t)/V_T] \end{aligned} \tag{20}$$

where n_k, μ_k, p_k are constant terms.

The subcircuits illustrated in Fig. 6(a), (b) [11], [12] [and any other subcircuit capable of generating $u_k(t)$ currents of this form] are suitable for the implementation of these $u_k(t)$ currents since

$$u_k(t) = I_{\text{ref}} \exp\{[V_{\text{ref}} - V_K(t)]/V_T\}$$

with $I_{\text{ref}} \exp(V_{\text{ref}}/V_T) = p_k$ = constant in time. The designer is left with the freedom to choose any appropriate circuit necessary for the generation of the voltage reference V_{ref}.

We turn now to Table II, which reveals the necessary conditions for the generic "log-domain state-space" equations to produce a theoretically ideal integrator and a bandpass biquad.

Integrator (see Table II Row 1): A first examination of the state equations in columns 2 and 3 suggests that the designer must set $u_1(t) = 0$ to ensure equivalence between the two representations. However, if $u_1(t) = 0$, the Bernoulli Cell BJT will be off (no dc bias current). If, however, we chose $u_1(t)$ = constant = I_d, the integrator would become lossy (Table I, row 1).

Effectively, the required ac conditions $(u_i(t) = 0)$ are incompatible with the necessary dc biasing. A solution to this problem is to set the product $u_1(t) w_1(t) = n_1$, where n_1 is constant

$$\begin{aligned} C_1 V_T \dot{w}_1 + u_1(t) w_1(t) &= I_{\text{in}}(t) \\ u_1(t) w_1(t) &= n_1. \end{aligned} \tag{21}$$

For class-A operation, the input signal is superimposed on a dc component, i.e., $I_{\text{in}}(t) = D + I_{\text{in, ac}}(t)$ with D the dc-bias current. Taking the Laplace transform of (21) and substituting $L[I_{\text{in}}(t)] = I_{\text{in, ac}}(s) + (D/s)$ yields

$$W_1(s) = \frac{w_1(t=0)}{s} + \frac{I_{\text{in, ac}}(s)}{C_1 V_T s} + \frac{(D - n_1)}{C_1 V_T s^2}. \tag{22}$$

$w_1(t=0)$ represents the initial value of the $w_1(t)$ variable at $t = 0$, i.e., when the ac input is applied. The second design equation in Table II states that $I_{\text{out}}(t) \propto w_1(t)$, which can be implemented as in the lossy integrator case. Referring to Fig. 8 and (22):

$$\begin{aligned} I_{\text{in}}(t) I_{01} &= (1/T_1(t)) I_{\text{out}}(t) \Rightarrow I_{\text{out}}(t) = I_{01} w_1(t) \;\Rightarrow \\ I_{\text{out}}(s) &= \frac{I_{01} w_1(t=0)}{s} + \left(\frac{I_{01}}{C_1 V_T}\right) \frac{I_{\text{in, ac}}(s)}{s} \\ &\quad + \left(\frac{I_{01}}{C_1 V_T}\right) \frac{D - n_1}{s^2}. \end{aligned} \tag{23}$$

The first term in (23) represents the dc component of the output current, the second term represents the desired integration of the ac component, whereas the third term must be actively cancelled. This cancellation is achieved when

$$D = n_1 = u_1(t) w_1(t). \tag{24}$$

Fig. 8 shows the complete integrator topology where the subcircuit of Fig. 6(b) is used to implement the constant product $u_1(t) w_1(t)$; for the loop comprised of $Q_{\text{in}} Q_1 Q_{\text{ref}} Q_{u1} V_{\text{ref}}$ it holds

$$\begin{aligned} V_{be,\,\text{in}} + V_{be,\,u_1} &= V_{be,\,(1/T_1)} + V_{be,\,I_{\text{ref}}} + V_{\text{ref}} \;\Rightarrow \\ u_1(t)[T_1(t) I_{\text{in}}(t)] &= u_1(t) w_1(t) = I_{\text{ref}} \exp\left(\frac{V_{\text{ref}}}{V_T}\right) = n_1. \end{aligned} \tag{25}$$

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Comparing (24) and (25), cancellation of the unwanted term is achieved when

$$I_{\rm ref}\,\exp\left(\frac{V_{\rm ref}}{V_T}\right)=D\;\Rightarrow$$
$$V_{\rm ref}=V_T\,\ln\left(\frac{D}{I_{\rm ref}}\right). \tag{26}$$

Equation (26) states the necessary condition for the topology of Fig. 8 to be theoretically an ideal lossless integrator with an output

$$I_{\rm out}(t)=I_{01}w_1(t=0)+\left(\frac{I_{01}}{C_1V_T}\right)\int_0^t I_{\rm in,\,ac}(\tau)\,d\tau. \tag{27}$$

Bandpass Biquad: A similar dc-biasing problem is encountered since—from Table II, row 2—$u_2(t)$ should be equal to zero. To avoid this situation, we again set $u_2(t)w_2(t)=$ constant, giving the necessary design equations:

$$u_1(t)w_1(t)\propto[w_1(t)+w_2(t)]$$
$$[\text{for example, } u_1(t)w_1(t)=p_1w_1(t)+p_2w_2(t)\ \text{with } p_1,p_2 \text{ constant}]$$
$$u_2(t)w_2(t)=n_2$$
$$I_{\rm out}(t)\propto w_1(t)$$

or, equivalently,

$$[u_1(t)-p_1]=p_2\frac{w_2(t)}{w_1(t)}$$
$$=p_2T_2(t)\Rightarrow[u_1(t)-p_1]\left(\frac{1}{T_2(t)}\right)=p_2 \tag{28a}$$
$$u_2(t)=\frac{n_2}{\mu_2}\,\exp[-V_2(t)/V_T] \tag{28b}$$
$$\frac{1}{T_1(t)}I_{\rm out}(t)\propto I_{\rm in}(t). \tag{28c}$$

Equation (28a) is conveniently implemented by means of either of the blocks of Fig. 6, similar to the case of the low-pass biquad. A constant current source I_d is added at the emitter of the first Bernoulli Cell to realize the constant quantity p_1 (see Fig. 9). It is straightforward to show that the TL loop formed by $Q_{01}Q_{03}Q_{u1}Q_2$ fulfills (28a) with $p_l=I_{01}I_{03}$. Equation (28c) corresponds to the TL loop formed by $Q_{\rm in}Q_1Q_{q1}Q_{\rm out}$ [compare with (16) and Fig. 4]. Equation (28b) corresponds to the necessary dc-biasing condition and is again realized by means of the subcircuits of Fig. 6. From Fig. 9 it can be seen that

$$V_{be,\,I_{\rm in}}+V_{be,\,I_{01}}+V_{be,\,u_2}$$
$$=V_{be,\,(1/T_1)}+V_{be,\,(1/T_2)}+V_{be,\,I_{\rm ref}}+V_{\rm ref}\;\Rightarrow$$
$$V_T\,\ln\left[\frac{I_{\rm in}(t)I_{01}u_2(t)}{\dfrac{1}{T_1(t)}\,\dfrac{1}{T_2(t)}\,I_{\rm ref}}\right]$$
$$=V_{\rm ref}\Rightarrow u_2(t)(T_2(t)T_1(t)I_{\rm in}(t))$$
$$=u_2(t)w_2(t)=\frac{I_{\rm ref}}{I_{01}}\,\exp\left(\frac{V_{\rm ref}}{V_T}\right). \tag{29}$$

The exact ac response is derived by applying the Laplace transform to the system of log-domain state-space equations. When (28a,b,c) are met by means of the additional circuitry described above, we can state

$$[u_1(t)-I_d]\,\frac{1}{T_2(t)}=I_{01}I_{03}$$
$$u_2(t)w_2(t)=\frac{I_{\rm ref}}{I_{01}}\,\exp\left(\frac{V_{\rm ref}}{V_T}\right)=n_2$$
$$\frac{1}{T_1(t)}\,I_{\rm out}(t)=I_{q1}I_{\rm in}(t)$$

or, equivalently,

$$u_1(t)w_1(t)=I_dw_1(t)+I_{01}I_{03}w_2(t)$$
$$\frac{V_{\rm ref}}{V_T}\,\exp\left(\frac{V_{\rm ref}}{VT}\right)=n_2$$
$$I_{\rm out}(t)=I_{q1}w_1(t). \tag{30}$$

Combining (30) with the generic log-domain state-space expressions (see Table II):

$$C_1V_T\dot{w}_1(t)+I_dw_1(t)+I_{01}I_{03}w_2(t)=I_{\rm in}(t)$$
$$C_2V_T\dot{w}_2(t)+n_2=w_1(t)$$
$$I_{\rm out}(t)=I_{q1}w_1(t). \tag{31}$$

Applying the Laplace transform to (31) and taking into consideration the initial conditions for $t=0$,

$$I_{\rm out}(s)=\frac{\left(\dfrac{I_{q1}}{C_1V_T}\right)s}{s^2+\left(\dfrac{\omega_0}{Q}\right)s+\omega_0^2}I_{\rm in}(s)$$
$$+\frac{I_{q1}w_1(t=0)s}{s^2+\left(\dfrac{\omega_0}{Q}\right)s+\omega_0^2}$$
$$-\frac{I_{q1}I_{01}I_{03}}{(C_1V_T)}\,\frac{w_2(t=0)}{s^2+\left(\dfrac{\omega_0}{Q}\right)s+\omega_0^2}$$
$$+\frac{I_{q1}I_{01}I_{03}}{(C_1C_2V_T^2)}\,\frac{n_2}{s\left[s^2+\left(\dfrac{\omega_0}{Q}\right)s+\omega_0^2\right]} \tag{32}$$

where $w_1(t=0)$ and $w_2(t=0)$ represent the initial value of the $w_1(t)$ and $w_2(t)$ variables, respectively, at $t=0$ (when the ac input is applied) and

$$s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2=s^2+\left(\frac{I_d}{C_1V_T}\right)s+\left(\frac{I_{01}I_{03}}{C_1C_2V_T^2}\right). \tag{33}$$

The first term of (32) represents the bandpass filtered version of the input which is characterized by a center frequency $\omega_0=\sqrt{I_{01}I_{03}}\Big/(\sqrt{C_1C_2}V_T)$, a quality factor $Q=\sqrt{C_1/C_2})(\sqrt{I_{01}I_{03}}/I_d)$ and a gain factor $K_g=(I_{q1}/I_d)$.

The second and third terms contribute only transient terms which are not of importance for the steady-state response (see the Appendix). The last term contributes both transient terms and a dc component which is present at the output and which equals (see the Appendix)

$$I_{q1}\,\frac{I_{01}I_{03}}{C_1C_2V_T^2}\,\frac{1}{\omega_0^2}\,n_2=\frac{I_{q1}}{I_{01}}\,I_{\rm ref}\,\exp\left(\frac{V_{\rm ref}}{V_T}\right).$$

Therefore, the selection of the additional constant term n_2 affects the dc level present at the output.

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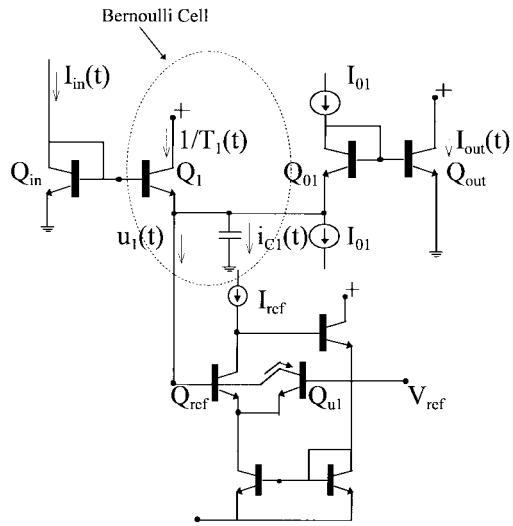

Fig. 8. A log-domain lossless integrator.

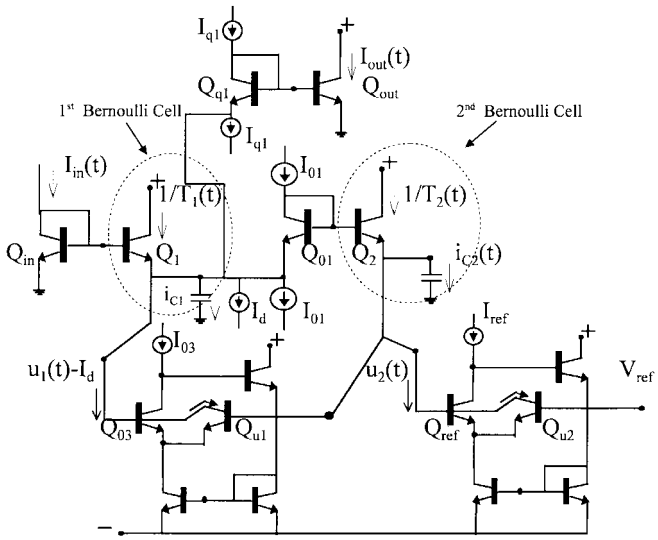

Fig. 9. A log-domain bandpass biquad.

VI. Practical Deviations and Considerations

In the foregoing sections of this paper, the BJT's have been considered as ideal exponential voltage-controlled current sources. This is a convenient simplification which eases the systematic formation of the log-domain state-space differential equations. However, the integrated implementation of BJT's leads to unavoidable physical deviations from a pure exponential V–I characteristic, the most important of these being parasitic ohmic resistances of the base and the emitter regions, finite beta (β), and the associated parasitic capacitance C_π. A more detailed analysis should also include the finite output impedance and the collector-substrate parasitic capacitance. Each of those factors will distort the ideal BJT exponential behavior. Since log-domain circuits are large-signal networks, certain limitations exist on how these parasitic effects can be reliably modeled to enable an analysis of distortion in log-domain circuits. The parasitic capacitances for instance are typically associated with the hybrid π-(small-signal) equivalent of the BJT [36], [37]; thus, if a realistic

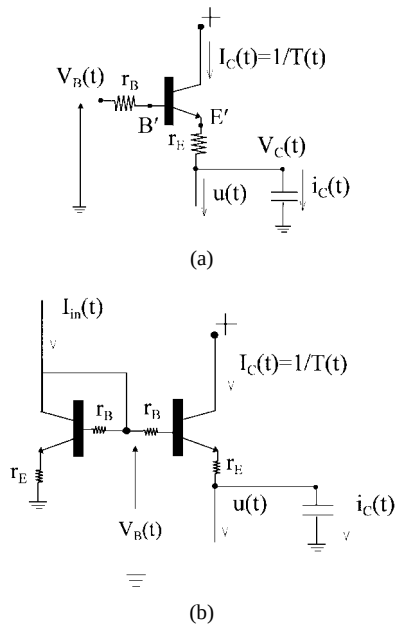

Fig. 10. (a) A nonideal Bernoulli cell. (b) A nonideal Bernoulli cell driven by an identical nonideal input transistor.

distortion mechanism analysis for log-domain structures is to be developed, large-signal ac models should be used [38]. Unfortunately the complexity of such models renders them fairly impractical for hand-calculations, even for the simplest log-domain structures.

These limitations have also been realized by other researchers in the field who have mainly concentrated on the only large-signal parasitic parameter of BJT's , i.e., β (beta) [21], [39]. The Bernoulli Cell-based formalism, being a low-level approach, seems to be well suited for both the identification of β-related distortion mechanisms and the evaluation of its effects. Although the present paper focuses mainly on synthesis issues of log-domain filters, in the following brief discussion we highlight certain aspects related to distortion.

When in the generic Bernoulli Cell BJT of Fig. 1, the finite β and the ohmic resistances of the base and the emitter (r_B and r_E, respectively] are taken into consideration, the actual base-emitter terminal voltage difference V_{BE} will have a value different than its ideal because of the voltage drops across r_B and r_E; this situation is illustrated in Fig 10(a).

Assuming that: 1) the collector current $I_C(t)$ has an ideal exponential dependence on $V_{B'E'}$; and 2) $I_C = \beta I_B$ and $I_E = (\beta+1)I_B$ (I_B and I_E are the base and the emitter current, respectively), then the dynamic behavior of the modified Bernoulli Cell of Fig. 10(a) can be derived as

$$\dot{I}_C(t) - \left[\frac{\dot{V}_B(t)}{V_T} + \frac{u(t)}{CV_T}\right] I_C(t) + \frac{[I_C(t)]^2}{\alpha C V_T} = -\left\{\frac{r_B(1-\alpha)+r_E}{2\alpha V_T}\right\} \frac{d}{dt}\left[I_C(t)^2\right] \tag{34}$$

with $\alpha = \beta/(\beta+1)$.

A direct comparison of (3) to (34) reveals that the inclusion of the parasitic voltage drops leads to the presence of an additional term [shown on the right-hand side of (34)], which

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distorts the ideal behavior of the cell. This transistor-level analysis yields a first qualitative insight into the distortion mechanism, and a clearer picture is created when a similar treatment is adopted for each transistor. Consider, for example, the nonideal Bernoulli cell being driven by an identical nonideal input transistor as shown in Fig. 10(b). The pair of BJT's are now approximately governed by the following distorted differential equation [compare with (8)]:

$$\begin{aligned} CV_T \frac{d}{dt}\left\{\ln\left(T(t)\left[I_{\rm in} - \frac{I_{\rm in}(t)+I_C(t)}{\beta}\right]\right)\right\} \\ + u(t) + C\frac{d}{dt}\left\{\frac{r_B(1-\alpha)+r_E}{\alpha} \right. \\ \left. \cdot \left(I_{\rm in}(t) - \frac{I_{\rm in}(t)+I_C(t)}{\beta}\right)\right\} \\ = \frac{1}{\alpha T(t)} + C\frac{d}{dt}\left\{\frac{r_B(1-\alpha)+r_E}{\alpha} I_C(t)\right\}. \end{aligned} \tag{35}$$

Taking into consideration that $T(t) = 1/I_C(t)$, the distorted capacitor current reduces to

$$\begin{aligned} \hat{i}_c(t) &= CV_T \frac{d}{dt}\left\{\ln\left(\left(1-\frac{1}{\beta}\right)[T(t)I_{\rm in}(t)] - \frac{1}{\beta}\right)\right\} \\ &\cong CV_T \frac{d}{dt}\left\{\ln\left[T(t)I_{\rm in}(t) - \frac{1}{\beta}\right]\right\}. \end{aligned} \tag{36}$$

For reasonably high values of β and for similar values of dc currents biasing the two transistors, the capacitor current does not deviate significantly from its expected value [see (8)]. In (35), two distorting terms remain present, which are clearly related to the parasitic voltage drops in each transistor. Luckily these terms affect the ideal behavior in a "symmetric" way (the terms are on opposite sides of the $=$ sign), and their values are proportional to a generally small parasitic time constant $\tau_{par} \approx (rC)$ with $r = (r_B(1-\alpha)+r_E)/\alpha$. When the frequency of the input signal is much lower than $\omega_{\rm par} = (rC)^{-1}$, it might thus be argued that the transformed KCL expression given by (35) is not severely affected by these parasitic terms. If, on the other hand, these parasitic terms may not be neglected, then the distorted value $\hat{w}(t)$ can still be *approximately* calculated since (35) yields [when (14b) and the comments accompanying (36) are taken into consideration]:

$$\begin{aligned} CV_T\dot{\hat{w}}(t) + \left\{u(t) + \left(rC\frac{d}{dt}\left[\left(1-\frac{1}{\beta}\right)I_{\rm in}\right.\right.\right. \\ \left.\left.\left. - \left(1+\frac{1}{\beta}\right)I_C\right]\right)\right\}\hat{w}(t) \cong \frac{I_{\rm in}(t)}{\alpha}. \end{aligned} \tag{37}$$

Equation (37) is linear in $\hat{w}(t)$ and can be solved analytically when the expected values of $u(t), I_C(t)$ are substituted.

Taking into consideration these parasitic components for all BJT's forming the Bernoulli "backbone" would lead to a modified set of log-domain state-space equations. Such an attempt is cumbersome and beyond the scope of the present article. Nevertheless, it is useful to discuss certain qualitative aspects.

Considering the effect of the parasitic voltage drops for a number of base-emitter junctions that form a TL loop—a common situation in log-domain structures—leads to the concept of "excess voltage" around the TL loop [40]. This concept is used both for analysis and optimization of (static) TL structures as described in [40] and [41]. The time-varying dependence of the excess voltage leads to residual distortion [42]. A rough estimation of the excess voltage is feasible if the ideal (i.e., expected) values of collector currents for each junction involved are known. A low-level analysis method suitable for determining the (nonlinear) currents internal to log-domain structures in closed analytical form is thus necessary, and the log-domain state-space can be used as an analysis tool [27] to derive these ideal current values [43]. As an example of the use of the excess voltage, consider how the condition $u_1(t)w_1(t) = n_1$ is affected by the presence of the parasitic voltage drops in each transistor comprising the loop $Q_{\rm in}Q_1Q_{\rm ref}Q_{u1}V_{\rm ref}$ of Fig. 8. An analysis with the parasitic voltage drops taken into consideration yields the following modified condition:

$$\begin{aligned} u_1(t)w_1(t) &\cong I_{\rm ref}\exp\left(\frac{V_{\rm ref}}{V_T}\right)\exp\left(\frac{\Delta\Phi_1(t)}{V_T}\right) \\ &= n_1 \exp\left(\frac{\Delta\Phi_1(t)}{V_T}\right) \end{aligned} \tag{38}$$

where $\Delta\Phi_1(t)$ is the excess voltage along the TL loop; $\Delta\Phi_1(t) = \varphi_{1/T_1} + \varphi_{I_{\rm ref}} - (\varphi_{I_{\rm in}} + \varphi_{u1})$, where φ_j represents the parasitic voltage drop at Q_j. Substituting the "distorted" (38) into (37) yields [when $\Delta\Phi_1(t)/V_T$ is reasonably small in comparison with unity, C is reasonably high, and the input frequency ω is much smaller than $\omega_{\rm par}$]

$$CV_T\dot{\hat{w}}_1(t) + n_1 + n_1\frac{\Delta\Phi_1(t)}{V_T} \cong D + I_{\rm in,ac}(t). \tag{39a}$$

Considering the quantity $\Delta\Phi_1(t)/V_T$ as a Fourier series—which can be done when the expected values of the internal log-domain currents are known—it should be clear that its presence leads to distortion. The output current is given by

$$\begin{aligned} \hat{I}_{\rm out}(t) &\cong I_{01}\hat{w}_1(t)\exp\left(\frac{\Delta\Phi_2(t)}{V_T}\right) \\ &\cong I_{01}\hat{w}_1(t)\left[1+\frac{\Delta\Phi_2(t)}{V_T}\right] \end{aligned} \tag{39b}$$

with $\hat{w}_1(t)$ the distorted value of $w_1(t)$ given by (39a) for $n_1 = D$ and $\Delta\Phi_2(t)$ representing the excess voltage around the TL loop $Q_{\rm in}Q_1Q_{01}Q_{\rm out}$. Clearly phase errors have now been introduced to the output current due both to $\hat{w}_1(t)$ and $\Delta\Phi_2(t)$. Similar comments hold for higher order topologies. For the case of the bandpass biquad, for example, each of the three TL loops described previously can be associated with an excess voltage quantity $\Delta\Phi(t)$, affecting the respective differential equations. A reliable large-signal calculation of $\Delta\Phi(t)$ around a TL loop should also take into account the operand nature of β for each transistor [2], as well as the fact that the internal collector currents are spectrally rich [43]. A very low-level approach seems unavoidable [44].

A further convenience of employing the excess voltage concept is that other sources of distortion such as emitter area mismatch and the Early effect can also be included.

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From the above largely qualitative discussion it becomes clear that the exact prediction of distortion in log-domain structures is fairly complicated. Therefore, small-signal approximations—like those of (39a) and (39b)—seem to be useful and insightful.

Consider, for example, the lossy integrator transfer function derived by large-signal equations (17); its pole frequency is given by the relation

$$\omega_0 = \frac{I_d}{CV_T}. \tag{40a}$$

Realizing that I_d/V_T equals the small-signal g_m of the respective BJT, a "small-signal" pole frequency can be defined

$$\omega_0 = \frac{g_m}{C}. \tag{40b}$$

From (40b), it is easy to understand the "shift to the left" of the frequency response which is often observed in log-domain filters; g_m is degraded due to the presence of the finite emitter resistance [45]

$$g_m = \frac{g_{mi}}{1 + g_{mi} r_E} \tag{40c}$$

with g_{mi} the ideal transconductance value. Substituting (40c) into (40b) yields

$$\begin{aligned}\omega_{0,\,\mathrm{real}} &= \frac{\left(\dfrac{g_{mi}}{C}\right)}{1 + g_{mi} r_E} \\ &\cong \omega_{0,\,\mathrm{ideal}}(1 - g_{mi} r_E) \\ &= \omega_{0,\,\mathrm{ideal}}(1 - r_E C \omega_{0,\,\mathrm{ideal}})\end{aligned} \tag{41}$$

assuming that the quantity $g_m r_E$ is reasonably small in comparison with unity. Equation (41) is identical to that calculated by means of small-signal approximations on a linear state-space representation of the lossy integrator, and reveals that the biasing currents should be appropriately scaled—as proposed in [21]—to compensate for the r_E-induced "shift to the left" of the frequency response. When g_{mi} is substituted for I_d/CV_T, the value of $\omega_{0,\,\mathrm{real}}$ in (41) describes the same deviation due to r_E as expressed in [21]. Similar comments hold for the case of the low-pass and the bandpass biquads.

Equations (17), (19), and (32) demonstrate that the filter parameters are proportional to biasing collector current values, which should be PTAT [46], [47] to prevent a drift of the filter parameters (ω_0, Q) with temperature variations (a situation which is not uncommon in bipolar designs). However, this leads to a higher current consumption at higher temperatures. In terms of power dissipation and chip area, the circuits described in the previous sections are typical representatives of class-A log-domain structures [4], [5], [12]. More economic realizations in terms of power dissipation can be achieved by using fully differential structures [24] but at the expense of increased circuit complexity. Finally the small values of V_{ref} (a few mV's) necessary for the appropriate tuning of the filters can be conveniently generated; voltage references of this order of magnitude can be produced when the circuit output voltage is proportional to the ΔV_{BE} of a pair of transistors. Alternatively V_{ref} can be set to some convenient value (e.g., 0 V), and I_{ref} can then be set appropriately [see (26)].

VII. Simulation Results

The design approach developed in Section IV was tested and confirmed by means of HSPICE simulations with process parameters from a commercial 11 GHz bipolar process. Due to a lack of space, the simulation results for the case of the lossy integrator and the low-pass biquad are not presented; the reader may consult [4], [5], [14], [15], and [22], where various low-pass frequency responses are presented. In the following we constrain ourselves to the cases of the integrator and the bandpass biquad, with the input having the form $I_{\mathrm{in}}(t) = D[1 + m\,\sin(\omega t)]$ (class-A operation). The results are *indicative* and aim at examining certain qualitative features of the approach.

For the Case of the Integrator: It was shown in Section V-B that when $V_{\mathrm{ref}} = V_T \ln(D/I_{\mathrm{ref}})$, the output current is composed of a dc component $I_{01} w_1(t = 0)$ and an ac component which ideally is a pure integration of the alternating input current. Simulations were carried out with $V_{\mathrm{ref}} = 0$ (i.e., $D = I_{\mathrm{ref}}$) and voltage power supply voltage ± 1.5 V. Referring to (27), the integration time constant $\tau = C_1 V_T / I_{01}$ depends both on the capacitance and the value of I_{01} which flows through the diode-connected level shifter. Fig. 11 shows the variation of τ as C_1 is varied and I_{01} held constant for a square wave input signal of 10 MHz frequency, and an ac amplitude of 15 μA superimposed on a dc input $D = 50$ μA. Fig. 12 shows how the variation of I_{01} (with C_1 held constant) alters both τ and the dc component present at the output as expected from (23). The results were also confirmed for input signal frequencies up to several tens of megahertz. The dependence of the unity gain frequency upon I_{01} was confirmed; however, the dc gain did not exceed 35–40 dB and in conjunction with the phase errors induced by transistor non-idealities, limits the circuit practicality as a pure integrator. For a sinusoidal input at 10 MHz modulated by 30% and with $\tau = 10.4$ ns, the output THD was 0.258%.

For the Case of the Bandpass Biquad: According to (32), the product of currents $I_{01} I_{03}$ controls the center frequency ω_0 and the ratio I_{q1}/I_d controls the gain factor K_g. The quality factor Q is dependent both on the capacitor values and I_{01}, I_{03}, I_d. Once these values have been selected to give the desired ac response, the designer must also choose the optimum values of V_{ref} and D. Fig. 13 illustrates various ac responses for a center frequency of 10 MHz and $Q = 1$. Observe that the center frequency remains constant—as predicted—when the values of I_{01} and I_{03} vary but their product remains constant. At low frequencies, a finite rejection band is observed, that is related to the finite β value [4], [5], i.e., the higher the β the higher the rejection. Curves (b) and (c) of Fig. 13 underline the importance of selecting the optimum value of V_{ref}, whereas (d) reveals that there are optimum values of currents I_{01} and I_{03}. Curves (a), (b), and

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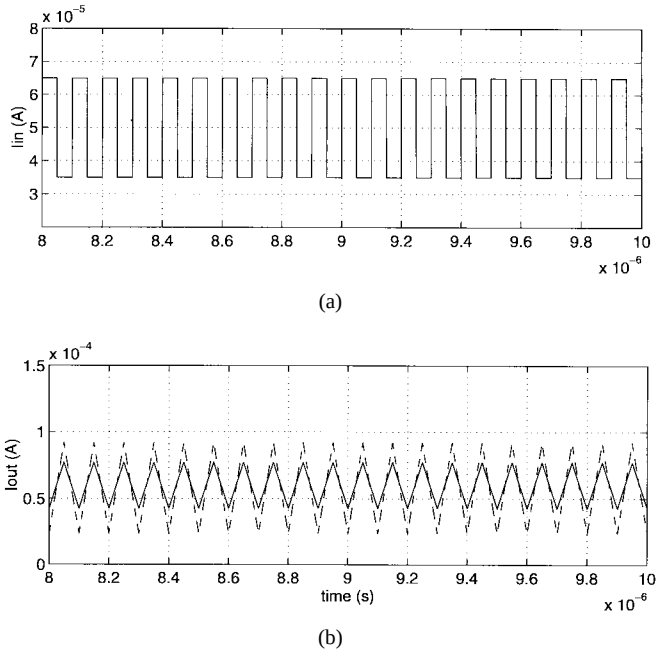

Fig. 11. Integrator output for $D = I_{01} = 50\ \mu$A, $f_{\rm in} = 10$ MHz. —— $C_1 = 40$ pF, $f_\tau = 7.65$ MHz. ----- $C_1 = 20$ pF, $f_\tau = 15.3$ MHz.

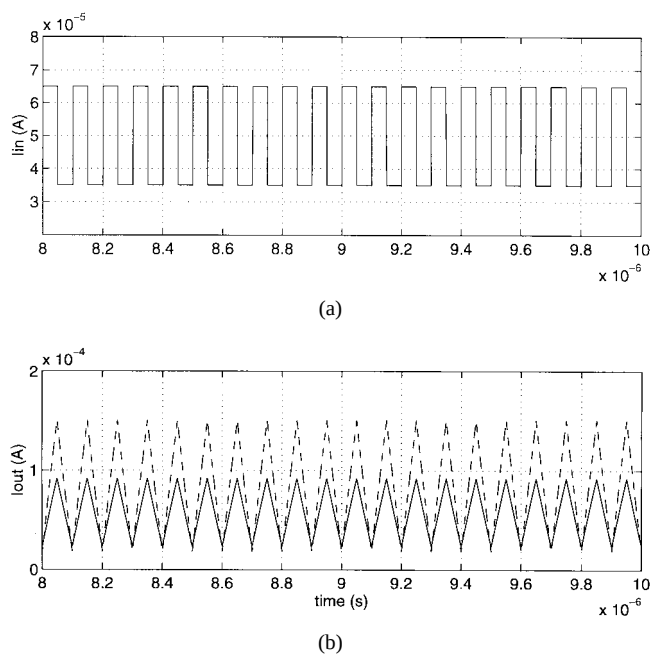

Fig. 12. Alteration of the integration time-constant with current I_{01} when $f_{\rm in} = 10$ MHz; the dc level varies. $D = 50\ \mu$A, $C_1 = 20$ pF. —— $I_{01} = 50\ \mu$A. ----- $I_{01} = 100\ \mu$A.

(d) were confirmed with multitone transient analysis for m up to $\cong$ 30% whereas curve (c) for m up to $\cong$ 10%. For the extreme case of curve (e)—which is very close to the ideal theoretical bandpass response—a 1 kHz tone with m higher than $\sim$0.5% would *not* be rejected by 70 dB; when $m = 10\%$ the rejection equals 50 dB, whereas when $m = 20\%$ the rejection reduces further to 40 dB. Referring to curve (c) a low frequency (10 kHz) input signal with $m \cong 30\%$ turns Q_{u1} off and the filter becomes a lossy integrator. For the design of log-domain filters, large multitone transient simulations should be considered as a time-consuming necessity when accurate large signal ac analysis are to be obtained especially when the BJT's are forced to operate with significant current level differences. Fig. 14 shows higher center frequency tuning and reveals that the higher the center frequency, the higher the deviation from the theoretically predicted response. This kind of deviation is primarily due to the presence of the parasitic ohmic resistances and the parasitic capacitances $(C_\pi, C_{\rm col-sub})$ [4], [21]. When $I_{01} > I_{03}$ (e.g., $I_{01} = 625\,\mu$A, $I_{03} = 400\,\mu$A, the circuit exhibits better rejection at low frequencies and better linearity in the passband. In Fig. 15, Q tuning for a given center frequency is shown; the curves correspond to quality factor values of 1, 2, and 3.33 accomplished by altering the value of I_d. For comparison the theoretical response for the case of $Q = 3.33$ is also shown. For these simulations small resistors in series with the capacitors were used to prevent Q-enhancement, as suggested in [12]. Better results were achieved when D was equal to the I_d value. However, when significant differences between the input and the output dc levels occur, then a small modulation index at the input would correspond to a large modulation index at the output. Finally, Fig. 16 illustrates an example of Q tuning by altering the capacitor values, with $C_1 = 100$ pF and $C_2 = 9$ pF. For comparison, the response for $Q = 1$ and the theoretical response for $Q = 3.33$ are also shown. The strong capacitor value assymetry affects the linearity in the passband. Better results can be obtained when $I_{01} > I_{03}$ withh the product $I_{01}I_{03}$ remaining constant (e.g., $I_{01} = 142.8\,\mu$A, $I_{03} = 70\,\mu$A, a case not shown in Fig. 16. The results shown in Figs. 13–16 are indicative only and do not correspond to optimized ones. In Figs. 15 and 16, for example, $I_{\rm ref}$ was kept constant; however, in general it is when all currents do not differ significantly that optimized results can be obtained. Thus different combinations of $I_{\rm ref}$, $V_{\rm ref}$ along with different gain factor values might result in improved performance. As a final comment it should be emphasized that the fact that all transistors have to operate in class-A (recall the remark concerning curve (c) of Fig. 13) dictates that the output dc level should be carefully determined when comparable modulation indices at both input and output can be obtained.

Generally speaking, the simulation results verified the validity of the transistor-level approach developed in Sections II–V and also revealed certain design options and performance limitations.

VIII. Conclusions

This paper has presented a systematic transistor-level approach suitable for the design of linear log-domain filters. The method is based on a set of linear differential equations termed log-domain state-space, and created via the identification of a low-level nonlinear analog cell governed by the Bernoulli differential equation. The approach identifies a convenient form of low-level nonlinear dynamics in log-domain structures, it reveals an alternative (other than exponential) current-related form for the log-domain state-variables, and also indicates the possibility for implementing nonlinear applications. Simula-

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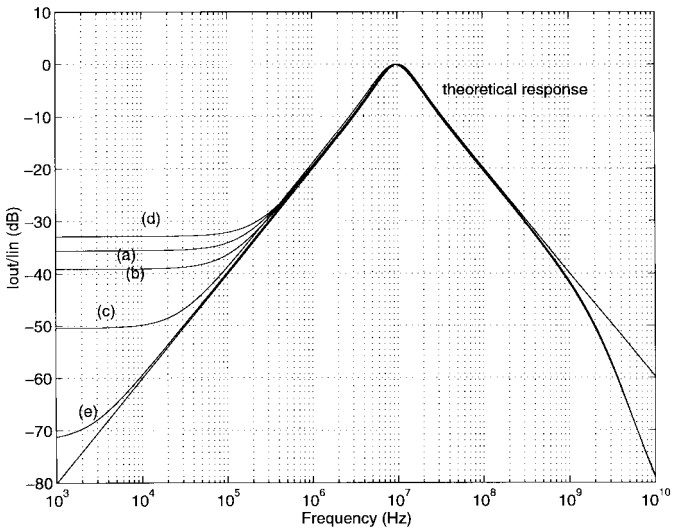

Fig. 13. Simulated bandpass frequency response with a center frequency $f_0 \cong 10$ MHz and $Q = 1$; $D = I_d = I_{q1} = I_{\rm ref} = 50\ \mu$A, $C_1 = C_2 = 30$ pF. (a) $I_{01} = 50\ \mu$A, $I_{03} = 50\ \mu$A, $V_{\rm ref} = -12$ mV. (b) $I_{01} = 35\ \mu$A, $I_{03} = 71.4\ \mu$A, $V_{\rm ref} = -23$ mV. (c) $I_{01} = 35\ \mu$A, $I_{03} = 71.4\ \mu$A, $V_{\rm ref} = -19$ mV. (d) $I_{01} = 71.4\ \mu$A, $I_{03} = 35\ \mu$A, $V_{\rm ref} = -12$ mV. (e) $I_{01} = 20\ \mu$A, $I_{03} = 125\ \mu$A, $V_{\rm ref} = -39$ mV.

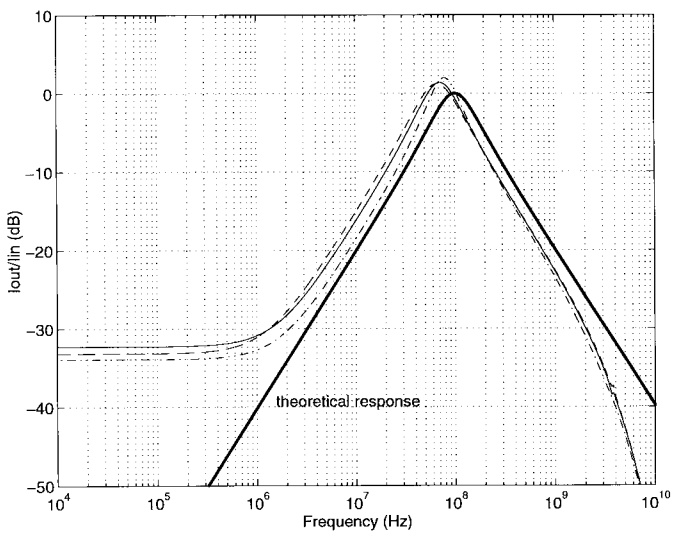

Fig. 14. Simulated bandpass frequency response with center frequency $f_0 = 100$ MHz and $Q = 1$. —— $D = I_d = I_{q1} = I_{\rm ref} = I_{01} = I_{03} = 500\ \mu$A, $C_1 = C_2 = 30$ pF, $V_{\rm ref} = -12$ mV. ——— $D = I_d = I_{q1} = I_{\rm ref} = 500\ \mu$A, $I_{01} = 400\ \mu$A, $I_{03} = 625\ \mu$A, $C_1 = C_2 = 30$ pF, $V_{\rm ref} = -17$ mV. -.-.-.-.-.-. $D = I_d = I_{q1} = I_{\rm ref} = 500\ \mu$A, $I_{01} = 625\ \mu$A, $I_{03} = 400\ \mu$A, $C_1 = C_2 = 30$ pF, $V_{\rm ref} = -12$ mV.

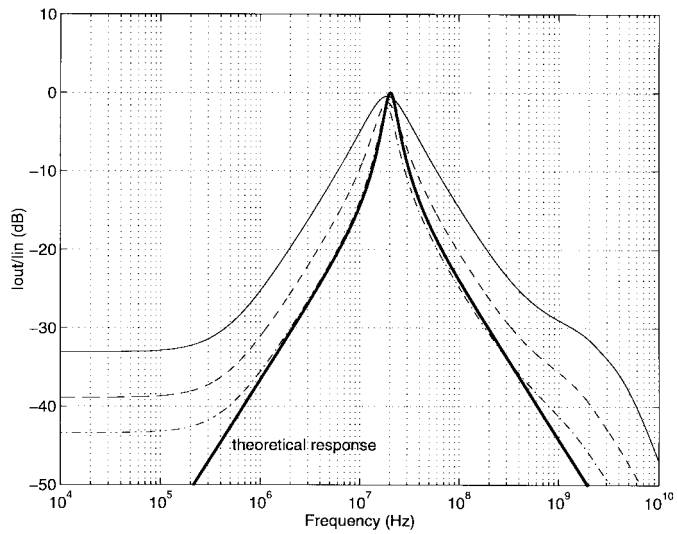

Fig. 15. Q-tuning via I_d. —— $D = 100\ \mu$A, $I_{01} = I_{03} = 100\ \mu$A, $I_d = 100\ \mu$A, $I_{\rm ref} = 50\ \mu$A, $C_1 = C_2 = 30$ pF, $R = 10\ \Omega$, $V_{\rm ref} = 0$ V, $I_{q1} = 100\ \mu$A. ----- $D = 50\ \mu$A, $I_{01} = I_{03} = 100\ \mu$A, $I_d = 50\ \mu$A, $I_{\rm ref} = 50\ \mu$A, $C_1 = C_2 = 30$ pF, $R = 10\ \Omega$, $V_{\rm ref} = -10$ mV, $I_{q1} = 50\ \mu$A. -.-.-.-.-.-. $D = 30\ \mu$A, $I_{01} = I_{03} = 100\ \mu$A, $I_d = 30\ \mu$A, $I_{\rm ref} = 50\ \mu$A, $C_1 = C_2 = 30$ pF, $R = 10\ \Omega$, $V_{\rm ref} = -20$ mV, $I_{q1} = 30\ \mu$A.

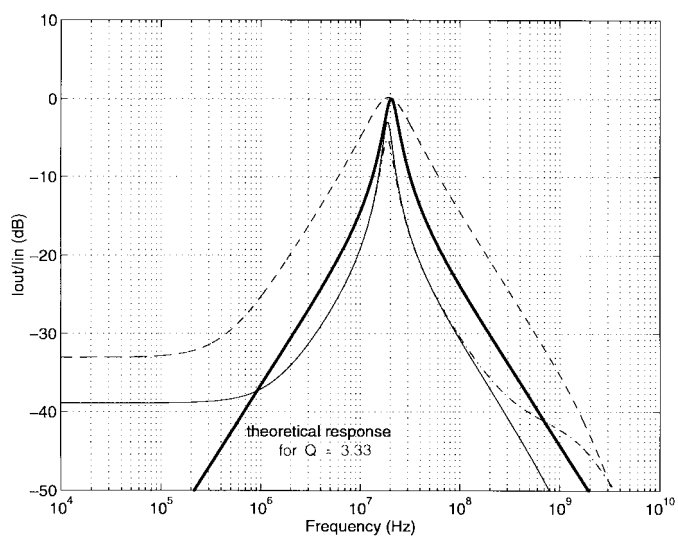

Fig. 16. Q-tuning via C_1, C_2. ---- $Q = 1$, $D = 100\ \mu$A, $I_d = 100\ \mu$A, $I_{\rm ref} = 50\ \mu$A, $C_1 = C_2 = 30$ pF, $R = 0\ \Omega$, $V_{\rm ref} = 0$ V, $I_{q1} = 100\ \mu$A. —— $Q = 6.67$, $D = 50\ \mu$A, $I_d = 50\ \mu$A, $I_{\rm ref} = 50\ \mu$A, $C_1 = 100$ pF, $C_2 = 9$ pF, $R = 0\ \Omega$, $V_{\rm ref} = -10$ mV, $I_{q1} = 50\ \mu$A. -.-.-.-.-. $Q = 6.67$, $D = 50\ \mu$A, $I_d = 50\ \mu$A, $I_{\rm ref} = 50\ \mu$A, $C_1 = 100$ pF, $C_2 = 9$ pF, $R = 5\ \Omega$, $V_{\rm ref} = -10$ mV, $I_{q1} = 50\ \mu$A.

tion results confirming the operation for an integrator and a bandpass biquad were also presented.

APPENDIX

For quality factor values $Q > 0.5$, the following will hold:

$$\frac{1}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} = \frac{1}{\left(s + \frac{\omega_0}{2Q}\right)^2 + \left[\omega_0\sqrt{1 - \frac{1}{4Q^2}}\right]^2}$$

$$\Rightarrow L^{-1}\left\{\frac{1}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}\right\} = \frac{\exp\left(-\frac{\omega_0}{2Q}t\right)}{\omega_0\sqrt{1 - \frac{1}{4Q^2}}}\ \sin\left\{\omega_0\sqrt{1 - \frac{1}{4Q^2}}t\right\} \tag{A.1}$$

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$$\begin{aligned}
&\frac{s}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2} \\
&\quad = \frac{\left(s+\frac{\omega_0}{2Q}\right)}{\left(s+\frac{\omega_0}{2Q}\right)^2+\left[\omega_0\sqrt{1-\frac{1}{4Q^2}}\right]^2} \\
&\qquad - \frac{\frac{\omega_0}{2Q}}{\left(s+\frac{\omega_0}{2Q}\right)^2+\left[\omega_0\sqrt{1-\frac{1}{4Q^2}}\right]^2} \\
&\quad \Rightarrow L^{-1}\left\{\frac{s}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2}\right\} \\
&\quad = \exp\left(-\frac{\omega_0}{2Q}t\right)\cos\left\{\omega_0\sqrt{1-\frac{1}{4Q^2}}t\right\} \\
&\qquad - \frac{\exp\left(-\frac{\omega_0}{2Q}t\right)}{\sqrt{4Q^2-1}}\sin\left\{\omega_0\sqrt{1-\frac{1}{4Q^2}}t\right\} \qquad \text{(A.2)}
\end{aligned}$$

$$\begin{aligned}
&\frac{1}{s\left[s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2\right]} \\
&\quad = \frac{\left(\frac{1}{\omega_0^2}\right)}{s} - \left(\frac{1}{\omega_0^2}\right)\frac{s}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2} \\
&\qquad - \frac{1}{(\omega_0 Q)}\,\frac{1}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2}. \qquad \text{(A.3)}
\end{aligned}$$

Equations (A.1) and (A.2) correspond to exponentially decaying time-domain terms. The last two terms of (A.3) similarly correspond to transient terms in the time domain. Thus, (32) (main text) describes a bandpass filtered version of the input superimposed on a dc component which equals

$$I_{q1}\,\frac{I_{01}I_{03}}{C_1C_2V_T^2}\,\frac{1}{\omega_0^2}n_2.$$

ACKNOWLEDGMENT

The authors would like to thank Ericsson Microelectronics Research Centre (MERC) for sponsoring this work, and the unknown reviewers for their fruitful comments and suggestions which significantly improved the readability of the paper.

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