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Synaptic Barristor Based on Phase-Engineered 2D Heterostructures

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The development of energy-efficient artificial synapses capable of manifoldly tuning synaptic activities can provide a significant breakthrough toward novel neuromorphic computing technology. Here, a new class of artificial synaptic architecture, a three-terminal device consisting of a vertically integrated monolithic tungsten oxide memristor, and a variable-barrier tungsten selenide/graphene Schottky diode, termed as a 'synaptic barrister,' are reported. The device can implement essential synaptic characteristics, such as short-term plasticity, long-term plasticity, and paired-pulse facilitation. Owing to the electrostatically controlled barrier height in the ultrathin van der Waals heterostructure, the device exhibits gate-controlled memristive switching characteristics with tunable programming voltages of 0.2–0.5 V. Notably, by electrostatic tuning with a gate terminal, it can additionally regulate the degree and tuning rate of the synaptic weight independent of the programming impulses from source and drain terminals. Such gate tunability cannot be accomplished by previously reported synaptic devices such as memristors and synaptic transistors only mimicking the two-neuronal-based synapse. These capabilities eventually enable the accelerated consolidation and conversion of synaptic plasticity, functionally analogous to the synapse with an additional neuromodulator in biological neural networks.

Tremendous efforts have been recently devoted to developing a neuroinspired electronic system, mimicking the exceptionally energy-efficient neural networks in the human brain.[1–5] The first step toward realizing a massively parallel neuromorphic system is to develop an artificial synapse capable of emulating diverse synaptic functionality, such as short- and long-term plasticity,[6–8] with ultralow power consumption and robust controllability. Diverse oxide, organic, or carbon-based materials have intensively investigated as promising candidates for artificial synaptic devices.[9–24] In addition, many synaptic device architectures, such as resistive memories, memristors, electrochemical transistors, have been employed to emulate a biological synapse linked between presynaptic and postsynaptic neurons, in which synaptic plasticity is solely determined by spatiotemporal input spikes from only two neurons. Despite remarkable progresses in recent years, for the realization of higher-level learning and computing capability, there have been continuously growing demands on developing new materials and synaptic architectures that can demonstrate a high order of synaptic activity without a large power consumption and undesirable interference between neighboring synapses in an artificial neural network.

Heterostructures built from various 2D layered materials, including semimetallic graphene, semiconducting transition metal dichalcogenides, and insulating hexagonal boron nitride, are emerging material platforms for low-power and high-performance electronic devices because of their high-quality heterointerfaces with atomic precision as well as the exceptional properties from their atomically thin constituent materials.[25–28] In addition, the competitive ability to electrostatically control the energy barrier (or band alignment) at the van der Waals (vdW) interfaces allows us to rationally design 2D functional heterostructures by band-structure engineering for a variety of gate-tunable electronic devices.[29–37] Particularly, a vertical triode with a gate-controlled Schottky barrier, so-called the 'barristor,' has been proposed as a new switching device with potential advantages in scaling and integrating highly networked device functionality. Such unique capabilities of 2D heterostructured devices can also offer unexplored opportunities for realizing an energy-efficient artificial synapse with high controllability. Nevertheless, the artificial synapse based on 2D heterostructures has rarely been demonstrated, as appropriate materials with robust memristive

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switching characteristics and an adequately integrated device architecture are not available.

Here, we demonstrate a modifiable synaptic architecture based on the phase-engineered tungsten oxide/selenide monolithic heterojunction for diverse synaptic functionality accompanied with low power and interference-controlled operation. Notably, the electrostatic gating can greatly accelerate the variation in synaptic weights and transform the intrinsic characteristics of synaptic plasticity; hence, we termed this device the 'synaptic barristor.' Such functionality is similar to that of the synapse with an additional neuromodulator in biological neural networks, which has rarely been emulated by other synaptic devices thus far (Table S1, Supporting Information).

Figure 1a presents a schematic illustration and a circuit diagram of the synaptic barristor. This three-terminal device can be considered a gate-tunable memristor composed of a WO_{3-x} resistive memory and a WSe_2/graphene barristor. The WSe_2/graphene heterojunction, which is formed by vdW assembly of the mechanically exfoliated WSe_2 layers on graphene, acts as a variable-barrier Schottky diode owing to the electrostatically tuned work function of graphene. Unlike typical memristors based on metal/oxide/metal structures, it is critical to have the layered semiconducting WSe_2 in our synaptic barristor because its vdW surface enables to form the variable-barrier contact with the graphene without Fermi-level pinning.[29,38] This bottom barristor component enables to electrically regulate the total current flow through the entire device by controlling the gate voltage; hence, the switching states in the vertically integrated memristor can be actively tuned. The WO_{3-x} layer, in contact with the top electrode, was monolithically grown by UV-ozone oxidation of WSe_2 (Figure 1b).[39] This oxide layer facilitates fundamental memristive functions in the phase-engineered 2D heterostructure. Figure 1c shows an optical image of the back-gated device fabricated on the ≈280 nm thick SiO_2/Si substrate, and the detailed fabrication processes are provided in Figure S1 in the Supporting Information.

We further performed cross-sectional transmission electron microscopy (TEM) and energy-dispersive spectroscopy (EDS) analyses to verify the compositions and structures of the constituent layers in the phase-engineered 2D monolithic heterojunction. The high-resolution TEM and EDS elemental mapping images in Figure 1d,e clearly show that an amorphous WO_{3-x} layer with a thickness of ≈10 nm is formed, forming an abrupt junction with layered WSe_2 owing to the monolithic oxidation in a layer-by-layer manner. The composition of the WO_{3-x} layer further confirmed by analyzing the

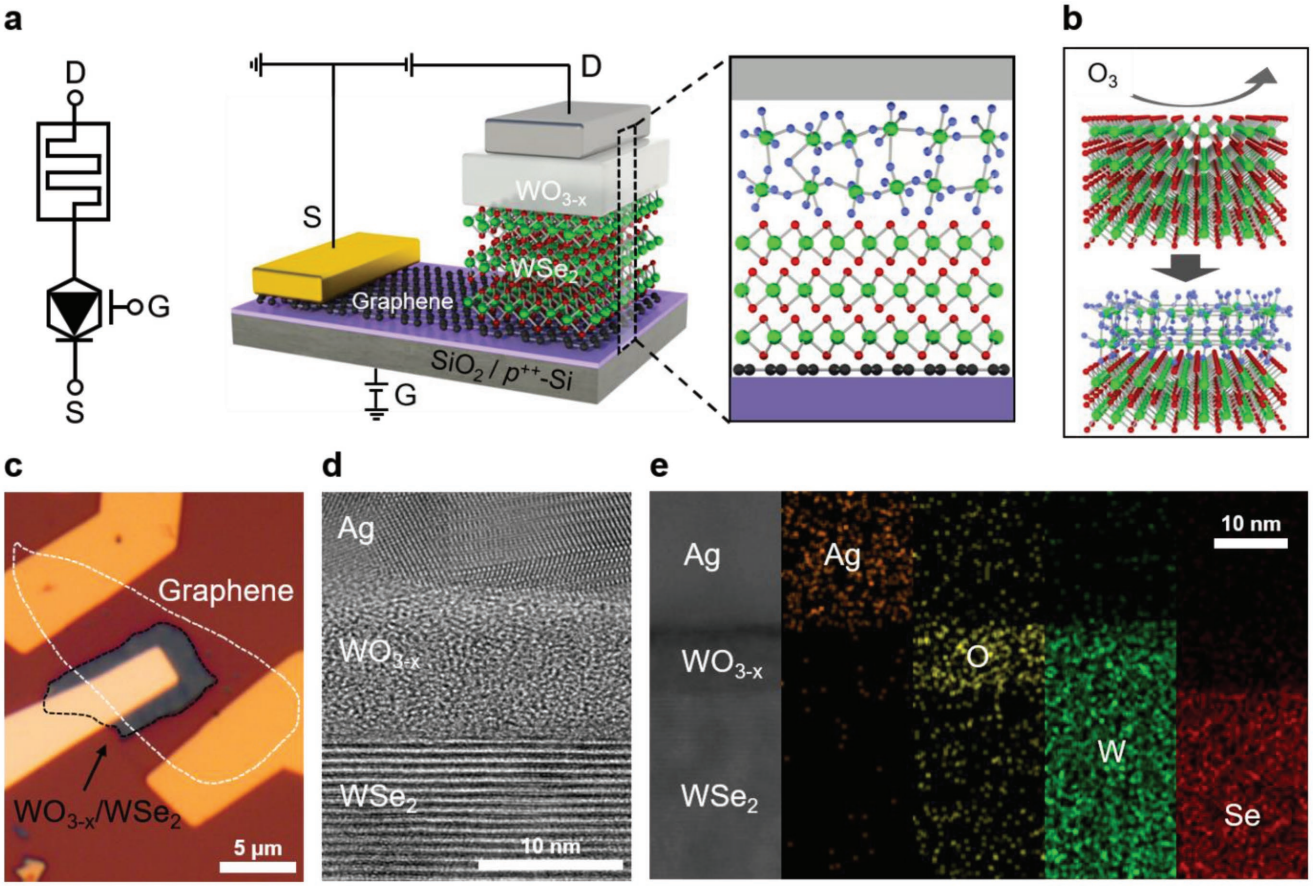

Figure 1. Synaptic barristor. a) Circuit and schematic representation of diagrams of the synaptic barristor consisting of a vertically integrated WO_{3-x} memristor and WSe_2/graphene barristor. b) Schematic illustration of the monolithic oxidation process by UV-ozone treatment. This process converts the topmost WSe_2 layer to amorphous WO_{3-x}. c) Optical image of the fabricated device. Scale bar is 5 μm. d) Cross-sectional HR-TEM image and e) EDS analysis with elemental mapping of silver (Ag), oxygen (O), tungsten (W), and selenium (Se) of the Ag/WO_{3-x}/WSe_2 structure, showing the heterointerfaces of the top Ag electrode, amorphous WO_{3-x}, and layered WSe_2 films. Scale bar is 10 nm.

oxidized WSe_2 layer using X-ray photoemission spectroscopy (Figures S2 and S3, Supporting Information). In addition, we observed the interfacial layer with a slightly different contrast at the Ag/WO_{3-x} interface (see the EDS line profile in Figure S8 in the Supporting Information). Such an ultrathin layer may be formed by partial oxidation of Ag, presumably inducing oxygen vacancies in the vicinity of the interface, which would attribute to memristive switching.[3,40–44]

The current–voltage (I_D–V_D) characteristics of the 2D heterostructured device are drastically altered by the presence of the intermediate WO_{3-x} layer, as shown in **Figure 2**a. The device composed of Ag/WO_{3-x}/WSe_2/graphene heterostructures exhibits a typical resistive switching hysteresis loop in the I_D–V_D curve upon sweeping the source-drain voltage (V_D) at the zero gate voltage (V_G). In contrast, such hysteresis is not observed in the Ag/WSe_2/graphene device (Figure S4, Supporting Information). The device with the WO_{3-x} layer exhibits a transition from a high-resistance state (HRS) to a low-resistance state (LRS) in negative V_D polarity corresponding to the "SET" process and vice versa in positive V_D polarity corresponding to the "RESET" process, indicating bipolar resistive switching. To verify the potential switching mechanism, we performed several additional experiments including electrical measurements (Figures S6 and S7, Supporting Information) and cross-sectional TEM/EDS analyses (Figures S8–S10, Supporting Information) for the control devices using different metal electrodes including titanium (Ti) and gold (Au). Based on the existence of interfacial oxide layer between Ag (or Ti) and WO_{3-x} and the bipolar switching with the negative SET voltage, the switching behavior may be attributed to the migration of oxygen vacancies and electrochemical redox reactions at the Ag (or Ti)/WO_{3-x} interface. Meanwhile, we believe that forming a metallic filament by diffusion of the top Ag cations may not be the dominant switching mechanism because of the low current level (≈10^{-8} A for LRS) measured in our controlled devices including Ag/WO_{3-x}/WSe_2/graphene (Figure 2a), Ag/WO_{3-x}/Au (Figure S5a, Supporting Information) and Ag/WO_{3-x}/WSe_2/Au (Figure S5b, Supporting Information) structures (see Supporting Information for the detailed results and discussion). Nevertheless, since the filament–dominant mechanism cannot

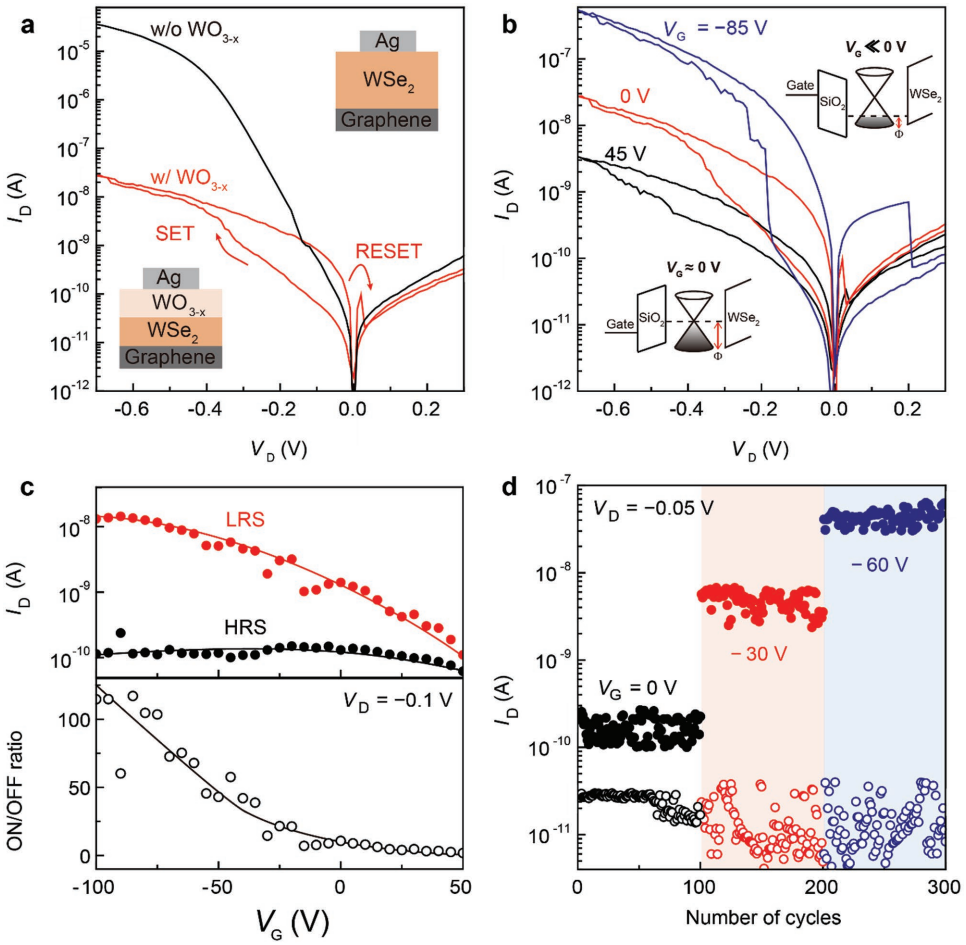

Figure 2. Gate-tunable-resistive switching characteristics. a) I_D–V_D curves of the devices with (red line) and without a WO_{3-x} layer (black line). Insets show schematic representation of the diagrams of the devices. The "SET" and "RESET" processes are indicated by the up and down arrows, respectively. b) Switching I_D–V_D curves at various V_G values of −85, 0, and 45 V. The V_{SET} values are indicated by the dashed arrows. c) I_D–V_G curves for the HRS and LRS (upper panel) and corresponding ON/OFF ratio as a function of V_G (bottom panel). Inset in the bottom panel shows band diagrams for the graphene/WSe_2 junction when V_G ≈0 V (right) and V_G << 0 V (left). The Schottky barrier height (Φ) indicated by the red arrow is lowered at V_G << 0 V. d) I_D as a function of the number of cycles for the HRS (open circles) and LRS (solid circles) as the V_G is adjusted to 0, −30, and −60 V.

be completely excluded and partly contributes to the switching in our devices, the advanced study such as in situ TEM analysis of a specifically designed junction structure should be further performed to understand the exact switching mechanism, which may be out of the scope of this work.

More interestingly, the switching phenomena are considerably modulated by varying the V_G, as shown in Figure 2b. Sweeping the V_G to a higher negative bias shifts the 'SET' voltage (V_{SET}) to a lower absolute value, reaching as low as –0.18 V at V_G = –85 V. Simultaneously, the size of resistive switching window is enlarged. The current level of the LRS (denoting ON) gradually increases from 0.1 to 10 nA, while that of the HRS (denoting OFF) remains nearly constant at ≈0.1 nA, achieving an ON/OFF ratio greater than 100 at V_G < –85 V (Figure 2c). This high ON/OFF ratio results from the overall conductance being limited by the highly resistive WO_{3-x} layer at the HRS. Meanwhile, at the LRS, the conductance is predominantly determined by the gate-tunable Schottky barriers formed at the WSe_2/graphene junction, hence increasing the switching current at a larger negative V_G. Note that the gate voltages applied here are determined by the gate capacitance, which can be easily reduced by adjusting the back-gate oxide thickness.

Such gate-tunable memristive switching characteristics can be qualitatively explained by the energy-band alignments according to the V_G (inset of Figure 2c). When the V_G changes from zero to negative bias, the Schottky barrier formed at the WSe_2/graphene heterojunction is lowered because the Fermi level of graphene decreases due to graphene hole doping,[38] thus allowing majority carriers, i.e., holes, to more easily flow from graphene to WSe_2 at a larger negative V_G. In addition, from the lowered barrier height and consequently reduced series resistance at the WSe_2/graphene junction, the effective voltage drop across the WO_{3-x} layer is enlarged, allowing a lower V_{SET} (from –0.45 to –0.18 V). Remarkably, the device consumes low switching power down to 0.1 nW presumably due to its atomic thinness. This value is several orders of magnitude lower than those of other WO_{3-x}-resistive memories (Figure S11, Supporting Information), suggesting the potential of this device as an energy-efficient artificial synapse. Furthermore, as shown in Figure 2d, the device increases the ON/OFF ratio up to 10^5 without degradation in their states upon varying V_G, exhibiting robust modulation and stability in switching. Note that our device shows good cycling endurance for ≈10^3 times and retention for ≈10^3 s (Figure S12, Supporting Information).

Another noteworthy feature of the device is its highly asymmetric memristive switching characteristics presumably due to the asymmetric Schottky barrier between Ag/WO_{3-x} (top) and graphene/WSe_2 (bottom) contacts (Figure 2a,b), which inherently prevents an unwanted interference effect among individual synapses.[41] The degree of asymmetry becomes larger at negative gate voltages because the WSe_2/graphene barrier is only lowered by electrostatic gating (Figure 2b). This feature along with gate tunability and low power consumption make our device promising for mimicking diverse synaptic functionalities with additional controllability in massively parallel neuromorphic computing.

Our monolithic memristor can basically emulate two-neuronal-based synaptic functions even without the application of gate voltages. As shown in **Figure 3**a, here, we define the top metal electrode (drain) and the bottom electrode (source) as pre- and postneurons, respectively. The synaptic weight represented by the degree of connectivity between the pre- and postneurons is simply described by the postsynaptic current (PSC) magnitude when the input spikes stimulate the synapse.[8] The ability to control and retain the synaptic weight over time is defined as synaptic plasticity, classified into two forms: short-term plasticity (STP) and long-term plasticity.[6–8] To examine the synaptic plasticity of the device, we first investigated the PSC change by diverse electrical stimuli of input spikes from pre- and postneurons. Figure 3b shows the PSC change corresponding to the drain current at V_D = –0.1 V and V_G = 0 V while applying sequential input spikes with an amplitude (V_A) of –3 V, width (V_W) of 10 ms and interval (Δt) of 2 s. The PSC gradually increases as consecutive input spikes are stimulated at the synapse, mimicking the behavior of long-term plasticity, namely, long-term potentiation (LTP).[6] This analog-like switching might be attributed to a change in the oxygen vacancy density at the Ag/WO_{3-x} interface depending on the accumulated input spikes.[3,44] Additionally, as shown in Figure 3c, the synaptic device can be further programmed to mimic either STP or LTP depending on the number of input spikes (N). For example, the increased PSC recovers to its original value when $N \leq 5$, mimicking STP, while the PSC is persistent when $N > 10$, mimicking LTP (Figure 3c).

Synaptic plasticity can also be modified by the time interval when two sequential spikes stimulate the synapse. Such behavior has been considered the paired-pulse facilitation (PPF) feature of a synapse, providing flexibility for several neuronal tasks, such as simple learning and information processing in the frequency domain.[7] Figure 3d shows the characteristic of PPF (= $(A_1 - A_2)/A_1 \times 100$ %) as a function of the time interval when two sequential spikes generate PSC peaks, A_1 and A_2 (Figure S13, Supporting Information). Note that a single spike (V_A = –2.0 V and V_W = 10 ms) used here is not sufficient to change the PSC upon individual stimulating. The PPF values exponentially decay as the interval increases, and this decay showed the best agreement with the fitting function with two decaying time constants of $C_1\exp(-\Delta t/\tau_1) + C_2\exp(-\Delta t/\tau_2)$ (Figure S14, Supporting Information). Using C_1 and C_2 as fitting parameters, we obtained two decaying time constants, τ_1 = 17 ms and τ_2 = 640 ms. This PPF behavior is similar to the reported one in biological synapses, indicating our synaptic barristor can functionally mimic the biological synapse.[7] As shown in Figure 3e, we could implement either STP or LTP using different intervals (Δt = 30 or 300 ms). At Δt = 30 ms, the PSC gradually increases and tends to saturate with an increasing number of spikes, mimicking LTP. In contrast, the PSC does not noticeably change at Δt = 300 ms, mimicking STP. Note that the device can also exhibit long-term depression (LTD)[6] by consecutively applying a series of depressing spikes (V_A = 0.5 V, V_W = 5 ms, and N = 30) at V_G = 0 V (Figure S15, Supporting Information).

Our synaptic barristor in a three-terminal configuration can similarly emulate the functional role of an additional neuromodulator operated in the biological synapse that consists of three essentials, including a non-neuronal neuromodulator, pre- and postneurons (**Figure 4**a). The neuromodulator such as an astrocyte was recently proposed to play a critical role in

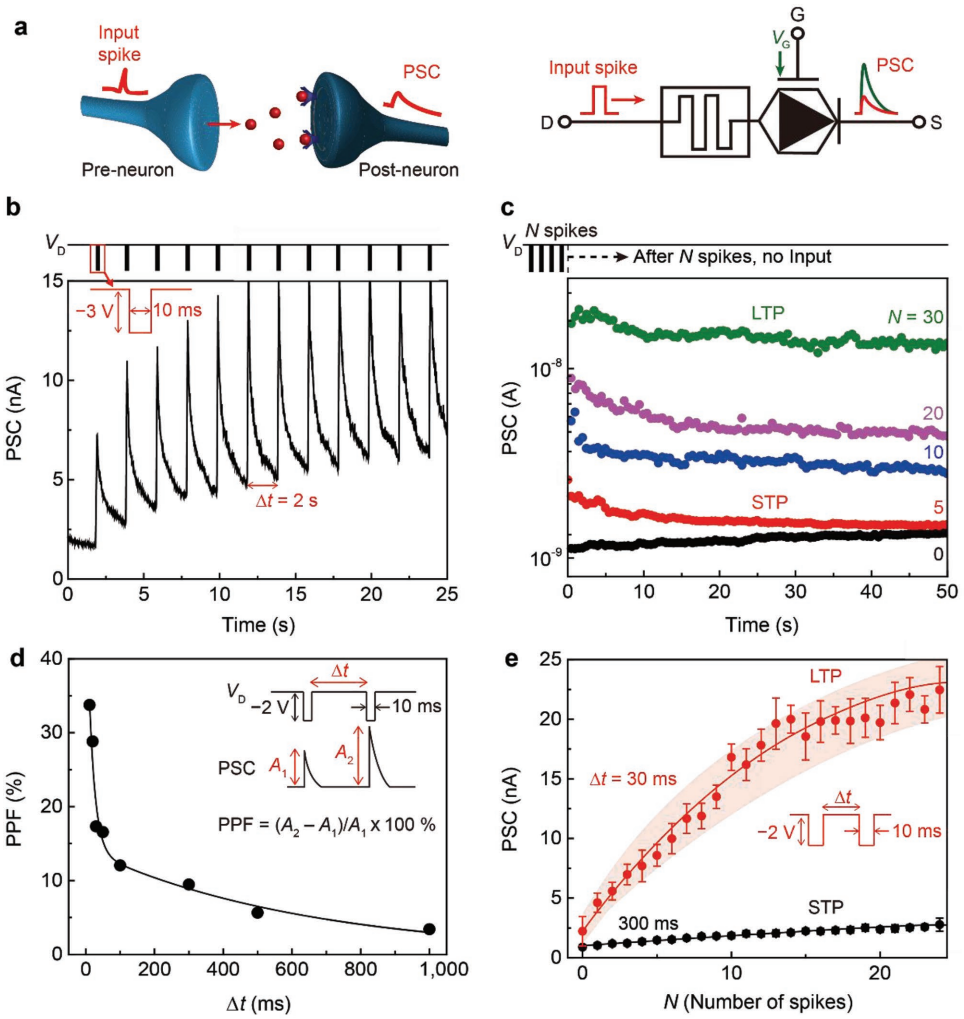

Figure 3. Artificial synaptic characteristics. a) Schematic illustration and the corresponding circuit diagram of the synaptic barristor at $V_G = 0$ V. Plots of PSC as a function of time b) while applying input spikes and c) after stimulating with a certain number of input spikes ($N = 0$, 5, 10, 20, and 30). Potentiating pulses ($V_W = 10$ ms, $V_A = -3$ V, and $\Delta t = 2$ s) were used. The PSCs are measured at $V_D = -0.1$ V in panel (b) and $V_D = -0.3$ V in panel (c). d) PPF characteristics as a function of the time interval. Two PSC peaks (A_1 and A_2) were triggered by the paired pulses ($V_A = -2$ V and $V_W = 10$ ms) with various intervals ($\Delta t = 11$, 20, 30, 50, 100, 500, and 1000 ms). The black solid circles and line are the experimentally measured values and the fitted curve, respectively. e) Plot of PSC as a function of the number of spikes with different intervals ($\Delta t = 30$ and 300 ms). The same input spikes ($V_A = -2$ V and $V_W = 10$ ms) were used, and the PSCs are measured at $V_D = -0.1$ V in panels (d) and (e).

cellular programing to achieve a high level of neural information processing.[45] Importantly, in those synapses, synaptic transmission can be further activated by intimate association of pre- and postsynaptic membranes with the surrounding neuromodulator.[45–48]

As shown in Figure 4a, here, we define the gate, drain, and source terminals of the synaptic device as a neuromodulator, pre- and postneurons, respectively. Unlike conventional two-neuronal-based synaptic devices, the synaptic weight in the synaptic barristor can be additionally controlled by modulating the V_G independent of the input spikes from neurons, where the role of the gate terminal is analogous to that of a neuromodulator as the gatekeeper for synaptic plasticity.[48] The collaborative contribution of the neuromodulator and neurons allows accelerated synaptic consolidation and conversion from short- to long-term memory.[46,47] Figure 4b clearly demonstrates that synaptic plasticity, such as LTP and LTD, is further accelerated by applying a larger negative V_G, corresponding to the consolidation of long-term memory. This behavior originates from the effective electric field across the WO_{3-x} layer strengthening as the Schottky barrier at the WSe_2/graphene junction decreases, resulting in an increasing dynamic variation range of the PSC. Utilizing this capability achieved by electrostatic gating, we could even modify the intrinsic type of the synaptic plasticity. As shown in Figure 4c, the PSC gradually increases by adjusting the V_G to −30 V (right panel), while the application of the same input spikes ($V_A = -1$ V, $V_W = 10$ ms, and $\Delta t = 1$ s) did not cause a noticeable increase in the PSC at $V_G = 0$ V (left panel). This result implies the conversion from STP to LTP, mimicking the essential role of a neuromodulator. Notably, gate-induced tuning of the synaptic functionality is controlled electrostatically, while considerable electrical power is inevitably consumed

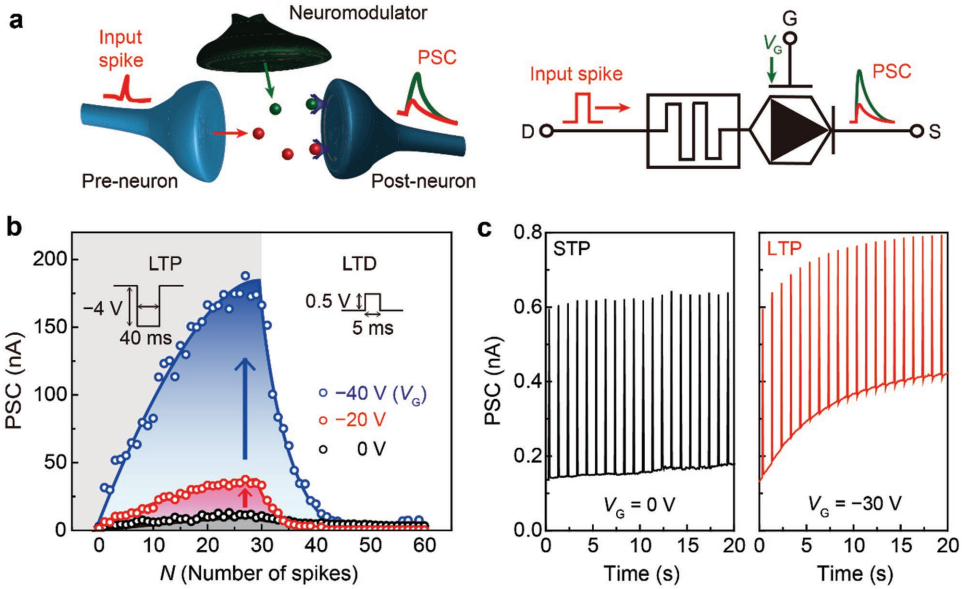

Figure 4. Gate-tunable synaptic characteristics. a) Schematic illustration of the synaptic barristor and the corresponding circuit diagram of the synaptic barristor. b) Plots of PSC as a function of the number of input spikes while consecutively applying a series of potentiating spikes ($V_A = -4$ V, $V_W = 40$ ms, and $N = 30$) and depressing spikes ($V_A = 0.5$ V, $V_W = 5$ ms, and $N = 30$) at various V_G values of 0, −20, and −40 V. c) Plots of PSC as a function of time while applying spikes ($V_A = -1.0$ V, $V_W = 10$ ms, and $\Delta t = 1$ s) at $V_G = 0$ V (left panel) and $V_G = -30$ V (right panel). All PSCs are measured at $V_D = -0.1$ V.

to achieve weight tuning by amplifying the potential and/or frequency of input spikes from neurons. Furthermore, the ability to accelerate the modulation of the synaptic weight can offer potential advantages to improve the recognizing accuracy and to reduce the learning time of the pattern recognition.[49]

In summary, we demonstrated a new artificial synaptic architecture by monolithically integrating a memristor and a barristor using phase-engineered 2D heterostructures. The synaptic barristor in a three-terminal configuration could implement fundamental synaptic functions, including STP, PPF, LTP, and LTD, with external gate controllability. This architecture potentially offers considerable power-saving benefits when greatly tuning the synaptic weights and intrinsically modifying the synaptic plasticity in comparison to conventional two-neuronal-based synaptic architectures. Our demonstration represents an important step toward highly networked and energy-efficient neuromorphic circuits.

Experimental Section

Fabrication: The WO_{3-x}/WSe_2/graphene stacks were fabricated using typical mechanical exfoliation, vdW assembly, and transfer methods. Graphene and WSe_2 layers were exfoliated separately on Si substrates with the thermally grown 285 nm thick SiO_2 layers. Then, the exfoliated WSe_2 layers with a thickness of 30–60 nm were monolithically oxidized by UV-ozone treatment at 300 °C, forming the ≈10 nm thick WO_{3-x} film from the topmost WSe_2 layers. This WO_{3-x}/WSe_2 heterostructure was lifted up using the polypropylene carbonate (PPC)/polydimethyl siloxane stamp, and then the entire structure was mechanically transferred onto the exfoliated graphene layer. The remained PPC layer was removed by dipping the substrate into acetone solution. To define the top and bottom electrodes, we performed an e-beam lithography using the poly(methylmethacrylate) bilayer as an e-beam resist, followed by metal deposition of Cr/Pd/Au (1/15/40 nm) for the bottom graphene contact and Ag (110 nm) for the top WO_{3-x} contact using an e-beam evaporator. The fabrication processes are schematically shown in Figure S1 in the Supporting Information.

Electrical Characterization: The basic electrical characteristics, including *I–V* curves, retention, and endurance properties, were measured using a vacuum probe station equipped with a semiconductor parameter analyzer (4155C, Keysight) and a low-leakage switch mainframe (E5250A, Keysight). For the artificial synaptic characterization, electrical pulses with various amplitudes, widths, and time intervals were applied with a pulse generator (81104A, Keysight). In addition, a device current waveform analyzer (CX3300, Keysight) was used for high-frequency current measurements at ≈105 Hz.

Cross-Sectional TEM Analysis: For the preparation of cross-sectional samples, the Ag/WO_{3-x}/WSe_2/graphene structure was milled with a focused ion beam (FIB, FEI Helios NanoLab 450). Then, cross-sectional high-resolution transmission electron microscope (HR-TEM) images were obtained using a FEI Titan^3 G2 60-300 at the acceleration voltage of 80 kV to reduce electron beam damage. Energy-dispersive X-ray (EDX) spectroscopic imaging was performed by a SuperX EDX spectrometer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D materials, artificial synapse, barristor, heterostructure, memristor, neuromorphic application

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[1] C. Mead, *Proc. IEEE* **1990**, *78*, 1629.
[2] T. Hasegawa, K. Terabe, T. Tsuruoka, M. Aono, *Adv. Mater.* **2012**, *24*, 252.
[3] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, *8*, 13.
[4] D. Kuzum, S. Yu, H.-S. P. Wong, *Nanotechnology* **2013**, *24*, 382001.
[5] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, D. S. Modha, *Science* **2014**, *345*, 668.
[6] M. F. Bear, R. C. Malenka, *Curr. Opin. Neurobiol.* **1994**, *4*, 389.
[7] R. S. Zucker, W. G. Regehr, *Annu. Rev. Physiol.* **2002**, *64*, 355.
[8] L. F. Abbott, W. G. Regehr, *Nature* **2004**, *431*, 796.
[9] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[10] T. Berzina, A. Smerieri, M. Bernabò, A. Pucci, G. Ruggeri, V. Erokhin, M. P. Fontana, *J. Appl. Phys.* **2009**, *105*, 124515.
[11] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **2010**, *10*, 1297.
[12] F. Miao, J. P. Strachan, J. J. Yang, M.-X. Zhang, I. Goldfarb, A. C. Torrezan, P. Eschbach, R. D. Kelley, G. Medeiros-Ribeiro, R. S. Williams, *Adv. Mater.* **2011**, *23*, 5633.
[13] Z. Q. Wang, H. Y. Xu, X. H. Li, H. Yu, Y. C. Liu, X. J. Zhu, *Adv. Funct. Mater.* **2012**, *22*, 2759.
[14] A. M. Shen, C.-L. Chen, K. Kim, B. Cho, A. Tudor, Y. Chen, *ACS Nano* **2013**, *7*, 6117.
[15] A. A. Bessonov, M. N. Kirikova, D. I. Petukhov, M. Allen, T. Ryhänen, M. J. A. Bailey, *Nat. Mater.* **2015**, *14*, 199.
[16] G. W. Burr, R. M. Shelby, S. Sidler, C. Di Nolfo, J. Jang, I. Boybat, R. S. Shenoy, P. Narayanan, K. Virwani, E. U. Giacometti, *IEEE. Trans. Electron Devices* **2015**, *62*, 3498.
[17] V. K. Sangwan, D. Jariwala, I. S. Kim, K.-S. Chen, T. J. Marks, L. J. Lauhon, M. C. Hersam, *Nat. Nanotechnol.* **2015**, *10*, 403.
[18] W. Xu, S.-Y. Min, H. Hwang, T.-W. Lee, *Sci. Adv.* **2016**, *2*, e1501326.
[19] C. J. Wan, Y. H. Liu, P. Feng, W. Wang, L. Q. Zhu, Z. P. Liu, Y. Shi, Q. Wan, *Adv. Mater.* **2016**, *28*, 5878.
[20] H. Tian, Q. Guo, Y. Xie, H. Zhao, C. Li, J. J. Cha, F. Xia, H. Wang, *Adv. Mater.* **2016**, *28*, 4991.
[21] Y. v. d. Burgt, E. Lubberman, E. J. Fuller, S. T. Keene, G. C. Faria, S. Agarwal, M. J. Marinella, A. Alec Talin, A. Salleo, *Nat. Mater.* **2017**, *16*, 414.
[22] S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, S. Xavier, J. Tomas, L. Bellaiche, M. Bibes, A. Barthélémy, S. Saïghi, V. Garcia, *Nat. Commun.* **2017**, *8*, 14736.
[23] P. M. Sheridan, F. Cai, C. Du, W. Ma, Z. Zhang, W. D. Lu, *Nat. Nanotechnol.* **2017**, *12*, 784.
[24] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G.-L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.
[25] A. K. Geim, I. V. Grigorieva, *Nature* **2013**, *499*, 419.
[26] K. S. Novoselov, A. Mishchenko, A. Carvalho, A. H. Castro Neto, *Science* **2016**, *353*, aac9439.
[27] K. Qian, R. Y. Tay, M.-F. Lin, J. Chen, H. Li, J. Lin, J. Wang, G. Cai, V. C. Nguyen, E. H. T. Teo, T. Chen, P. S. Lee, *ACS Nano* **2017**, *11*, 1712.
[28] H. Tian, X. Cao, Y. Xie, X. Yan, A. Kostelec, D. DiMarzio, C. Chang, L.-D. Zhao, W. Wu, J. Tice, J. J. Cha, J. Guo, H. Wang, *ACS Nano* **2017**, *11*, 7156.
[29] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, K. Kim, *Science* **2012**, *336*, 1140.
[30] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, L. A. Ponomarenko, *Science* **2012**, *335*, 947.
[31] L. Britnell, R. M. Ribeiro, A. Eckmann, R. Jalil, B. D. Belle, A. Mishchenko, Y.-J. Kim, R. V. Gorbachev, T. Georgiou, S. V. Morozov, A. N. Grigorenko, A. K. Geim, C. Casiraghi, A. H. C. Neto, K. S. Novoselov, *Science* **2013**, *340*, 1311.
[32] W. J. Yu, Y. Liu, H. Zhou, A. Yin, Z. Li, Y. Huang, X. Duan, *Nat. Nanotechnol.* **2013**, *8*, 952.
[33] H. Fang, C. Battaglia, C. Carraro, S. Nemsak, B. Ozdol, J. S. Kang, H. A. Bechtel, S. B. Desai, F. Kronast, A. A. Unal, G. Conti, C. Conlon, G. K. Palsson, M. C. Martin, A. M. Minor, C. S. Fadley, E. Yablonovitch, R. Maboudian, A. Javey, *Proc. Natl. Acad. Sci. U. S. A.* **2014**, *111*, 6198.
[34] N. Huo, J. Kang, Z. Wei, S.-S. Li, J. Li, S.-H. Wei, *Adv. Funct. Mater.* **2014**, *24*, 7025.
[35] C.-H. Lee, G.-H. Lee, A. M. v. d. Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls, T. F. Heinz, J. Guo, J. Hone, P. Kim, *Nat. Nanotechnol.* **2014**, *9*, 676.
[36] X. Cui, G.-H. Lee, Y. D. Kim, G. Arefe, P. Y. Huang, C.-H. Lee, D. A. Chenet, X. Zhang, L. Wang, F. Ye, F. Pizzocchero, B. S. Jessen, K. Watanabe, T. Taniguchi, D. A. Muller, T. Low, P. Kim, J. Hone, *Nat. Nanotechnol.* **2015**, *10*, 534.
[37] T. Roy, M. Tosun, X. Cao, H. Fang, D.-H. Lien, P. Zhao, Y.-Z. Chen, Y.-L. Chueh, J. Guo, A. Javey, *ACS Nano* **2015**, *9*, 2071.
[38] J. Shim, H. S. Kim, Y. S. Shim, D.-H. Kang, H.-Y. Park, J. Lee, J. Jeon, S. J. Jung, Y. J. Song, W.-S. Jung, J. Lee, S. Park, J. Kim, S. Lee, Y.-H. Kim, J.-H. Park, *Adv. Mater.* **2016**, *28*, 5293.
[39] M. Yamamoto, S. Dutta, S. Aikawa, S. Nakaharai, K. Wakabayashi, M. S. Fuhrer, K. Ueno, K. Tsukagoshi, *Nano Lett.* **2015**, *15*, 2067.
[40] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat. Nanotechnol.* **2008**, *3*, 429.
[41] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, M.-J. Tsai, *Proc. IEEE* **2012**, *100*, 1951.
[42] Y. Li, S. Long, Q. Liu, H. Lv, M. Liu, *Small* **2017**, *13*, 1604306.
[43] R. Muenstermann, T. Menke, R. Dittmann, R. Waser, *Adv. Mater.* **2010**, *22*, 4819.
[44] R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.
[45] G. Perea, M. Navarrete, A. Araque, *Trends Neurosci.* **2009**, *32*, 421.
[46] C. Henneberger, T. Papouin, S. H. R. Oliet, D. A. Rusakov, *Nature* **2010**, *463*, 232.
[47] A. Suzuki, S. A. Stern, O. Bozdagi, G. W. Huntley, R. H. Walker, P. J. Magistretti, C. M. Alberini, *Cell* **2011**, *144*, 810.
[48] S. Valtcheva, L. Venance, *Nat. Commun.* **2016**, *7*, 13845.
[49] S. Kim, B. Choi, M. Lim, J. Yoon, J. Lee, H.-D. Kim, S.-J. Choi, *ACS Nano* **2017**, *11*, 2814.

