| **Both Platforms** |
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| Monolithic integration of light sources, detectors, memory devices, and electronics |
| At least 4 planes of photonic planes |
| Wafer-scale processing |
| Inter-wafer optical links |
| Demonstrate memory meeting requirements in section 4.1 |
| **Semiconductor Platform** |
| Demonstrate femtojoule optical receivers, ideally with low static power dissipation |
| III-V integration with electronics (1 million light sources/wafer) |
| Synapses and local plasticity mechanisms reach 10μm x 10μm |
| **Superconductor Platform** |
| *Either* III-V integration *or* cryogenic silicon light sources (1 million light sources/wafer) |
| Interface superconducting electronics with semiconductor light sources |
| Serial biasing or current-recycling schemes for current biasing of synapses and neurons |
| Demonstrate 8 planes of Josephson junctions per wafer |