#### Process sheet for **stf\_res\_01**

### Physics and Hardware for Intelligence project

Physical Measurement Laboratory, NIST Boulder

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#### Abstract

Fabrication flow for the SPD/JJ integration process. WSi SNSPDs are integrated with Nb/Si/Nb, externally shunted JJs. This process includes the superconducting thin-film layer and associated Nb wiring and Au resistors, a ground plane, the JJ tri-layer stack and associated PdAu shunt resistor layer, and an upper Nb wiring layer.

The process starts with a thermally oxidized Si wafer with 160 nm SiO<sub>2</sub>.

The entire wafer is clad with oxide, and openings are etched to the bond pads ( $\mathbf{v4}$ ). A Nb ground plane is deposited, and alignment marks are etched in this layer. Features are then etched in the ground plane ( $\mathbf{m0}$ ).

Insert screen shot of die and image distribution from stepper:

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# 1 Deposit M1 (lower Nb wiring)

- Begin with oxidized Si substrate
- $\bullet\,$  Deposit  $120\,\mathrm{nm}$  Nb with the Lesker SNS tool
- $\bullet$  Instructions for tool use: One Note/a4/fab/SNS
- Recipe: Nb\_wire\_js.rcp
- Rate: 80 nm/min; check log book for latest rate
- Insert picture of log book entry

### 2 PM (alignment marks)

• Expose:  $220 \,\mathrm{mJ/cm^2}$ 

 $\bullet\,$  Develop: double puddle,  $30\,\mathrm{s},\,30\,\mathrm{s}$ 

• Run through spin rinse dry

• Inspect with microscope

• Etch with Oxford fluorine ICP RIE

- Recipe: Nb PM He

 $* SF_6: 30 sccm$  \* RF: 25 W\* ICP: 800 W

\* Pressure:  $15\,\mathrm{mTorr}$ 

\* He: 5 Torr

- Etch: 70 s

- Typical DC bias:  $60\,\mathrm{V}$  @  $25\,\mathrm{W}$  RF

- No endpoint monitoring

• Ash:  $2 \min$ 

### 3 Pattern and Etch M1 (lower Nb wiring)

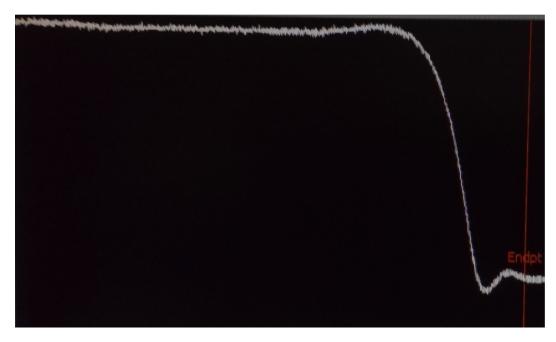


Figure 1: Typical endpoint signal of Nb etch. The small peak after the dip is interpreted as the end of the etch. Endpoint is called  $10 \, \text{s-} 20 \, \text{s}$  after that.

- Spin: SPR600 @ 3000 rpm
- Expose:  $220 \,\mathrm{mJ/cm^2}$
- Develop: double puddle, 30 s, 30 s
- Run through spin rinse dry
- Inspect with microscope
- Etch with PlasmaTherm
  - Recipe: 150mm\_Nb\_sloped\_ManEP
    - \* SF<sub>6</sub>:  $40 \operatorname{sccm}$
    - \* O<sub>2</sub>:  $16 \, sccm$
    - \* RF: cut after strikie
    - \* ICP: 500 W
    - \* Pressure: 6.5 mTorr
    - \* He: 4 Torr
    - \* Rate:  $\sim 0.51 \, \text{nm/s}$ ;  $\sim 31 \, \text{nm/min}$
    - \* Note: Selectivity over resist is poor; limit to 300 nm Nb to be etched
  - Etch:  $\sim 230 \,\mathrm{s}$
  - No DC bias
  - Use endpoint; typical signal shown in Fig. 1
  - Insert picture of endpoint signal and log book entry
- Ash: 2 min
- Clean: acetone dirty 2 min, acetone clean 2 min, IPA, spin rinse dry
- Inspect with microscope
- Measure thickness with profilometer

# 4 STF (superconducting thin film)

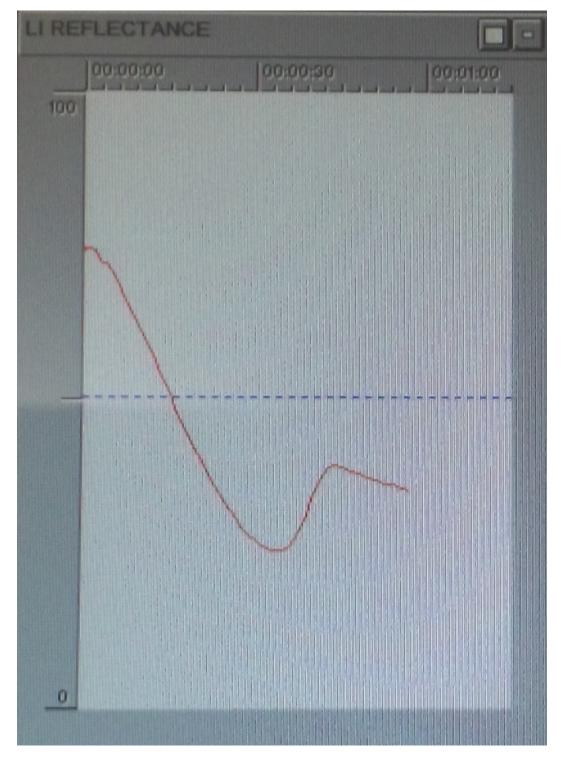


Figure 2: Typical endpoint signal of MoSi etch. The small peak after the dip is interpreted as the end of the etch. Overetch by 10 s- 20 s after that peak.

- Ash  $5 \min$
- Deposit MoSi in AJA

- Recipe: MoSi \_ jms
  - RF plasma clean for  $150\,\mathrm{s}$  at  $80\,\mathrm{W}$
  - Typical DC voltage:  $100\,\mathrm{V}$
  - Deposit MoSi:  $50\,\mathrm{s}$
  - Voltage:  $460\,\mathrm{V}$
  - Current: 440 mA
  - Deposit a-Si: 66 s
  - Voltage: 183 V

#### • Pattern

- Spin: SPR600 @  $3000\,\mathrm{rpm}$
- Expose:  $220 \,\mathrm{mJ/cm^2}$
- Develop: double puddle,  $30\,\mathrm{s}$ ,  $30\,\mathrm{s}$
- Run through spin rinse dry
- Inspect with microscope
- Etch with Oxford Fl
  - \* Recipe: opto-WSi-v2-lowHeForCarrier
    - $SF_6$ : 1 sccm
    - · Ar: 80 sccm
    - · RF: strike at 30 W, cut to 10 W as quickly as possible
    - · ICP: 600 W
    - Pressure: 10 mTorr
    - · He: 5 Torr
    - Rate:  $\sim 8 \, \text{nm/min}$
  - \* Etch:  $\sim 60 \,\mathrm{s}\text{-}70 \,\mathrm{s}$
  - \* DC bias: 67 V
  - \* Use endpoint; typical signal shown in Fig. ??
  - \* Insert picture of endpoint signal and log book entry
- Ash:  $2 \min$
- Clean: acetone dirty 2 min, acetone clean 2 min, IPA, spin rinse dry
- Inspect with microscope

#### 5 R1 (Au resistors)

- Pattern for liftoff
  - Ash: 3 min
  - Spin: LOR3A @  $2000\,\mathrm{rpm}$
  - Clean wafer backside if necessary with EBR
  - Bake:  $150\,^{\circ}$ C for  $5\,\mathrm{min}$
  - Spin: SPR660 @ 3000 rpm, no P20 (recipe: OPTO/3IN-SPR660-NO-3000-LOR IDI)
  - Expose:  $220 \,\mathrm{mJ/cm^2}$
  - Bake: 110°C
  - Develop: double puddle,  $30 \,\mathrm{s}$ ,  $30 \,\mathrm{s}$
  - Run through spin rinse dry
  - Inspect with microscope
- Deposit Au in Lesker Lab18
  - Load wafer in load lock
  - Pump down
  - Run Plasma clean from vacuum fast
  - Record DC voltage in log book (typical: 245 V)
  - Plasma clean runs in load lock
  - Transfer wafer to process chamber
  - Deposit: 4 nm Ti
  - Typical dep params: 0.2 nm/s; 78 mA
  - Deposit: 120 nm Au
  - Typical dep params: 1 nm/s; 58 mA
  - Deposit: 4 nm Ti
  - Transfer wafer to load lock
  - Vent load lock
  - Insert picture of log book entry
- Perform liftoff
  - Begin heating NMP (PG remover) to 150°C
  - Soak in acetone as long as possible
  - Transfer wafer to dirty acetone beaker
  - Sonicate in dirty for 5 min
  - Exchange acetone
  - Sonicate in dirty for 5 min
  - Exchange acetone
  - If all material is visibly lifted off, move to clean acetone beaker
  - If not, repeat until removed, but at least  $10\,\mathrm{min}$  sonics in dirty acetone with acetone exchange at  $5\,\mathrm{min}$
  - Sonicate in clean for 5 min
  - Spray wafer with acetone spray bottle into sink
  - Place wafer in hot NMP
  - Soak wafer in hot NMP for  $20\,\mathrm{min}$
  - Spray wafer with IPA into sink
  - Rinse wafer in beaker with IPA
  - Run through spin rinse dry

#### 6 R2 (PdAu resistors)

- Pattern for liftoff
  - Ash: 3 min
  - Spin: LOR3A @  $2000\,\mathrm{rpm}$
  - Clean wafer backside if necessary with EBR
  - Bake: 150 °C for 5 min
  - Spin: SPR660 @ 3000 rpm, no P20 (recipe: OPTO/3IN-SPR660-NO-3000-LOR IDI)
  - Expose:  $220 \,\mathrm{mJ/cm^2}$
  - Bake: 110°C
  - Develop: double puddle, 30 s, 30 s
  - Run through spin rinse dry
  - Inspect with microscope
- Deposit PdAu in Lesker Lab18
  - Load wafer in load lock
  - Pump down
  - Run Plasma clean from vacuum fast
  - Record DC voltage in log book (typical: 245 V)
  - Plasma clean runs in load lock
  - Transfer wafer to process chamber
  - Deposit: 4 nm Ti
  - Typical dep params:  $0.2\,\mathrm{nm/s}$ ;  $78\,\mathrm{mA}$
  - Deposit: 135 nm PdAu
  - Typical dep params: 1 nm/s; 79 mA
  - Deposit: 4 nm Ti
  - Transfer wafer to load lock
  - Vent load lock
  - Insert picture of log book entry
- Perform liftoff
  - Begin heating NMP (PG remover) to 150°C
  - Soak in acetone as long as possible
  - Transfer wafer to dirty acetone beaker
  - Sonicate in dirty for 5 min
  - Exchange acetone
  - Sonicate in dirty for 5 min
  - Exchange acetone
  - If all material is visibly lifted off, move to clean acetone beaker
  - If not, repeat until removed, but at least  $10\,\mathrm{min}$  sonics in dirty acetone with acetone exchange at  $5\,\mathrm{min}$
  - Sonicate in clean for 5 min
  - Spray wafer with acetone spray bottle into sink
  - Place wafer in hot NMP
  - Soak wafer in hot NMP for  $20\,\mathrm{min}$
  - Spray wafer with IPA into sink
  - Rinse wafer in beaker with IPA
  - Run through spin rinse dry