Process sheet for **vt02**

Physics and Hardware for Intelligence project

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Abstract

Fabrication flow for the SPD/JJ integration process. WSi SNSPDs are integrated with Nb/Si/Nb, externally shunted JJs. This process includes the superconducting thin-film layer and associated Nb wiring and Au resistors, a ground plane, the JJ tri-layer stack and associated PdAu shunt resistor layer, and an upper Nb wiring layer.

The process starts with a thermally oxidized Si wafer with 160 nm SiO_2.

The entire wafer is clad with oxide, and openings are etched to the bond pads (**v4**). A Nb ground plane is deposited, and alignment marks are etched in this layer. Features are then etched in the ground plane (**m0**).

Insert screen shot of die and image distribution from stepper:

Contents

1 Alignment Marks

A

2 M1 (lower Nb wiring)

M1

3 STF (superconducting thin film)

STF

4 R1 (Au resistors)

R1

5 I1 (first insulator layer)

I1

6 V1 (via from M1 to M2)

V1

7 M2 (Nb ground plane)

M2

8 I2 (second insulator layer)

I2

9 V2 (via from M2 to JJ1)

V2

10 Tri-layer dep

Tri

11 JJ2 (etch upper JJ layer)

JJ2

12 JJ1 (etch lower JJ layer)

JJ1

13 I3 (third insulator layer)

I3

14 V3 (via from JJ1/JJ2 to M3)

V3

15 M3 (upper Nb wiring)

M3

16 R2 (Au resistors)

R2

17 I4 (fourth insulator layer)

I4

18 V4 (via to R2/pad opening)

V4

19 PKG (SU8 fiber collars/glue boxes)

PKG