Process sheet for **vt01**

Physics and Hardware for Intelligence project

Physical Measurement Laboratory, NIST Boulder

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Process overview: Fabrication flow for the Nb/Si/Nb, externally shunted JJ process. This process includes a ground plane, JJ tri-layer, upper Nb wiring layer, and PdAu resistors.

The process starts with a thermally oxidized Si wafer with 160 nm SiO_2.

The entire wafer is clad with oxide, and openings are etched to the bond pads (**v4**). A Nb ground plane is deposited, and alignment marks are etched in this layer. Features are then etched in the ground plane (**m0**).

Insert screen shot of die and image distribution from stepper:

Step 1: Etched alignment marks for ebeam and stepper (global ebeam, local ebeam, and ASML)

GDS layer(s): none/shared marks reticle

Step 2: Clean wafer and deposit protective SiO_2 for implants and anneal

GDS layer(s): none/full wafer Insert endpoint signal and logbook screenshots here.

Step 26: Dice wafer

GDS layer(s): none / full wafer Additional notes: Insert microscope screen shots if desired.