電路實驗報告

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Part 1.

一、 Verilog Code

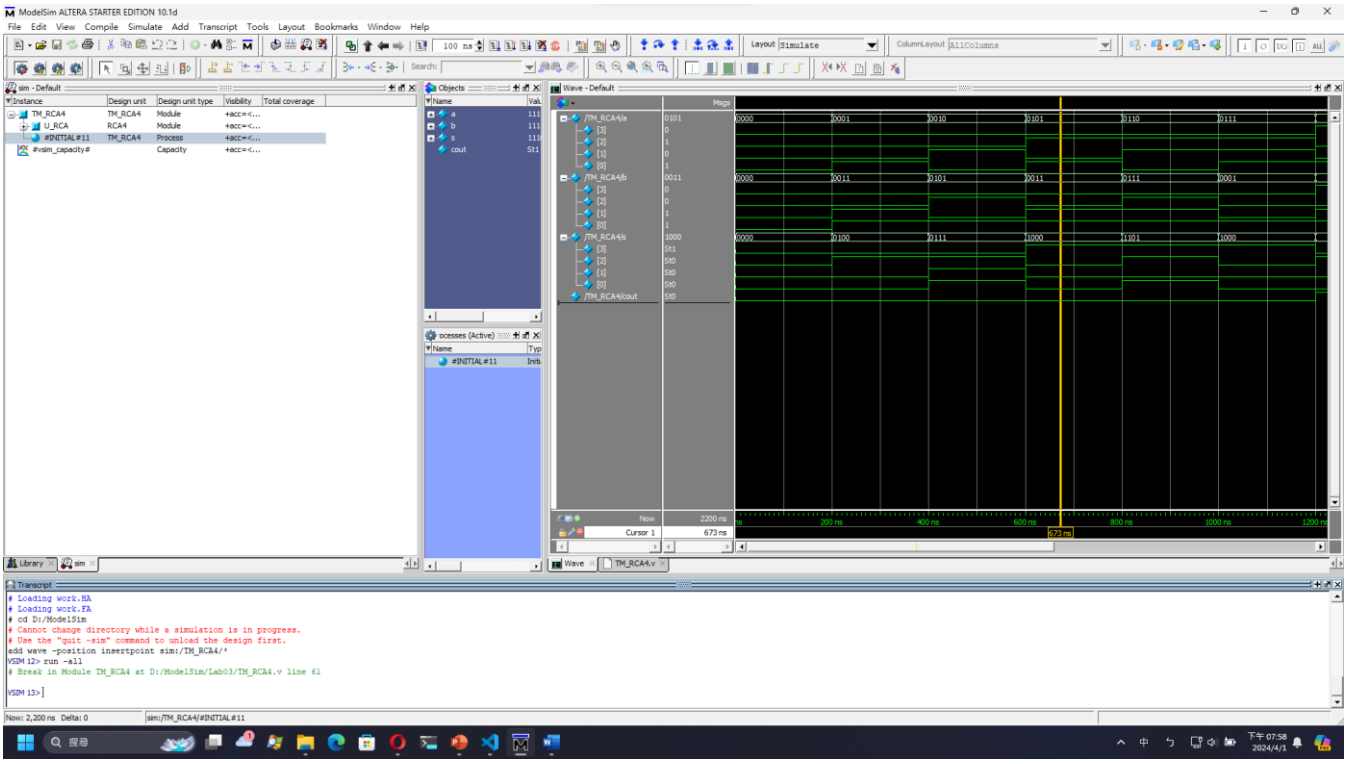
FA.v

```
`timescale  1ns/1ns

module FA(a, b, c, cout, sum);

input a, b, c;

output cout, sum;

assign sum = a ^ b ^ c;

assign cout = (a & b) | ((a ^ b) & c);

endmodule
```

HA.v

```
`timescale 1ns/1ns

module HA(a, b, sum, cout);

input a, b;

output sum, cout;

assign sum = a ^ b;

assign cout = a & b;

endmodule
```

二、 結果



根據模擬結果，表格如下：

被加（減）數 A				加（減）數 B				末端進位	和			
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_4	S_3	S_2	S_1	S_0
0	0	0	1	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	0	1	0	0	1	1	1
0	1	0	1	0	0	1	1	0	1	0	0	0
0	1	1	0	0	1	1	1	0	1	1	0	1
0	1	1	1	0	0	0	1	0	1	0	0	0
1	0	0	1	1	0	1	1	1	0	1	0	0

1	0	0	0	1	1	0	1	1	0	1	0	1
1	0	1	0	1	0	0	1	1	0	0	1	1
1	0	1	1	1	1	0	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0

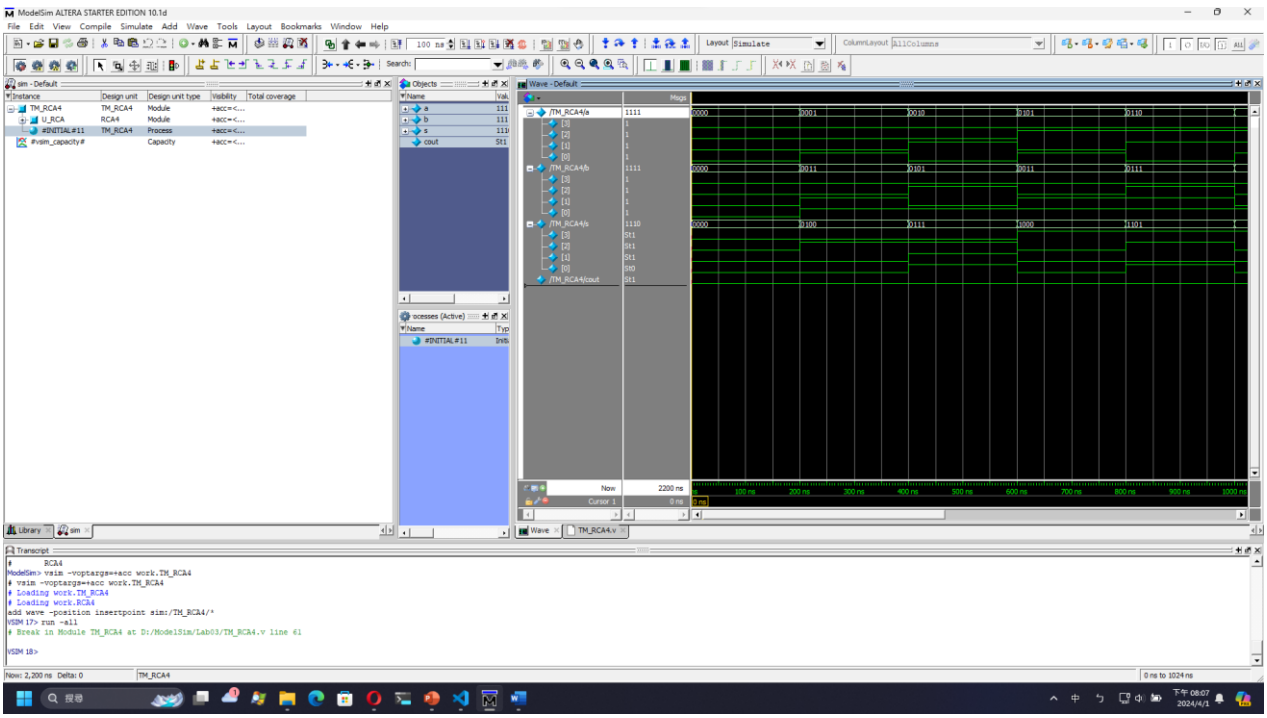
經數學計算後進行比對，結果正確。

Part 2.

一、 Verilog Code

```
`timescale 1ns/1ns
module RCA4(a, b, cout, s);
input [3:0] a, b;
output [3:0] s;
output cout;
wire [4:0] at, bt, st;
assign at = {1'b0, a};
assign bt = {1'b0, b};
assign st = at + bt;
assign s = st[3:0];
assign cout = st[4];
endmodule
```

二、 結果


ModelSim ALTERA STARTER EDITION 10.1d
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Wave - Default
Transcript
RCA4
ModelSim> vsim -voptargs=+acc work.TM_RCA4
vsim -voptargs=+acc work.TM_RCA4
Loading work.TM_RCA4
Loading work.RCA4
add wave -position insertpoint sim:/TM_RCA4/*
VSIM 17> run -all
Break in Module TM_RCA4 at D:/ModelSim/Lab03/TM_RCA4.v line 61
VSIM 18>