電路實驗報告

資工二甲

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一、 Verilog Code

FA.v

```
`timescale  1ns/1ns


module FA(a, b, c, cout, sum);


input a, b, c;
output cout, sum;


wire e1, e2, e3;


xor(e1, a, b);
and(e2, a, b);
and(e3, e1, c);
or(cout, e2, e3);
xor(sum, e1, c);


endmodule
```

HA.v

```
`timescale 1ns/1ns

module HA(a, b, sum, cout);

input a, b;
output sum, cout;

xor(sum, a, b);

and(cout, a, b);

endmodule
```

RCA4.v

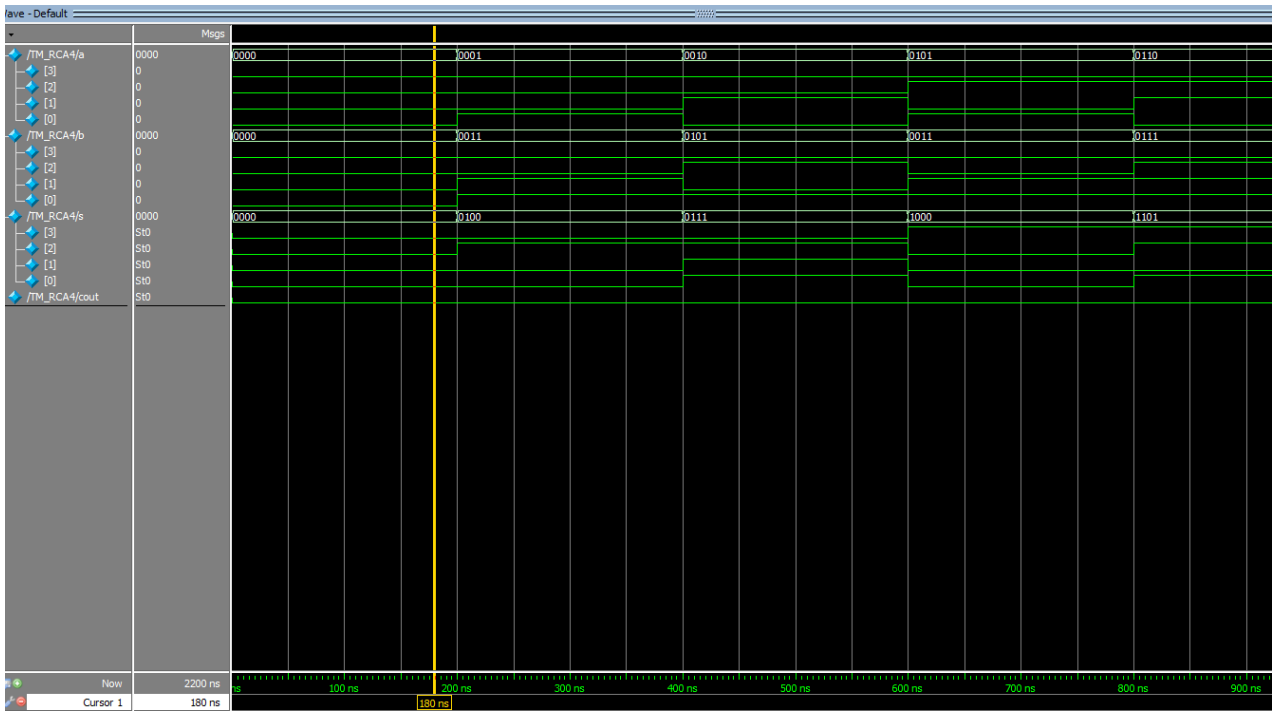
```
`timescale 1ns/1ns

module RCA4(a, b, cout, s);

input [3:0] a, b;
output [3:0] s;
output cout;

wire [3:0] c;

HA tha0(.a(a[0]), .b(b[0]), .sum(s[0]), .cout(c[0]));
FA tfa1(.a(a[1]), .b(b[1]), .c(c[0]), .sum(s[1]), .cout(c[1]));

FA tfa2(.a(a[2]), .b(b[2]), .c(c[1]), .sum(s[2]), .cout(c[2]));

FA tfa3(.a(a[3]), .b(b[3]), .c(c[2]), .sum(s[3]), .cout(c[3]));

assign cout = c[3];

endmodule
```

TM_RCA4.v

```
`timescale 1ns/1ns

module TM_RCA4;

reg [3:0] a, b;
wire [3:0] s;
wire cout;

RCA4 U_RCA (.a(a), .b(b), .s(s), .cout(cout));

initial begin

    a = 4'd0;
    b = 4'd0;
    // #200
    // a = 4'd10; // 1010
    // b = 4'd5; // 0101



    #200
    a = 4'd1; // 0001
    b = 4'd3; // 0011

    #200
    a = 4'd2; // 0010
    b = 4'd5; // 0101

    #200
    a = 4'd5; // 0101
    b = 4'd3; // 0111

    #200
    a = 4'd6; // 0110
    b = 4'd7; // 0111

    #200
```

```
    a = 4'd7;
    b = 4'd1;

    #200
    a = 4'd9;
    b = 4'd11;

    #200
    a = 4'd8;
    b = 4'd13;

    #200
    a = 4'd10;
    b = 4'd9;

    #200
    a = 4'd11;
    b = 4'd13;

    #200
    a = 4'd15;
    b = 4'd15;

    #200
    $stop;
end

endmodule
```

二、 結果



根據模擬結果，表格如下：

被加（減）數 A				加（減）數 B				末端進位	和			
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_4	S_3	S_2	S_1	S_0
0	0	0	1	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	0	1	0	0	1	1	1
0	1	0	1	0	0	1	1	0	1	0	0	0
0	1	1	0	0	1	1	1	0	1	1	0	1
0	1	1	1	0	0	0	1	0	1	0	0	0
1	0	0	1	1	0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	1	1	0	1	0	1

1	0	1	0	1	0	0	1	1	0	0	1	1
1	0	1	1	1	1	0	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0

經數學計算後進行比對，結果正確。

三、 心得

黃乙家：做完這次實驗後我對 Verilog 這個硬體描述語言有了初步的了解，也學會如何使用 ModelSim 模擬四位元加法器。希望之後如果有需要自己開發電路時能夠順利解決問題與需求。

梁凱哲：這個實驗相比上周的二位元加法器複雜了不少，還是被之前寫 C 的思路影響導致修改嘞很多次還是有問題，完成這個實驗後更加了解 modelsim 的寫法，之後的實作會更加順利。