**電路實驗報告**

**資工二甲**

**11127137 黃乙家**

1. Verilog Code
2. 結果

|  |  |  |  |
| --- | --- | --- | --- |
| 被加（減）數 A | 加（減）數 B | 末端進位 | 和 |
|  |  |  |  |
| 0 0 0 1 | 0 0 1 1 | 0 | 0 1 0 0 |
| 0 0 1 0 | 0 1 0 1 | 0 | 0 1 1 1 |
| 0 1 0 1 | 0 0 1 1 | 0 | 1 0 0 0 |
| 0 1 1 0 | 0 1 1 1 | 0 | 1 1 0 1 |
| 0 1 1 1 | 0 0 0 1 | 0 | 1 0 0 0 |
| 1 0 0 1 | 1 0 1 1 | 1 | 0 1 0 0 |
| 1 0 0 0 | 1 1 0 1 | 1 | 0 1 0 1 |
| 1 0 1 0 | 1 0 0 1 | 1 | 0 0 1 1 |
| 1 0 1 1 | 1 1 0 1 | 1 | 1 0 0 0 |
| 1 1 1 1 | 1 1 1 1 | 1 | 1 1 1 0 |

1. 心得