GÖPEL electronic GmbH

Customer name:

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Parameter-Checklist for Automotive Video Projects

Please fill in the table as detailed as possible and send it to ats.sales@goepel.com:

General Information				
	Technical contact person (with e-mail address):			
	Project title:			
	Expected use case (What is the application like?):			
Technical basics	Planned quantity of hardware:			
	Desired test hardware format:	Box (GigE)	PCIe Card*	PXIe Card*
ech	Number of Video inputs on UUT:			
	Number of Video outputs on UUT:			
	Please fill in a new table	block for each input/	output:	
	UUT Video IN/OUT 1			
	☐ Input	Output		
ion	Source/ Sink IC (de-/serializer type) of UUT			
Hardware Information	Video connector type (Coax (Fakra), STP, etc.) and vendor ID:			
	Pinning of video connector:			
	Power supply of UUT via video cable? If Yes - voltage and current consumption:	Yes	☐ No	
	Pixel clock:			
ters	Image width:			
ame	Image height:			
Video Parameters	Frame rate:			
	HorizontalSyncPolarity:	High	Low	
	VerticalSyncPolarity:	High	Low	
	DataEnablePolarity:	High	Low	

Directors
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Local court Jena, HR B 20 1550 VAT ID no DE 150520615 WEEE reg no DE 887416033 Bank information

Commerzbank Filiale Jena BIN 820 400 00

Account no 2581 833 SWIFT COBA DE FF 821 IBAN DE57 8204 0000 0258 1833 00

Sparkasse Jena
BIN 830 530 30
Account no 260 525
SWIFT HELA DEF 1 JEN
IBAN DE24 8305 3030 0000 2605 25





Video Parameters	PixelClockPolarity:	High	Low
	LockOutputEnable:	High	Low
	LockPolarity:	High	Low
	Video format (RGB888, YUV422, RAW12, etc.):		
	Number of video channels per stream:		
	Is HDCP used?	Yes	No
Sideband Communication	I ² C:	Yes	No
	UART:	Yes	No
	SPI:	Yes	No
	MII:	Yes	No
iši	CAN:	Yes	No
	Texas Instruments Chip		
L	FPD Link:	FPD Link I FF	PD Link II FPD Link III
natik	Backward compatible mode:	Yes	No
forn	Low frequency mode:	Yes	No
ıt In	FPD Link III Transfer Mode:	Single Lane	Dual Lane
nder	APIX Chip	J	
Chip dependent Information	APIX version:	APIX I AF	PIX II APIX III
jb d	Maxim Chip		'
Chi	GMSL version:	GMSL I GI	MSL II GMSL III
	Bus width/ Bus mode:	24 bit 32	2 bit 64 bit
	UUT Video IN/OUT 2		
	Input	Output	
Ē	Source/ Sink IC (de-/serializer type) of UUT:		
mation	Video connector type (Coax (Fakra), STP, etc.) and		
	vendor ID:		
e Inf	Pinning of video connector:		
ware			
Hardware Infor			
	Davida ankla		
	Power supply of UUT via video cable? If Yes - voltage and current consumption:	Yes	No
	Pixel clock:		
ers	Image width:		
Video Parameters	Image height:		
	Frame rate:		
	HorizontalSyncPolarity:	High	Low
	VerticalSyncPolarity:	High	Low
	DataEnablePolarity:	High	Low



Video Parameters	PixelClockPolarity:	High	Low	
	LockOutputEnable:	High	Low	
	LockPolarity:	High	Low	
	Video format (RGB888, YUV422, RAW12, etc.):			
	Number of video channels per stream:			
	Is HDCP used?	Yes	No	
Sideband Communication	I ² C:	Yes	No	
	UART:	Yes	No	
	SPI:	Yes	No	
	MII:	Yes	No	
iši	CAN:	Yes	No	
	Texas Instruments Chip			
L	FPD Link:	FPD Link I FF	PD Link II FPD Link III	
natik	Backward compatible mode:	Yes	No	
forn	Low frequency mode:	Yes	□ No	
ıt In	FPD Link III Transfer Mode	Single Lane	Dual Lane	
nder	APIX Chip			
Chip dependent Information	APIX version:	APIX I AI	PIX II APIX III	
jb d	Maxim Chip		<u>'</u>	
Chi	GMSL version:	GMSLI G	MSL II GMSL III	
	Bus width/ Bus mode:	24 bit 32	2 bit 64 bit	
	UUT Video IN/OUT 3			
	Input	Output		
Ē	Source/ Sink IC (de-/serializer type) of UUT:			
mation	Video connector type (Coax (Fakra), STP, etc.) and			
	vendor ID:			
e Inf	Pinning of video connector:			
ware				
Hardware Infor				
	Deves ever by af IIIIT via vide a pakin?			
	Power supply of UUT via video cable? If Yes - voltage and current consumption:	Yes	No	
	Pixel clock:			
ers	Image width:			
Video Parameters	Image height:			
	Frame rate:			
	HorizontalSyncPolarity:	High	Low	
	VerticalSyncPolarity:	High	Low	
	DataEnablePolarity:	High	Low	



Video Parameters	PixelClockPolarity:	High	Low	Low	
	LockOutputEnable:	High	Low		
	LockPolarity:	High	Low		
	Video format (RGB888, YUV422, RAW12, etc.):				
	Number of video channels per stream:				
	Is HDCP used?	Yes	□ No		
Sideband Communication	l ² C:	Yes	☐ No	No	
	UART:	Yes	☐ No	No	
	SPI:	Yes	☐ No	No	
	MII:	Yes	☐ No	No	
	CAN:	Yes	☐ No		
	Texas Instruments Chip				
on	FPD Link:	FPD Link I	FPD Link II	FPD Link III	
nati	Backward compatible mode:	Yes	☐ No		
ıforr	Low frequency mode:	Yes	☐ No		
nt Ir	FPD Link III Transfer Mode:	Single Lane	Dual	Lane	
nde	APIX Chip				
Chip dependent Information	APIX version:	APIX I	APIX II	APIX III	
b di	Maxim Chip				
ਨ	GMSL version:	GMSLI	GMSL II	GMSL III	
	Bus width/ Bus mode:	24 bit	32 bit	64 bit	
Any other Business	Are you interested in the Dragon Suite Advanced software? **	Yes	□ No		
	Do you need start-up support? ***	Yes	☐ No		
	Remarks:				

Some parameters are not supported by all our video devices. Please be not confused when unnecessary information is requested for your project. Please give us as much information as possible about your project. Only in this way we can create an offer that fits your application.

Please add a detailed schematic of your application to the checklist.

- * Only available for Series 62 (Video Dragon 2)
- ** The **Dragon Suite** software is provided free of charge to our customers to help them work with their Göpel video devices. This includes configuring the device, generating and capturing images and videos, sideband communication as well as various IO and CAN functions.

In addition, the tool offers additional features that are available as a paid **Dragon Suite Advanced** (such as Script Interface and Raw Data Recording) and are constantly being further developed. If you have any additional expansion requests, please contact our support team (ats.support@goepel.com).

*** We are delighted to support our customers in the start-up and development of their applications. In case of increased effort, we will offer you a fee-based support.