EECS 281, March 9, 2015

Sequential logic circuit: outputs depend on current and past inputs

State: collection of state variables whose values at any one time contain all the information about the past necessary to determine the future behavior.

In digital logic circuit: state variables are binary values corresponding to certain logic signals.

n binary state variables $\longrightarrow$ 2^n possible states

2^n: always finite $\Rightarrow$ finite-state machines.

Clock signal: active high if state changes occur at rising edge.

Clock tick: first edge or pulse in clock period, or period itself.

Duty cycle: percentage of time clock @ its asserted level.

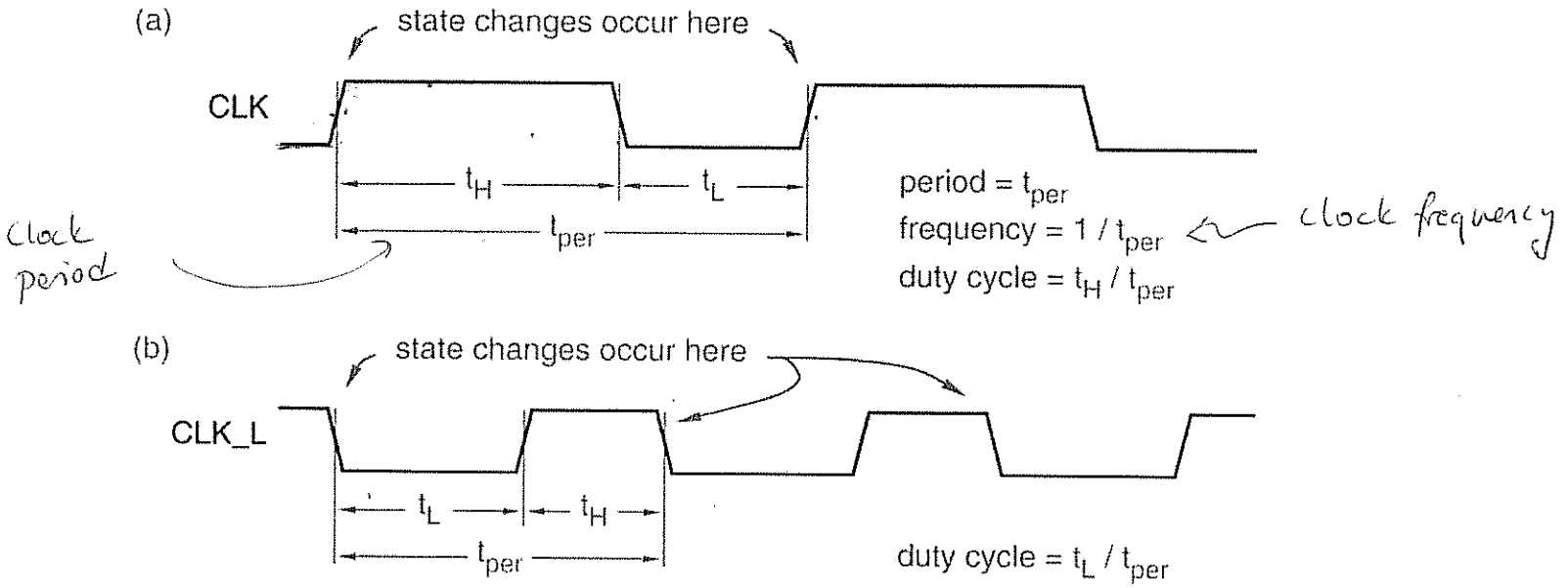
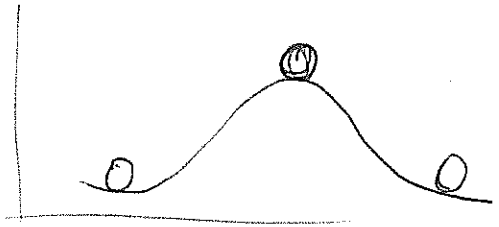
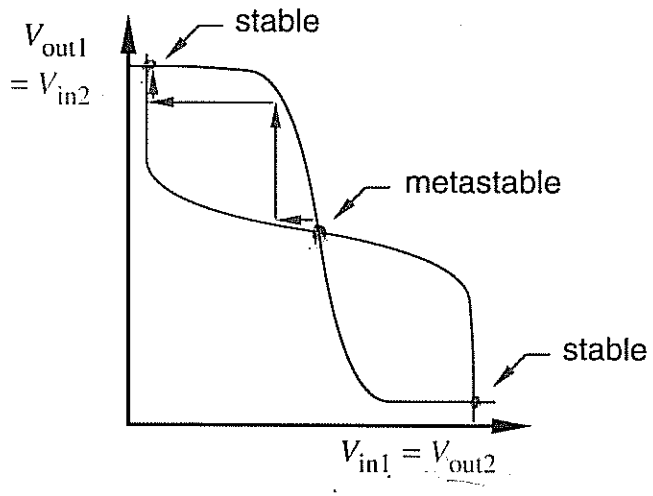


Figure 7-1

Clock signals: (a) active high; (b) active low.





Transfer function:

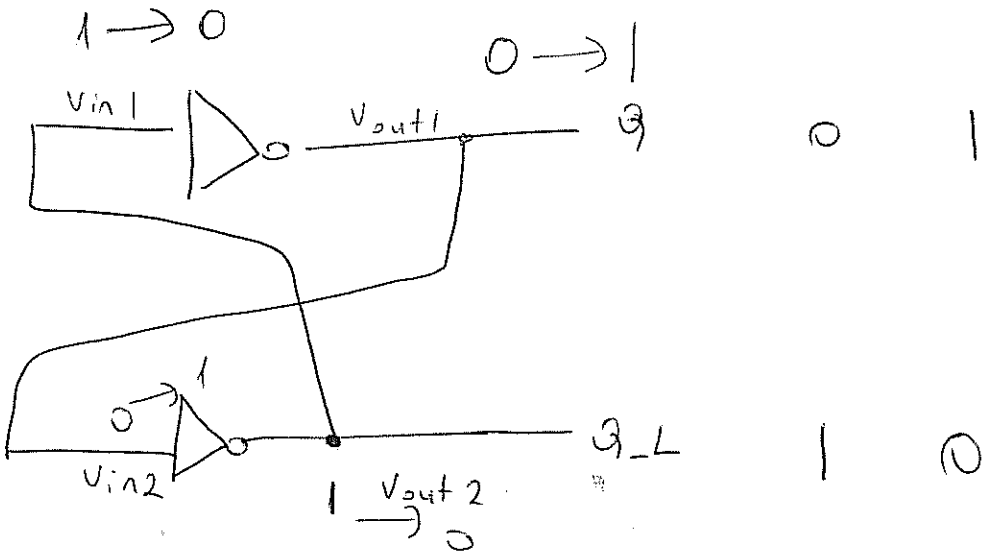
$V_{out1} = T(V_{in1})$

$V_{out2} = T(V_{in2})$

Figure 7-3

Transfer functions for inverters in a bistable feedback loop.

Bistable element

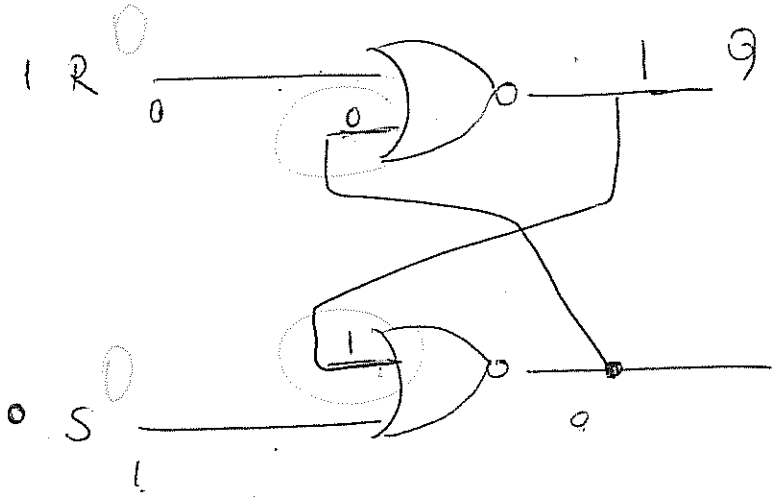


Latches: watch inputs continuously, can change output at any time.

Flip-flops: ~~watch inputs continuously~~, ~~catch~~ change outputs with clock change only.

S-R Latch

(set - reset)



↳ normally complement of Q

S	R	Q	QN
0	0	Last Q	Last QN
0	1	0	1
1	0	1	0
1	1	0	0

If pulse-width < minimum-pulse-width (from specs) ⇒ may go into metastable state.

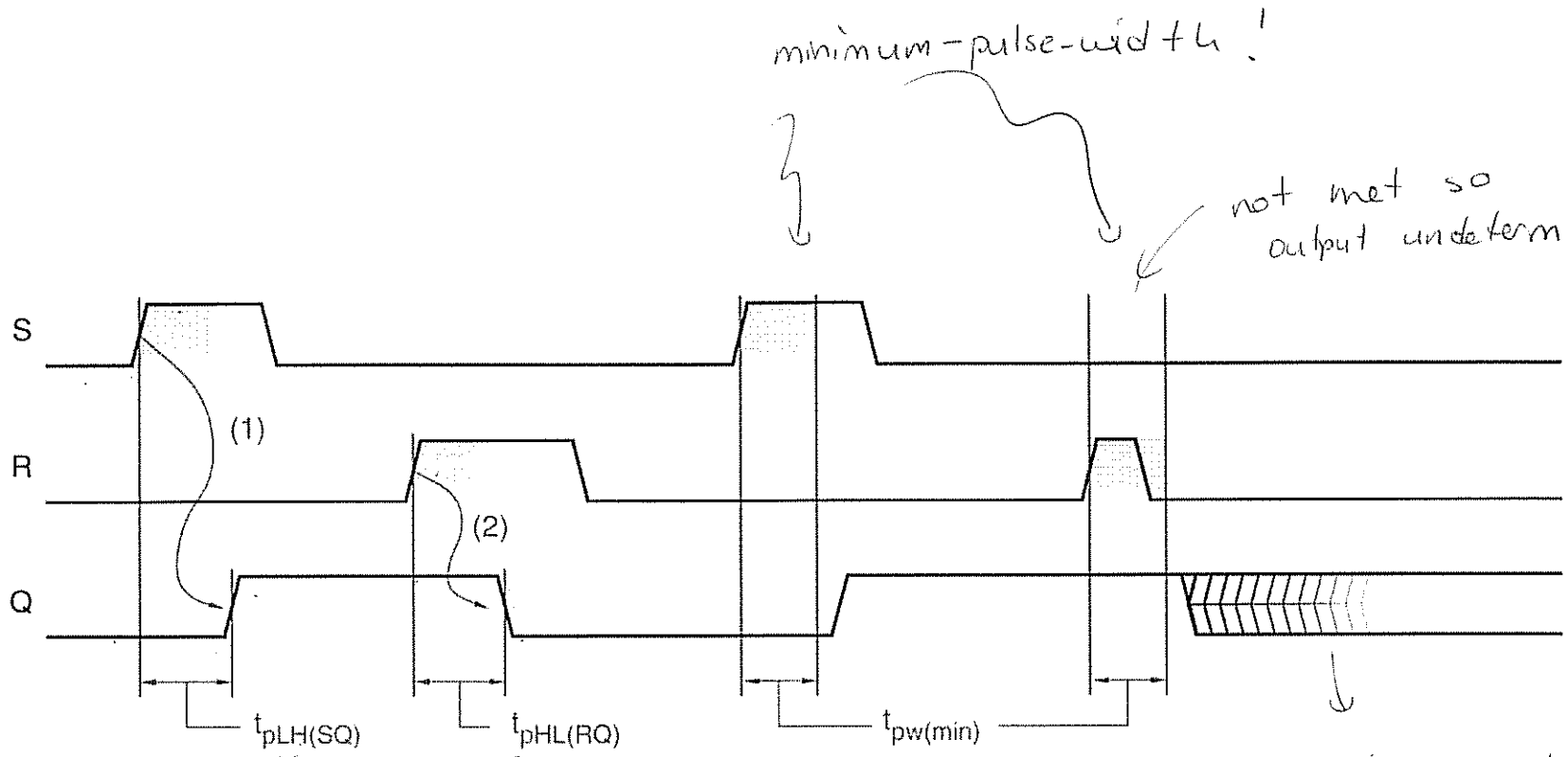


Figure 7-8

Timing parameters for an S-R latch.

S R
1 1 → 0 0

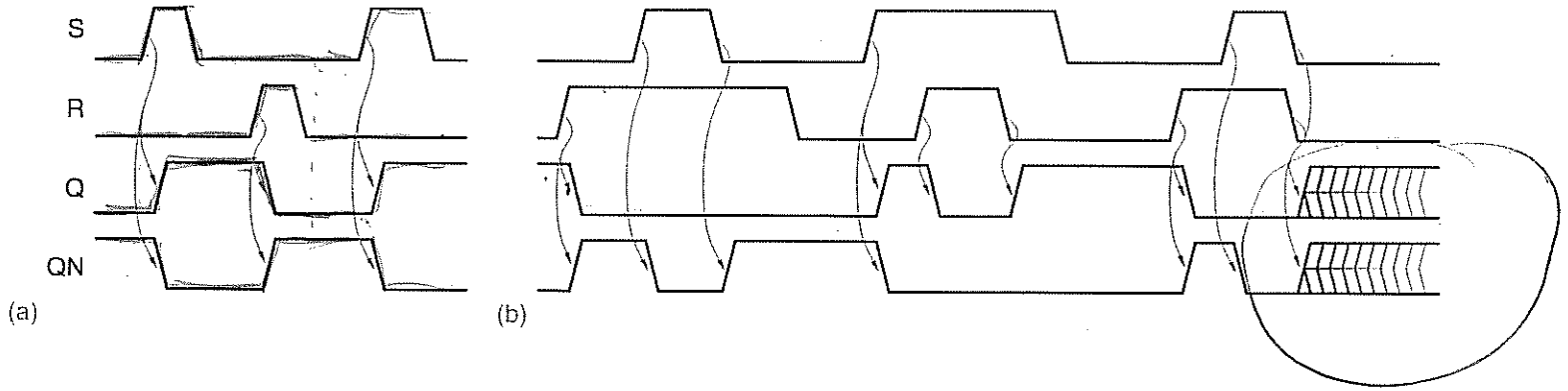
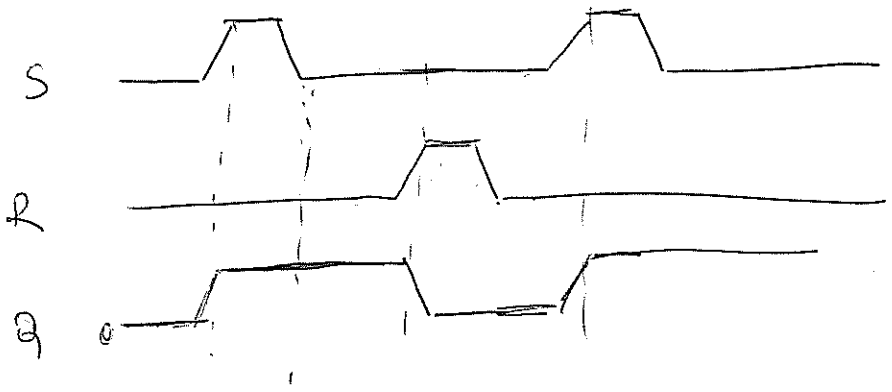


Figure 7-6

Typical operation of an S-R latch: (a) "normal" inputs; (b) S and R asserted simultaneously.

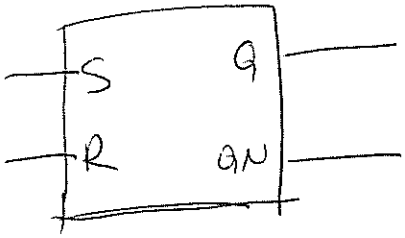
output undefined / undetermined

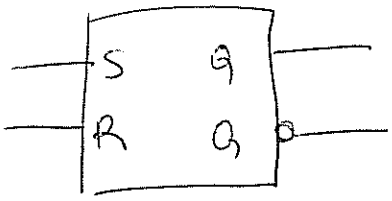


when both S = R = 1 ⇒ both outputs are forced to be 0.

once either input is negated ⇒ complementary operation

If both negated simultaneously ⇒
unpredictable next state ⇒ may oscillate, or may end up at a nonlogic level.

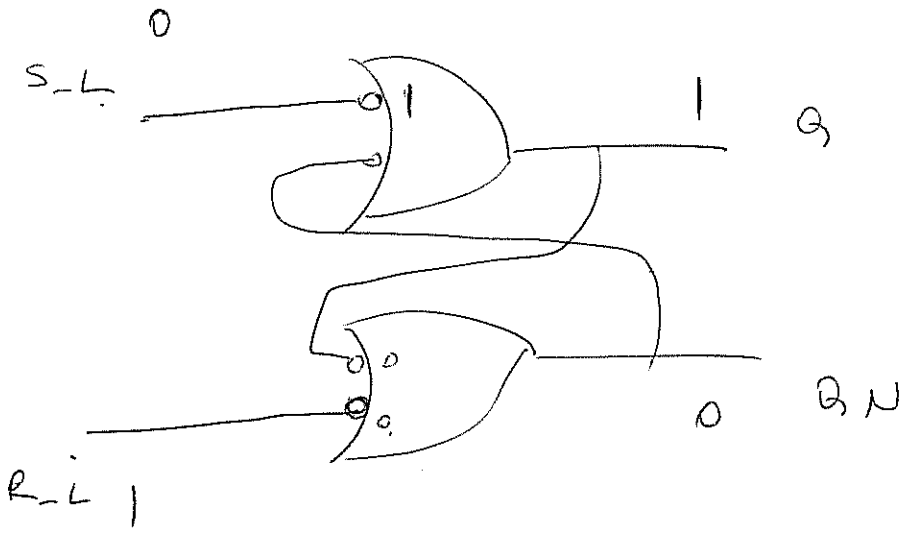




$\overline{S}$ - $\overline{R}$ Latch

Active low set and reset inputs

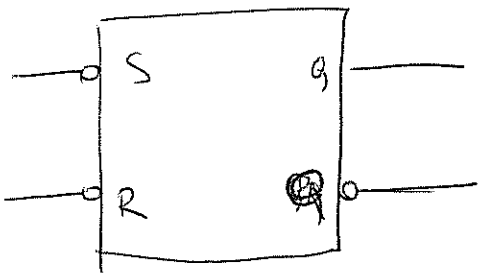
More often used because uses NAND gates.



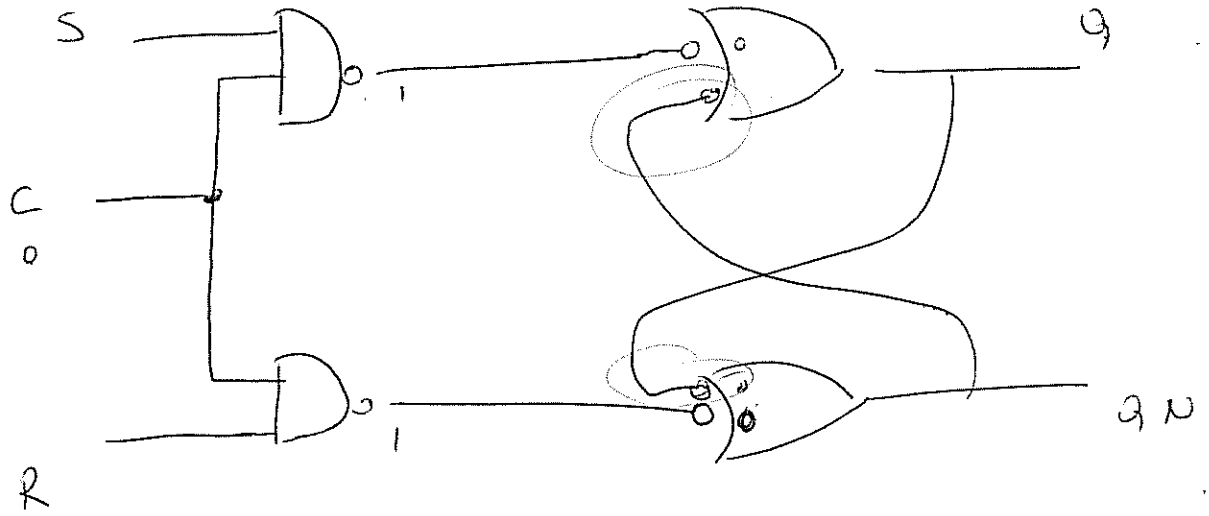
S_L	R_L	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Last Q	Last QN

Remembers previous state when $\bar{S} = \bar{R} = 1$

Both outputs are 1 when $\bar{S} = \bar{R} = 0$



S-R latch with Enable



S	R	C	Q	QN
X	X	0	Last Q	Last QN
0	0	1	last Q	Last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1

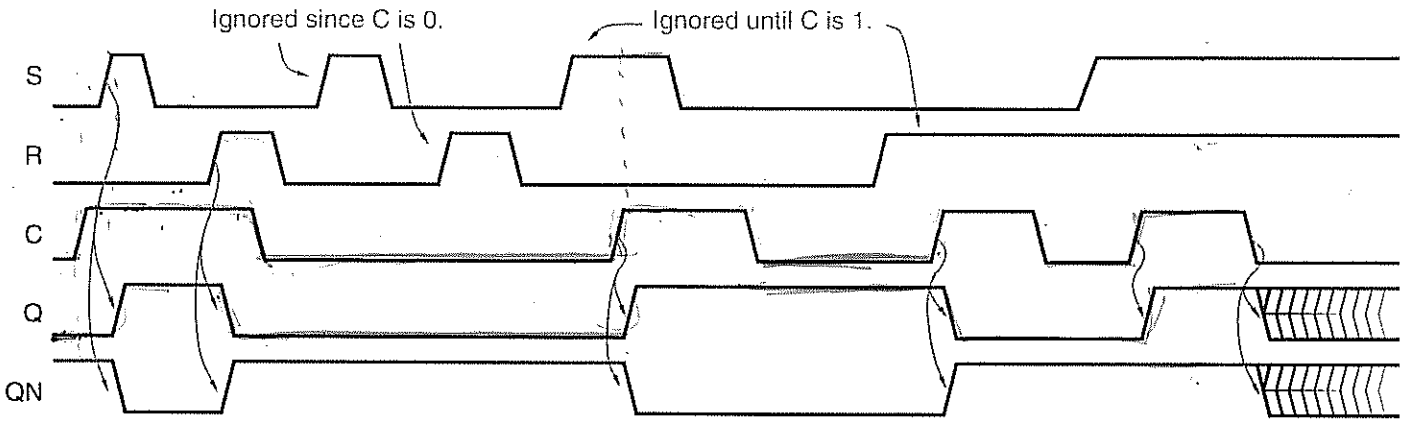


Figure 7-11

Typical operation of an S-R latch with enable.