

EECS 281, February 26, 2015

Multiplexer: digital switch, connects data

from one of  $n$  sources to its output.

$n$  sources of data, each  $b$  bits wide.

$b$  output bits.

commercially available:  $n = 1, 2, 4, 8, 16$

$b = 1, 2, 4$

$s$  inputs that select among  $n$  sources.

$$n = 2^s$$

$$s = \log_2 n$$

EN : enable input .  $EN = 0 \Rightarrow$  all outputs are 0.

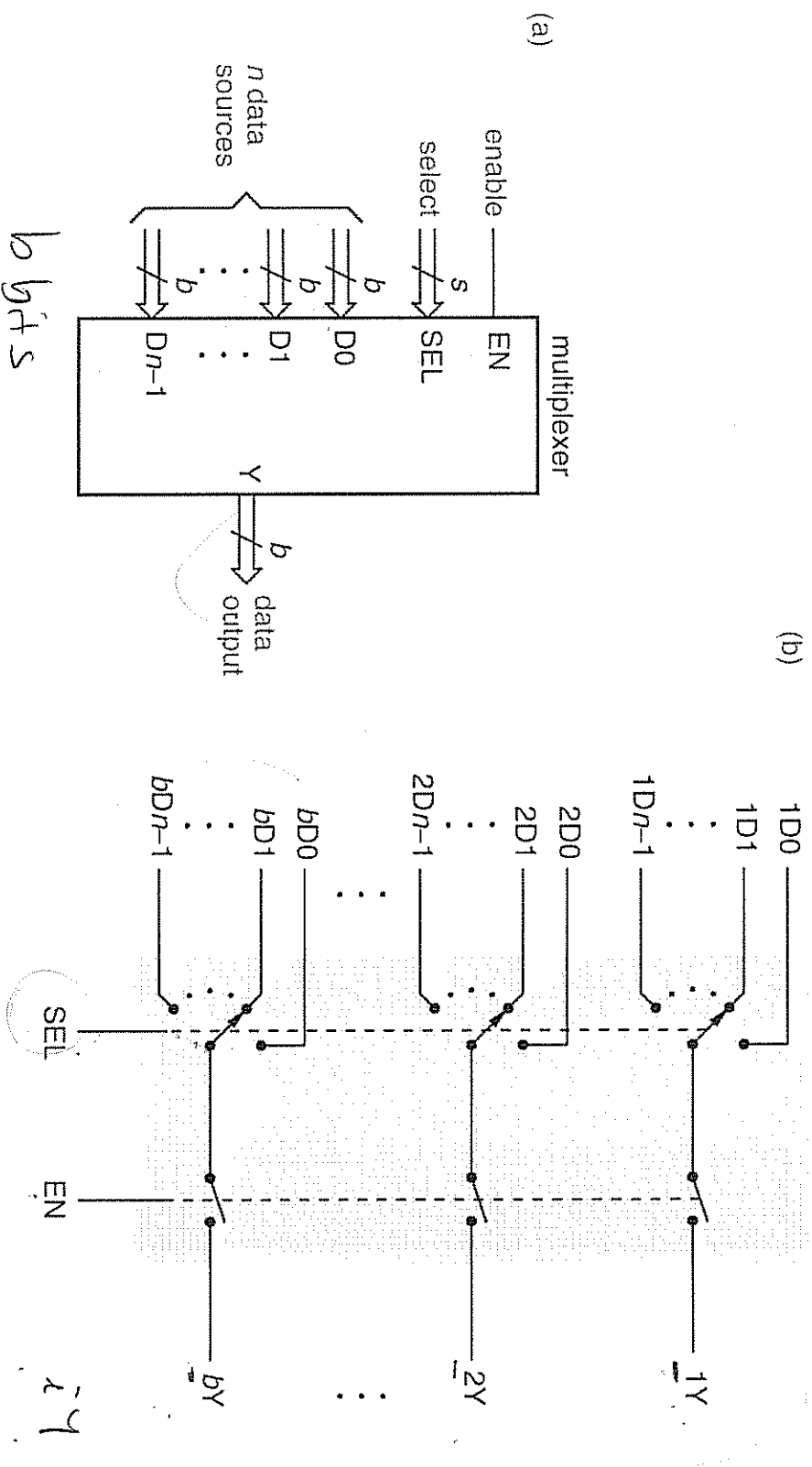
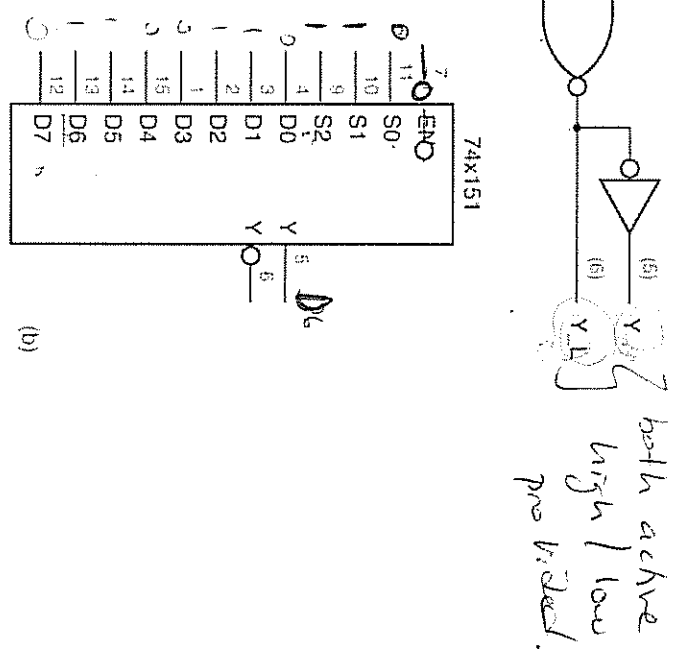
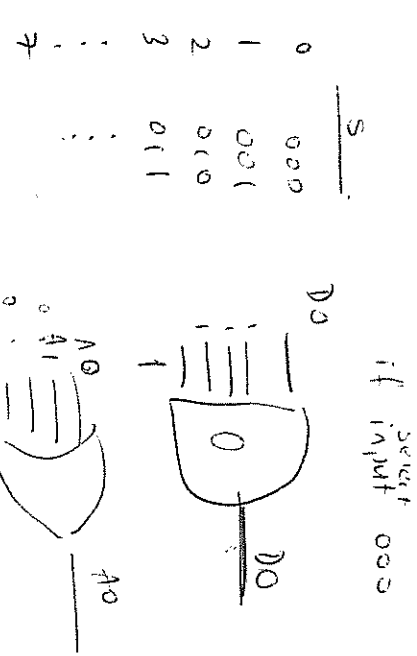
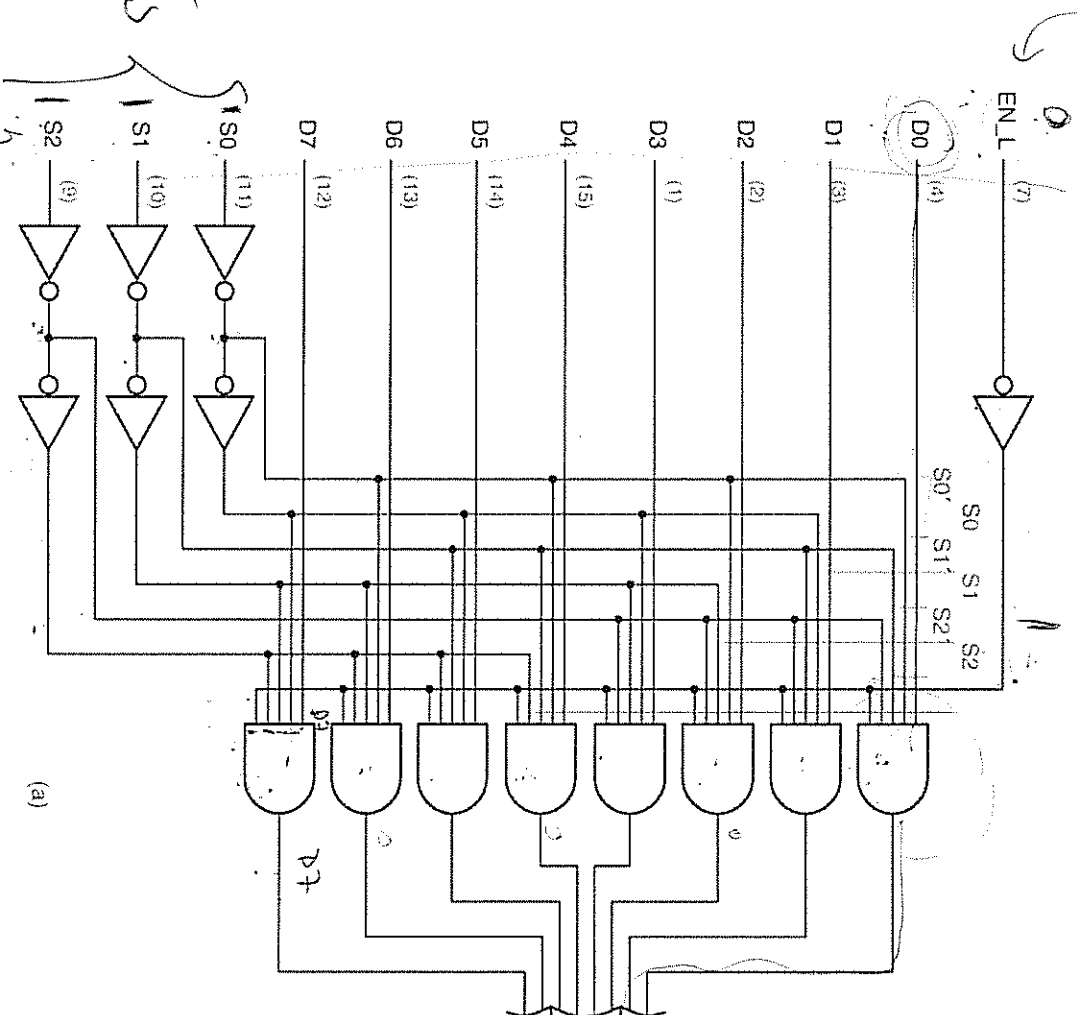


Figure 6-59

Multiplexer structure: (a) inputs and outputs; (b) functional equivalent.

enable input: active low



most significant select inputs

Figure 6-60

The 74x151 8-input, 1-bit multiplexer: (a) logic diagram; (b) traditional logic symbol.

Inputs				Outputs	
EN_L	S2	S1	S0	Y	Y_L
1	x	x	x	0	1
0	0	0	0	<u>D0</u>	<u>D0'</u>
0	0	0	1	D1	D1'
0	0	1	0	D2	D2'
0	0	1	1	D3	D3'
0	1	0	0	<u>D4</u>	<u>D4'</u>
0	1	0	1	D5	D5'
0	1	1	0	D6	D6'
0	1	1	1	D7	D7'

Table 6-42

Truth table for a 74x151 8-input, 1-bit multiplexer.

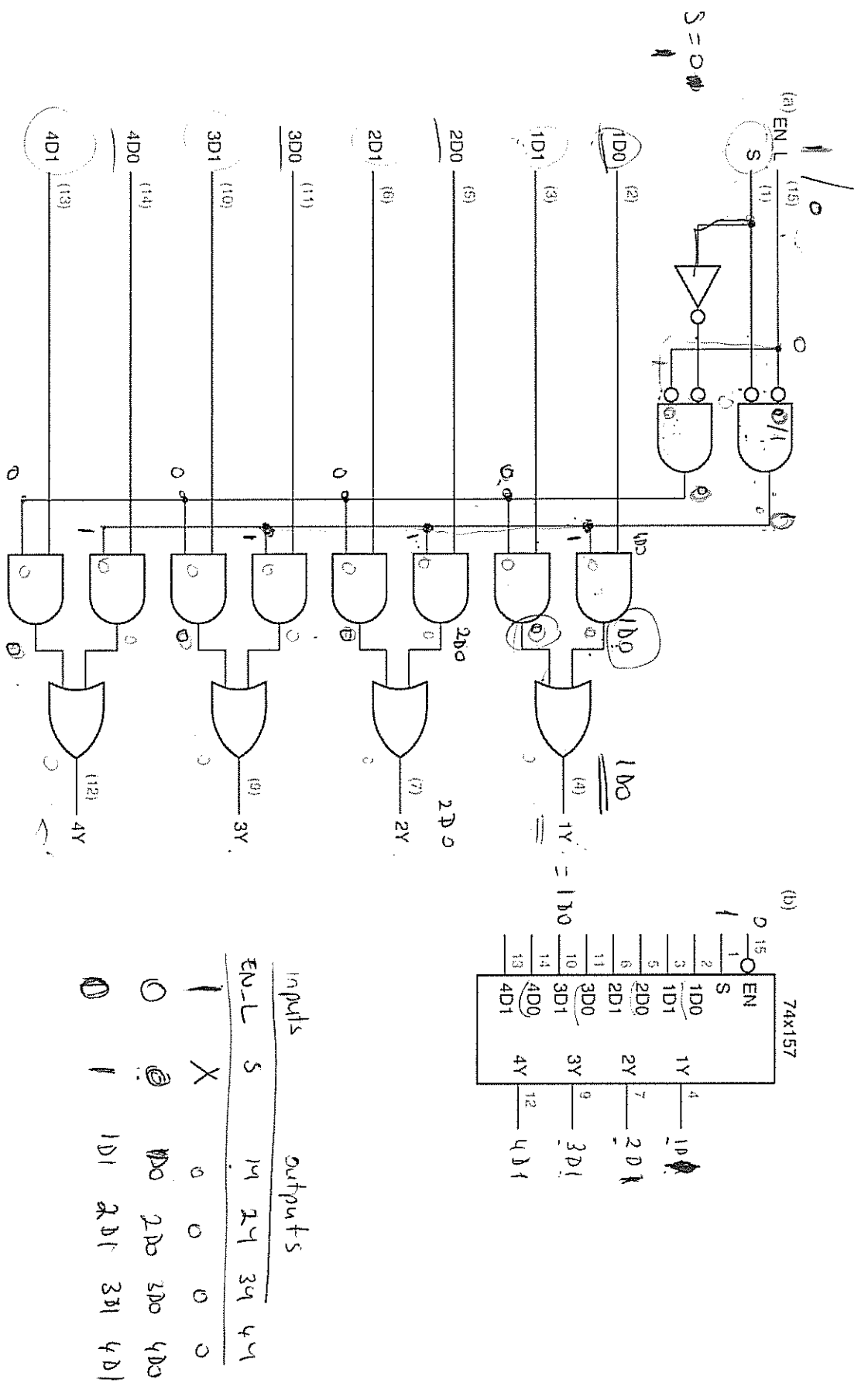


Figure 6-61

The 74x157 2-input, 4-bit multiplexer: (a) logic diagram; (b) traditional logic symbol.

From *Digital Design: Principles and Practices*, Fourth Edition, John F. Wakerly, ISBN 0-13-186389-4.

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<i>Inputs</i>		<i>Outputs</i>			
EN_L	S	1Y	2Y	3Y	4Y
1	x	0	0	0	0
0	0	1D0	2D0	3D0	4D0
0	1	1D1	2D1	3D1	4D1

Table 6-43

Truth table for a 74x157 2-input, 4-bit multiplexer.

$$iY = \sum_{j=0}^{n-1} \epsilon_{N_j} M_j \cdot iD_j$$

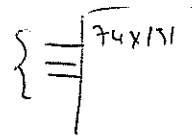
$iY$ : particular output bit  
 $(0 \leq i \leq b)$

$iD_j$ : input bit  $i$  of source  $j$   
 $0 \leq j \leq n-1$

$M_j$ : minterm  $j$  of  $s$  select inputs.

example:

$$74 \times 151$$



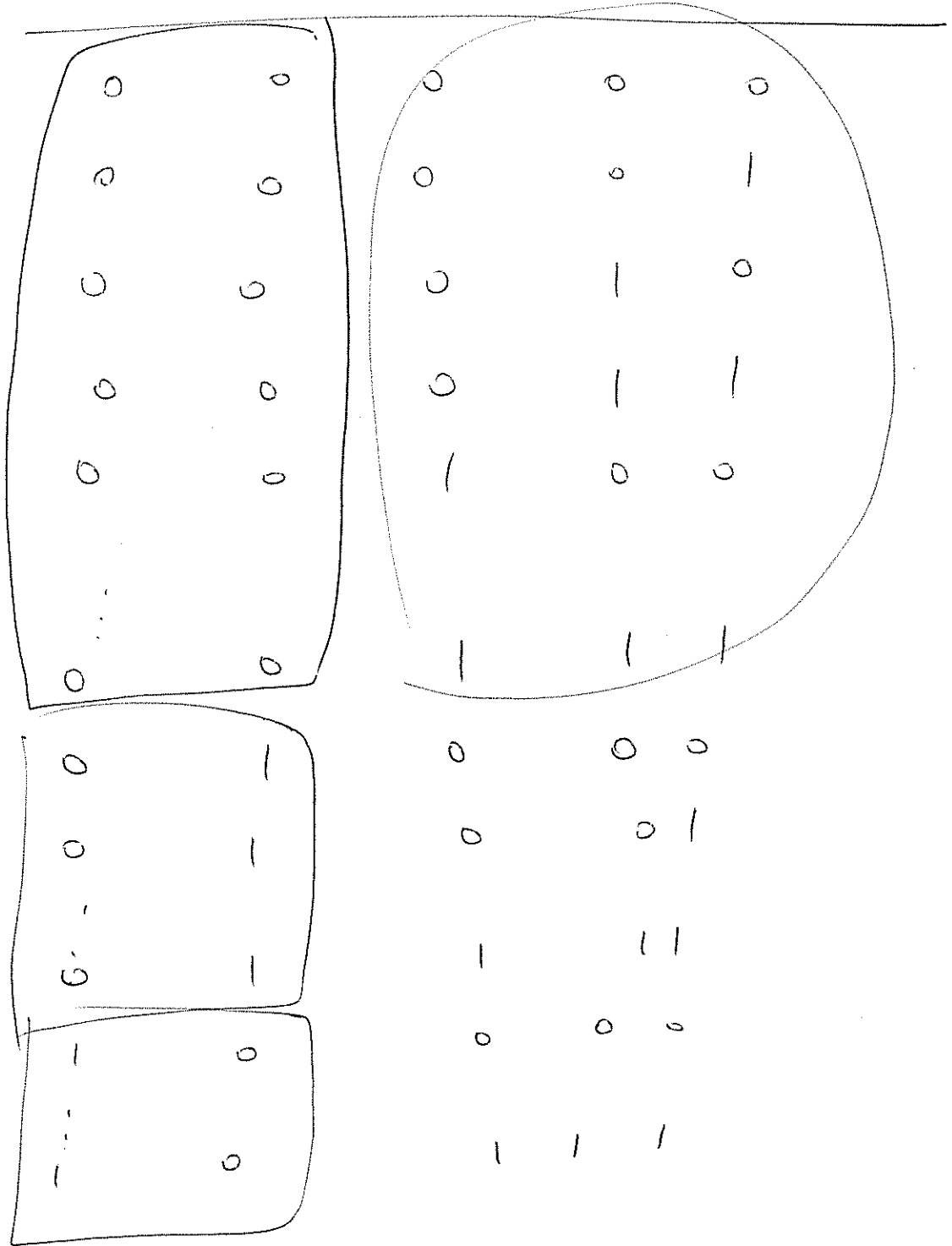
$XA_4$

$XA_3$

$XA_2$

$XA_1$

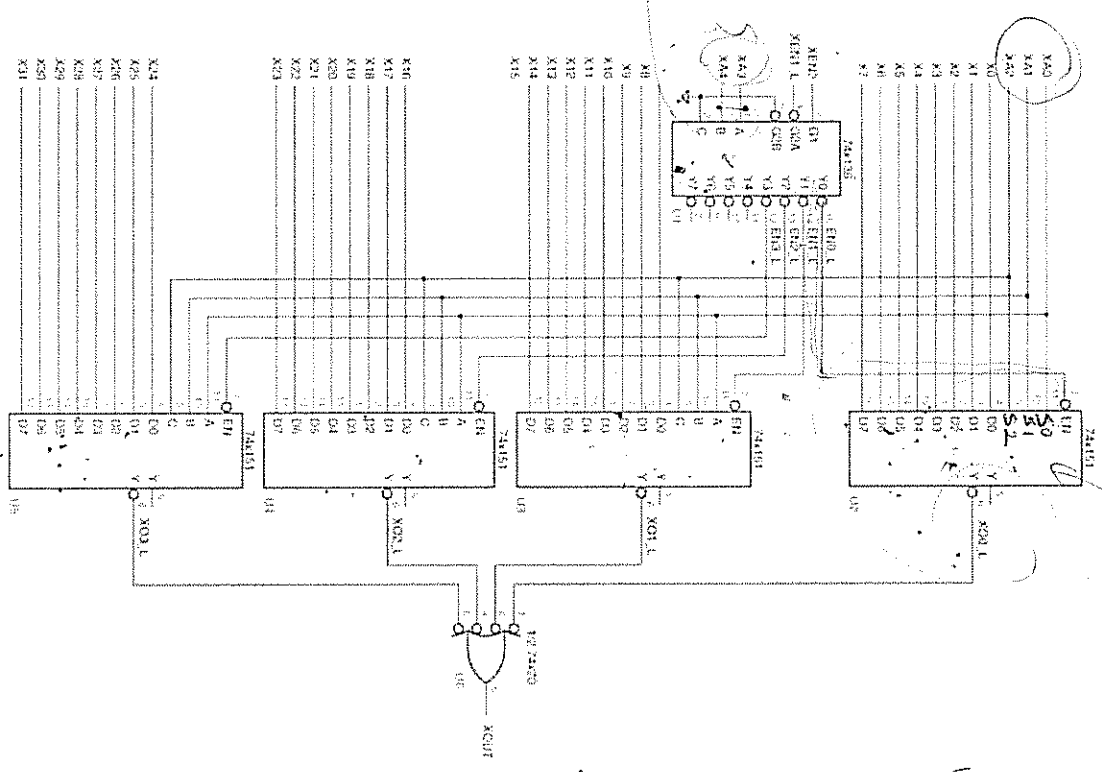
$XA_0$





two higher order select bits  
to enable one of four

2 to 4 decoder



XA4 XA3				XA2 XA1 XA0			
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Figure 6-62

Combining 74x151s to make a 32-to-1 multiplexer.

Exclusive OR : XOR

2 input gate: output is 1 if  
exactly one of its inputs is 1.

X		Y		$X \oplus Y$		$(X \oplus Y)'$	
0	0			0		1	
0	1			1		0	
1	0			1		0	
1	1			0		1	

Exclusive NOR (XNOR) : Equivalence gate.

produces 1 output if its inputs are  
the same.

$$X \oplus Y = X' \cdot Y + X \cdot Y'$$

$I_1 \mid I_2 \mid I_3 \mid I_4 \mid \dots \mid I_N$   
 $0 \mid 1 \mid 0 \mid 1 \mid \dots \mid 0$

odd - parity circuit: output = 1  
 if odd number of inputs = 1.

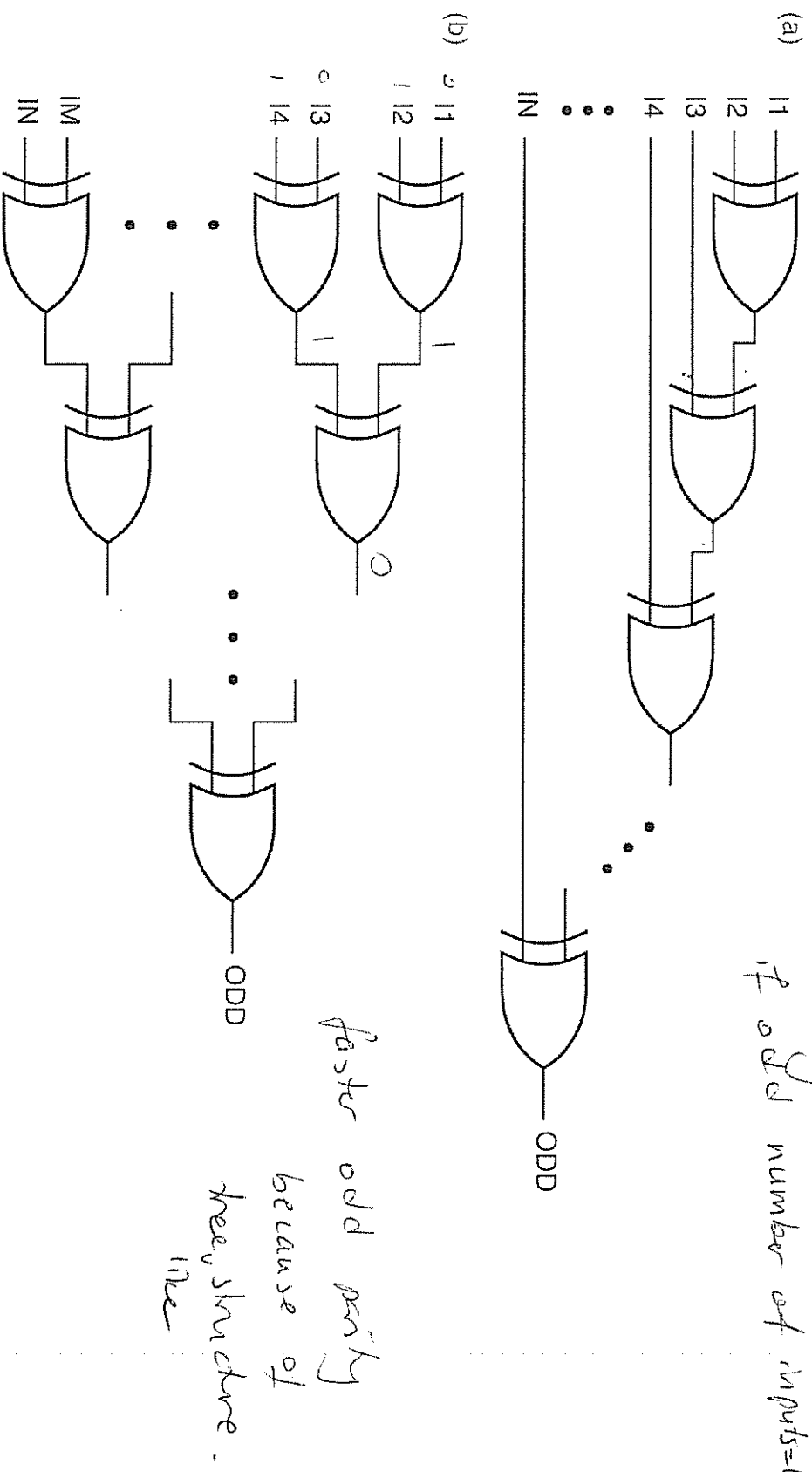


Figure 6-70

Cascading XOR gates: (a) daisy-chain connection; (b) tree structure.

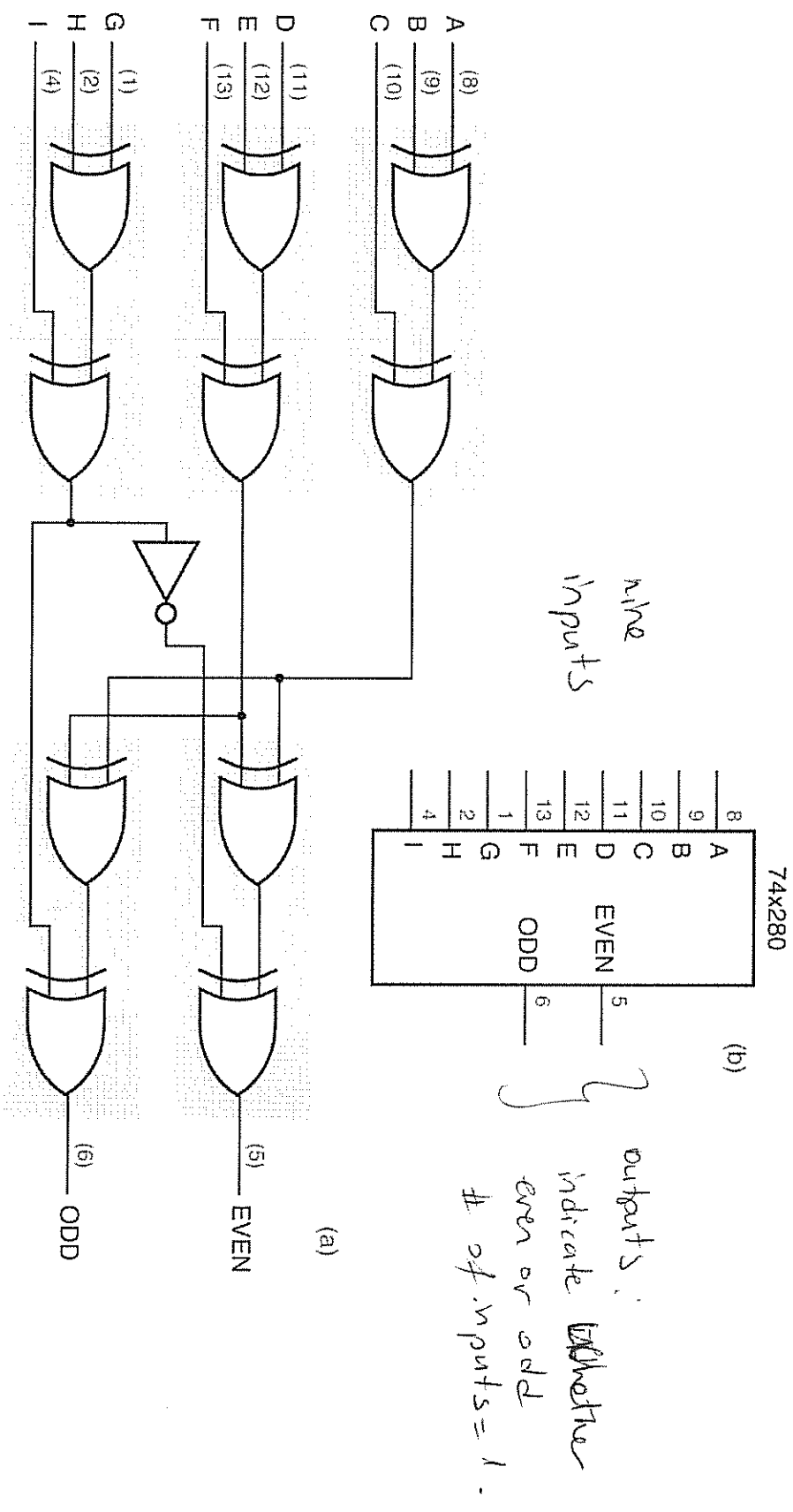


Figure 6-71

The 74x280 9-bit odd/even parity generator: (a) logic diagram; (b) traditional logic symbol.

## comparators

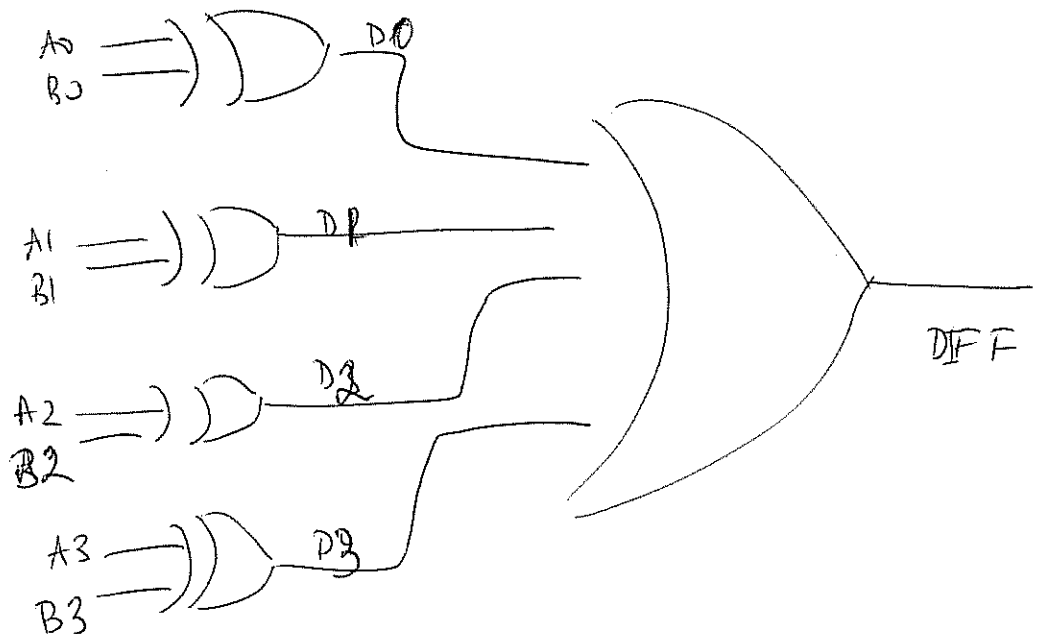
a circuit that compares two binary words for equality.



If inputs are different  $\Rightarrow$  DIFF = 1

## 4-bit comparator

$\left. \begin{array}{l} A_3 A_2 A_1 A_0 \\ B_3 B_2 B_1 B_0 \end{array} \right\}$



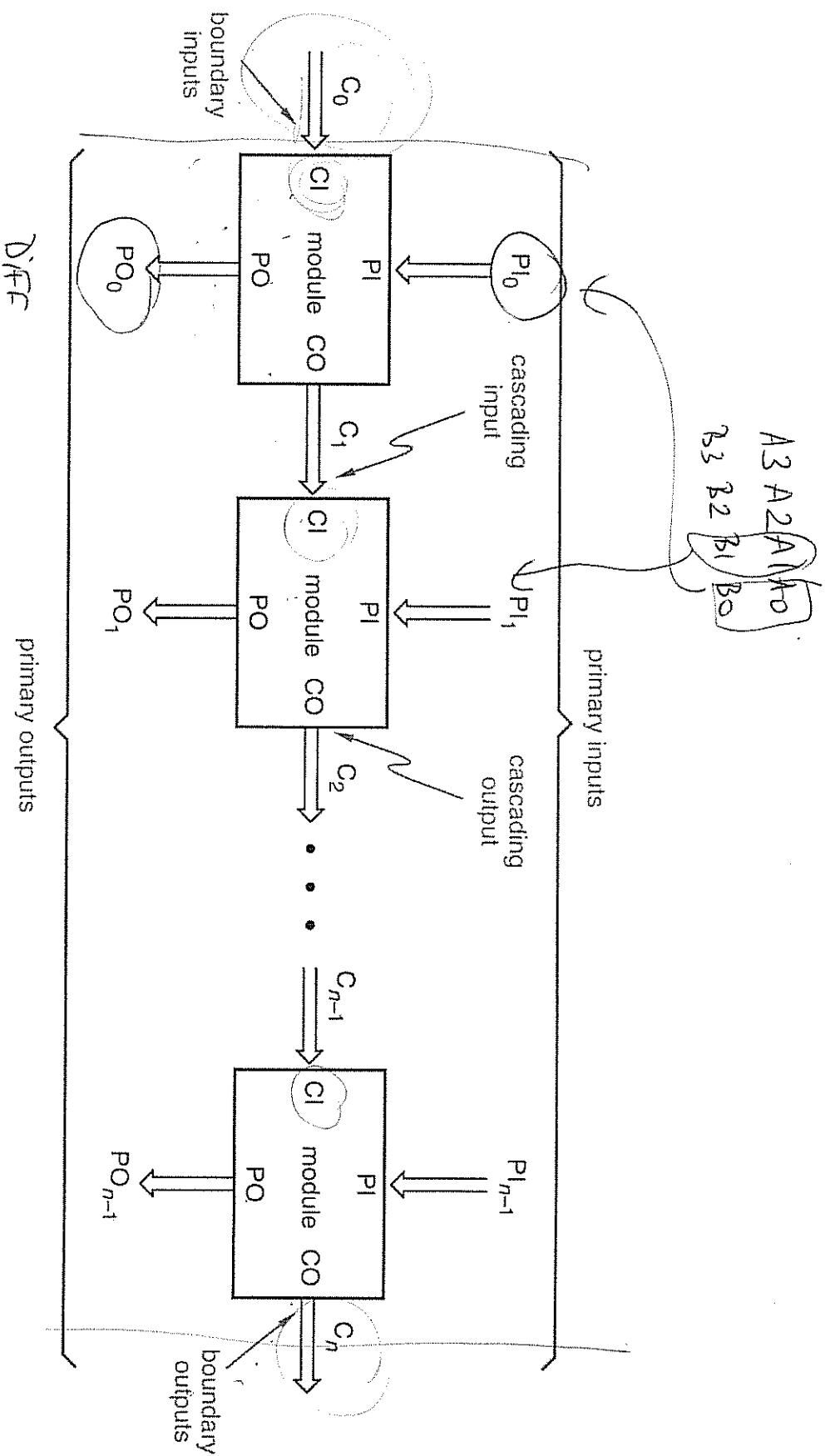


Figure 6-76

General structure of an iterative combinational circuit.

Example: Iterative Comparator. (equivalence)

