EECS 281 January 22, 2015

Subtraction:

two's complement numbers:

negate subtrahend by taking two's complement, then add it to the minuend.

$$\begin{array}{r} 4 \\ -3 \\ \hline 1 \end{array} \qquad \begin{array}{r} 0100 \\ -0011 \end{array} \qquad \begin{array}{r} {\scriptstyle 1} \\ 0100 \\ +1101 \\ \hline \cancel{1}0001 \end{array}$$

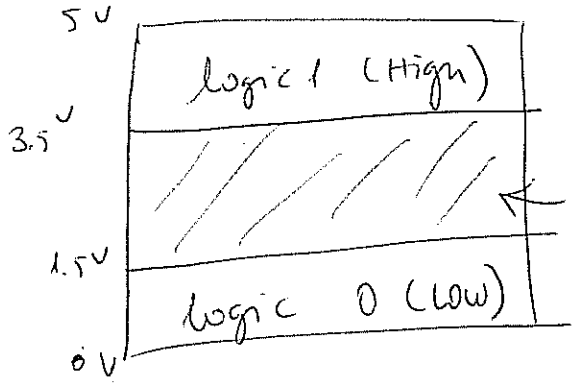
$$\begin{array}{r} 0011 \leftarrow 3 \\ 1100 \\ +\quad 1 \leftarrow \\ \hline 1101 \leftarrow -3 \end{array}$$

$$\begin{array}{r} {\scriptstyle 1}\leftarrow \text{cin} \\ 0100 \\ +1100 \\ \hline \end{array}$$

overflow: examine the signs of minuend and complemented of subtrahend: same rules apply as in addition.

Digital Circuits:

Map real values for physical quantities into two logic values 0 and 1.



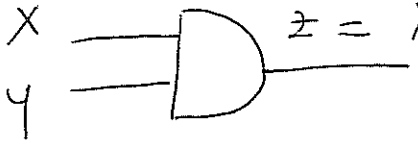
Combinational circuit: outputs depend only on its current inputs.

operation fully defined by a truth table.

Sequential Circuit: circuit with memory, outputs depend on current input and sequence of past inputs.

Three basic logic functions: AND, OR, NOT

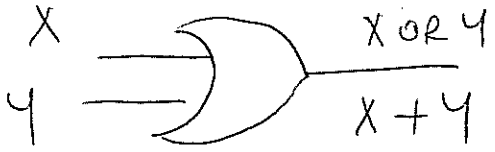
can be used to build any combinational digital logic circuit.



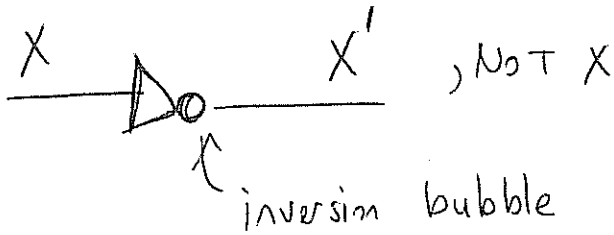
$Z = X \text{ AND } Y = X \cdot Y$

$2^2 = 4$

X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

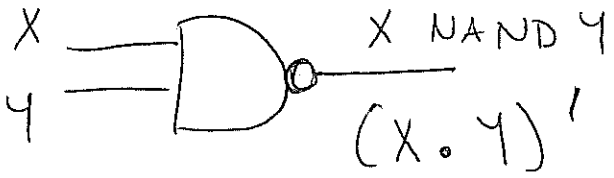


X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

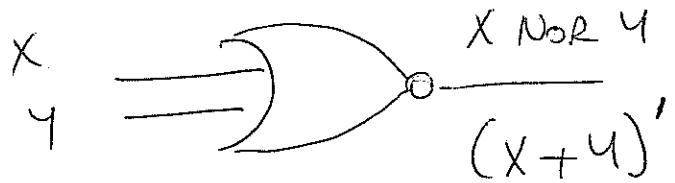


X	NOT X
0	1
1	0

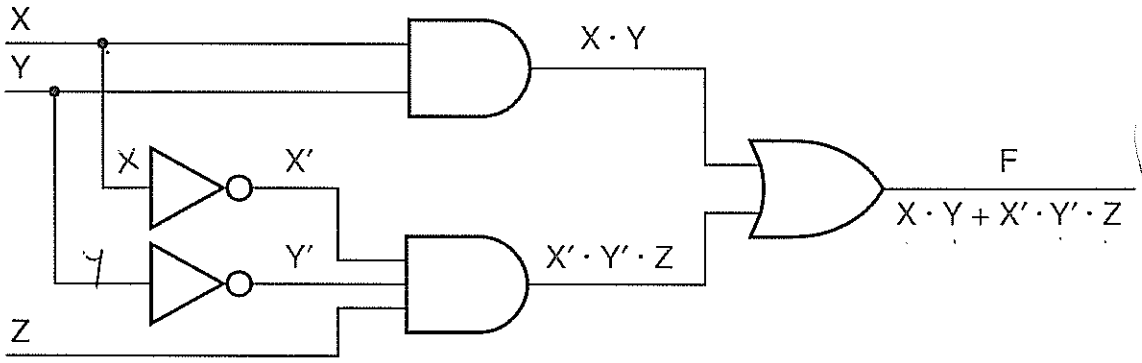
NAND : NOT - AND



X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0



X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0



X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Figure 3-4

Logic circuit with the truth table of Table 3-2.

$$F = X \cdot Y + X' \cdot Y' \cdot Z$$

$X=0, Y=0, Z=0 \quad F = 0 \cdot 0 + 1 \cdot 1 \cdot 0 = 0$

logic signals : do not change from 0→1 instantaneously

lag between input change and corresponding output change.

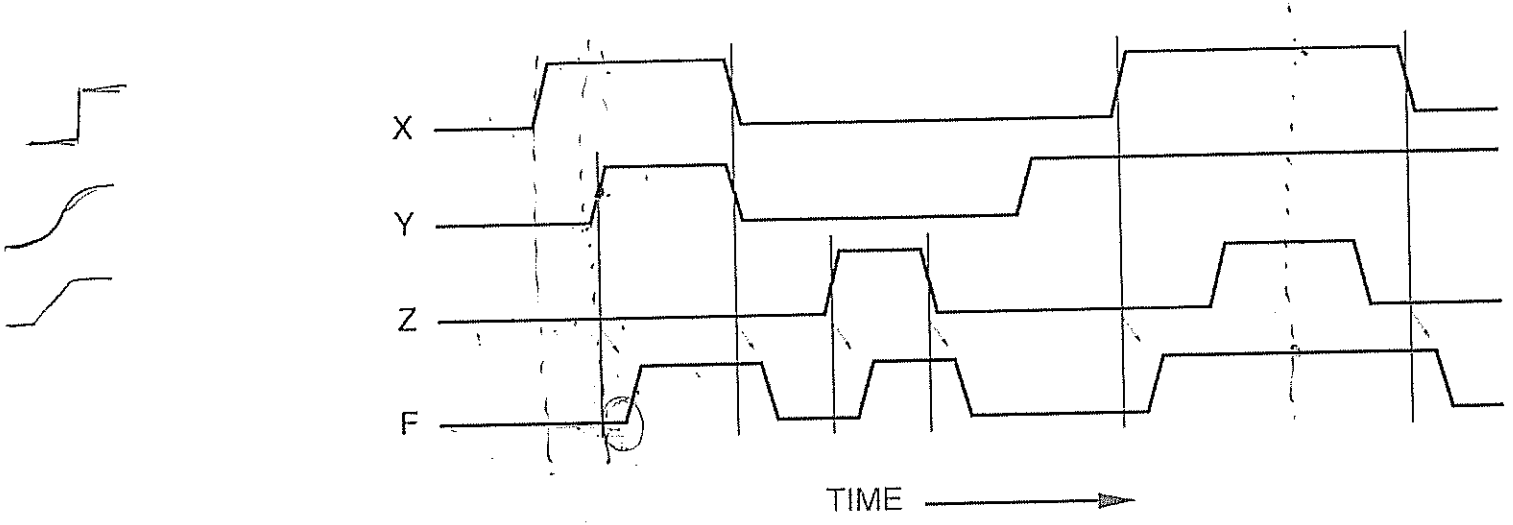


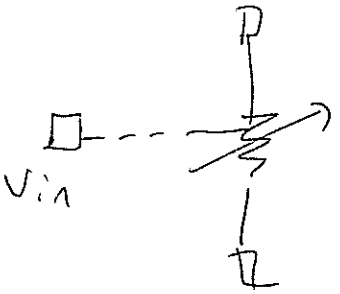
Figure 3-5

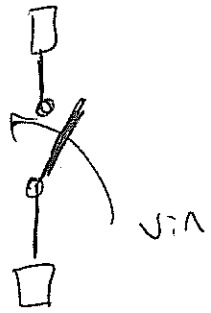
Timing diagram for a logic circuit.

CMOS logic circuits

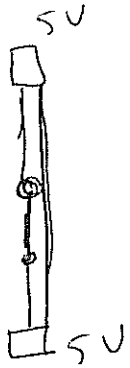
building blocks MOS transistors.

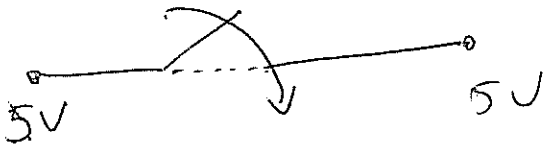
modeled them as 3-terminal device that acts like a voltage controlled resistance.

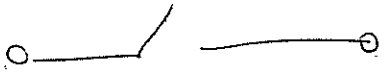




e.g. $V_{in} = 0$

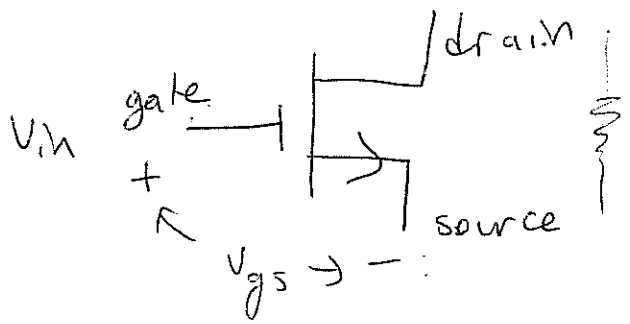






MOS transistors → n-channel
↓ p-channel

n-channel : NMOS



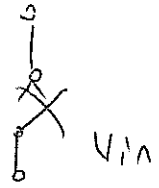
normally $V_{gs} \geq 0$

increase V_{gs} ⇒ decrease R_{ds}

$V_{gs} = 0 \Rightarrow$ R_{ds} = very high.

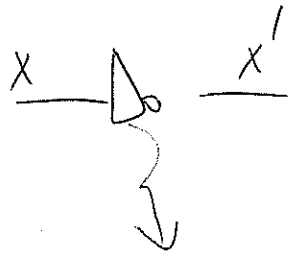
V_{in} = H = 5V ⇒ switch is closed.

p-channel : PMOS



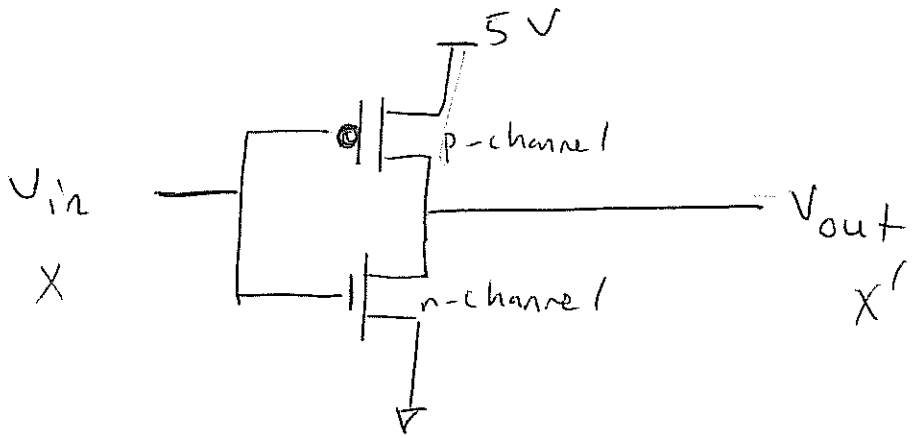
V_{in} = L

switch is closed.

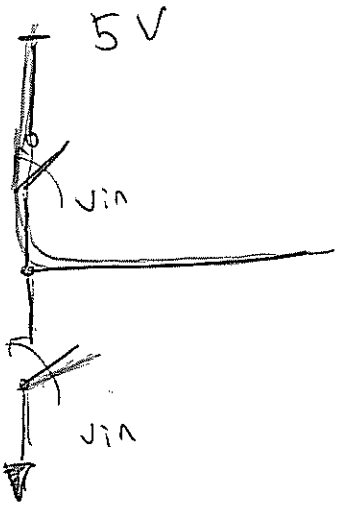


$\frac{1}{7}$ ⏚ :

ground = 0'
= L

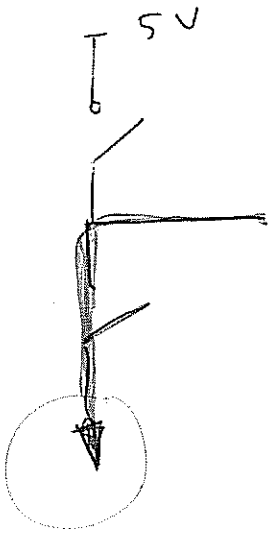


V_{in} = L

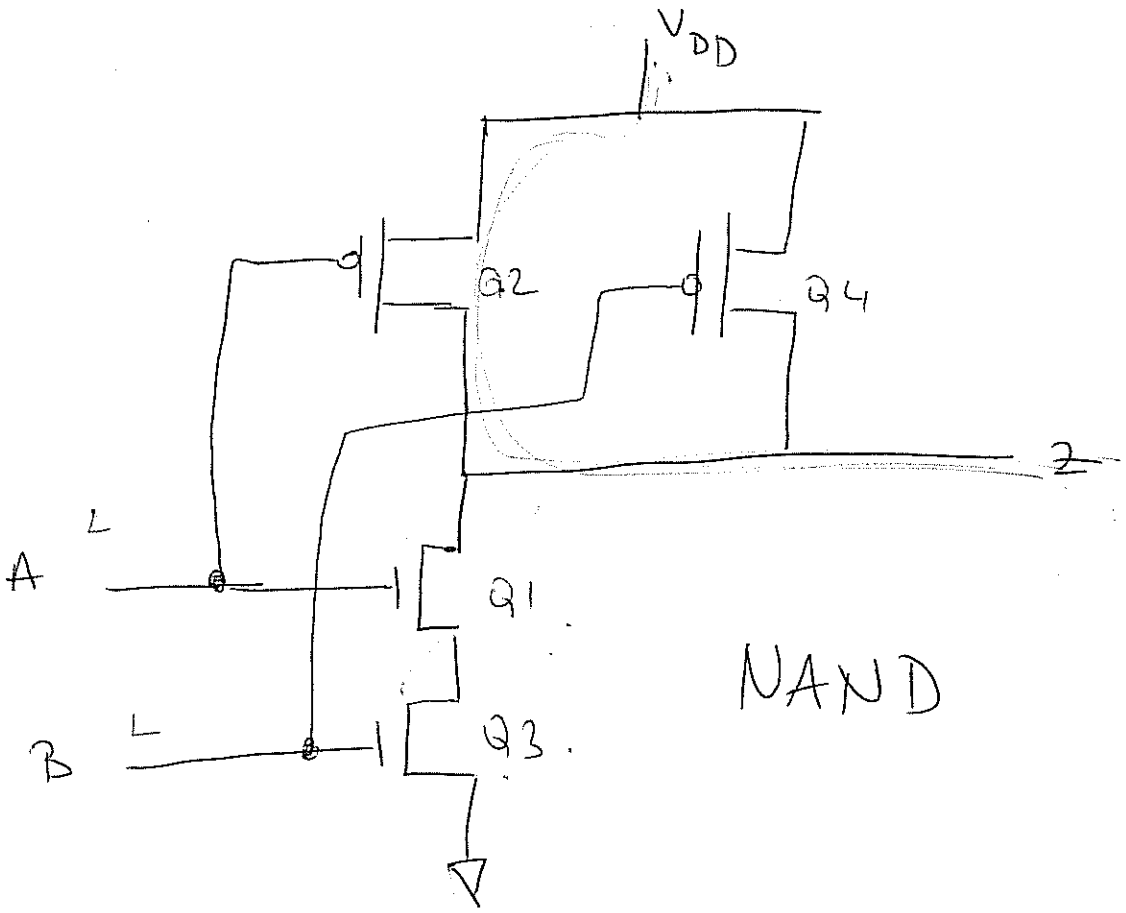


V_{out} = 5V = H

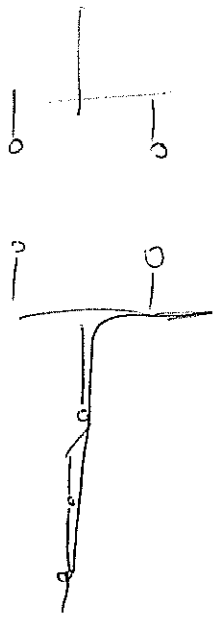
V_{in} = H



V_{out} = L



NAND



A	B	Q1	Q2	Q3	Q4	Z
L	L	OFF	ON	OFF	ON	H
L	H	OFF	ON	ON	OFF	H
H	L					H
H	H					L