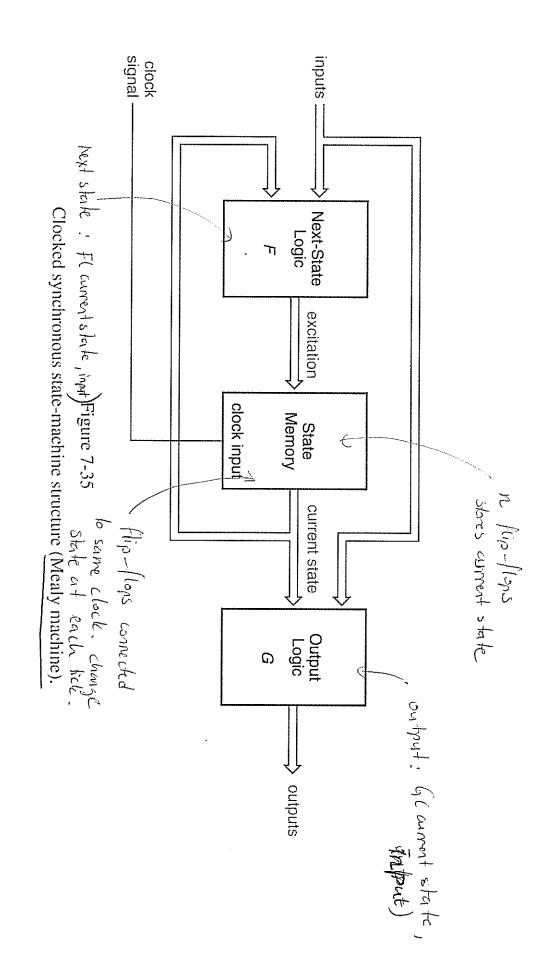
a SR	٥o.	Ġ!		10.
0	0	0	0	$\left(\left(i\right) \right)$
		0	0	

$$QX = RQ + SR' = S + RQ$$



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At ising edge of clock signed: 9x = D.

state variables: 90,91 To determine current D.

, CFK I input clock signal ő, S m Z Ē ō 8 Next-State Logic F 6 60 G_ G_ Ŷ 9 m 35 45 E J 0/ excitation State Memory VOLK O Ω ō 8 current state Output Logic G 90 * 11 00 MAK= 90. 91. EN - MAX output

Figure 7-38

Clocked synchronous state machine using positive-edge-triggered D flip-flops.

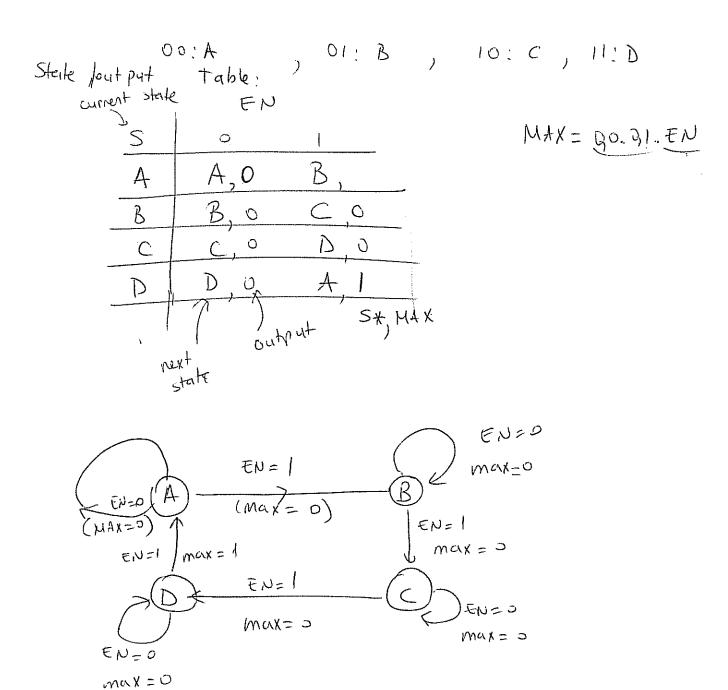
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Transition equations

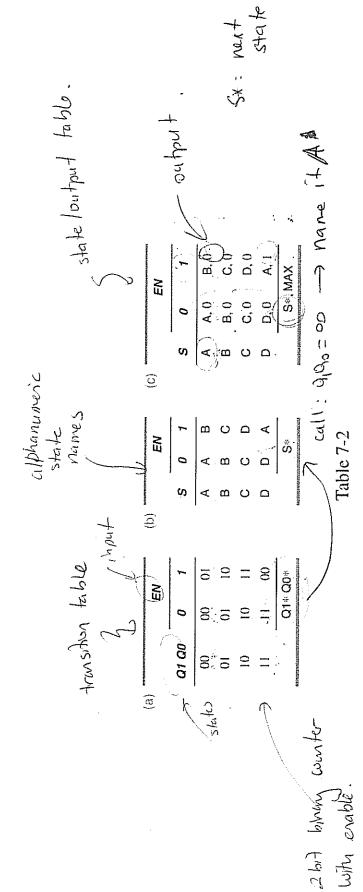
output equation:

Transition, state, state/output Tables.

Trav	olties	n Table	? :	EN			
	0 1	0.0	1 0	1 1			
	91	90	00	01	_		
	0	1	91	10			
	1	0	10	11			
	l	1	11	00			
	31* 40*						
			ai x				



she to ble:



(c = XXW) Transition, state, and state/output tables for the state machine in Figure 7-38. (MAX = 0)th= (10° TE (MAK=0) malhlain current When the o . なる

(MAK=0)

EN= (

FNIO

(MAK=0)

6√20

あること

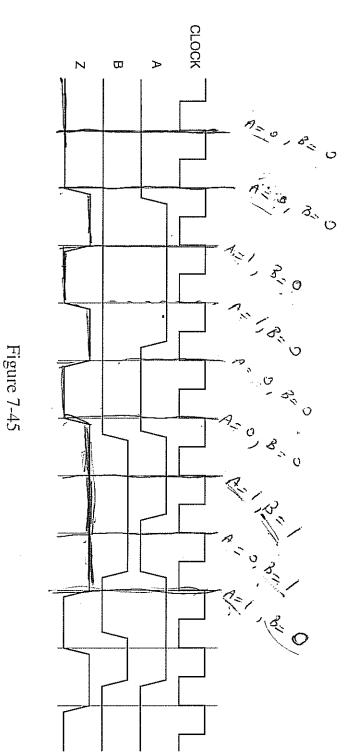
EN=1 (CMAK= 1)

1 at each hick.

odvance by

When the 1)

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Timing diagram for example state machine.

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Example: Design a clocked synchronous state machine with two inputs A and B and a single output 2:

2 becomes 1 when:

- A had the same value at each of the two previous clock ticks or

B has been I since the last time that the first wondition was true.

o|w 2=0.

Got A=0 A = 0	on previous fick on the hick before that		A B				12
A +	meening	Stelle	00	10 · (.		(10)	
1	Init state	INIT	Ao	AO	Al	A J	0
	Got a O dn A	AO	oK0	OKO	Al	Al	0
,	Got a l onA	A	AO	Аo	OKI	OKI	(0
`		OK O	OK0	oko	oK	A-/	
`		0 (<)	AD	OKO	OKI	PKI	
	And the second s	-					7