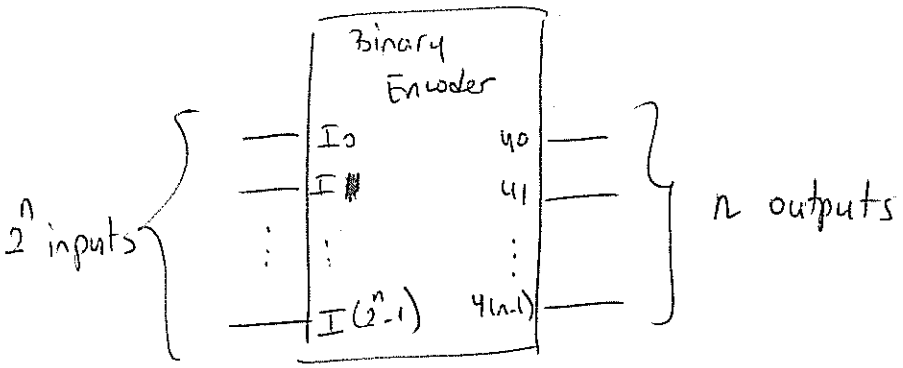
EECS 281, February 17, 2015

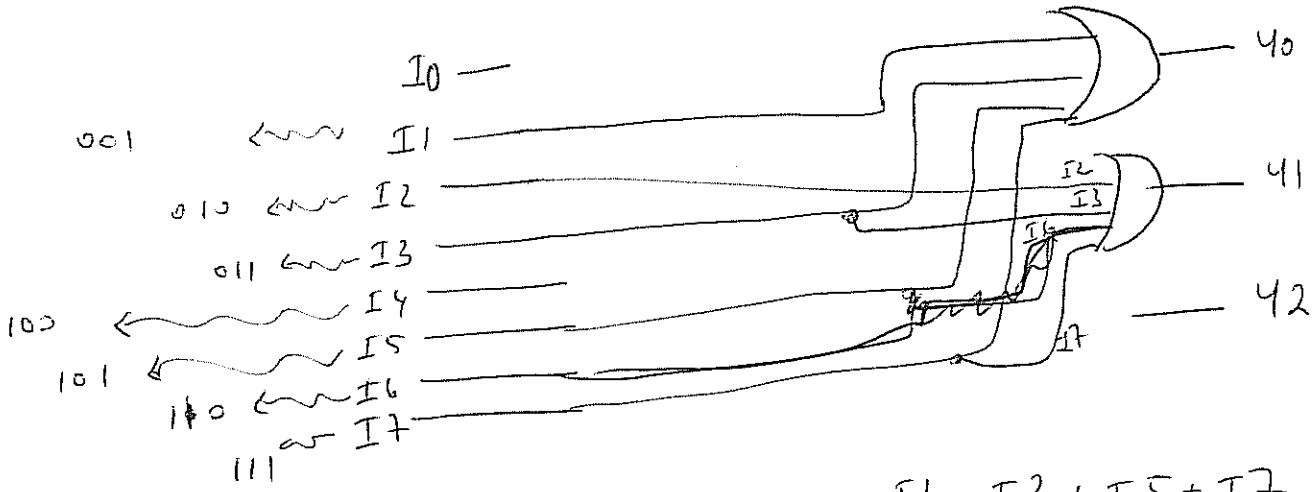
Encoders

Output code has fewer bits than input code.

simplest encoder to build: 2^n-to-n binary encoder.



e.g. 8-to-3 Encoder



$Y_0 = I_1 + I_3 + I_5 + I_7$

$Y_1 = I_2 + I_3 + I_6 + I_7$

$Y_2 = I_4 + I_5 + I_6 + I_7$

I1 : active → 001 Y0 = I3

I7	I6	...	I2	I1	I0
0	0	...	0	1	0

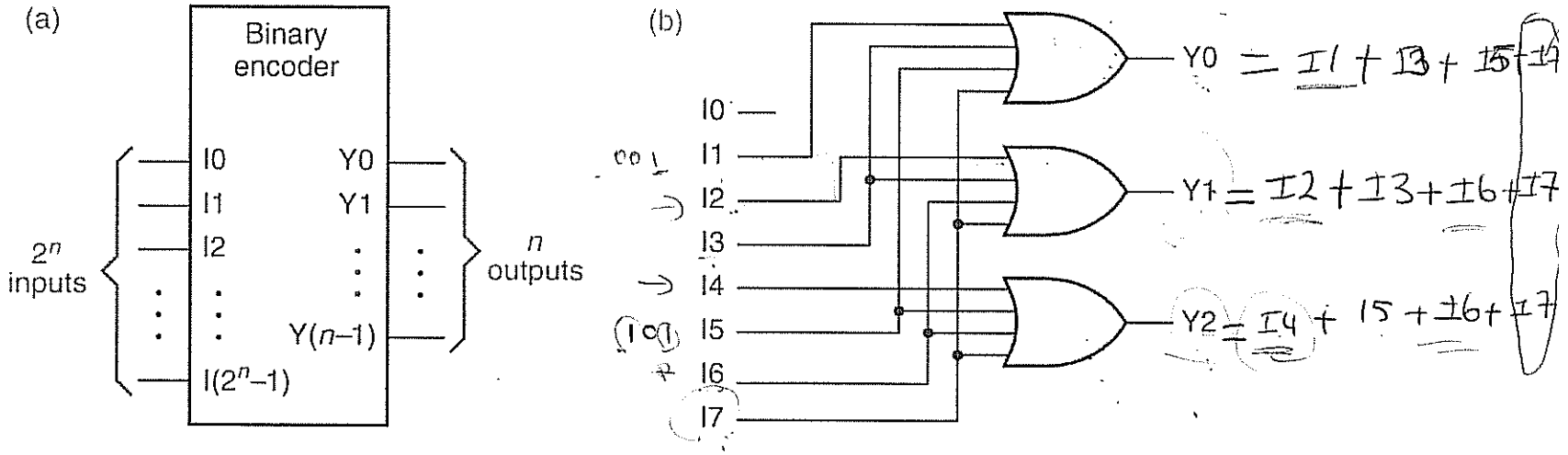


Figure 6-45

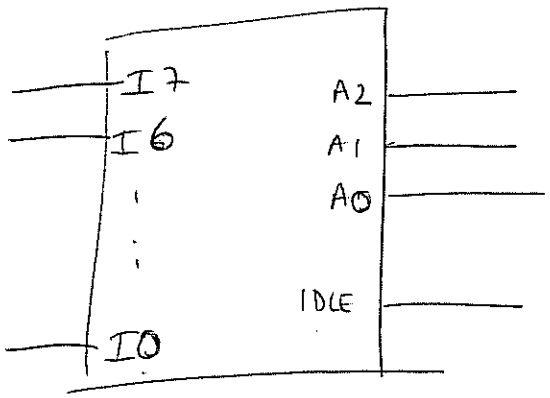
Binary encoder: (a) general structure; (b) 8-to-3 encoder.

	Y2	Y1	Y0
I0 = 1	0	0	0
I1 = 1	0	0	1
I2 = 1	0	1	0

	Y2	Y1	Y0
I3 =	0	1	1
I4 =	1	0	0
I5 =	1	0	1
I6 =	1	1	0
I7 =	1	1	1

Priority Encoders

I7 has highest priority.



IDLE output is asserted if no inputs are asserted. $H_0 - H_7$: such that $H_i = 1$ iff I_i is the highest priority 1 input.

$$H_7 = I_7$$

$$H_6 = I_6 \cdot I_7'$$

$$H_5 = I_5 \cdot I_6' \cdot I_7'$$

$$\vdots$$

$$H_0 = I_0 \cdot I_1' \cdot I_2' \cdot I_3' \cdots I_7'$$

$$A_2 = H_4 + H_5 + H_6 + H_7$$

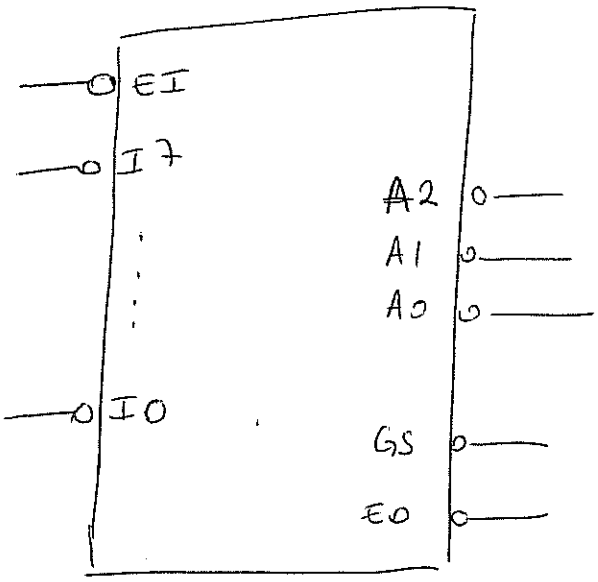
$$A_1 = H_2 + H_3 + H_6 + H_7$$

$$A_0 = H_1 + H_3 + H_5 + H_7$$

$$IDLE = (I0 + I1 + \ldots + I7)'$$

$$= I0' \cdot I1' \cdot \ldots \cdot I7'$$

74x148 : Priority Encoder



GS_L is asserted when the device is enabled and one or more request inputs are asserted.

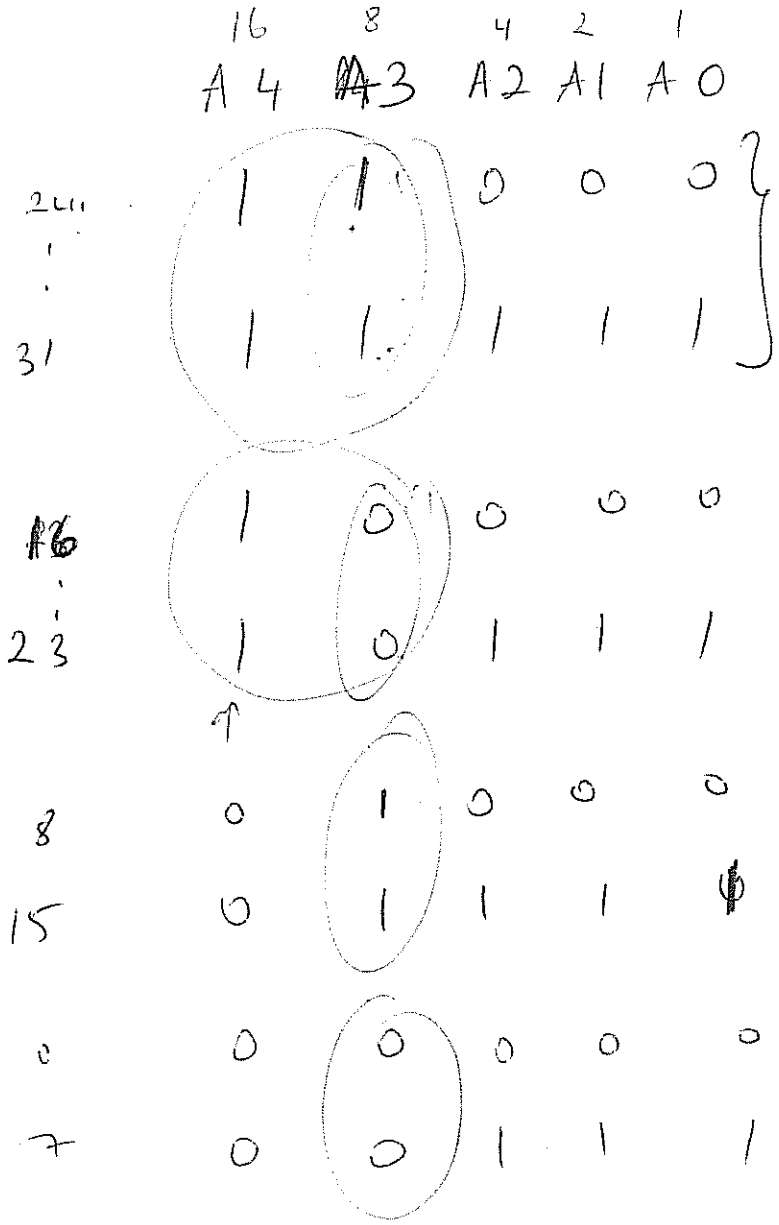
EO_L: enable output for cascading. Designed to be connected to the EI_L input of another '148 that handles lower-priority requests. asserted if EI_L is asserted but no request input is asserted.

highest priority input

Inputs									Outputs				
EI_L	I0_L	I1_L	I2_L	I3_L	I4_L	I5_L	I6_L	I7_L	A2_L	A1_L	A0_L	GS_L	EO_L
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

Table 6-27

Truth table for a 74x148 8-input priority encoder.


16 8 4 2 1
A4 A3 A2 A1 A0
24
31
16
23
8
15
0
7

inputs:
0 - 31
↑
highest
priority

32 X 5

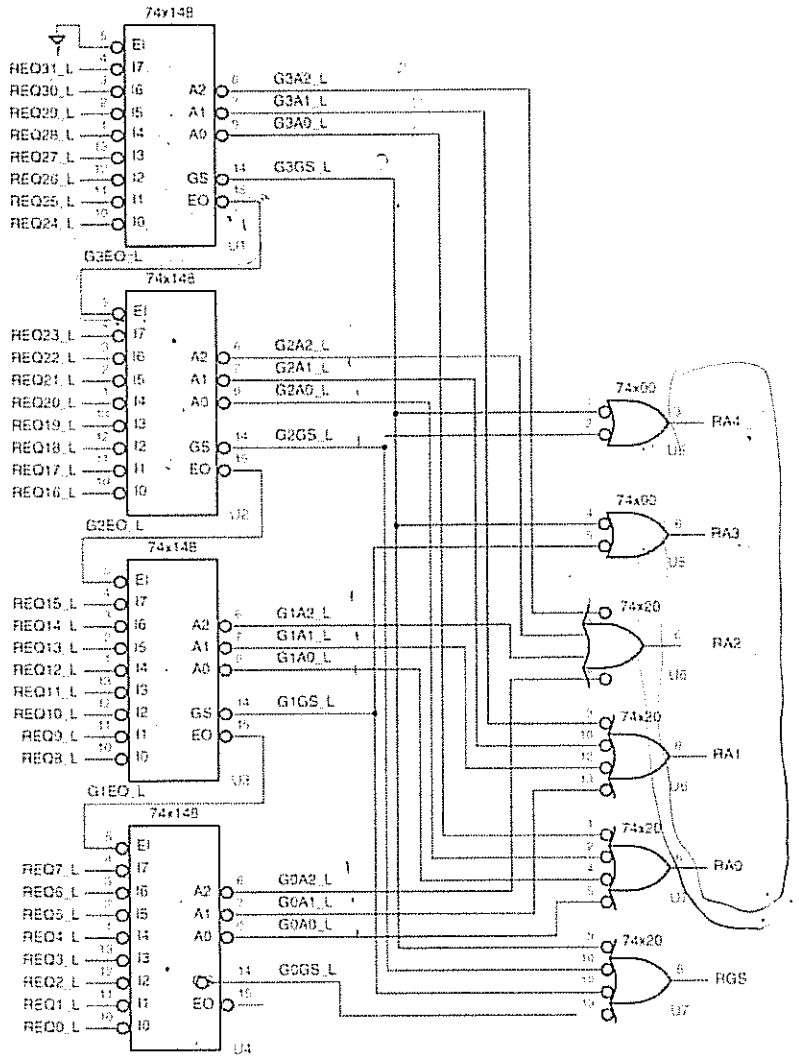
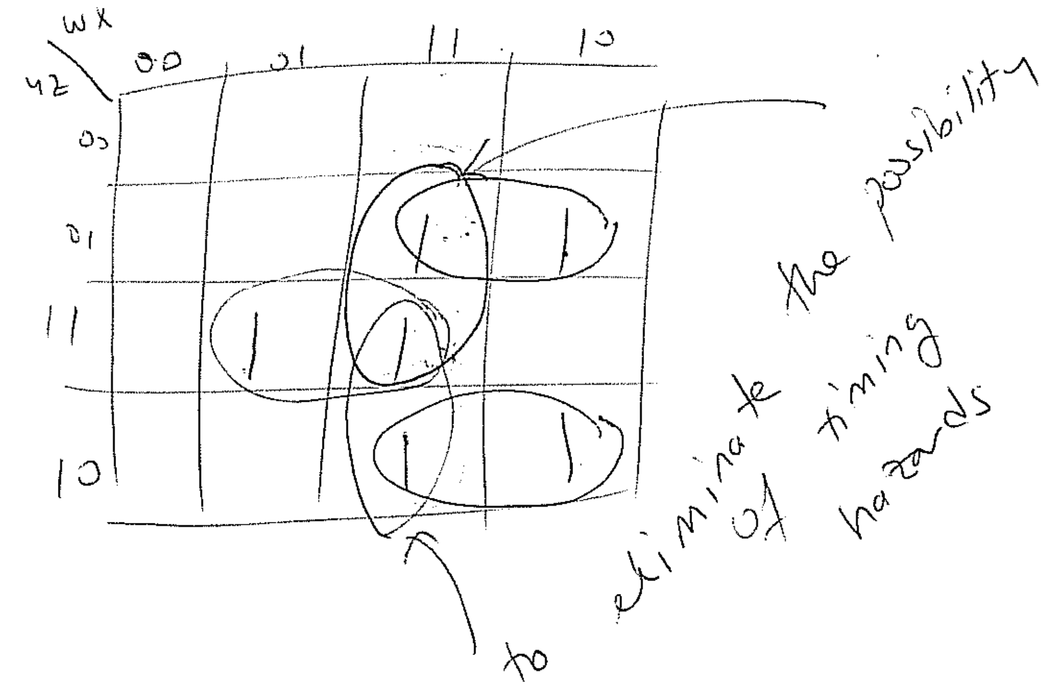


Figure 6-49

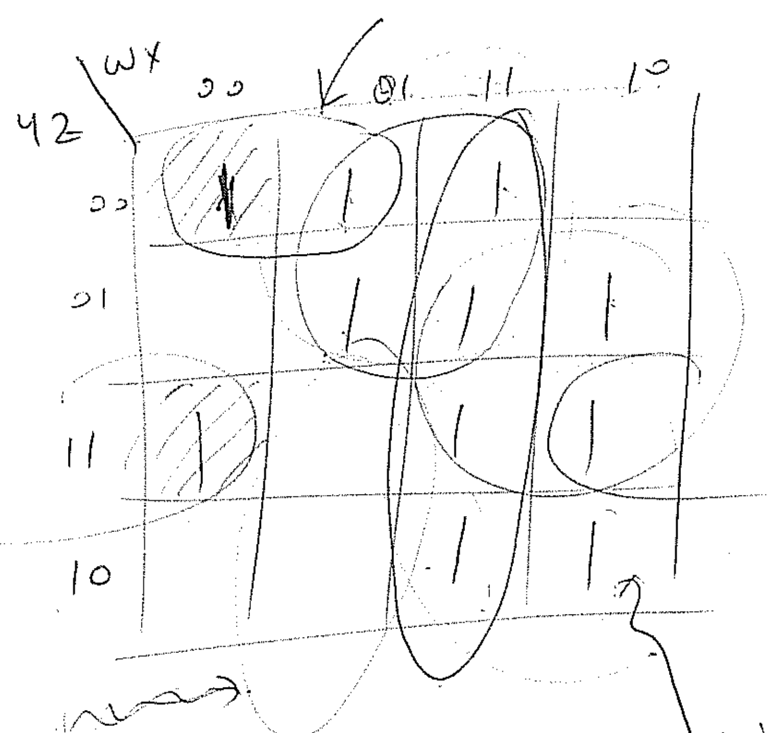
Four 74×148s cascaded to handle 32 requests.

timing hazard

e.g.



e.g.



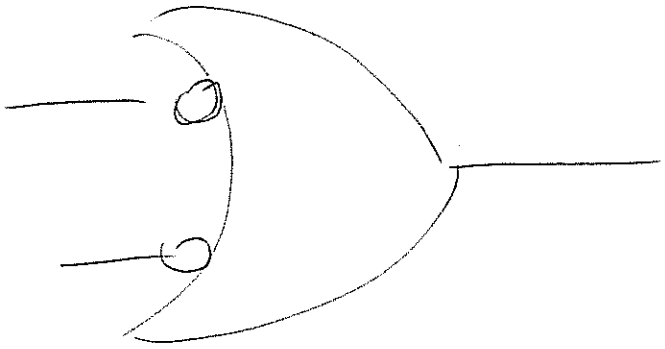
$(w + x' + y')$

$(w + x' + y' + z') \cdot (w + x' + y' + z)$

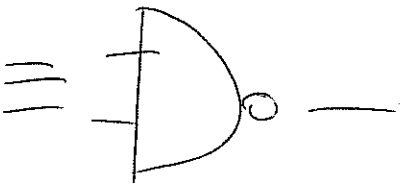
wxyz
1010

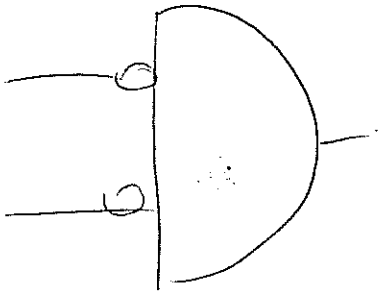
minterm: $wx'yz'$

maxterm: $w' + x + y' + z$

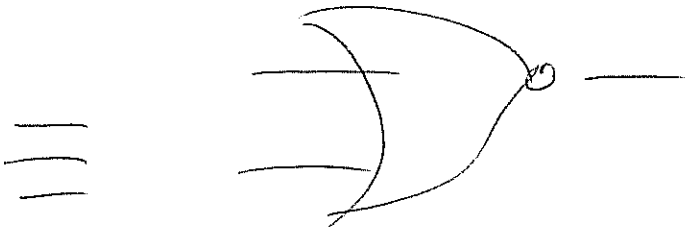


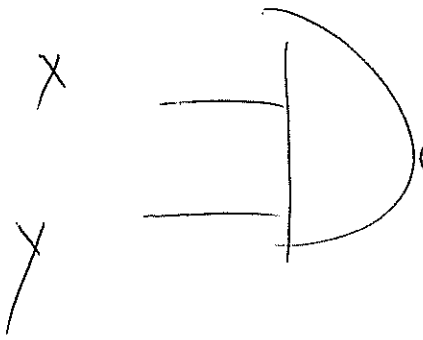
≡





≡





$(X \cdot Y)'$ ≡

$X' + Y'$