EECS 281, March 26, 2015

Example: state machine that controls tail lights of a car.

For turns Two input signals: LEFT, RIGHT.

Emergency flasher: input HAZ OR LEFT or RIGHT at the same time all tail lights are on.

Free running clock signal with freq. of desired flashing rate.

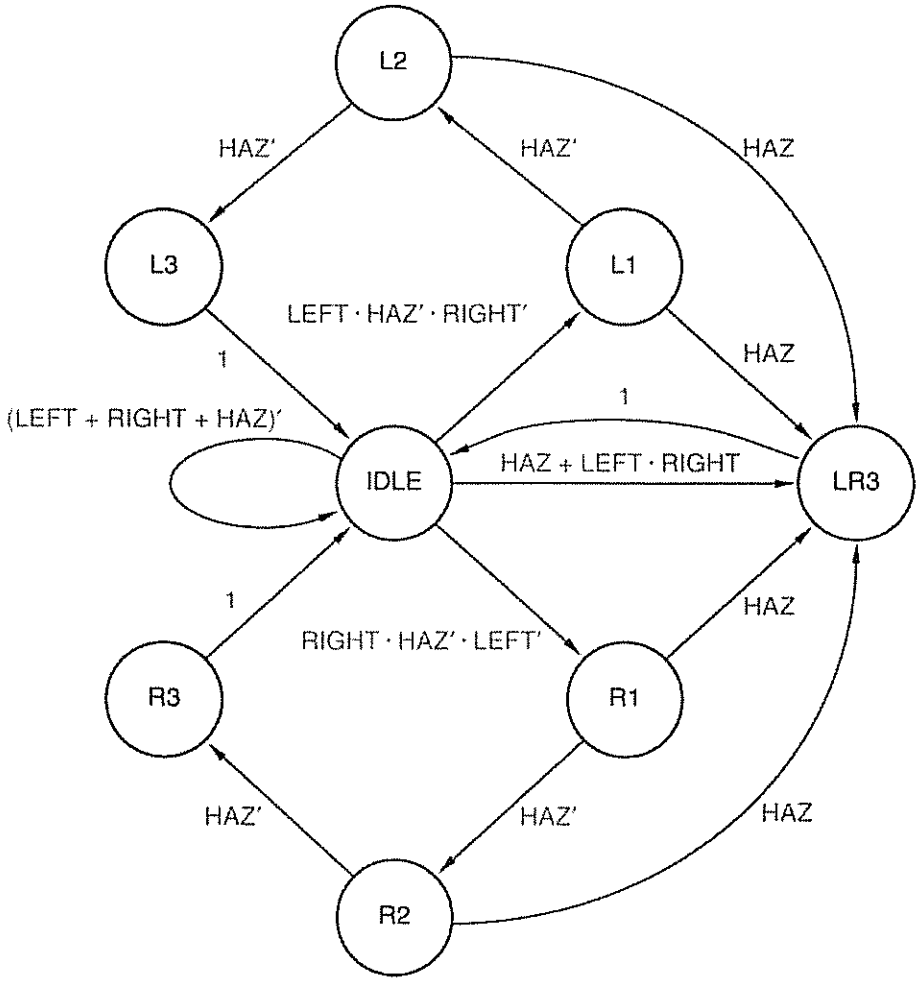
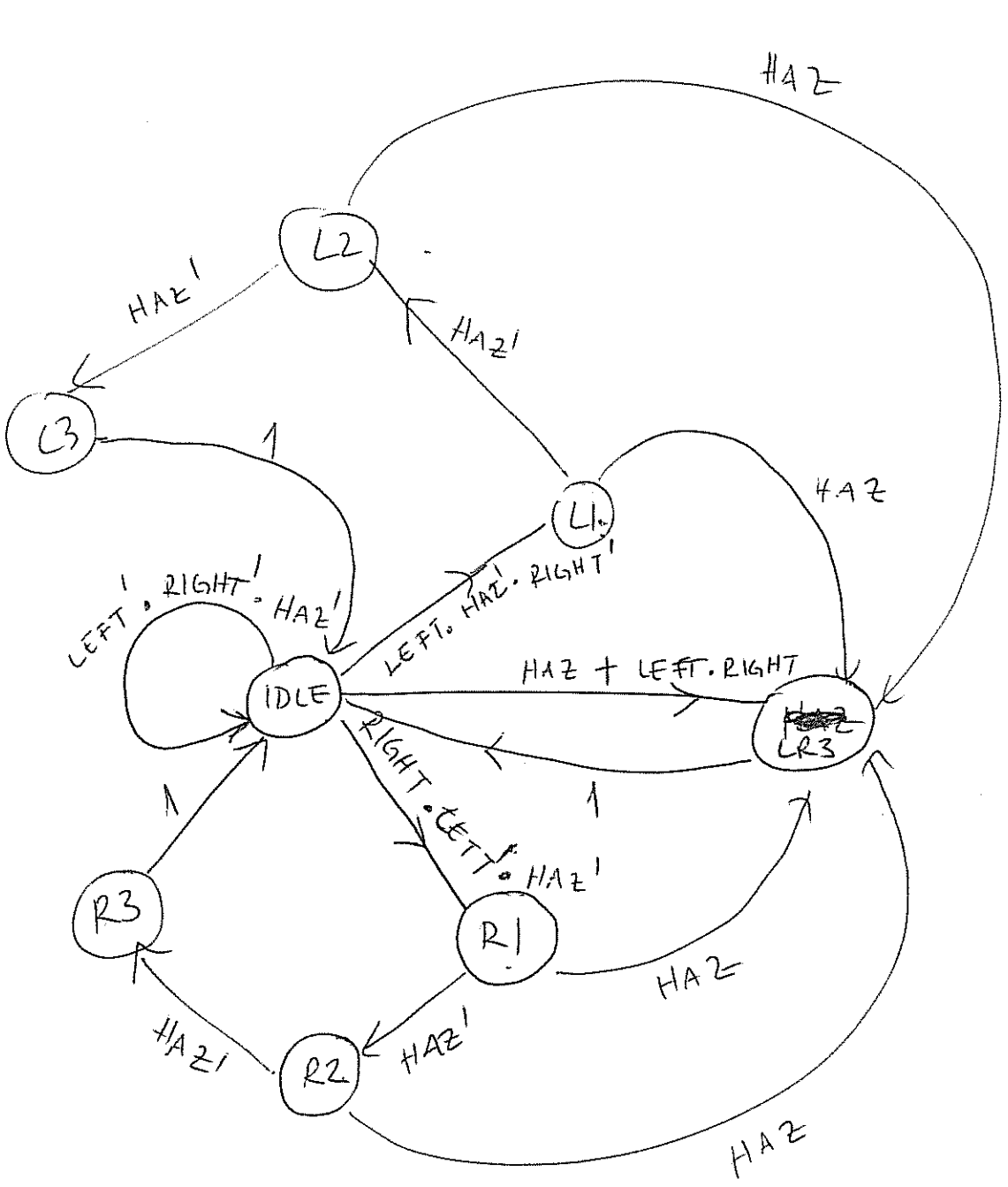


Figure 7-58

Enhanced state diagram for T-bird tail lights.



output table

state	outputs LC	LB	LA	RA	RB	RC
IDLE	0	0	0	0	0	0
L1	0	0	1	0	0	0
L2	0	1	1	0	0	0
L3	1	1	1	0	0	0
⋮						
LR3	1	1	1	1	1	1

$$LA = 1 + L2 + L3 + LR3$$

$$LB = L2 + L3 + LR3$$

$$LC = L3 + LR3$$

$$\vdots$$

I have 8 states $\Rightarrow$ will need a minimum of 3 flip-flops.

state assignments:

state	q2	q1	q0
IDLE	0	0	0
L1	0	0	1
L2	0	1	1
L3	0	1	0
R1	1	0	1
R2	1	1	1
R3	1	1	0
LR3	1	0	0

$Q2^* = Q2' \cdot Q1' \cdot Q0 \cdot HAZ' + Q2' Q1 Q0 HAZ' +$
$Q2 Q1' Q0 HAZ' + Q2 Q1 Q0 HAZ'$

S	Q2	Q1	Q0	Transition Expression	S	Q2	Q1	Q0
IDLE	0	0	0	(LEFT + RIGHT + HAZ)'	IDLE	0	0	0
IDLE	0	0	0	LEFT · HAZ' · RIGHT'	L1	0	0	1
IDLE	0	0	0	HAZ + LEFT · RIGHT	LR3	1	0	0
IDLE	0	0	0	RIGHT · HAZ' · LEFT'	R1	1	0	1
L1	0	0	1	HAZ'	L2	0	1	1
L1	0	0	1	HAZ	LR3	1	0	0
L2	0	1	1	HAZ'	L3	0	1	0
L2	0	1	1	HAZ	LR3	1	0	0
L3	0	1	0	1	IDLE	0	0	0
R1	1	0	1	HAZ'	R2	1	1	1
R1	1	0	1	HAZ	LR3	1	0	0
R2	1	1	1	HAZ'	R3	1	1	0
R2	1	1	1	HAZ	LR3	1	0	0
R3	1	1	0	1	IDLE	0	0	0
LR3	1	0	0	1	IDLE	0	0	0

Table 7-14

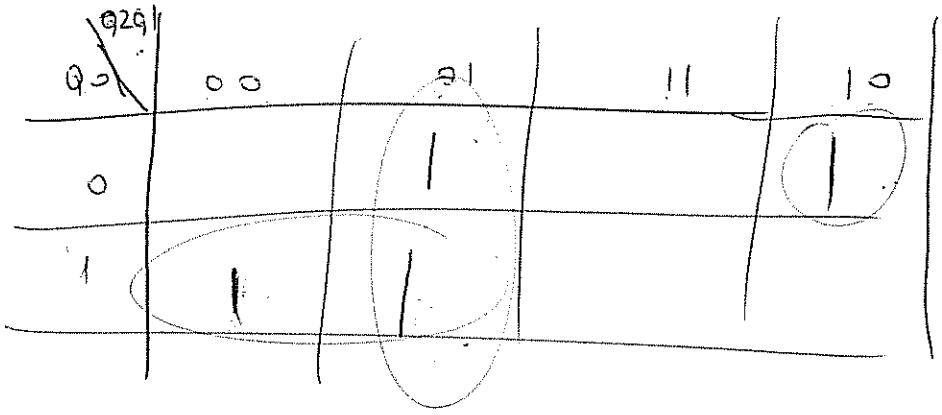
Transition list for T-bird tail-lights state machine.

LA = 1 when L1 + L2 + L3 + LR3

Output table LA

	Q2	Q1	Q0	LA
L1 →	0	0	1	1
L2 →	0	1	1	1
L3 →	0	1	0	1
LR3 →	1	0	0	1

K-map:



$$LA = Q2'.Q0 + Q2'.Q1 + Q2Q1'.Q0'$$

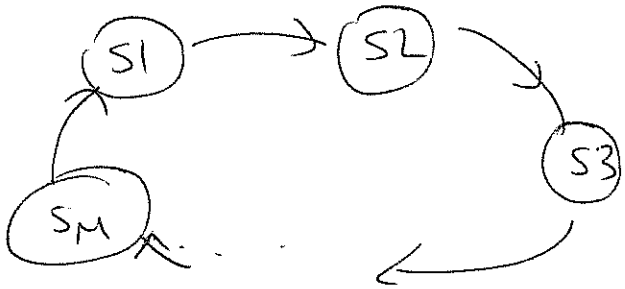
Register: a collection of two or more D flip-flops with a common clock input.

often used to store a collection of related bits.

Counters:

Any clocked sequential circuit with state diagram containing a single cycle.

e.g.



modulo-m counter / divide-by-m counter.

Modulus of a counter: # of states in the cycle.

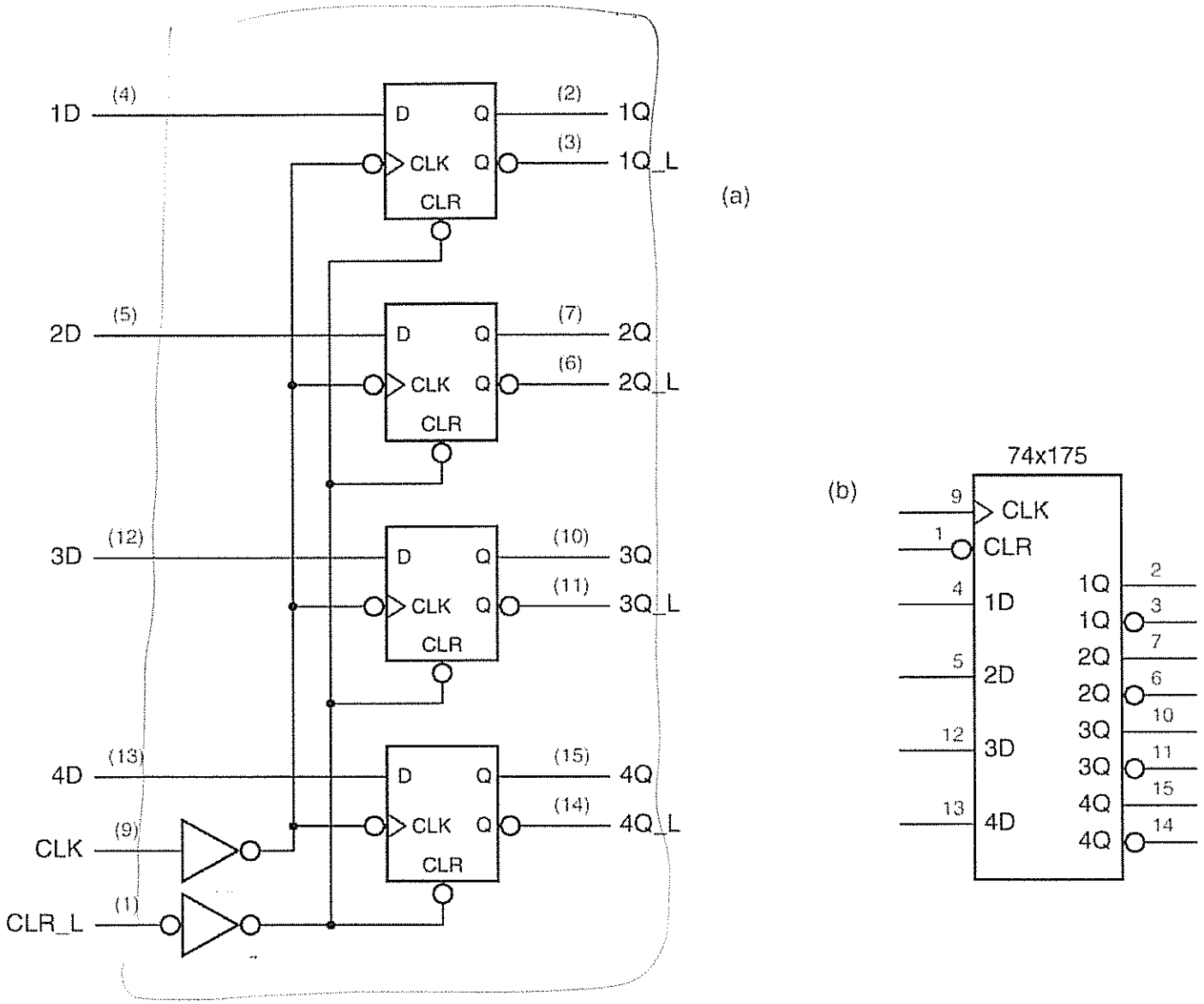


Figure 8-8

The 74×175 4-bit register: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol.

From *Digital Design: Principles and Practices*, Fourth Edition, John F. Wakerly, ISBN 0-13-186389-4.

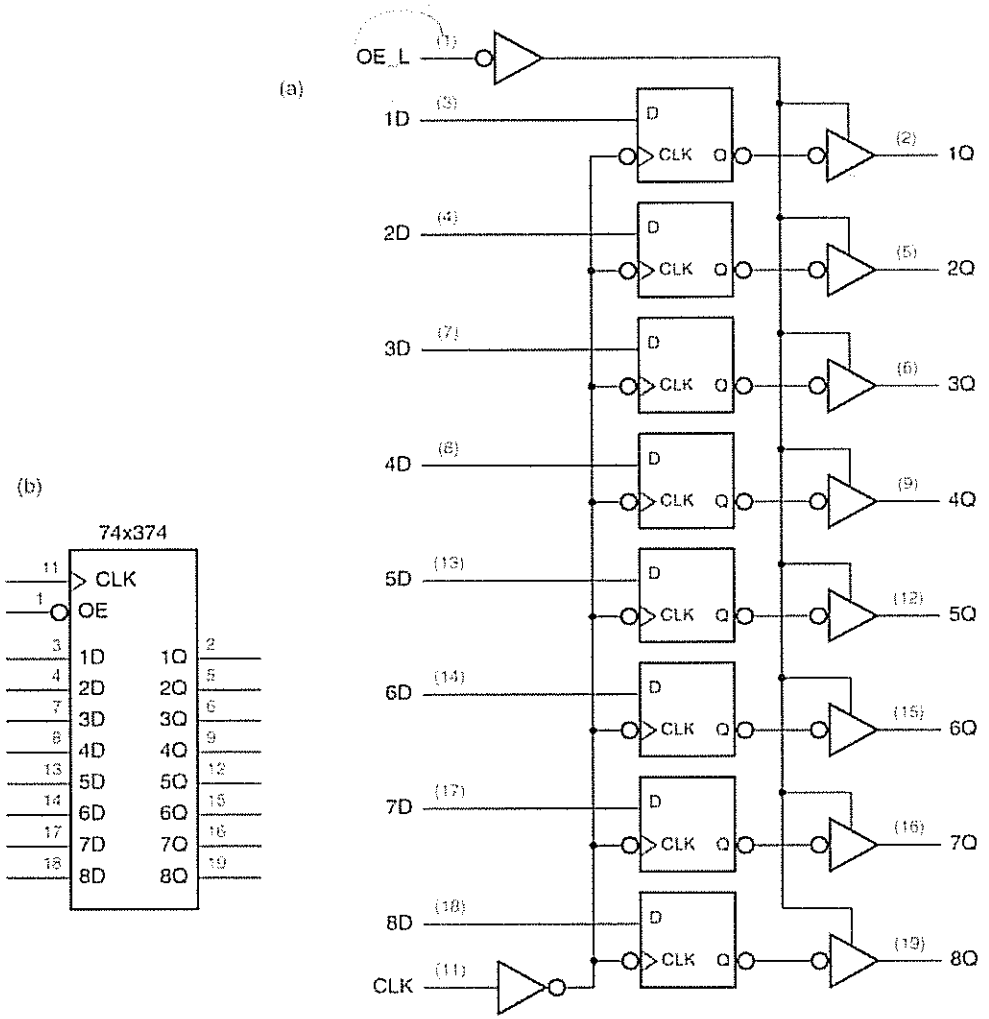
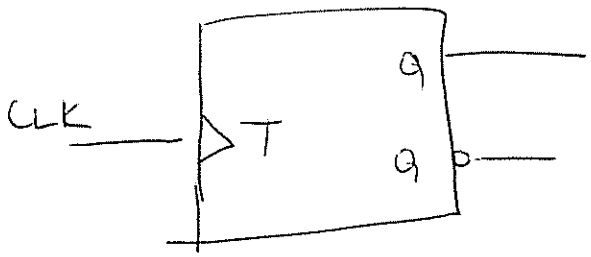


Figure 8-10

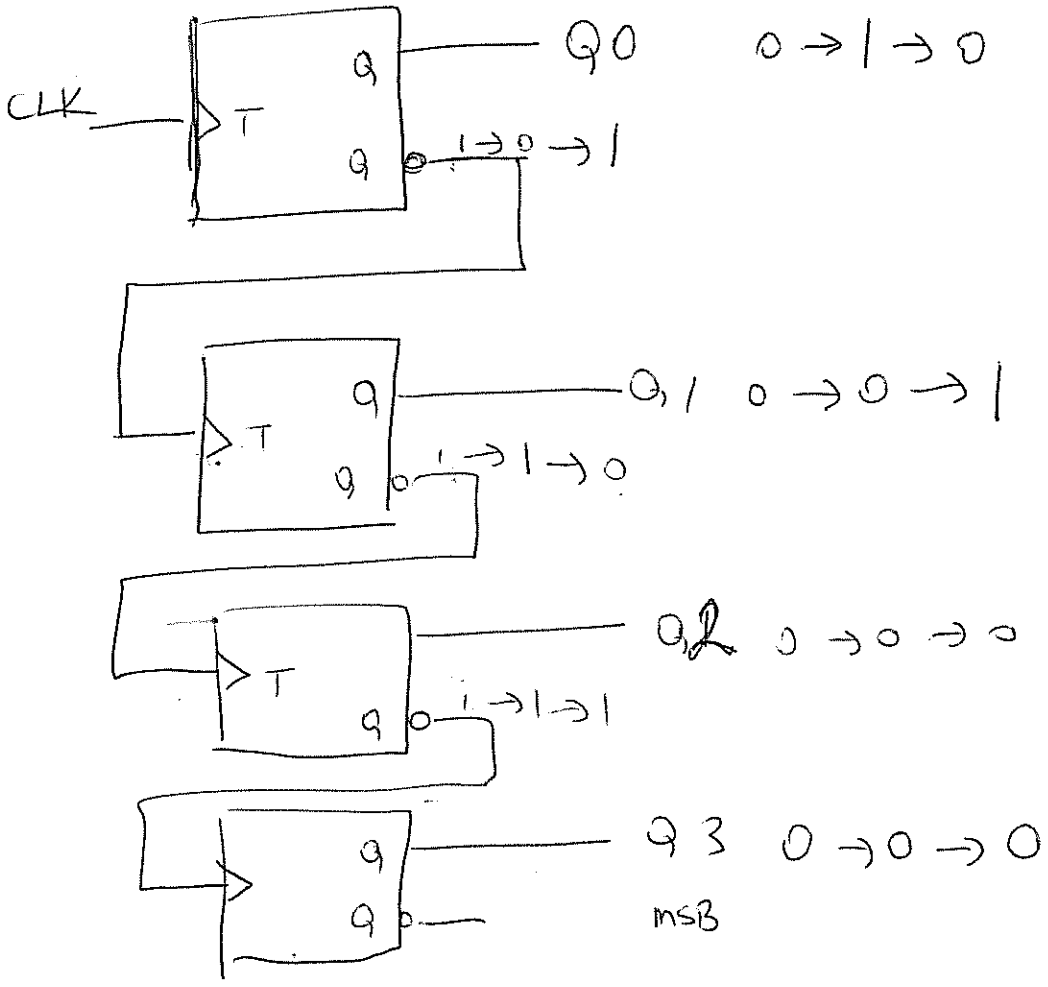
The 74×374 8-bit register: (a) logic diagram, including pin numbers for a standard 20-pin dual in-line package; (b) traditional logic symbol.

From *Digital Design: Principles and Practices*, Fourth Edition, John F. Wakerly, ISBN 0-13-186389-4.

Ripple counters :



T flip-flop changes state (toggles) on every rising edge of its clock input.



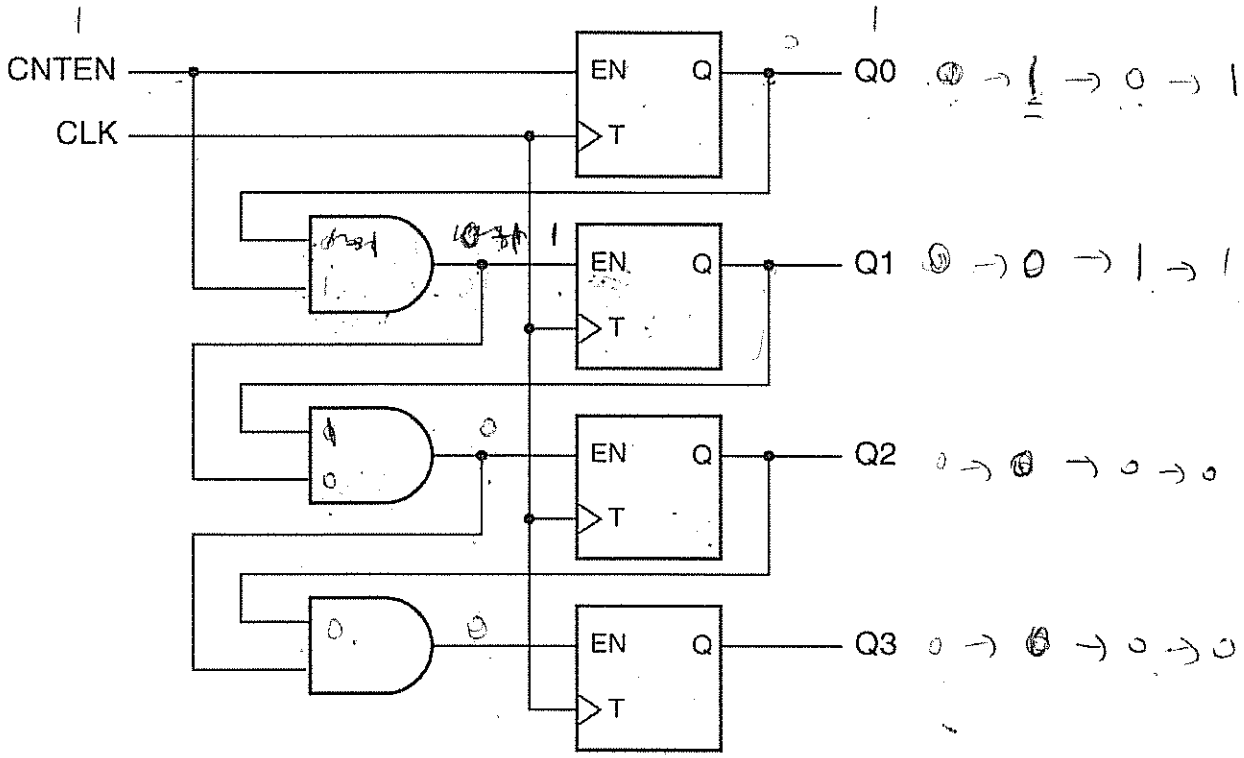


Figure 8-25

A synchronous 4-bit binary counter with serial enable logic.