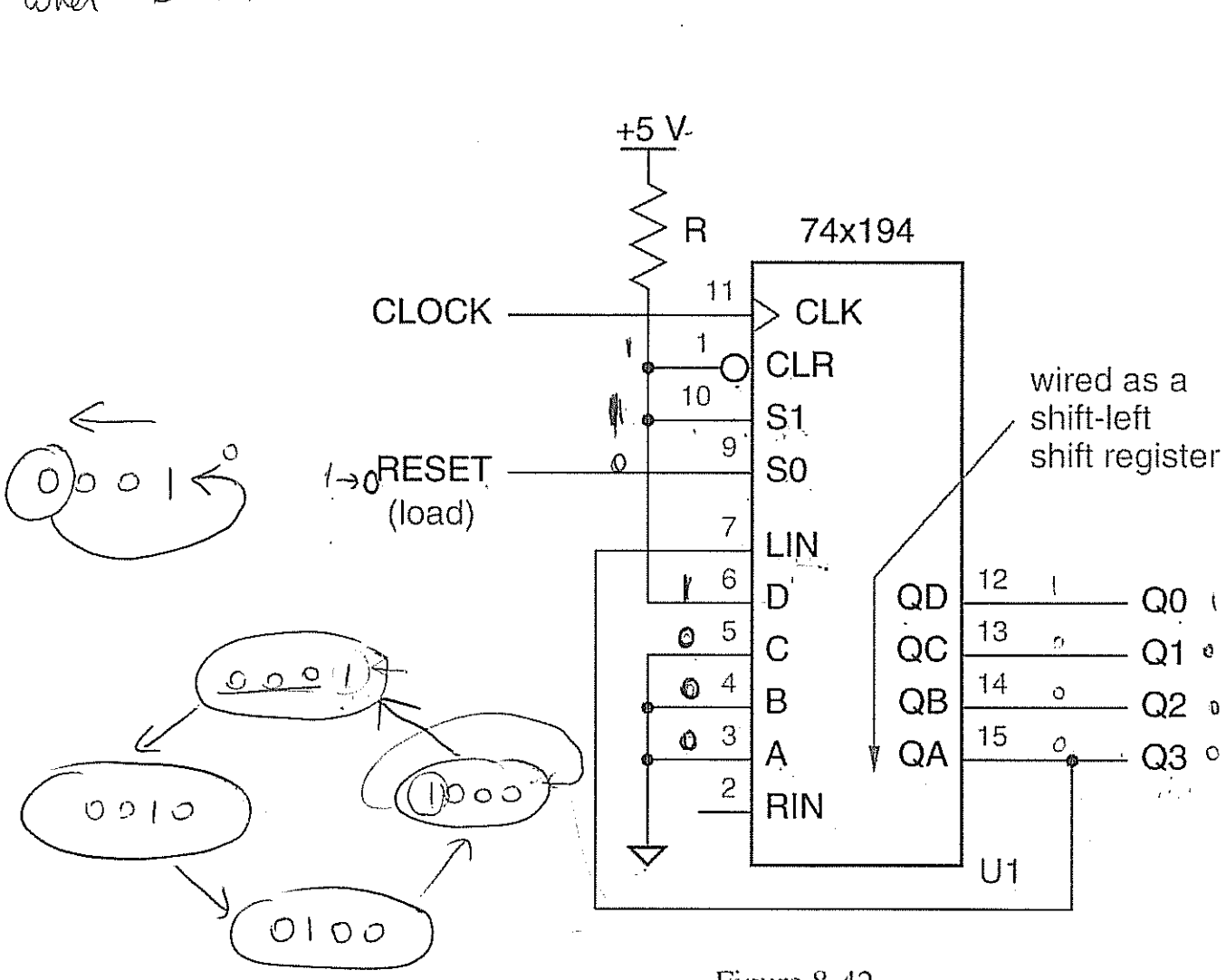
Normally performs a left shift (Reset negated).

When RESET asserted: loads 0001.



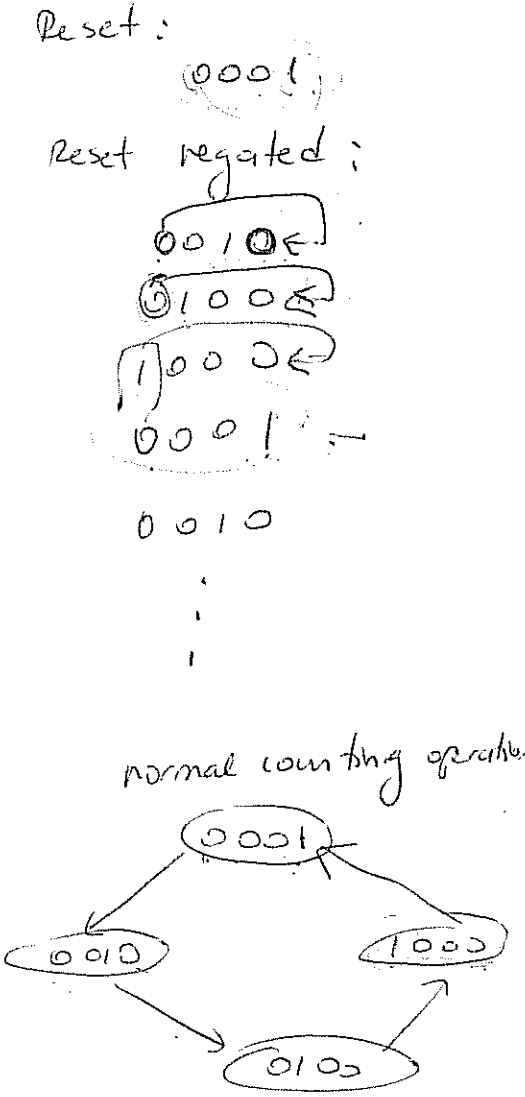


Figure 8-42

Simplest design for a 4-bit, 4-state ring counter with a single circulating 1.

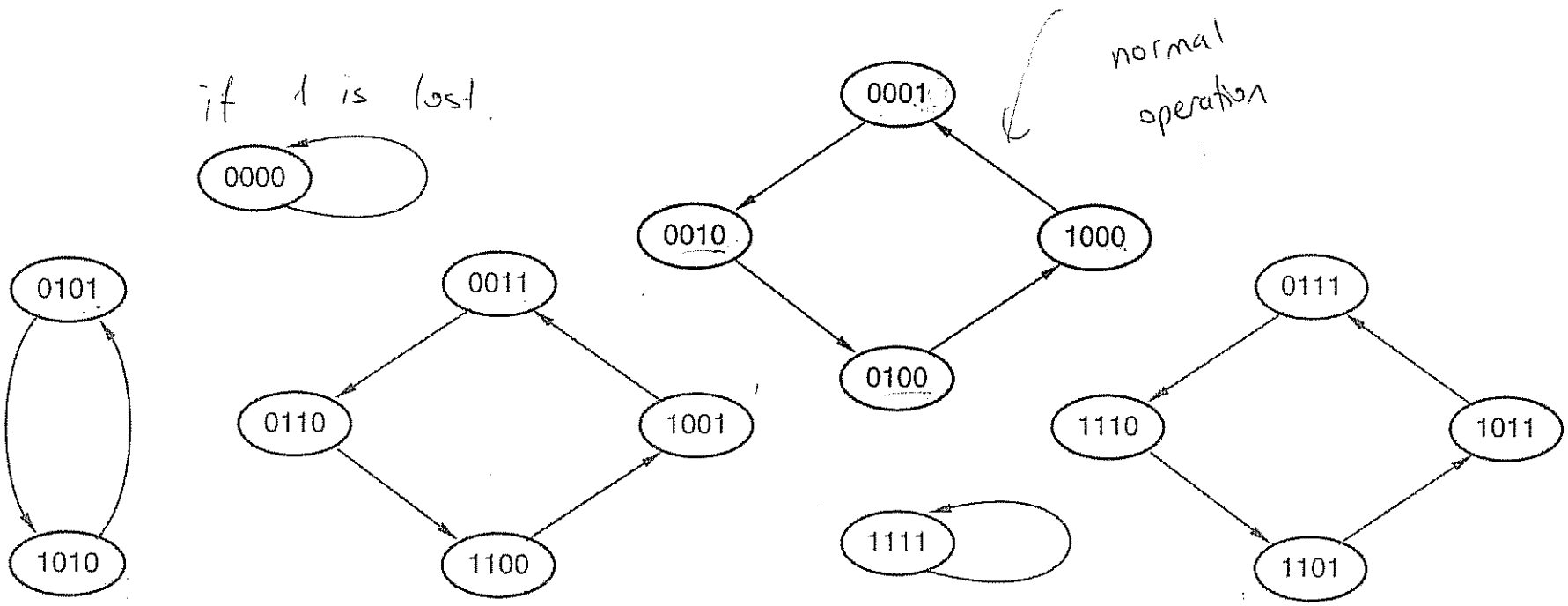


Figure 8-44

State diagram for a simple ring counter.

Uses NOR gate : shifts a 1 into LIN only when the three LSBs are 0.

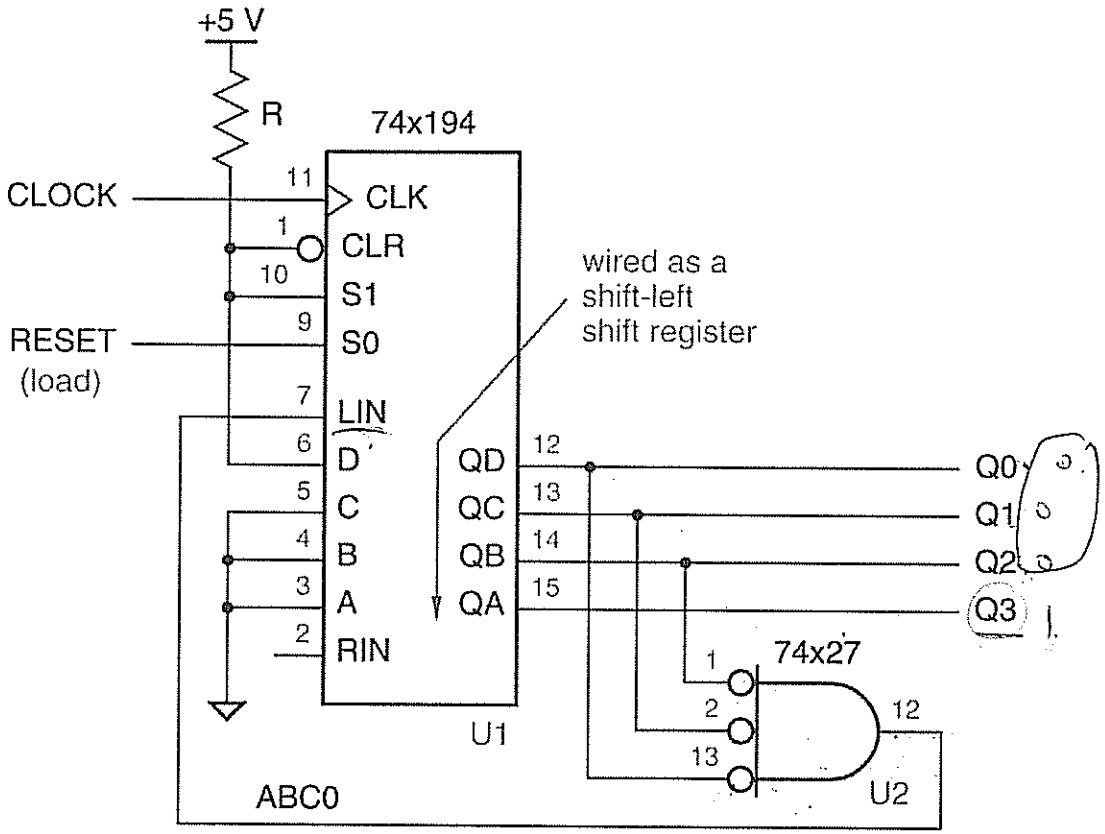


Figure 8-45

Self-correcting 4-bit, 4-state ring counter with a single circulating 1.

an abnormal state corrected within n-1 clock ticks.
in this example within 3 clock ticks.

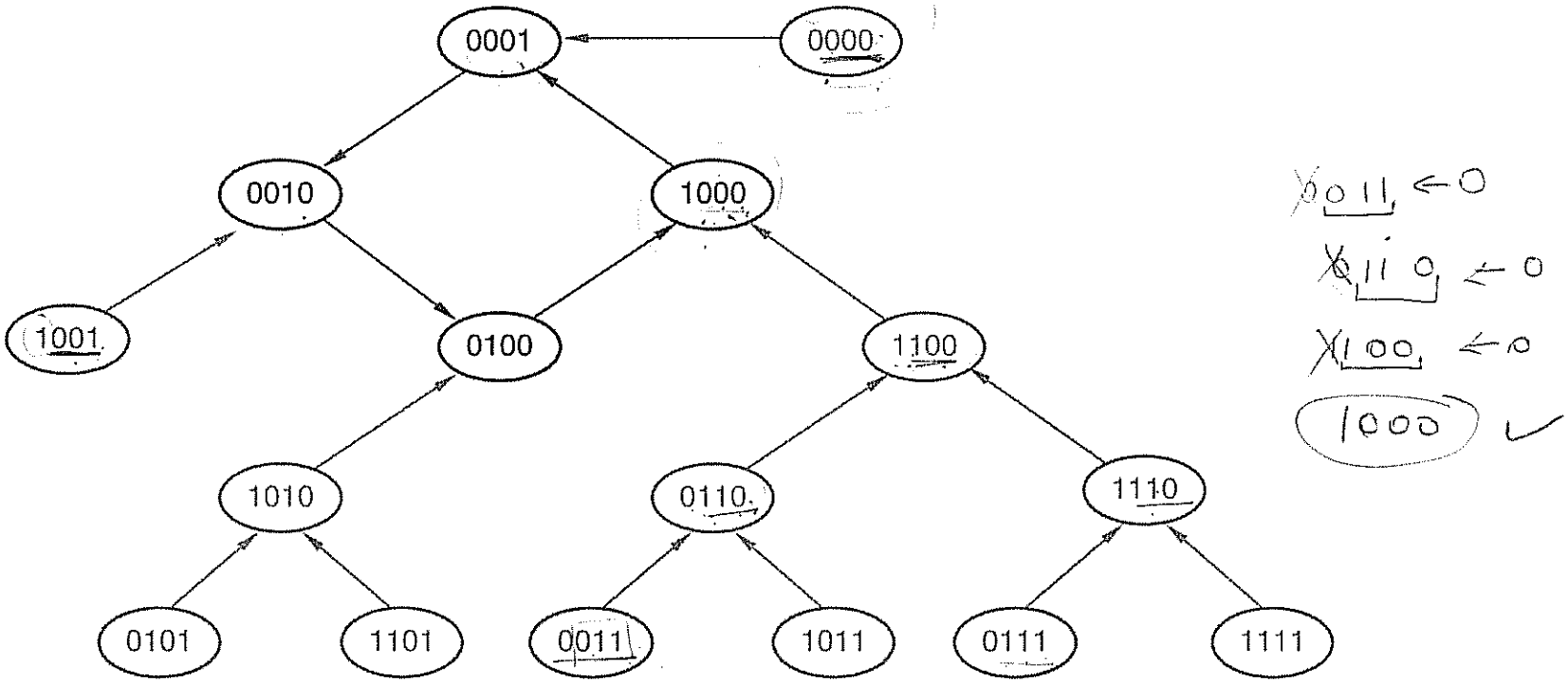


Figure 8-46
State diagram for a self-correcting ring counter.

EECS 281, April 7, 2015

Read-Only Memory (ROM)

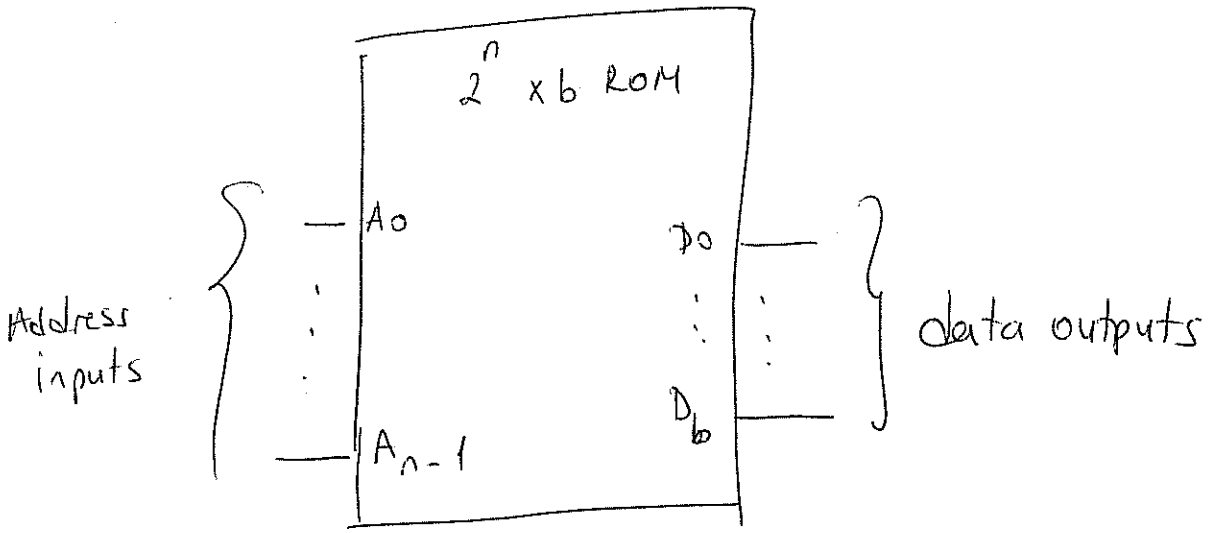
Combinational circuit with n inputs and b outputs.

inputs are called: address inputs

named $A_0, A_1, \ldots, A_{n-1}$

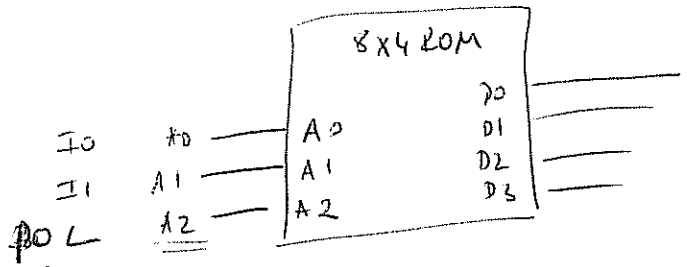
outputs are called: data outputs

named: $D_0, D_1, \ldots, D_{b-1}$



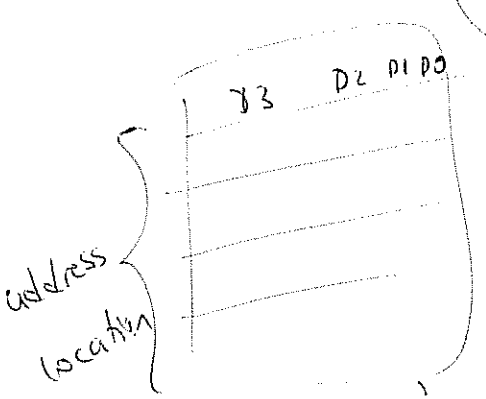
can be stored in $2^3 \times 4$ (8x4) ROM.

can store this truth table in a 8x4 ROM:



Inputs			Outputs			
A2	A1	A0	D3	D2	D1	D0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

truth table for 2-to-4 decoder with output-polarity control.



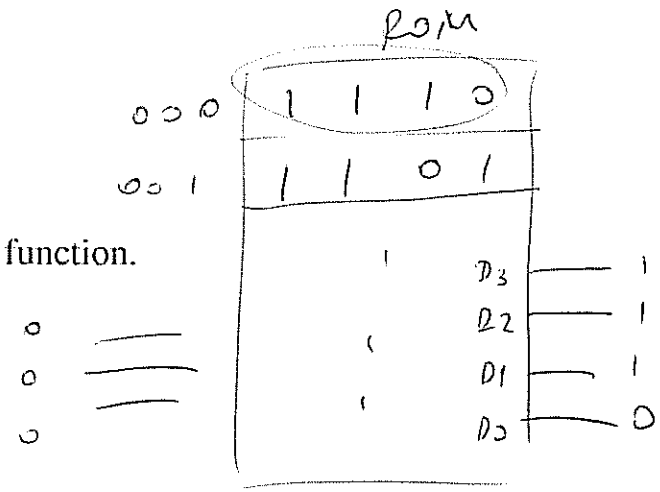


Table 9-1

Truth table for a 3-input, 4-output combinational logic function.

Type	*Technology*	*Read cycle*	*Write cycle*	*Comments*
Mask ROM	NMOS, CMOS	10–200 ns	4 weeks	Write once; low power
Mask ROM	Bipolar	< 100 ns	4 weeks	Write once; high power; low density
PROM	Bipolar	< 100 ns	10–50 μs/byte	Write once; high power; no mask charge
EPROM	NMOS, CMOS	25–200 ns	10–50 μs/byte	Reusable; low power; no mask charge
EEPROM	NMOS	50–200 ns	10–50 μs/byte	10,000–100,000 writes/location limit

Table 9-5

Commercial ROM types.

Stores the truth table of an n-input b~~i~~ output combinational logic function.

ROM's data outputs are equal to the output bits in the truth table row selected by the address inputs.

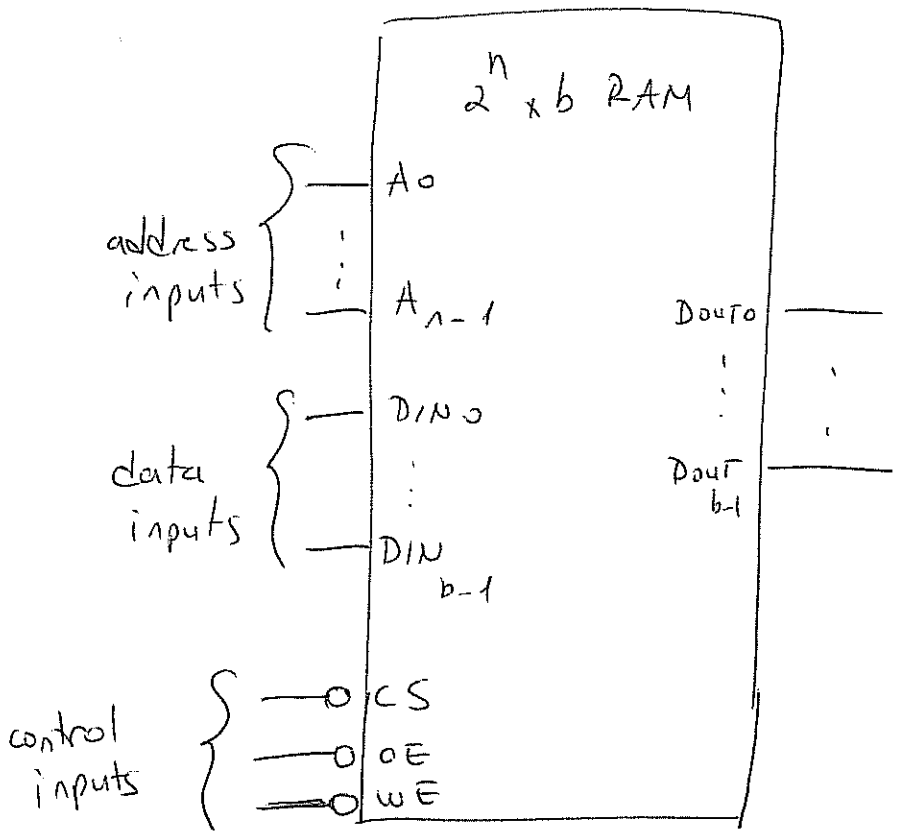
ROM is a nonvolatile memory: contents preserved even if no power is applied.

Read / write Memory (RWM)

Most common: ~~Read~~ Random Access Memories (RAMs)

RAM: time it takes to read or write a bit is independent of bit's location in the RAM.

Volatile memory: loses memory when powered off.



When WE is asserted, data ~~outputs~~ inputs are written into selected memory location.

Read: OE: 0 ← asserted

WE: 1 ← not asserted, write is not enabled.

address bits should contain the address that you are trying to access.

SEL_L asserted : output is stored data.

SEL_L and WR_L asserted : latch open.
New data bit stored.

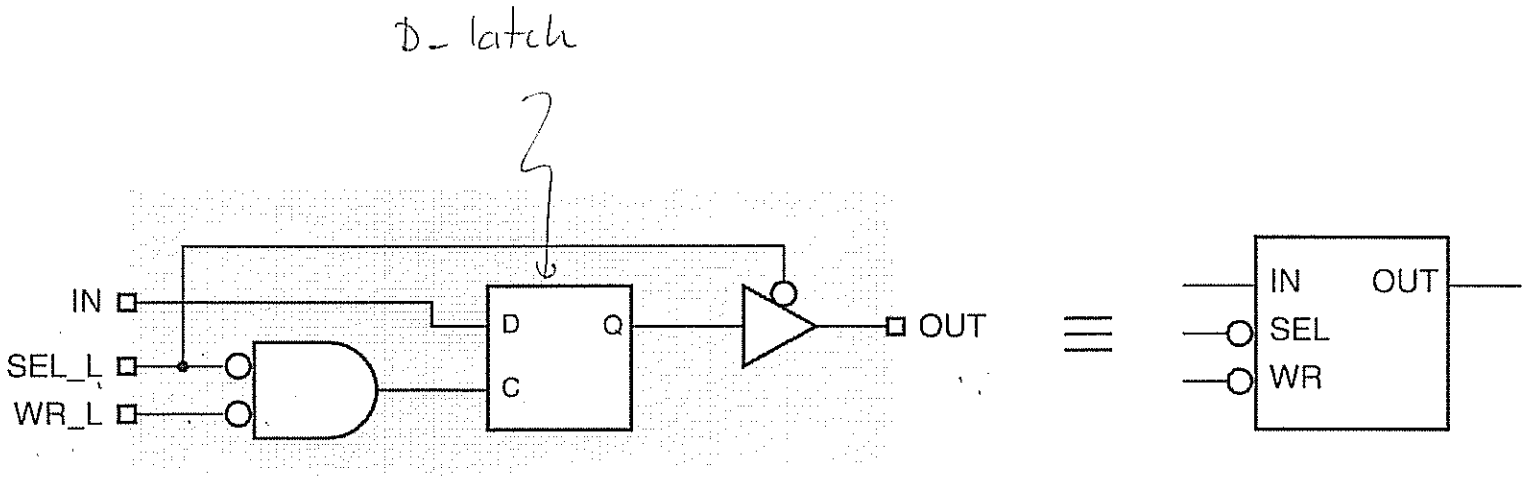


Figure 9-20

Functional behavior of a static-RAM cell.

selects a row to be accessed

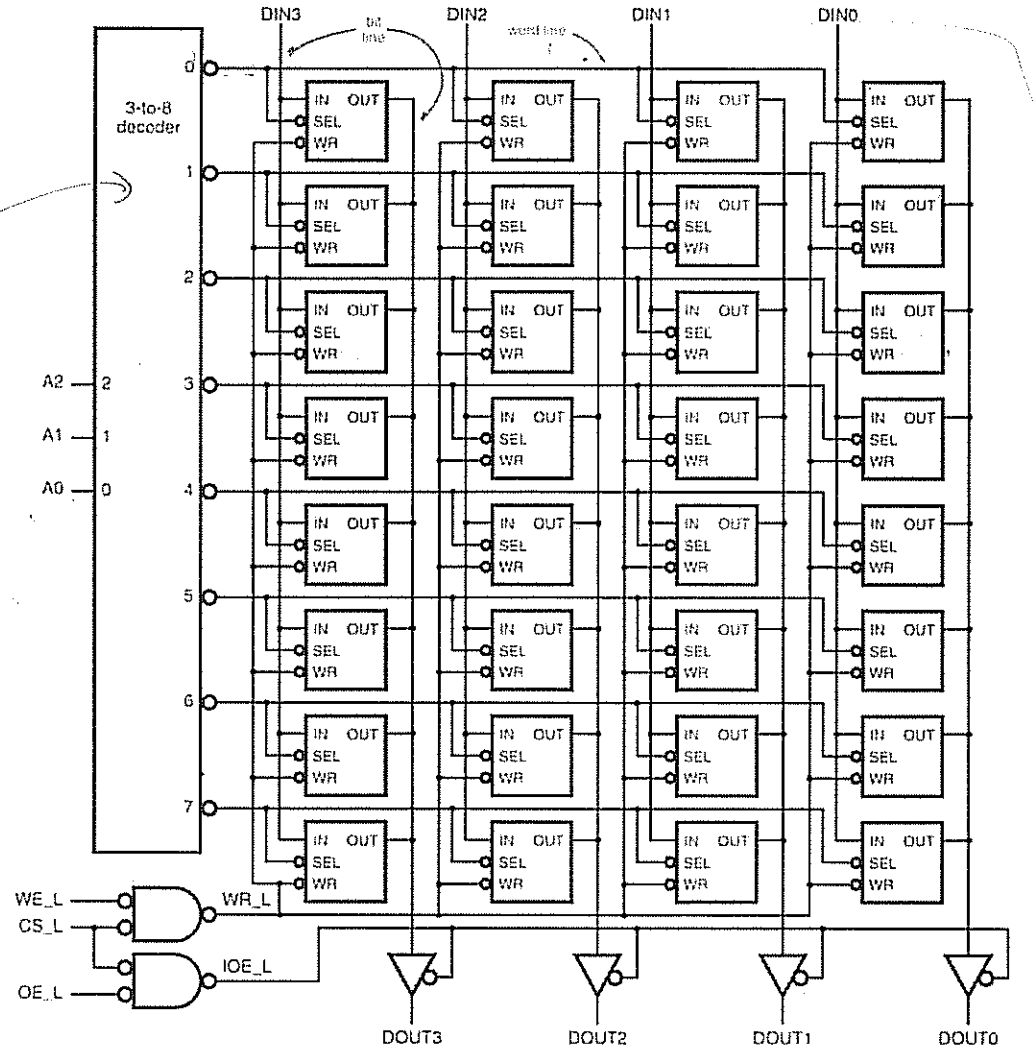


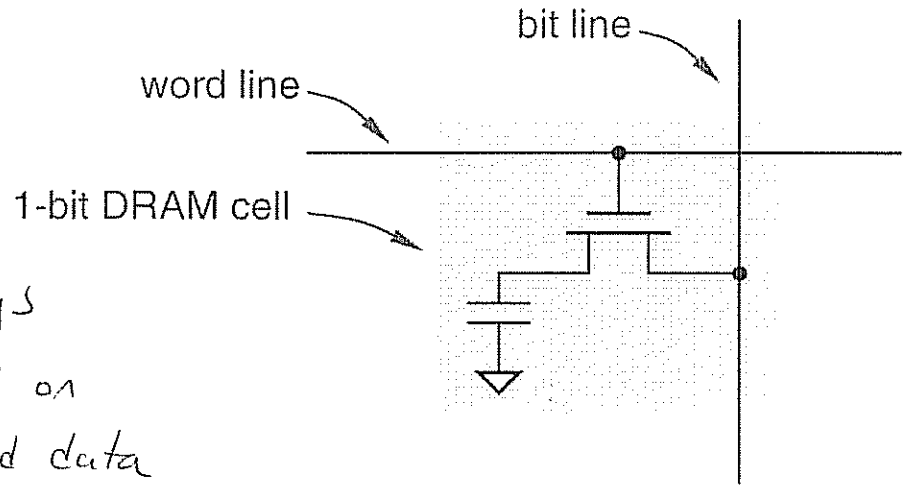
Figure 9-21

Internal structure of an 8 × 4 static RAM.

Accessed by setting word line to HIGH.

To store "1": HIGH voltage placed on bit line ⇒ capacitor charged through an transistor.

To store "0": Low voltage placed on bit line ⇒ capacitor discharges.



Reading a cell destroys original voltage stored on capacitor ⇒ recovered data must be written back after reading!

Figure 9-31

Storage cell for one bit in a DRAM.

To read: Bit line precharged to a voltage halfway between High and Low. word line set to HIGH. If capacitor voltage is high (low), precharged bit one pulled slightly higher (lower). Sense amplifier detects this change, and recovers a 1 (or 0).

The Guessing Game

Four inputs G1 - G4 connected to push buttons

Four outputs L1 - L4 connected to lamps / LEDS located near like-numbered push buttons.

ERR output connected to a red lamp.

Normal operation: L1 - L4: 1-out-of 4 pattern.

at each clock tick, pattern rotates by one position.

Guess: by pressing a push button. G1-G4

If $G_i = L_i \Rightarrow$ stop the game goto OK state

$G_i \neq L_i \Rightarrow$ goto ERR

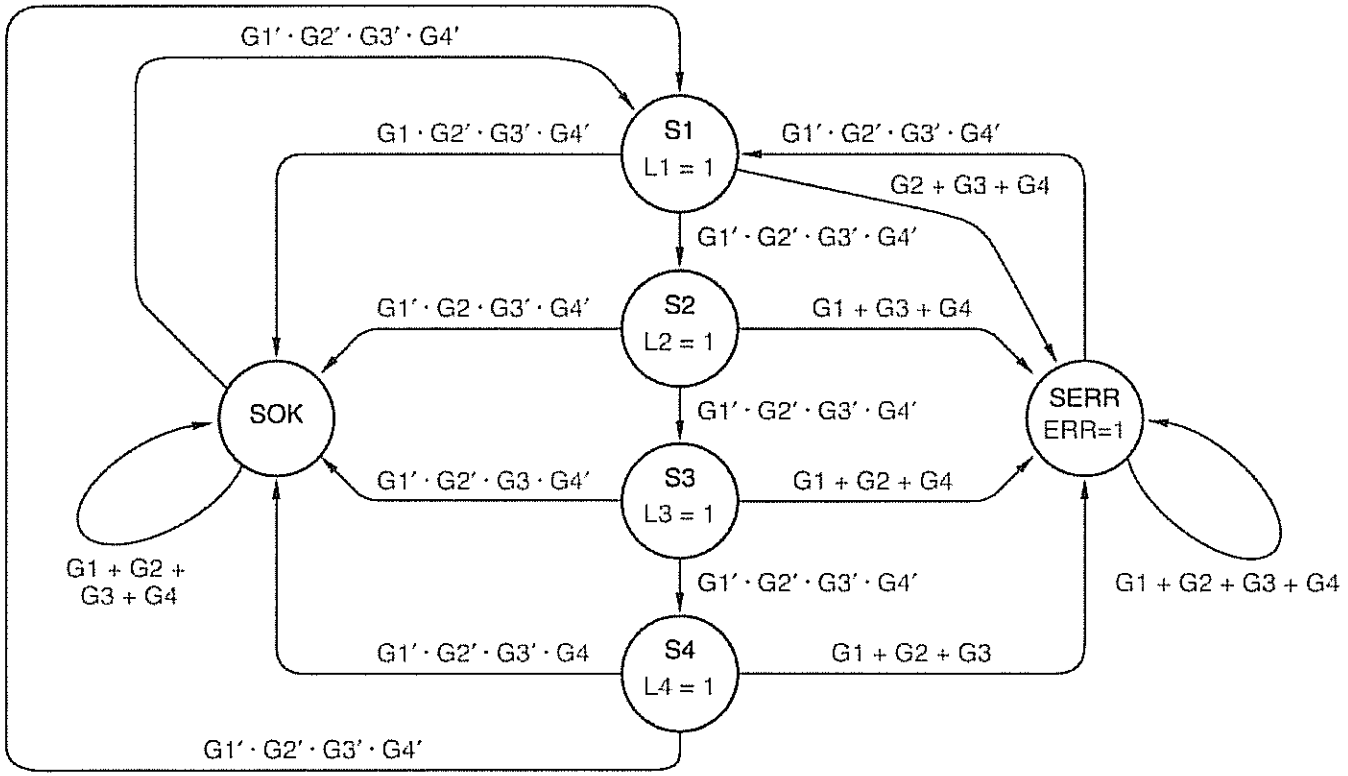


Figure 7-60

Correct state diagram for the guessing game.