EECS 281, March 3, 2015

Note. $A + A'CD$

Adders

Simplest adder: Half Adder

adds two 1-bit operands X an Y.

produces a 2-bit sum

Low order bit of the sum may be named half sum (HS), high order bit may be named carry out (CO).

$$HS = X \oplus Y = XY' + X'Y$$

$$CO = X \cdot Y$$

Full adder

inputs: addend bit inputs

carry in input CI

Cin	X	Y	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

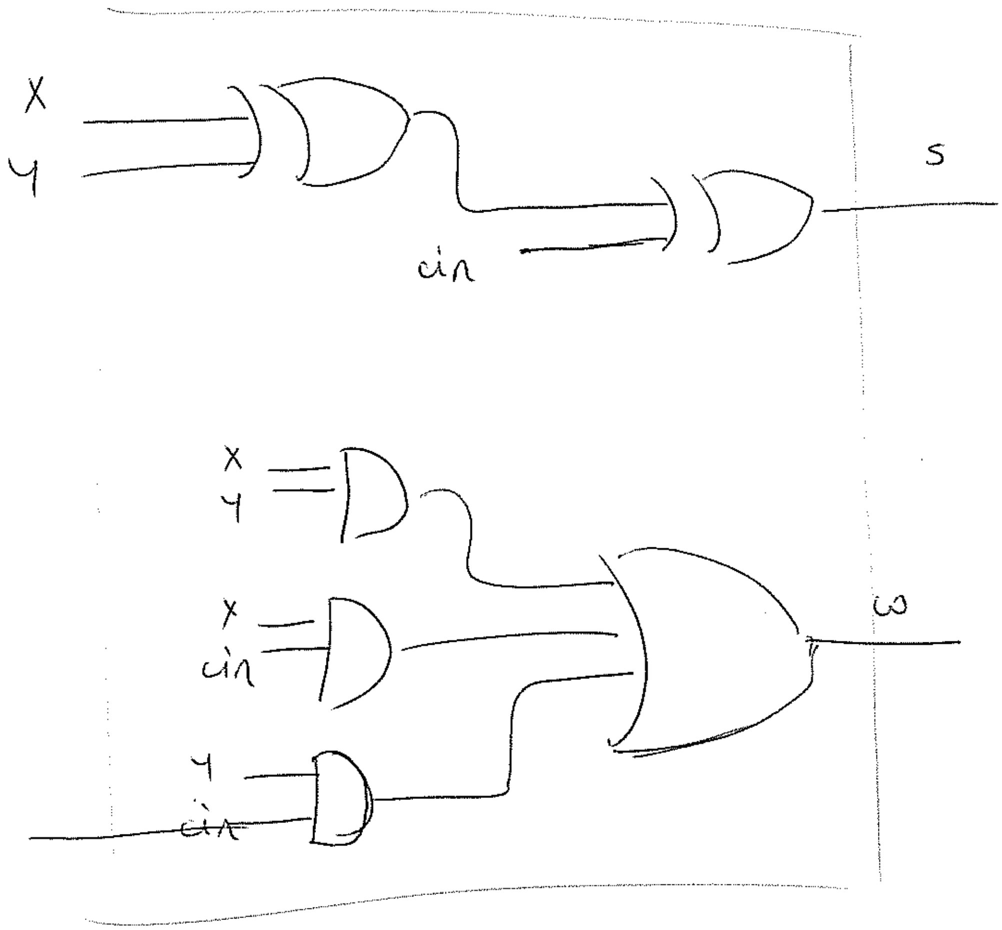
$$S = X \oplus Y \oplus CIN$$

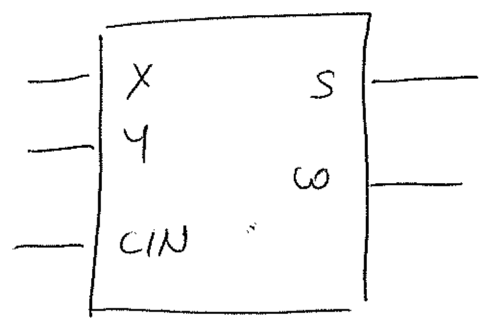
$$= X \cdot Y' \cdot CIN' + X' \cdot Y \cdot CIN' + X'Y'\,CIN + X \cdot Y \cdot CIN$$

$$CO = XY + X\,CIN + Y \cdot CIN$$

S = 1 if odd number of inputs are 1.

CO = 1 if two or more inputs are 1.





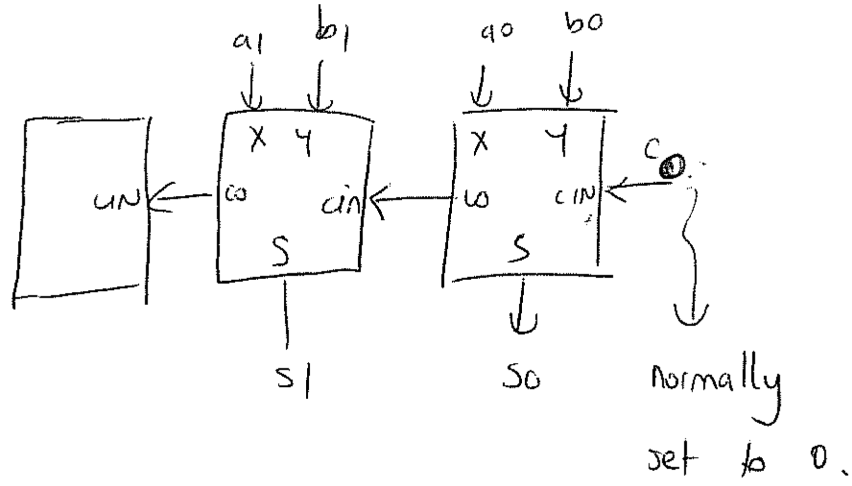
Full adder

Ripple Adders:

Two n-bit binary words are added using ripple adder: cascade of n full-adder stages, each handles one bit.

a3 a2 a1 a0
b3 b2 b1 b0

e.g. 4-bit ripple adder!



Subtractors

Binary adder can perform unsigned subtraction operation $X - Y$ by performing

$$X + \overline{Y} + 1$$

bit-wise complement of Y

use an adder with inputs
X, $\overline{Y}$ and $CIN = 1$.

Three-state Devices

Two normal states for logic outputs: LOW and HIGH

Some outputs have a third electrical state that is not a logic state: high-impedance, hi-Z or floating state.

if not all of the EN are asserted ⇒ none of the three-state buffers are enabled ⇒ SDATA undefined.

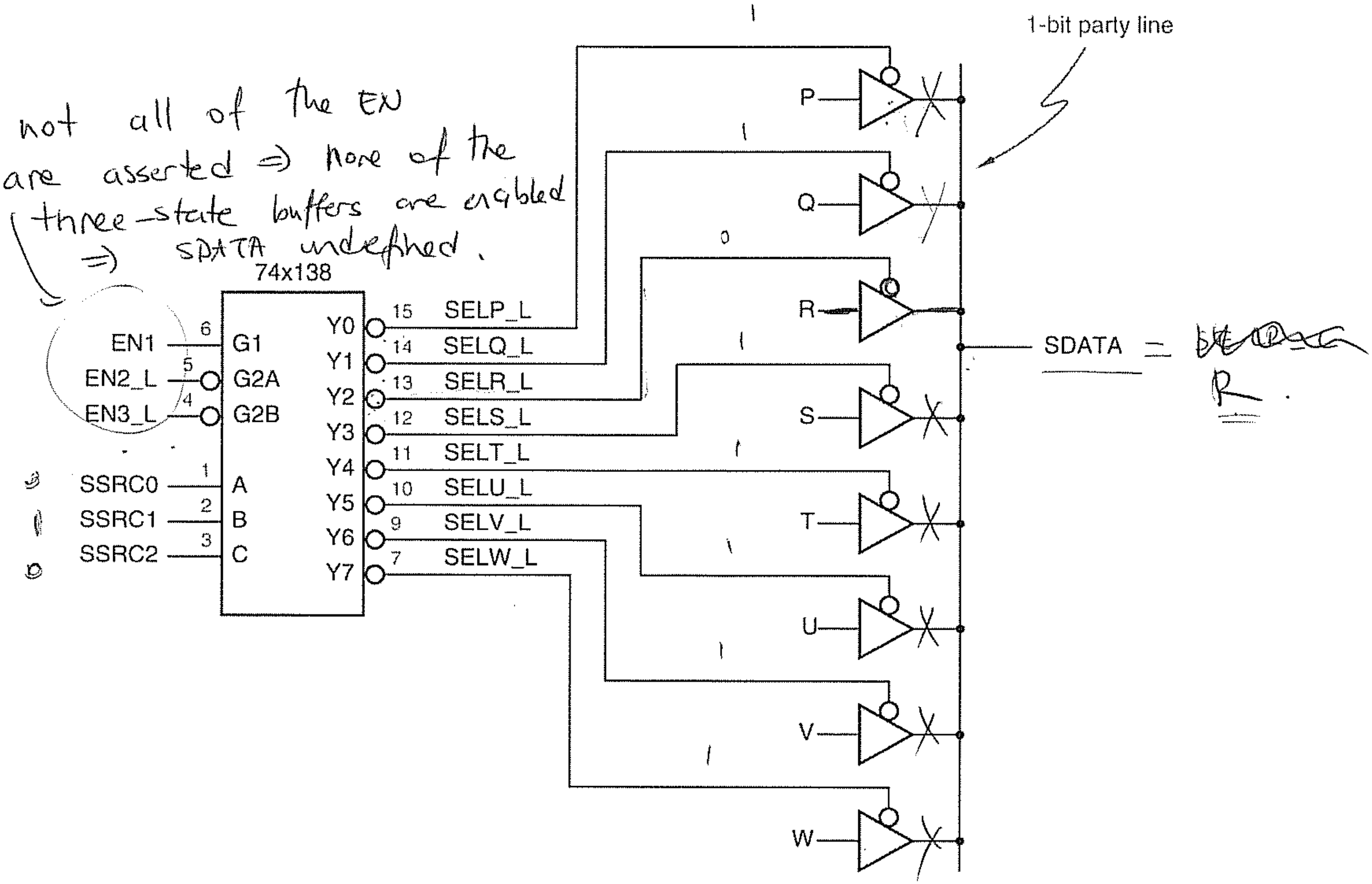


Figure 6-52

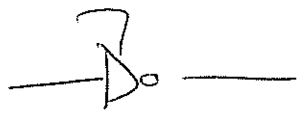
Eight sources sharing a three-state party line.

In Hi-Z state, output behaves as if it isn't even connected to the circuit.

Three-State Buffers

noninverting buffer / active high enable

" " / active low enable

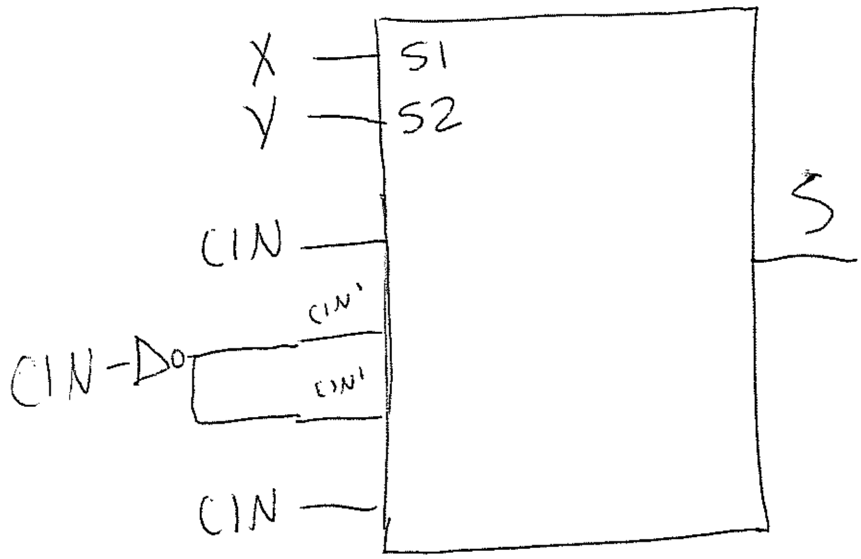


inverting / active high enable

" / " low "

Example: Design a circuit using only a 4 input 1 bit multiplexer with select inputs and an inverter for the sum output of a full adder.

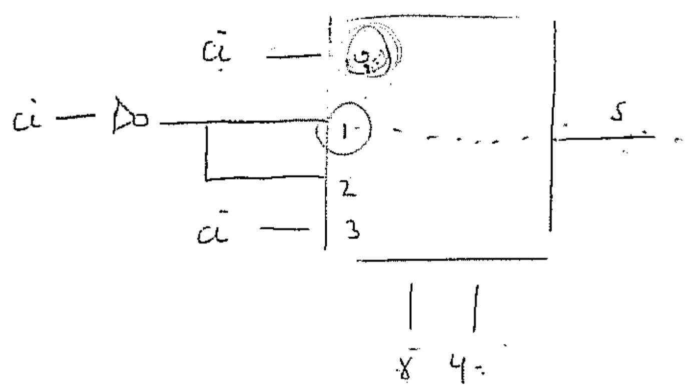
CIN	X	Y	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

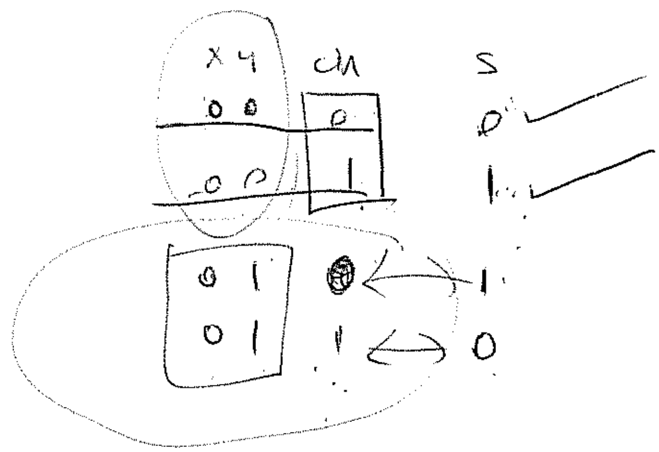


Q2. (30 pts.) a. Write the truth table for a full adder.

x	y	ci	s	co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

b. Design a circuit using only a 4x1 multiplexer with two select inputs and an inverter for the sum output of a full adder.





Q2. (20 pts.) a. Using a truth table, show that $a \cdot b + a \cdot c + b \cdot c = a \cdot b + (a \oplus b) \cdot c$

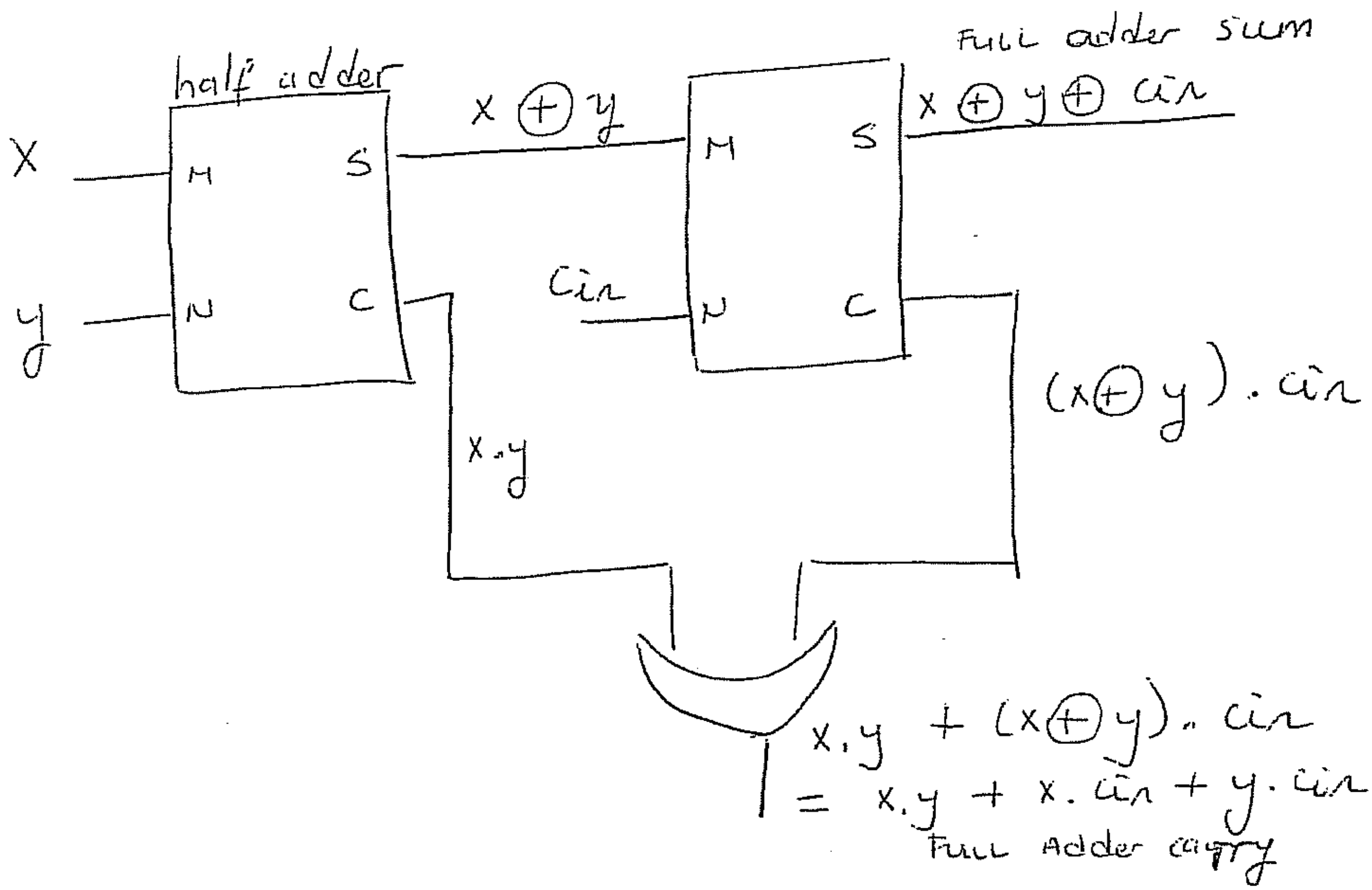
a b c	ab + ac + bc	ab + (a ⊕ b) . c
0 0 0	0	0
0 0 1	0	0
0 1 0	0	0
0 1 1	1	1
1 0 0	0	0
1 0 1	1	1
1 1 0	1	1
1 1 1	1	1

b. Implement a full adder using two half adders and a single combinational logic gate.

The half adder output equations for inputs M and N are given as:

Sum: $S = M \oplus N$

Carry: $C = M \cdot N$

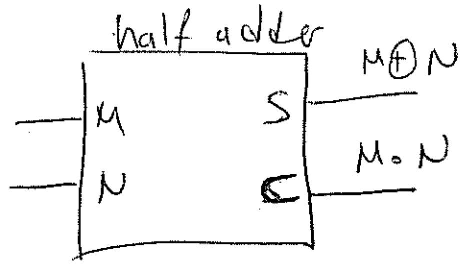


Example: Implement a full adder using two half adders and a single gate.

Half adder equations:

$$S = M \oplus N$$

$$C = M \cdot N$$



$$a \cdot b + a \cdot c + b \cdot c = a \cdot b + (a \oplus b) \cdot c$$