

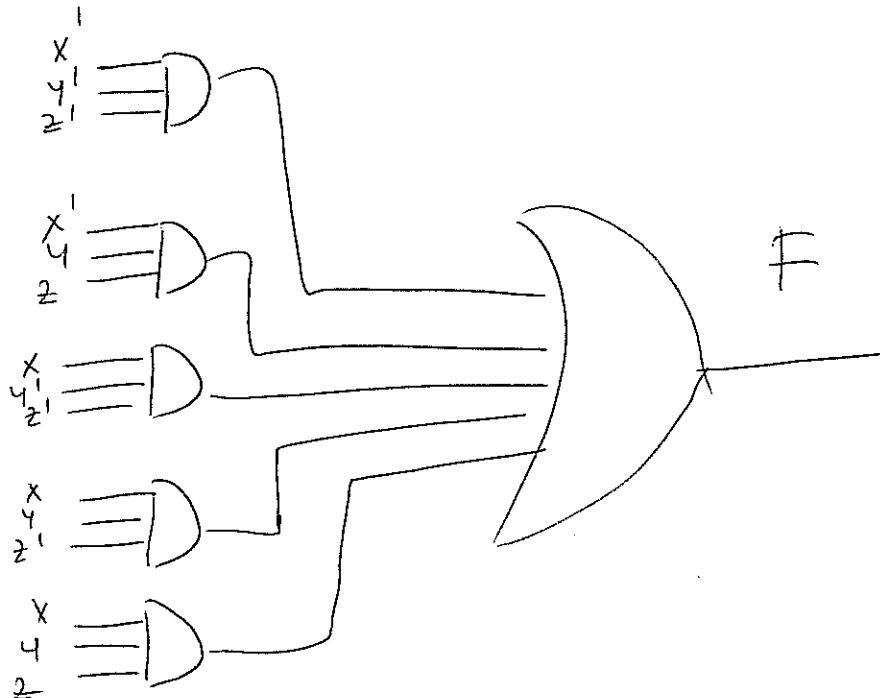
EECS 281, February 3, 2015

example:

| Row | X | Y | Z | F | minterms | maxterms |
|-----|---|---|---|---|------------------------|---------------|
| 0 | 0 | 0 | 0 | 1 | $X' \cdot Y' \cdot Z'$ | |
| 1 | 0 | 0 | 1 | 0 | | $X + Y + Z'$ |
| 2 | 0 | 1 | 0 | 0 | | $X + Y' + Z$ |
| 3 | 0 | 1 | 1 | 1 | $X' \cdot Y \cdot Z$ | |
| 4 | 1 | 0 | 0 | 1 | $X \cdot Y' \cdot Z'$ | |
| 5 | 1 | 0 | 1 | 0 | | $X' + Y + Z'$ |
| 6 | 1 | 1 | 0 | 1 | $X \cdot Y \cdot Z'$ | |
| 7 | 1 | 1 | 1 | 1 | $X \cdot Y \cdot Z$ | |

$$F = \sum_{X,Y,Z} (0, 3, 4, 6, 7)$$

$$= X' \cdot Y' \cdot Z' + X' \cdot Y \cdot Z + X \cdot Y' \cdot Z' + X \cdot Y \cdot Z' + X \cdot Y \cdot Z$$



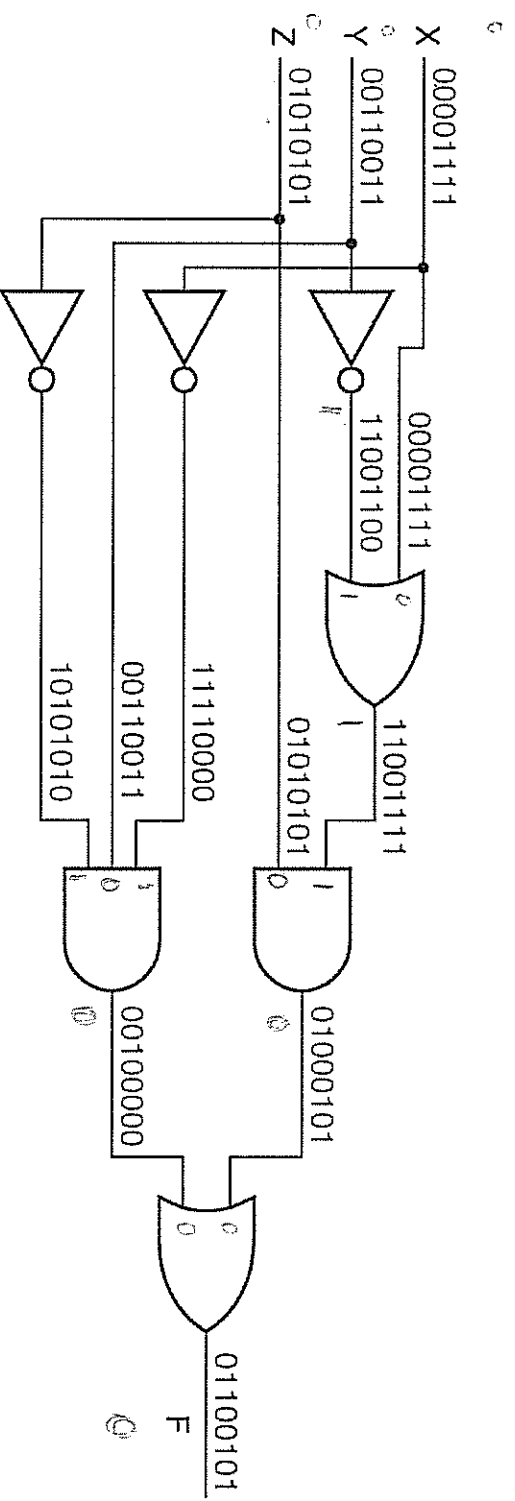


Figure 4-10

Gate outputs created by all input combinations.

| <i>Row</i> | X | Y | Z | F |
|------------|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 0 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 0 |
| 7 | 1 | 1 | 1 | 1 |

Table 4-7

Truth table for the logic circuit of Figure 4-9.

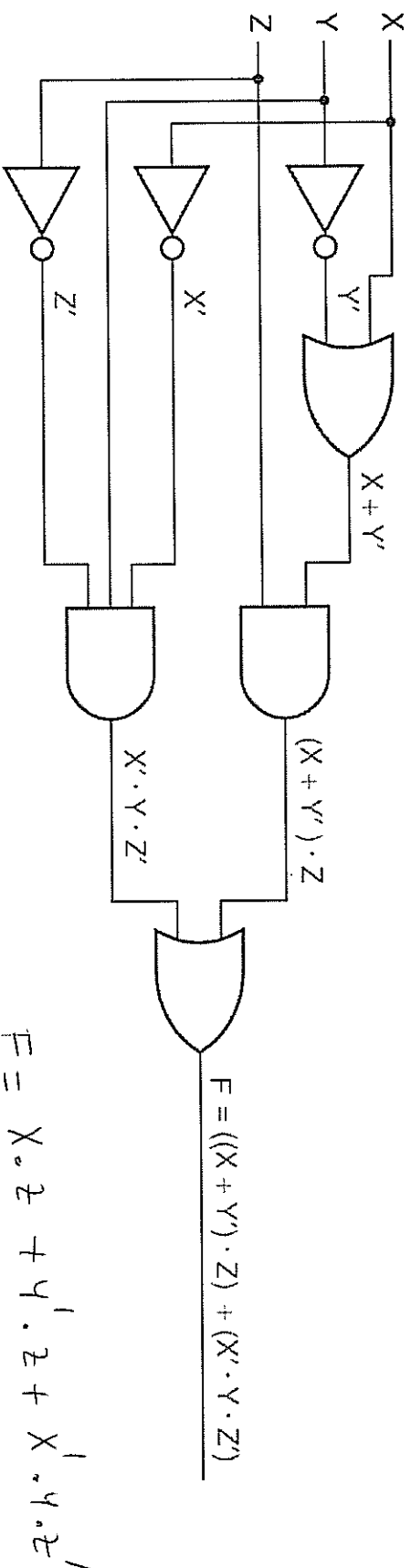


Figure 4-11

Logic expressions for signal lines

Canonical product: product of maxterms
corresponding to input combinations
for which function produces a 0-output.

$$F = \prod_{x,y,z} (1, 2, 5)$$

$$F = \sum_{x,y,z} (0, 3, 4, 6, 7)$$

$$F = (X + Y + Z') \cdot (X + Y' + Z) \cdot (X' + Y + Z')$$

Example: The ALARM output is 1 if the
PANIC input is 1, or if the
ENABLE input is 1 and the EXITING input
is 0, and the house is not SECURE;
The house is SECURE if the WINDOW,
DOOR and GARAGE inputs are all 1.

$$ALARM = PANIC + ENABLE \cdot EXITING' \cdot SECURE'$$

$$SECURE = WINDOW \cdot DOOR \cdot GARAGE$$

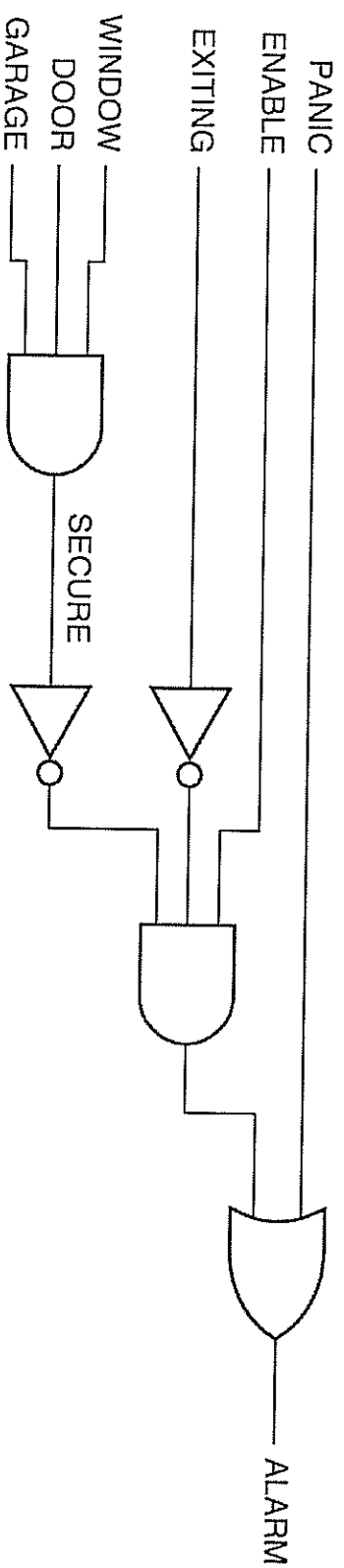
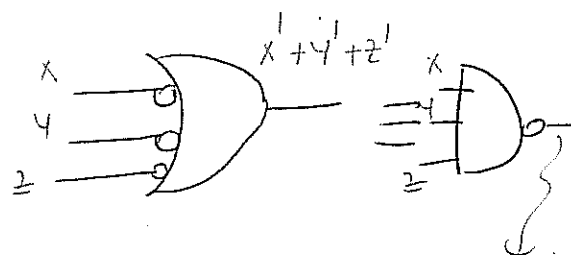
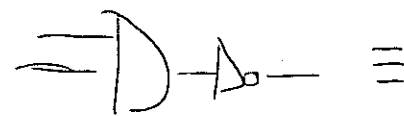
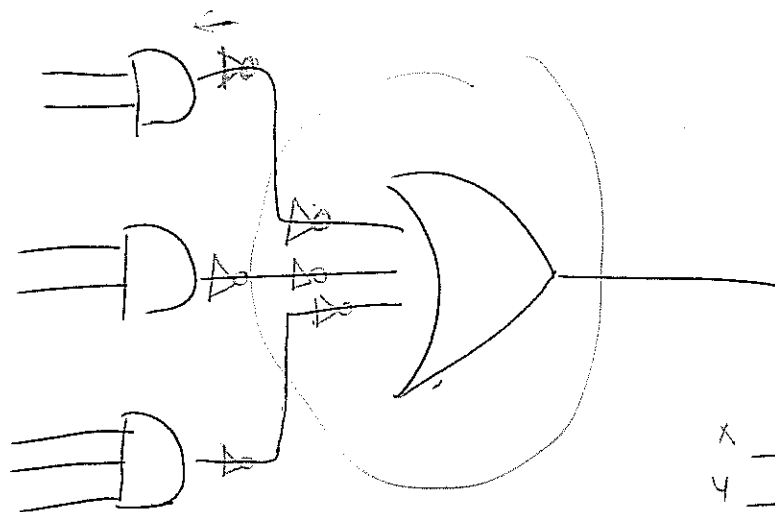
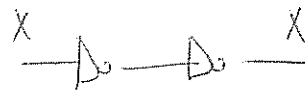
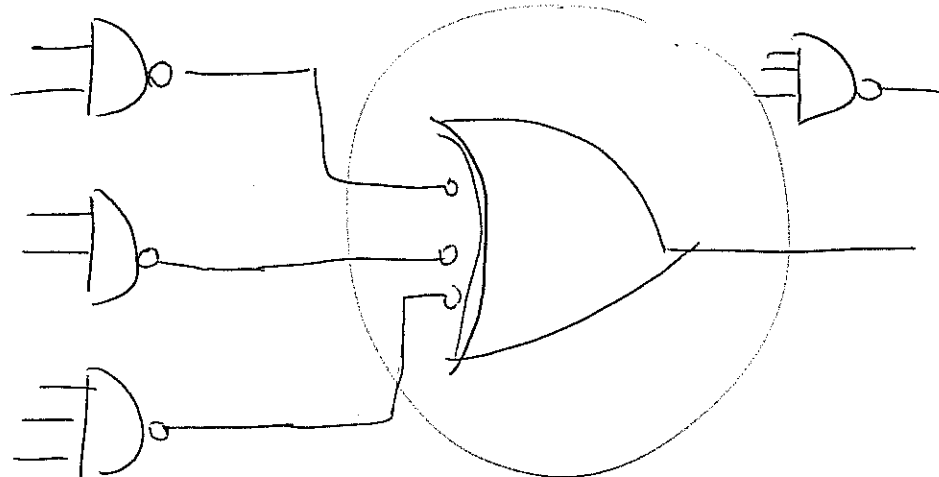


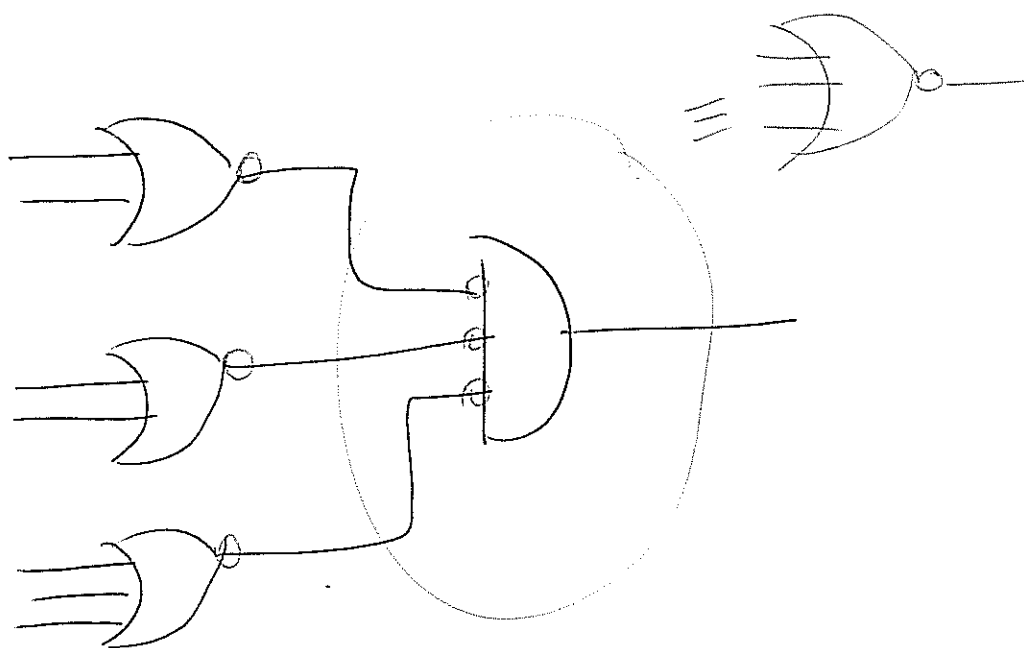
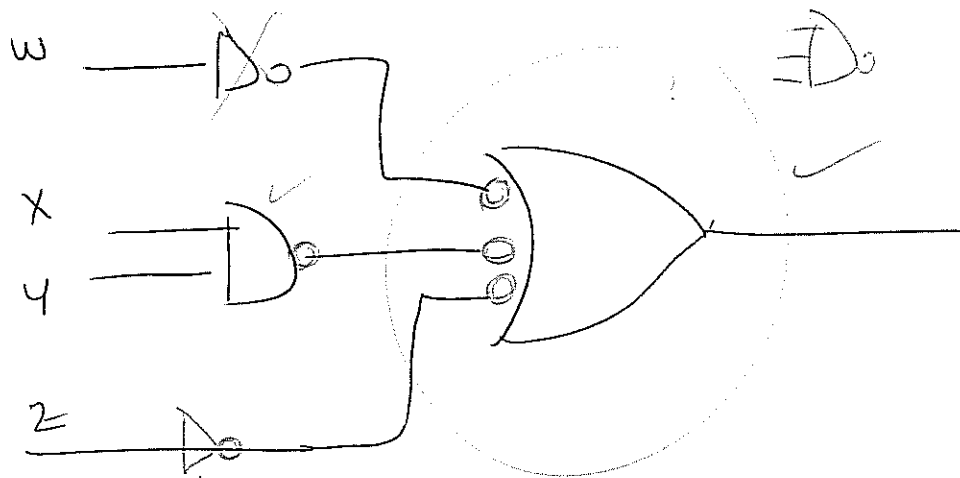
Figure 4-19

Alarm circuit derived from logic expression.



$$(X \cdot Y \cdot Z)' = X' + Y' + Z'$$





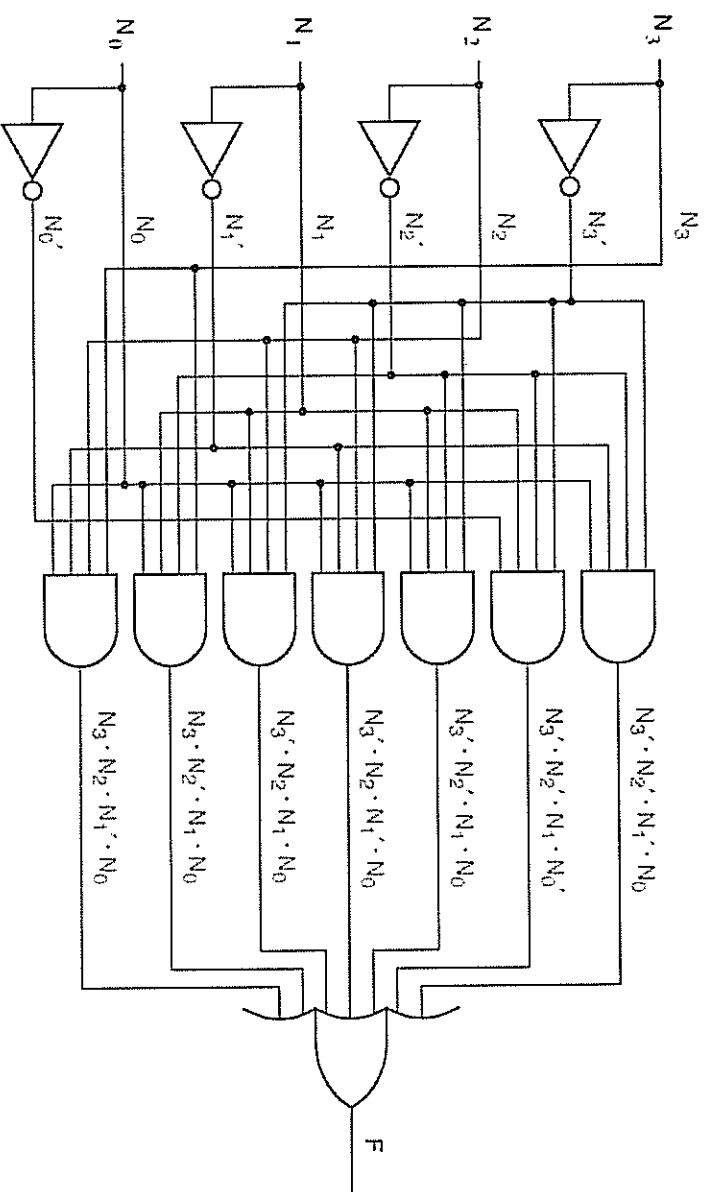


Figure 4-18

Canonical-sum design for 4-bit prime-number detector.

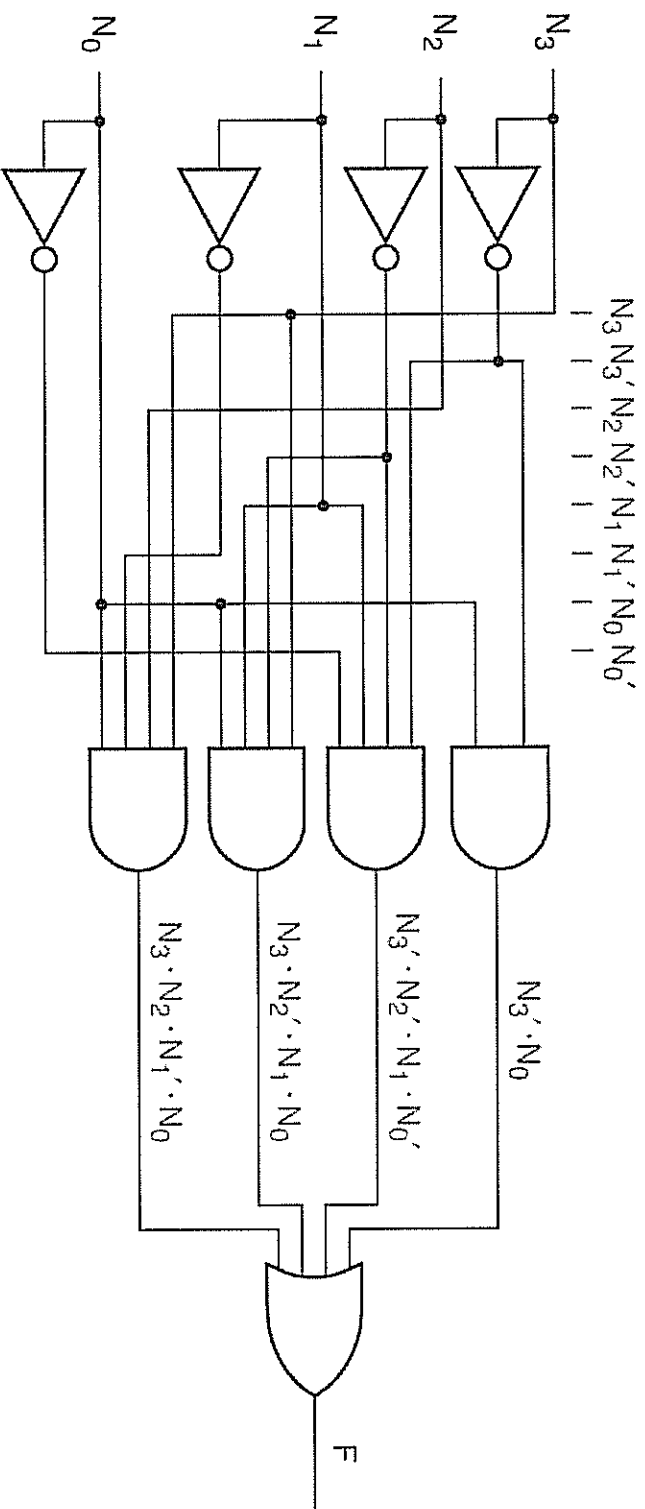


Figure 4-25

Simplified sum-of-products realization for 4-bit prime-number detector.

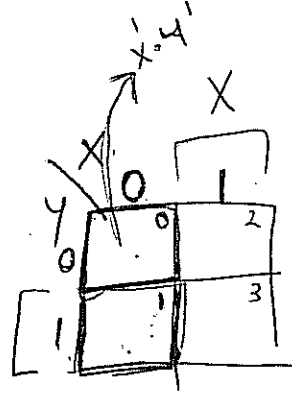
Karnaugh Maps

Graphical representations of the truth table.

For n -input logic function: array with 2^n cells, one for each possible input combination or minterm.

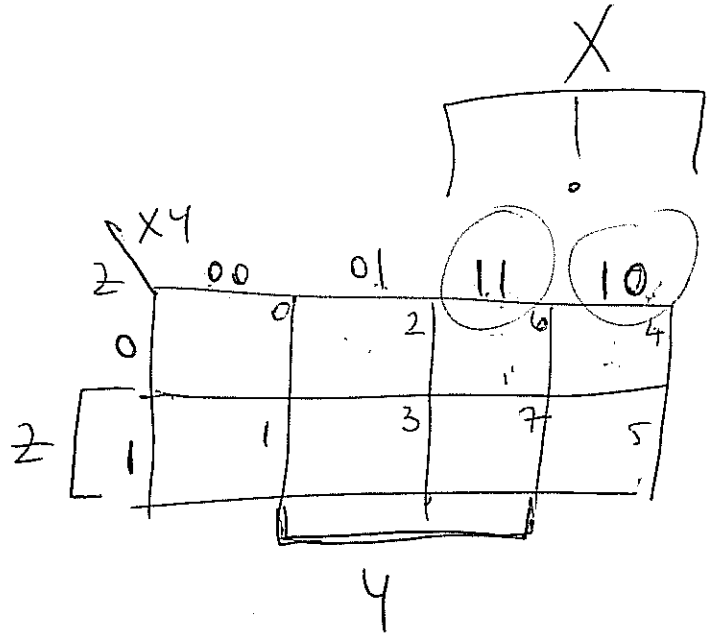
e.g.

| Row | X | Y |
|-----|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |



e.g.

| X | Y | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 1 |



WX

WX Y Z

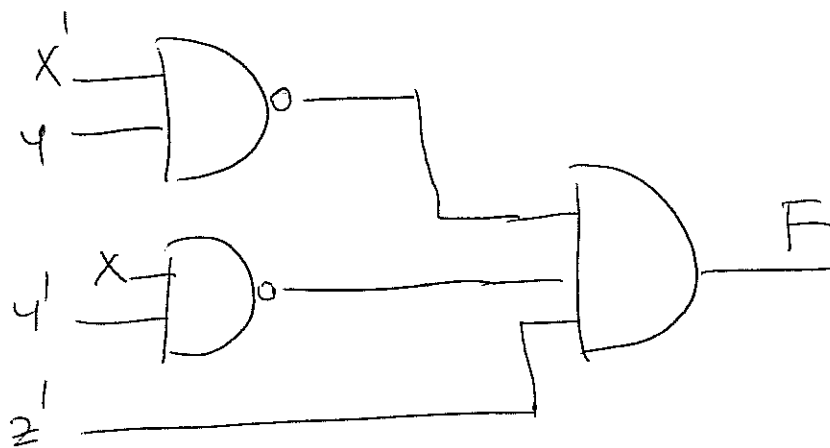
| | | | | |
|----|----|----|----|----|
| WX | 00 | 01 | 11 | 10 |
| YZ | 00 | 01 | 11 | 10 |
| 00 | 0 | 4 | 12 | 8 |
| 01 | 1 | 5 | 13 | 9 |
| 11 | 3 | 7 | 15 | 11 |
| 10 | 2 | 6 | 14 | 10 |

Example:

$$F = (x' \cdot y + x \cdot y' + z)'$$

use two nand gates and one and gate.
complements of the inputs are available.

$$F = ((x' \cdot y)' \cdot (x \cdot y')' \cdot z)'$$



Example:

$$F = \underbrace{A' B' C}_{\text{two-input}} + D'$$

two-input
two NAND gates
one NOR gate

