EECS 281, January 27, 2015

Noninverting Gates:

In CMOS: simplest gates are inverters and next simplest are NAND and NOR gates.

Not possible to design a noninverting gate with a smaller number of transistors than an inverting one.

Switching Algebra

X : variable, represents conditions of a logic signal.

low/high, on/off, 0/1

Axioms:

A1: $X = 0$ if $X \neq 1$

A1': $X = 1$ if $X = 0$

A2: If $X = 0$, then $X' = 1$

A2': If $X = 1$, then $X' = 0$

(In a logic expression: multiplication has precedence)

e.g. $w \cdot x + y \cdot z = (w \cdot x) + (y \cdot z)$

A3: $0 \cdot 0 = 0$ A3': $1 + 1 = 1$

A4: $1 \cdot 1 = 1$ A4': $0 + 0 = 0$

A5: $0 \cdot 1 = 1 \cdot 0 = 0$ A5': $1 + 0 = 0 + 1 = 1$

A1 - A5 and A1' to A5' completely define switching algebra

single-Variable Theorems

T1: $X + 0 = X$

Proof by perfect induction:

X	$X + 0 = X$
0	$0 + 0 = 0$ true by A4'

T1': $X \cdot 1 = X$

T2: $X + 1 = 1$
T2': $X \cdot 0 = 0$
} (Null elements)

(Idempotency) T3: $X + X = X$ T3': $X \cdot X = X$

T4: $(X')' = X$ (Involution)

(Complements) T5: $X + X' = 1$ T5': $X \cdot X' = 0$

T6: $X + Y = Y + X$ T6' $X \cdot Y = Y \cdot X$
Commutativity.

T7: $(X + Y) + Z = X + (Y + Z)$
T7': $(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$
Associativity

~~Distributivity~~ Distributivity:

T8: $X \cdot Y + X \cdot Z = X \cdot (Y + Z)$

T8': $(X + Y) \cdot (X + Z) = X + Y \cdot Z$

Covering:

$$X \cdot (\underbrace{1 + Y}_{1}) = X$$

T9: $X + X \cdot Y = X$

Combining:

$$X \cdot (\overbrace{Y + Y'}^{1}) = X$$

T10: $X \cdot Y + X \cdot Y' = X$

T10': $(X+Y) \cdot (X+Y') = X$

Consensus:

T11: $X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$

$Y \cdot Z = 0$ $\quad \underbrace{X \cdot Y + X' \cdot Z} + 0 = X \cdot Y + X' \cdot Z$

$Y \cdot Z = 1 \Rightarrow \underbrace{Y = 1, Z = 1}$

$X = 0$ $\quad X \cdot Y + X' \cdot Z = 1$

$Y = 1$

$Z = 1$

$x = 1$ $\qquad x \cdot y + x' \cdot z = 1$

$y = 1$

$z = 1$

A = L

B = H

Q1 : OFF

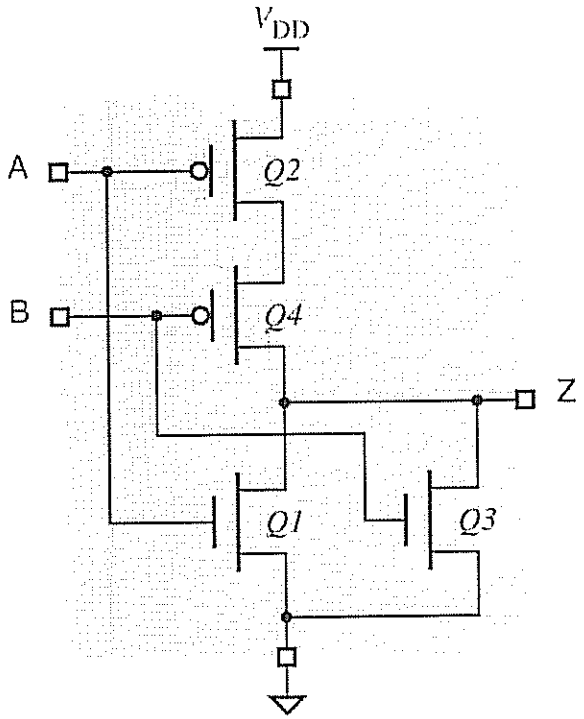
Q2 : ON

Q3 : ON

Q4 : OFF

Z = 0 (L)

(a)



(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)

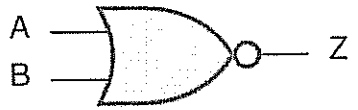
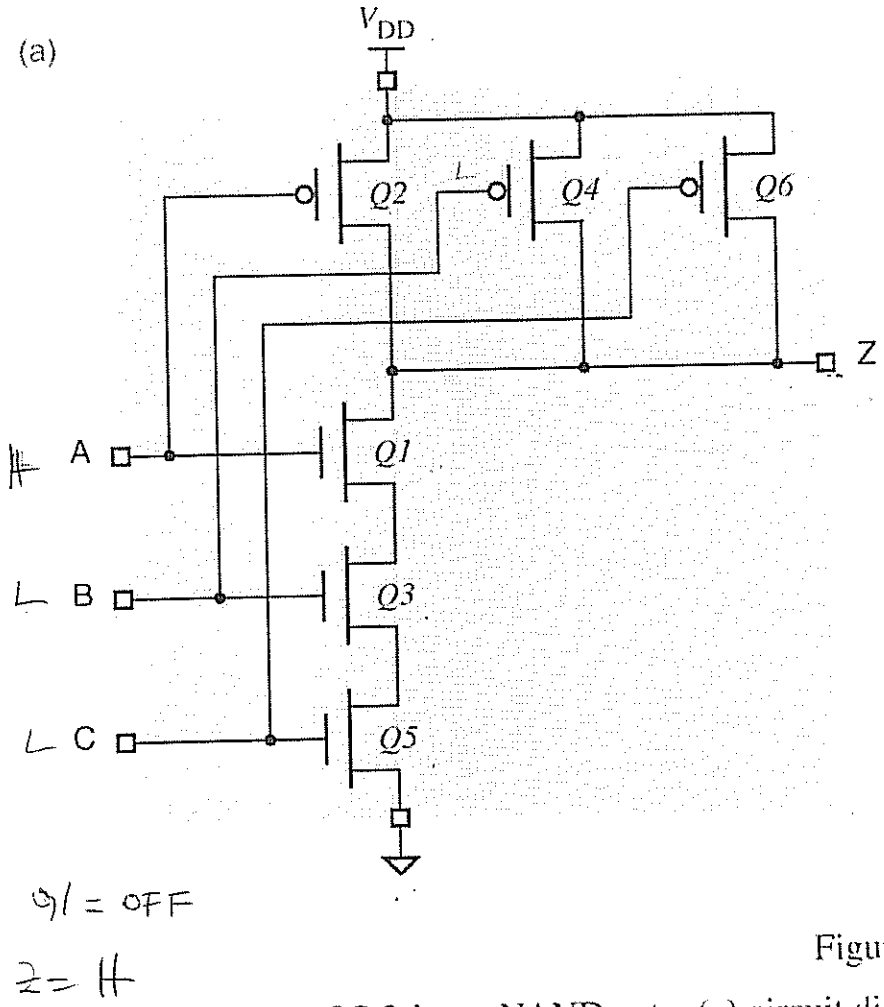


Figure 3-15

CMOS 2-input NOR gate: (a) circuit diagram; (b) function table; (c) logic symbol.

(a)



(b)

A	B	C	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	Z
L	L	L	off	on	off	on	off	on	H
L	L	H	off	on	off	on	on	off	H
L	H	L	off	on	on	off	off	on	H
L	H	H	off	on	on	off	on	off	H
H	L	L	on	off	off	on	off	on	H
H	L	H	on	off	off	on	on	off	H
H	H	L	on	off	on	off	off	on	H
H	H	H	on	off	on	off	on	off	L

(c)

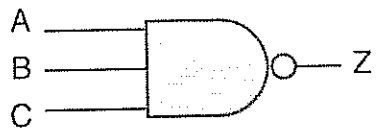
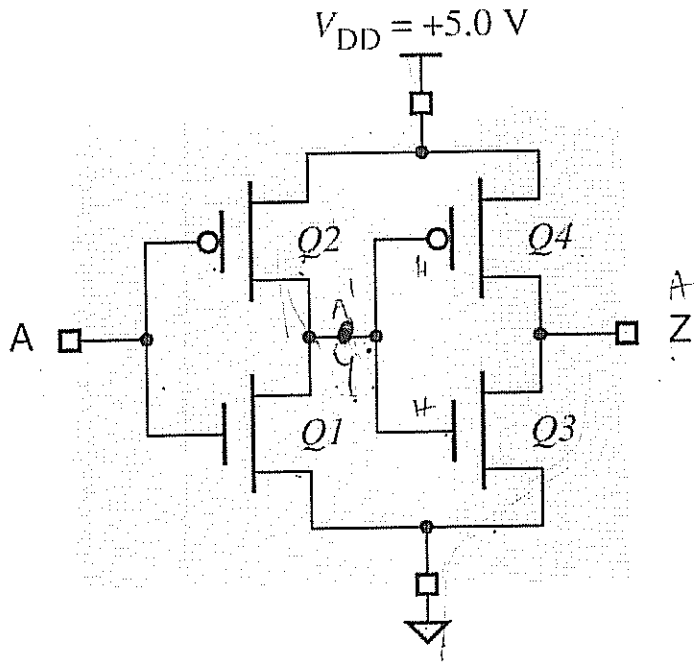


Figure 3-16

CMOS 3-input NAND gate: (a) circuit diagram; (b) function table; (c) logic symbol.

(a)



(b)

A	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	off	on	on	off	L
H	on	off	off	on	H

(c)

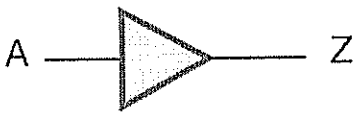
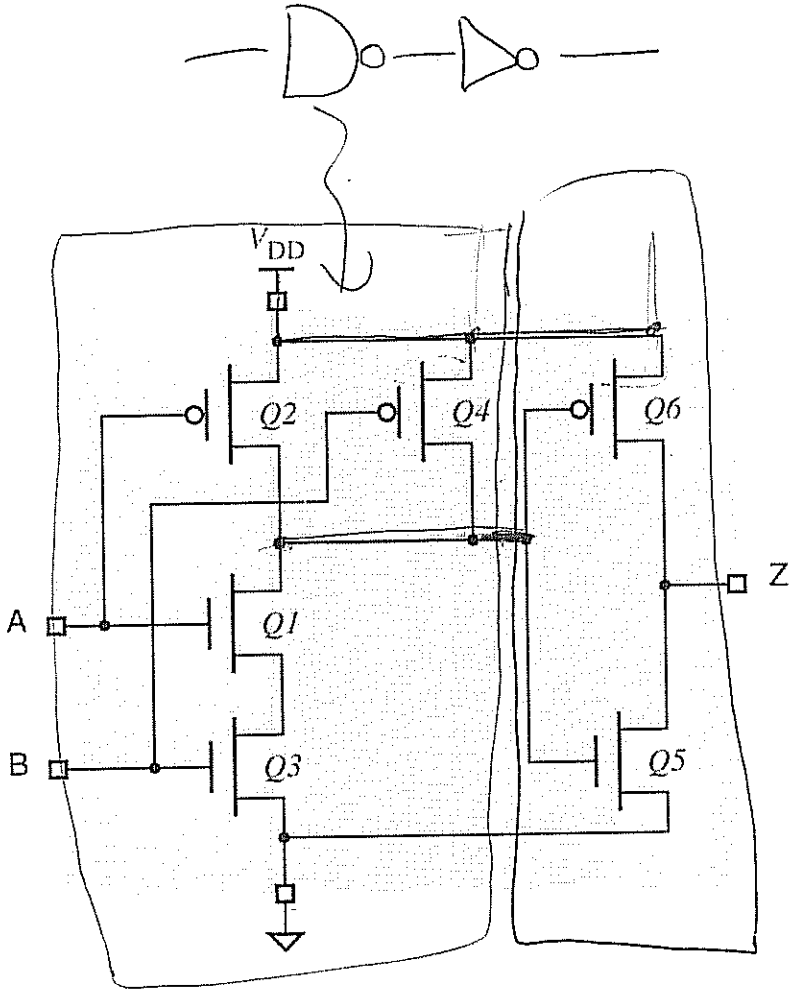


Figure 3-18

CMOS noninverting buffer: (a) circuit diagram; (b) function table; (c) logic symbol.

(a)



(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	Z
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	on	off	L
H	L	on	off	off	on	on	off	L
H	H	on	off	on	off	off	on	H

(c)

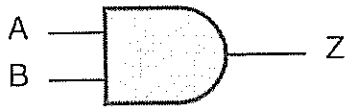
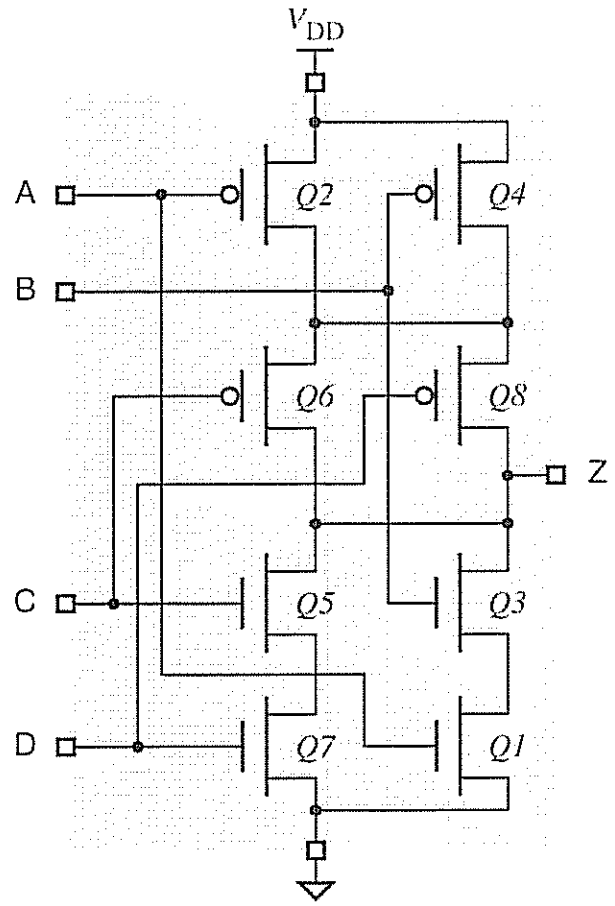


Figure 3-19

CMOS 2-input AND gate: (a) circuit diagram; (b) function table; (c) logic symbol.

(a)



(b)

A	B	C	D	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	*Q7*	*Q8*	Z
L	L	L	L	off	o	off	on	off	on	off	on	H
L	L	L	H	off	o	off	on	off	on	o	off	H
L	L	H	L	off	o	off	on	o	off	off	on	H
L	L	H	H	off	o	off	on	o	off	o	off	L
L	H	L	L	off	o	o	off	off	on	off	on	H
L	H	L	H	off	o	o	off	off	on	o	off	H
L	H	H	L	off	o	o	off	o	off	off	on	H
L	H	H	H	off	o	o	off	o	off	o	off	L
H	L	L	L	o	off	off	on	off	on	off	on	H
H	L	L	H	o	off	off	on	off	on	on	off	H
H	L	H	L	o	off	off	on	o	off	off	on	H
H	L	H	H	o	off	off	on	o	off	on	off	L
H	H	L	L	o	off	o	off	off	on	off	on	L
H	H	L	H	o	off	o	off	off	on	on	off	L
H	H	H	L	o	off	o	off	o	off	off	on	L
H	H	H	H	o	off	o	off	o	off	on	off	L

Figure 3-20

CMOS AND-OR-INVERT gate: (a) circuit diagram; (b) function table.

From *Digital Design: Principles and Practices*, Fourth Edition, John F. Wakerly, ISBN 0-13-186389-4.

For simplicity assume: $t_r = t_f = 0$.

t_p can be different depending on direction of change.

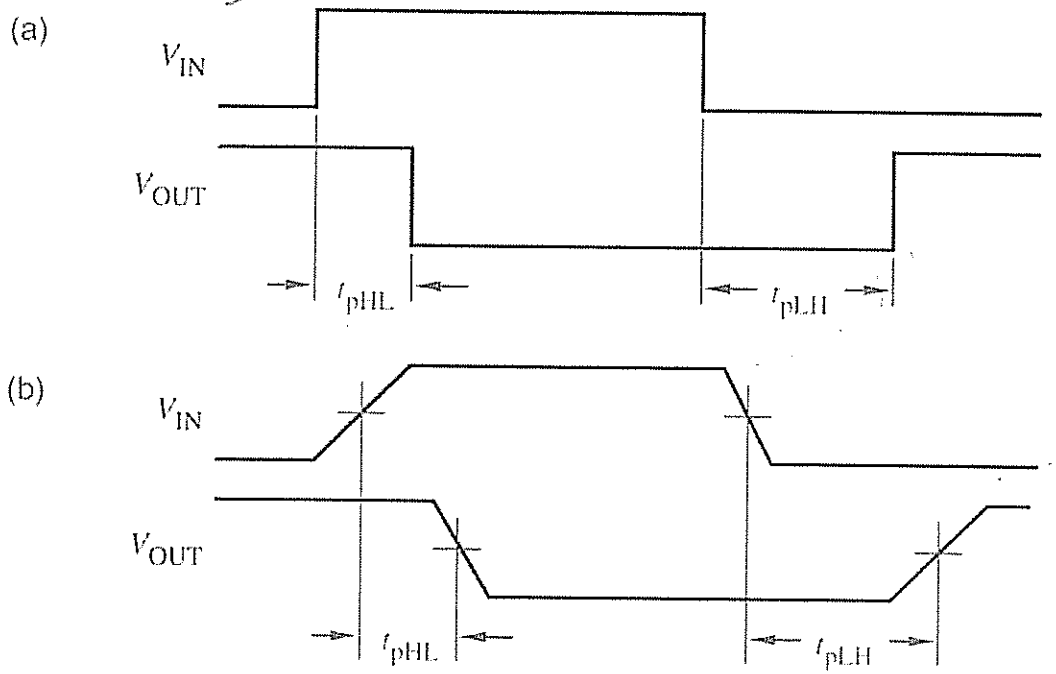


Figure 3-42

Propagation delays for a CMOS inverter: (a) ignoring rise and fall times; (b) measured at midpoints of transitions.