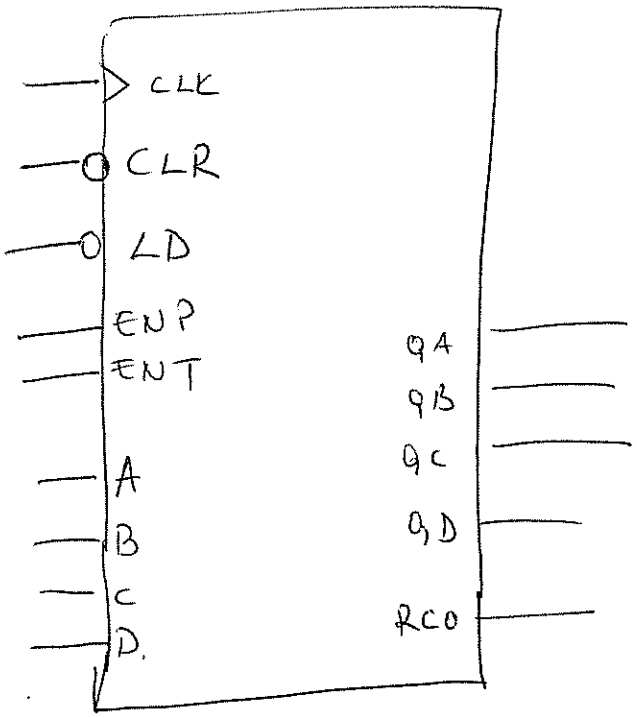
EECS 281, March 31, 2015

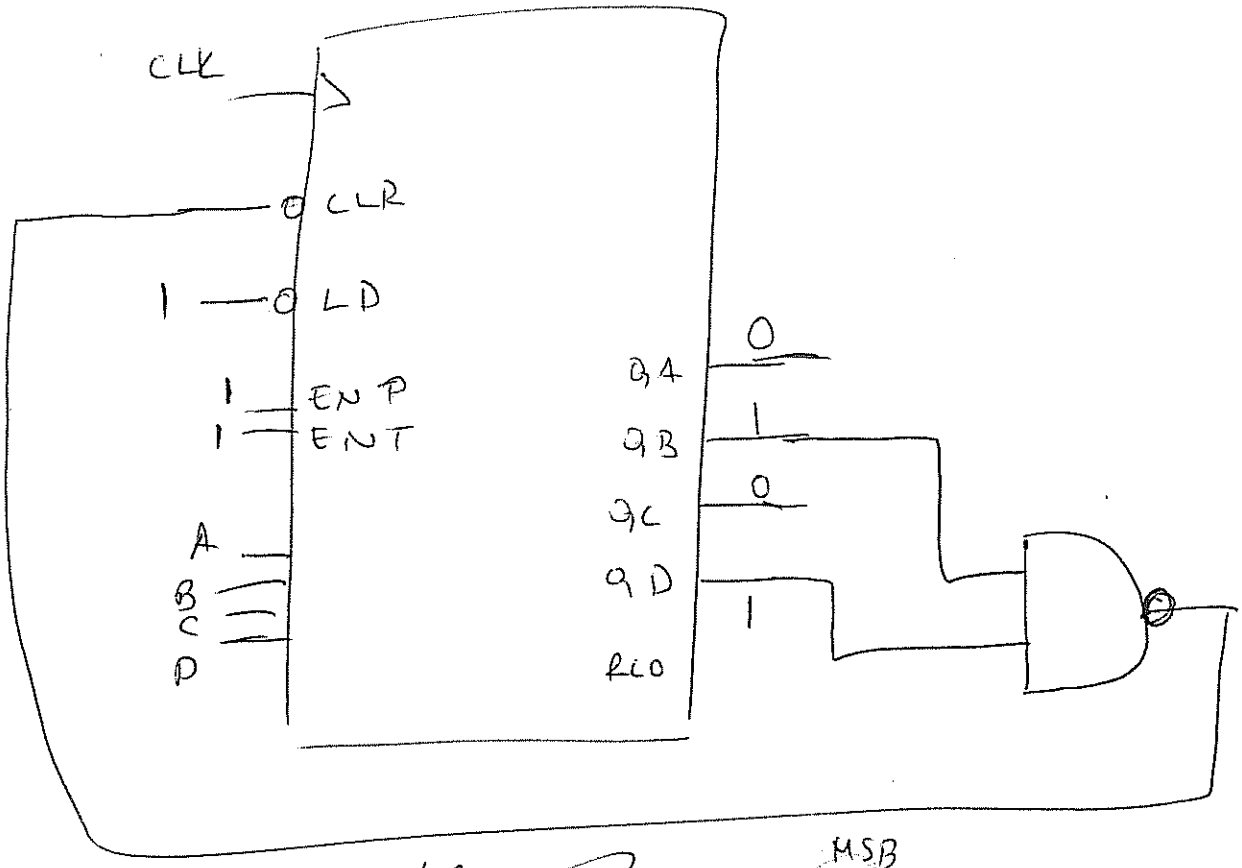
Most popular MSI counter:

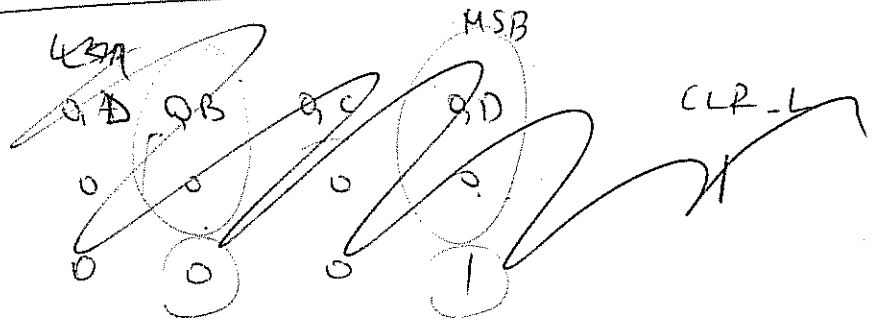
74x163 synchronous 4-bit binary counter.



Example: Counting sequence 0, 1, 2, ... 10, 0, 1, ...

74x163





QD	QC	QB	QA	CLR_L
0	0	0	0	1
0	0	0	1	1
1	0	1	0	0

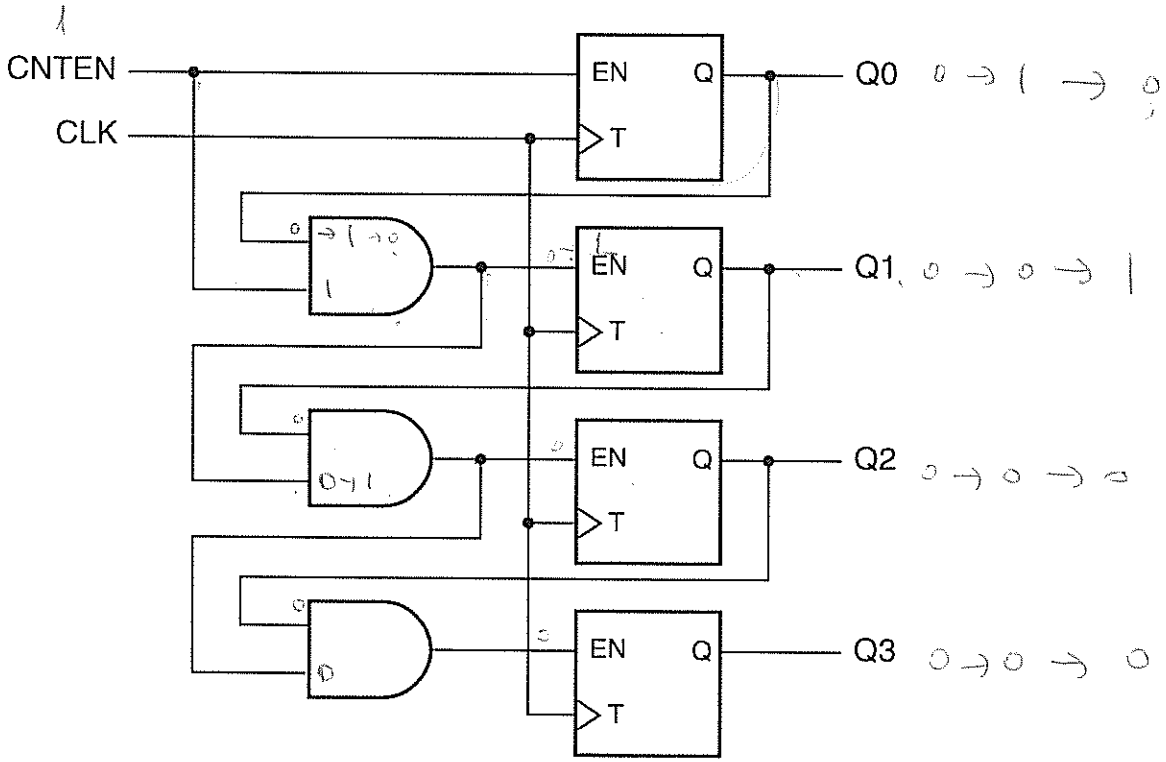


Figure 8-25

A synchronous 4-bit binary counter with serial enable logic.

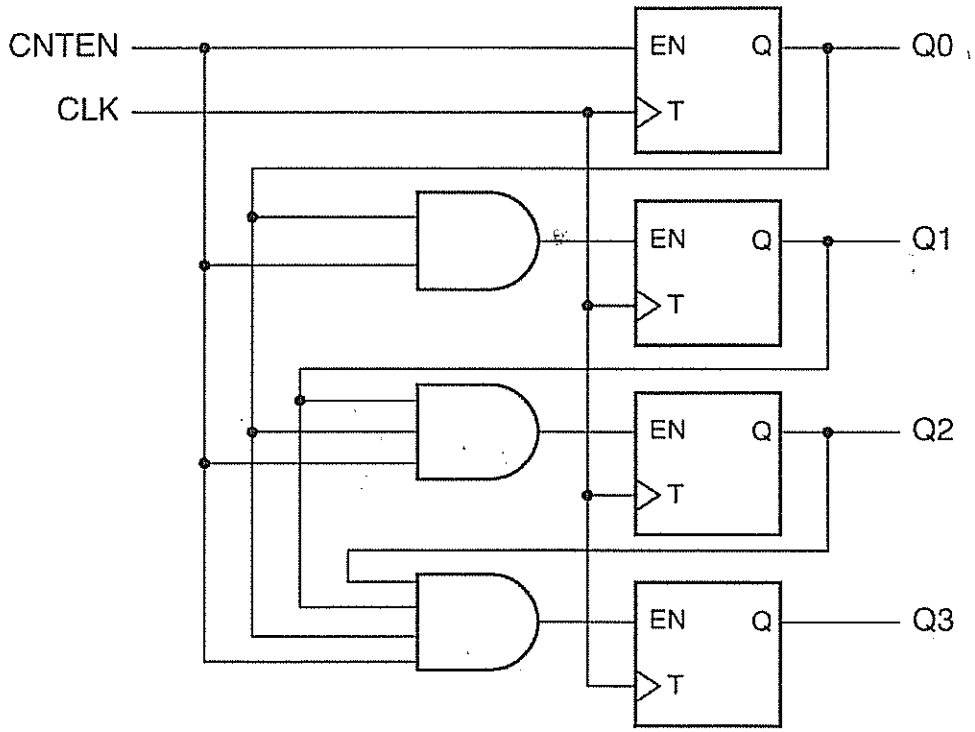


Figure 8-26

A synchronous 4-bit binary counter with parallel enable logic.

Fastest binary counter structure.

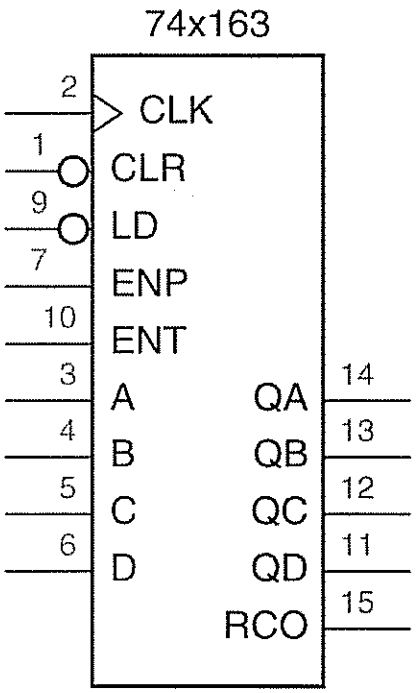


Figure 8-27

Traditional logic symbol for the 74×163.

synchronous 4-bit binary counter.

Inputs				Current State				Next State			
CLR_L	LD_L	ENT	ENP	QD	QC	QB	QA	QD*	QC*	QB*	QA*
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

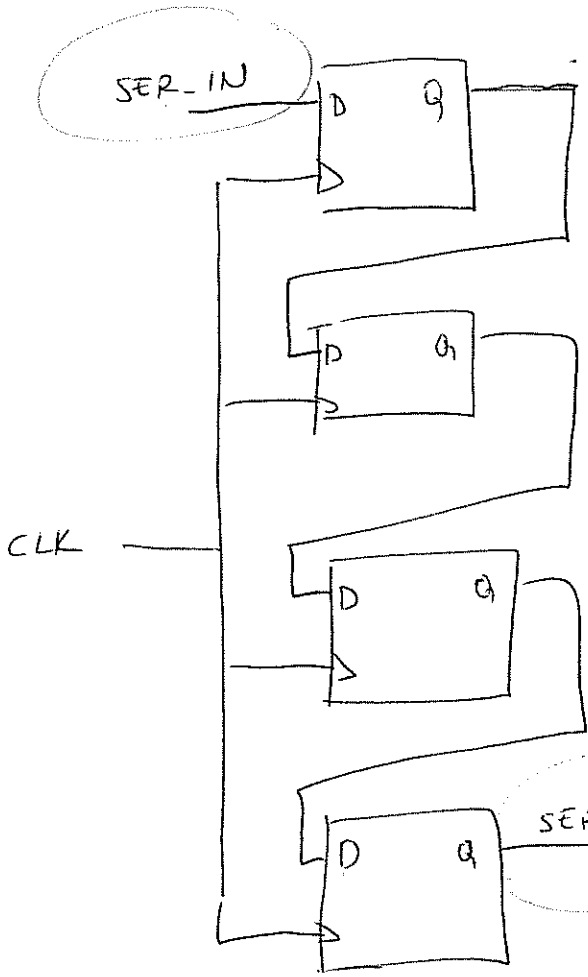
Table 8-13

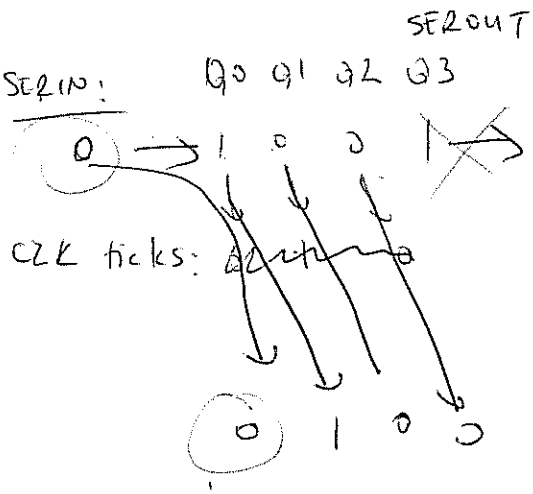
State table for a 74×163 4-bit binary counter.

Shift Register

n-bit register: shifts its stored data by one bit position at each clock tick.

Serial-in, serial-out:





This register can be used to delay a signal by n clock ticks.

at clock tick: either loads new data from 1D–ND.
or shifts current contents.

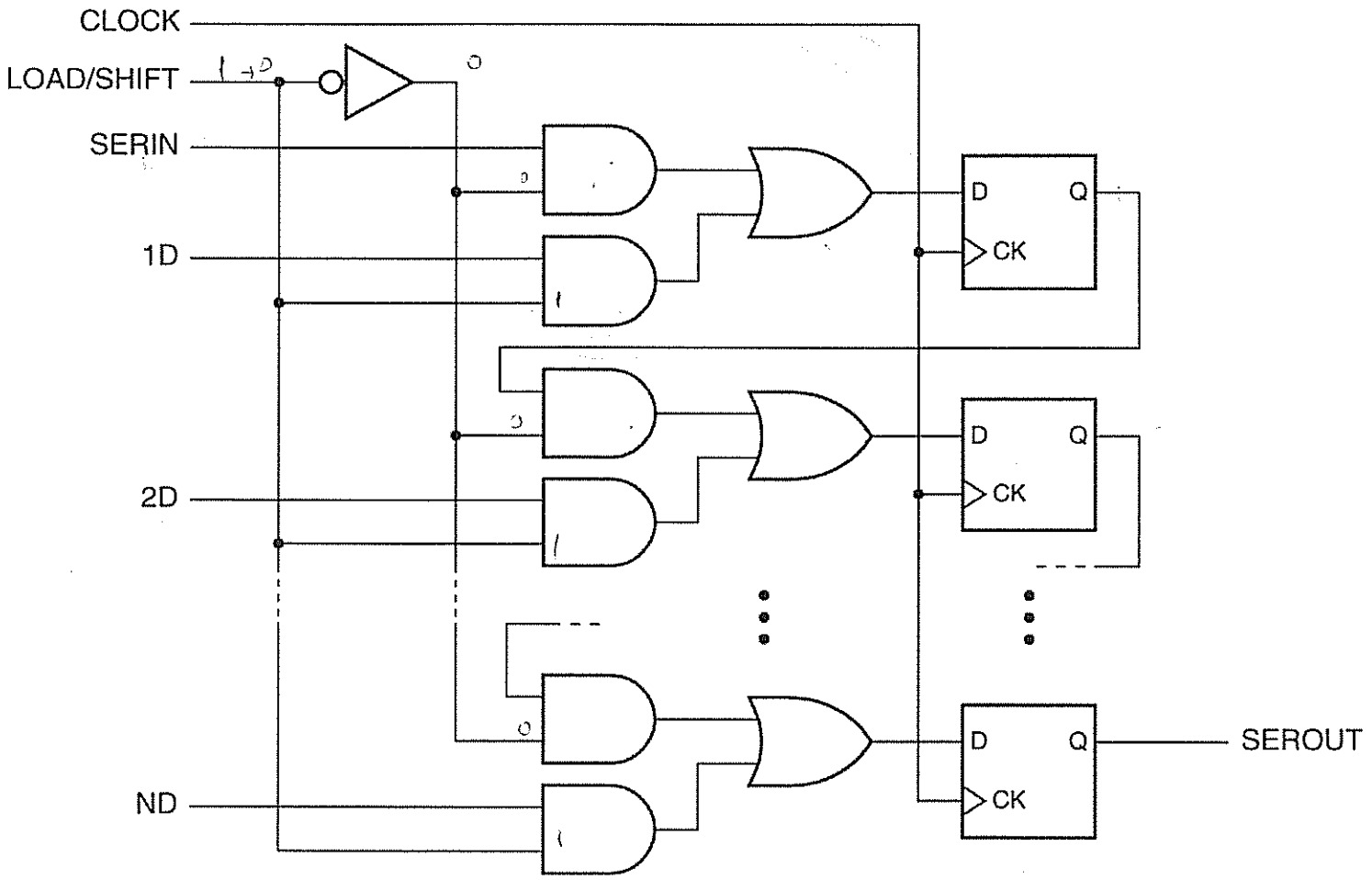
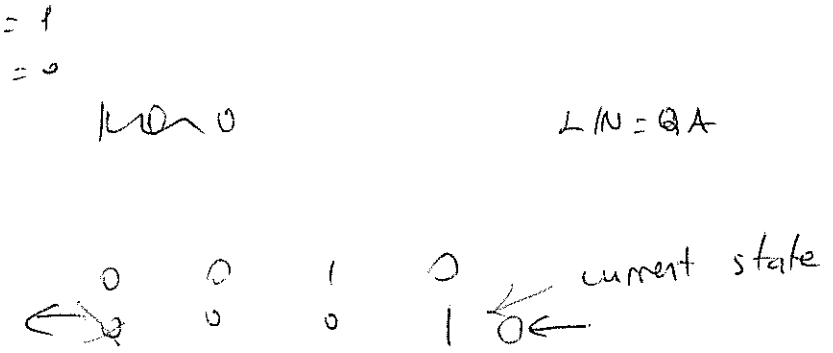


Figure 8-39

Structure of a parallel-in, serial-out shift register.



Function	Inputs S1	Inputs S0	Next state QA*	Next state QB*	Next state QC*	Next state QD*
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D

Table 8-24

Function table for the 74×194 4-bit universal shift register.

Normally performs a left shift (Reset negated).

When RESET asserted: loads 0001.

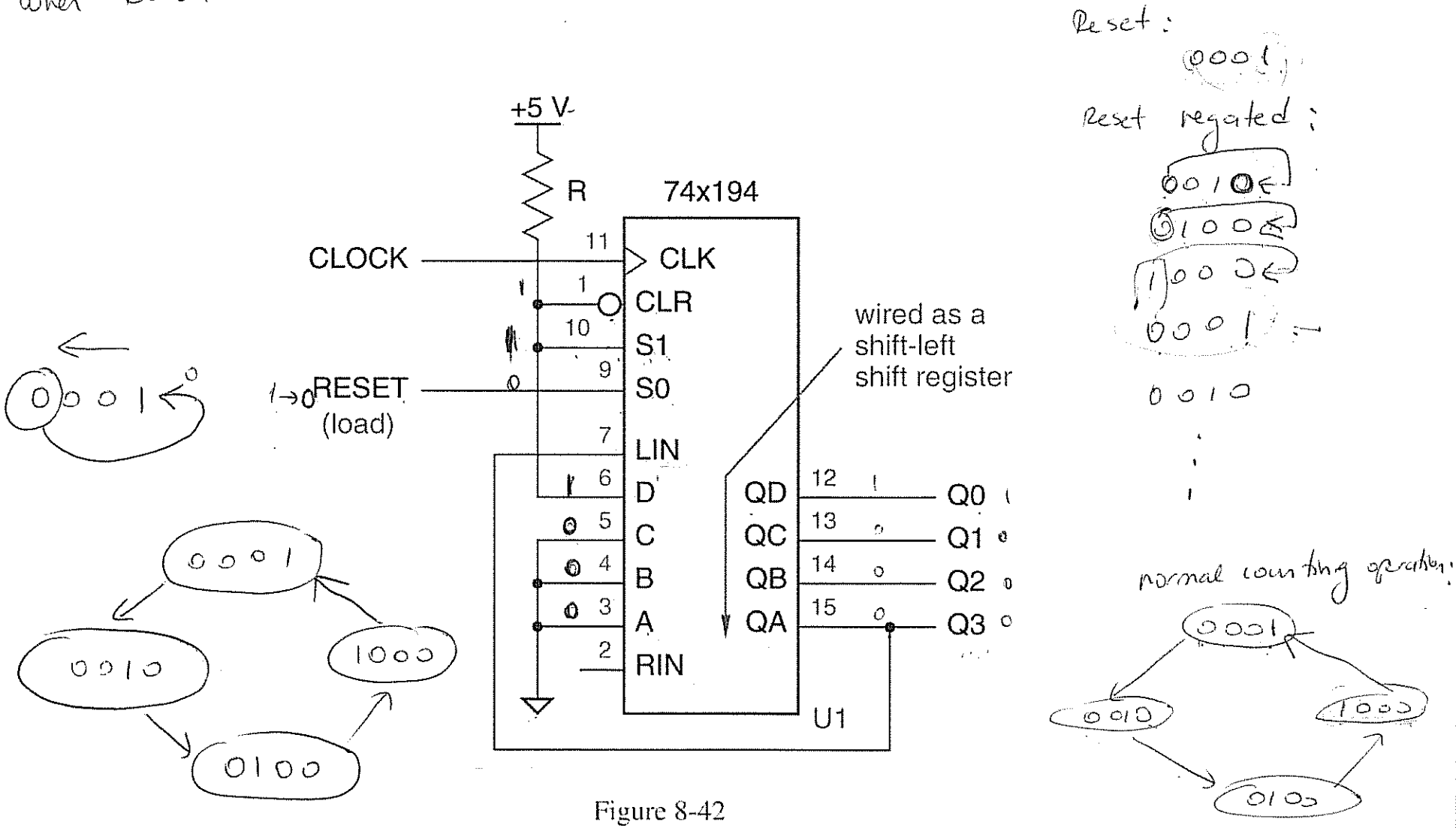


Figure 8-42

Simplest design for a 4-bit, 4-state ring counter with a single circulating 1.

bidirectional: contents may be shifted in two directions.

Left: in the direction from QD to QA

Right: in the direction from QA to QD.

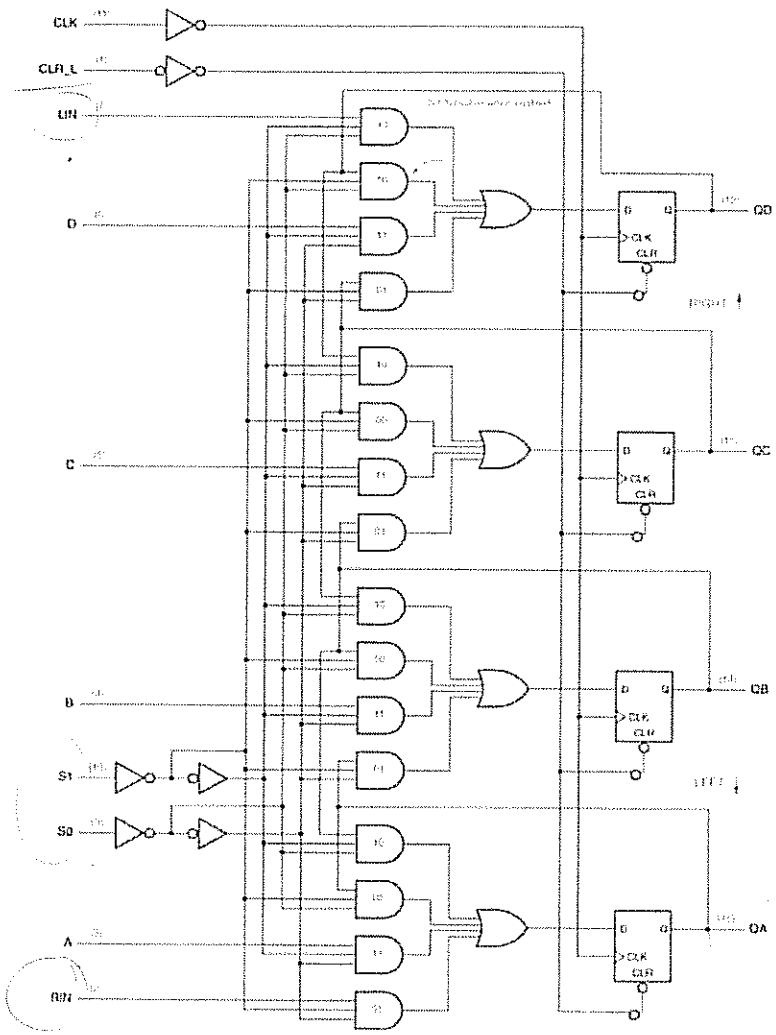


Figure 8-41

Logic diagram for the 74×194 4-bit universal shift register, including pin numbers for a standard 16-pin dual in-line package.

general enough to be used in any applications of shift registers.

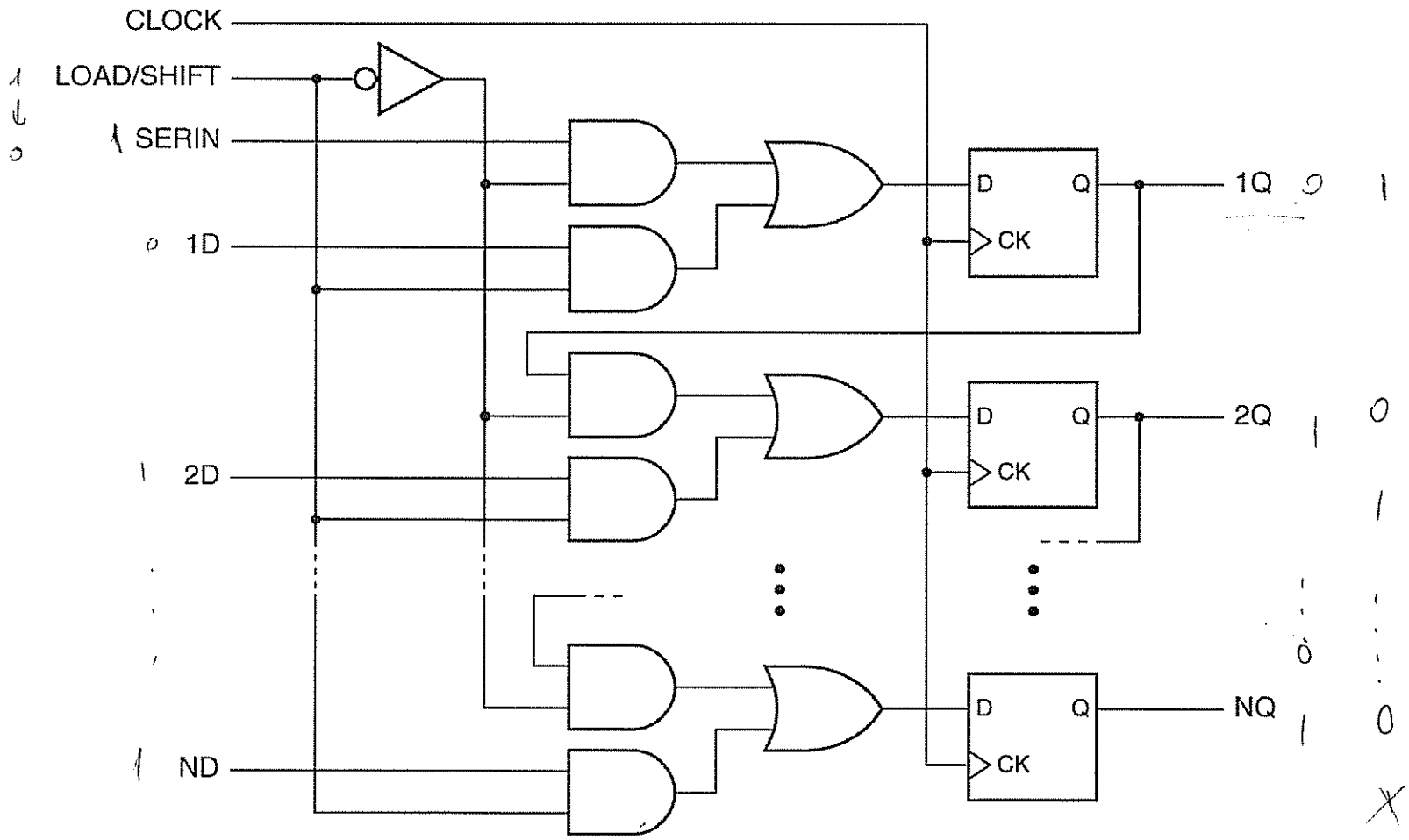


Figure 8-40

Structure of a parallel-in, parallel-out shift register.