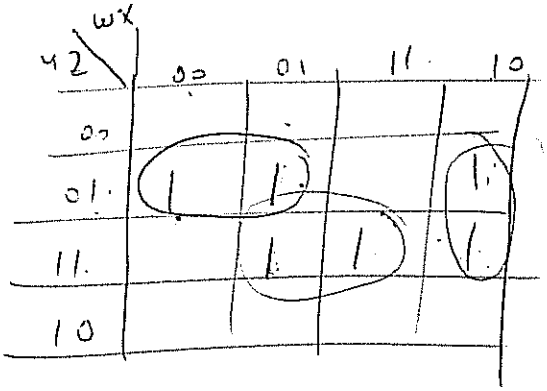
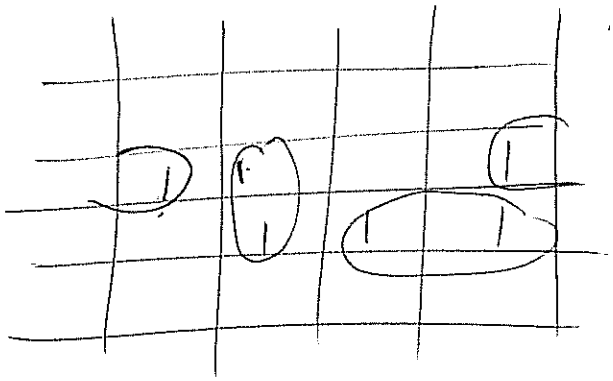
EECS 281, February 10, 2015

Example:



$F = w'y'z + xyz + wx'z$

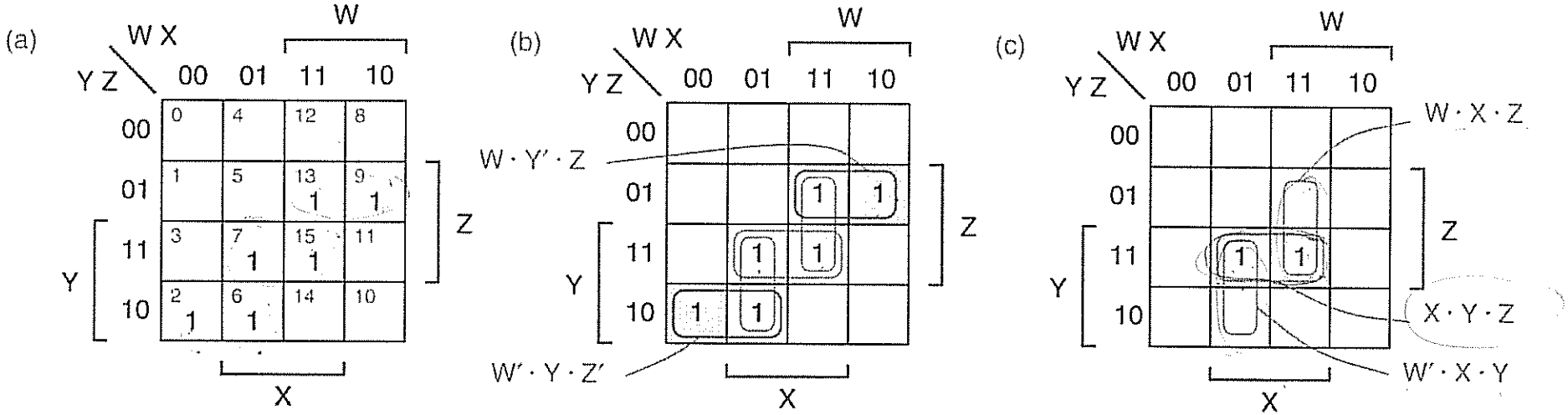


Timing Hazards

Because of circuit delays, transient behavior may be different than steady-state.

A circuit's output may produce a short pulse, called a glitch at a time when steady-state analysis predict no change.

X, Y, Z eclipses two prime implicants.
⇒ two 1-cells covered only by X·Y·Z



$F = \Sigma_{W,X,Y,Z}(2,6,7,9,13,15)$

$F = W \cdot Y' \cdot Z + W' \cdot Y \cdot Z' + X \cdot Y \cdot Z$

Figure 4-36

$F = \Sigma_{W,X,Y,Z}(2,6,7,9,13,15)$: (a) Karnaugh map; (b) prime implicants and distinguished 1-cells; (c) reduced map after removal of essential prime implicants and covered 1-cells.

X, Y, Z : secondary essential prime implicant.
(that must be included in minimal sum)

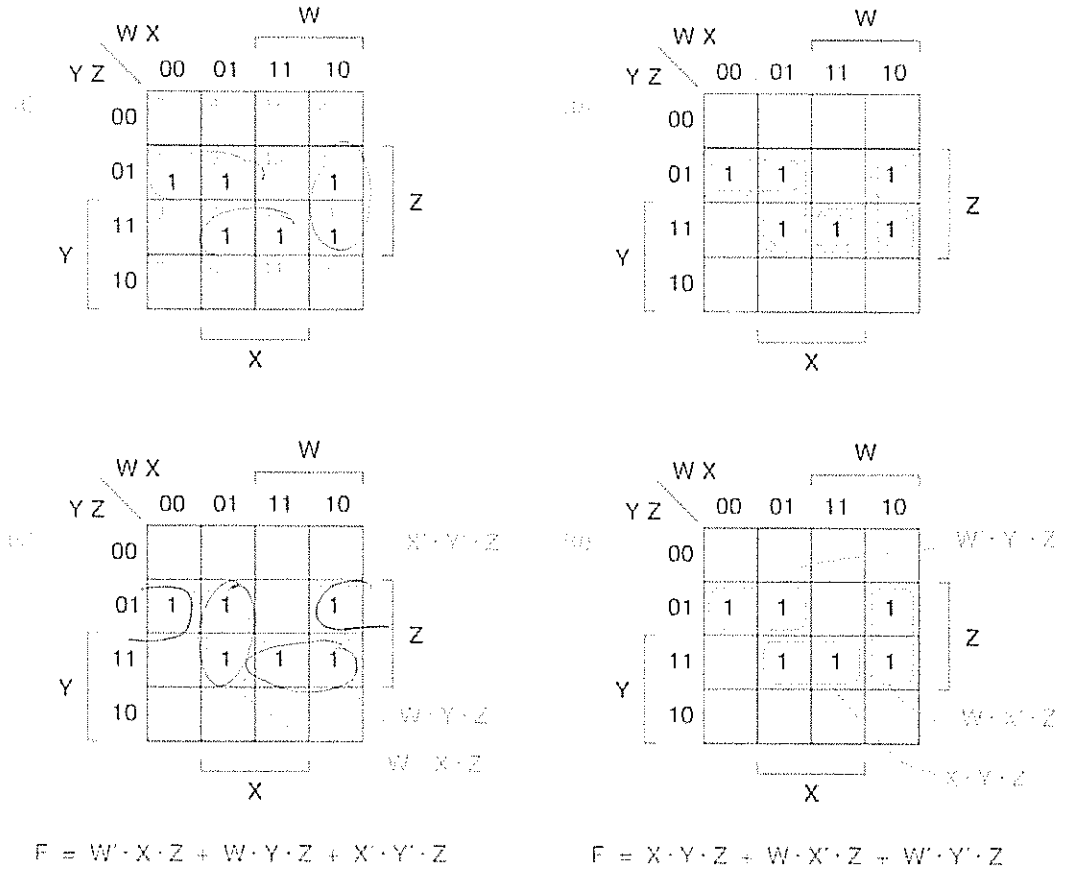


Figure 4-37

$F = \Sigma_{W,X,Y,Z}(1,5,7,9,11,15)$: (a) Karnaugh map; (b) prime implicants; (c) a minimal sum; (d) another minimal sum.

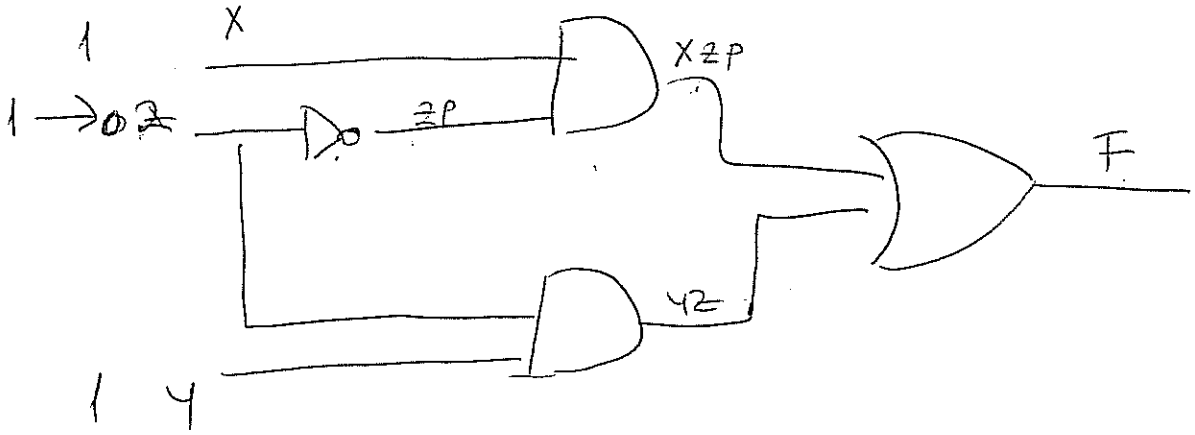
Static Hazards

static-1 Hazard: possibility of a 0 glitch at the output when output is expected to stay at a steady 1.

A static-1 hazard is a pair of input combinations that

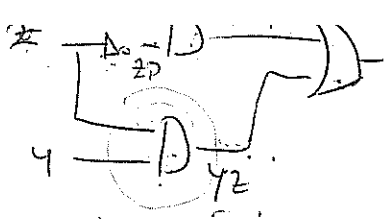
- differ in only one input variable.
- both give a 1-output

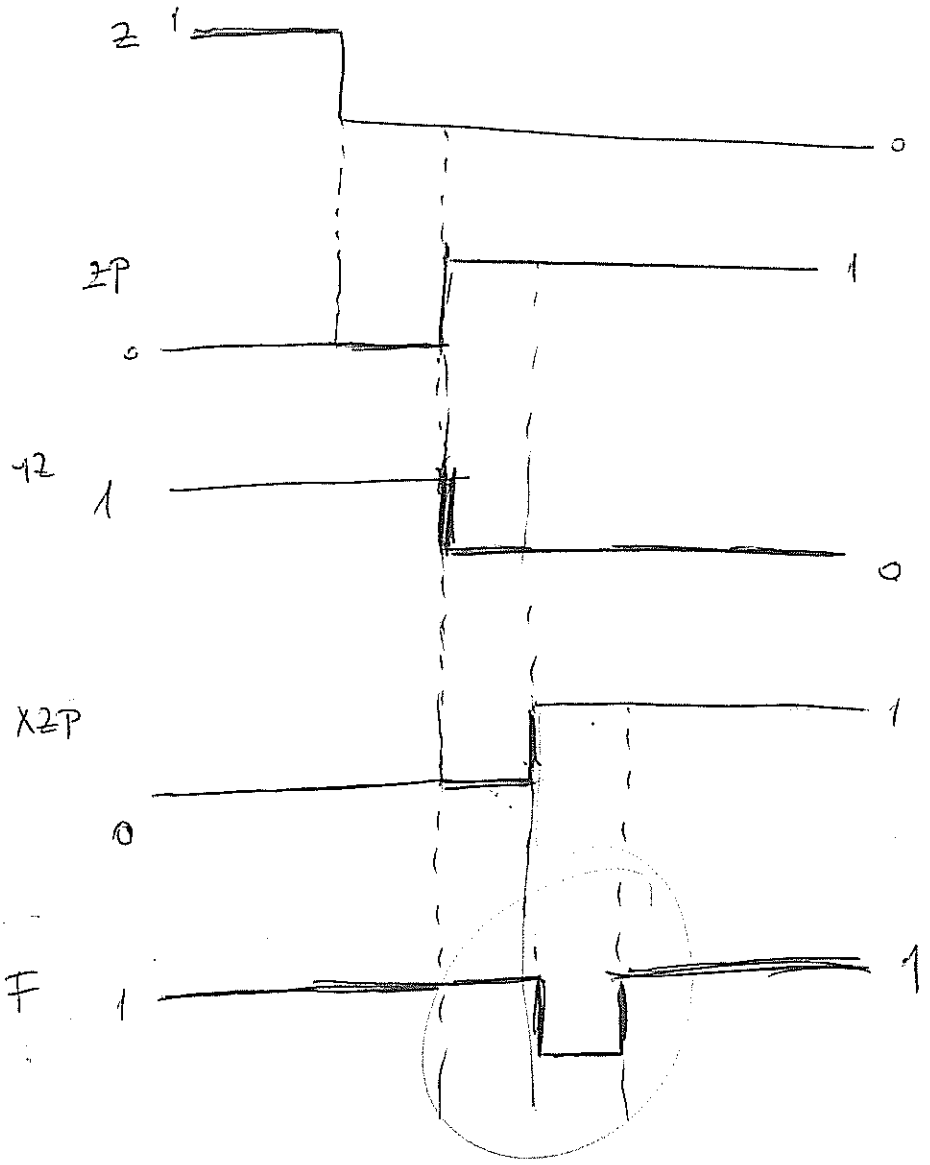
Example:



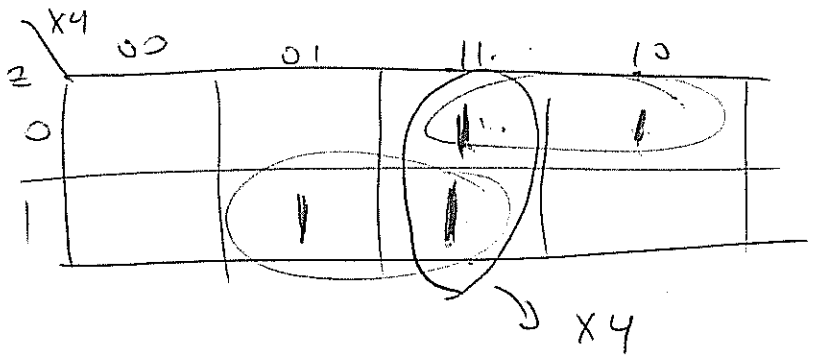
All the gates have a unit delay.

XYZ	→	XYZ
1 1 1		1 1 0
F= 1		1





Example: $F = xz' + yz + xy$



xyz → F

111 → 1

xyz

110 → 1

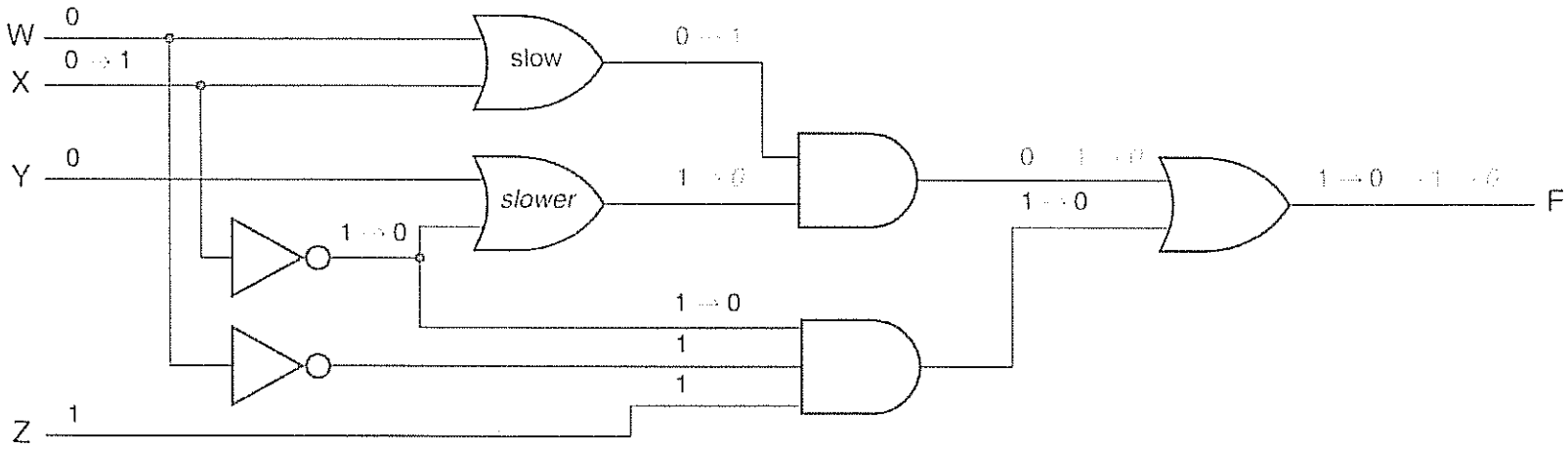
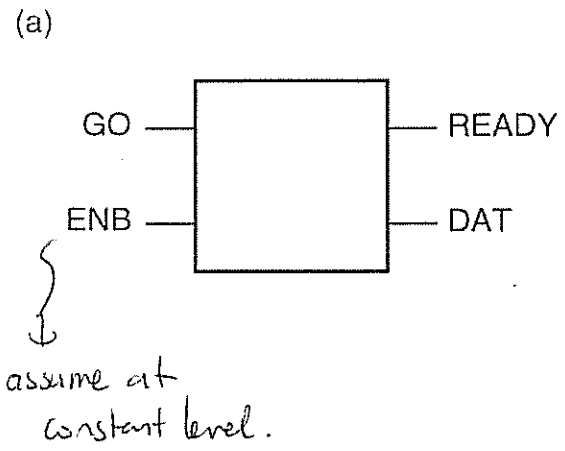


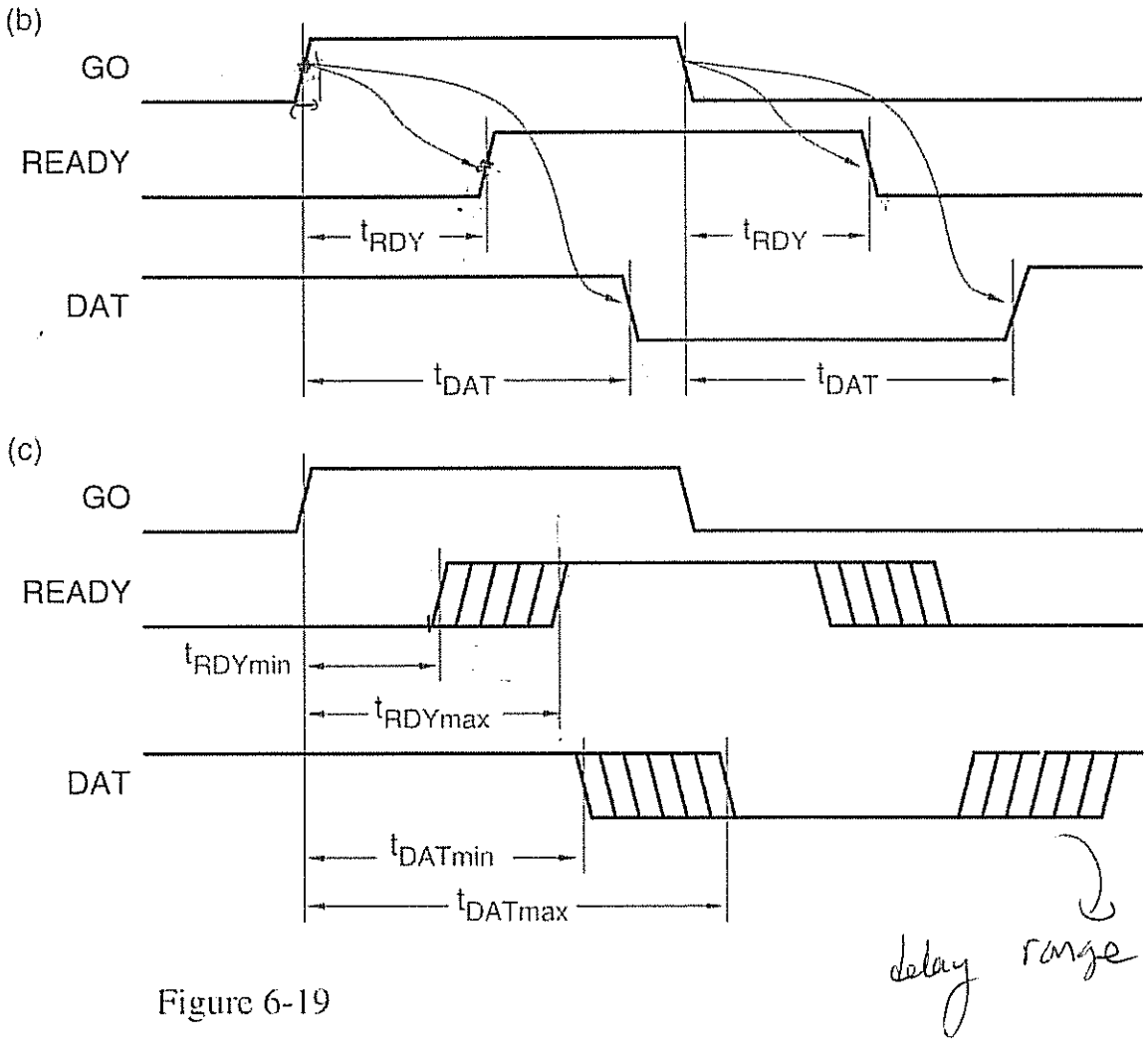
Figure 4-43
Circuit with a dynamic hazard.

Different paths may have different delays!

Delays may be different for L→H or H→L transition for a certain path.



assume at constant level.



delay range

Figure 6-19

Timing diagrams for a combinational circuit: (a) block diagram of circuit; (b) causality and propagation delay; (c) minimum and maximum delays.

	74HCT		74AHCT				74LS			
	Typical	Maximum	Typical		Maximum		Typical		Maximum	
Part Number	t_{pLH}, t_{pHL}	t_{pLH}, t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
'00, '10	11	35	5.5	5.5	9.0	9.0	9	10	15	15
'02	9	29	3.4	4.5	8.5	8.5	10	10	15	15
'04	11	35	5.5	5.5	8.5	8.5	9	10	15	15
'08, '11	11	35	5.5	5.5	9.0	9.0	8	10	15	20
'14	16	48	5.5	5.5	9.0	9.0	15	15	22	22
'20	11	35					9	10	15	15
'21	11	35					8	10	15	20
'27	9	29	5.6	5.6	9.0	9.0	10	10	15	15
'30	11	35					8	13	15	20
'32	9	30	5.3	5.3	8.5	8.5	14	14	22	22
'86 (2 levels)	13	40	5.5	5.5	10	10	12	10	23	17
'86 (3 levels)	13	40	5.5	5.5	10	10	20	13	30	22

Table 6-2

Propagation delay in nanoseconds of selected 5-V CMOS and TTL SSI parts.

From *Digital Design: Principles and Practices*, Fourth Edition, John F. Wakerly, ISBN 0-13-186389-4.

Part	From	To	74HCT Typ.	74HCT Max.	74AHCT Typ.	74AHCT Max.	74FCT Typ.	74FCT Max.	74LS Typ.		74LS Max.	
			t_{pLH},t_{pHL}	t_{pLH},t_{pHL}	t_{pLH},t_{pHL}	t_{pLH},t_{pHL}	t_{pLH},t_{pHL}	t_{pLH},t_{pHL}	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
'138	any select	output (2)	23	45	8.1	13	5	9	11	18	20	41
	any select	output (3)	23	45	8.1	13	5	9	21	20	27	39
	$\overline{G2A}$, $\overline{G2B}$	output	22	42	7.5	12	4	8	12	20	18	32
	G1	output	22	42	7.1	11.5	4	8	14	13	26	38
'139	any select	output (2)	14	43	6.5	10.5	5	9	13	22	20	33
	any select	output (3)	14	43	6.5	10.5	5	9	18	25	29	38
	enable	output	11	43	5.9	9.5	5	9	16	21	24	32
'151	any select	Y	17	51			5	9	27	18	43	30
	any select	$\overline{Y}$	18	54			5	9	14	20	23	32
	any data	Y	16	48			4	7	20	16	32	26
	any data	$\overline{Y}$	15	45			4	7	13	12	21	20
	enable	Y	12	36			4	7	26	20	42	32
	enable	$\overline{Y}$	15	45			4	7	15	18	24	30
'153	any select	output	14	43			5	9	19	25	29	38
	any data	output	12	43			4	7	10	17	15	26
	enable	output	11	34			4	7	16	21	24	32
'157	select	output	15	46	6.8	11.5	7	10.5	15	18	23	27
	any data	output	12	38	5.0	9.5	4	6	9	9	14	14
	enable	output	12	38	7.1	12.0	7	10.5	13	14	21	23
'182	any $\overline{Gi}$, $\overline{Pi}$	C1–3	13	41					4.5	4.5	7	7
	any $\overline{Gi}$, $\overline{Pi}$	$\overline{G}$	13	41					5	7	7.5	10.5
	any $\overline{Pi}$	$\overline{P}$	11	35					4.5	6.5	6.5	10
	C0	C1–3	17	50					6.5	7	10	10.5
'280	any input	EVEN	18	53			6	10	33	29	50	45
	any input	ODD	19	56			6	10	23	31	35	50
'283	C0	any Si	22	66					16	15	24	24
	any Ai, Bi	any Si	21	61					15	15	24	24
	C0	C4	19	58					11	11	17	22
	any Ai, Bi	C4	20	60					11	12	17	17
'381	CIN	any Fi							18	14	27	21
	any Ai, Bi	$\overline{G}$							20	21	30	33
	any Ai, Bi	$\overline{P}$							21	33	23	33
	any Ai, Bi	any Fi							20	15	30	23
	any select	any Fi							35	34	53	51
	any select	$\overline{G}$, $\overline{P}$							31	32	47	48
'682	any Pi	$\overline{PEQO}$	26	69			7	11	13	15	25	25
	any Qi	$\overline{PEQO}$	26	69			7	11	14	15	25	25
	any Pi	$\overline{PGTO}$	26	69			9	14	20	15	30	30
	any Qi	$\overline{PGTO}$	26	69			9	14	21	19	30	30

Table 6-3

Propagation delay in nanoseconds of selected CMOS and TTL MSI parts.

X: potential connections.

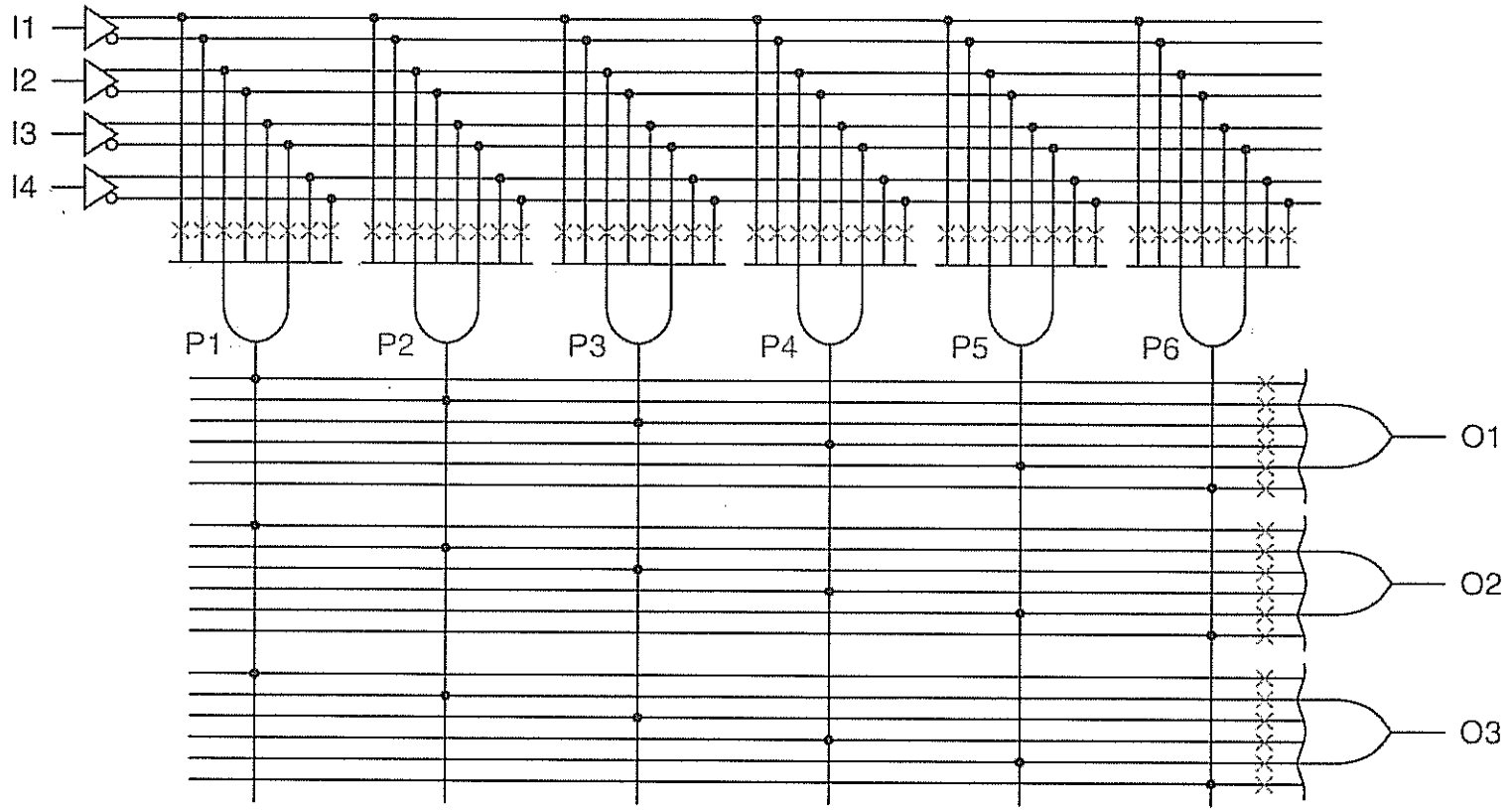


Figure 6-21

A 4 × 3 PLA with six product terms.

$$O1 = \underbrace{I1 \cdot I2}_{P1} + \underbrace{I1 \cdot I3'}_{P2} + \underbrace{I1' \cdot I2' \cdot I4'}_{P3}$$

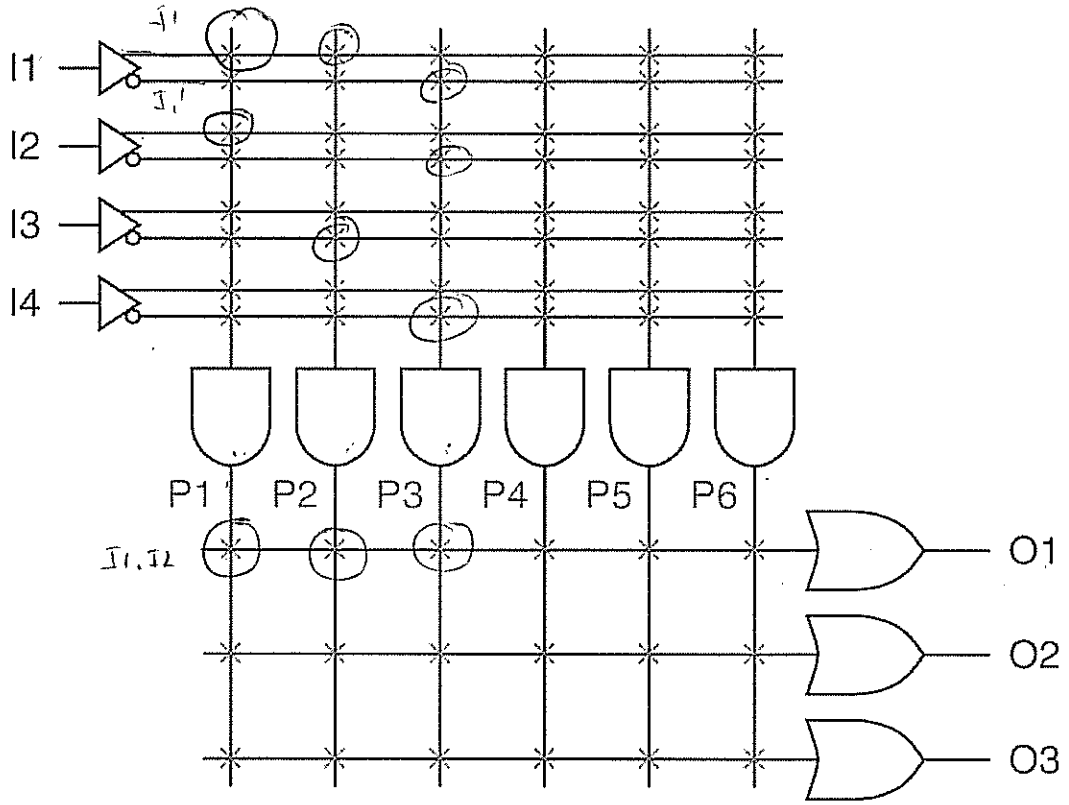


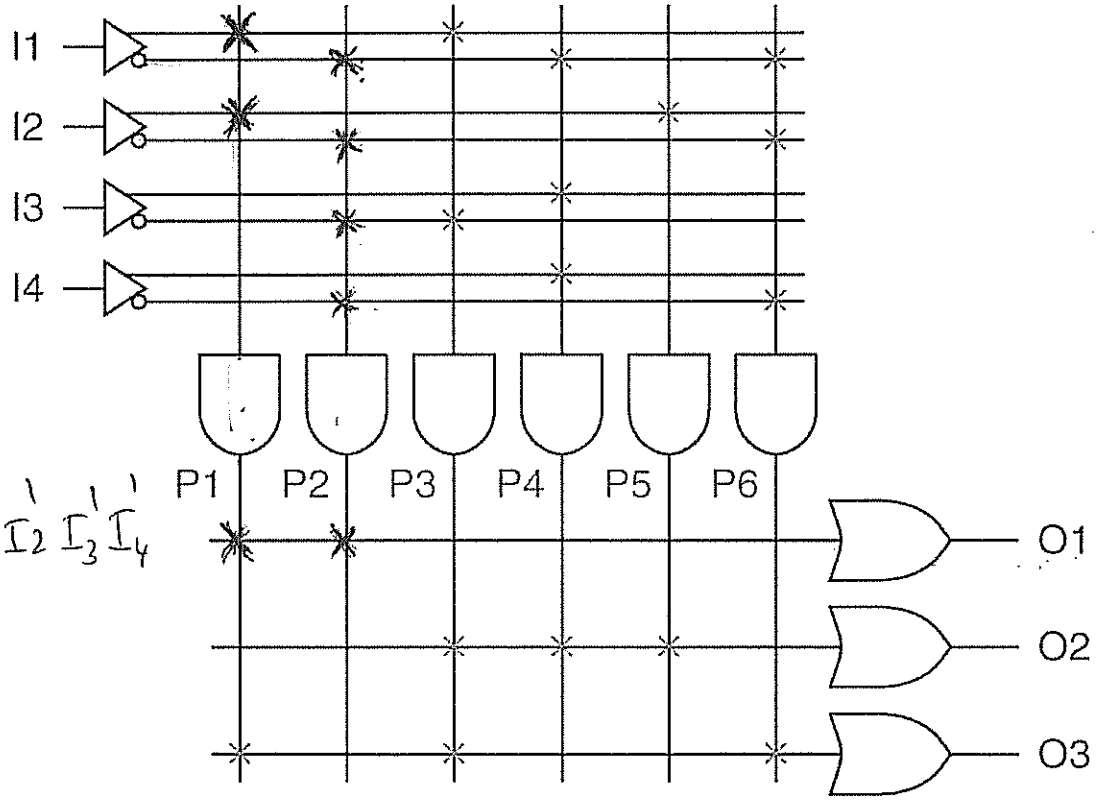
Figure 6-22

Compact representation of a 4 × 3 PLA with six product terms.

$O1 = I1 \cdot I2 + I1' \cdot I2' \cdot I3' \cdot I4'$

$O2 = I1 \cdot I3' + I1' \cdot I3 \cdot I4 + I2$

$O3 = I1 \cdot I2 + I1 \cdot I3' + I1' \cdot I2' \cdot I4'$



$O1 = I1 \cdot I2 + I_1' I_2' I_3' I_4'$

Figure 6-23

A 4 × 3 PLA programmed with a set of three logic equations.

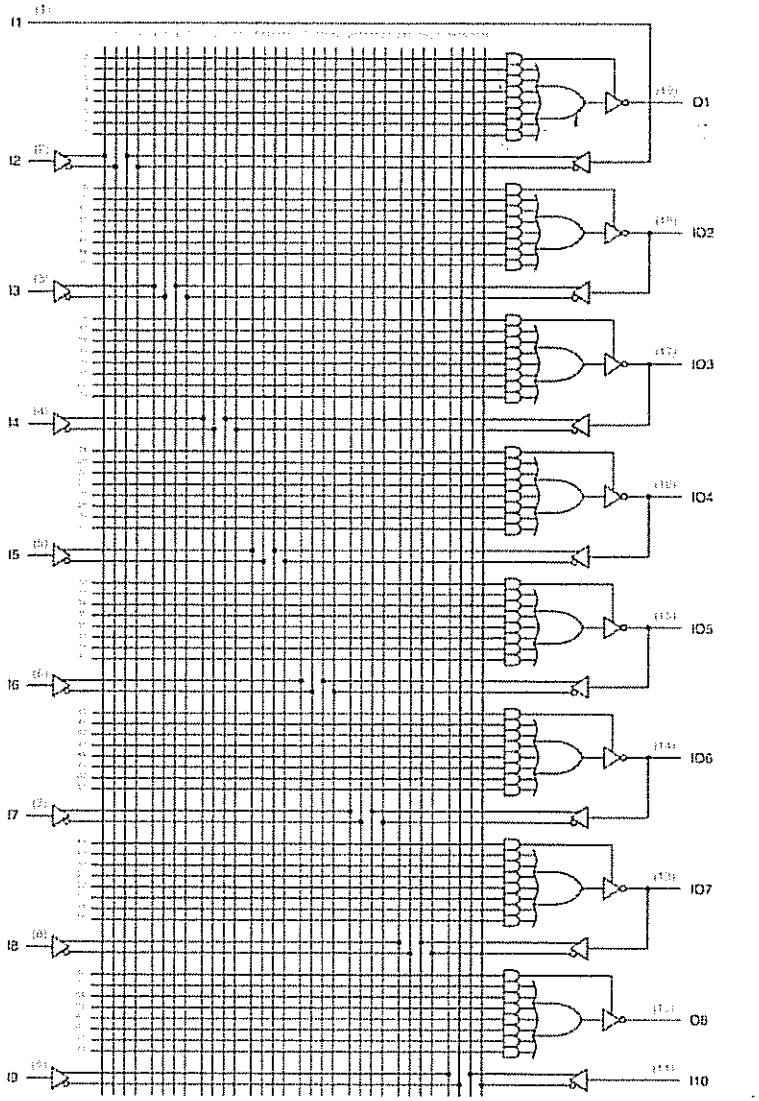


Figure 6-25

Logic diagram of the PAL16L8.

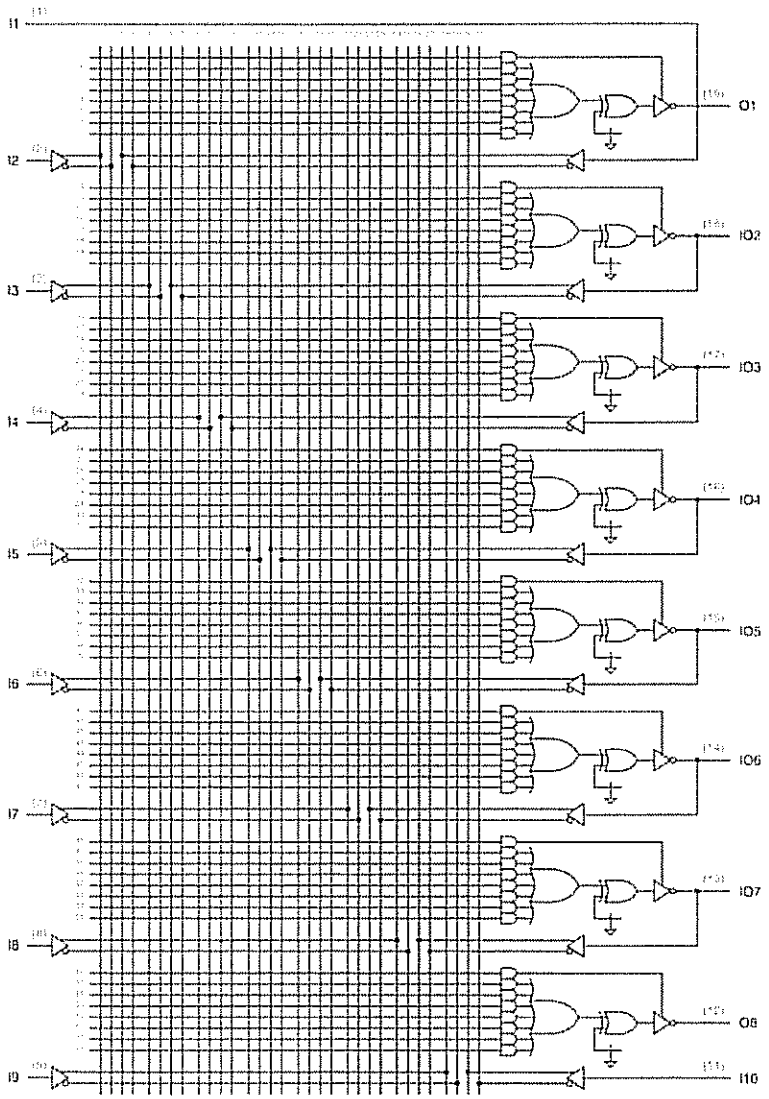


Figure 6-27

Logic diagram of the GAL16V8C.

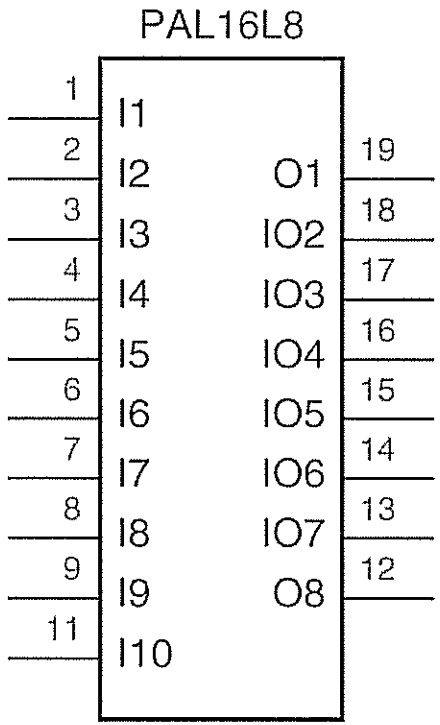


Figure 6-26

Logic symbol for the PAL16L8.

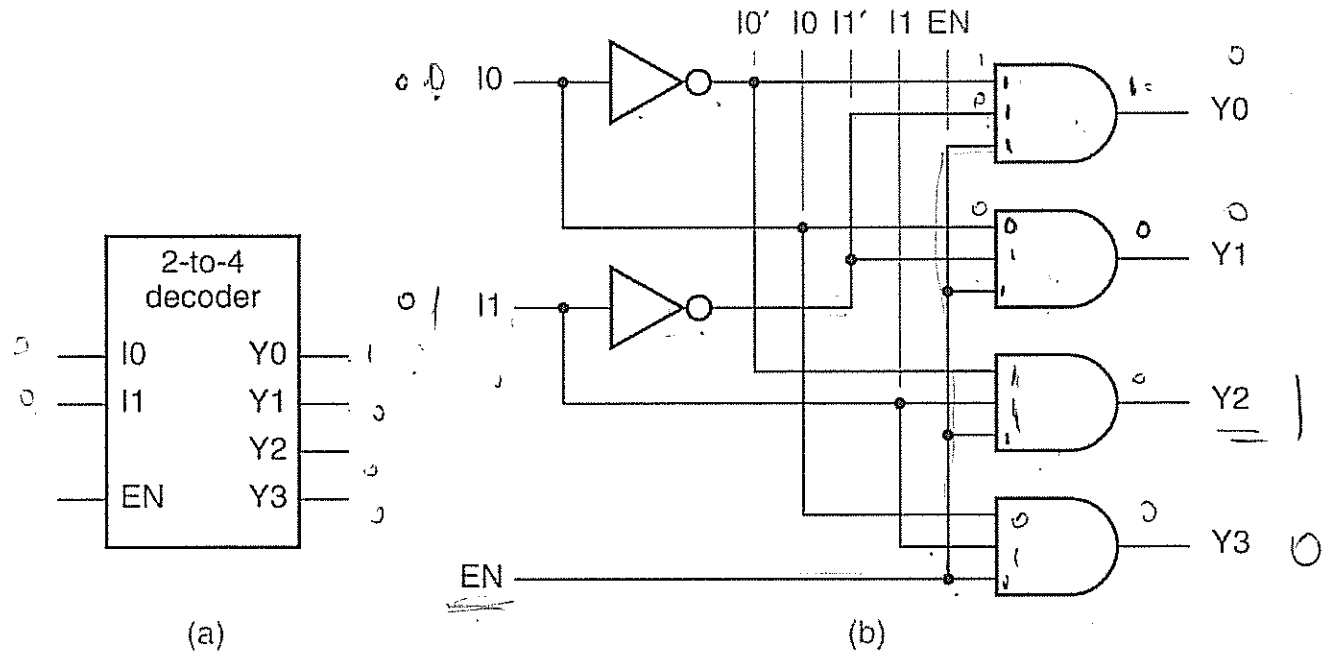


Figure 6-32

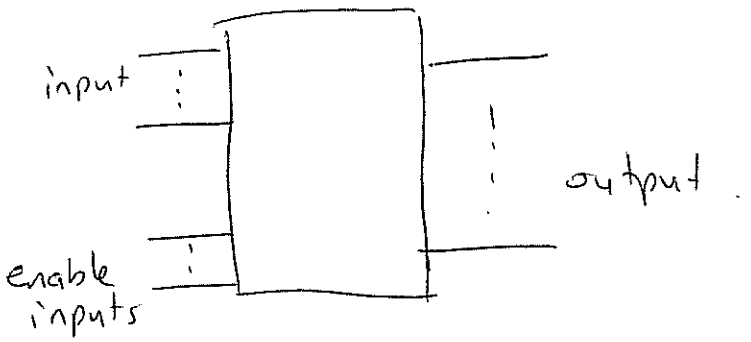
A 2-to-4 decoder: (a) inputs and outputs; (b) logic diagram.

Inputs			Outputs			
EN	I1	I0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Table 6-4

Truth table for a 2-to-4 binary decoder.

Decoders



Convert coded inputs to coded outputs.

input code generally has fewer bits than output.

1-out-of-m code outputs.

e.g. 1-out-of-4 code:

0001, 0010, 0100, 1000.

Binary Decoders:

n-bit binary input code, 1-out-of-2^n output code.

Don't care on K-maps: