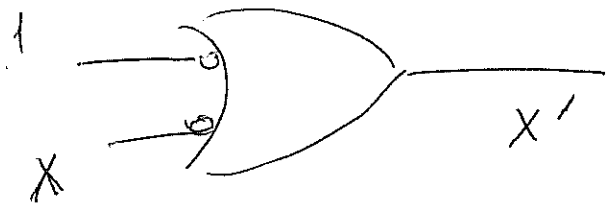
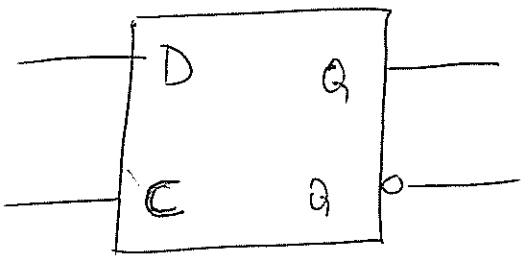
EECS 281, March 17, 2015



D - latch:



C	D	Q	QN
0	X	lastQ	lastQX
1	0	0	1
1	1	1	0

D latch is used to store bits of information.

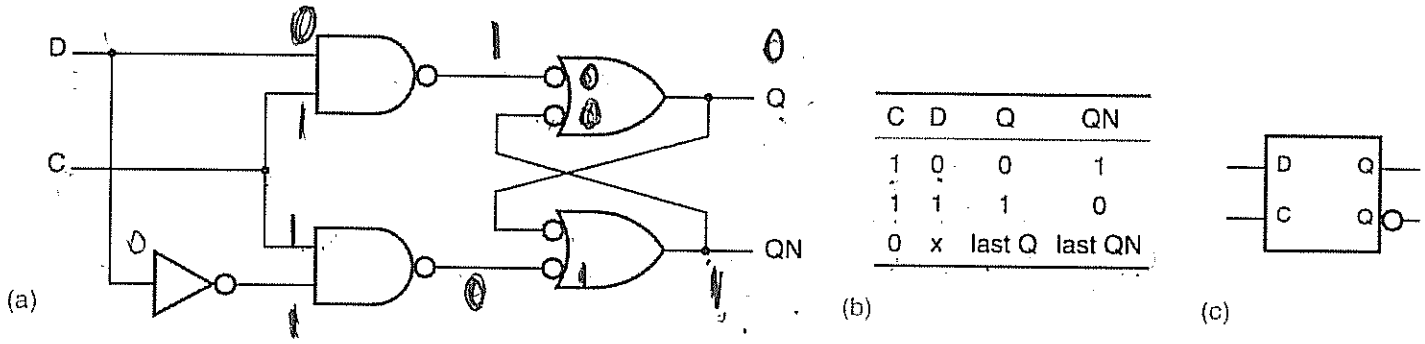


Figure 7-12

D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

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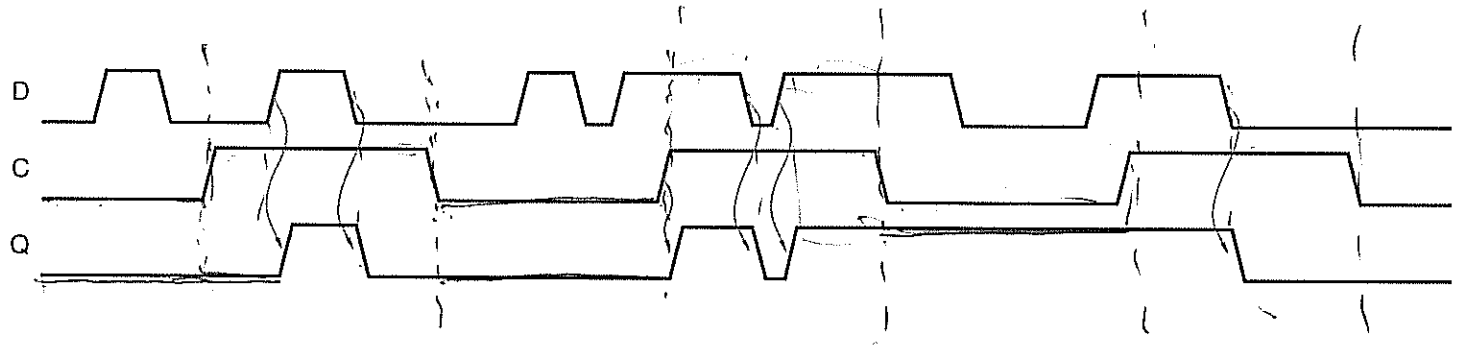

Figure 7-13

Functional behavior of a D latch for various inputs.

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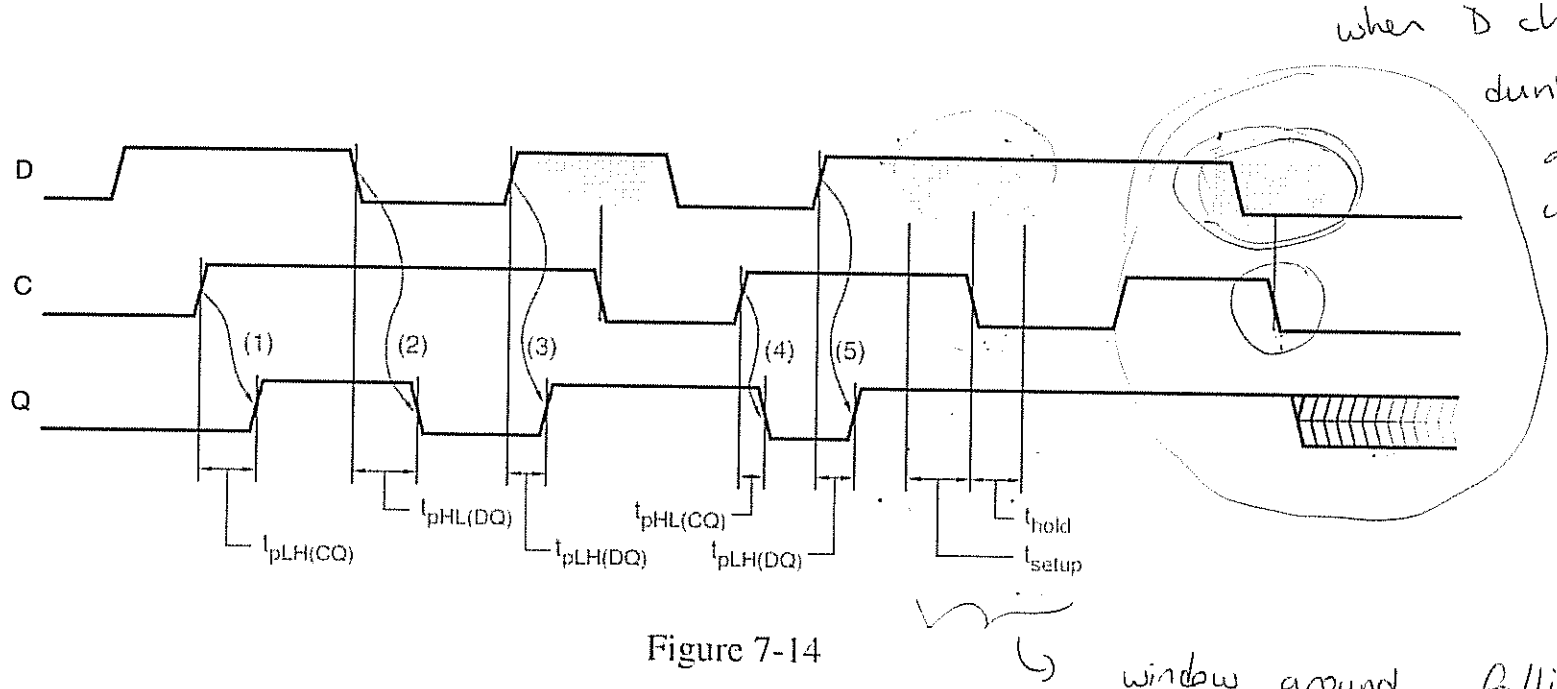
metastability: still a problem.



when D changes during setup- and hold-time window ⇒ output unpredictable.

Figure 7-14
Timing parameters for a D latch.

window around falling edge of C when D must NOT change.

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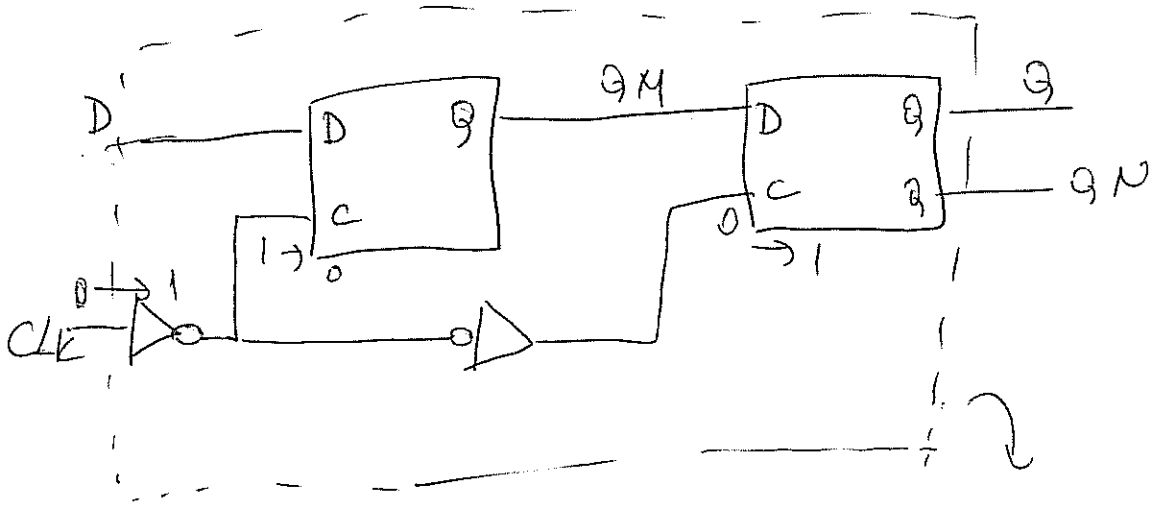
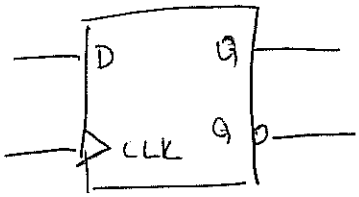
Positive - Edge Triggered D Flip - Flop



CLK = 0 → 1



D	CLK	Q	Q N
X	0	last Q	last Q N
X	1	last Q	last Q N
0	↑	0	1
1	↑	1	0

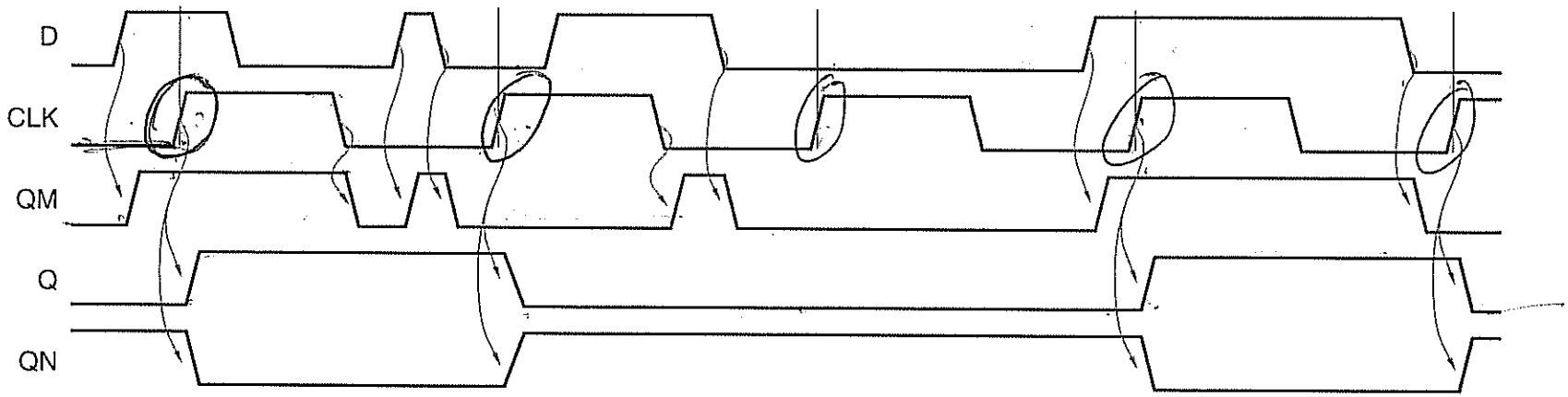


Figure 7-16

Functional behavior of a positive-edge-triggered D flip-flop.

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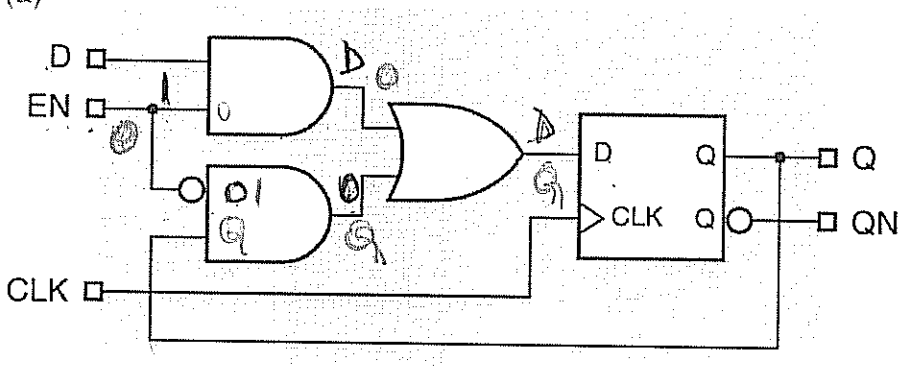
2-input mux controls the value applied to flip-flop D input.

EN = 1 ⇒ external D is input to internal D.

EN = 0 ⇒ current Q is used as input to internal D

(a)



(b)

D	EN	CLK	Q	QN
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	last Q	last QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN

(c)

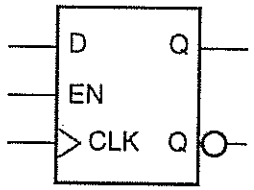


Figure 7-21

Positive-edge-triggered D flip-flop with enable: (a) circuit design; (b) function table; (c) logic symbol.

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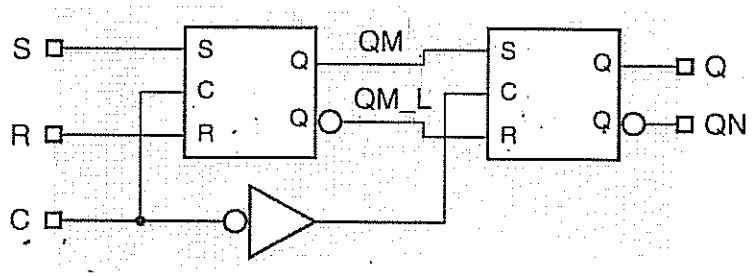
S-R flip-flop: changes output only at falling edge of C.
(negative-edge-triggered) output depends on input values not just at falling edge, but during entire interval when C = 1.

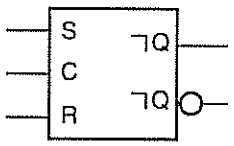
(a)



(b)

S	R	C	Q	QN
x	x	0	last Q	last QN
0	0	⊓	last Q	last QN
0	1	⊓	0	1
1	0	⊓	1	0
1	1	⊓	undef.	undef.

(c)



postponed output indicator: output does not change until C negated.

Figure 7-24

Master/slave S-R flip-flop: (a) circuit using S-R latches; (b) function table; (c) logic symbol.

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unpredictable: If both S = R = 1 at falling edge of C.

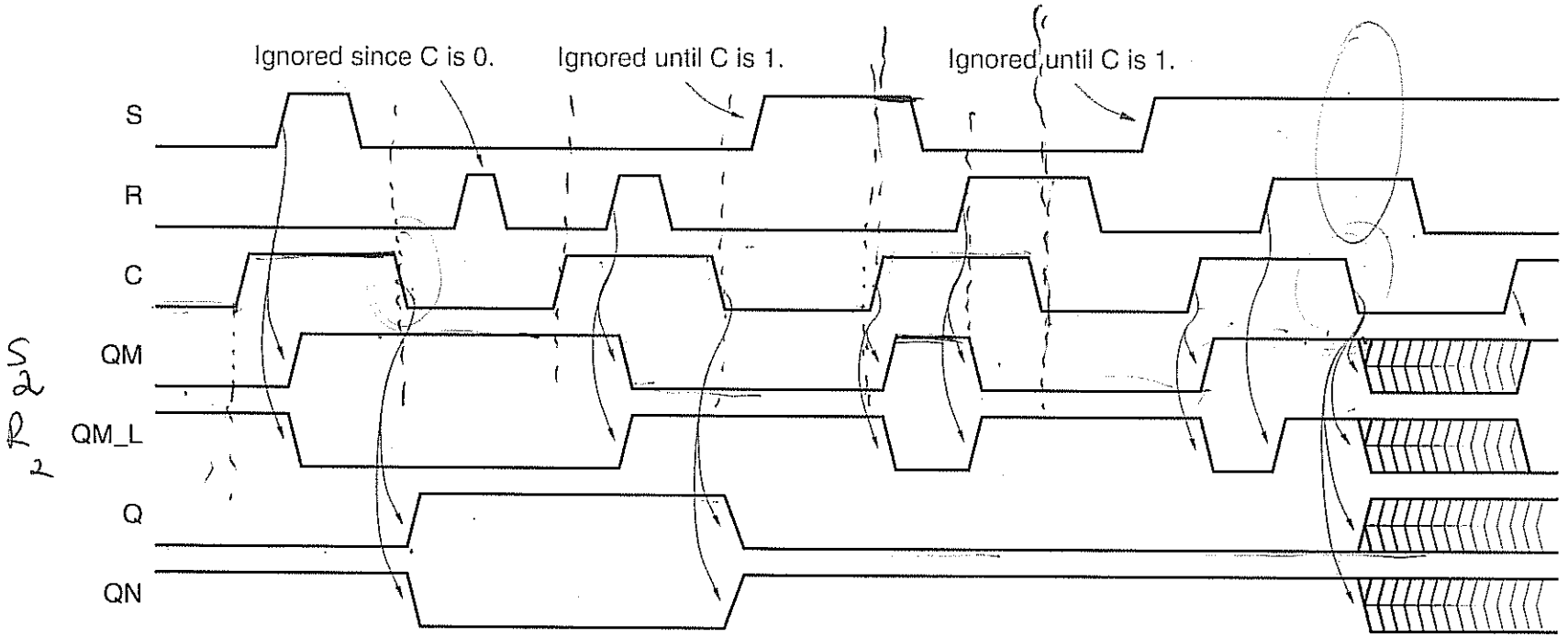

Figure 7-25
Internal and functional behavior of a master/slave S-R flip-flop.

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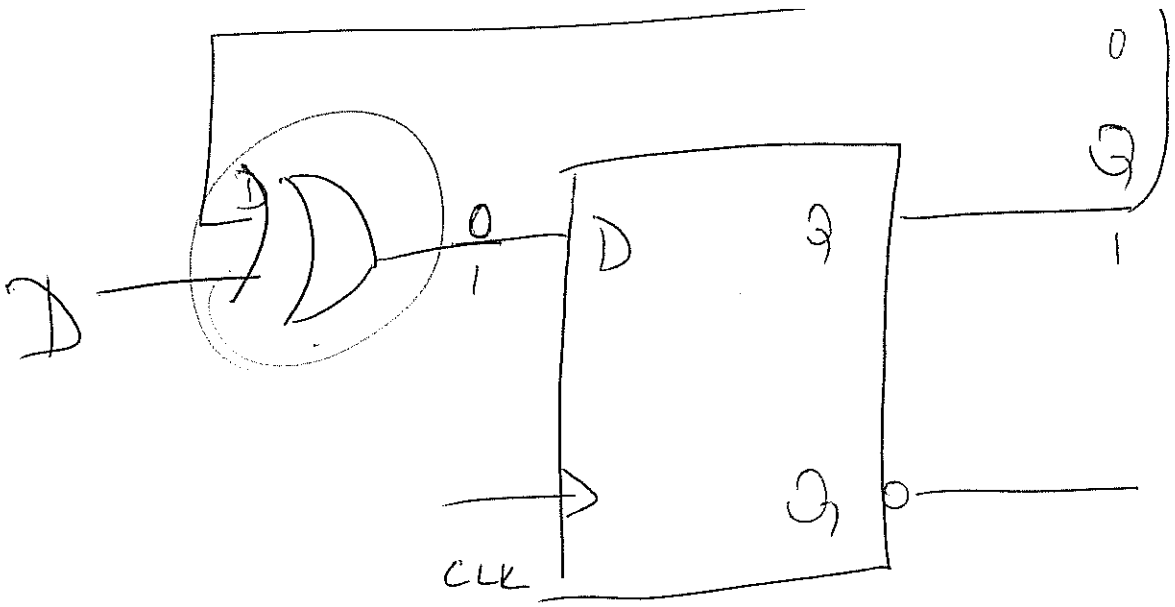

D	0	1	1	0	1	1
Q 0	0	1	0	0	1	0

Q	D	Q*
0	0	0
0	1	1
1	0	1
1	1	0