EECS 281, February 26, 2015

Multiplexer: digital switch, connects data from one of n sources to its output.

n sources of data, each b bits wide.

b output bits.

commercially available: $n = 1, 2, 4, 8, 16$

$b = 1, 2, 4$

s inputs that select among n sources.

$$n = 2^s$$

$$s = \log_2 n$$

EN: enable input. EN=0 $\Rightarrow$ all outputs are 0.

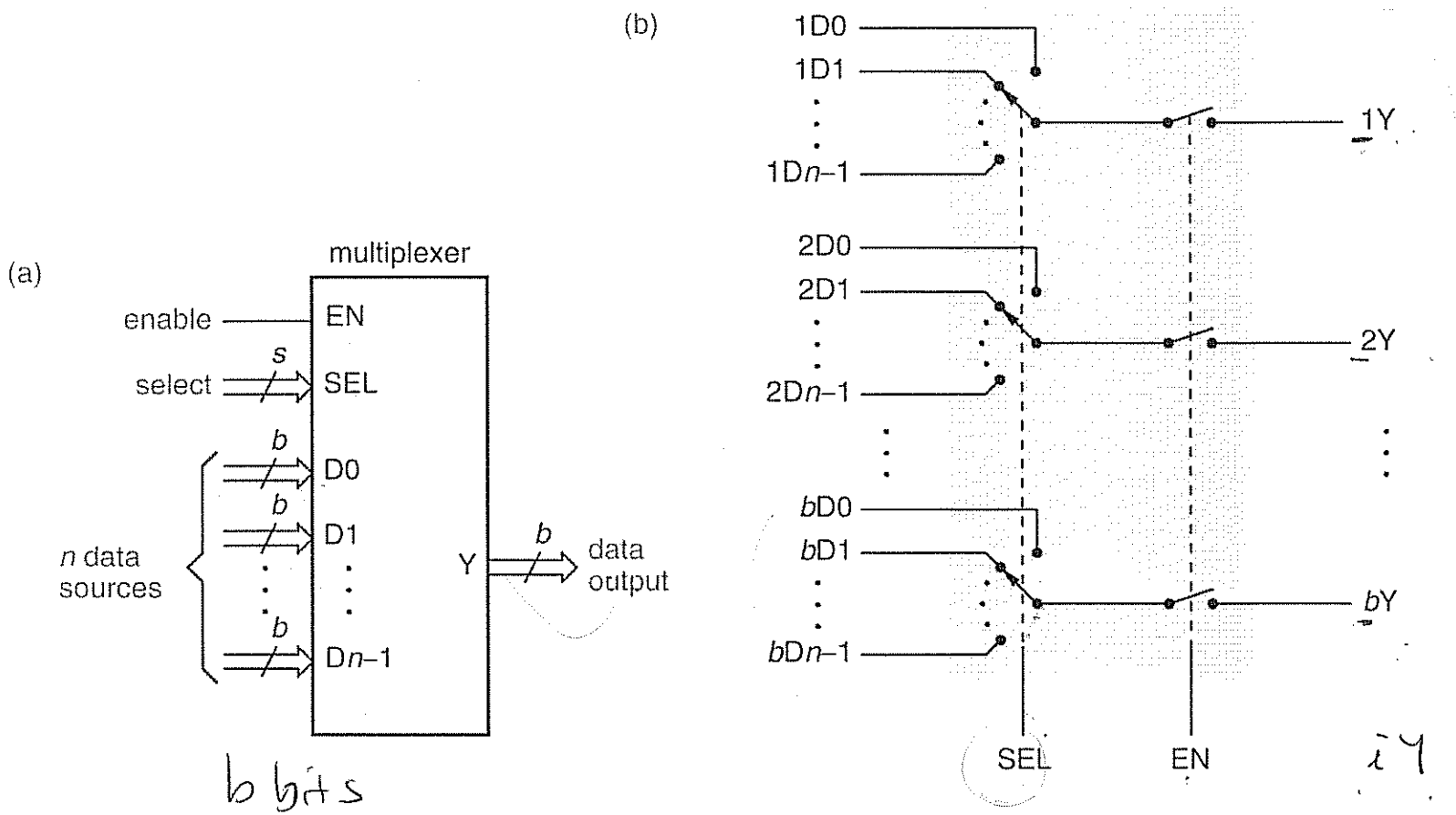


Figure 6-59

Multiplexer structure: (a) inputs and outputs; (b) functional equivalent.

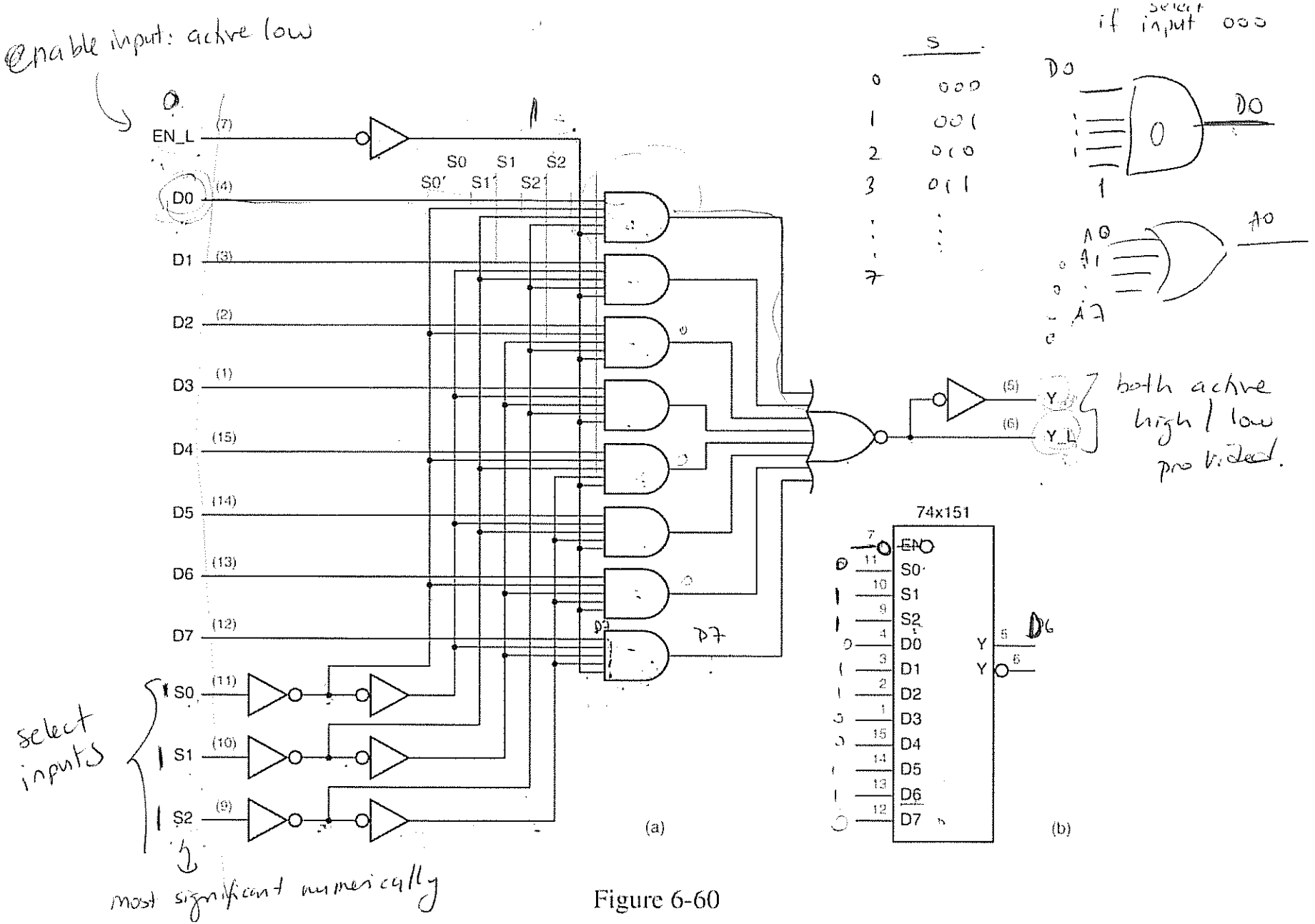


Figure 6-60

The 74×151 8-input, 1-bit multiplexer: (a) logic diagram; (b) traditional logic symbol.

Inputs				*Outputs*	
EN_L	S2	S1	S0	Y	Y_L
1	x	x	x	0	1
0	0	0	0	D0	D0′
0	0	0	1	D1	D1′
0	0	1	0	D2	D2′
0	0	1	1	D3	D3′
0	1	0	0	D4	D4′
0	1	0	1	D5	D5′
0	1	1	0	D6	D6′
0	1	1	1	D7	D7′

Table 6-42

Truth table for a 74×151 8-input, 1-bit multiplexer.

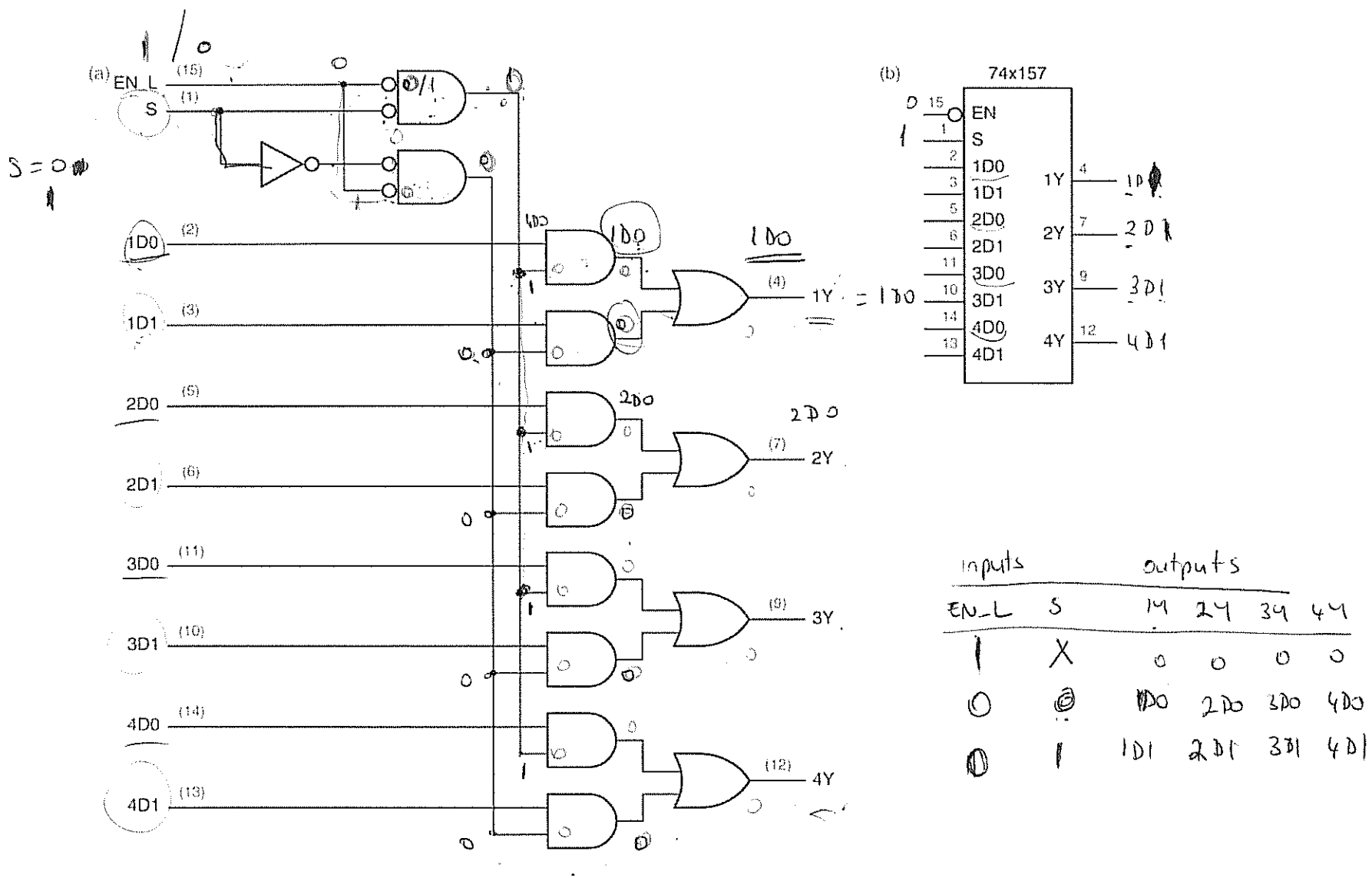


Figure 6-61

The 74×157 2-input, 4-bit multiplexer: (a) logic diagram; (b) traditional logic symbol.

Inputs		Outputs			
EN_L	S	1Y	2Y	3Y	4Y
1	x	0	0	0	0
0	0	1D0	2D0	3D0	4D0
0	1	1D1	2D1	3D1	4D1

Table 6-43

Truth table for a 74x157 2-input, 4-bit multiplexer.

$$iY = \sum_{j=0}^{n-1} EN \cdot M_j \cdot iD_j$$

iY: particular output bit

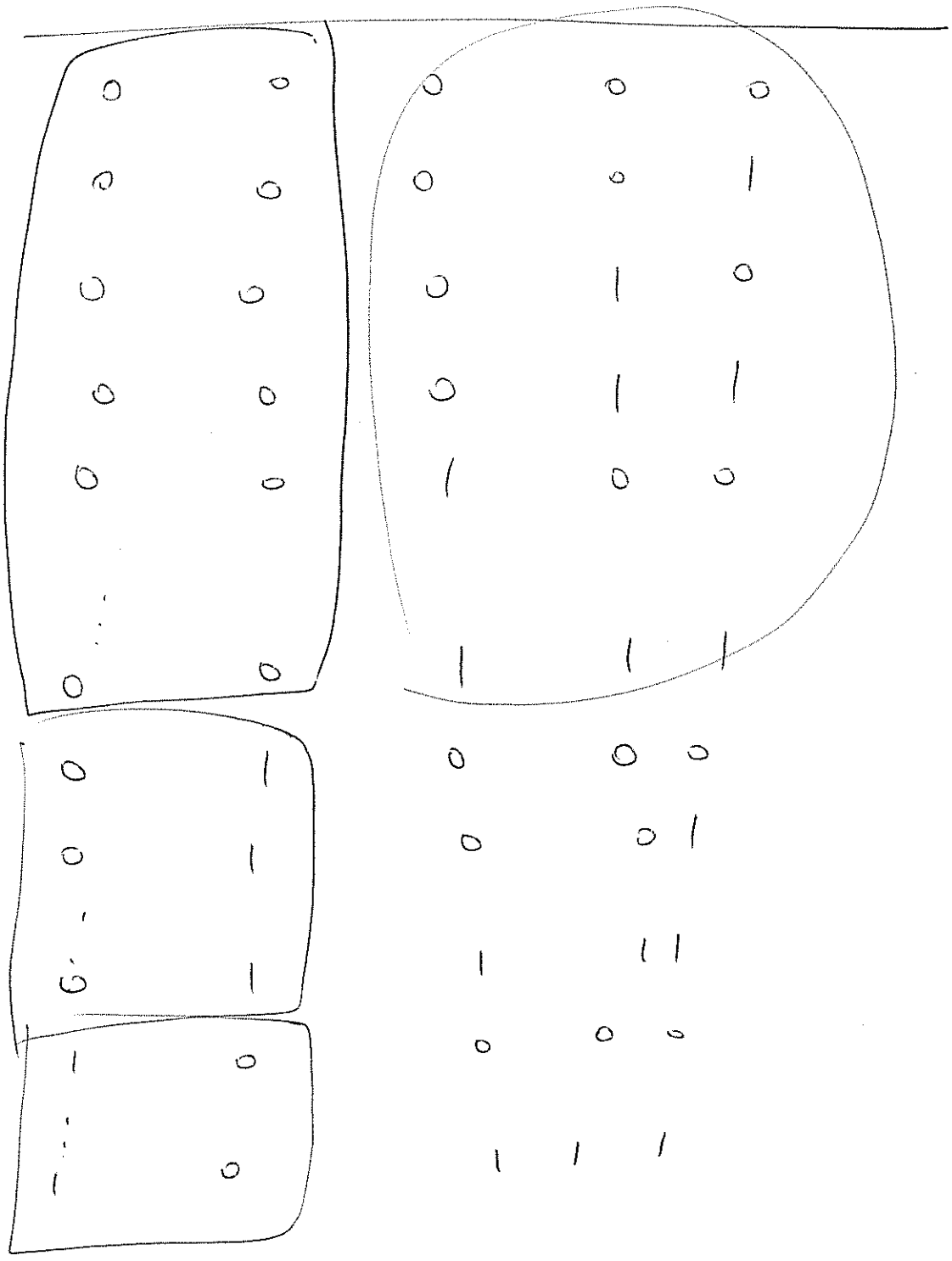
$(0 \leq i \leq b)$

iD_j : input bit i of source j

$0 \leq j \leq n-1$

M_j : minterm j of s select inputs.

example: 74 x 151



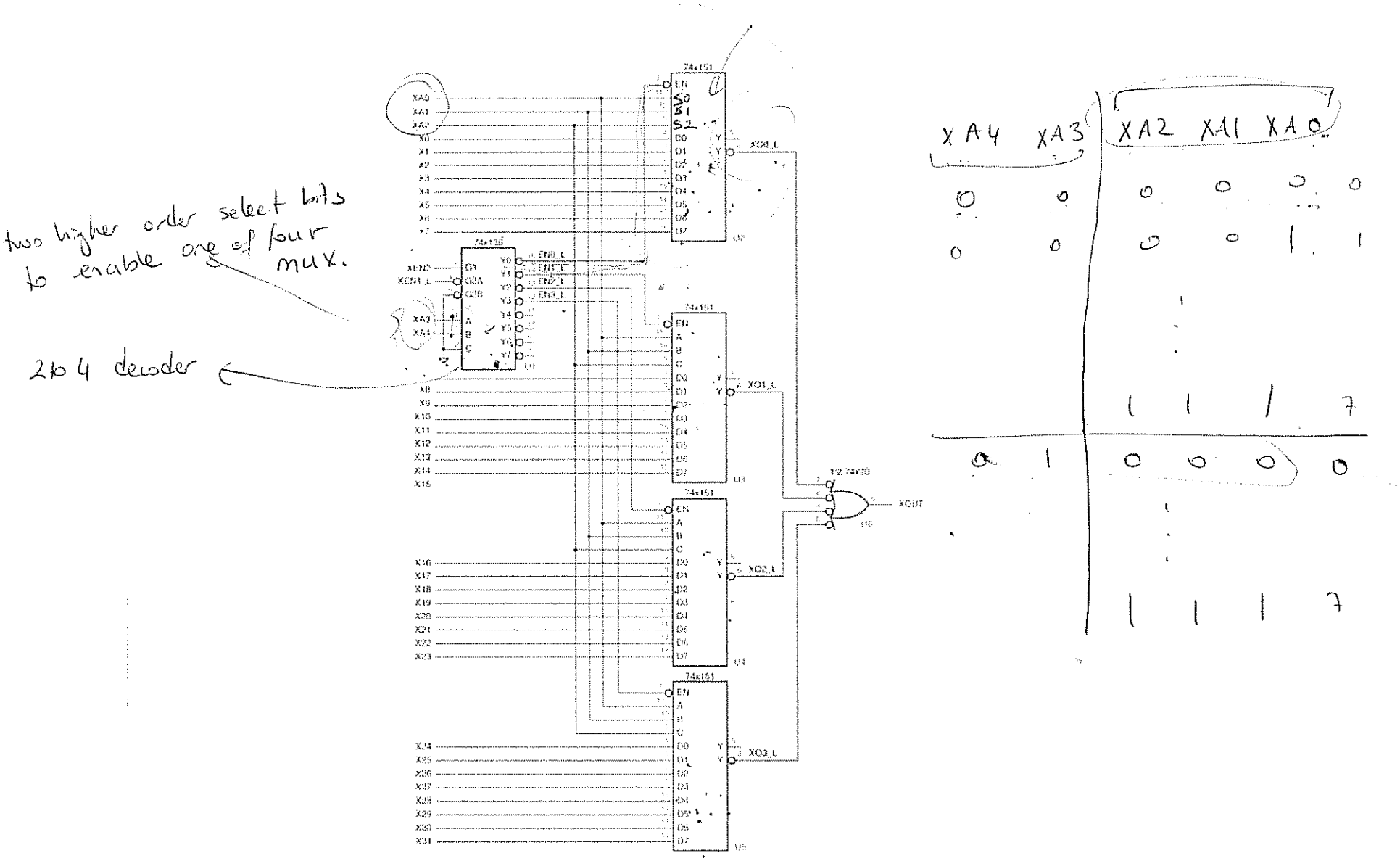


Figure 6-62

Combining 74×151s to make a 32-to-1 multiplexer.

Exclusive OR : XOR

2 input gate: output is 1 if exactly one of its inputs is 1.

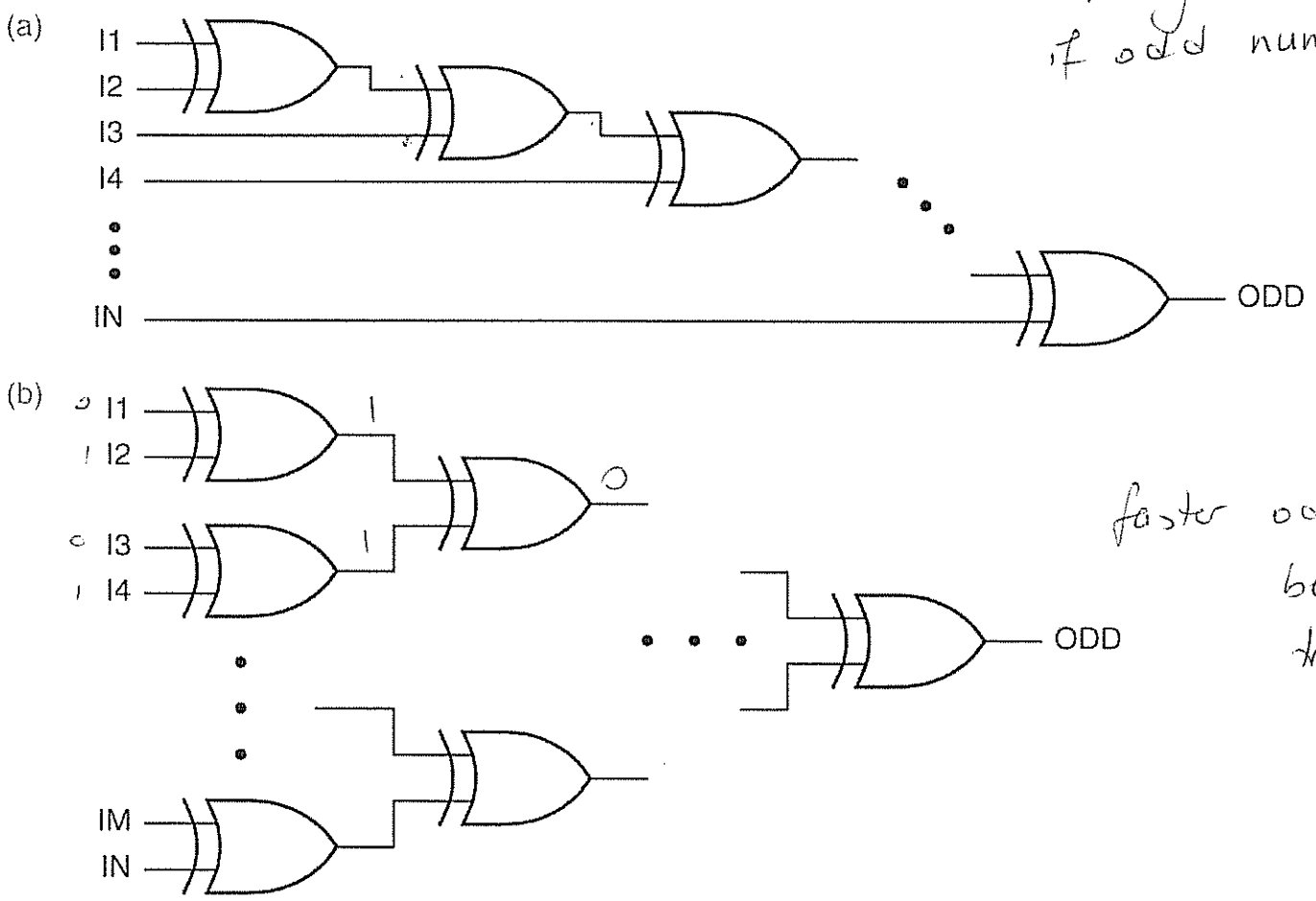
X	Y	$X \oplus Y$	$(X \oplus Y)'$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Exclusive NOR (XNOR) : Equivalence gate produces 1 output if its inputs are the same.

$$X \oplus Y = X' \cdot Y + X \cdot Y'$$

I1 I2 I3 I4 ... IN
0 1 0 1 ... 0

odd-parity circuit: output = 1 if odd number of inputs = 1.



faster odd parity because of tree structure like

Figure 6-70

Cascading XOR gates: (a) daisy-chain connection; (b) tree structure.

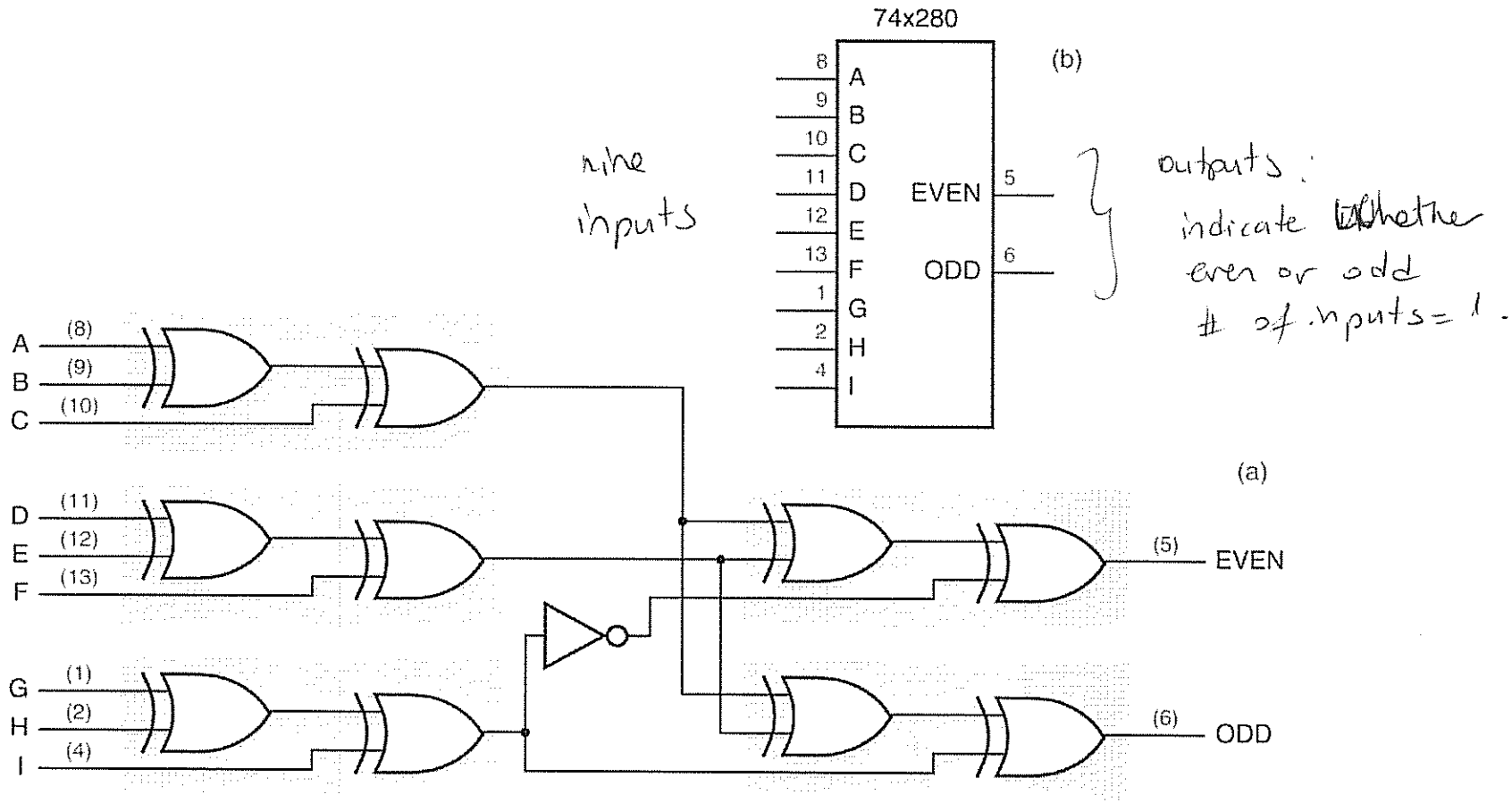


Figure 6-71

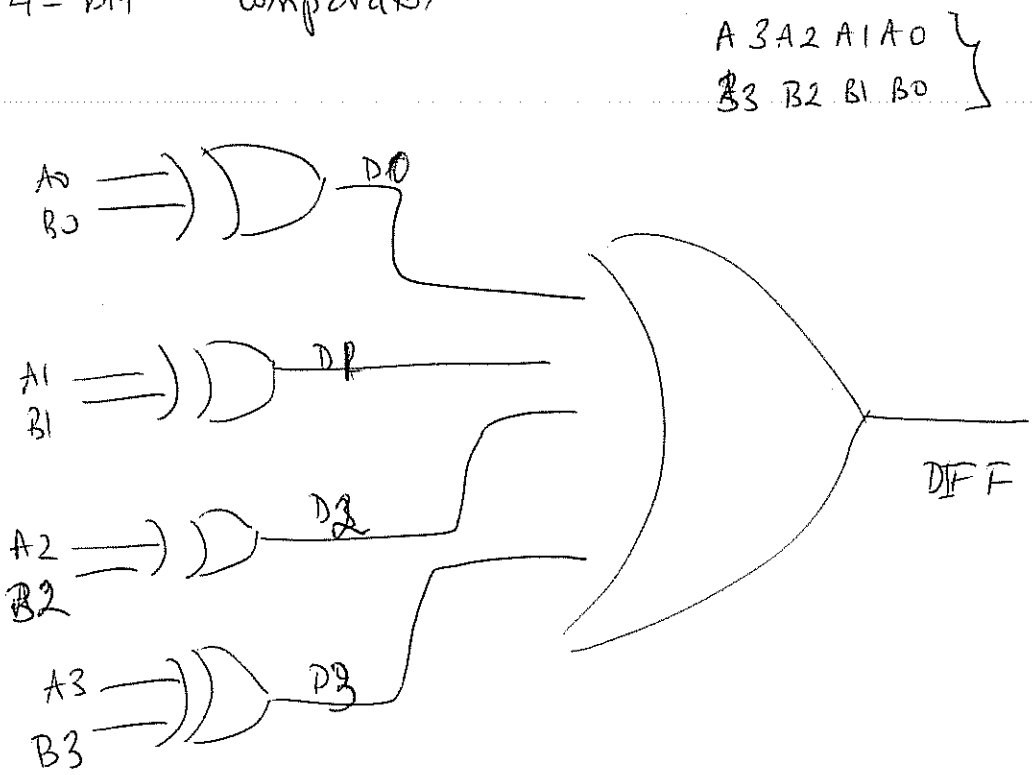
The 74x280 9-bit odd/ even parity generator: (a) logic diagram; (b) traditional logic symbol.

Comparators

a circuit that compares two binary words for equality.

If inputs are different ⇒ DIFF = 1

4-bit comparator



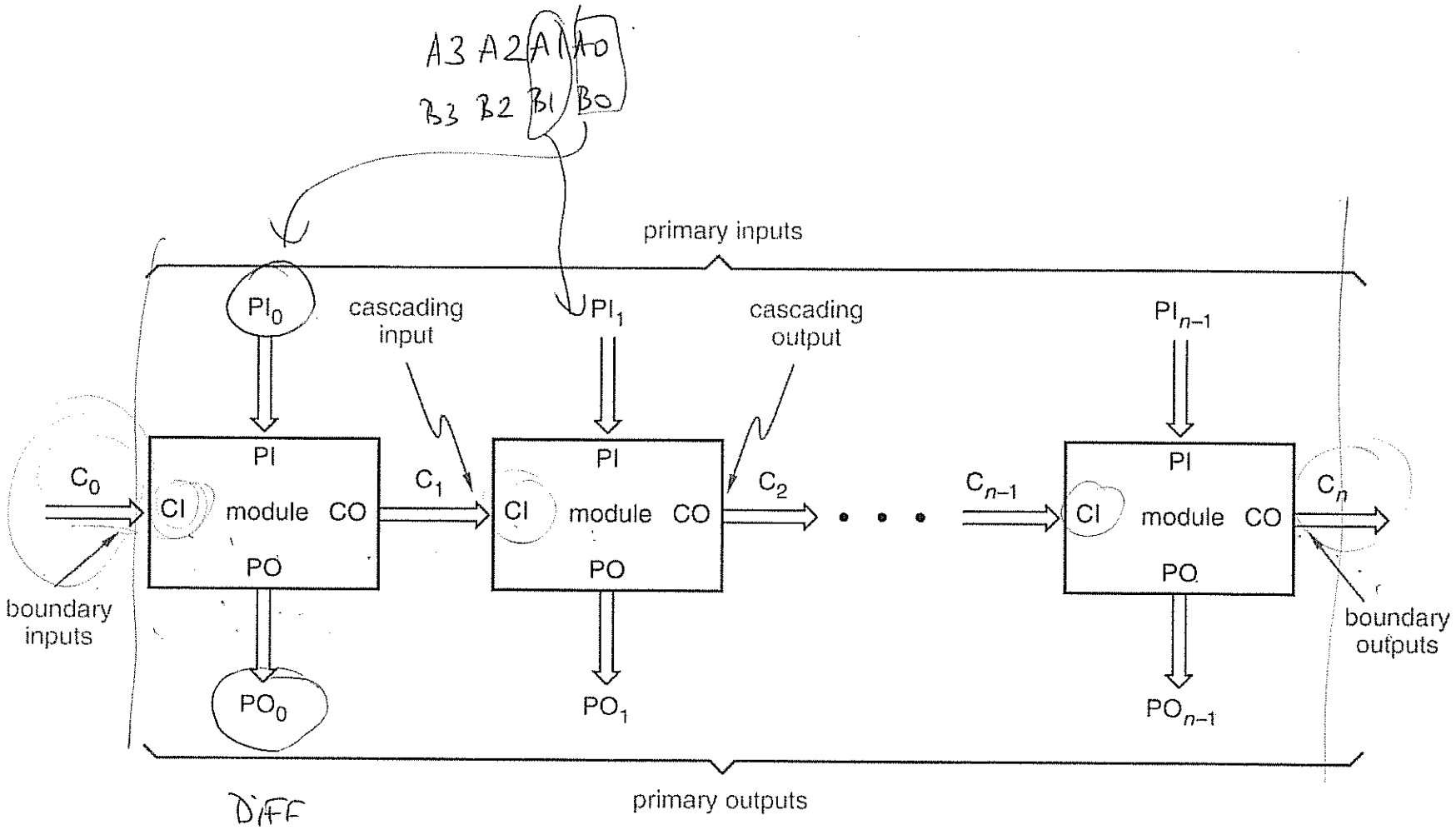


Figure 6-76

General structure of an iterative combinational circuit.

Example: Iterative comparator. (equivalence)