Constraint based scheduling of Weakly Consistent C programs for Reconfigurable Hardware

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Problem

Constraint
based
scheduling of
Weakly
Consistent C
programs for
Reconfigurable
Hardware

- Scheduling concurrent C programs for HLS.
- When using atomics, scheduling can be incorrect.
- Existing solution assumes no constraints on resources.

Current Approach

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- Introduce memory dependency edges to influence scheduling.
- Map each thread to an independent H/W Accelerator.
- No constraints on resources.

Proposed Solution: Sequentialize

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- Merge two or more concurrent threads to meet resource constraints.
- Give the merged program to be synthesized by the same HLS tool.
- Merging would also expose other thread-local optimizations in synthesis which may reduce clock cycles(why?).

Current Progress

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- Added shared memory accesses to coursework code base.
- Added new dependency order to respect memory consistency rules.
- Modified scheduling algorithm of coursework to handle shared memory programs.
- Identified a good benchmark to showcase advantage of merging.

Benchmark Programs

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```
a1 = c1 + d1;
b1 = e1 + f1;
```

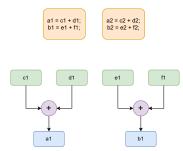
$$a2 = c2 + d2;$$

 $b2 = e2 + f2;$

- Change any access above to shared one eg: c1–¿cs.
- Do this for all memory accesses total 4096 possibilitie giving us 4096 programs.

Test Example 0: No shared memory

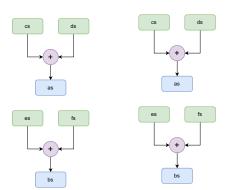
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Test Example 1: All Shared memory

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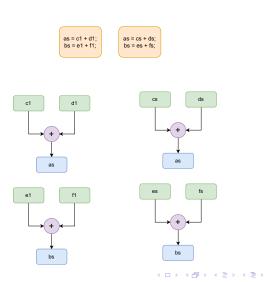
T1;T2



Test Example 2: Save Clock Cycles

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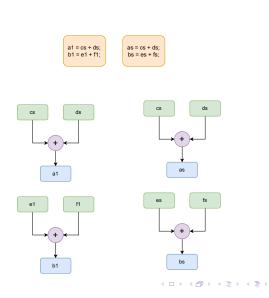
T2;T1



Test Example 3: Save Both Clock Cycles and Resources

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T1;T2

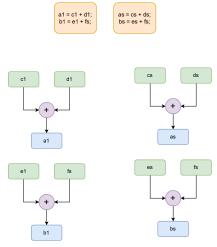


Can do even better

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T2-T1-T1-T2



Pending

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- Global Analysis to identify best merging combination.
- Implement Redundant R/W elimination to improve scheduling (identified how to implement this)
- Graphs of relevance summarizing all 4096 examples and the effect of merging different ways.