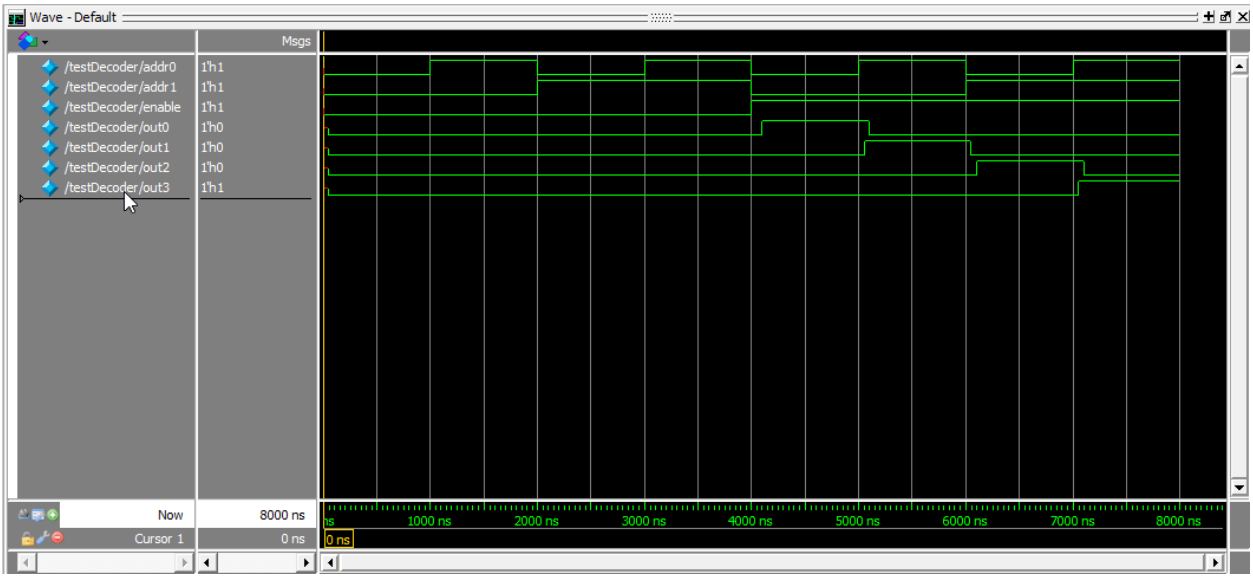
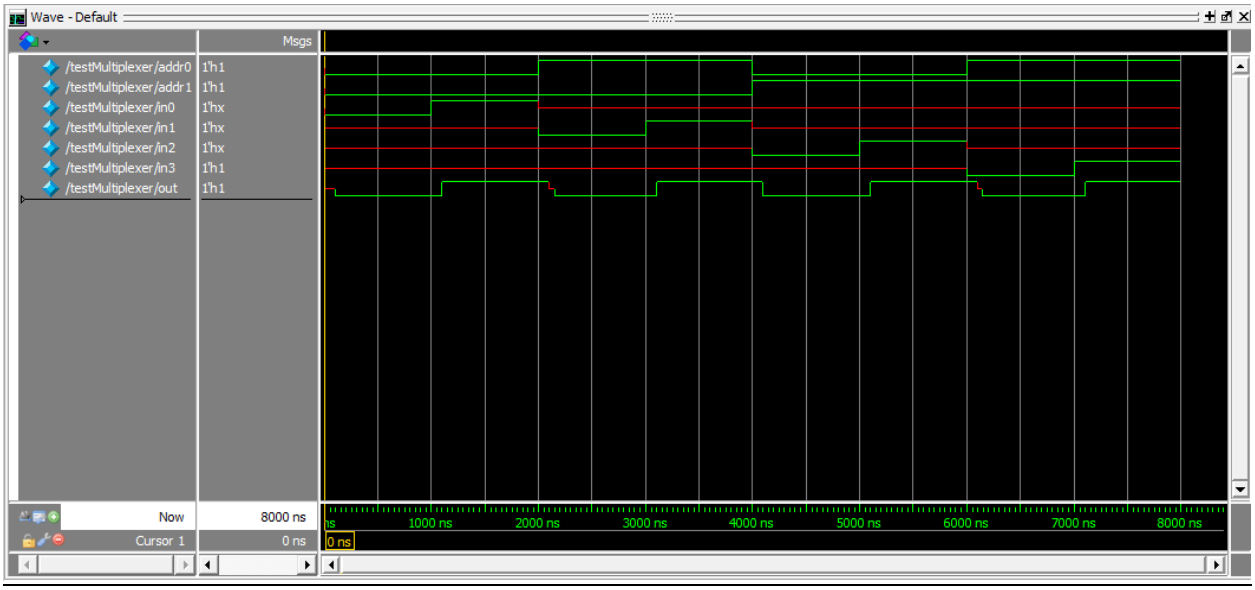
Decoder




```
# vsim
# Start time: 20:45:58 on Sep 24,2015
# Loading work.testDecoder
# Loading work.structuralDecoder
# En A0 A1| O0 O1 O2 O3 | Expected Output
# 0  0  0 |  0  0  0  0 | All false
# 0  1  0 |  0  0  0  0 | All false
# 0  0  1 |  0  0  0  0 | All false
# 0  1  1 |  0  0  0  0 | All false
# 1  0  0 |  1  0  0  0 | O0 Only
# 1  1  0 |  0  1  0  0 | O1 Only
# 1  0  1 |  0  0  1  0 | O2 Only
# 1  1  1 |  0  0  0  1 | O3 Only
# 0 ns
# 8400 ns
```

This tests all possible cases for the Decoder. The results match the expected outcome.

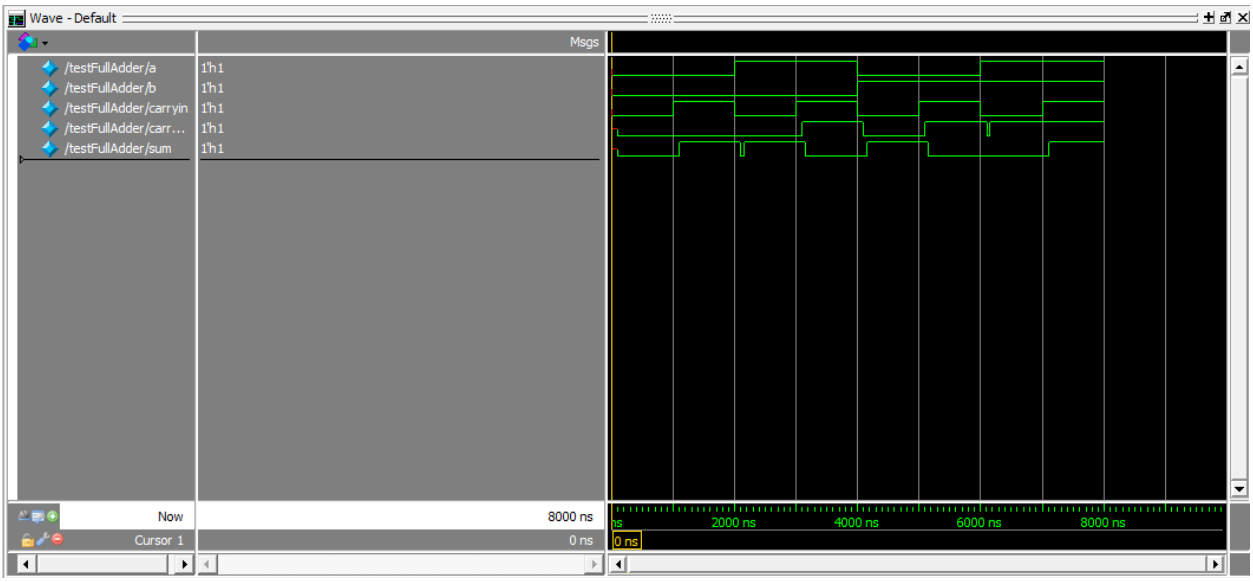
Multiplexer




```
# vsim
# Start time: 21:14:55 on Sep 24,2015
# Loading work.testMultiplexer
# Loading work.structuralMultiplexer
# A1 A0| I3 I2 I1 I0 | O | Expected Output
# 0  0 |  x  x  x  0 | 0 | 0
# 0  0 |  x  x  x  1 | 1 | 1
# 0  1 |  x  x  0  x | 0 | 0
# 0  1 |  x  x  1  x | 1 | 1
# 1  0 |  x  0  x  x | 0 | 0
# 1  0 |  x  1  x  x | 1 | 1
# 1  1 |  0  x  x  x | 0 | 0
# 1  1 |  1  x  x  x | 1 | 1
# 0 ns
# 8400 ns
```

We only need to test the cases above, rather than every case because the multiplexer only chooses one input to pass through to the output. Therefore, the other inputs are non-essential.

Full Adder




```
# vsim
# Start time: 20:46:04 on Sep 24,2015
# Loading work.testFullAdder
# Loading work.structuralFullAdder
# A  B  Ci | Co  O  | Expected Output
# 0  0  0  |  0  0  | 0  0
# 0  0  1  |  0  1  | 0  1
# 1  0  0  |  0  1  | 0  1
# 1  0  1  |  1  0  | 1  0
# 0  1  0  |  0  1  | 0  1
# 0  1  1  |  1  0  | 1  0
# 1  1  0  |  1  0  | 1  0
# 1  1  1  |  1  1  | 1  1
# 0 ns
# 8400 ns
```

This tests every possible case for the Full Adder. There is a slight timing anomaly that can be seen in the wave form graph above.