Computer Architecture: Midterm

Due on Nov 15, 2015

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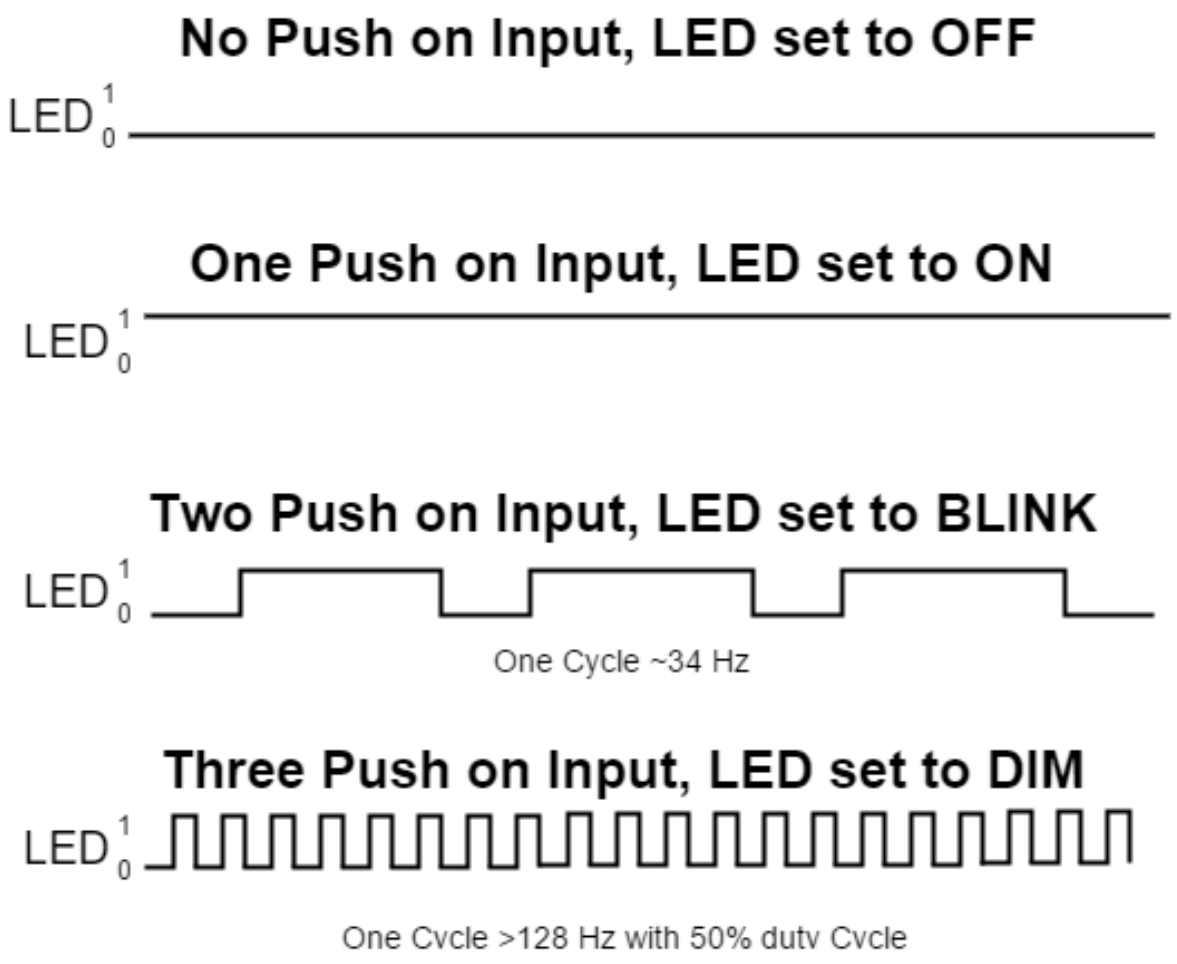

Figure 1: The waveforms above show the operation modes of the Bike Light Controller

Specification Document

The input to the Bike Light Controller is one Button. The output to the Bike Light Controller is on LED.
With the provided clock speed of 32,768 Hz, producing an output with 50% duty cycle at a frequency of 16,384 Hz will provide the proper waveform for a Dim setting. To produce a Blink setting, alternate every 1000 clock cycles to produce a flash on the LED at 32 Hz. See Figure 1 on page 2 to see the graphical representation of the modes described.

To control the state of the Bike Light, a Finite State Machine will cycle through the modes. With the four modes, (Off, On, Blink, and Dim) there are four states that the FSM can take. Each push of the button push should advance the state by one. The light starts on state OFF and to returns to OFF on the forth button push. See Figure 2 on page 3 for a graphical representation.

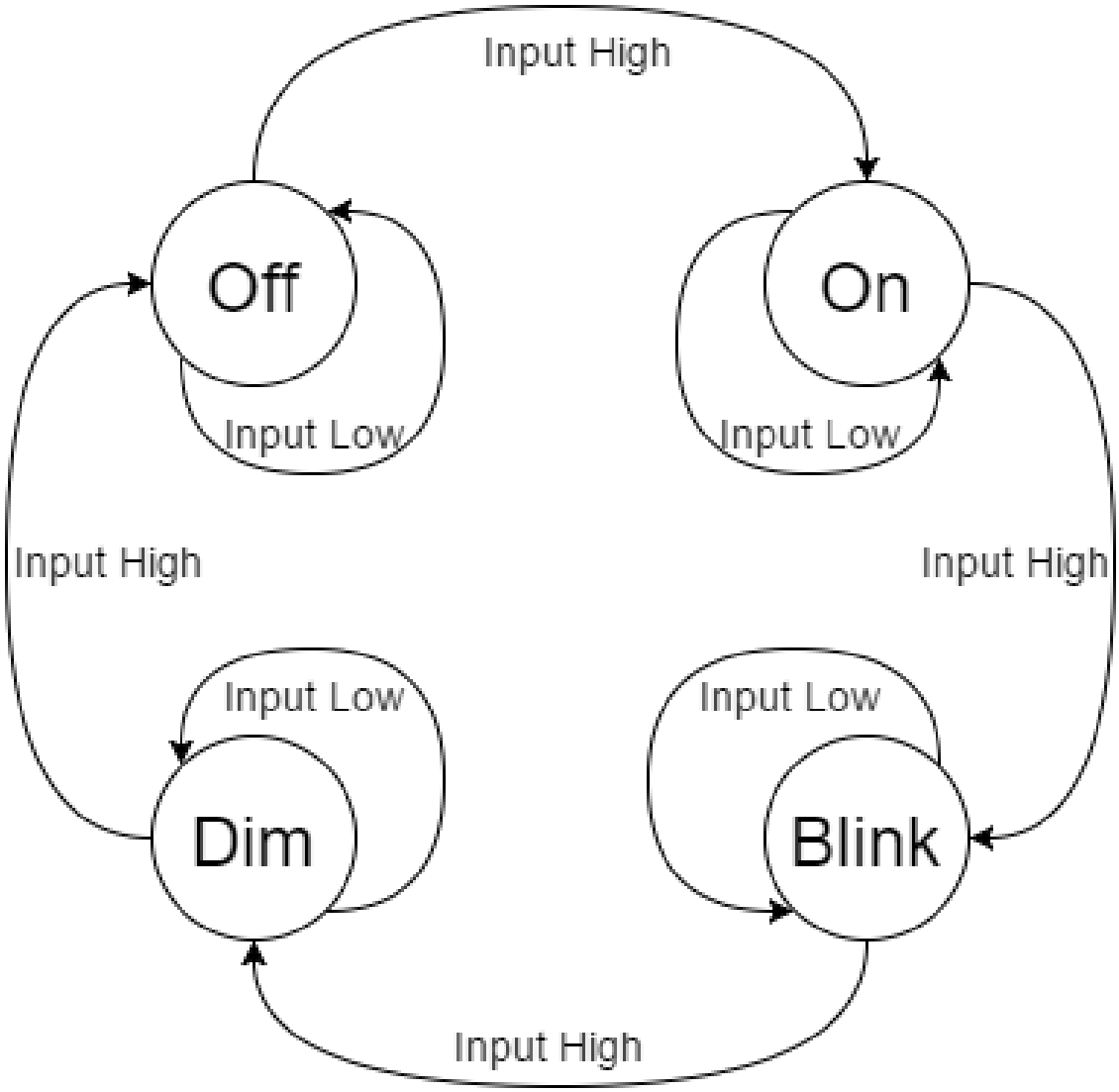

Figure 2: The Finite State Machine Diagram

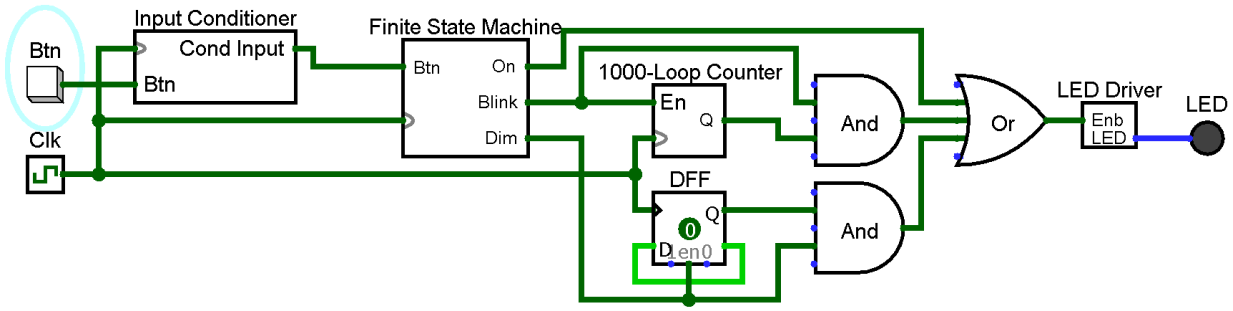

Figure 3: The block diagram shows each unit needed to create a working bike light controller

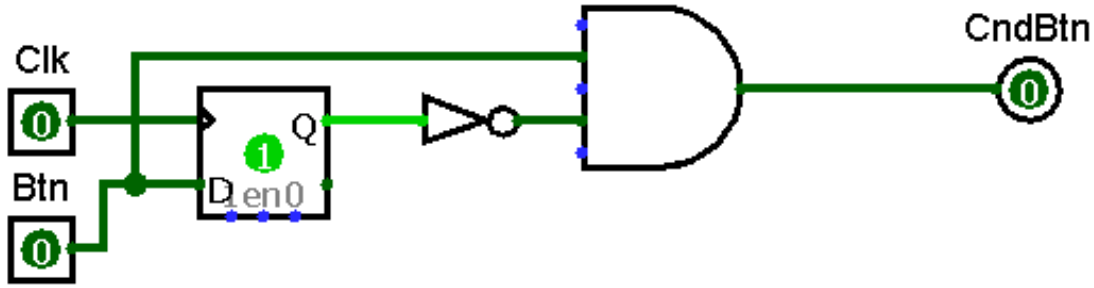

Figure 4: The Input Conditioner

Block Diagram

See Figure 3 To implement the controller to meet the requirements laid out in the Specification Document, the button must control the finite state machine and select the mode. To ensure that the FSM only moves one mode per button push, an input conditioner is implemented. The Loop Counter is in charge of creating the delay to produce the 32 Hz blink function. The DFF halves the clock rate while producing a 50% duty cycle. The two AND gates require an enable for the signals from the DIM or the BLINK functions to reach the LED driver. The LED driver powers the LED when the enable is active.

Schematics

See Figure 4 to analyze the input conditioner. This circuit uses precise timing to produce one positive pulse every time the button is pressed. This pulse lasts one clock cycle, no matter how long the button is pressed. The inputs to this circuit are a clock and button. The button runs to the DFF and an AND gate. The clock is used on the DFF. The output is a conditioned input, a single pulse, the width of one clock cycle. The total cost of this

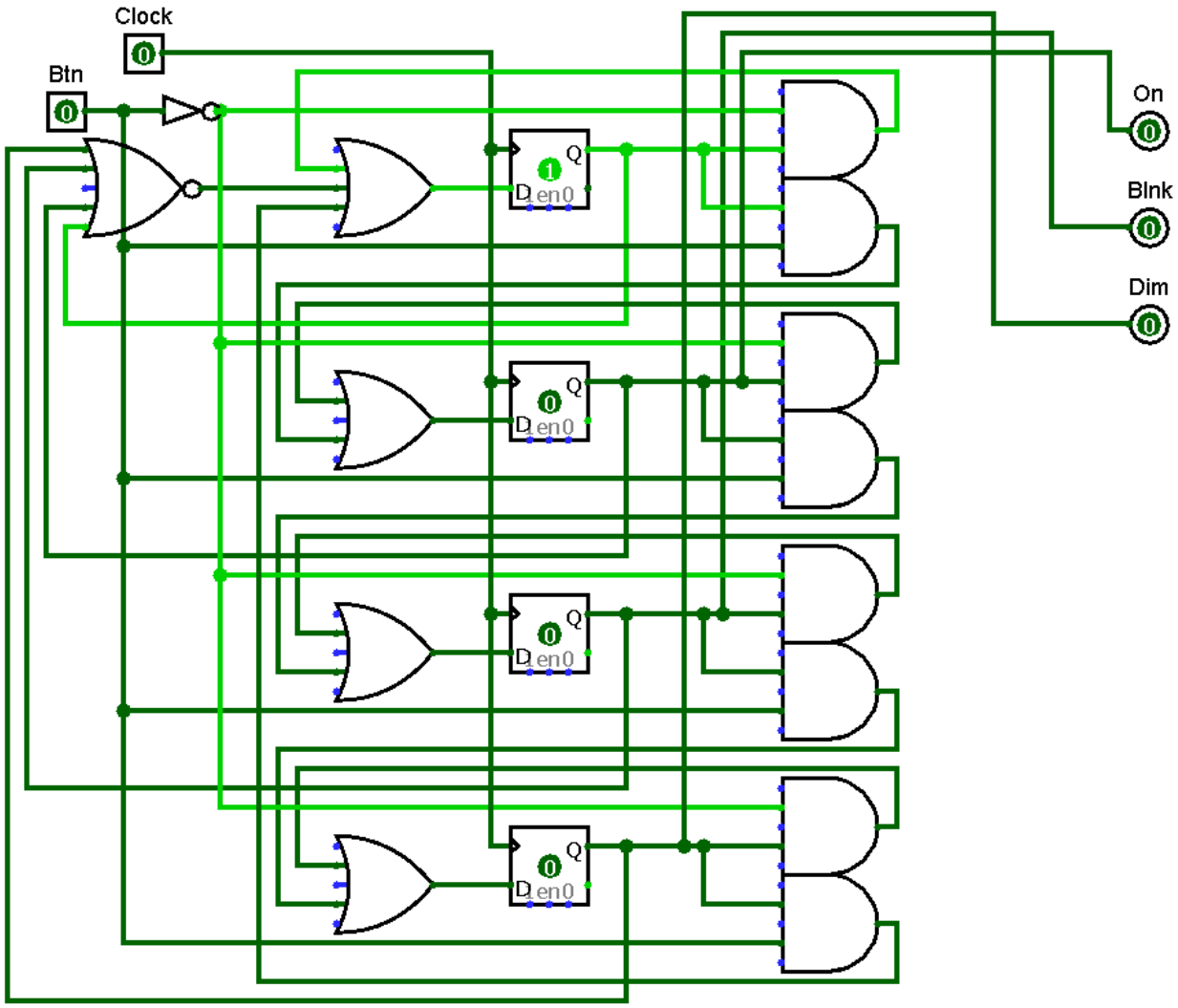

Figure 5: The Finite State Machine Schematic

schematic is 17.

See Figure 5 to analyze the finite state machine. This signal moves between the DFFs when the button is pressed. To prime the circuit, the XNOR gate checks if all other DFF outputs are low. If so, set the input to the DFF which triggers the OFF mode to high. The inputs to this circuit are a conditioned button and the clock. The outputs are an enable for each mode other than off. The modes are in the order: OFF ON BLINK DIM. This cycles back to OFF if the button is hit when the light is at DIM. The 4-input XNOR gate has a cost of 4. The 3-input OR gate has a cost of 4. The 3 2-input OR gate have total cost of 9. The 4 DFFs have a total cost of 52. The 8 2-input AND gates have a total cost of 24. All of this, plus the one inverter leads to a total cost of 94.

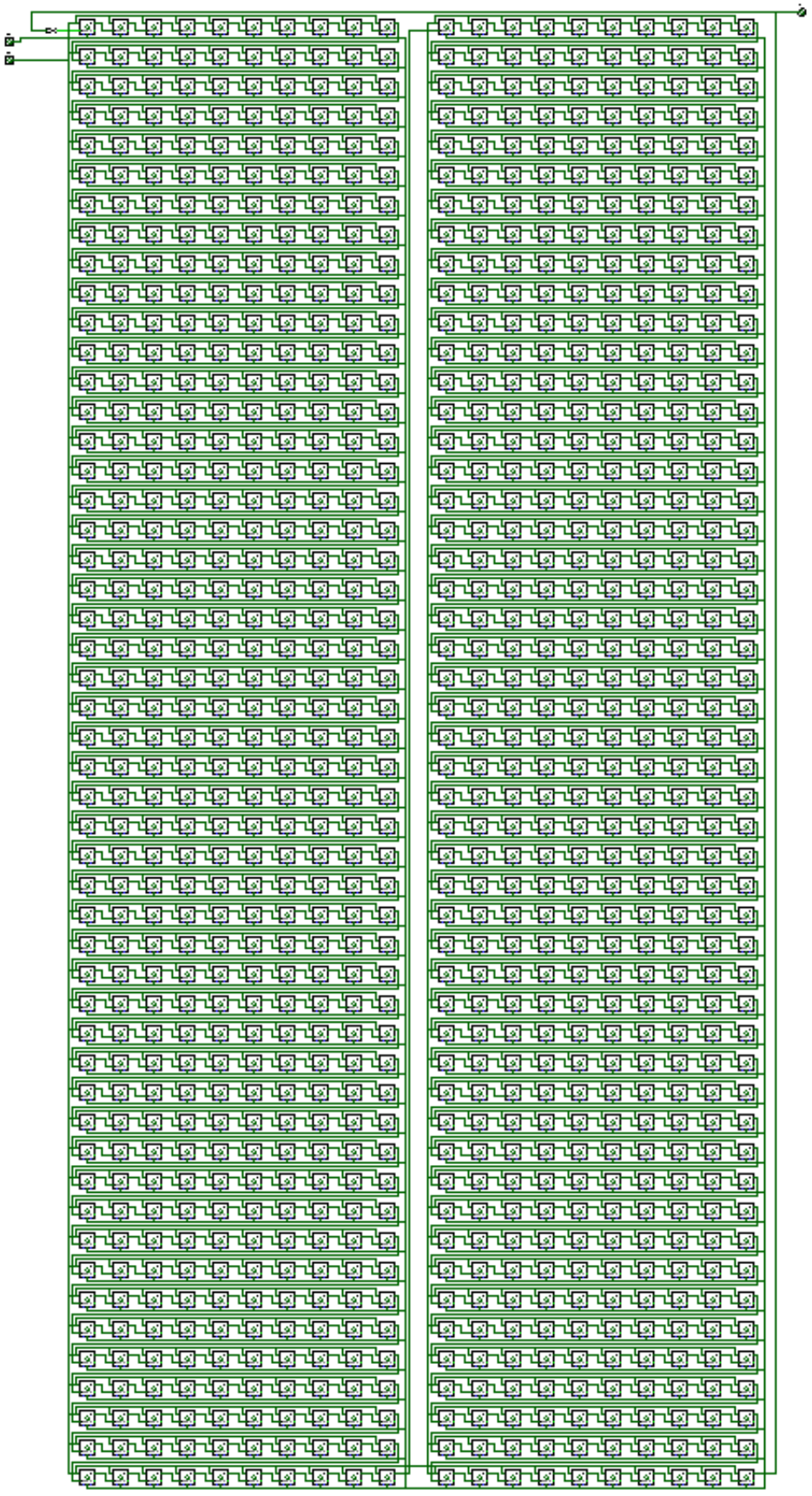

Figure 6: The Loop Counter used to slow the Clk for BLINK mode

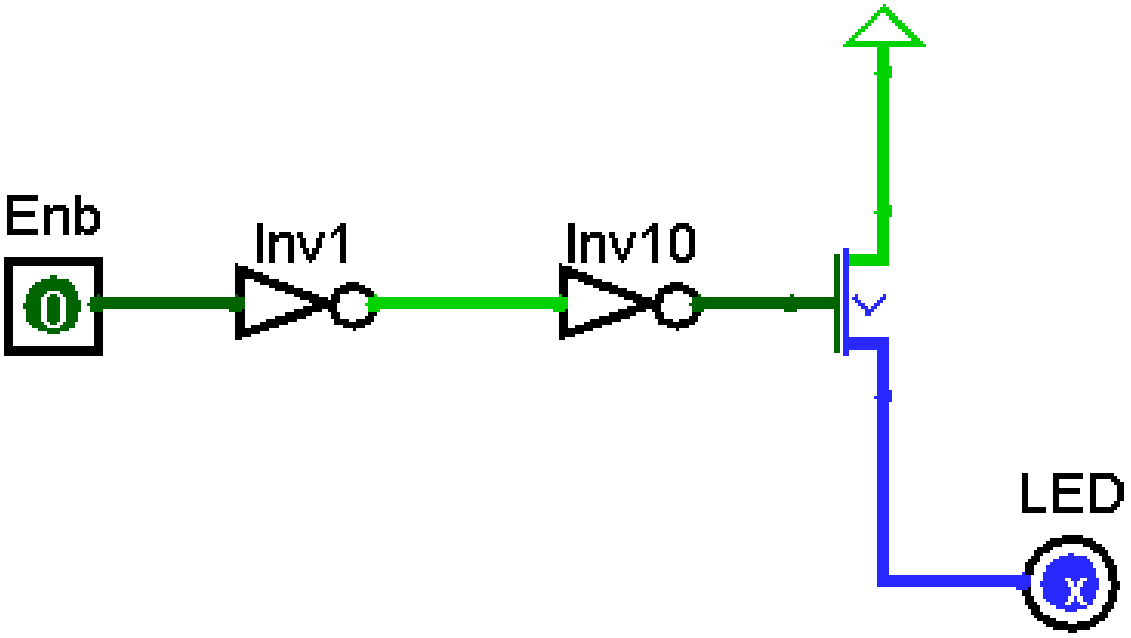

Figure 7: The Loop Counter used to slow the Clk for BLINK mode

See Figure 6 to briefly look at the Loop Counter. The signal is passed from one DFF to the next. Since there are 1000 DFFs in a row here, it takes 1000 clock cycles to move the signal from the first input, to the last. Since the clock rate is 32,768 Hz, this produces a a flip-flop rate of 32 Hz. The inputs here are an enable, which triggers all the DFFs, allowing the loop to continue, and a clock for the DFFs. The output is the Q of the last DFF in the chain. This will change value every 1000 clock cycles. The space used here is equivalent to 1000 DFF and one inverter, or 20001.

See Figure 7 to briefly look at the LED Driver. Since the LED I used in my circuit only has a power in line, I reversed the transistor to an N-Mos which sources the Vin line. The other end of the LED would normally be connected to ground(Not shown). This circuit has an enable which is driven by any of the modes from the finite state machine. The output is the driven LED signal, amplified enough to provide proper power to the LED. The total cost of this unit is 211, as per the spec sheet.

With all of the individual units now properly costed, The main circuit is left. The clock has an intrinsic cost of 2. The 2 2-input AND gates sum to 6. The 3-input OR gate has a cost of 4. These costs, along with the rest of the circuit sums to a total space cost of 20335. With a smaller loop, the cost could be greatly reduced.