**COEN 313 – Digital System Design II**  **Jafar Abbas**

Winter 2017 – February 13th 2017 26346650

**Objectives**

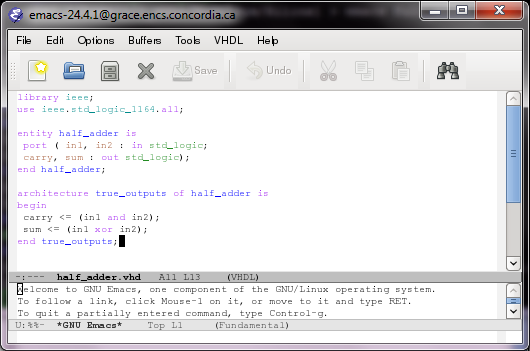
The objective of this intrudoctory lab experiment is to become acquainted with the VHDL simulation software tool, logic synthesis tools, and FPGA implementation software tools and to learn the rudiments of ModelSim DO files.

**Procedure**

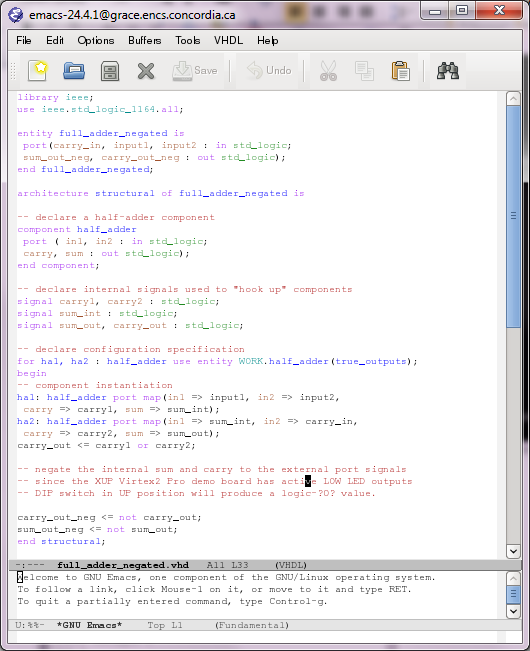
This lab follows the procedure outlined in Parts I, II, III, and IV of the tutorial “Digital Logic Simulation and Synthesis Using Modelsim, Precision RTL, and Xilinx ISE”. The end-goal is to simulate, synthesize and download to the Xilinx FPGA board the full adder example given in Part II of the tutorial.

**Results**

The full adder is built upon a half adder design show below:

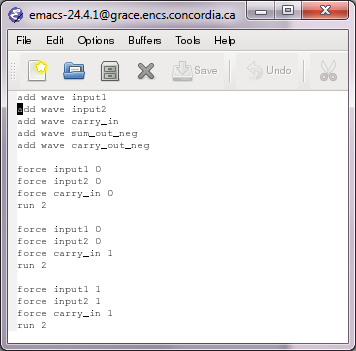


Using the half-adder, we construct our full adder show below:

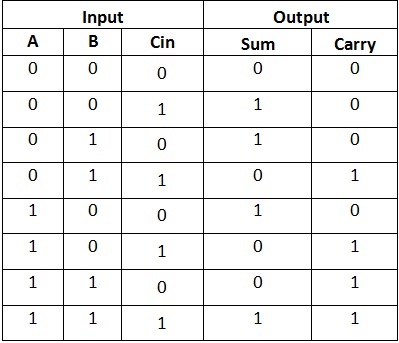


The DO file used to simulate our design:

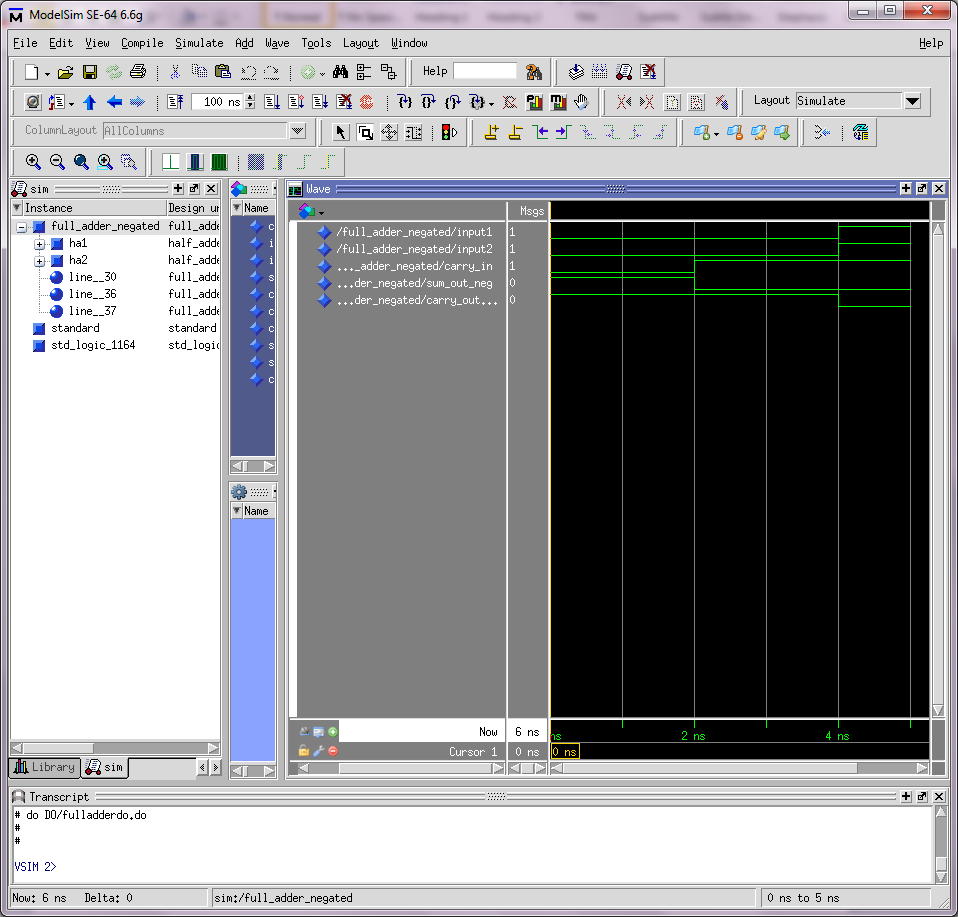
It is by no means comprehensive but the idea is to show the DO file can be used to test pre-defined inputs and expected outputs.



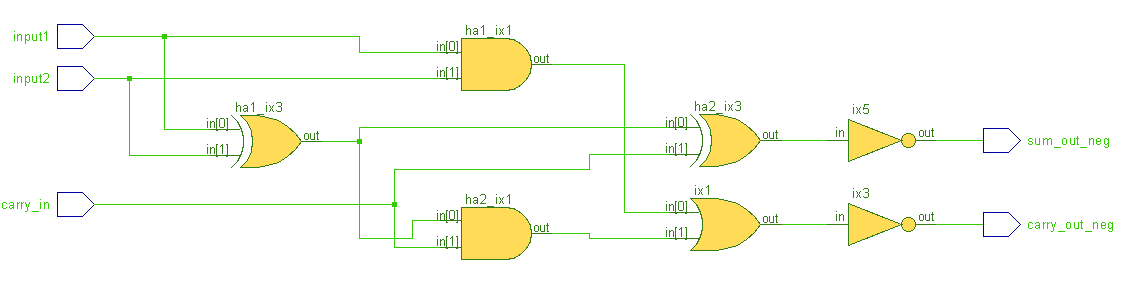
The truth table associated with a full-adder. This is used to build our DO file and later used during the demonstration to prove our implementation is valid.

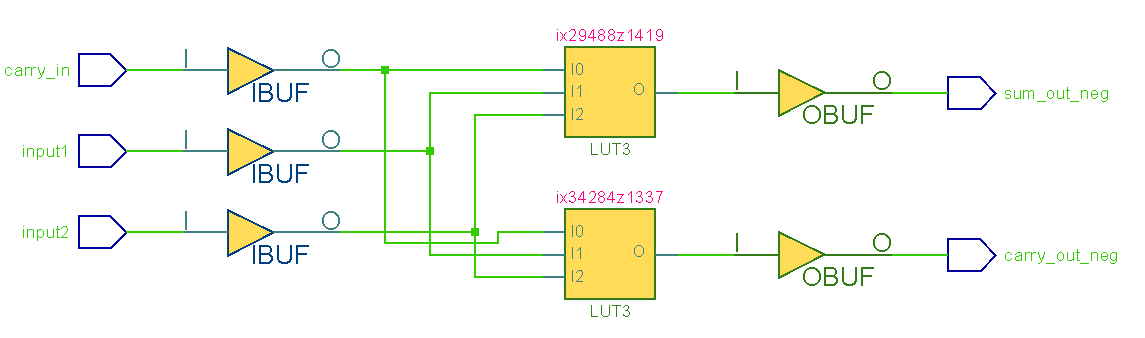


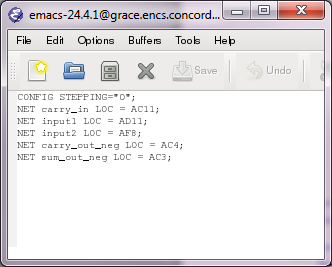
We can visualize the results of our DO file in the following screenshot by watching the waveform changing over time:

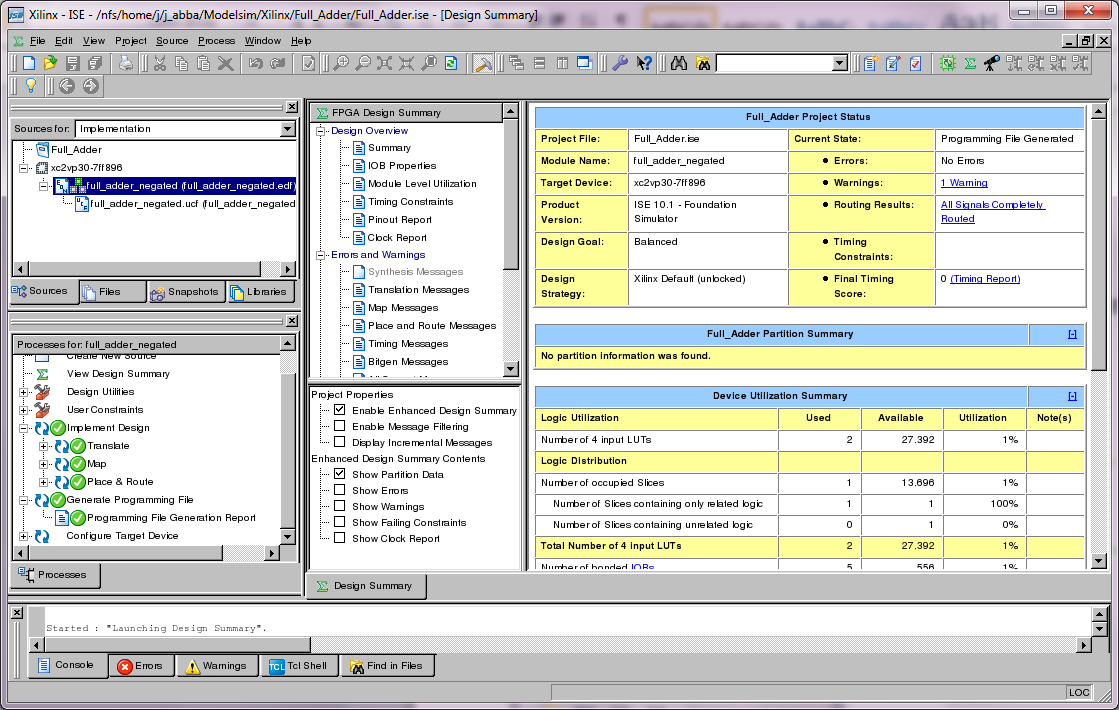


After synthesis, the following gate-level logical circuit is generated for our full adder:



The previous logical diagram can also represented by its corresponding hardware mapping:

After completing the hardware mapping, also the following given configuration file was used:



**Conclusion**

This lab experiment was a successful introduction to the implementation of digital circuits. The process involves VHDL simulation software tools, logic synthesis tools, and FPGA implementation software tools and application of DO files.

**Questions:**

1. What is the advantage of using the -r option in a force command within a DO file?

The –r option in the force command is used to repeat the action.

The advantage of this method is to easily create a periodic clock signal over many cycles without typing out many force commands repeatedly.

1. Briefly explain two methods of creating a repeating periodic signal using DO files.

Method 1: Use two separate force commands (with –r option) with shifted periods:

Example:

force clk 1 2 -r 4

force clk 0 4 -r 4

Method 2: Combined force command with –r option:

Example:

force clk 1 2, 0 4 -r 4