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ECEN 5730 – Fall 2025

Board 2 Report: Switching noise with good and bad layout

Objective

The objective of this lab is to demonstrate best measurement practices for measuring switching noise and how layout decisions affect switching noise in a PCB.

Plan of record

- Design two circuits: one following best practices (continuous ground plane and close decoupling capacitor) and one with poor practices (no ground plane, distant decoupling capacitor).
- Each circuit can switch to 5V or 3.3V power.
- Create a clock signal of about 500 Hz and about 50% duty cycle.
- A switch to selectively connect the 555 output to either the good or bad layout.
- Calculate the current through the 50Ω resistor load.
- Extract the Thevenin resistance at the output pin of the inverter IC
- Add isolation switch between the output of the LDO and a 22uF filter capacitor

Component Listing

The bill of materials is listed in the table below.

Name	Quantity	Name	Quantity	Name	Quantity
22uF	5	AMS1117-3.3	1	2Pin Header	7
1uF	1	1k Chip Resistor	4	3Pin Header	1
Red LED	8	10k Chip Resistor	2	Test Point	10
Power Jack	1	50 Chip Resistor	6	LMC555CMX/NOPB	1

Circuit Diagram

A sketch of the schematic is shown in Fig. 1 and the actual schematic is shown in Fig. 2. A screenshot of the board layout is shown in Fig. 1. The fabricated board and the assembled board are shown in Fig. 3.

Measurement and Discussion

The frequency and duty cycle of the 555 timer is 504 Hz and 66% respectively as shown in Fig. 4. The rise and fall times are 45.6 ns and 27 ns respectively. The peak to peak voltage is about 5 volts as expected. The LDO output is expected to be 3.3 volts, but noise fluctuations can cause oscillations causing the output to vary. To prevent oscillations, a filtering capacitor is connected in parallel to the output of the LDO. Fig. 5 and Fig. 6 shows the LDO output with and without a

filtering capacitor. It is seen that the peak to peak voltage of the oscillations is about 170 mV but with a filtering capacitor, the output is constant at 3.256 volt

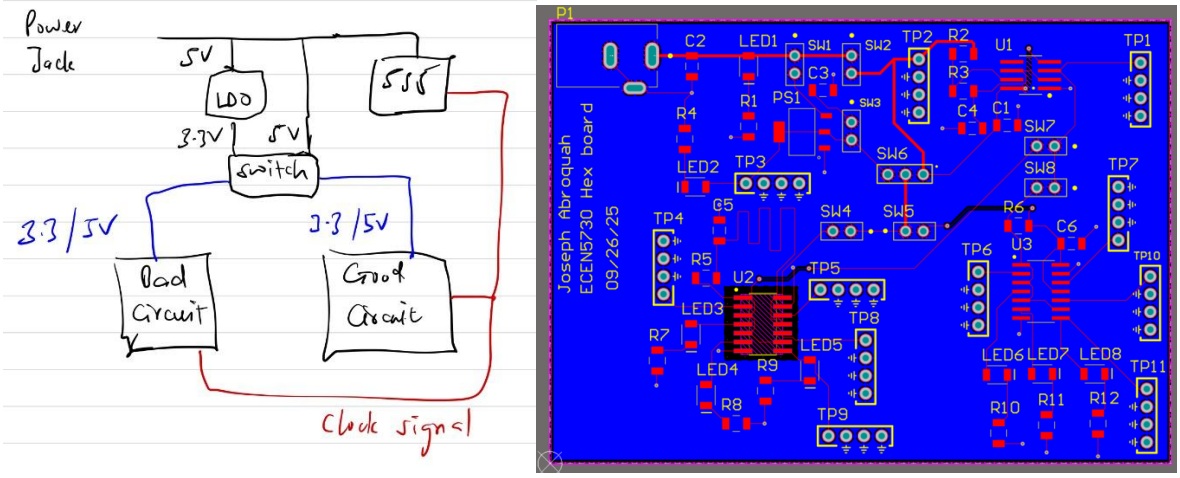

Fig. 1. Sketch of circuit (left) and layout of circuit (right)

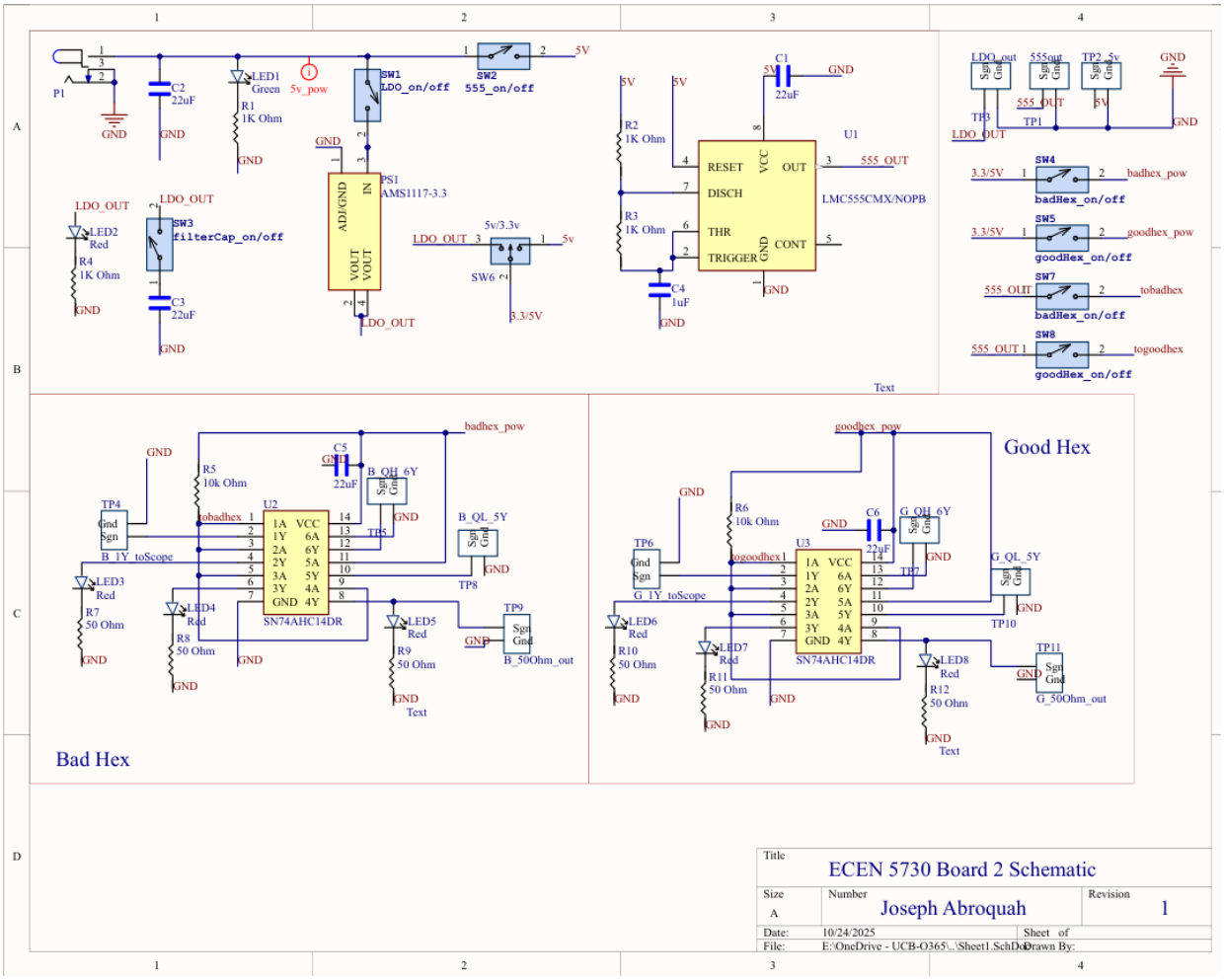

Fig. 2. Actual schematic of circuit

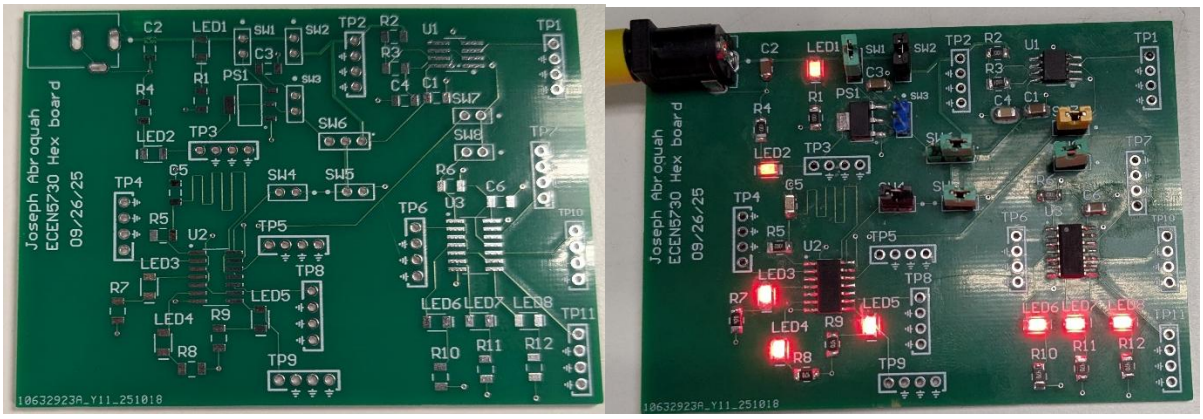

Fig. 3. Fabricated (unassembled) board on the left and assembled board on the right

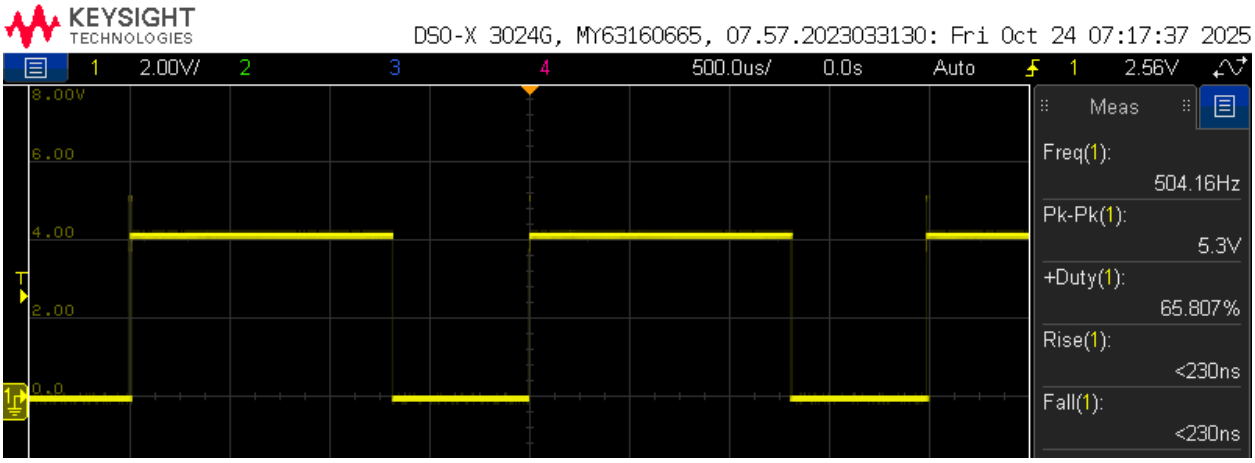

Fig. 4. Frequency and duty cycle of the 555 timer

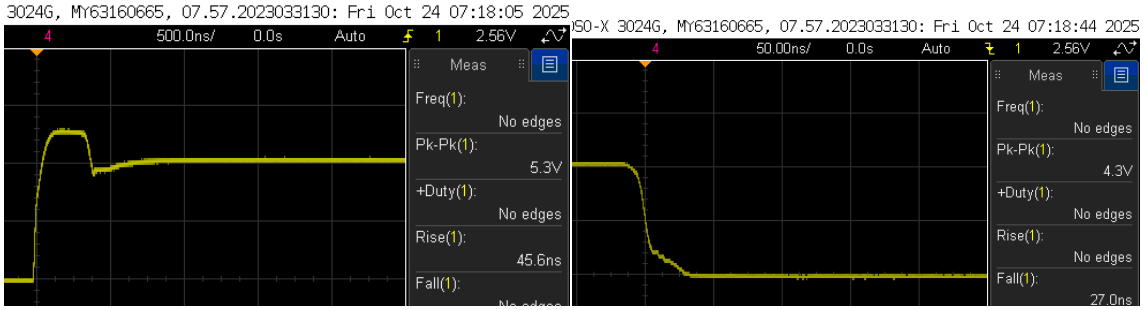

Fig. 5. Rise time and fall time of the timer

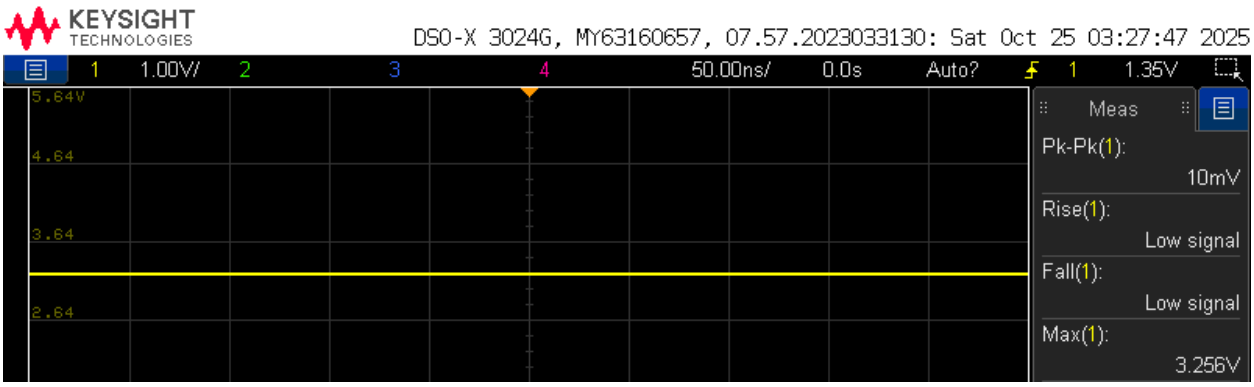

Fig. 6. LDO output with a filtering capacitor connected

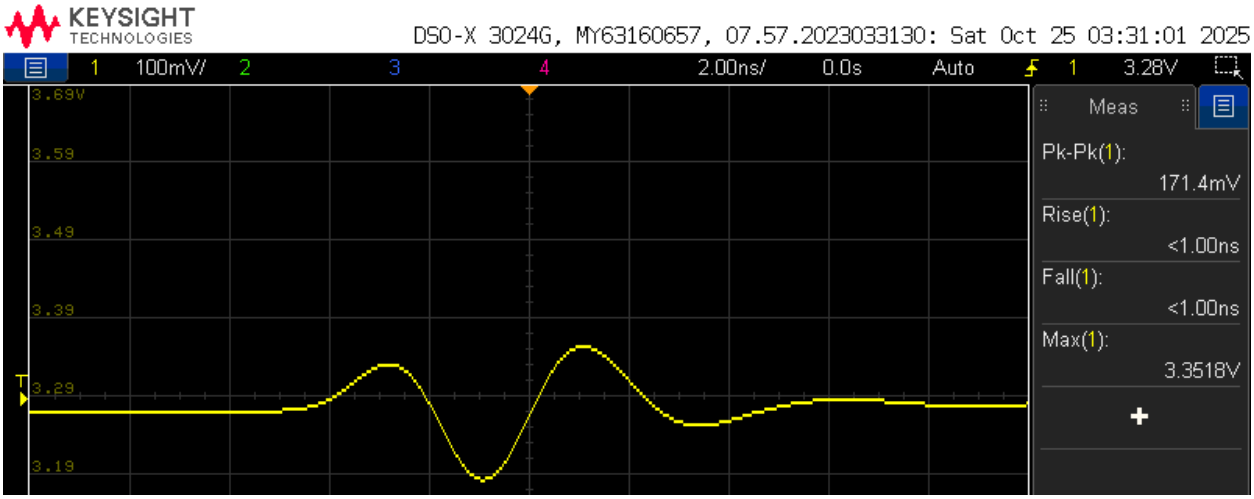

Fig. 7. LDO output without a filtering capacitor connected

The bad circuit shown at the lower left of the board in Fig. 3 has no ground plane under the IC and the decoupling capacitor is far from the VCC pin. On the other hand, the good circuit has continuous return plane and the decoupling capacitor is close to the IC's power pin. A comparison of the quiet high and quiet lows are shown in Fig. 8 and Fig. 9 respectively for a 5V power supply. Measured results show that the bad circuit (green trace) is noisy compared to the good circuit (blue trace), the peak to peak voltages for the quiet highs are 813mV for the good circuit and 1.863V for the bad circuit with respect to the rising edge of the trigger. Simiarly, peak to peak voltages for the quiet lows are 410mV and 447mV for the good and bad circuit respectively. Similar result is obtained for when the circuits are powered by 3V.

The rise and fall times of the bad and good circuits as well as the rail collapse are shown in Fig. 10 and Fig. 11. A comparison of measured values are presented in Table 1. It is seen that the rail collapse in the bad circuit is worse. Also, the rising and falling times are slower.

The output voltage across the resistors for the good and bad circuit is shown in Fig. 12. For the bad circuit, the current is approximately 65 mA and for the good about 63 mA.

Table 1: A comparison of peak to peak of bad and good circuit

	Bad	Good
P2P (v)	1.604	1.144
Rising Time (ns)	1.9711	1.607
P2P (mV)	1304	339
Falling Time (ns)	1.64	1.33

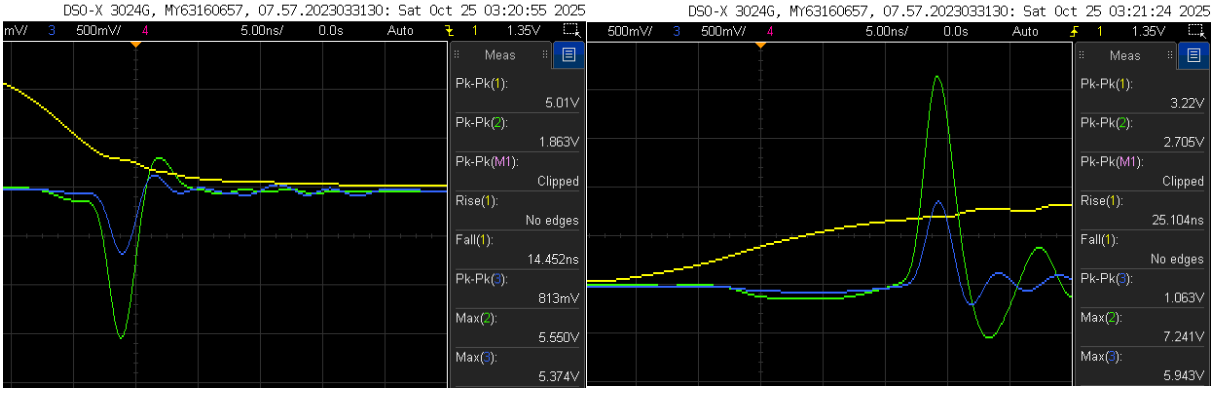

Fig. 8. A comparison of quiet highs of good (blue trace) and bad circuit (green trace) for a 5V power supply

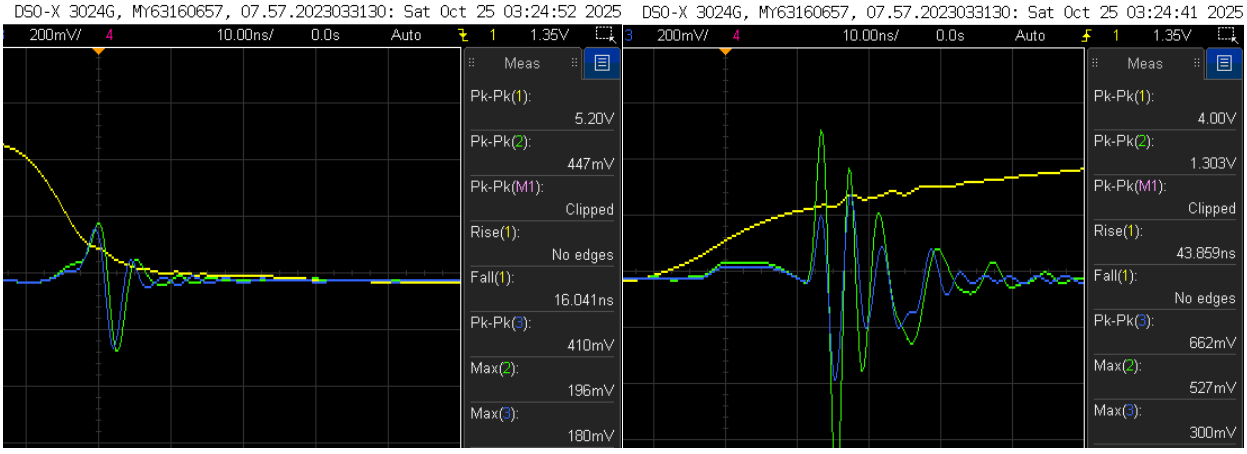

Fig. 9. A comparison of quiet lows of good (blue trace) and bad circuit (green trace) for a 5V power supply

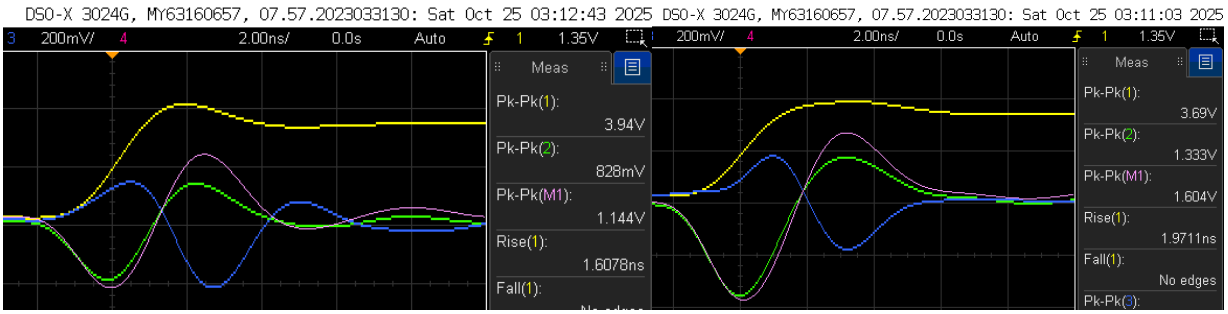

Fig. 10. Power rail comparison between good (left) and bad (right) circuit for rising edge

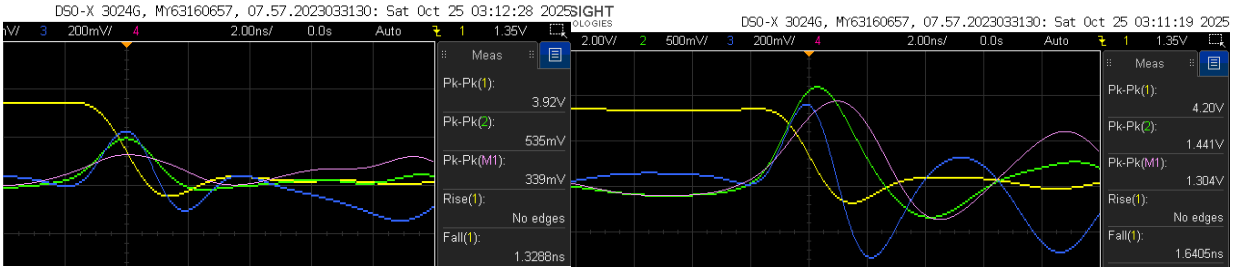

Fig. 11. Power rail comparison between good (left) and bad (bad) circuit for falling edge

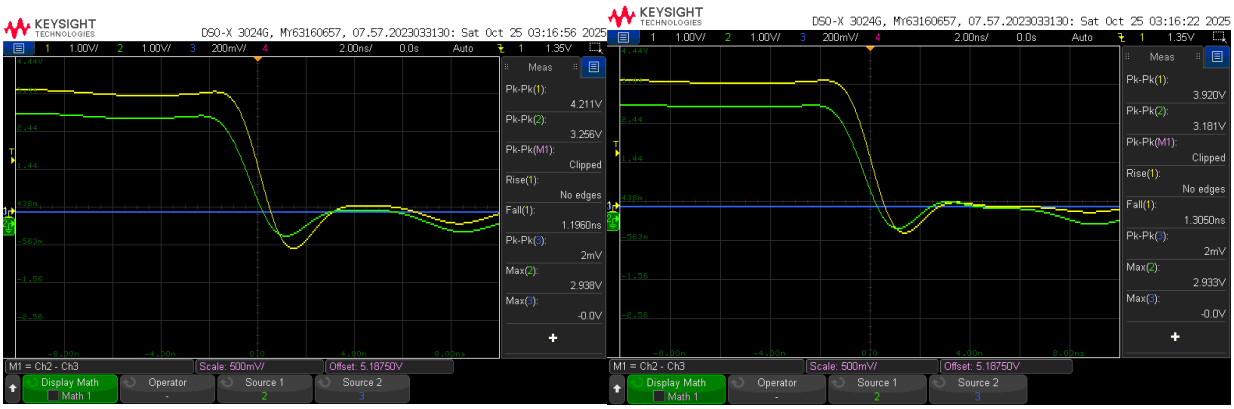

Fig. 12. Peak to Peak voltage across 50 Ω resistor (left is bad circuit, right is good circuit)

What worked

- The clock signal is about 500 Hz and about 50% duty cycle as expected
- LED polarity was considered before soldering blindly. This improved the soldering time compared to previous experience

What I did wrong and will improve in future designs

- I did not put texts to indicate what the test points are for. The switches too did not have any labels. This made debugging difficult

Conclusion

In this lab, two identical circuits but with different layout rules are compared to quantify the impacts of return plane and decoupling. Measured results indicate that identical circuit designs perform badly when good design practices are violated.